MP2348

High-Efficiency, 4A, 24V, 650kHz, Synchronous Step-Down Converter in SOT583 Package

DESCRIPTION

The MP2348 is a fully integrated, high-frequency, synchronous, rectified, step-down, switch-mode converter with internal power MOSFETs. It offers a compact solution to achieve 4A of continuous output current across a wide input range, with excellent load and line regulation. The MP2348 has synchronous mode operation for higher efficiency across the output current load range.

Constant-on-time (COT) control provides fast transient response and easy loop design, as well as tight output regulation.

Full protection features include short-circuit protection (SCP), over-current protection (OCP), under-voltage protection (UVP), and thermal shutdown.

The MP2348 requires a minimal number of readily available, standard external components, and is available in a space-saving SOT583 (1.6mmx2.1mm) package.

FEATURES

- Wide 4.2V-to-24V Operating Input Range
- 75mΩ/40mΩ Low $R_{DS(ON)}$ Internal Power MOSFETs
- 200µA Low I_Q
- High-Efficiency Synchronous Mode Operation
- Selectable Forced PWM, Auto-PFM/PWM and Ultrasonic Mode
- Fast Load Transient Response
- 650kHz Switching Frequency
- Configurable Soft-Start Time
- Over-Current Protection and Hiccup Mode
- Pre-Biased Start-Up
- Thermal Shutdown
- Available in an SOT583 (1.6mmx2.1mm) Package
- The MPL-AL6050 Inductor Series Matches Best Performance

APPLICATIONS

- Game Consoles
- Digital Set-Top Boxes
- Flat-Panel Televisions and Monitors
- General Purposes

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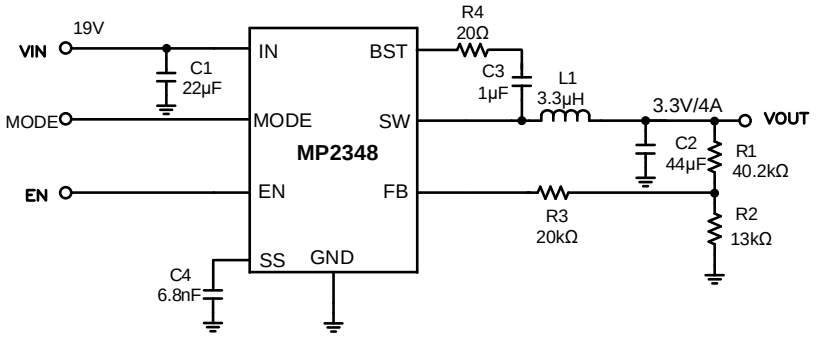
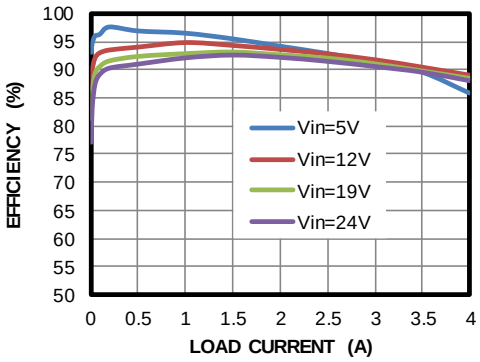
TYPICAL APPLICATION



Efficiency

PFM without USM, V_{OUT} = 3.3V,
L = 3.3µH, DCR = 11.7mΩ



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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP2348GTL	SOT583	*See Below*	1

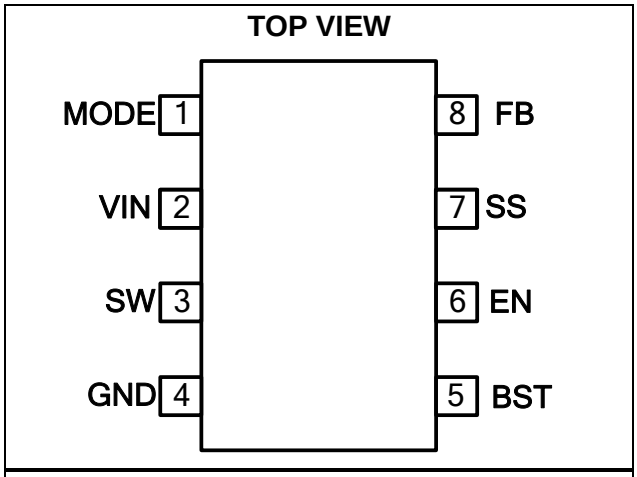
* For Tape & Reel, add suffix –Z (e.g. MP2348GTL–Z).

TOP MARKING

BHUY
LLL

BHU: Product code of MP2348GTL
Y: Year code
LLL: Lot number

PACKAGE REFERENCE



SOT583 (1.6mmx2.1mm)

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PIN FUNCTIONS

Pin #	Name	Description
1	MODE	**USM, PFM, and PWM mode selection**. For forced PWM mode, float MODE or pull it above 2.3V. For PFM mode with ultrasonic mode (USM) at light load, connect a 499kΩ resistor from MODE to GND. For PFM mode with USM, connect MODE directly to GND.
2	VIN	**Supply voltage.** The MP2348 operates from a 4.2V to 24V input rail. Use a capacitor (C1) to decouple the input rail. Connect using a wide PCB trace.
3	SW	**Switch output.** Connect using a wide PCB trace.
4	GND	**System ground.** Reference ground of the regulated output voltage. Requires additional consideration during PCB layout. Connect to GND with copper traces and vias.
5	BST	**Bootstrap.** Connect a capacitor and a resistor between the SW and BST pins to form a floating supply across the high-side switch driver. A 1µF BST capacitor is recommended.
6	EN	**Enable.** Pull EN high to enable the MP2348. For automatic start-up, connect EN to V_{IN} through a 604kΩ pull-up resistor.
7	SS	**Soft start.** Connect an external capacitor to program the soft-start time for the switch-mode regulator.
8	FB	**Feedback**. To set the output voltage, connect to the tap of an external resistor divider from the output to GND.

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ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} ..... -0.3V to +26V
V_{SW}…….-0.3V (-5V for <10ns, -0.6V for <2μs) to 26V (28V for <10ns)
V_{BST} .....V_{SW} + 4V
V_{EN} ..... -0.3V to +5V (2)
All other pins..... -0.3V to +4V
Continuous power dissipation (T_A = 25°C) (3)
……...2.2W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature..... -65°C to +150°C

ESD Rating

Human body model (HBM) .....±1800V
Charged device model (CDM).....±1500V

Recommended Operating Conditions (4)

Supply voltage (V_{IN}) ..... 4.2V to 24V
Output voltage (V_{OUT})….0.8V to 0.9 x V_{IN} to 13V
Operating junction temp (T_J)….-40°C to +125°C

Thermal Resistance

SOT583	θ_{JA}	θ_{JC}	
EV2348-TL-00A (5)	55	21	°C/W
JESD51-7 (6)	130	60	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) For details of EN pin's ABS MAX rating, see the Enable Control section on page X.
3) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation on EV2348 Board at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on EV2348-TL-00A, 2-layer PCB, 64mmx48mm.
6) The value of θ_{JA} given in this table is only valid for comparison with other packages, and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +125°C [7], typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply current (shutdown)	I_{IN}	V_{EN} = 0V			10	μA
Supply current (quiescent)	I_Q	V_{EN} = 2V, V_{FB} = 0.85V		200		μA
HS switch on resistance	HS_{RDS-ON}	V_{BST-SW} = 3.3V		75		mΩ
LS switch on resistance	LS_{RDS-ON}			40		mΩ
Switch leakage	SW_{LKG}	V_{EN} = 0V			1	μA
Low-side switching current limit during OCP	$I_{LIMIT_LS_OC}$		2.7	4		A
Low-side sink current limit	$I_{LIMIT_N_OC}$			-0.8		A
ZCD	I_{ZCD}			20		mA
Oscillator frequency	f_{SW}	V_{FB} = 0.75V, in CCM mode	485	650	815	kHz
Minimum on time [8]	t_{ON_MIN}			45		ns
Minimum off time [8]	t_{OFF_MIN}			190		ns
Feedback voltage	V_{REF}			802		mV
Feedback current	I_{FB}			10	50	nA
Hiccup duty cycle [8]				25		%
EN rising threshold	V_{EN_RISING}		1.16	1.23	1.29	V
EN hysteresis	V_{EN_HYS}			100		mV
EN input current	I_{EN}	V_{EN} = 2V		2		μA
		V_{EN} = 0V		0		
EN turn off delay time [9]	t_{DENL}			2		μS
VIN under-voltage lockout rising threshold	I_{NUVVth}			4		V
VIN under-voltage lockout hysteresis threshold	I_{NUVHYS}			330		mV

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +125°C [7], typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
PWM mode input logic low threshold	V_{MODE_H}		2.5			V
PFM with USM threshold	V_{MODE_MID}		0.8		2.5	V
PFM without USM threshold	V_{MODE_L}				0.8	V
Soft-start current	I_{SS}		5.3	7.3	9.3	μA
Thermal shutdown [8]				150		°C
Thermal hysteresis [8]				20		°C

Notes:

7) Not tested in production. Guaranteed by over-temperature correlation.
8) Guaranteed by design and engineering sample characterization.
9) Not tested in production.

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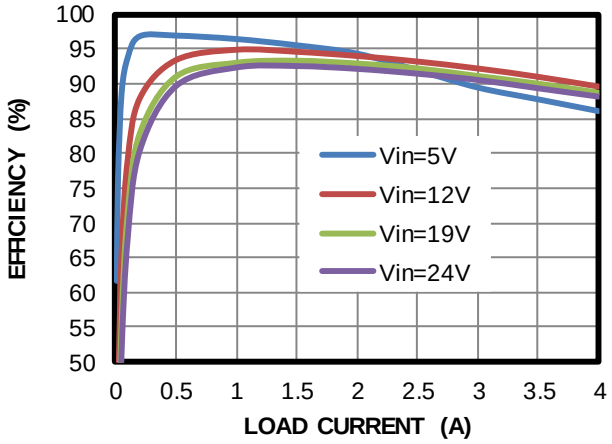
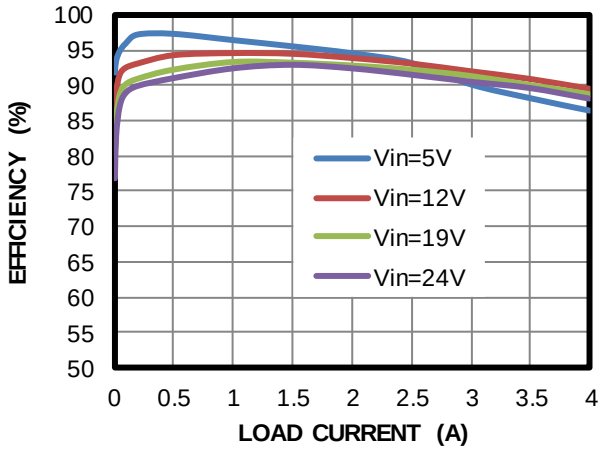
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 19V, V_{OUT} = 3.3V, L = 3.3µH, T_A = 25°C, unless otherwise noted.

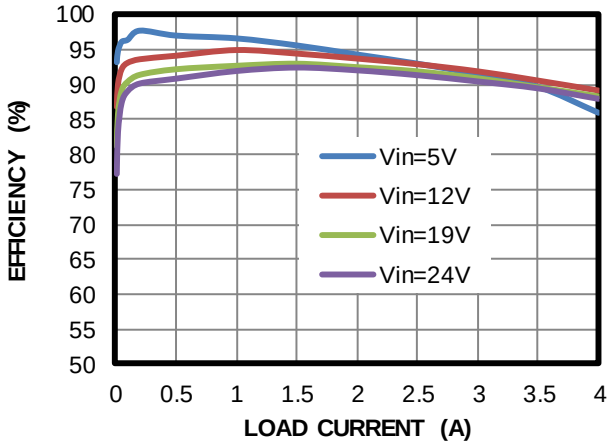
Efficiency
PWM, DCR = 11.7mΩ



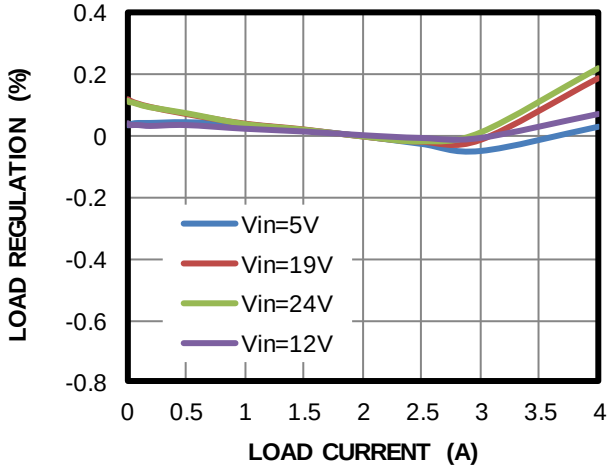
Efficiency
PFM with USM, DCR = 11.7mΩ



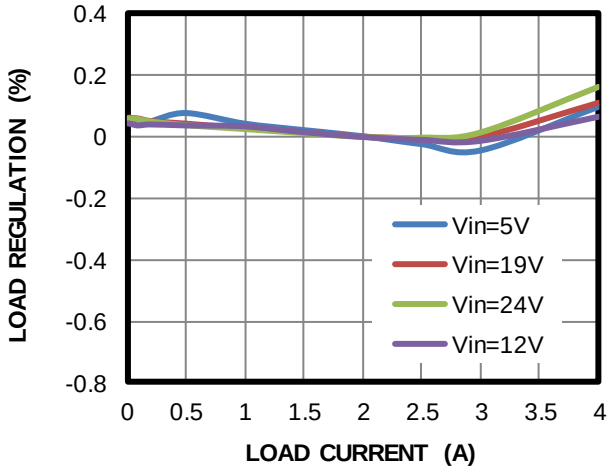
Efficiency
PFM without USM, DCR = 11.7mΩ



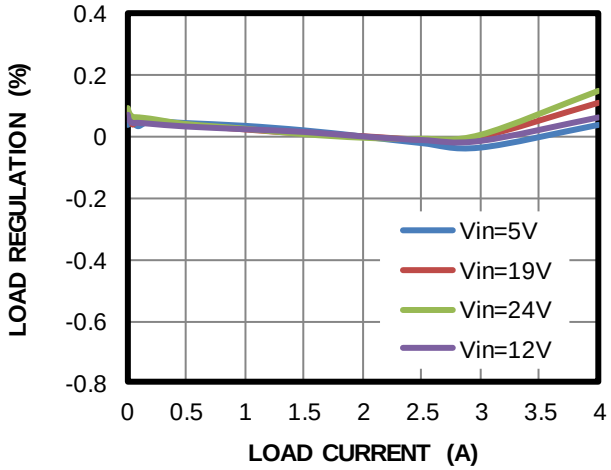
Load Regulation
PWM



Load Regulation
PFM with USM



Load Regulation
PFM without USM



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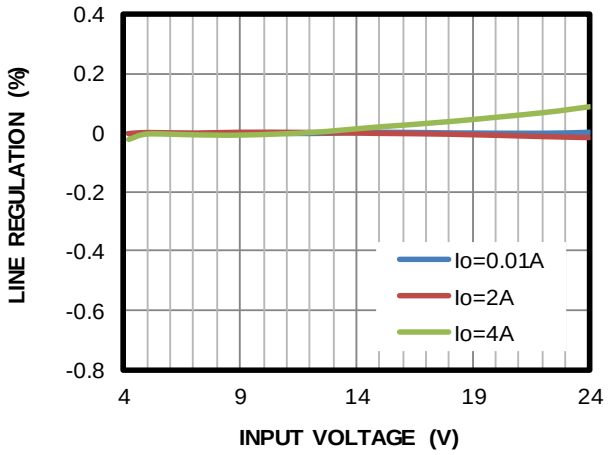
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 19V, V_{OUT} = 3.3V, L = 3.3µH, T_A = 25°C, unless otherwise noted.

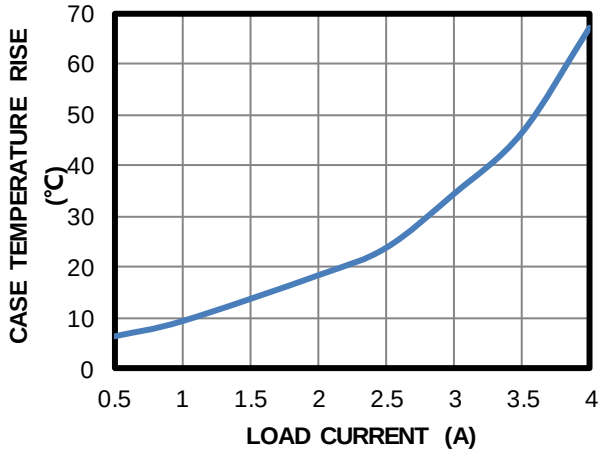
Line Regulation

V_{IN} = 4.2V to 24V



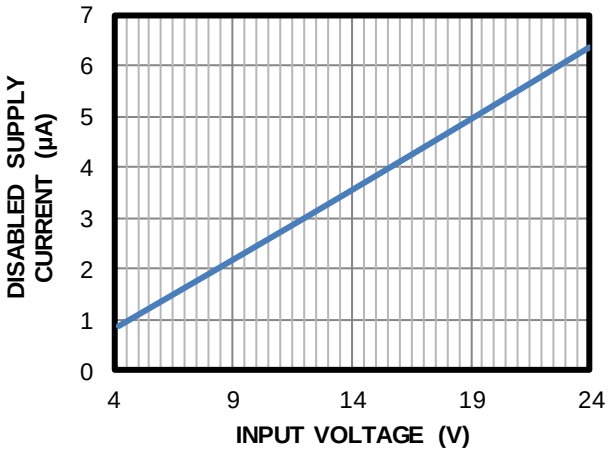
Case Temperature Rise vs. Load Current

I_{OUT} = 0.5A to 4A



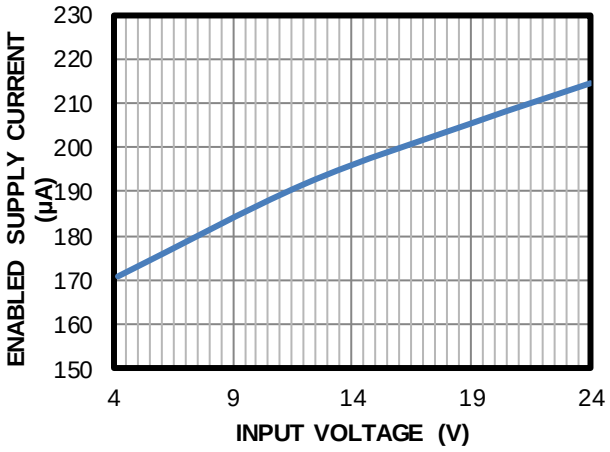
Disabled Supply Current vs. Input Voltage

V_{EN} = 0V

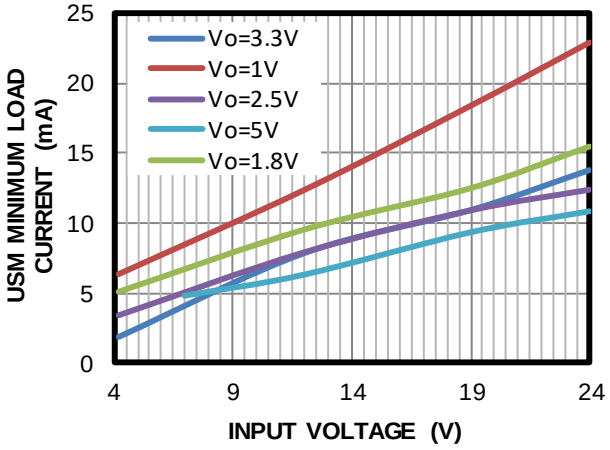


Enabled Supply Current vs. Input Voltage

V_{EN} = 2V, V_{FB} = 0.85V



USM Minimum Load Current vs. Input Voltage



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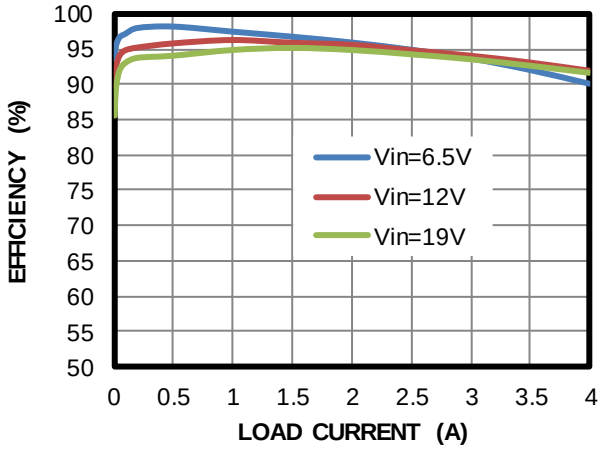
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 19V, V_{OUT} = 3.3V, L = 3.3µH, T_A = 25°C, unless otherwise noted.

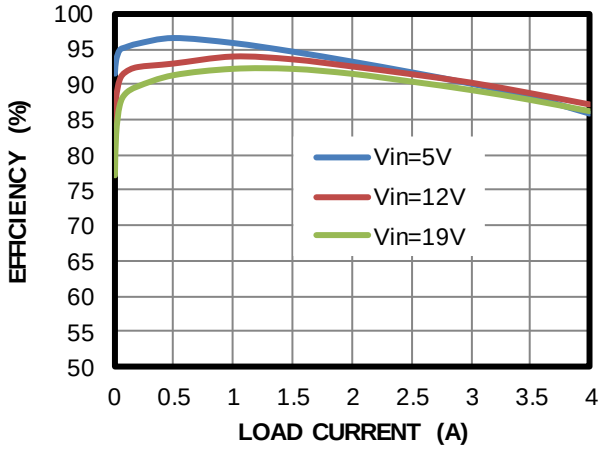
Efficiency

V_{OUT} = 5V, L = 4.7µH, DCR = 16.5mΩ



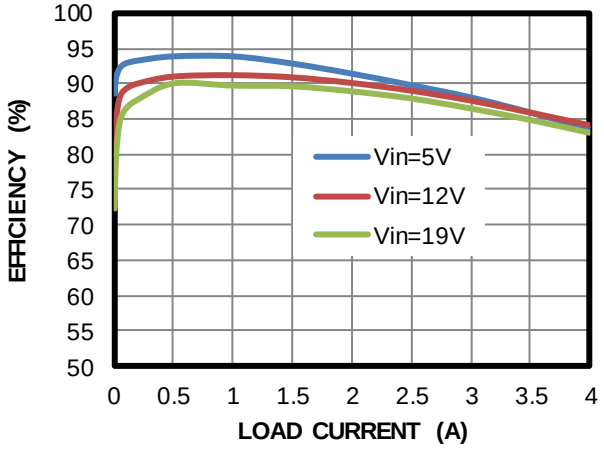
Efficiency

V_{OUT} = 2.5V, L = 3.3µH, DCR = 11.7MΩ



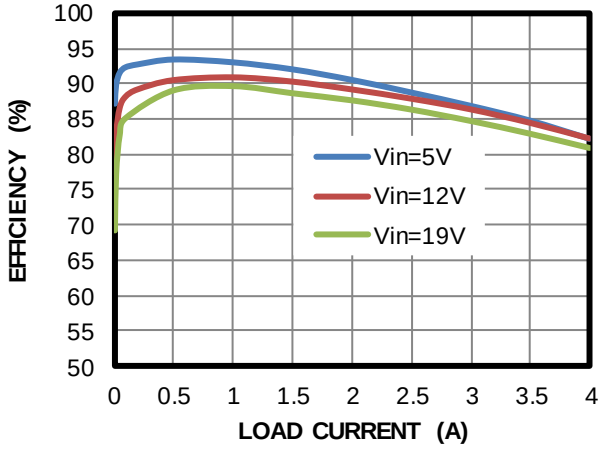
Efficiency

V_{OUT} = 1.8V, L = 2.2µH, DCR = 8.3mΩ



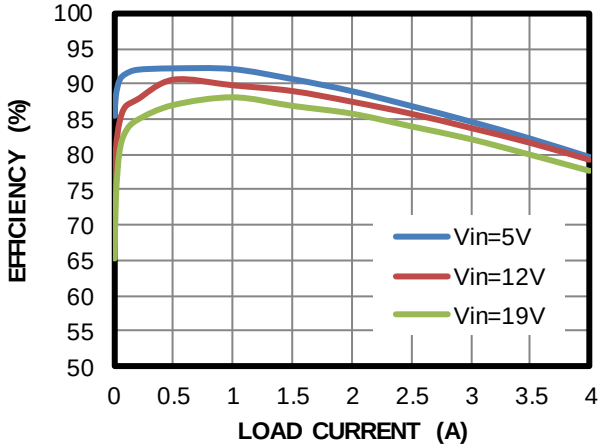
Efficiency

V_{OUT} = 1.5V, L = 2.2µH, DCR = 8.3mΩ



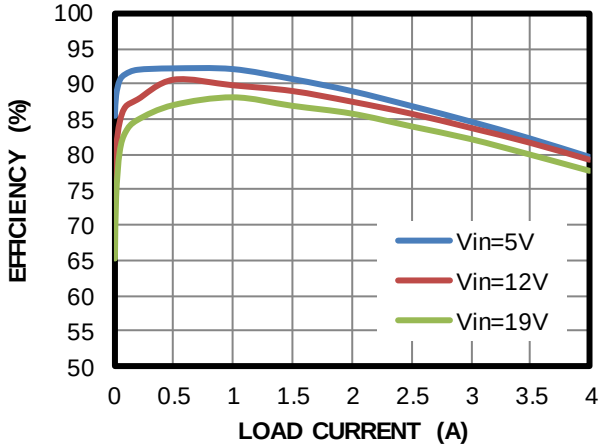
Efficiency

V_{OUT} = 1.2V, L = 1.5µH, DCR = 6mΩ



Efficiency

V_{OUT} = 1V, L = 1.5µH, DCR = 6mΩ



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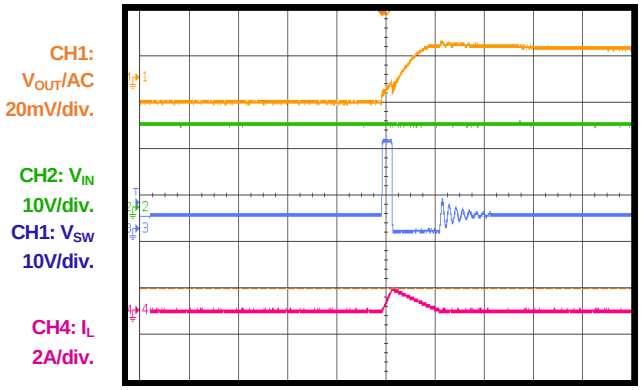
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 19V, V_{OUT} = 3.3V, L = 3.3μH, T_A = 25°C, unless otherwise noted.

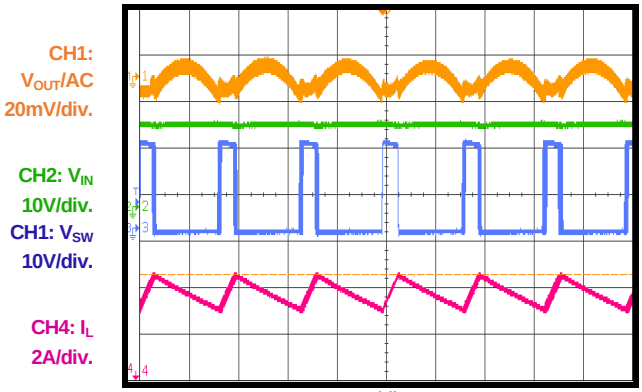
Input/Output Ripple

I_{OUT} = 0A, PFM



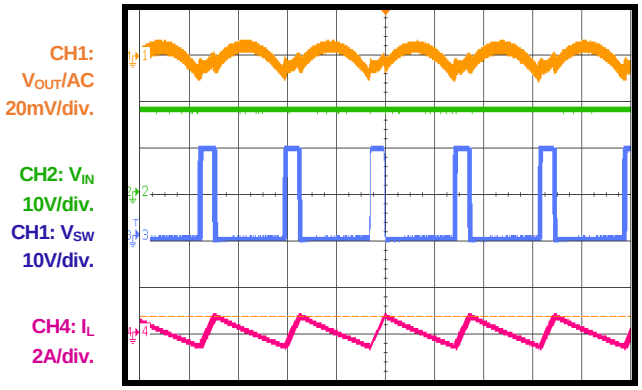
Input/Output Ripple

I_{OUT} = 4A



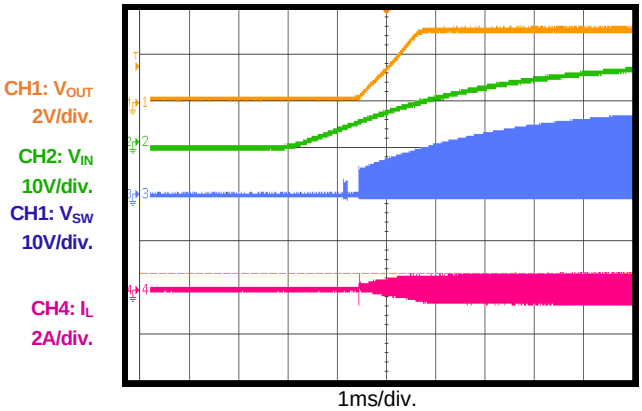
Input/Output Ripple

I_{OUT} = 0A, PWM



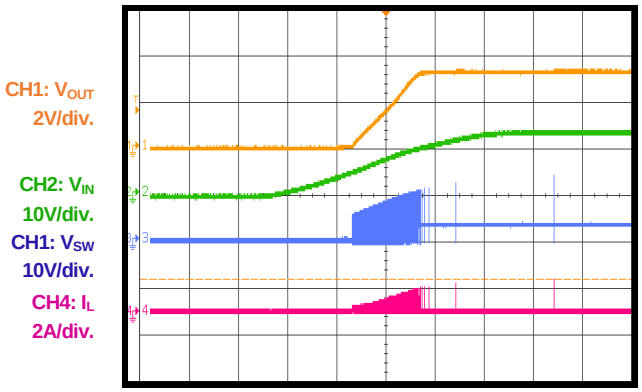
Start-Up through Input Voltage

I_{OUT} = 0A, PWM



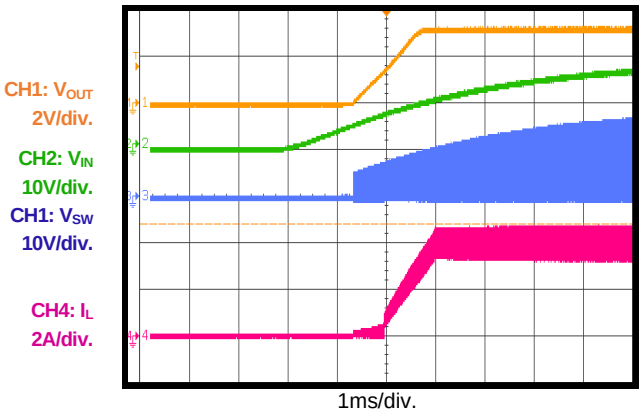
Start-Up through Input Voltage

I_{OUT} = 0A, PFM



Start-Up through Input Voltage

I_{OUT} = 4A



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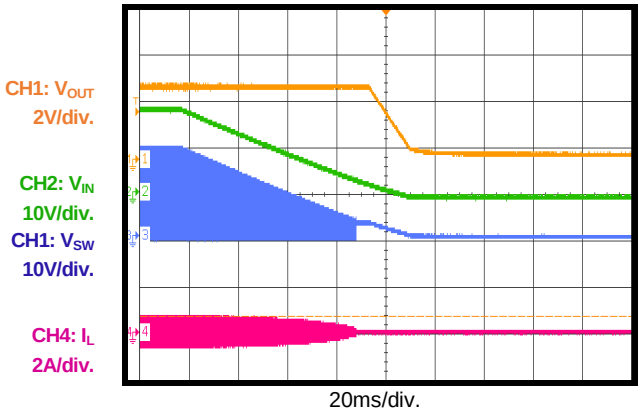
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 19V, V_{OUT} = 3.3V, L = 3.3μH, T_A = 25°C, unless otherwise noted.

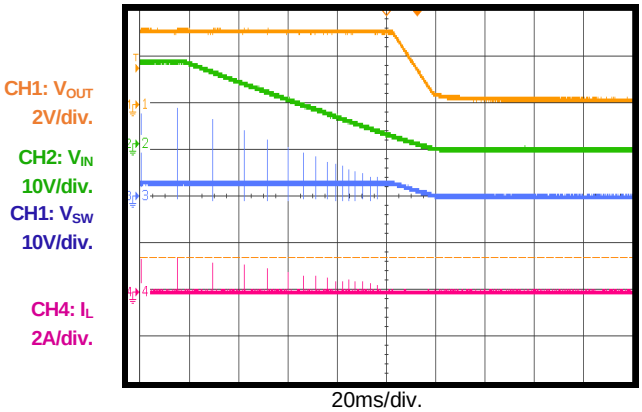
Shutdown through Input Voltage

I_{OUT} = 0A, PWM



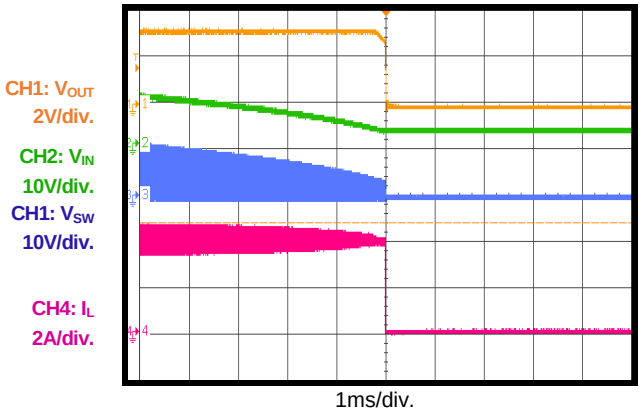
Shutdown through Input Voltage

I_{OUT} = 0A, PFM



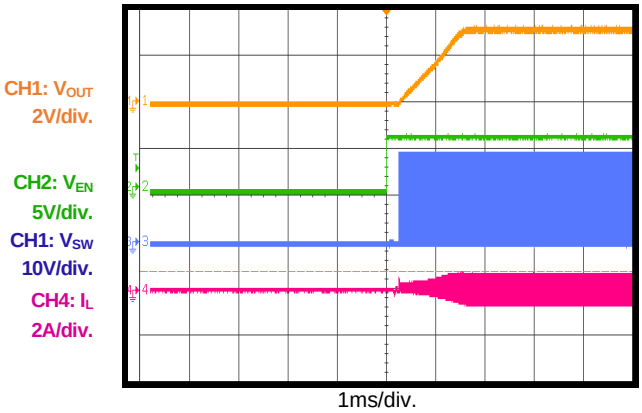
Shutdown through Input Voltage

I_{OUT} = 4A



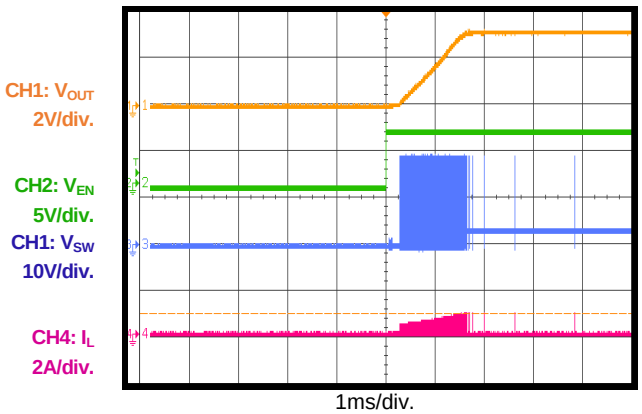
Start-Up through Enable

I_{OUT} = 0A, PWM



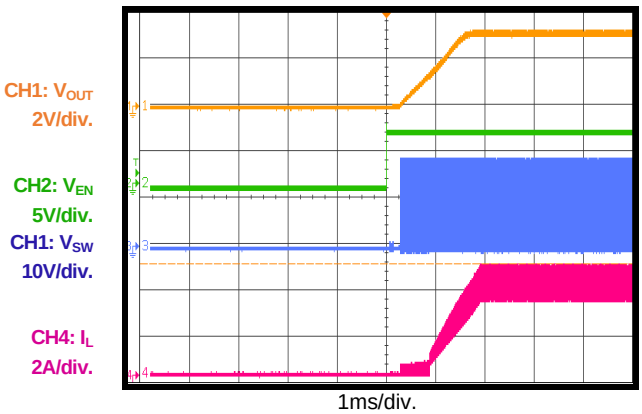
Start-Up through Enable

I_{OUT} = 0A, PFM



Start-Up through Enable

I_{OUT} = 4A



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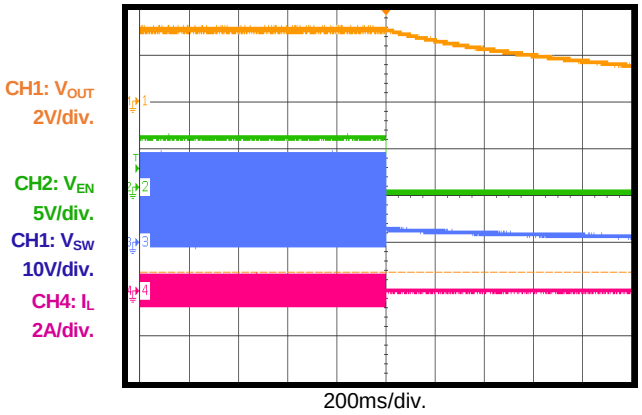
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 19V, V_{OUT} = 3.3V, L = 3.3μH, T_A = 25°C, unless otherwise noted.

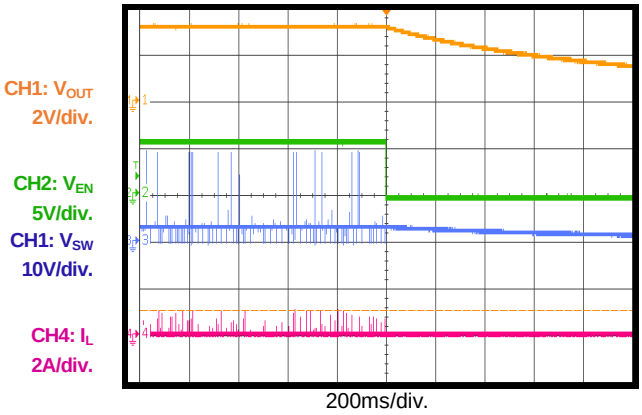
Shutdown through Enable

I_{OUT} = 0A, PWM



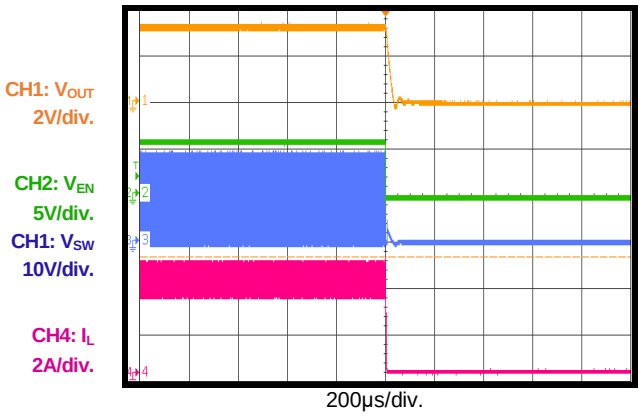
Shutdown through Enable

I_{OUT} = 0A, PFM

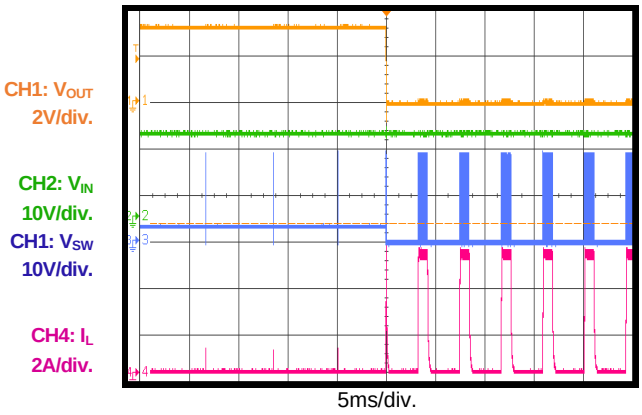


Shutdown through Enable

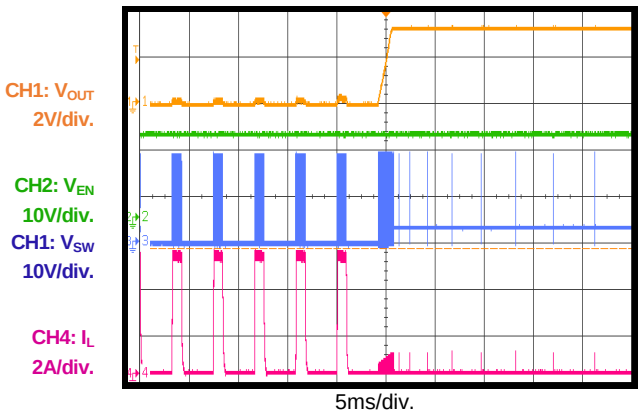
I_{OUT} = 4A



Short-Circuit Entry

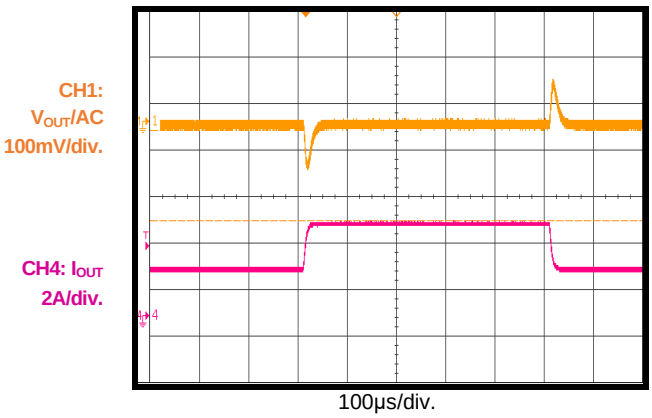


Short-Circuit Recovery



Load Transient

I_{OUT} = 2A to 4A



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FUNCTIONAL BLOCK DIAGRAM

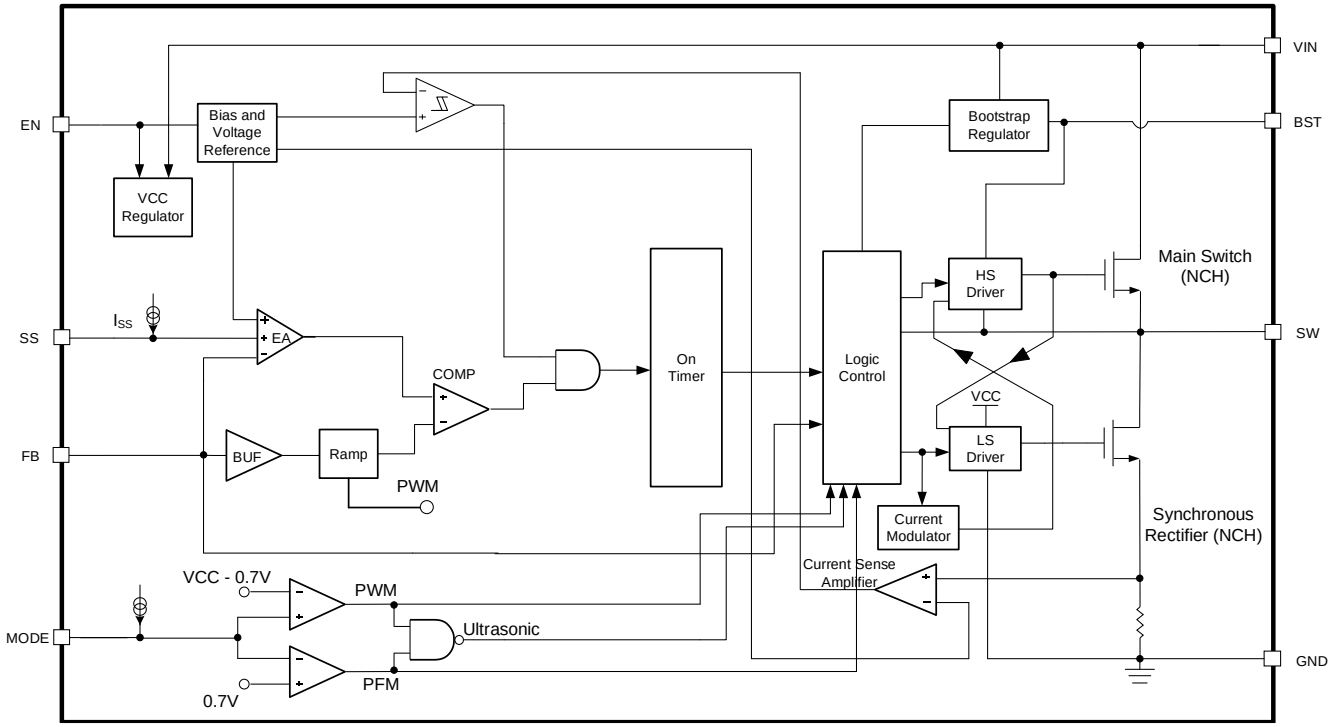

Figure 1: Functional Block Diagram

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OPERATION

The MP2348 is a fully integrated, synchronous, rectified, step-down, switch-mode converter. Constant-on-time (COT) control is employed to provide fast transient response and ease loop stabilization.

At the beginning of each cycle, the high-side MOSFET (HS-FET) turns on when the feedback voltage (V_{FB}) drops below the reference voltage (V_{REF}). The HS-FET turns on for a fixed interval determined by the one-shot on timer. The on timer is determined by both the output voltage and input voltage to ensure the switching frequency remains constant across the input voltage range. After the on period elapses, the HS-FET turns off until the next period begins. By repeating this operation, the converter regulates the output voltage.

Continuous conduction mode (CCM) occurs when the output current is high and the inductor current is above 0A. The low-side MOSFET (LS-FET) turns on when the HS-FET is off to minimize conduction loss. A dead short occurs between the input and GND if both the HS-FET and LS-FET are turned on at the same time; this is called shoot-through. To prevent shoot-through, a dead time is generated internally between the time when the HS-FET is off and the LS-FET is on, and vice versa.

When the MP2348 works in pulse-frequency modulation (PFM) mode during light-load operation, the device automatically reduces the switching frequency to maintain high efficiency, and the inductor current drops almost to zero. When the inductor current reaches zero, the low-side driver enters tri-state (Hi-Z). The output capacitors discharge slowly to GND through resistors R1 and R2. When V_{FB} drops below V_{REF}, the HS-FET turns on. This operation greatly improves device efficiency when the output current is low.

Light-load operation is also called skip mode because the HS-FET does not turn on as frequently as it does under heavy-load conditions. The frequency at which the HS-FET turns on is a function of the output current. As the output current increases, the current modulator regulates over a shorter period, and the HS-FET turns on more frequently. This causes the switching frequency to increase. The output current reaches critical levels when the current modulator time is zero, calculated with Equation (1):

$$I_{OUT} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times f_{SW} \times V_{IN}} \quad (1)$$

The MP2348 reverts to PWM mode once the output current exceeds the critical level. Afterward, the switching frequency remains fairly constant over the output current range.

Light-Load Ultrasonic Mode (USM)

Ultrasonic mode (USM) maintains the switching frequency above audible frequency areas during light-load conditions. Once the device goes into light-load, the on time (t_{ON}) shrinks to ensure the IC's switching frequency does not drop below 20kHz.

If the load current drops below the USM minimum load threshold, the IC's switching frequency falls below 20kHz. A dummy load is required if the load current drops below the USM minimum load (see the USM Minimum Load Current vs. Input Current curve in the Typical Performance Characteristics TPC section on page 8).

Enable (EN) Control

EN is a digital control pin that turns the regulator on and off. Drive EN high to turn the regulator on; drive it low to turn the device off.

EN is clamped internally using a 2.8V series Zener diode (see Figure 2). Connect the EN input through a pull-up resistor to VIN to limit the EN input current below 40µA. This helps prevent damage to the Zener diode. For example, when connecting a 604kΩ pull-up resistor to 12V VIN:

$$I_{Zener} = (12V - 2.8V) / (604k\Omega + 35k\Omega) = 14\mu A$$

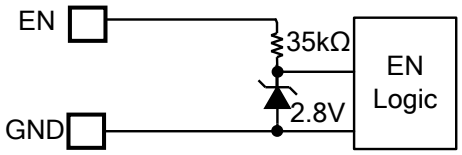

Figure 2: Zener Diode between EN and GND

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Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The MP2348 UVLO comparator monitors the output voltage of the internal regulator (VCC). The UVLO rising threshold is about 4V, while its falling threshold is 3.67V.

Soft Start (SS)

The MP2348 employs a soft start (SS) mechanism to ensure the output ramps smoothly during start-up. When the part starts, an internal current source (about 7.3μA) charges up the SS capacitor to generate a soft-start voltage (V_{SS}). When V_{SS} / 2 is below V_{REF}, V_{SS} / 2 overrides V_{REF}. The error amplifier uses V_{SS} / 2 as the reference, and the output voltage smoothly ramps up. Once V_{SS} / 2 rises above V_{REF}, the error amplifier uses V_{REF} as the reference. At this point, soft start finishes, and the part enters steady state operation.

The SS capacitor value can be calculated with Equation (2):

$$C_{SS}(nF) = \frac{t_{SS}(ms) \times I_{SS}(uA)}{2V_{REF}} \quad (2)$$

Over-Current Protection (OCP) and Short-Circuit Protection (SCP)

The MP2348 has valley limit control. When the low-side MOSFET (LS-FET) is on, the inductor current is monitored. If the sensed inductor current reaches the valley current limit, the LS limit comparator turns over (see Figure 1). Then the device enters over-current protection (OCP) mode, and the high-side MOSFET (HS-FET) remains off until sensed inductor current falls below the valley current limit. Meanwhile, the output voltage drops until the feedback voltage (V_{FB}) falls below the under-voltage (UV) threshold. Once UV is triggered, the MP2348 enters hiccup mode to periodically restart the part.

During OCP, the device tries to recover from the over-current fault with hiccup mode. In hiccup mode, the chip disables the output power stage, discharges the soft start, and then automatically tries to soft start again. If the over-current condition remains after soft start finishes, the device repeats this operation cycle until the over-current condition disappears, and the output rises back to regulation level. OCP is a non-latch protection.

Mode Selection

Float MODE or pull it above 2.3V to operate in forced PWM mode. Connect a 499kΩ resistor from MODE to GND to operate in PFM mode with ultrasonic mode (USM) under light-load conditions. Connect MODE to ground to operate in PFM mode without USM.

Pre-Biased Start-Up

The MP2348 is designed for monotonic start-up into pre-biased loads. If the output is pre-biased to a certain voltage during start-up, the BST voltage is refreshed and charged, as well as the soft-start voltage. If the BST voltage exceeds its rising threshold voltage, and V_{SS} / 2 exceeds the sensed output voltage at the FB pin, the part enters normal operation.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 150°C, the whole chip shuts down. When the temperature falls below its lower threshold (typically 130°C), the chip is enabled again.

Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own UVLO protection, with a rising threshold of 2.2V and a hysteresis of 150mV. VIN regulates the bootstrap capacitor voltage internally through D1, M1, R4, C3, L1, and C2 (see Figure 3). If (V_{IN} - V_{SW}) exceeds 3.3V, U2 regulates M1 to maintain a 3.3V BST voltage across C3.

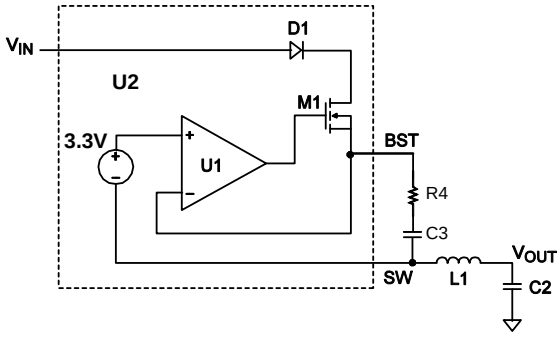

Figure 3: Internal Bootstrap Charger

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Start-Up and Shutdown

If both VIN and EN exceed their respective thresholds, the chip starts. The reference block starts first by generating a stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuits.

Three events can shut down the chip: EN going low, VIN going low, and thermal shutdown. The shutdown procedure starts by initially blocking the signaling path to avoid any fault triggering, then the internal supply rail is pulled down.

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APPLICATION INFORMATION

COMPONENT SELECTION

Setting the Output Voltage

The external resistor divider sets the output voltage. First, choose an appropriate value for R2. A small R2 leads to considerable quiescent current loss, while a large R2 makes FB noise sensitive. Then R1 can be estimated with Equation (3):

$$R1 = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R2 \qquad (3)$$

Figure 4 shows the feedback circuit.

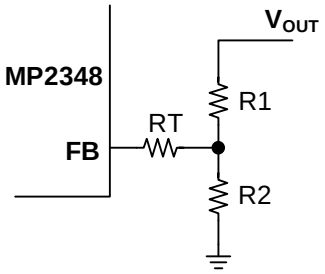

Figure 4: Feedback Network

Table 1 and Table 2 list the recommended parameters for common output voltages.

Table 1: Parameter Selection for Common Output Voltages when V_{IN} = 19V (9)

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	RT (kΩ)	L (μH)
1.0	33	133	120	1.5
1.2	40.2	82	75	1.5
1.5	40.2	45.3	47	2.2
1.8	40.2	32.4	36	2.2
2.5	40.2	19.1	24	3.3
3.3	40.2	13	20	3.3
5	40.2	7.68	15	4.7

Note:

9) Different output inductor values and output capacitor values may affect the selection of R1, R2, and RT. For additional component parameters, see the Typical Application Circuits.

Table 2: Parameter Selection for Common Output Voltages When V_{IN} = 5V

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	RT (kΩ)	L (μH)
1.0	33	133	120	1.5
1.2	40.2	82	75	1.5
1.5	40.2	45.3	47	2.2
1.8	40.2	32.4	36	2.2
2.5	40.2	19.1	24	2.2
3.3	40.2	13	30	1.5
5 (10)	40.2	7.68	15	2.2

Note:

10) For VOUT = 5V, VIN should be no lower than 6.5V.

Selecting the Inductor

The inductor must supply a constant current to the output load while being driven by the switched input voltage. A larger-value inductor results in less ripple current and lower output ripple voltage. However, a larger-value inductor will have a larger physical size, higher series resistance, and lower saturation current.

A good rule to determine the inductance value is to design the peak-to-peak ripple current in the inductor to be between 30% and 60% of the maximum output current, and ensure the peak inductor current is below the maximum switch current limit. The inductance value can be calculated with Equation (4):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \qquad (4)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

The inductor should not saturate under the maximum inductor peak current. The peak inductor current can be estimated with Equation (5):

$$I_{LP} = I_{OUT} + \frac{V_{OUT}}{2 f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \qquad (5)$$

MPS inductors are optimized and tested to be used with our complete line of integrated circuits.

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Table 3 lists recommended power inductors. Part numbers should be selected based on design requirements.

Table 3: Power Inductor Selection

Part Number	Inductor Value	Manufacturer
Select family series (MPL-AL)	1.5µH to 4.7µH	MPS
MPL-AL6050-1R5	1.5µH	MPS
MPL-AL6050-2R2	2.2µH	MPS
MPL-AL6050-3R3	3.3µH	MPS
MPL-AL6050-4R7	4.7µH	MPS

For additional information, visit the MPS website.

Selecting the Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply the AC current to the converter while maintaining the DC input voltage. Ceramic capacitors are recommended for optimal performance, and should be placed as close to the VIN pin as possible. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are fairly stable amid temperature fluctuations.

The capacitors must also have a ripple current rating greater than the maximum input ripple current of the converter. The input ripple current can be estimated with Equation (6):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (6)$$

The worst-case condition occurs when V_{IN} = $2V_{OUT}$, calculated with Equation (7):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (7)$$

For simplification, choose the input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitance value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose an input capacitor that meets the specification.

The input voltage ripple can be estimated with Equation (8):

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (8)$$

The worst-case condition occurs when V_{IN} = $2V_{OUT}$, calculated with Equation (9):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{f_{SW} \times C_{IN}} \quad (9)$$

Selecting the Output Capacitor

The output capacitor must maintain the DC output voltage. Ceramic or POSCAP capacitors are recommended. The output voltage ripple can be estimated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \quad (10)$$

With ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes most of the output voltage. For simplification, the output voltage ripple can be estimated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^{2} \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (11)$$

The output voltage ripple caused by ESR is very small. With POSCAP capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be calculated with Equation (12):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (12)$$

Besides the output ripple, a larger output capacitor also can improve load transient response, but the maximum output capacitor limit should be considered when designing the application. If the output capacitance is too high, the output voltage cannot reach the design value during the soft-start time and the device will fail to regulate. The maximum output capacitor value (C_{O_MAX}) can be estimated with Equation (13):

$$C_{O_MAX} = (I_{LIM_AVG} - I_{OUT}) \times t_{SS} / V_{OUT} \quad (13)$$

Where I_{LIM_AVG} is the average start-up current during soft start, and t_{ss} is the soft-start time.

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Design Example

Table 4 shows a design example using ceramic capacitors.

Table 4: Design Example

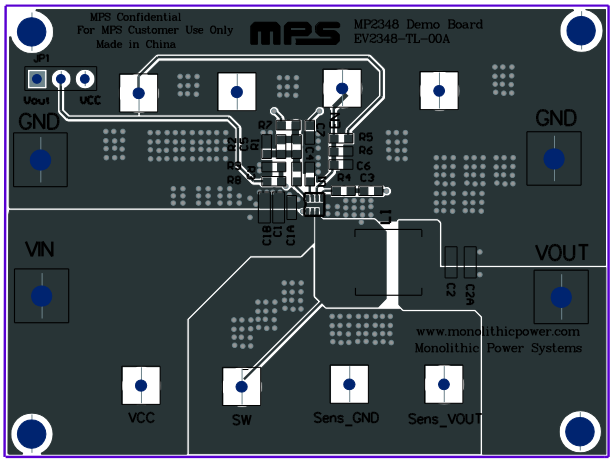
V_{IN}	19V
V_{OUT}	3.3 V
I_{OUT}	4A

See Figure 6 for a detailed application schematic. For the typical performance and waveforms, see the Typical Characteristics section on page 7. For additional device applications, refer to the related evaluation board datasheet.

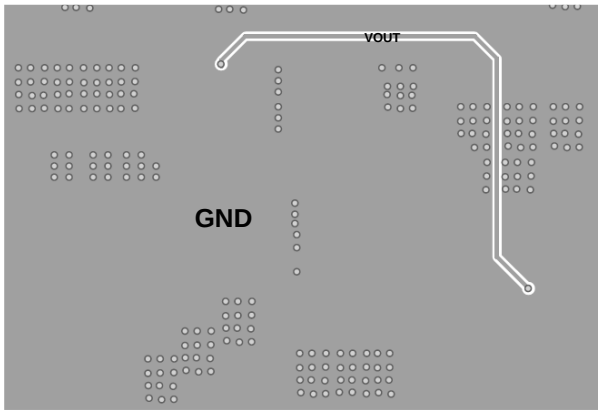
PCB Layout Guidelines

Proper PCB layout is critical for stable operation. Suboptimal layout design can result in poor line or load regulation and stability issues. For the best results, refer to Figure 5 and follow the guidelines below:

1. Place the high-current paths (GND, VIN, and SW) as close to the device as possible with short, direct, and wide traces.
2. Place the input capacitor as close to IN and GND as possible (recommended within 1mm).
3. Place the external feedback resistors next to FB.
4. Keep the switching node (SW) short and route it away from the feedback network.



Top Layer



Bottom Layer

Figure 5: Recommended PCB Layout

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TYPICAL APPLICATION CIRCUITS

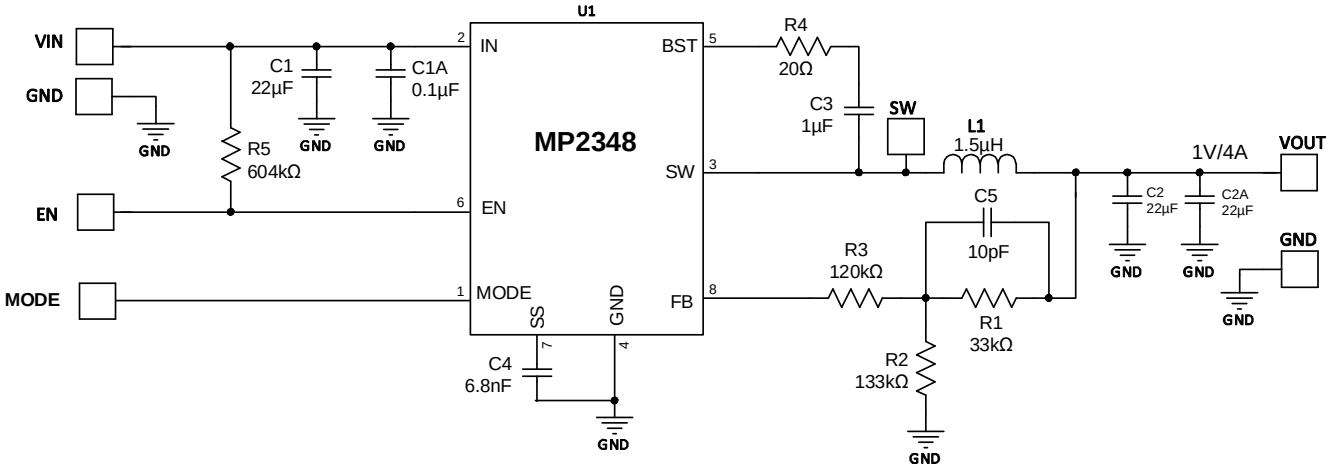

Figure 6: V_{OUT} = 1V

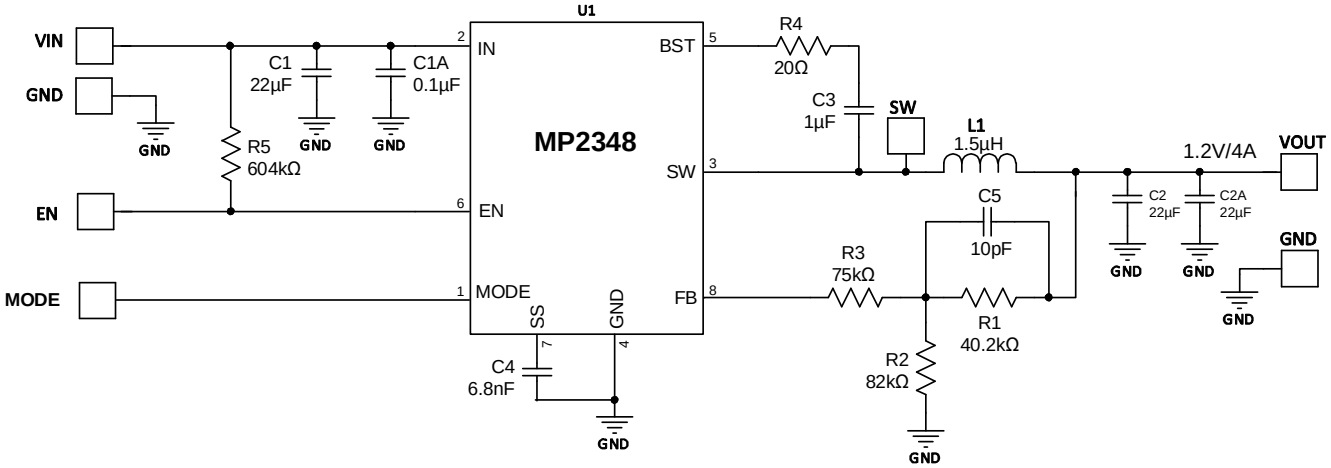

Figure 7: V_{OUT} = 1.2V

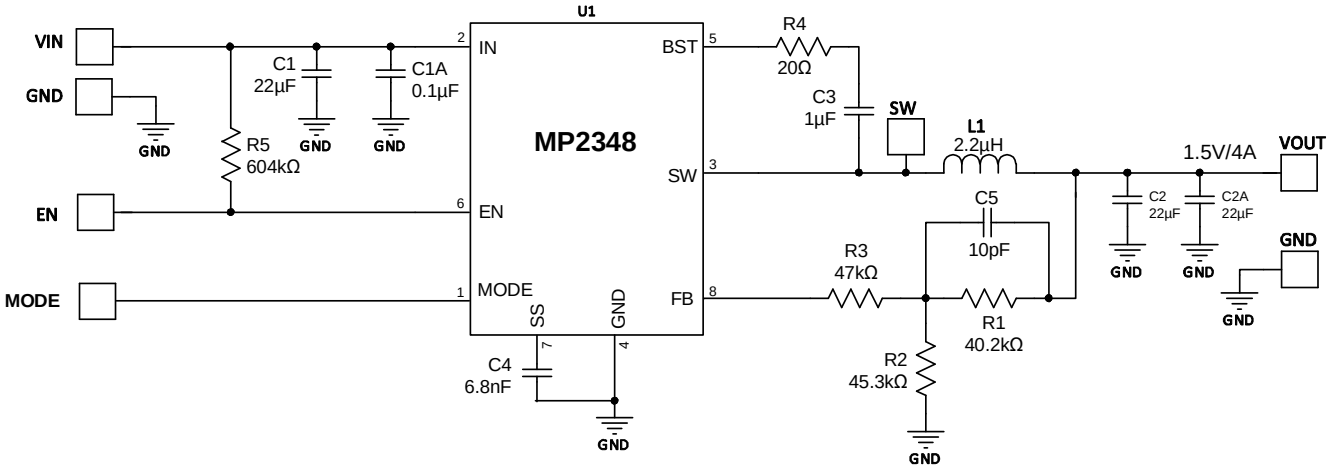

Figure 8: V_{OUT} = 1.5V

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TYPICAL APPLICATION CIRCUITS *(continued)*

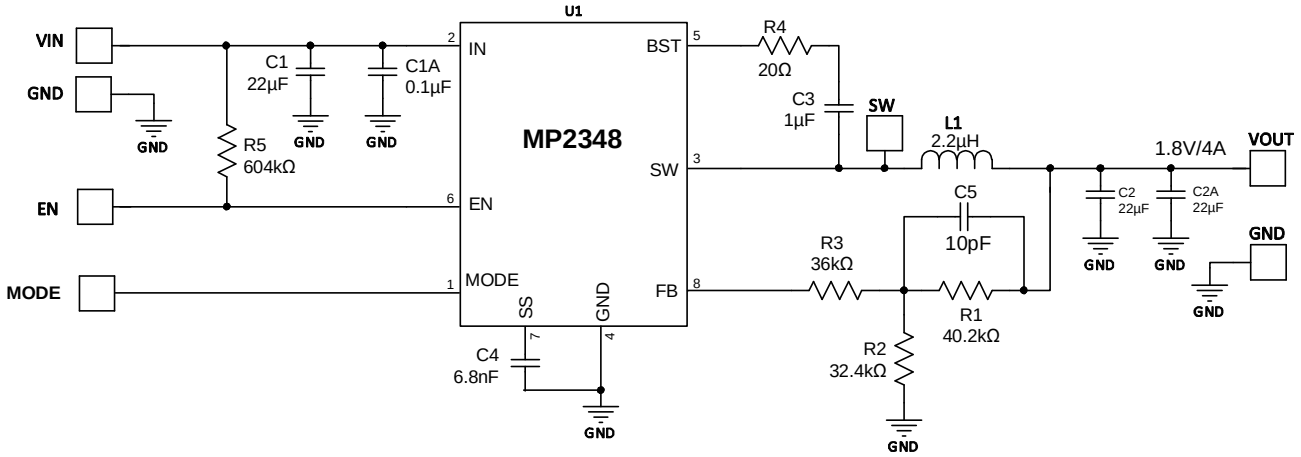

Figure 9: V_{OUT} = 1.8V

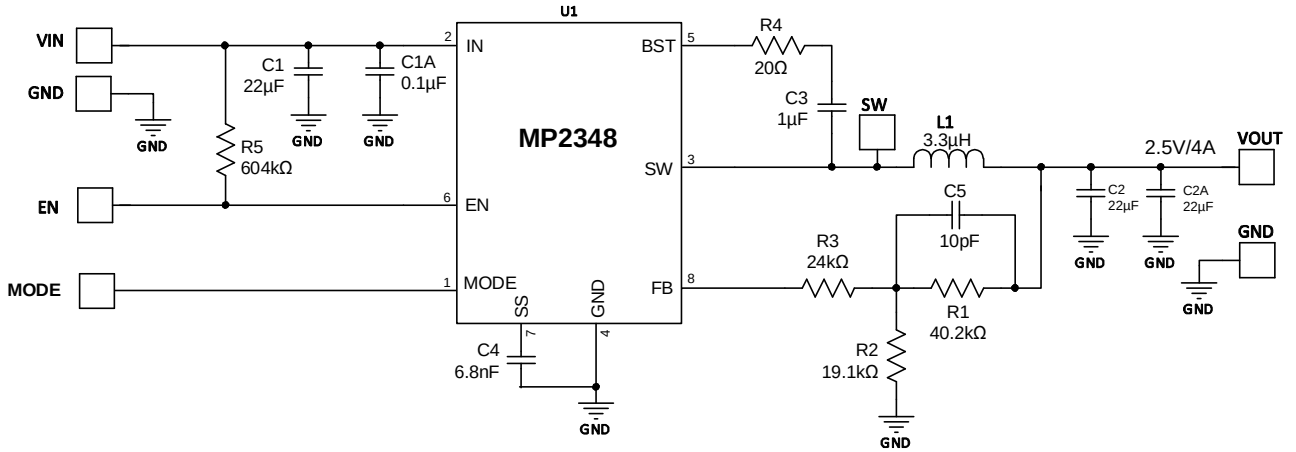

Figure 10: V_{OUT} = 2.5V

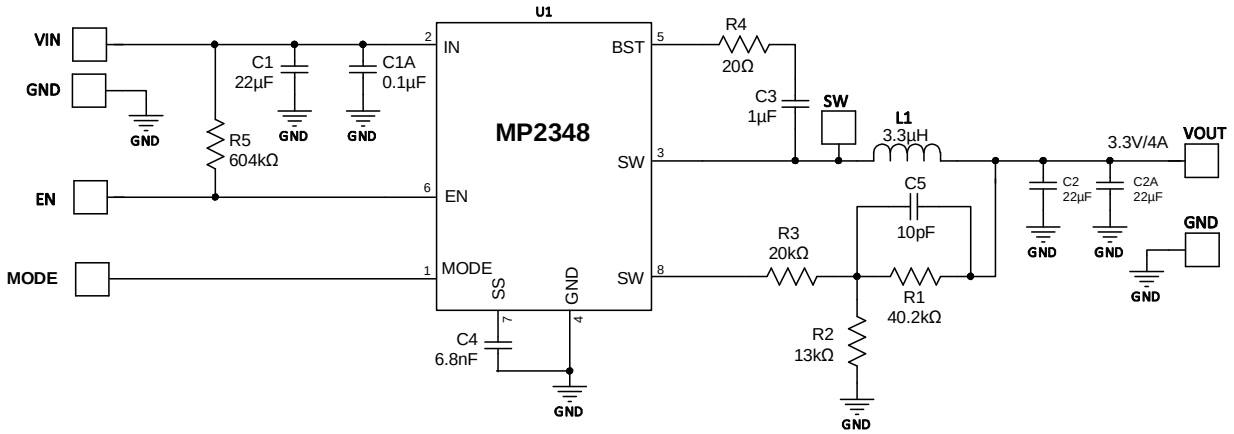

Figure 11: V_{IN} = 19V, V_{OUT} = 3.3V/4A

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TYPICAL APPLICATION CIRCUITS *(continued)*

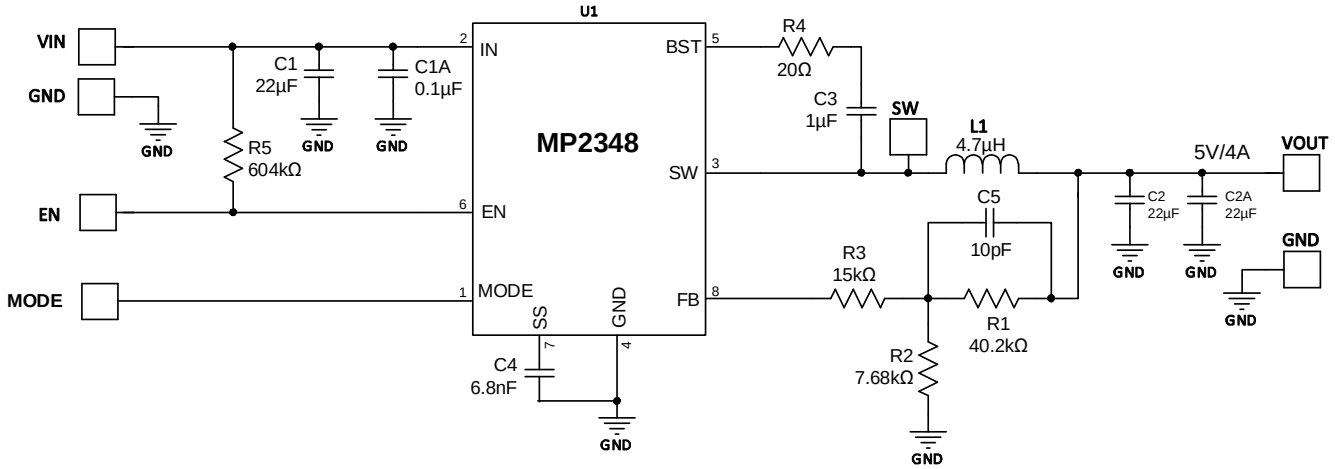

Figure 12: V_{OUT} = 5V

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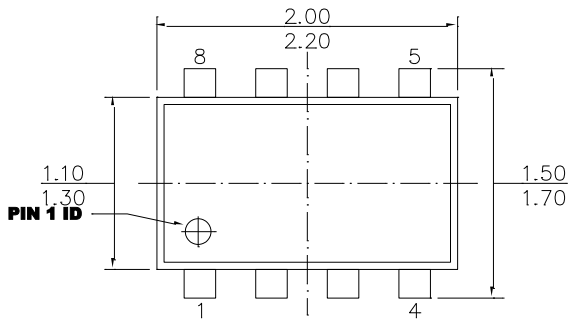
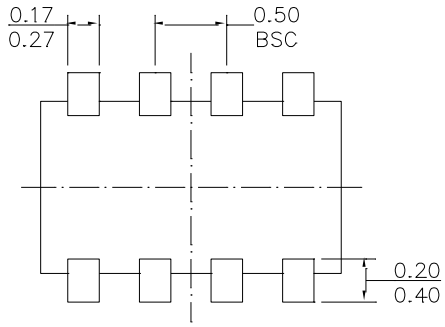
PACKAGE INFORMATION

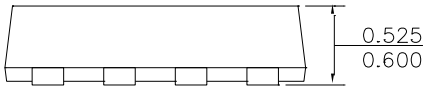
SOT583 (1.6mmx2.1mm)



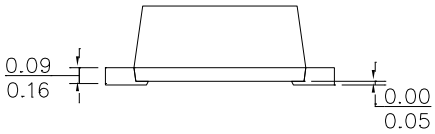
TOP VIEW



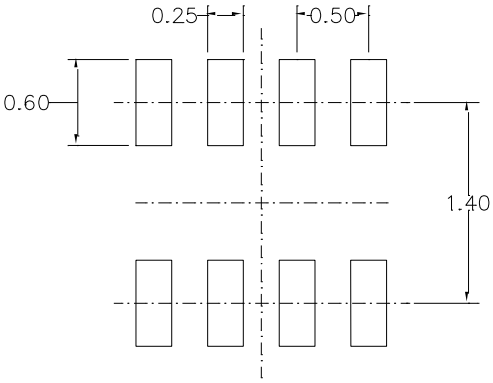
BOTTOM VIEW



FRONT VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
3) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
4) DRAWING IS NOT TO SCALE.

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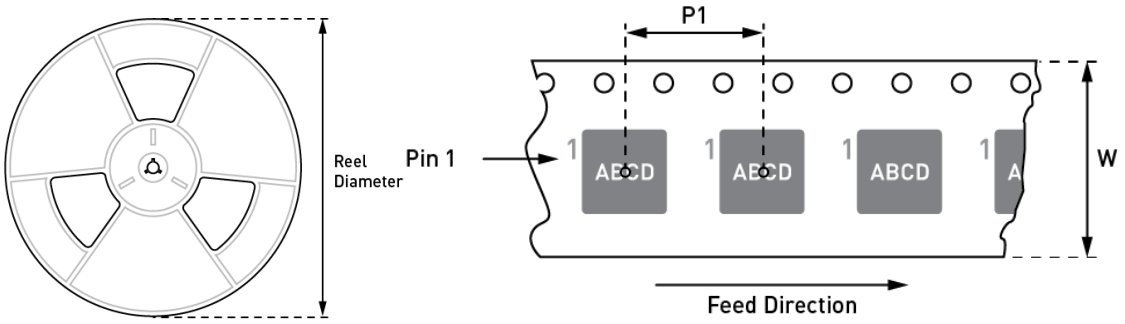
CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP2348GTL	SOT583	5000	N/A	N/A	7in	8mm	4mm

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