

DESCRIPTION

The MP2002A is a low-current, low-dropout linear regulator operating over a single input supply between 1.35V to 6.5V. The output voltage of the MP2002A is adjustable via an external resistor divider. The MP2002A can supply up to 500mA of load current. The enable pin (EN) allows the part to be put into a low current shutdown mode (EN = 0).

The MP2002A features thermal overload and current limit protection. It is available in an 8-pin QFN (2x 3mm) package

FEATURES

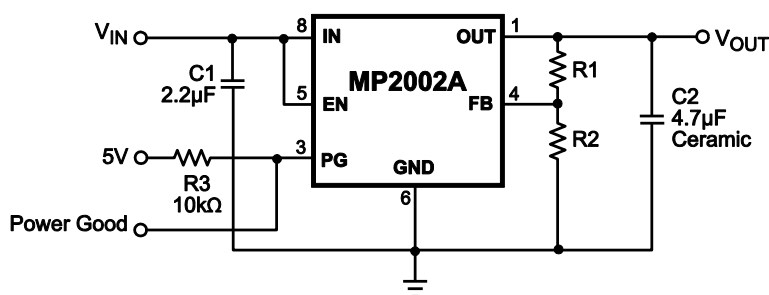
- Power Good Open-Drain Output
- Operates from 1.35V to 6.5V Input
- Low 300mV Dropout at 500mA Output
- Stable with Very Small Ceramic Capacitors
- 2% Feedback Reference
- Adjustable Output Voltage Option from 0.5V to 5V Using an External Resistor Divider
- Better Than 0.001%/mA Load Regulation
- Low 100 μ A Ground Current
- Internal Thermal Protection
- Current Limit Protection
- 7 μ A Typical Shutdown Current
- Available in a QFN-8 (2mmx3mm) Package

APPLICATIONS

- Low-Current Regulators
- Battery-Powered Systems
- Cellular Phones

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TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP2002AGD	QFN-8 (2mmx3mm)	See Below	1

* For Tape & Reel, add suffix -Z (e.g. MP2002AGD-Z).

TOP MARKING

BLRY

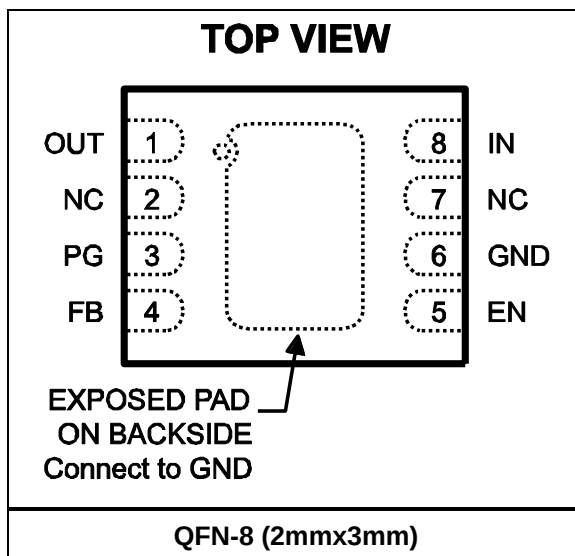
LLLL

BLR: Product code of MP2002AGD

Y: Year code

LLLL: Lot number

PACKAGE REFERENCE



PIN FUNCTIONS

Pin #	Name	Description
1	OUT	Regulator output. OUT is the output of the linear regulator. Bypass OUT to GND with a 4.7 μ F or greater capacitor.
2	NC	No connection.
3	PG	Power good open-drain output. If PG is pulled up to an external voltage, PG will be de-asserted (pulled high by external power source) if input power is off. See the Application Information section on page 10 for additional details.
4	FB	Feedback input. Connect a resistive voltage divider from OUT to FB to set the output voltage. OUT feedback threshold is 0.5V.
5	EN	Enable input. Drive EN above 1.2V to turn on the MP2002A; drive EN below 0.4V to turn it off.
6	GND, Exposed pad	Ground. The exposed pad must be connected to the GND plane.
7	NC	No connection.
8	IN	Power source input. IN supplies the internal power to the MP2002A, and is the source of the pass transistor. Bypass IN to GND with a 2.2 μ F or greater capacitor.

ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

IN, PG, FB to GND.....-0.3V to +7V
 EN to GND.....-0.3V to $V_{IN} + 0.3V$
 OUT.....-0.3V to $V_{IN} + 0.3V$
 Continuous power dissipation ($T_A = 25^{\circ}C$) ⁽²⁾
2.27W
 Junction temperature150 $^{\circ}C$
 Lead temperature260 $^{\circ}C$
 Storage temperature..... -65 $^{\circ}C$ to +150 $^{\circ}C$

Recommended Operating Conditions ⁽³⁾

Input Voltage (V_{IN}).....1.35V to 6.5V
 Output voltage0.5V to 5V
 Load current.....500mA maximum
 Maximum junction temp (T_J)125 $^{\circ}C$

Thermal Resistance

 θ_{JA} θ_{JC}

QFN-8 (2mmx3mm)

JESD51-7 ⁽⁴⁾ 55 12... $^{\circ}C/W$

Notes:

- 1) Exceeding these ratings may damage the device.
- 2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA} , and the ambient temperature, T_A . The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = $(T_J$ (MAX) - T_A) / θ_{JA} . Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- 3) The device is not guaranteed to function outside of its operating conditions.
- 4) Measured on JESD51-7 4-layer board. The value of θ_{JA} is only valid for comparison with other packages, and cannot be used for design purposes. These values are calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

$V_{IN} = 1.8V$, $V_{OUT} = 1.2V$, $C_{OUT} = 4.7\mu F$, $C_{IN} = 2.2\mu F$, $T_A = 25^\circ C$, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ ⁽⁵⁾	Max	Units
Operating voltage		$I_{OUT} = 1mA$	1.35		6.5	V
Ground pin current		$I_{OUT} = 1mA$ ⁽⁷⁾		100		μA
		$I_{OUT} = 500mA$		5		mA
Shutdown current		$V_{EN} = 0V$, $V_{IN} = 5V$		7		μA
FB regulation voltage			0.482	0.500	0.508	V
		$-40^\circ C \leq T_A \leq +85^\circ C$	0.477	0.495	0.513	
Dropout voltage ⁽⁸⁾		$I_{OUT} = 500mA$		290		mV
Line regulation ⁽⁶⁾		$I_{OUT} = 1mA$, $V_{IN} = (V_{OUT} + 0.5V)$ to $6.5V$ ⁽⁸⁾		0.005		%/V
Load regulation ⁽⁶⁾		$I_{OUT} = 1mA$ to $500mA$, $V_{IN} = V_{OUT} + 0.5V$		0.001		%/mA
Power good low output voltage ⁽⁹⁾	V_{OL}	$I_{SINK} = 0.5mA$		0.5		V
EN high input voltage			1.2			V
EN low input voltage					0.4	V
EN input bias current		$V_{EN} = 1.5V, 5V$		0.01	1	μA
Thermal protection				155		$^\circ C$
Current limit			550	730		mA

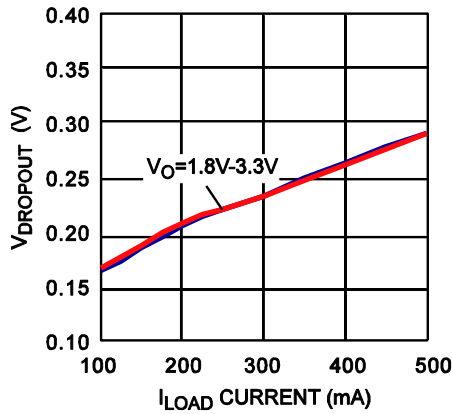
Notes:

- 5) Parameter is guaranteed by design. Not tested in production.
- 6) Resistors for V_{OUT} are measured as 10k Ω , 14k Ω , 1%.
- 7) The ground current does not include the current through the feedback current.
- 8) Dropout voltage is defined as the input to output differential when the output voltage drops 1% below its nominal value.
- 9) $V_{FEEDBACK}$ is 90% of the regulated value with a 10k Ω pull-up resistor to 5V

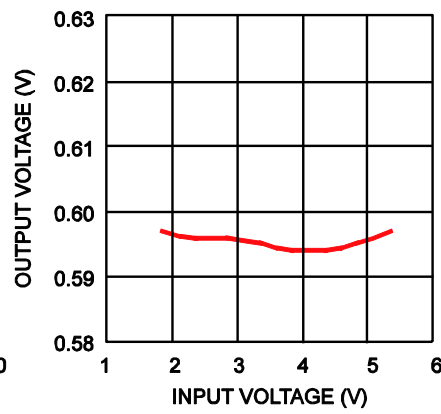
TYPICAL PERFORMANCE CHARACTERISTICS

C1 = 2.2μF, C2 = 4.7μF, C3 = 1nF, T_A = 25°C, unless otherwise noted.

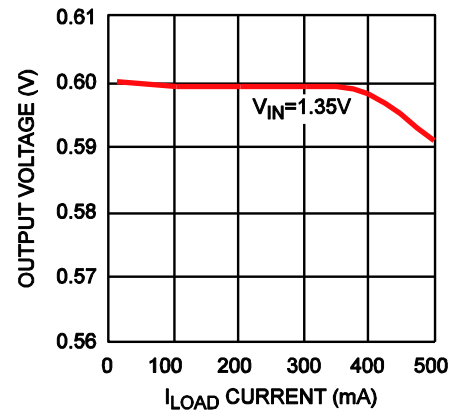
Voltage Dropout vs. Current



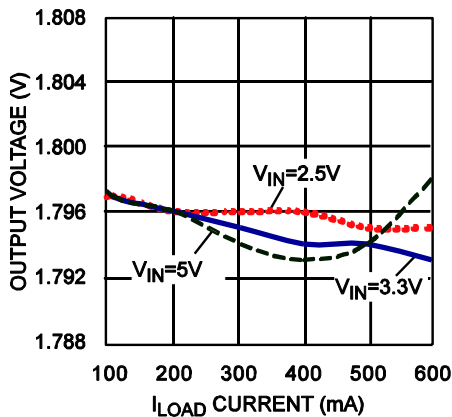
Line Regulation



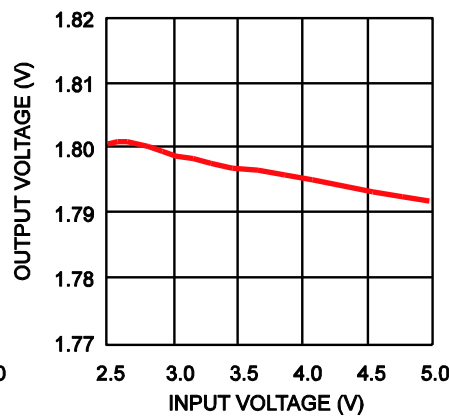
Load Regulation



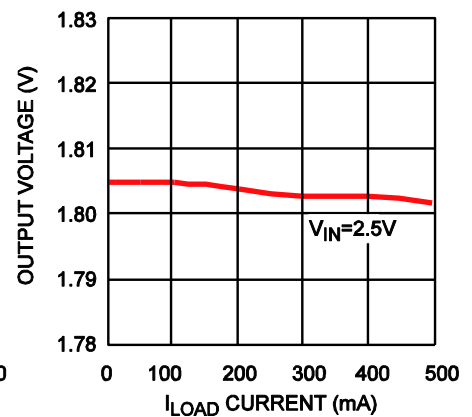
Load Regulation at 85°C



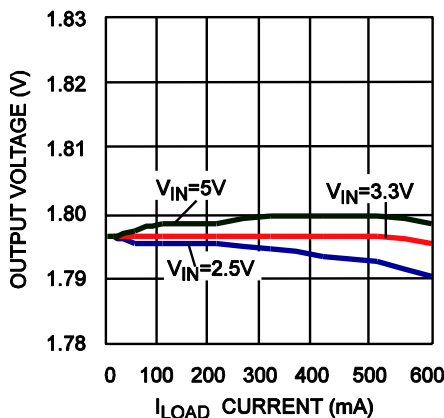
Line Regulation



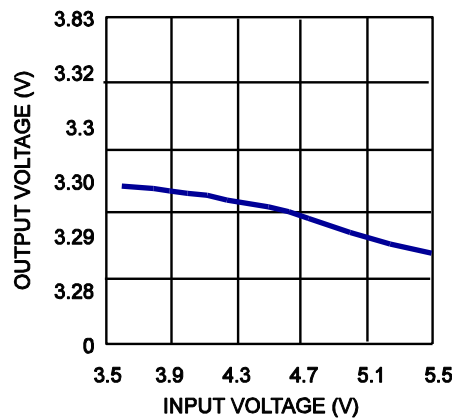
Load Regulation



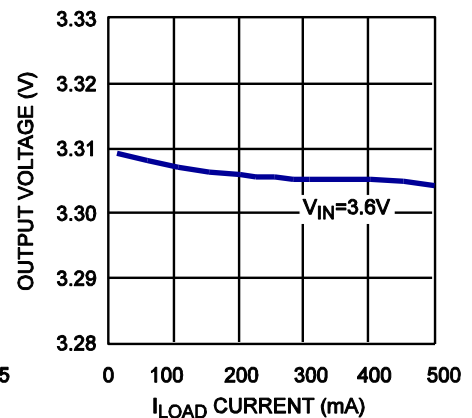
Load Regulation at -40°C



Line Regulation

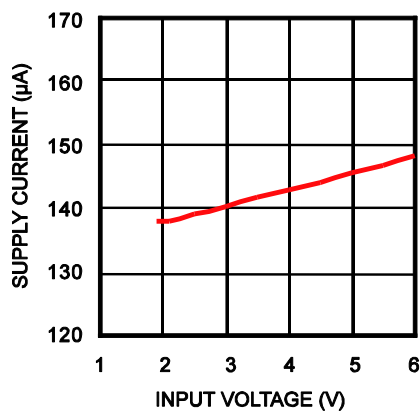
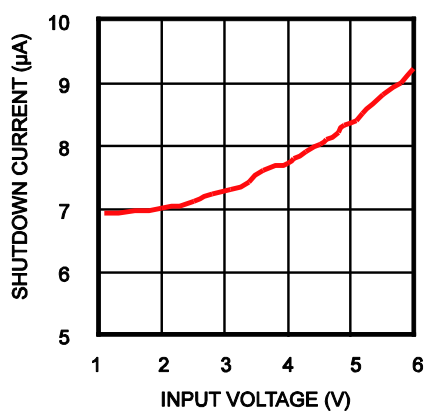
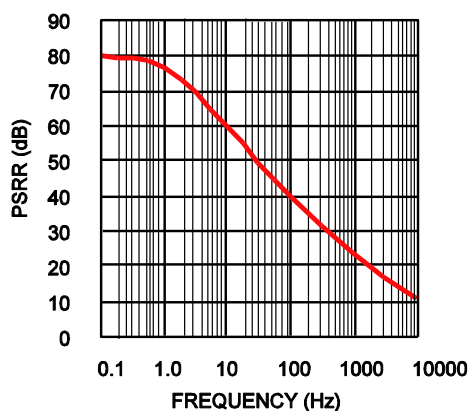


Load Regulation

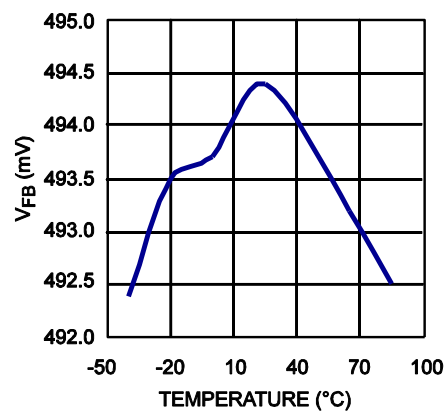


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

C1 = 2.2 μ F, C2 = 4.7 μ F, C3 = 1nF, T_A = 25°C, unless otherwise noted.

Supply Current

Shutdown Current vs. Input Voltage

PSRR vs. Frequency

Feedback Voltage vs. Temperature

V_{IN} = 1.8V, V_{EN} = V_{IN}, I_{LOAD} = 1mA

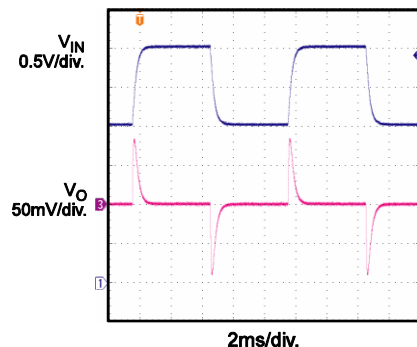


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

C1 = 2.2μF, C2 = 4.7μF, C3 = 1nF, T_A = 25°C, unless otherwise noted.

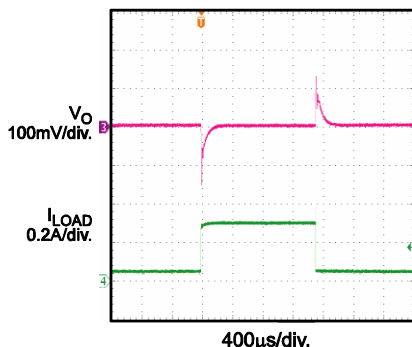
Line Transient

V_{IN} = 2V to 3V, V_O = 1.8V, V_{EN} = V_{IN},
I_{LOAD} = 50mA, with resistor load



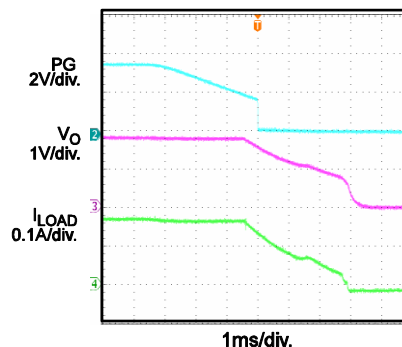
Load Transient

V_{IN} = 2.5V, V_O = 1.8V, V_{EN} = V_{IN},
I_{LOAD} = 50mA to 300mA, with resistor load



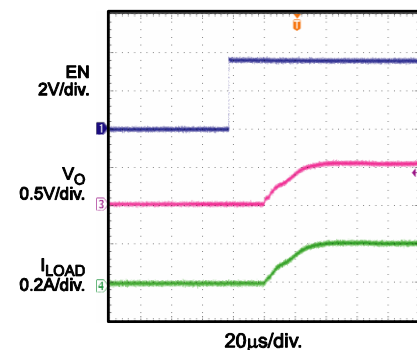
Power Good Off

V_{IN} = 3.6V, V_O = 1.8V,
V_{EN} = V_{IN}, I_{LOAD} = 0.17A, with resistor load



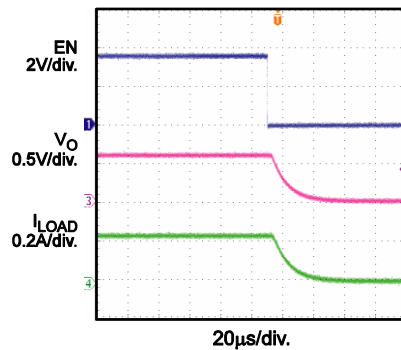
Enable Turn-On

V_{IN} = 1.35V, V_O = 0.6V, V_{EN} = 0V to 3.6V,
I_{LOAD} = 200mA, with resistor load



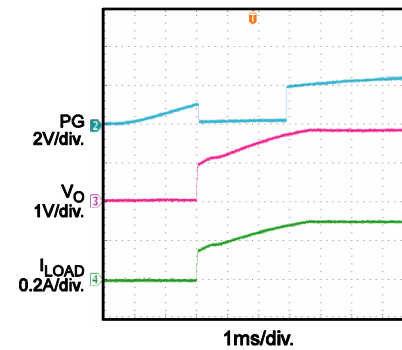
Enable Turn-Off

V_{IN} = 1.35V, V_O = 0.6V, V_{EN} = 3.6V to 0V,
I_{LOAD} = 200mA, with resistor load



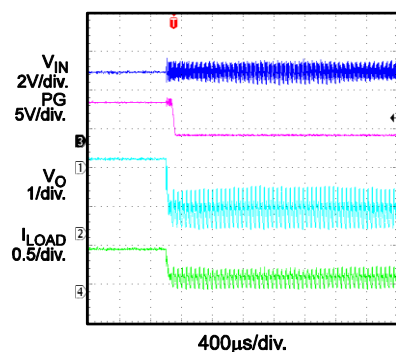
Power Good On

V_{IN} = 2.5V, V_O = 1.8V, V_{EN} = V_{IN},
I_{LOAD} = 0.3A, with resistor load



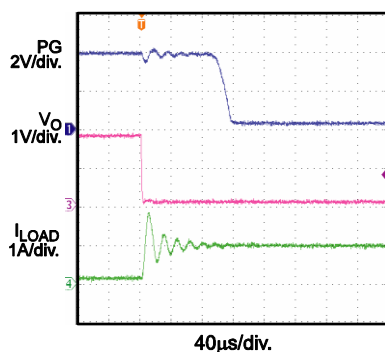
Thermal Protection

V_{IN} = V_{EN} = 5V, V_O = 1.8V, I_{LOAD} = 0.5A



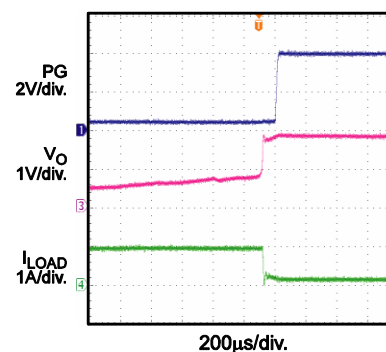
Short-Circuit Protection

V_{IN} = 4V, V_O = 1.8V, V_{EN} = V_{IN}



Short-Circuit Recovery

V_{IN} = 4V, V_O = 1.8V, V_{IN} = V_{EN}



FUNCTIONAL BLOCK DIAGRAM

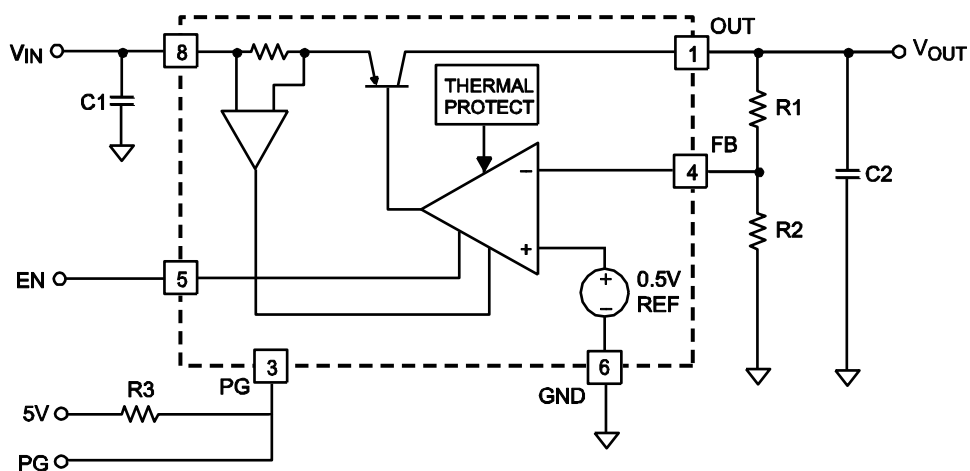


Figure 1: Functional Block Diagram

OPERATION

The MP2002A is a low-current, low-voltage, high power supply rejection ratio (PSRR), low-dropout linear regulator. It is intended for devices that require very low voltage, low quiescent current power, and high PSRR (e.g. wireless modems, pagers, and cellular phones).

The MP2002A uses a PNP transistor. It features internal thermal shutdown and an internal current limit circuit.

APPLICATION INFORMATION

Setting the Output Voltage

The MP2002A has an adjustable output voltage, set via an external resistor divider (R1 and R2). R1 can be calculated with Equation (1):

$$R1 = R2 \times \left(\frac{V_{OUT} - V_{FB}}{V_{FB}} \right) \quad (1)$$

Where V_{FB} is the feedback voltage threshold on the OUT pin (about 0.5V).

For example, if the output voltage is 2.5V and R2 is 10kΩ, R1 would be 40kΩ. A standard 40kΩ ($\pm 1\%$) resistor can be used for R1.

Table 1 lists R1 values for typical output voltages (assuming R2 = 10kΩ).

Table 1: Adjustable Output Voltage and R1 Values

V _{OUT} (V)	R1 (kΩ)
1.25	15
1.5	20
1.8	26
2	30
2.5	40
2.8	46
3	50
3.3	56
4	70
5	90

Power Good (PG)

The power good (PG) pin is an open-drain output with a pull-up resistor (10kΩ recommended). The pull-up resistor can be tied to a 0V to 5.5V supply within the voltage range of the pin. For example, the pull-up resistor can be tied to the input voltage when it is being monitored by an IC powered from this input voltage.

PG monitors the output voltage. If the output voltage is 10% below its regulation point, the PG pin is pulled low.

PG can be pulled up by external power source. PG is pulled high by the external VCC when V_{IN} is below 0.86V (typically), because the internal control circuits are disabled and the open-drain FET is off. When EN is off and V_{IN} drops below the under-voltage lockout (UVLO) threshold, PG is pulled low.

Selecting the Bypass Capacitor

To reduce noise, the reference voltage can be bypassed via an external capacitor. It is recommended to use a low-ESR ceramic capacitor for the best performance.

PCB Layout Guidelines

PCB layout is critical for good regulation, ripple rejection, transient response, and thermal performance. It is highly recommended to duplicate the EVB layout for optimal performance. For the best results, refer to Figure 2 and follow the guidelines below:

1. Place ceramic input ceramic capacitors close to the IN pin.
2. Place ceramic output capacitors close to the OUT pin.
3. Ensure all feedback connections are short and direct.
4. Place the feedback resistors and compensation components as close to the chip as possible.
5. Connect IN, OUT, and especially GND to a large copper area to cool the chip, and improve thermal performance and long-term reliability.

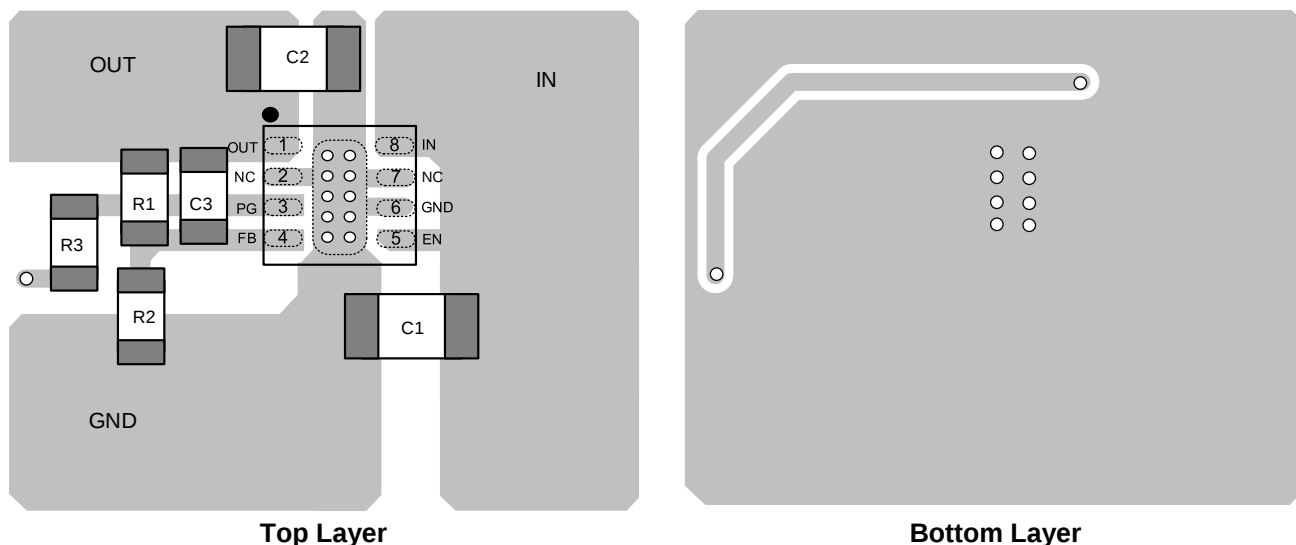


Figure 2: Recommended PCB Layout

TYPICAL APPLICATION CIRCUIT

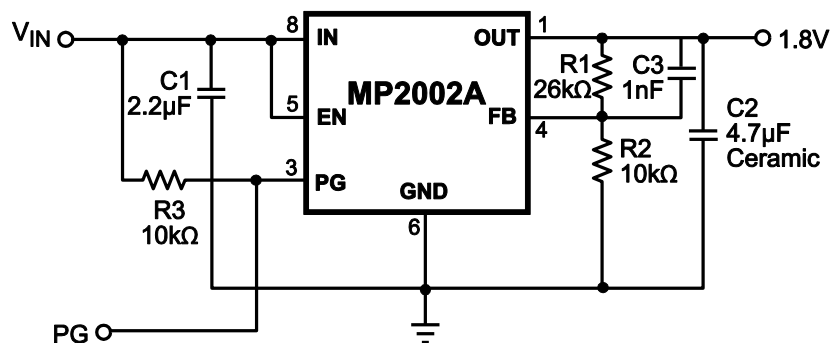


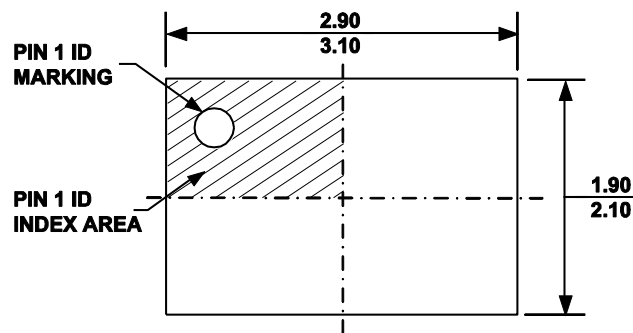
Figure 3: Typical Application Circuit with Fixed OUT Pin ⁽¹⁰⁾

Note:

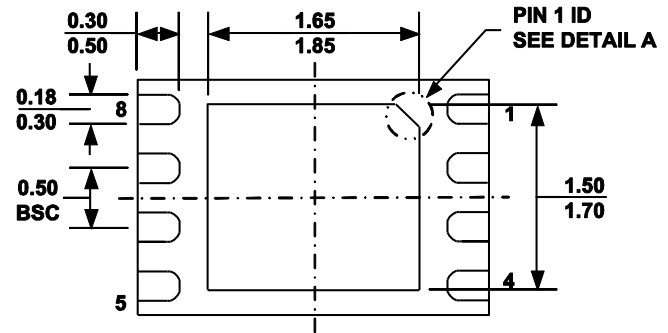
10) If PG is pulled up to an external power supply, see the Power Good (PG) section on page 10.

PACKAGE INFORMATION

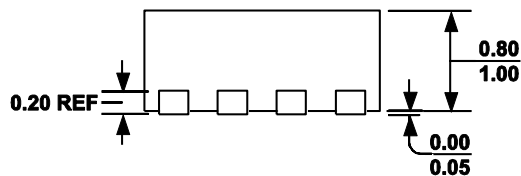
QFN-8 (2mmx3mm)



TOP VIEW

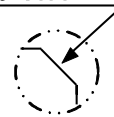


BOTTOM VIEW

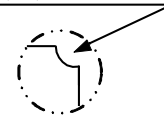


SIDE VIEW

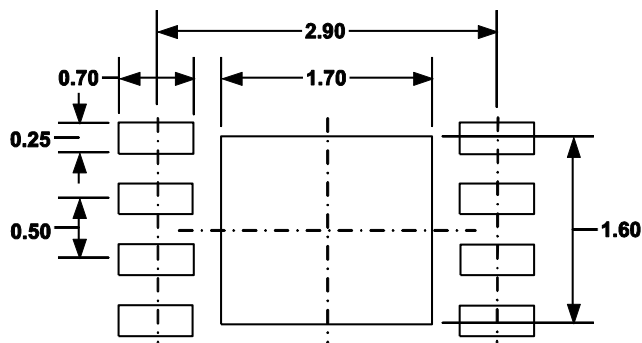
PIN 1 ID OPTION A
0.30x45° TYP.



PIN 1 ID OPTION B
R0.20 TYP.



DETAIL A

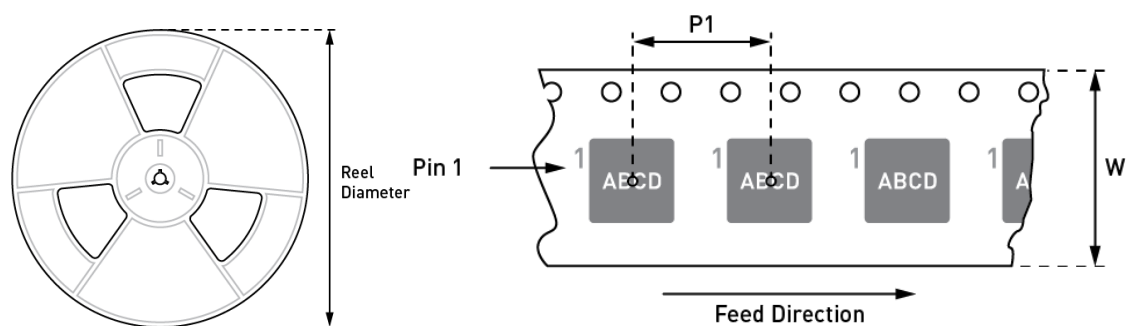


RECOMMENDED LAND PATTERN

NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
- 3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
- 4) DRAWING CONFORMS TO JEDEC MO-229, VARIATION VCED-2.
- 5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP2002AGD-Z	QFN-8 (2mmx3mm)	5000	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	4/23/2021	Initial Release	-

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