The Future of Analog IC Technology®

MPQ4430

36V, 3.5A, Low Quiescent Current, Synchronous, Step-Down Converter AEC-Q100 Qualified

DESCRIPTION

The MPQ4430 is a frequency-programmable (350kHz to 2.5MHz), synchronous, step-down, switching regulator with integrated internal high-side and low-side power MOSFETs. It provides up to 3.5A of highly efficient output current with current mode control for fast loop response.

The wide 3.3V to 36V input range accommodates a variety of step-down applications in automotive input environments and is ideal for battery-powered applications due to its extremely low quiescent current.

The MPQ4430 employs advanced asynchronous mode (AAM), which helps achieve high efficiency in light-load condition by scaling down the switching frequency to reduce switching and gate driving losses.

Standard features include soft start (SS), external clock synchronization, enable (EN) control, and a power good (PG) indicator. High-duty cycle and low dropout mode are provided for automotive cold-crank condition.

Over-current protection (OCP) with valley-current detection is employed to prevent the inductor current from running away. Hiccup mode reduces the average current in short-circuit condition greatly. Thermal shutdown provides reliable and fault-tolerant operation.

The MPQ4430 is available in a QFN-16 (3mmx4mm) package.

FEATURES

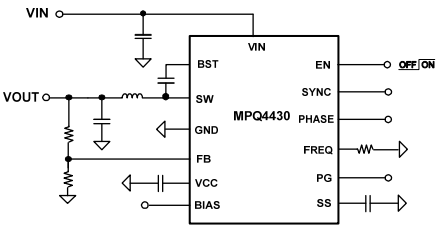
- Wide 3.3V to 36V Operating Input Range
- 3.5A Continuous Output Current
- 1μA Low Shutdown Mode Current
- 10μA Sleep Mode Quiescent Current
- Internal 90mΩ High-Side and 40mΩ Low-Side MOSFETs
- 350kHz to 2.5MHz Programmable Switching Frequency
- Fixed Output Options: 3.3V, 3.8V, 5V
- Synchronize to External Clock
- Selectable In-Phase or 180° Out-of-Phase
- Power Good (PG) Indicator
- Programmable Soft-Start (SS) Time
- 80ns Minimum On Time
- Selectable Forced CCM or AAM
- Low Dropout Mode
- Over-Current Protection (OCP) with Valley-Current Detection and Hiccup
- Available in a QFN-16 (3mmx4mm) Package
- Available with Wettable Flank
- AEC-Q100 Grade 1

APPLICATIONS

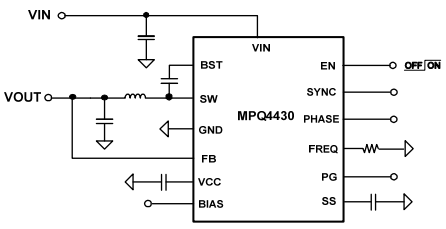
- Automotive Systems
- Industrial Power Systems

All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance. "MPS" and "The Future of Analog IC Technology" are registered trademarks of Monolithic Power Systems, Inc.

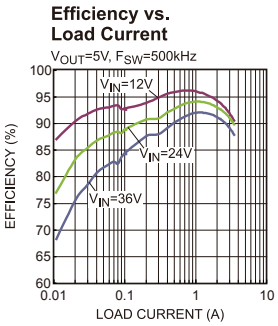
TYPICAL APPLICATION



Output Adjustable Version



Output Fixed Version



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating**
MPQ4430GL	QFN-16 (3mmx4mm)	*See Below*	1
MPQ4430GL-AEC1			
MPQ4430GLE-AEC1***		*See Below*	
MPQ4430GLE-38-AEC1***		*See Below*	
MPQ4430GLE-5-AEC1***		*See Below*	

* For Tape & Reel, add suffix –Z (e.g. MPQ4430GL–Z)
** Moisture Sensitivity Level Rating
*** Wettable Flank

TOP MARKING (MPQ4430GL & MPQ4430GL-AEC1)

MPYW
4430
LLL

MP: MPS prefix
Y: Year code
W: Week code
4430: First four digits of the part number
LLL: Lot number

TOP MARKING (MPQ4430GLE-AEC1)

MPYW
4430
LLL
E

MP: MPS prefix
Y: Year code
W: Week code
4430: First four digits of the part number
LLL: Lot number
E: Wettable lead flank

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

TOP MARKING (MPQ4430GLE-38-AEC1)

MPYW
4430
LLL
E38

MP: MPS prefix
Y: Year code
W: Week code
4430: First four digits of the part number
LLL: Lot number
E: Wettable lead flank
38: 3.8V fixed output

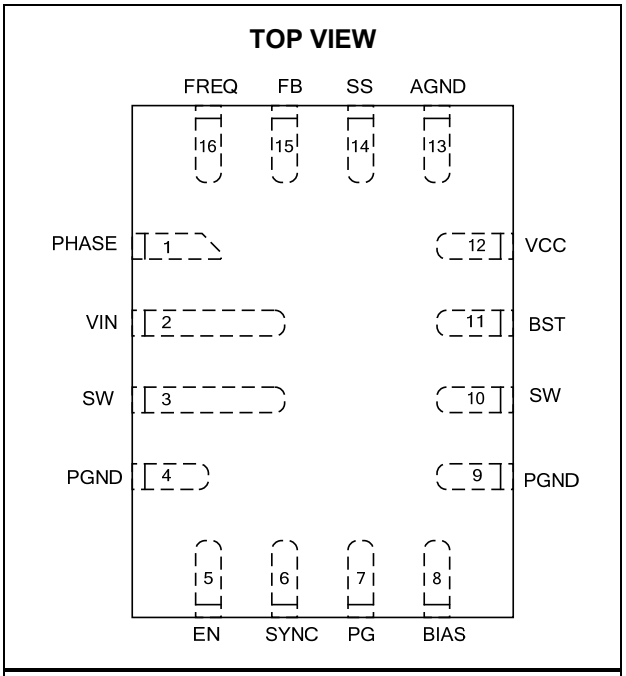
TOP MARKING (MPQ4430GLE-5-AEC1)

MPYW
4430
LLL
E5

MP: MPS prefix
Y: Year code
W: Week code
4430: First four digits of the part number
LLL: Lot number
E: Wettable lead flank
5: 5V fixed output

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

PACKAGE REFERENCE



QFN-16 (3mmx4mm)

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (VIN) ..... -0.3V to 40V
Switch voltage (V_{SW}) ..... -0.3V to VIN +0.3V
BST voltage (V_{BST}) ..... V_{SW} + 6.5V
EN voltage (V_{EN}) ..... -0.3V to 40V
BIAS voltage (V_{BIAS}) ..... -0.3V to 20V
All other pins ..... -0.3V to 6V
Continuous power dissipation (T_A = +25°C) (2)
QFN-16 (3mmx4mm) 2.6W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to 150°C

Electrostatic Discharge (ESD)

HBM (human body model) ..... ±2kV
CDM (charged device model) ..... ±750V

Recommended Operating Conditions

Supply voltage (VIN) ..... 3.3V to 36V
Operating junction temp. (T_J) (3)
……..-40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

QFN-16 (3mmx4mm)
JESD51-7(4) ..... 48 ..... 11 ... °C/W
EV4430-L-00A (5) ..... 43 ..... 5 .... °C/W

NOTES:

1) Absolute maximum ratings are rated under room temperature unless otherwise noted. Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D(MAX)=(T_J(MAX)-T_A)/ θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Mission profiles requiring operation above 125°C T_J may be supported; contact MPS for details.
4) Measured on JESD51-7, 4-layer PCB.
5) Measured on EV4430-L-00A, 6.35cm * 6.35cm size, 2oz, 4-layer PCB.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS

VIN = 12V, V_{EN} = 2V, T_J = -40°C to +125°C, unless otherwise noted. Typical values at T_J = +25°C.

Parameter	Symbol	Condition	Min	Typ	Max	Units
VIN quiescent current	I_Q	V_{FB} = 0.85V, no load, no switching, T_J = +25°C		10	18	μA
		V_{FB} = 0.85V, no load, no switching		10	25	
VIN shutdown current	I_{SHDN}	V_{EN} = 0V		1	5	μA
VIN under-voltage lockout threshold rising	$INUV_{RISING}$		2.4	2.8	3.2	V
VIN under-voltage lockout threshold hysteresis	$INUV_{HYS}$			150		mV
Feedback reference voltage	V_{REF}		784	800	816	mV
		T_J = 25°C	792	800	808	mV
Output voltage accuracy of MPQ4430-38	V_{OUT}		3705	3800	3895	mV
		T_J = 25°C	3743	3800	3857	mV
Output voltage accuracy of MPQ4430-5	V_{OUT}		4875	5000	5125	mV
		T_J = 25°C	4925	5000	5075	mV
Switching frequency	f_{SW}	R_{FREQ} = 180kΩ or from sync clock	400	475	550	kHz
		R_{FREQ} = 82kΩ or from sync clock	850	1000	1150	kHz
		R_{FREQ} = 27kΩ or from sync clock	2250	2500	2750	kHz
Minimum on time (6)	T_{ON_MIN}			80		ns
SYNC input low voltage	V_{SYNC_LOW}				0.4	V
SYNC input high voltage	V_{SYNC_HIGH}		1.8			V
Current limit	I_{LIMIT_HS}	Duty cycle = 40%	4.7	5.8	7.3	A
Low-side valley current limit	I_{LIMIT_LS}	V_{OUT} = 3.3V, L = 4.7μH	3.1	4.4	5.7	A
ZCD current	I_{ZCD}			0.1		A
Reverse current limit	$I_{LIMIT_REVERSE}$			3		A
Switch leakage current	I_{SW_LKG}			0.01	1	μA
HS switch on resistance	R_{ON_HS}	V_{BST} - V_{SW} = 5V		90	155	mΩ
LS switch on resistance	R_{ON_LS}			40	75	mΩ
Soft-start current	I_{SS}	V_{SS} = 0.8V	5	10	15	μA
EN rising threshold	V_{EN_RISING}		0.9	1.05	1.2	V
EN threshold hysteresis	V_{EN_HYS}			120		mV
PG rising threshold (V_{FB}/V_{REF})	PG_{RISING}	V_{FB} rising	85	90	95	%
		V_{FB} falling	105	110	115	
PG falling threshold (V_{FB}/V_{REF})	$PG_{FALLING}$	V_{FB} falling	79	84	89	%
		V_{FB} rising	113.5	118.5	123.5	%
PG deglitch timer	$T_{PG_DEGLITCH}$	PG from low to high		30		μs
		PG from high to low		50		μs
PG output voltage low	V_{PG_LOW}	I_{SINK} = 2mA		0.2	0.4	V
VCC regulator	V_{CC}			5		V
VCC load regulation		I_{CC} = 5mA			3	%

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS *(continued)*

VIN = 12V, V_{EN} = 2V, T_J = -40°C to +125°C, unless otherwise noted. Typical values at T_J = +25°C.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Thermal shutdown (6)	T_{SD}			170		°C
Thermal shutdown hysteresis (6)	T_{SD_HYS}			20		°C

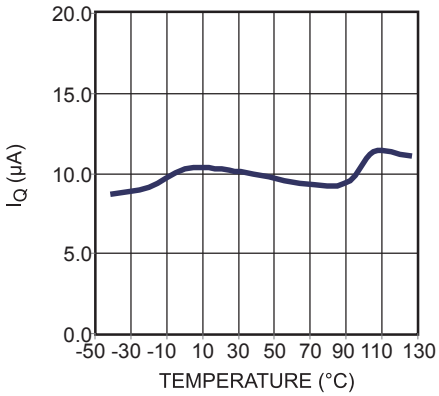
NOTE:
6) Not tested in production and guaranteed by design and characterization.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

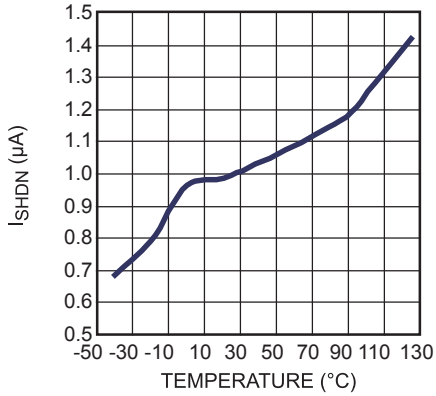
TYPICAL CHARACTERISTICS

VIN = 12V, T_J = -40°C to +125°C, unless otherwise noted.

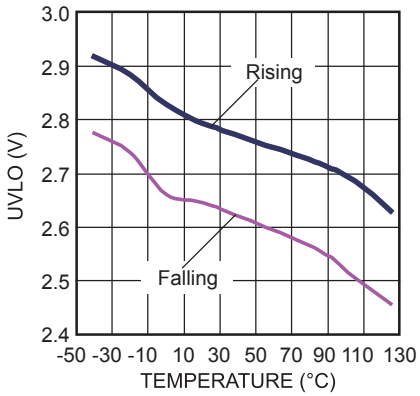
Quiescent Current vs. Temperature



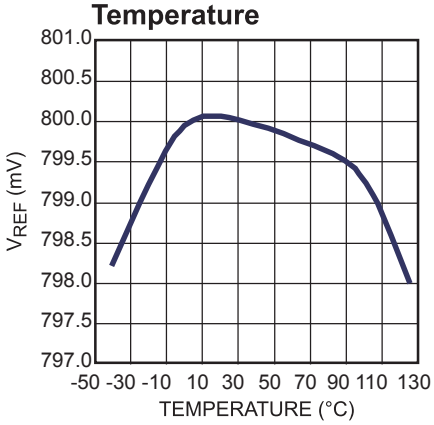
Shutdown Current vs. Temperature



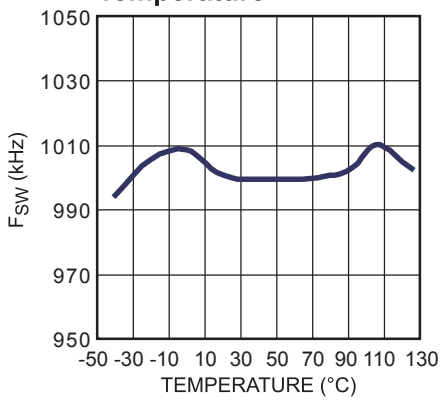
VIN UVLO Threshold vs. Temperature



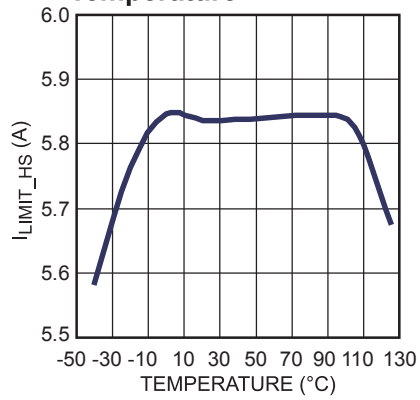
Feedback Reference vs. Temperature



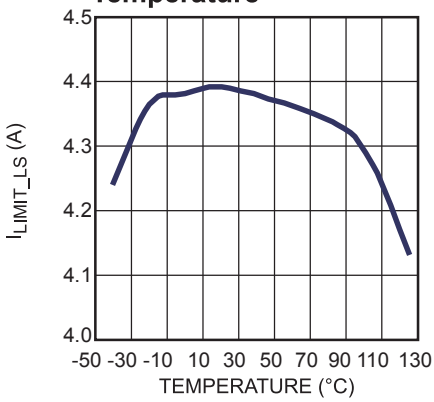
Switching Frequency vs. Temperature



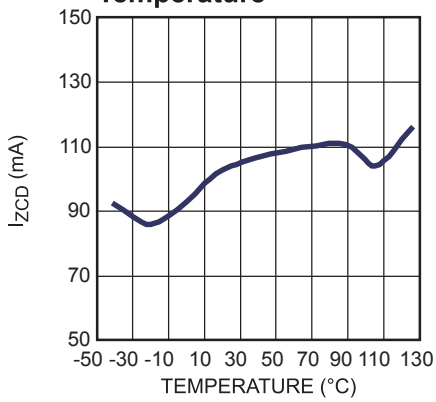
Current Limit vs. Temperature



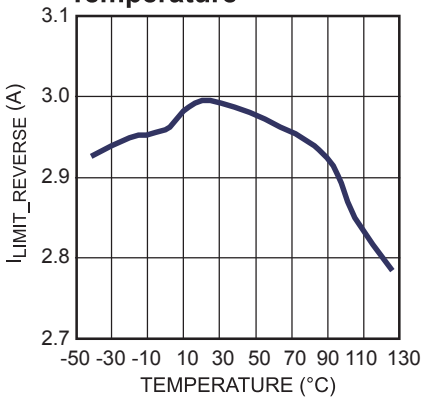
Valley Current Limit vs. Temperature



ZCD Current vs. Temperature



Reverse Current Limit vs. Temperature

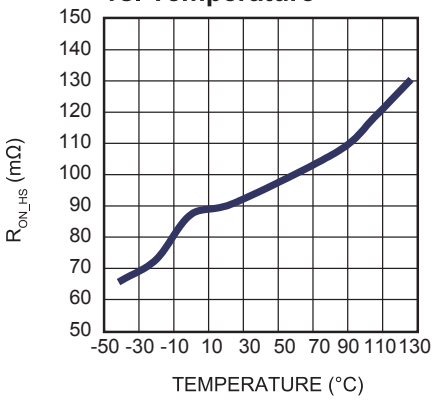


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

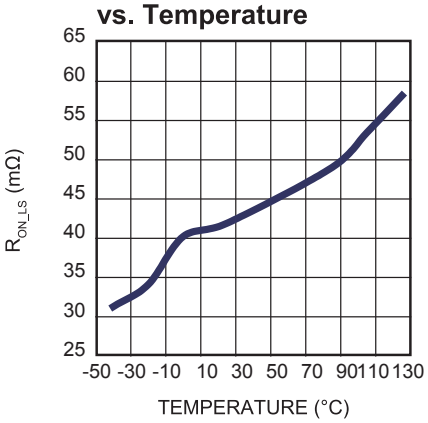
TYPICAL CHARACTERISTICS *(continued)*

VIN = 12V, T_J = -40°C to +125°C, unless otherwise noted.

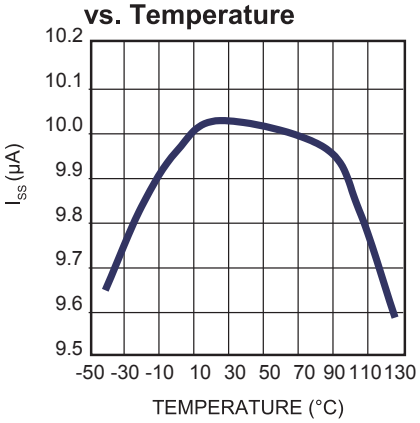
HS-FET On Resistance vs. Temperature



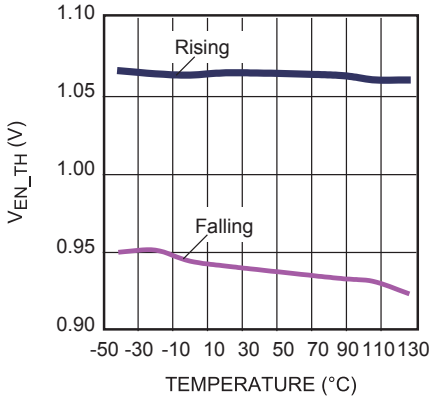
LS-FET On Resistance vs. Temperature



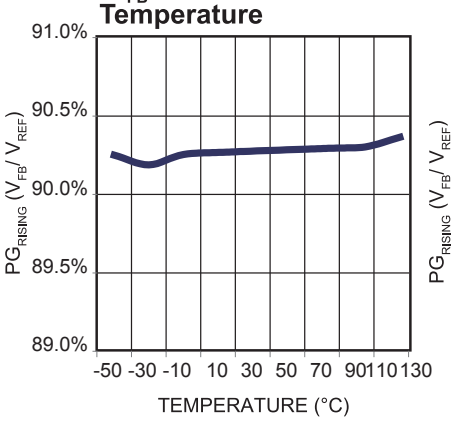
Soft-Start Current vs. Temperature



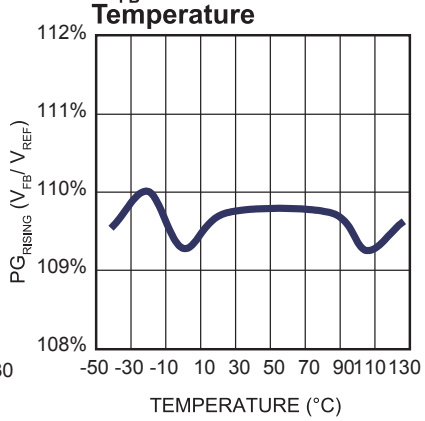
EN Threshold vs. Temperature



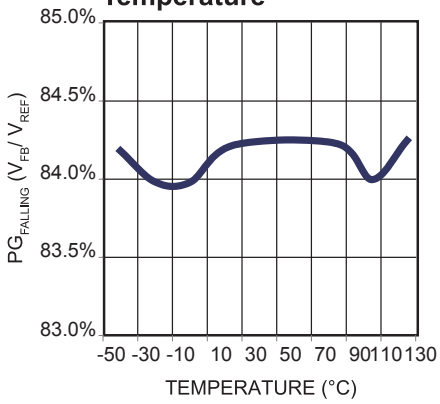
PG Rising Threshold (V_{FB} Rising) vs. Temperature



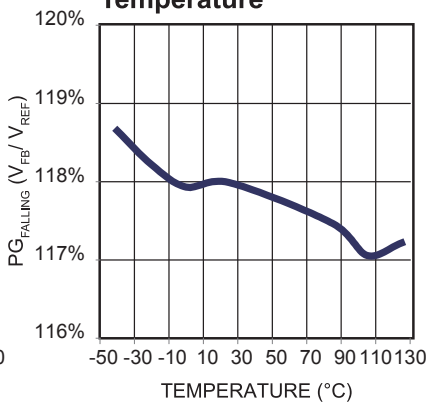
PG Rising Threshold (V_{FB} Falling) vs. Temperature



PG Falling Threshold (V_{FB} Falling) vs. Temperature



PG Falling Thershold (V_{FB} Rising) vs. Temperature

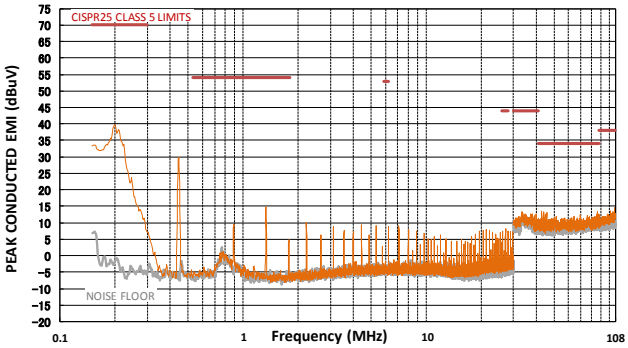


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

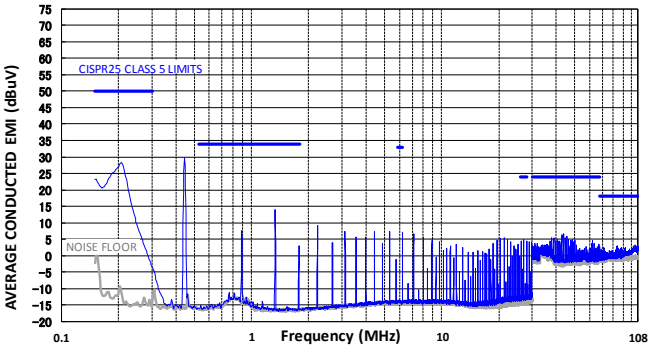
TYPICAL PERFORMANCE CHARACTERISTICS

VIN = 12V, V_{OUT} = 5V, Io=3.5A, L = 4.7µH, f_{SW} = 450kHz, with EMI filters, T_A = +25°C, unless otherwise noted. (7)

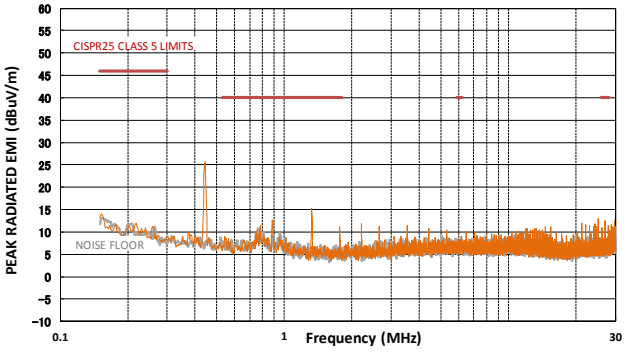
CISPR25 Class 5 Peak Conducted Emissions
150kHz -108MHz



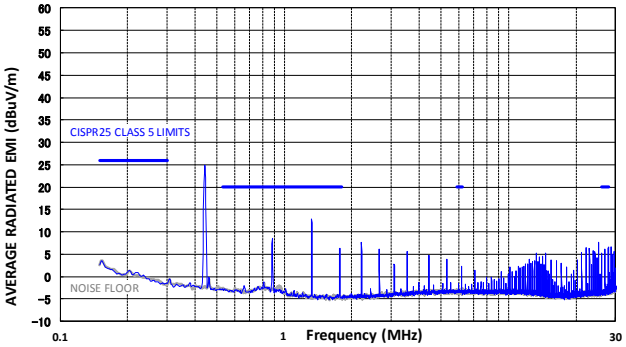
CISPR25 Class 5 Average Conducted Emissions
150kHz - 108MHz



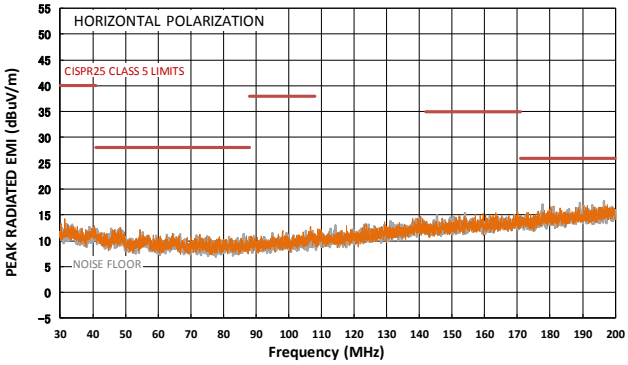
CISPR25 Class 5 Peak Radiated Emissions
150kHz-30MHz



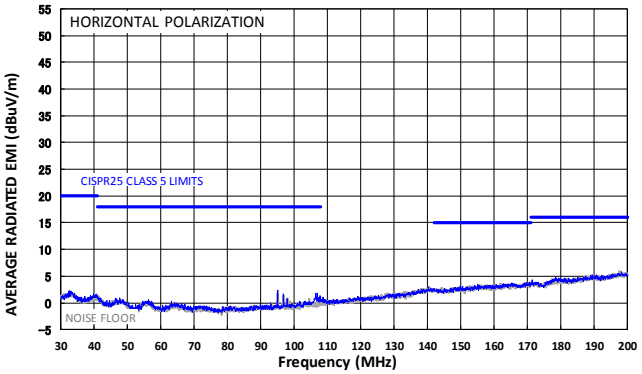
CISPR25 Class 5 Average Radiated Emissions
150kHz-30MHz



CISPR25 Class 5 Peak Radiated Emissions
Horizontal, 30MHz-200MHz



CISPR25 Class 5 Average Radiated Emissions
Horizontal, 30MHz-200MHz

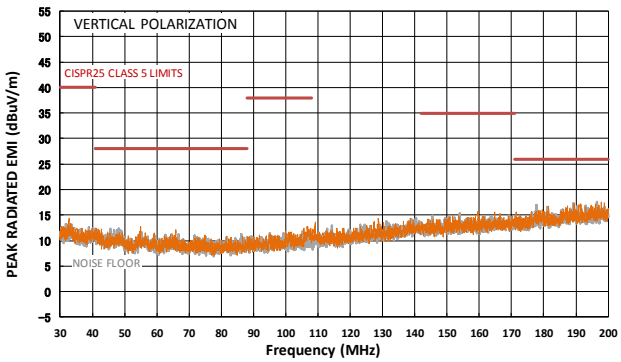


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

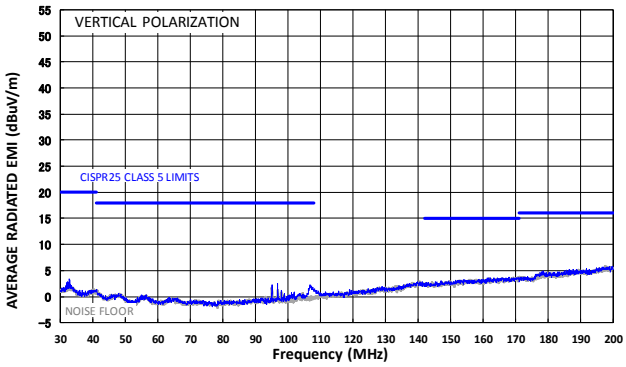
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

VIN = 12V, V_{OUT} = 5V, Io=3.5A, L = 4.7μH, f_{SW} = 450kHz, with EMI filters, T_A = +25°C, unless otherwise noted. (7)

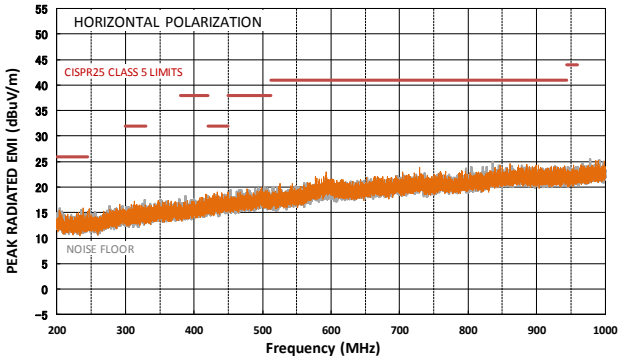
CISPR25 Class 5 Peak Radiated Emissions
Vertical, 30MHz-200MHz



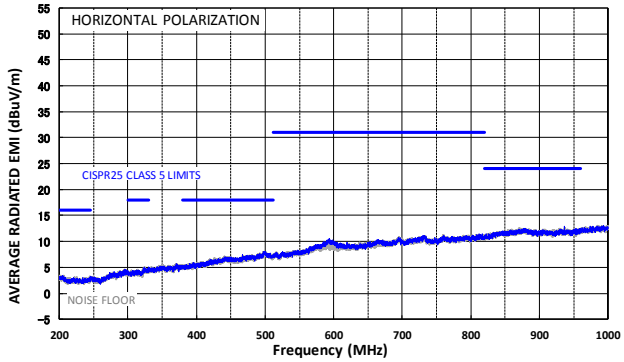
CISPR25 Class 5 Average Radiated Emissions
Vertical, 30MHz-200MHz



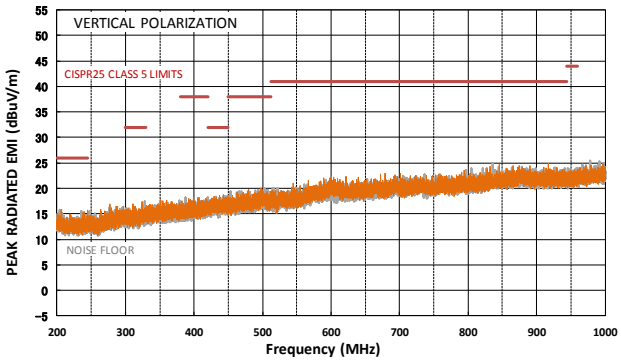
CISPR25 Class 5 Peak Radiated Emissions
Horizontal, 200MHz-1GHz



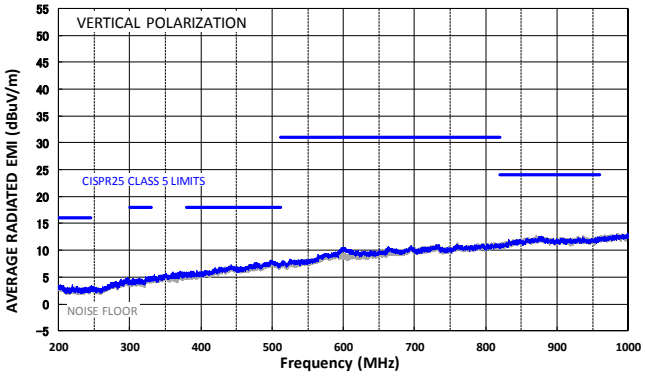
CISPR25 Class 5 Average Radiated Emissions
Horizontal,200MHz-1GHz



CISPR25 Class 5 Peak Radiated Emissions
Vertical, 200MHz-1GHz



CISPR25 Class 5 Average Radiated Emissions
Vertical,200MHz-1GHz



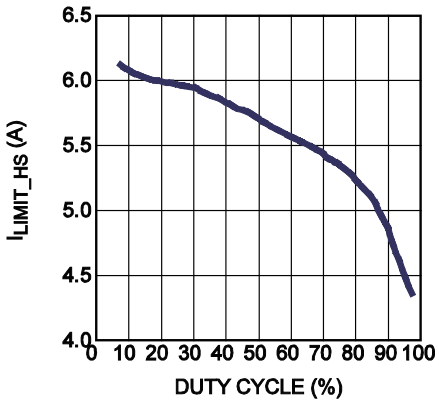
NOTE:
7) The EMC test results are based on the application circuit with EMI filters as shown in Figure17.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

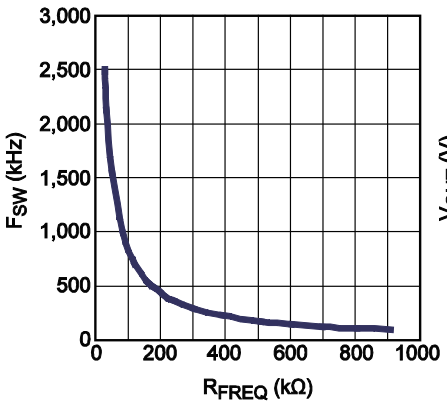
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

VIN = 12V, V_{OUT} = 3.3V, L = 10μH, f_{SW} = 500kHz, AAM, T_A = +25°C, unless otherwise noted.

Current Limit vs. Duty Cycle



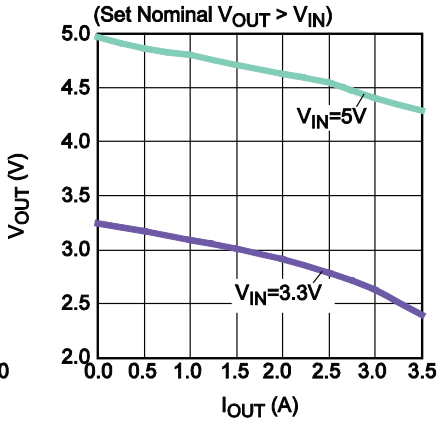
f_{SW} vs. R_{FREQ}



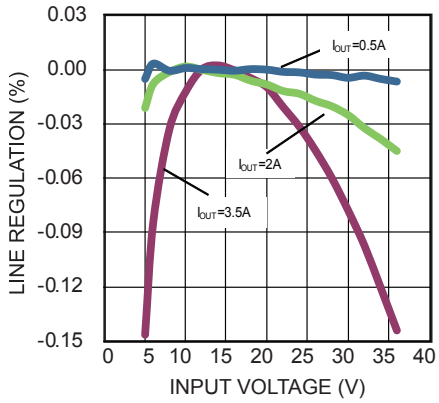
Output Voltage vs. Load Current

Dropout Performance

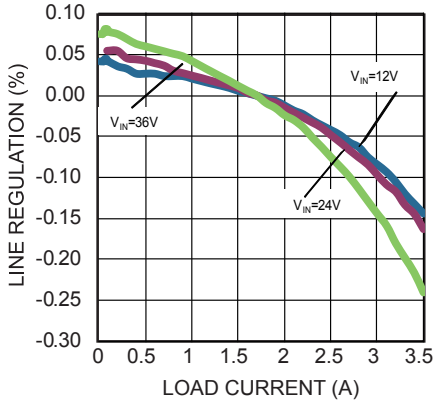
(Set Nominal V_{OUT} > V_{IN})



Line Regulation



Load Regulation

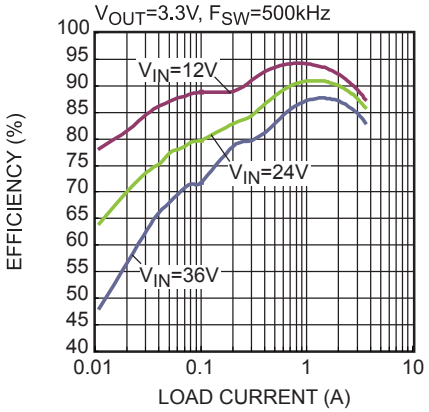


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

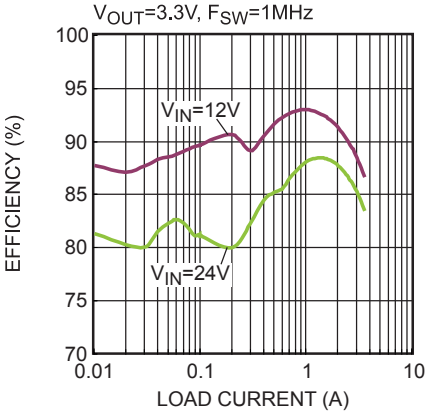
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

VIN = 12V, V_{OUT} = 3.3V, L = 10μH, f_{SW} = 500kHz, AAM, T_A = +25°C, unless otherwise noted.

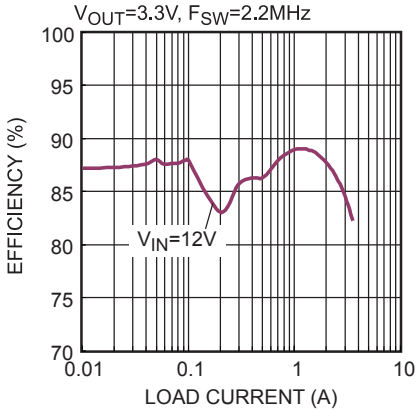
Efficiency vs. Load Current



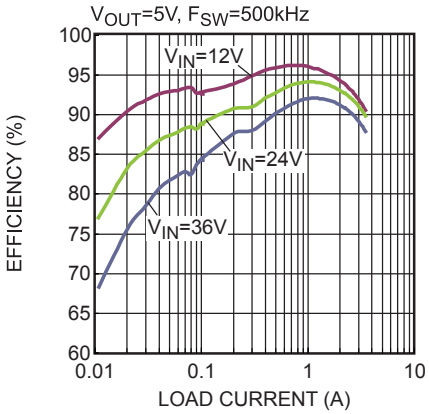
Efficiency vs. Load Current



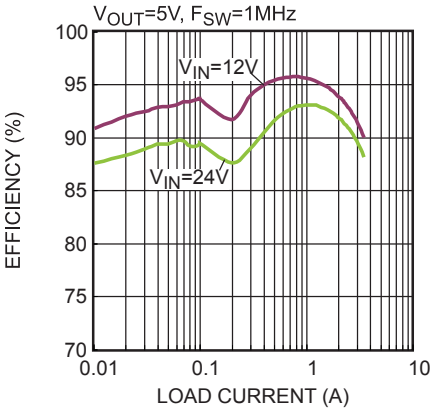
Efficiency vs. Load Current



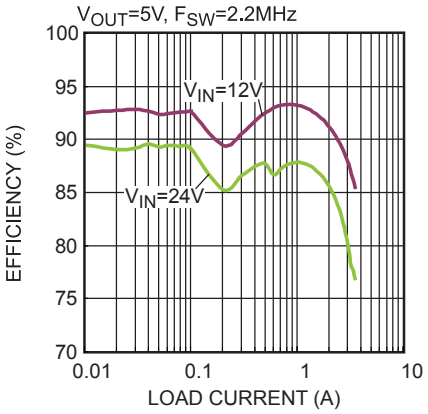
Efficiency vs. Load Current



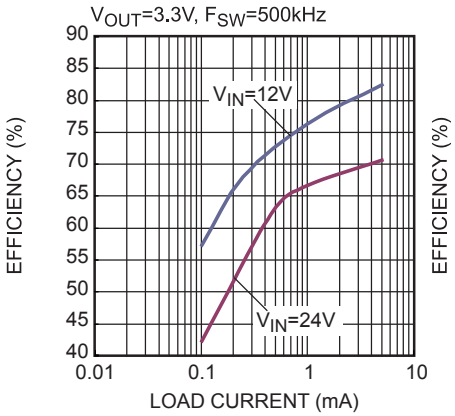
Efficiency vs. Load Current



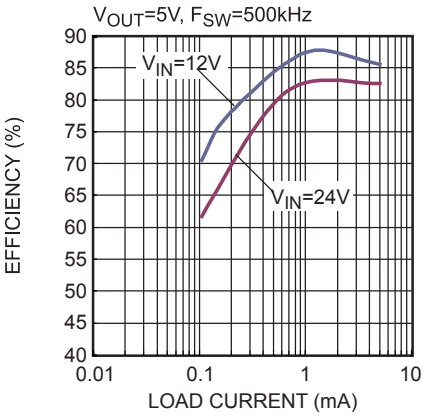
Efficiency vs. Load Current



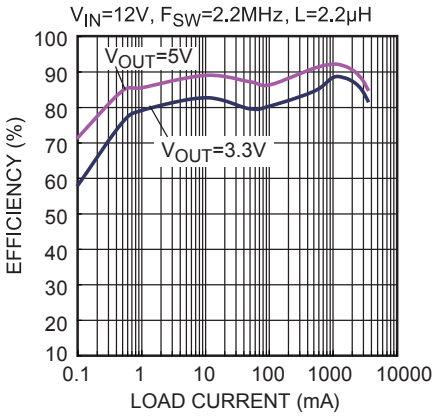
Efficiency vs. Load Current (Extreme Light Load)



Efficiency vs. Load Current (Extreme Light Load)



Efficiency vs. Load Current



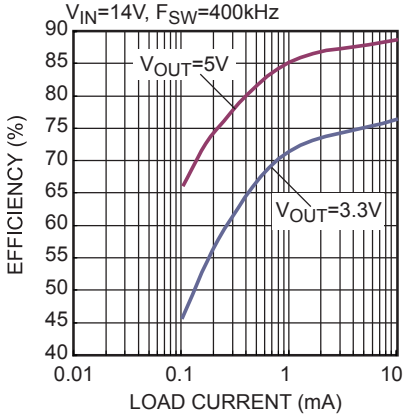
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

VIN = 12V, V_{OUT} = 3.3V, L = 10μH, f_{SW} = 500kHz, AAM, T_A = +25°C, unless otherwise noted.

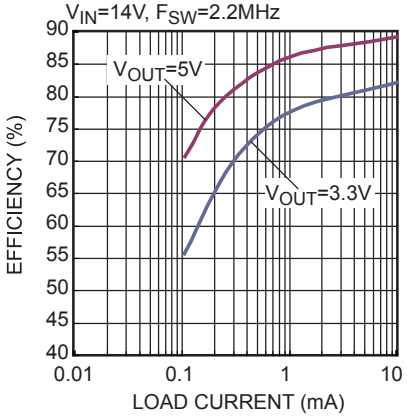
Efficiency vs. Load Current (Extreme Light Load)

V_{IN}=14V, F_{SW}=400kHz



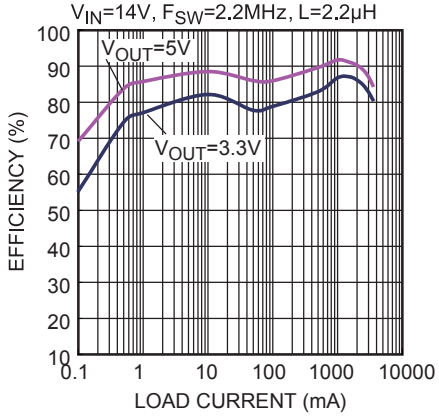
Efficiency vs. Load Current (Extreme Light Load)

V_{IN}=14V, F_{SW}=2.2MHz



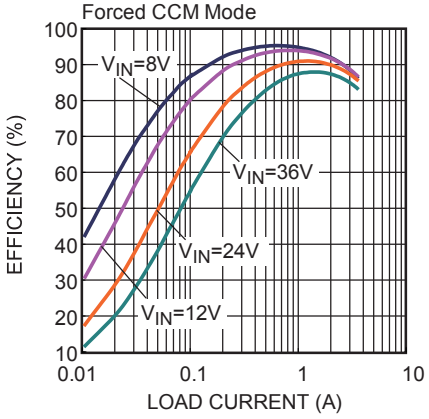
Efficiency vs. Load Current

V_{IN}=14V, F_{SW}=2.2MHz, L=2.2μH



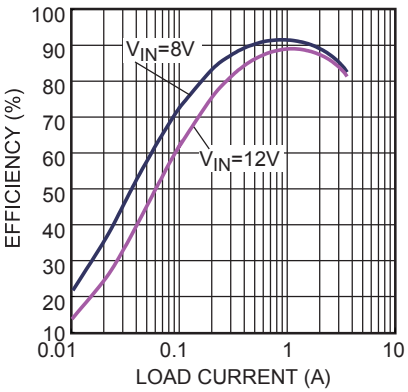
Efficiency vs. Load Current

V_{OUT}=3.3V, F_{SW}=500kHz, Forced CCM Mode



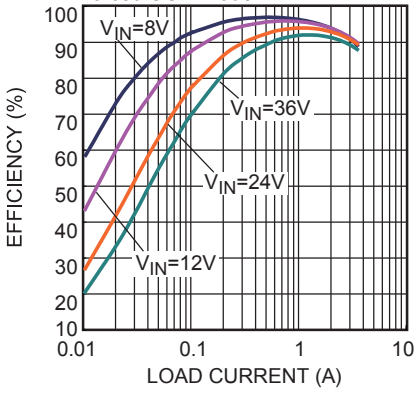
Efficiency vs. Load Current

V_{OUT}=3.3V, F_{SW}=2.2MHz, Forced CCM Mode



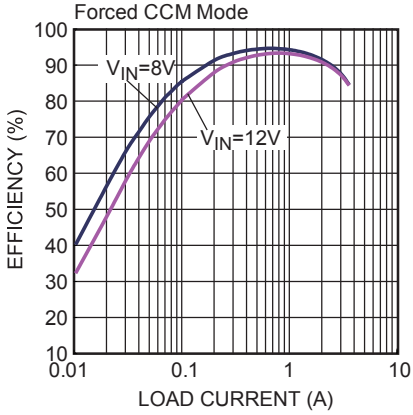
Efficiency vs. Load Current

V_{OUT}=5V, F_{SW}=500kHz, Forced CCM Mode



Efficiency vs. Load Current

V_{OUT}=5V, F_{SW}=2.2MHz, Forced CCM Mode

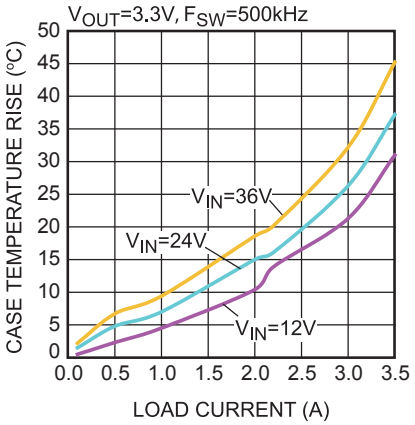


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

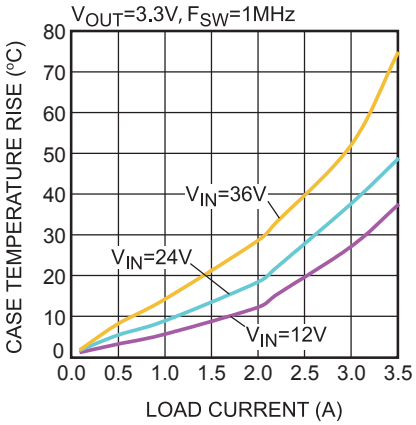
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

VIN = 12V, V_{OUT} = 3.3V, L = 10μH, f_{SW} = 500kHz, AAM, T_A = +25°C, unless otherwise noted.

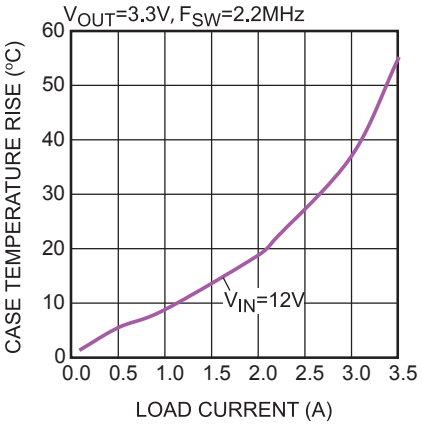
Case Temperature Rise vs. Load Current



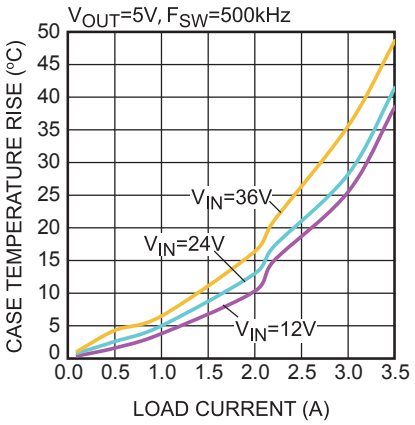
Case Temperature Rise vs. Load Current



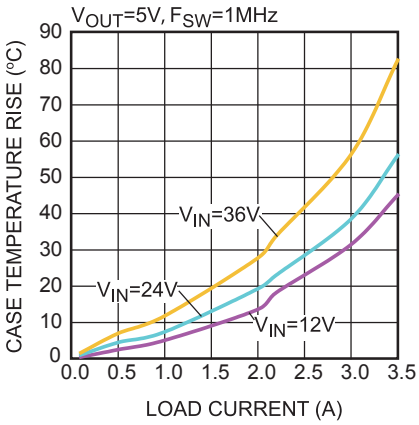
Case Temperature Rise vs. Load Current



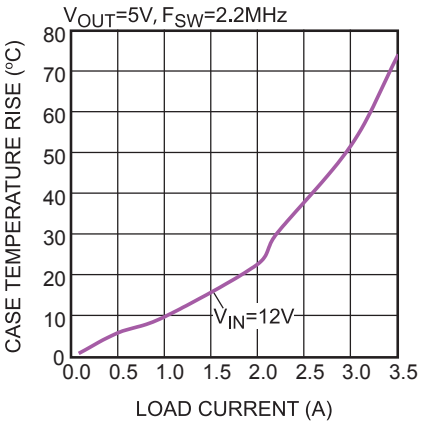
Case Temperature Rise vs. Load Current



Case Temperature Rise vs. Load Current



Case Temperature Rise vs. Load Current

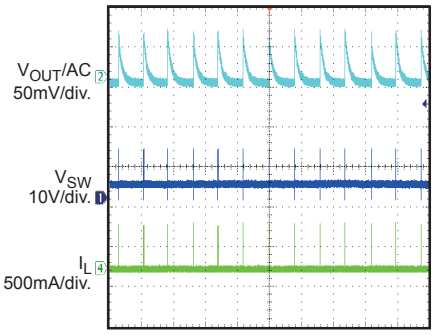


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

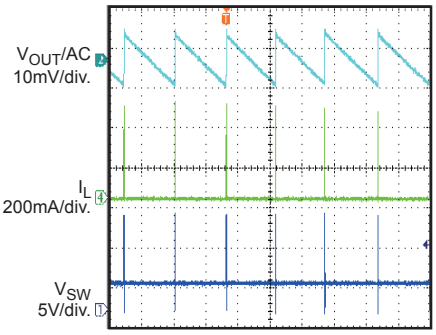
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

VIN = 12V, V_{OUT} = 3.3V, L = 10μH, f_{SW} = 500kHz, AAM, T_A = +25°C, unless otherwise noted.

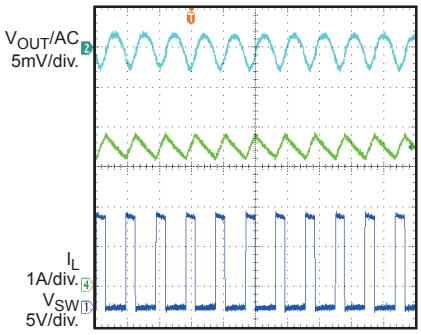
Steady State
I_{OUT}=0A, AAM Mode



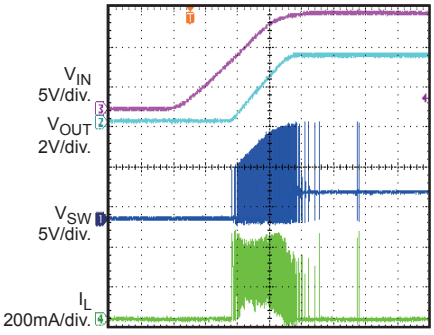
Steady State
I_{OUT}=1mA, AAM Mode



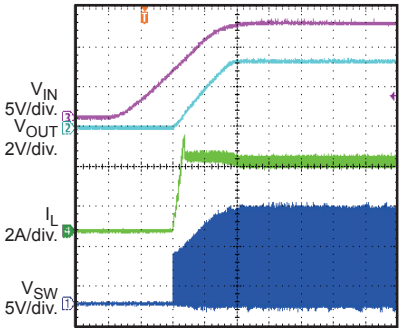
Steady State
I_{OUT}=3.5A



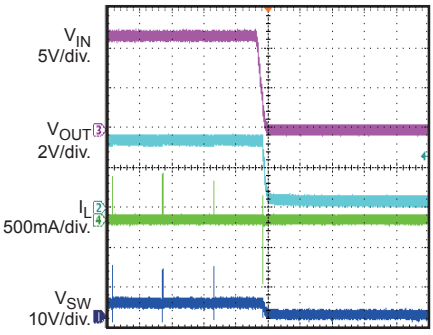
Start-Up through VIN
I_{OUT}=0A



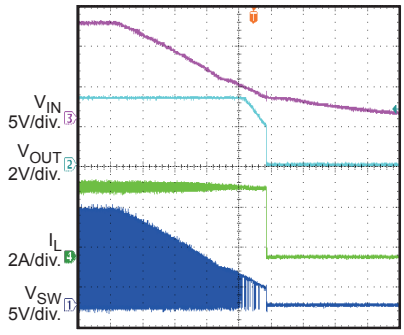
Start-Up through VIN
I_{OUT}=3.5A



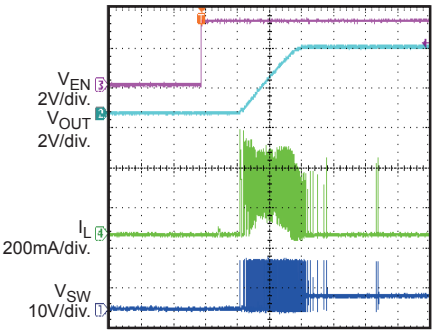
Shutdown through VIN
I_{OUT}=0A



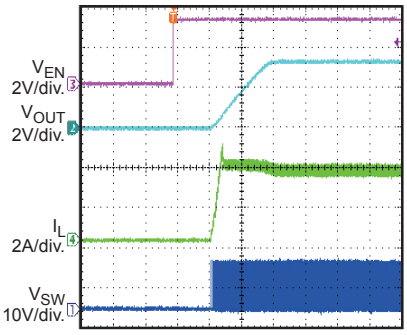
Shutdown through VIN
I_{OUT}=3.5A



Start-Up through EN
I_{OUT}=0A



Start-Up through EN
I_{OUT}=3.5A



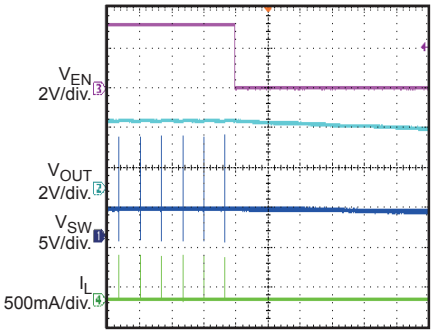
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

VIN = 12V, V_{OUT} = 3.3V, L = 10μH, f_{SW} = 500kHz, AAM, T_A = +25°C, unless otherwise noted.

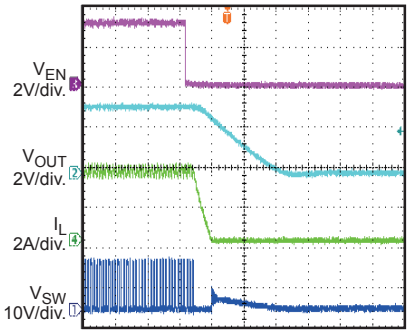
Shutdown through EN

I_{OUT}=0A



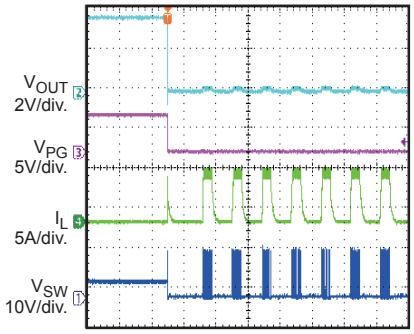
Shutdown through EN

I_{OUT}=3.5A



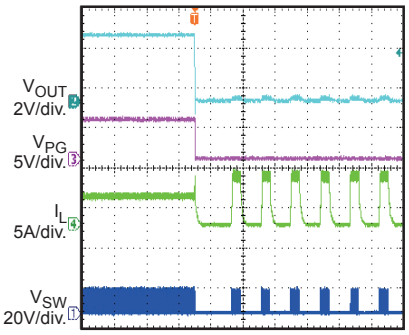
SCP Entry

I_{OUT}=0A to Short Circuit

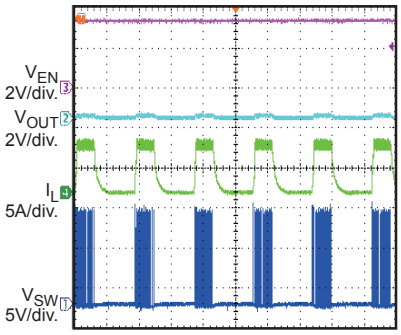


SCP Entry

I_{OUT}=3.5A to Short Circuit

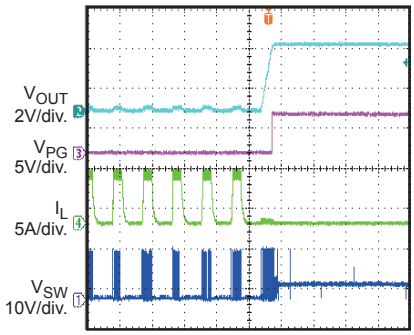


SCP Steady State



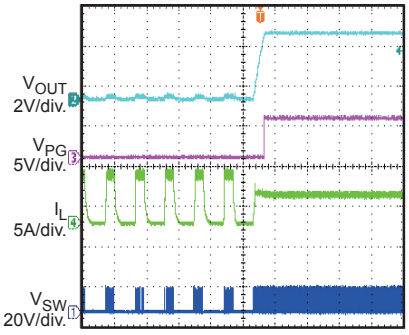
SCP Recovery

Short Circuit to I_{OUT}=0A



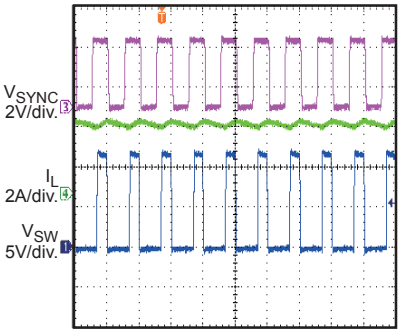
SCP Recovery

Short Circuit to I_{OUT}=3.5A



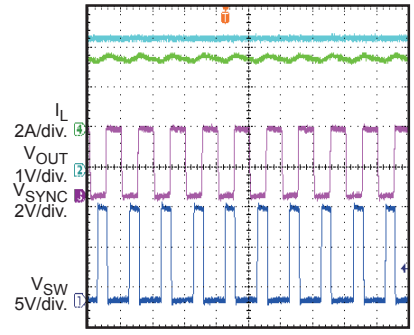
SYNC Operation (In-Phase)

Drive PHASE High, I_{OUT}=3.5A



SYNC Operation (180° Out-of-Phase)

Drive PHASE Low, I_{OUT}=3.5A



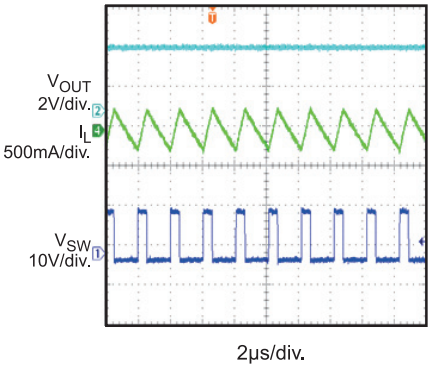
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

VIN = 12V, V_{OUT} = 3.3V, L = 10μH, f_{SW} = 500kHz, AAM, T_A = +25°C, unless otherwise noted.

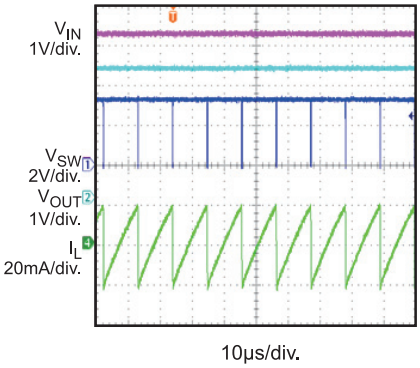
Forced CCM Operation

I_{OUT}=0A, Forced CCM Mode



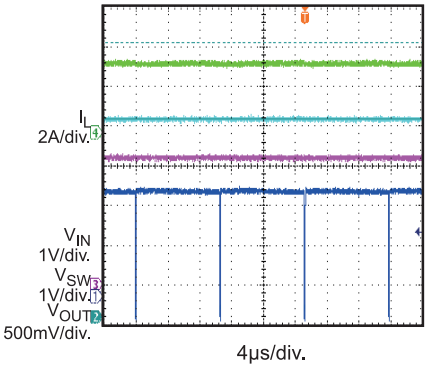
Dropout Operation

V_{IN}=3.3V, V_{OUT} Set to 3.3V, I_{OUT}=0A



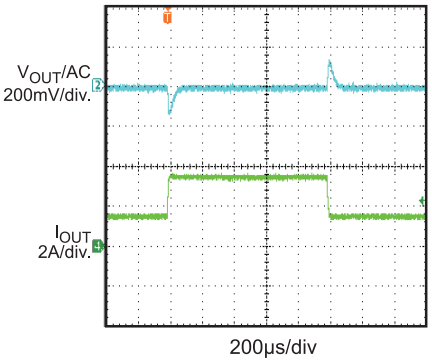
Dropout Operation

V_{IN}=3.3V, V_{OUT} Set to 3.3V, I_{OUT}=3.5A



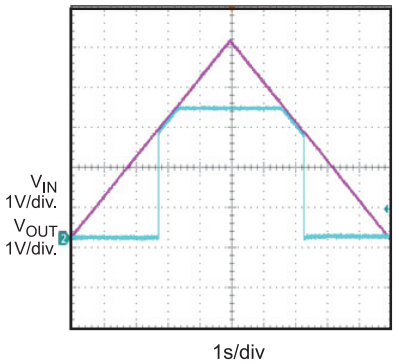
Load Transient

I_{OUT}=1.5A<->3.5A, 1.6A/μs



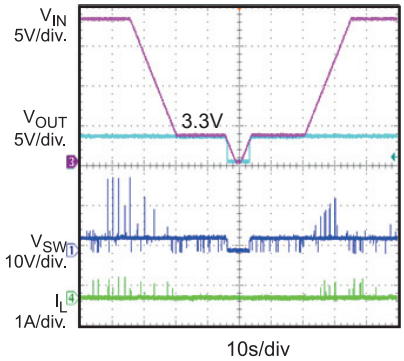
VIN Ramp Up and Down

I_{OUT}=0.1A



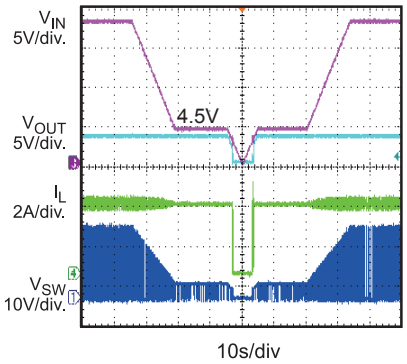
VIN Ramp Down and Up

I_{OUT}=1mA



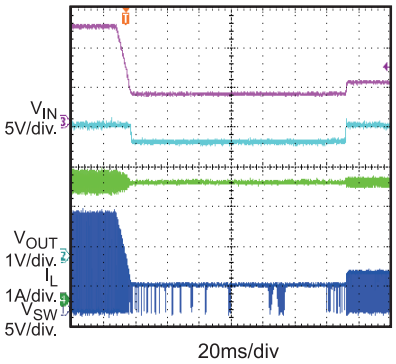
VIN Ramp Down and Up

I_{OUT}=3.5A



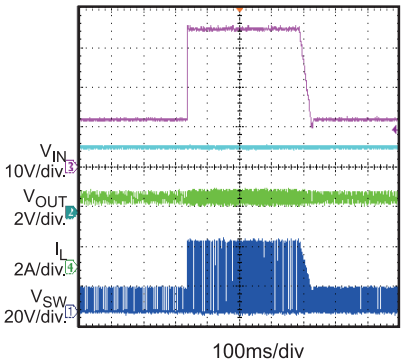
Cold Crank

V_{IN}=12V->3.3V->5V, I_{OUT}=3.5A



Load Dump

V_{IN}=12V<->36V, I_{OUT}=3.5A



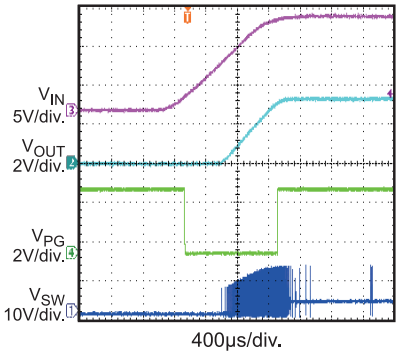
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

VIN = 12V, V_{OUT} = 3.3V, L = 10μH, f_{SW} = 500kHz, AAM, T_A = +25°C, unless otherwise noted.

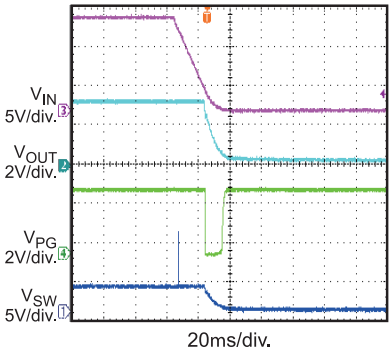
PG in Start-Up through VIN

I_{OUT} = 0A, PG is Pulled to 3.3V through 100k Resistor



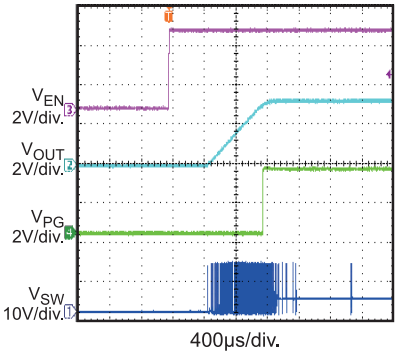
PG in Shutdown through VIN

I_{OUT} = 0A, PG is Pulled to 3.3V through 100k Resistor



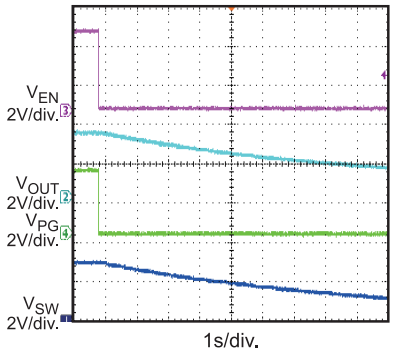
PG in Start-Up through EN

I_{OUT} = 0A, PG is Pulled to 3.3V through 100k Resistor



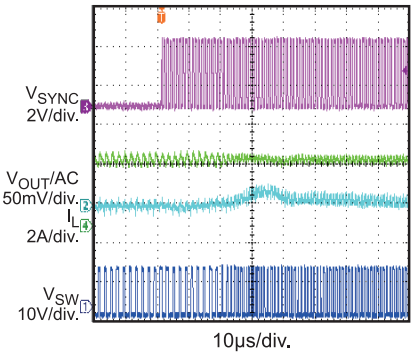
PG in Shutdown through EN

I_{OUT} = 0A, PG is Pulled to 3.3V through 100k Resistor



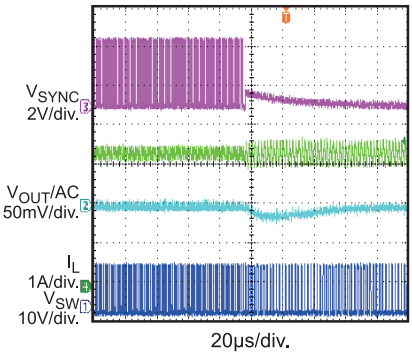
Sync In Transient

I_{OUT} = 3.5A, SYNC = 1MHz



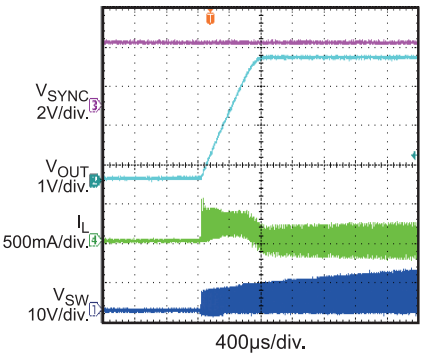
Sync Out Transient

I_{OUT} = 3.5A, SYNC = 1MHz



Forced CCM Entry

I_{OUT} = 0A, Pull Sync High before Startup



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

PIN FUNCTIONS

Pin #	Name	Description
1	PHASE	**Selectable in-phase or 180° out-of-phase of SYNC input.** Drive PHASE high to be in-phase. Drive PHASE low to be 180° out-of-phase. Recommend to connect this pin to GND if not used.
2	VIN	**Input supply.** VIN supplies power to all of the internal control circuitries and the power switch connected to SW. A decoupling capacitor to ground must be placed close to VIN to minimize switching spikes.
3, 10	SW	**Switch node.** SW is the output of the internal power switch. Pin 3 and Pin 10 are internally connected.
4, 9	PGND	**Power ground.** PGND is the reference ground of the power device and requires careful consideration during PCB layout. For best results, connect PGND with copper pours and vias.
5	EN	**Enable.** Pull EN below the specified threshold to shut the chip down. Pull EN above the specified threshold to enable the chip.
6	SYNC	**Synchronize.** Apply a 350kHz to 2.5MHz clock signal to SYNC to synchronize the internal oscillator frequency to the external clock. The external clock should be at least 250kHz larger than the R_{FREQ} set frequency. SYNC can also be used to select forced continuous conduction mode (CCM) or advanced asynchronous mode (AAM). Before the chip starts up, drive SYNC low or leave SYNC floating to choose AAM, and drive SYNC high to external power source or pull up SYNC to VCC directly to set the part forced CCM mode.
7	PG	**Power good indicator.** The output of PG is an open drain and goes high if the output voltage is within ±10% of the nominal voltage. Float PG if not used.
8	BIAS	**External power supply for the internal regulator.** Connect BIAS to an external power supply (5V ≤ V_{BIAS} ≤ 18V) to reduce power dissipation and increase efficiency. Float BIAS or connect BIAS to ground if not used.
11	BST	**Bootstrap.** BST is the positive power supply of the high-side MOSFET driver connected to SW. Connect a bypass capacitor between BST and SW.
12	VCC	**Internal bias supply.** VCC supplies power to the internal control circuit and gate drivers. A ≥1μF decoupling capacitor to ground is required close to VCC.
13	AGND	**Analog ground.** AGND is the reference ground of the logic circuit.
14	SS	**Soft-start input.** Place an external capacitor from SS to AGND to set the soft-start period. The MPQ4430 sources 10μA from SS to the soft-start capacitor during start-up. As the SS voltage rises, the feedback threshold voltage increases to limit inrush current during start-up. Floating the PIN will activate the internal 0.7ms soft-tart setting.
15	FB	**Feedback input.** For adjustable output version, connect FB to the tap of an external resistor divider from the output to AGND to set the output voltage. The feedback threshold voltage is 0.8V. Place the resistor divider as close to FB as possible. Avoid placing vias on the FB traces. For fixed output version, connect FB pin to the output directly.
16	FREQ	**Switching frequency program.** Connect a resistor from FREQ to ground to set the switching frequency.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

BLOCK DIAGRAM

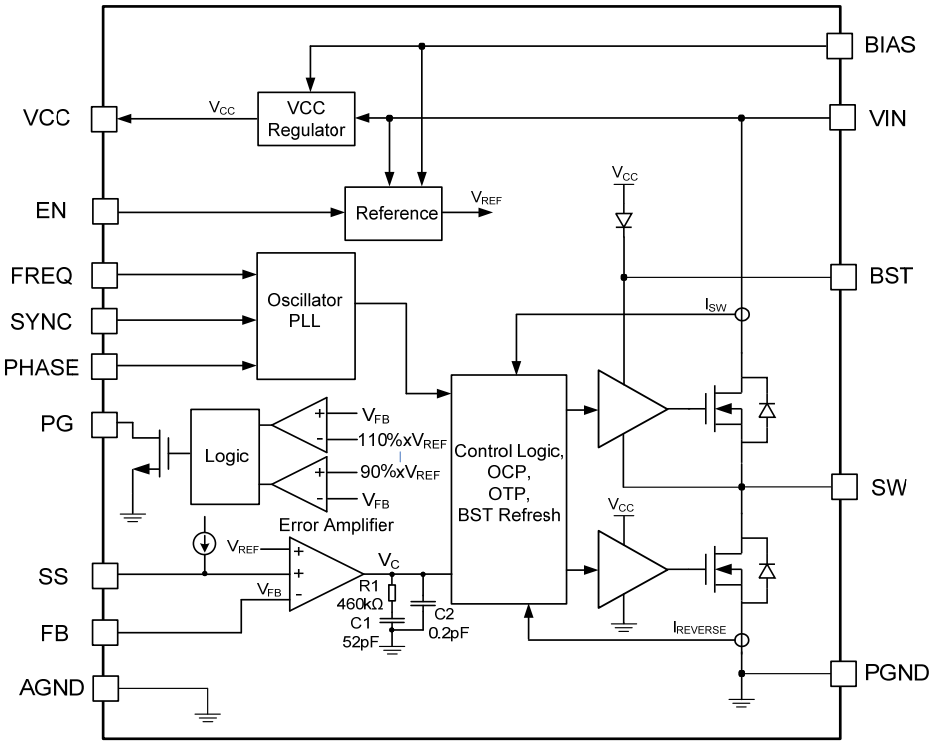


Figure 1-1: Functional Block Diagram of Output Adjustable Version

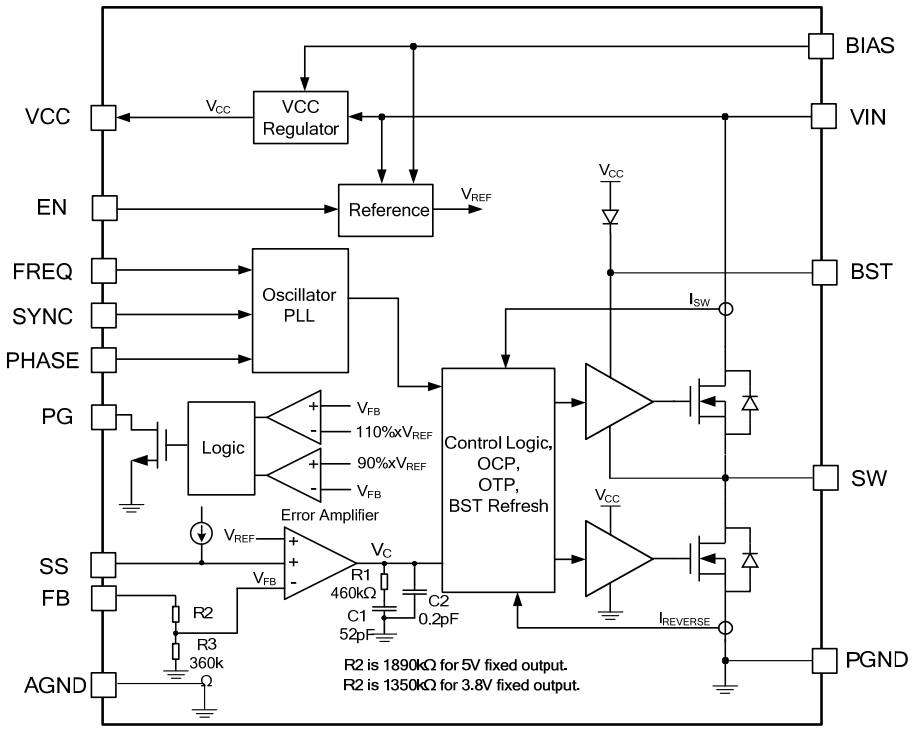


Figure 1-2: Functional Block Diagram of Fixed Output Version

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

TIMING SEQUENCE

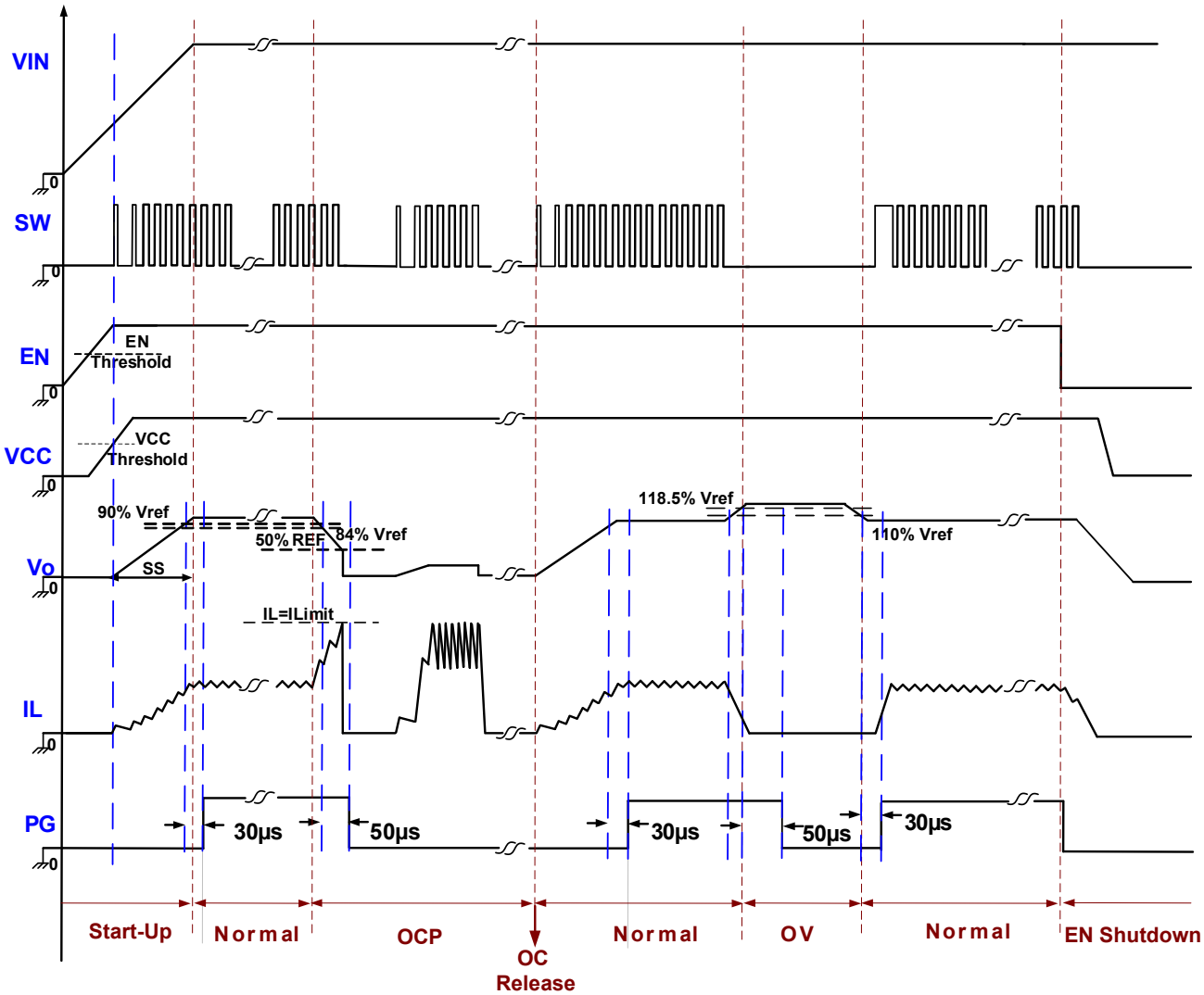


Figure 2: Time Sequence

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

OPERATION

The MPQ4430 is a high-frequency, synchronous, rectified, step-down, switch-mode converter with integrated internal high-side and low-side power MOSFETs. The MPQ4430 offers a very compact solution that achieves 3.5A of continuous output current with excellent load and line regulation over a wide 3.3V to 36V input supply range.

The MPQ4430 features a switching frequency programmable from 350kHz to 2.5MHz, external soft start, power good indication, and precision current limit. Its very low operational quiescent current makes it suitable for battery-powered applications.

Pulse-Width Modulation (PWM) Control

At moderate to high output current, the MPQ4430 operates in a fixed-frequency, peak-current-control mode to regulate the output voltage. An internal clock initiates a pulse-width modulation (PWM) cycle. At the rising edge of the clock, the high-side power MOSFET (HS-FET) is turned on, and the inductor current rises linearly to provide energy to the load. The HS-FET remains on until its current reaches the value set by the COMP voltage (V_{COMP}), which is the output of the internal error amplifier. If in one PWM period, the current in the HS-FET does not reach V_{COMP}, the HS-FET remains on, saving a turn-off operation.

When the HS-FET is off, it remains off until the next clock cycle begins. The low-side MOSFET (LS-FET) is turned on immediately while the inductor current flows through it.

To prevent shoot-through, a dead time is inserted to prevent the HS-FET and LS-FET from being on at the same time. For each turn-on and -off in a switching cycle, the HS-FET turns on or off with minimum on and off time limit.

Forced CCM and AAM

The MPQ4430 has selectable forced continuous conduction mode (CCM) and advanced asynchronous mode (AAM) (see Figure 3). Driving SYNC higher than its specified threshold (1.8V) before the chip starts up forces the device into CCM with a fixed frequency regardless of the output load current.

Once the device is in CCM, SYNC can be pulled low again, or with an external clock if needed. The advantage of CCM is the controllable frequency and smaller output ripple, but it also has low efficiency at light load.

Driving SYNC below its specified threshold (0.4V) or leaving SYNC floating before the chip starts up enables AAM power-save mode. The MPQ4430 first enters non-synchronous operation for as long as the inductor current approaches zero at light load. If the load is further decreased or is at no load, then V_{COMP} is below the internally set AAM value (V_{AAM}). The MPQ4430 then enters sleep mode, which consumes very low quiescent current to further improve light-load efficiency.

In sleep mode, the internal clock is blocked first, so the MPQ4430 skips some pulses. Since the FB voltage (V_{FB}) is lower than the internal 0.8V reference (V_{REF}) at this time, V_{COMP} ramps up until it crosses over V_{AAM}. Then the internal clock is reset, and the crossover time is taken as the benchmark of the next clock. This control scheme helps achieve high efficiency by scaling down the frequency to reduce switching and gate driver losses during light-load or no-load conditions.

When the output current increases from light-load condition, V_{COMP} becomes larger, and the switching frequency increases. If the DC value of V_{COMP} exceeds V_{AAM}, the operation mode resumes DCM or CCM, which have a constant switching frequency.

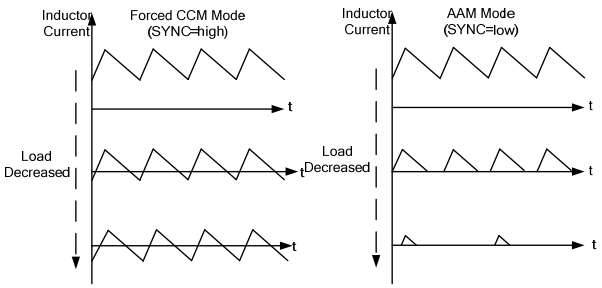


Figure 3 : Forced CCM and AAM

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

Error Amplifier (EA)

The error amplifier compares V_{FB} with V_{REF} and outputs a current proportional to the difference between the two. This output current then charges or discharges the internal compensation network to form V_{COMP}, which controls the power MOSFET current. The optimized internal compensation network minimizes the external component count and simplifies the control loop design.

Internal Regulator and BIAS

Most of the internal circuitry is powered on by the 5V internal regulator. This regulator takes the VIN input and operates in the full VIN range. When VIN exceeds 5V, the output of the regulator is in full regulation. When VIN falls below 5V, the output decreases following VIN. A decoupling ceramic capacitor is needed close to VCC.

For better thermal performance, connect BIAS to an external power supply between 5V and 18V. The BIAS supply overrides VIN to power the internal regulator. Using the BIAS supply allows VCC to be derived from a high-efficiency external source, such as V_{OUT}. Float BIAS or connect BIAS to ground if not used.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The UVLO comparator monitors the output voltage of the internal regulator (VCC). The UVLO rising threshold is about 2.8V with a 150mV hysteresis.

Enable Control (EN)

EN is a digital control pin that turns the regulator on and off. When EN is pulled below its threshold voltage, the chip is put into the lowest shutdown current mode. Pulling EN above its threshold voltage turns on the part. Do not float EN.

Power Good Indicator (PG)

The MPQ4430 has a power good (PG) indicator. PG is the open drain of a MOSFET and should be connected to VCC or another voltage source through a resistor (e.g.: 100kΩ). In the presence of an input voltage, the MOSFET turns on so that PG is pulled low before SS is ready. When the regulator output is within ±10% of its nominal output, the PG output is pulled high after a delay, typically 30μs. When the output voltage moves outside of this range with a hysteresis, the PG output is pulled low with a 50μs delay to indicate a failure output status.

Programmable Frequency

The oscillating frequency of the MPQ4430 can be programmed either by an external frequency resistor (R_{FREQ}) or by a logic level synchronous clock. The frequency resistor should be located between FREQ and ground as close as to the device as possible.

The value of R_{FREQ} can be estimated with Equation (1):

$$R_{FREQ}(k\Omega) = \frac{170000}{f_{SW}^{1.11}(kHz)} \quad (1)$$

The calculated resistance may need fine-tuning during the bench test.

FREQ is not allowed to be floated even if an external SYNC clock is added.

SYNC and PHASE

The internal oscillator frequency can be synchronized to an external clock ranging from 350kHz up to 2.5MHz through SYNC. The external clock should be at least 250kHz larger than the R_{FREQ} set frequency. Ensure that the high amplitude of the SYNC clock is higher than 1.8V, and the low amplitude is lower than 0.4V. There is no pulse width requirement, but there is always parasitic capacitance of the pad, so if the pulse width is too short, a clear rising and falling edge may not be seen due to the parasitic capacitance. A pulse longer than 100ns is recommended in application.

PHASE is used when two or more MPQ4430 devices are in parallel with the same SYNC clock. Pulling PHASE high forces the device to operate in-phase of the SYNC clock. Pulling it low forces the device to be 180° out-of-phase of the SYNC clock. By setting different voltages for PHASE, two devices can operate 180° out-of-phase to reduce the total input current ripple so a smaller input bypass capacitor can be used (see Figure 4). The PHASE rising threshold is about 2.5V with a 400mV hysteresis.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

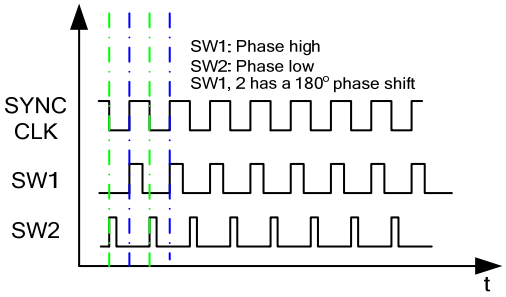


Figure 4 : In-Phase and 180° Out-of-Phase

Soft Start (SS)

Soft start (SS) is implemented to prevent the converter output voltage from overshooting during start-up. When the chip starts up, an internal current source begins charging the external soft-start capacitor. The internal SS voltage (V_{SSI}) rises with the soft-start voltage (V_{SS}), but V_{SSI} is a little different with V_{SS} due to a 0.5V offset and some delay. When V_{SS} is lower than 0.5V, V_{SSI} is 0V. V_{SSI} rises from 0V to 0.8V during the period of V_{SS} rises from 0.5V to 1.6V. At this time the error amplifier uses V_{SSI} as the reference, and the output voltage ramps up from 0V to the regulated value following V_{SSI} rising. When V_{SS} reaches 1.6V, V_{SSI} is 0.8V and overrides the internal V_{REF}, so the error amplifier uses the internal V_{REF} as the reference.

The soft-start time (t_{SS}) set by the external SS capacitor can be calculated with Equation (2):

$$t_{SS}(ms) = \frac{C_{SS}(nF) \times 1.1V}{I_{SS}(\mu A)} \quad (2)$$

Where C_{SS} is the external SS capacitor, and I_{SS} is the internal 10μA SS charge current. There is also an internal 0.7ms soft start when SS PIN float, the final SS time is determined by the longer time between 0.7ms and external SS setting time.

SS can be used for tracking and sequencing.

Pre-Bias Start-Up

At start-up, if V_{FB} is higher than V_{SSI}-155mV, which means the output has a pre-bias voltage, neither the HS-FET nor the LS-FET are turned on until V_{SSI}-155mV is higher than V_{FB}.

Over-Current Protection (OCP) and Hiccup

The MPQ4430 has cycle-by-cycle peak current-limit protection with valley-current detection and hiccup mode.

The power MOSFET current is accurately sensed via a current sense MOSFET. It is then fed to the high-speed current comparator for current-mode control purposes. During the HS-FET on state, if the sensed current exceeds the peak-current limit value set by the COMP high-clamp voltage, the HS-FET turns off immediately. Then the LS-FET turns on to discharge the energy, and the inductor current decreases. The HS-FET remains off unless the inductor valley current is lower than a certain current threshold (the valley current limit), even though the internal clock pulses high. If the inductor current does not drop below the valley current limit when the internal clock pulses high, the HS-FET misses the clock, and the switching frequency decreases to half the nominal value. Both the peak and valley current limits assist in keeping the inductor current from running away during an overload or short-circuit condition.

When the output is shorted to ground, causing the output voltage to drop below 55% of its nominal output, the peak current limit is kicked, and the device considers this to be an output dead short and triggers hiccup mode immediately to restart the part periodically.

In hiccup mode, the MPQ4430 disables its output power stage and discharges the soft-start capacitor slowly. The MPQ4430 restarts with a full soft-start when the soft-start capacitor is fully discharged. If the short-circuit condition still remains after the soft start ends, the device repeats this operation until the fault is removed and output returns to the regulation level. This protection mode reduces the average short circuit current greatly to alleviate thermal issues and protect the regulator.

Floating Driver and Bootstrap Charging

A 0.1μF to 1μF external bootstrap capacitor powers the floating power MOSFET driver. The floating driver has its own UVLO protection with a rising threshold of 2.5V and hysteresis of 200mV.

The bootstrap capacitor voltage is charged to ~5V from VCC through a PMOS pass transistor when the LS-FET is on.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

At a high duty cycle operation or sleep mode condition, the time period available to the bootstrap charging is less, so the bootstrap capacitor may not be charged sufficiently. In case the external circuit does not have sufficient voltage or time to charge the bootstrap capacitor, extra external circuitry can be used to ensure that the bootstrap voltage is in the normal operation region.

BST Refresh

To improve dropout, the MPQ4430 is designed to operate at close to 100% duty cycle for as long as the BST to SW voltage is greater than 2.5V. When the voltage from BST to SW drops below 2.5V, the HS-FET is turned off using a UVLO circuit, which forces the LS-FET on to refresh the charge on the BST capacitor.

Since the supply current sourced from the BST capacitor is low, the HS-FET can remain on for more switching cycles than are required to refresh the capacitor, making the effective duty cycle of the switching regulator high.

The effective duty cycle during the dropout of the regulator is mainly influenced by the voltage drops across the HS-FET, LS-FET, inductor resistance, and printed circuit board resistance.

In low dropout mode, the COMP is high clamped; when VIN fast rising, the COMP need time to jump out high clamped condition, which may generate overshoot on V_{OUT}; Adjusting the loop response faster and with bigger C_{OUT} capacitance can help improve the overshoot.

Thermal Shutdown

Thermal shutdown is implemented to prevent the chip from running away thermally. When the silicon die temperature exceeds its upper threshold, the power MOSFETs shut down. When the temperature drops below its lower threshold, the chip is enabled again.

Start-Up and Shutdown

If both VIN and EN exceed their appropriate thresholds, the chip starts up. The reference block starts first, generating a stable reference voltage and current, and then the internal regulator is enabled. The regulator provides a stable supply for the rest of the circuitries.

While the internal supply rail is up, an internal timer holds the power MOSFET off for about 50μs to blank start-up glitches. When the soft-start block is enabled, it first holds its SS output low to ensure that the rest of the circuitries are ready and slowly ramps up.

Three events can shut down the chip: VIN low, EN low, and thermal shutdown. During the shutdown procedure, the signaling path is blocked first to avoid any fault triggering. V_{COMP} and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command, but its charging path is disabled.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

APPLICATION INFORMATION

Setting the Output Voltage

For adjustable output version, the external resistor divider connected to FB sets the output voltage (see Figure 5).

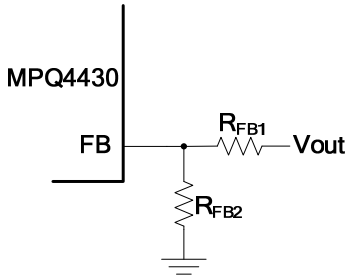


Figure 5: Feedback Network

Choose R_{FB1} first, then calculate R_{FB2} with Equation (3):

$$R_{FB2} = \frac{R_{FB1}}{\frac{V_{OUT}}{0.8V} - 1} \quad (3)$$

Table 1 lists the recommended feedback resistor values for common output voltages.

Table 1: Resistor Selection for Common Output Voltages

V_{OUT} (V)	R_{FB1} (kΩ)	R_{FB2} (kΩ)
3.3	41.2 (1%)	13 (1%)
5	68.1 (1%)	13 (1%)

For fixed output version, connect FB pin to the output directly.

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current to the converter while maintaining the DC input voltage. For the best performance, use low ESR capacitors. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients.

For most applications, use a 4.7μF to 10μF capacitor. It is strongly recommended to use another lower-value capacitor (e.g.: 0.1μF) with a small package size (0603) to absorb high-frequency switching noise. Place the smaller capacitor as close to VIN and GND as possible.

Since C_{IN} absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (4):

$$I_{CIN} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (4)$$

The worst-case condition occurs at VIN = $2V_{OUT}$, shown in Equation (5):

$$I_{CIN} = \frac{I_{LOAD}}{2} \quad (5)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g.: 0.1μF) as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple caused by the capacitance can be estimated with Equation (6):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (6)$$

Selecting the Output Capacitor

The output capacitor maintains the DC output voltage. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For best results, use low ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \cdot (1 - \frac{V_{OUT}}{V_{IN}}) \cdot (R_{ESR} + \frac{1}{8 f_{SW} \times C_{OUT}}) \quad (7)$$

Where L is the inductor value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes the majority of the output voltage ripple.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

For simplification, the output voltage ripple can be estimated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (8)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (9)$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MPQ4430 can be optimized for a wide range of capacitance and ESR values.

Selecting the Inductor

A 1μH to 10μH inductor with a DC current rating at least 25% higher than the maximum load current is recommended for most applications. For higher efficiency, choose an inductor with a lower DC resistance. A larger-value inductor results in less ripple current and a lower output ripple voltage, but also has a larger physical size, higher series resistance, and lower saturation current. A good rule for determining the inductor value is to allow the inductor ripple current to be approximately 30% of the maximum load current. The inductance value can then be calculated with Equation (10):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (10)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current can be calculated with Equation (11):

$$I_{LP} = I_{LOAD} + \frac{V_{OUT}}{2 f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (11)$$

VIN UVLO Setting

The MPQ4430 has an internal fixed under-voltage lockout (UVLO) threshold. The rising threshold is 2.8V, while the falling threshold is about 2.65V. For the applications that need a higher UVLO point, an external resistor divider between VIN and EN can be used to achieve a higher equivalent UVLO threshold (see Figure 6).

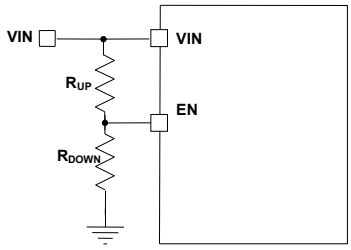


Figure 6: Adjustable UVLO Using EN Divider

The UVLO threshold can be calculated with Equation (12) and Equation (13):

$$INUV_{RISING} = (1 + \frac{R_{UP}}{R_{DOWN}}) \times V_{EN_RISING} \quad (12)$$

$$INUV_{FALLING} = (1 + \frac{R_{UP}}{R_{DOWN}}) \times V_{EN_FALLING} \quad (13)$$

Where V_{EN_RISING} is 1.05V, and $V_{EN_FALLING}$ is 0.93V.

External BST Diode and Resistor

An external BST diode can enhance the efficiency of the regulator when the duty cycle is high. A power supply between 2.5V and 5V can be used to power the external bootstrap diode. VCC or V_{OUT} is recommended to be this power supply in the circuit (see Figure 7).

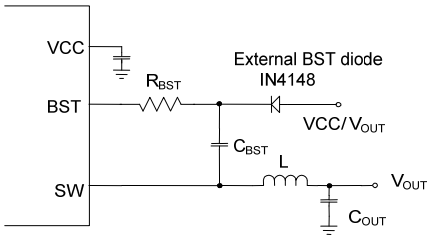


Figure 7: Optional External Bootstrap Diode to Enhance Efficiency

The recommended external BST diode is IN4148, and the recommended BST capacitor value is 0.1μF to 1μF. A resistor in series with the BST capacitor (R_{BST}) can reduce the SW rising rate and voltage spikes. This helps enhance EMI performance and reduce voltage stress at a high VIN. A higher resistance is better for SW spike reduction but compromises efficiency. To make a tradeoff between EMI and efficiency, a ≤20Ω R_{BST} is recommended.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

Hot-Plug Application

In a hot-plug application, the VIN pin of the IC may turn on and off frequently before the power supply can establish a connection with the IC. In applications where the input power turns on and off frequently, the BST capacitor may have a residual voltage when the IC is turned on. This may turn on high-side MOSFET (HS-FET) for a short time before VCC can rise high enough, which causes an unexpected overshoot on VOUT.

To protect the IC, hot-plug applications are not recommended. If a hot-plug application must be initiated, use a small BST capacitor (e.g. 47nF), a large VCC capacitor (e.g. 4.7μF), and a large PG resistor (e.g. 1MΩ) to reduce the overshoot risk. Contact an MPS FAE to confirm the design.

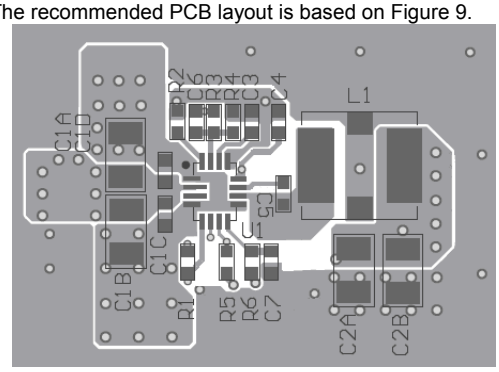
PCB Layout Guidelines [8]

Efficient PCB layout, especially for input capacitor placement, is critical for stable operation. A four-layer layout is strongly recommended to achieve better thermal performance. For best results, refer to Figure 8 and follow the guidelines below.

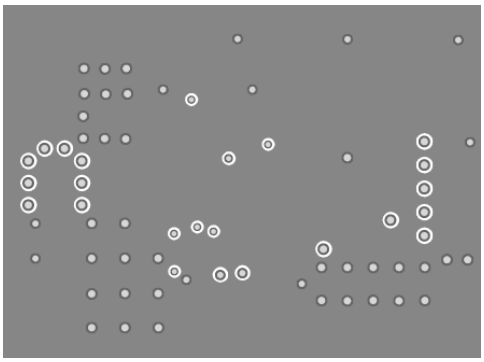
1. Place symmetric input capacitors as close to VIN and GND as possible. Recommend to connect pin1 to GND for symmetric input structure if in-phase not used. Pin3 and pin10 are internally connected. Connecting together on layout or not are both OK. Recommend to leave pin3 floating for shorter pin4 and pin1 trace and smaller input hot loop.
2. Use a large ground plane to connect to PGND directly.
3. Add vias near PGND if the bottom layer is a ground plane.
4. Ensure that the high-current paths at GND and VIN have short, direct, and wide traces.
5. Place the ceramic input capacitor, especially the small package size (0603) input bypass capacitor, as close to VIN and PGND as possible to minimize high-frequency noise.
6. Keep the connection of the input capacitor and VIN as short and wide as possible.
7. Place the VCC capacitor as close to VCC and GND as possible.
8. Route SW and BST away from sensitive analog areas, such as FB.
9. Place the feedback resistors close to the chip to ensure that the trace which connects to FB is as short as possible.
10. Use multiple vias to connect the power planes to the internal layers.

NOTE:

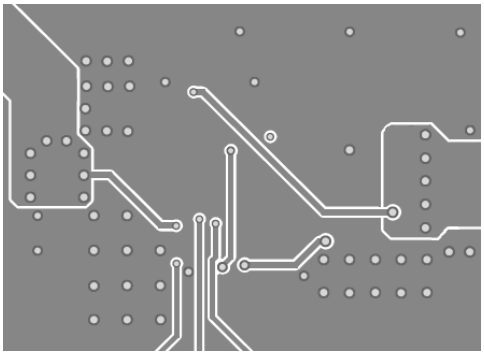
8) The recommended PCB layout is based on Figure 9.



Top Layer

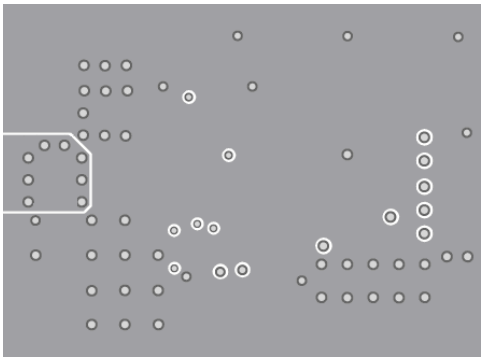


Inner Layer 1



Inner Layer 2

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.



Bottom Layer
Figure 8: Recommended PCB Layout

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

TYPICAL APPLICATION CIRCUITS

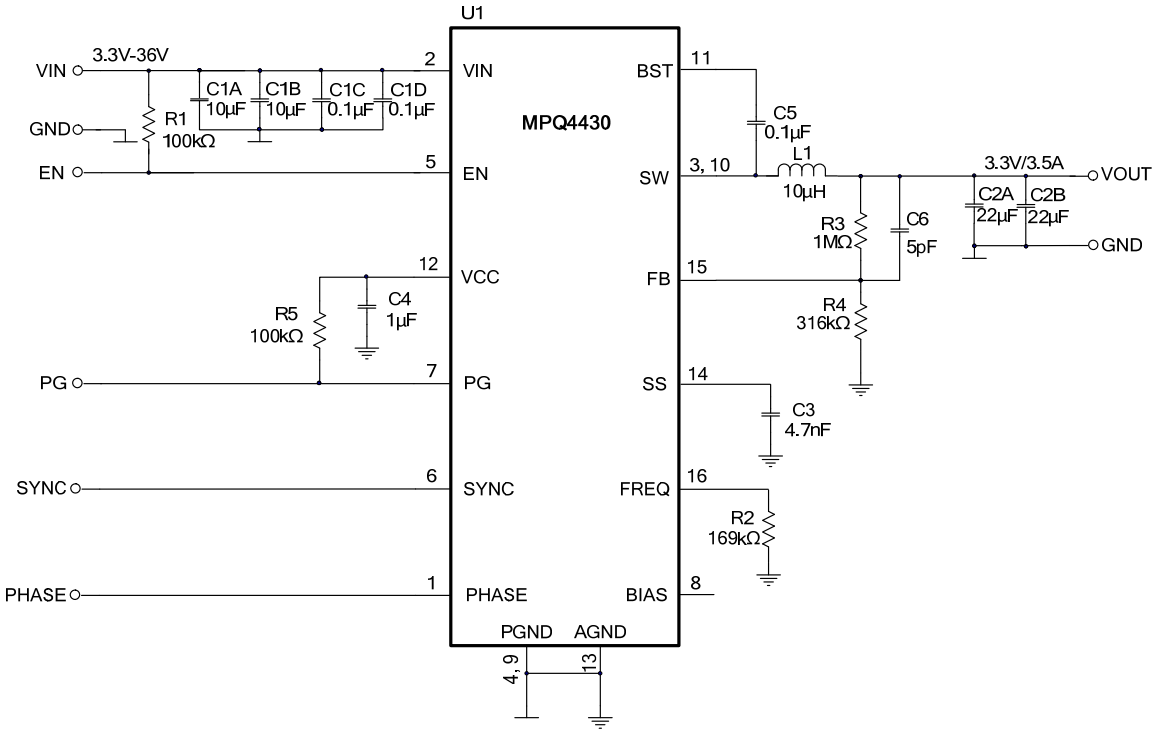


Figure 9: V_{OUT} = 3.3V, f_{SW} = 500kHz

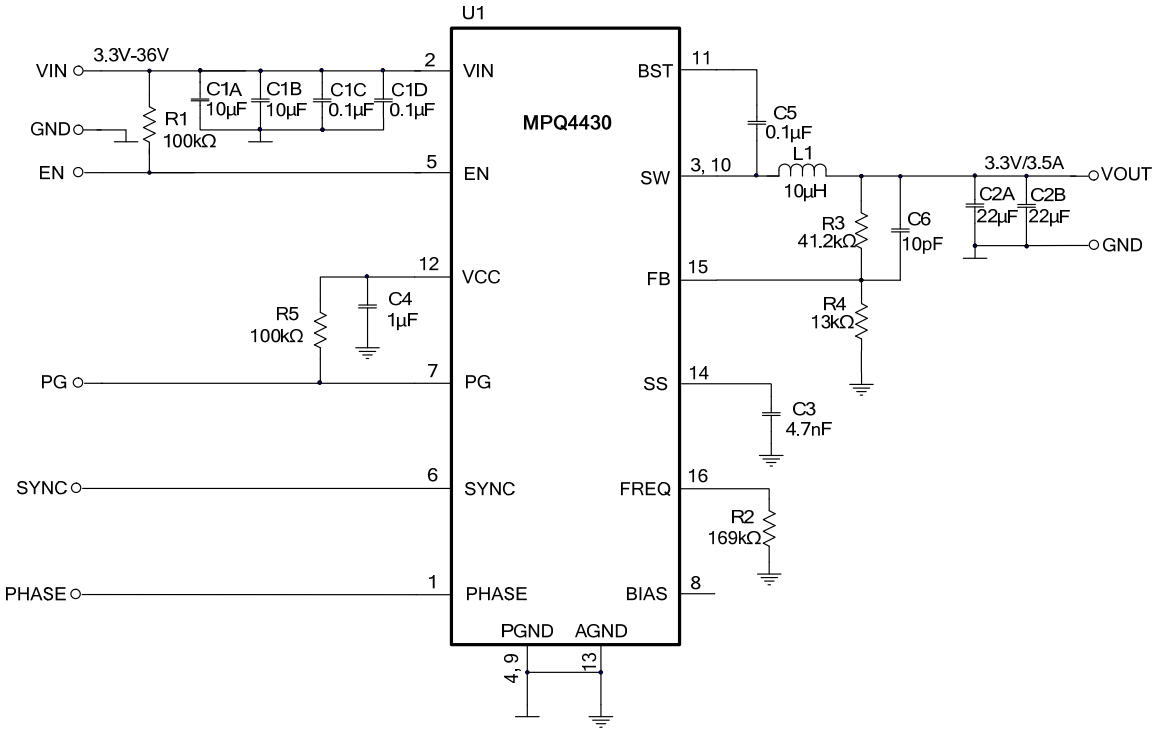


Figure 10: V_{OUT} = 3.3V, f_{SW} = 500kHz for <100kΩ FB Divider Application

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

TYPICAL APPLICATION CIRCUITS *(continued)*

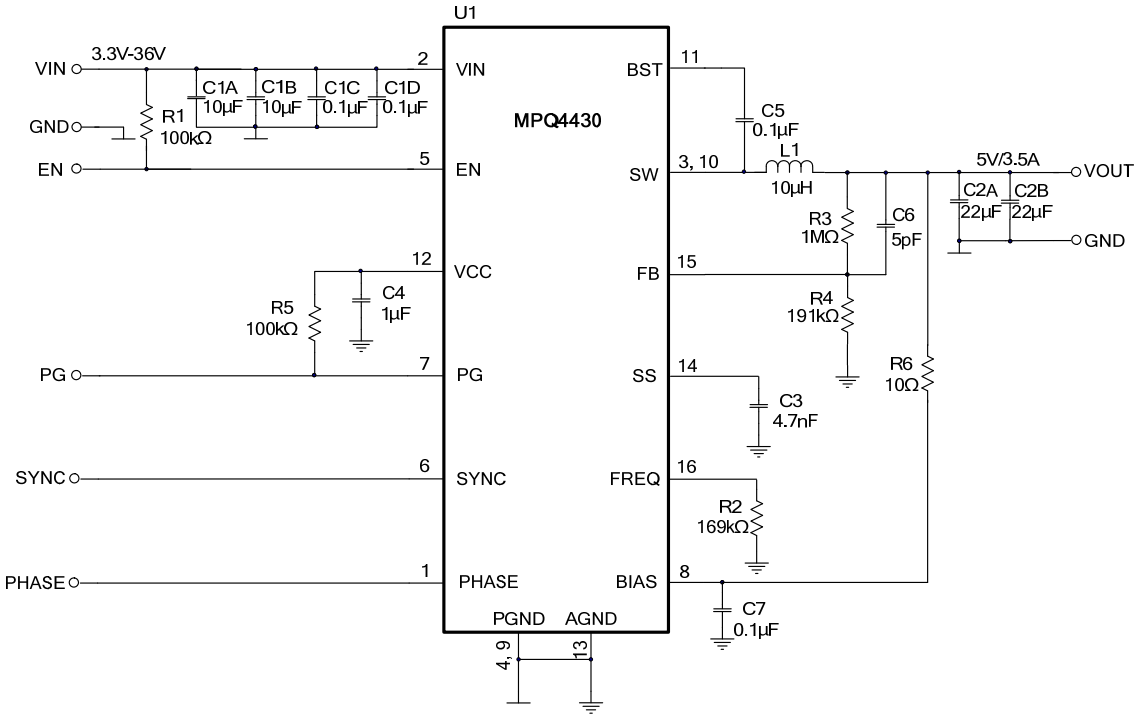


Figure 11: V_{OUT} = 5V, f_{SW} = 500kHz

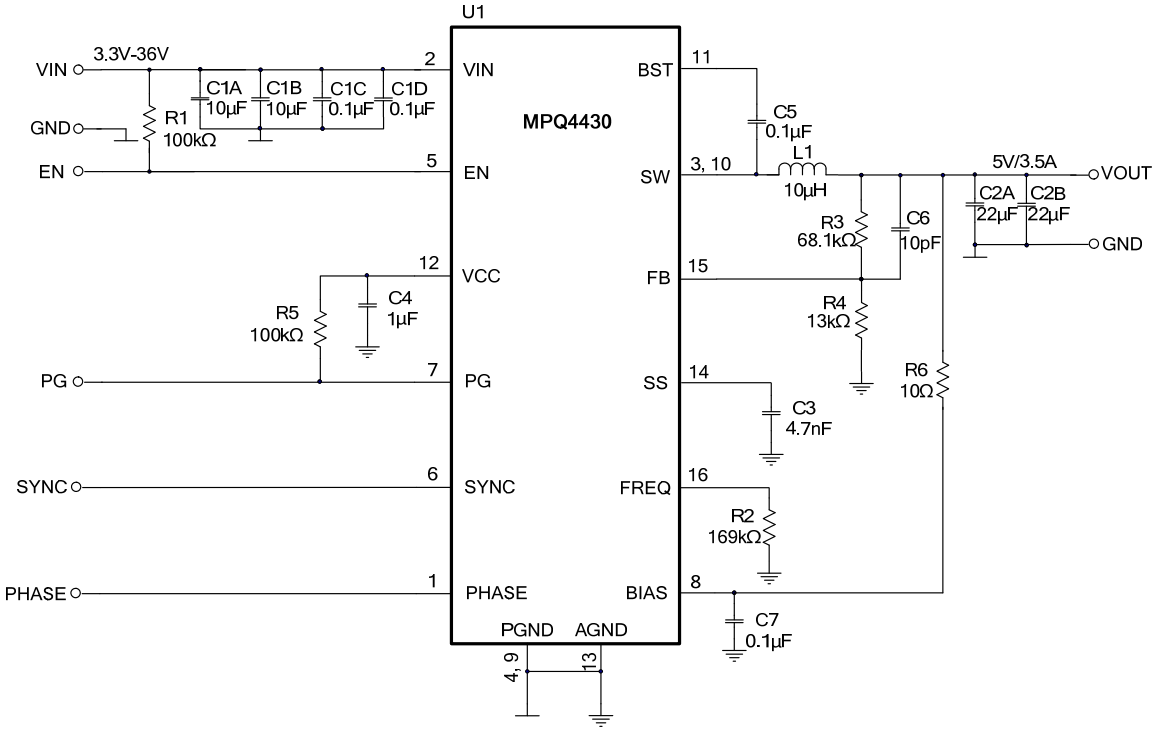


Figure 12: V_{OUT} = 5V, f_{SW} = 500kHz for <100kΩ FB Divider Application

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

TYPICAL APPLICATION CIRCUITS *(continued)*

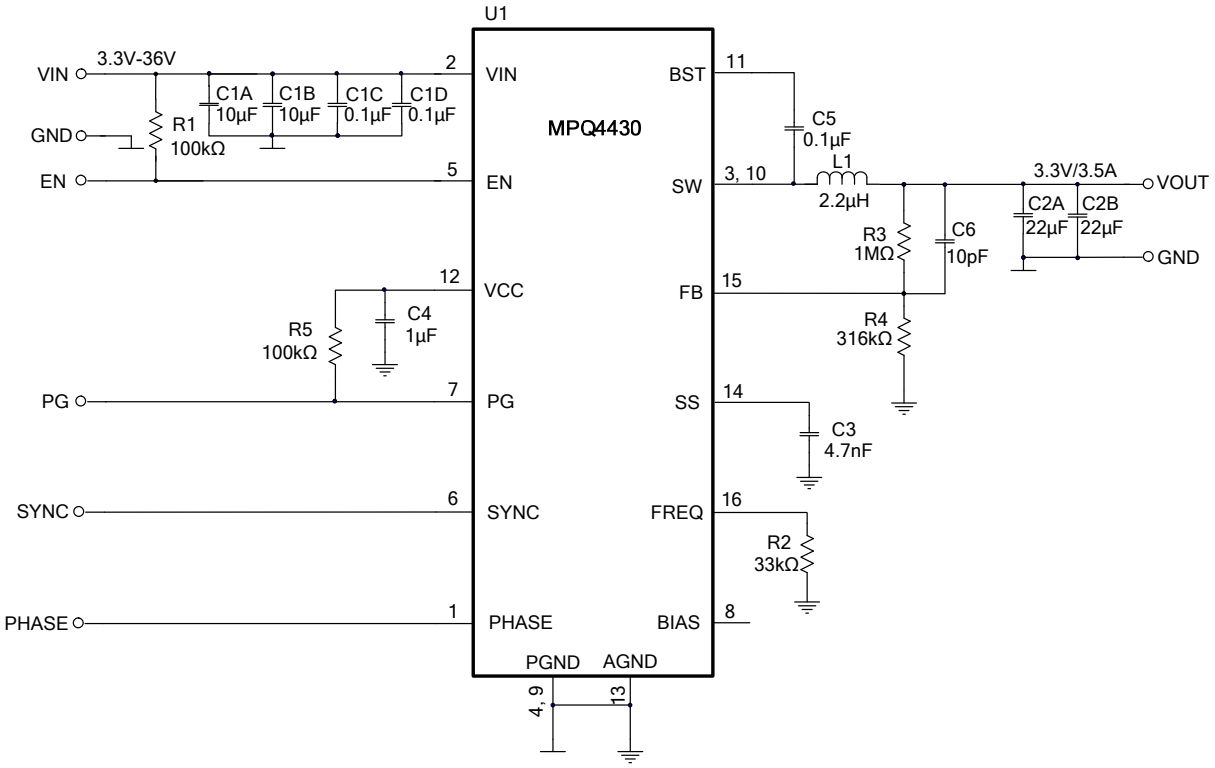


Figure 13: V_{OUT} = 3.3V, f_{SW} = 2.2MHz

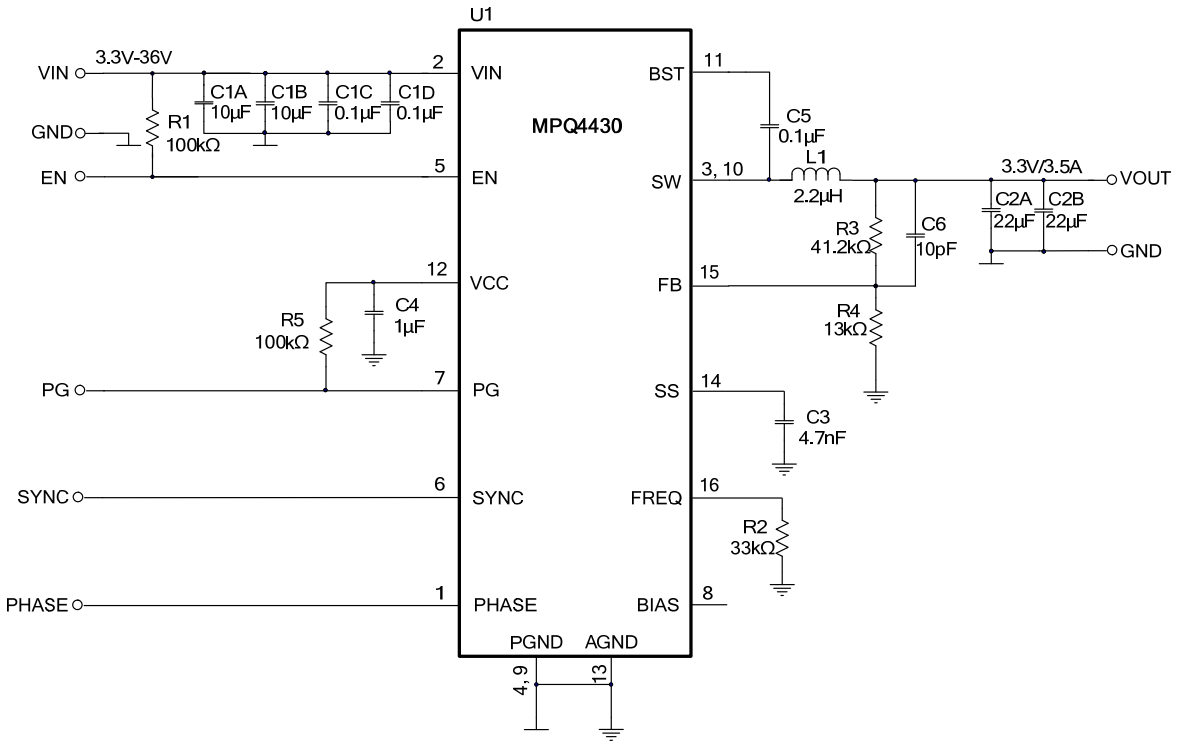


Figure 14: V_{OUT} = 3.3V, f_{SW} = 2.2MHz for <100kΩ FB Divider Application

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

TYPICAL APPLICATION CIRCUITS *(continued)*

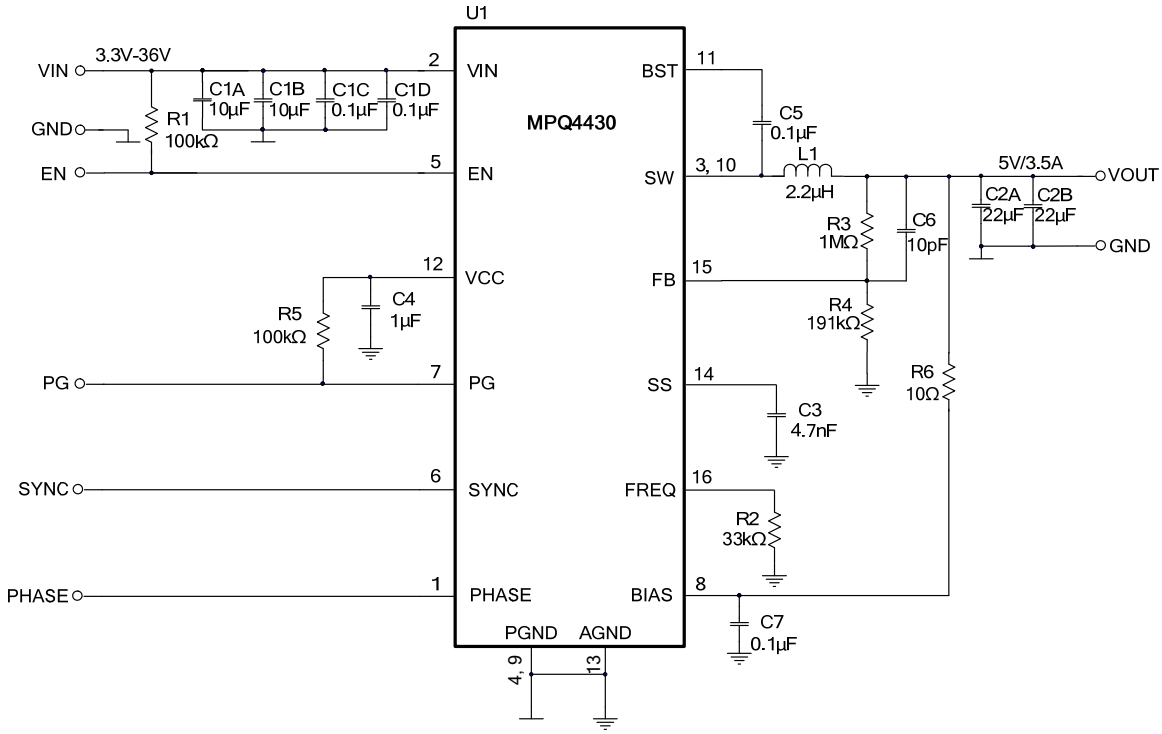


Figure 15: V_{OUT} = 5V, f_{SW} = 2.2MHz

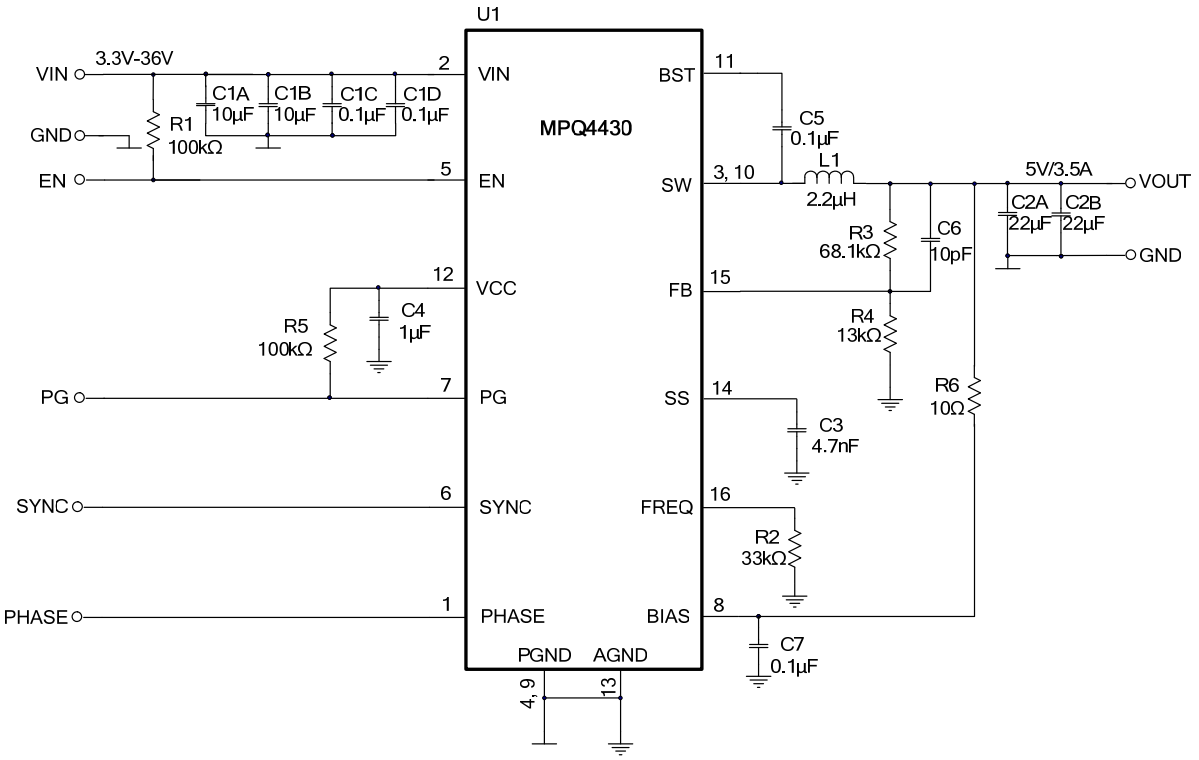


Figure 16: V_{OUT} = 5V, f_{SW} = 2.2MHz for <100kΩ FB Divider Application

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

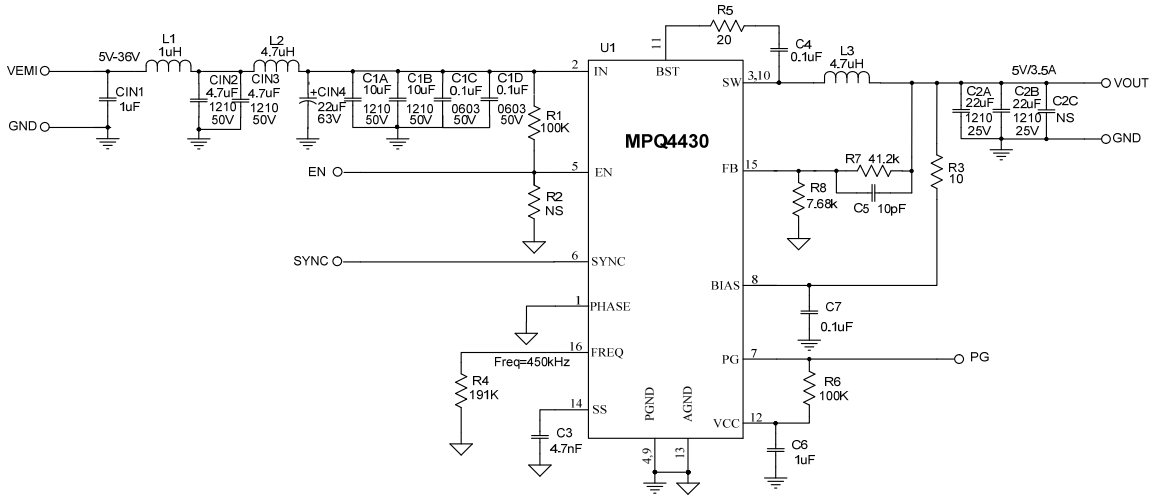


Figure 17: Application Circuit with EMI Filter @V_{OUT} = 5V/3.5A, f_{SW} = 450kHz

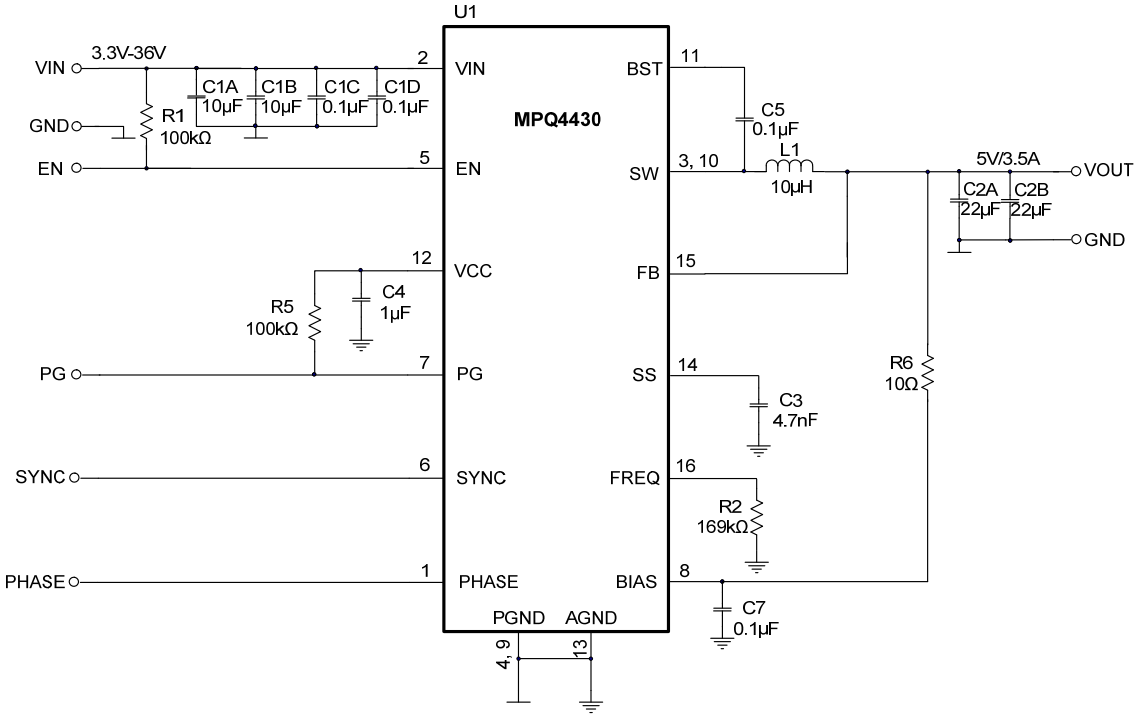
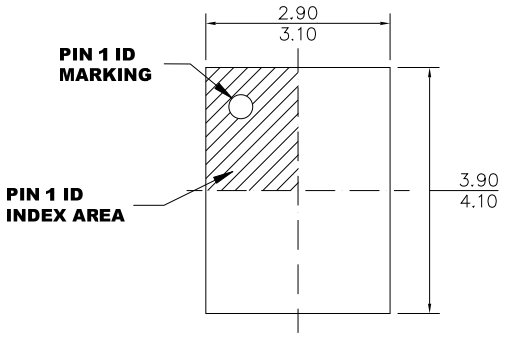


Figure 18: Fixed Output, f_{SW} = 500kHz

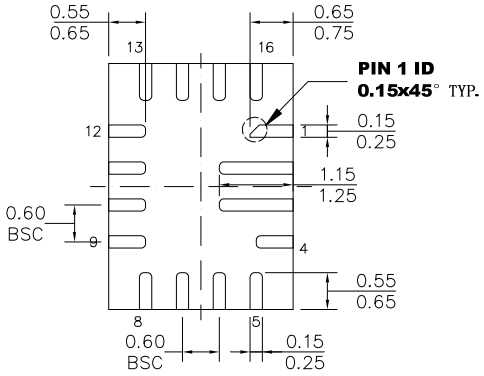
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

PACKAGE INFORMATION

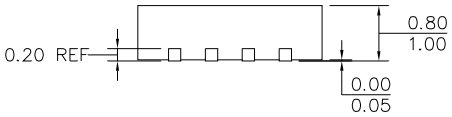
QFN-16 (3mmx4mm)
Non-Wettable Flank



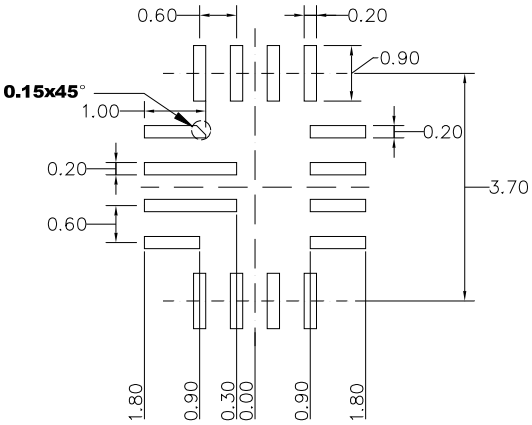
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

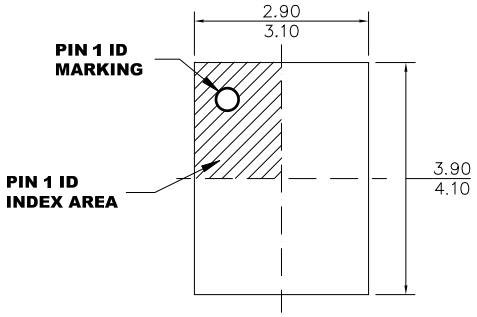
NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

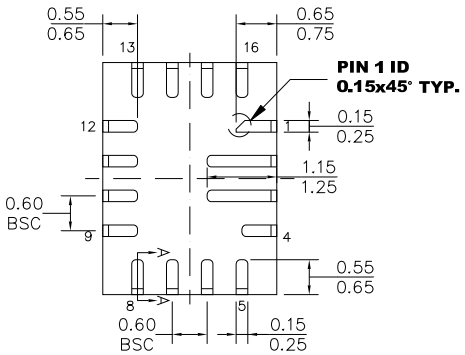
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

PACKAGE INFORMATION *(continued)*

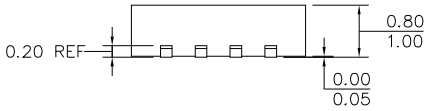
QFN-16 (3mmx4mm)
Wettable Flank



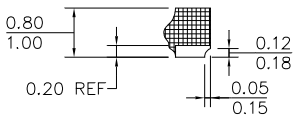
TOP VIEW



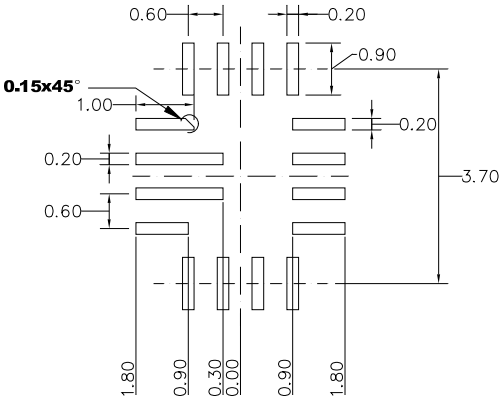
BOTTOM VIEW



SIDE VIEW



SECTION A-A



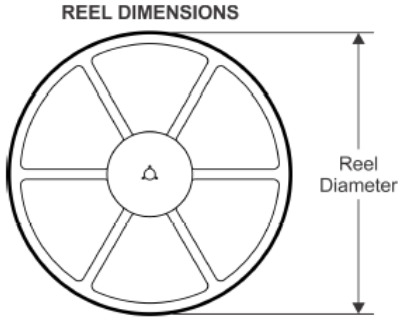
RECOMMENDED LAND PATTERN

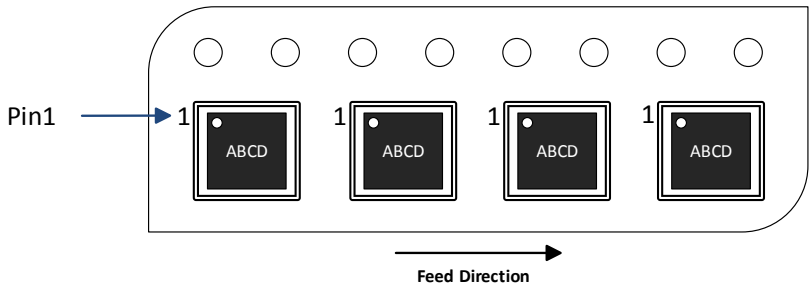
NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

CARRIER INFORMATION





Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ4430GL	QFN-16 (3mmx4mm)	5000	N/A	N/A	13 in.	12 mm	8 mm
MPQ4430GL-AEC1							
MPQ4430GLE-AEC1							
MPQ4430GLE-38-AEC1							
MPQ4430GLE-5-AEC1							

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

Revision History

Revision #	Revision Date	Description	Pages Updated
1.0	3/2/2017	Initial Release	-
1.01	10/24/2017	Update Recommended Operating Conditions	3
1.02	19/04/2019	Add MPQ4430-5 order & package information	1, 3, 19
		Update Recommended Operating Conditions	4
		Add EMC result of CISPR 25 class 5	8, 9
		Add PHASE and PG pin connection when not used in pin description	18
		Add force CCM setting when start up in pin description	18
1.1	5/26/2020	Add MPQ4430-38 order & package & accuracy information	2, 3, 5
		Add MSL and ESD rating	2
		Add thermal resistance based on EVB	4
		Correct load and line regulation curve	11
		Adjust the efficiency curve	12, 13
		Add soft start time when SS pin float	19, 24
		Add limitation of hot plug application	28
		Correct the error of wettable flank package	36
		Add carrier information	37

NOTICE: The information in this document is subject to change without notice. Please contact MPS for current specifications. Users should warrant and guarantee that third party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.