MP174

700V Non-Isolated Off-Line Regulator, Up to 400mA Output Current

The Future of Analog IC Technology

DESCRIPTION

MP174 is a primary-side regulator that provides accurate constant voltage (CV) regulation without opto-coupler. It supports Buck, Buck-Boost, Boost and Flyback topologies. It has an integrated 700V MOSFET to simplify the structure and reduce costs. These features make it an ideal regulator for off-line low power applications, such as home appliances and standby power.

MP174 is a green-mode-operation regulator. Both the peak current and switching frequency decrease as the load decreases. This feature provides excellent efficiency at light load, and improves the overall average efficiency.

MP174 features various protections, including thermal shutdown (OTP), VCC under-voltage lockout (UVLO), overload protection (OLP), short-circuit protection (SCP), and open loop protection.

MP174 is available in small TSOT23-5 package and SOIC8 package.

FEATURES

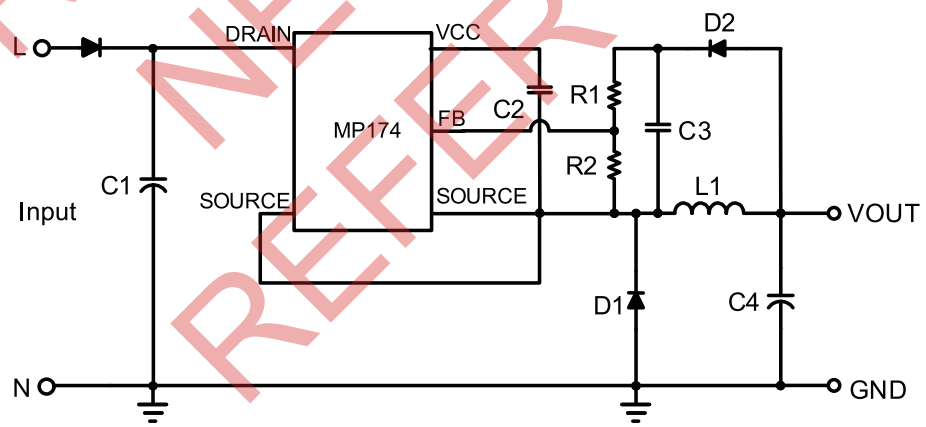
- Primary-side CV control, supporting Buck, Buck-Boost, Boost and Flyback topologies
- Integrated 700V/13.5Ω MOSFET and current source
- <30mW no-load power consumption
- Up to 5W output power
- Maximum DCM output current less than 250mA
- Maximum CCM output current less than 400mA
- Low VCC Operating Current
- Frequency foldback
- Limited maximum frequency
- Peak-current compression
- Internally biased VCC
- OTP, UVLO, OLP, SCP, open loop protection

APPLICATIONS

- Home appliances, white goods and consumer electronics
- Industrial controls
- Standby power

All MPS parts are lead-free, halogen free, and adhere to the RoHS directive. For MPS green status, please visit MPS website under Quality Assurance. “MPS” and “The Future of Analog IC Technology” are Registered Trademarks of Monolithic Power Systems, Inc.

TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number*	Package	Top Marking
MP174GJ	TSOT23-5	*See Below*
MP174GS	SOIC-8	*See Below*

* For Tape & Reel, add suffix –Z (e.g. MP174GJ–Z);
* For Tape & Reel, add suffix –Z (e.g. MP174GS–Z);

TOP MARKING

|AKCY

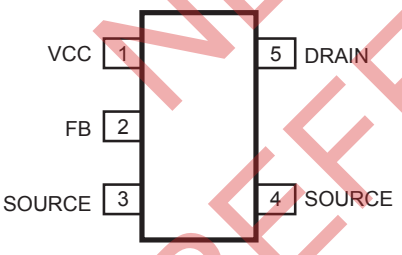
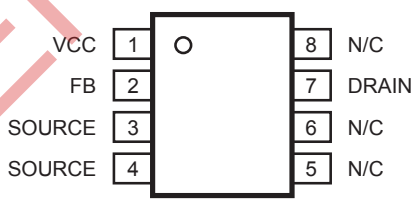
AKC: product code of MP174GJ;
Y: year code;

TOP MARKING

MP174
LLLLLLLL
MPSYWW

MP174: part number of MP174GS;
LLLLLLLL: lot number;
MPS: MPS prefix:
Y: year code;
WW: week code:

PACKAGE REFERENCE

TOP VIEW	TOP VIEW
	
TSOT23-5	SOIC-8

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ABSOLUTE MAXIMUM RATINGS (1)

Drain to source ..... -0.3V to 700V
All other pins ..... -0.3V to 6.5V
Continuous Power Dissipation.... (T_A = +25°C)(2)
TSOT23-5 ..... 1W
SOIC8..... 1W
Junction Temperature..... 150°C
Lead Temperature ..... 260°C
Storage Temperature.....-60°C to +150°C
ESD Capability Human Body Mode 2.0kV
ESD Charged Device Model
TSOT23-5 ..... 1.5kV
SOIC8..... 2.0kV

Recommended Operating Conditions (3)

Operating Junction Temp. (T_J). -40°C to +125°C
Operating VCC range ..... 5.3V to 5.6V

Thermal Resistance (4)

	θ_{JA}	θ_{JC}
TSOT23-5	100	55 ... °C/W
SOIC-8	96	45 ... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature TA. The maximum allowance continuous power dissipation at any ambient temperature is calculated by PD(MAX)=(TJ(MAX)-TA)/θ_{JA}. Exceeding the maximum allowance power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuit protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

VCC = 5.5V, T_J=-40°C~125°C, Min & Max are guaranteed by characterization, typical is tested under 25°C, unless otherwise specified.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Start-up Current Source and Internal MOSFET (Drain Pin)						
Internal regulator supply current	$I_{regulator}$	VCC=4V;V_{Drain}=100V	2.2	4.1	6	mA
Drain pin leakage current	I_{Leak}	VCC=5.8V;V_{Drain}=400V		10	17	μA
Breakdown Voltage	$V_{(BR)DSS}$	T_J=25°C	700			V
ON resistance	R_{on}	T_J=25°C		13.5	17	Ω
		T_J=125°C		21	25	Ω
Supply Voltage Management (VCC Pin)						
VCC level (increasing) where the internal regulator stops	VCC_{OFF}		5.4	5.6	6	V
VCC level (decreasing) where the internal regulator turns on	VCC_{ON}		5.1	5.3	5.7	V
VCC regulator on and off hysteresis			130	250		mV
VCC level (decreasing) where the IC stops	VCC_{stop}		3	3.4	3.6	V
VCC level (decreasing) where the protection phase ends	VCC_{pro}			2.4	2.8	V
Internal IC consumption	I_{CC}	f_s=28kHz, D=67.8%			720	μA
Internal IC consumption (No switching)	I_{CC}				200	uA
Internal IC consumption, latch-off phase	$I_{CCLATCH}$	VCC=5.3V		16	24	μA
Internal Current Sense						
Peak current limit	I_{Limit}	T_J=25°C	600	660	720	mA
Leading-edge blanking	τ_{LEB1}			350		ns
SCP threshold	I_{SCP}	T_J=25°C	750	900		mA
Leading-edge blanking for SCP (1)	τ_{LEB2}			180		ns
Feedback Input (FB Pin)						
Minimum off time	τ_{minoff}		9.5	12	15	μs
Maximum on time	τ_{manon}		19	24	31	μs
Primary MOSFET feedback turn-on threshold	V_{FB}		2.45	2.55	2.65	V
OLP feedback trigger threshold	V_{FB_OLP}		1.6	1.7	1.8	V
OLP delay time	τ_{OLP}	f_s=28kHz		220		ms
Open-loop detection	V_{OLD}		0.4	0.5	0.6	V
Thermal Shutdown						
Thermal shutdown threshold (1)				150		°C
Thermal shutdown recovery hysteresis (1)				30		°C

Notes:

1) This parameter is guaranteed by design.

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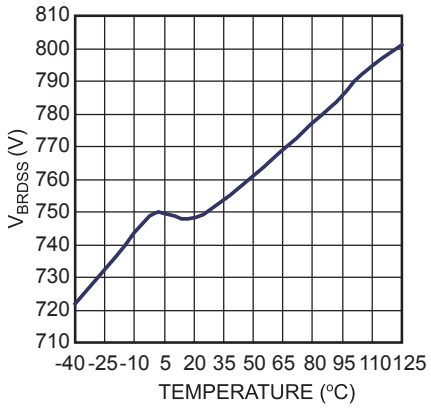
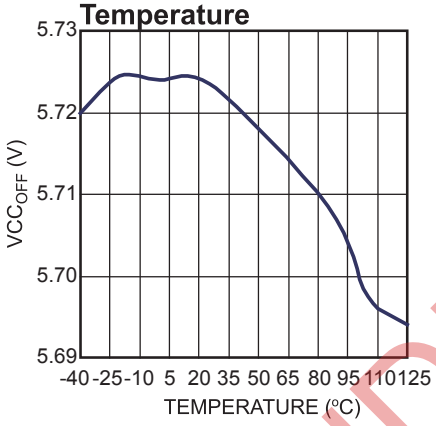
TYPICAL CHARACTERISTICS

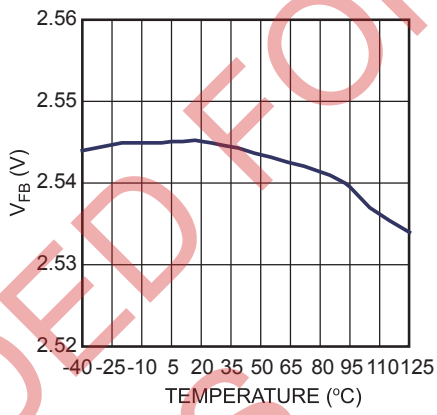
Breakdown Voltage vs. Temperature



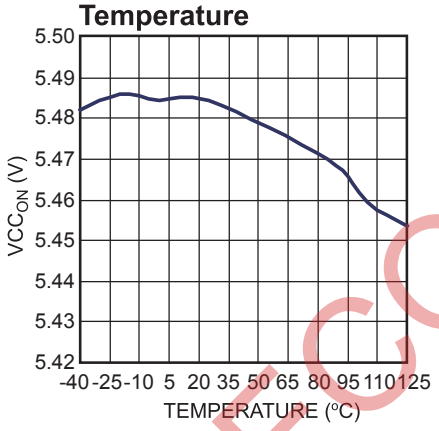
VCC Increasing Level at which the Internal Regulator Stops vs. Temperature



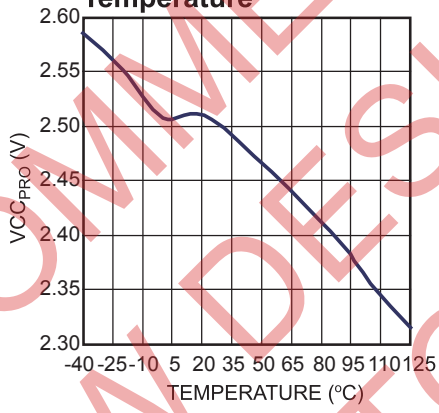
Feedback Voltage vs. Temperature



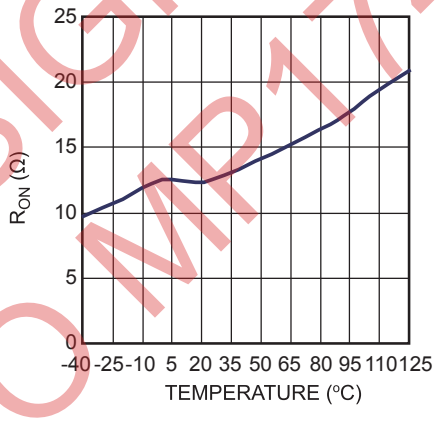
VCC Decreasing Level at which the Internal Regulator Turns On vs. Temperature



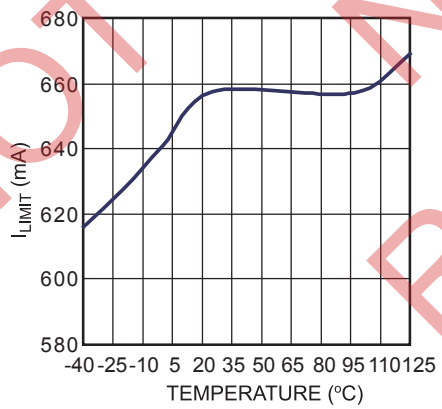
VCC Decreasing Level at which the Protection Phase Ends vs. Temperature



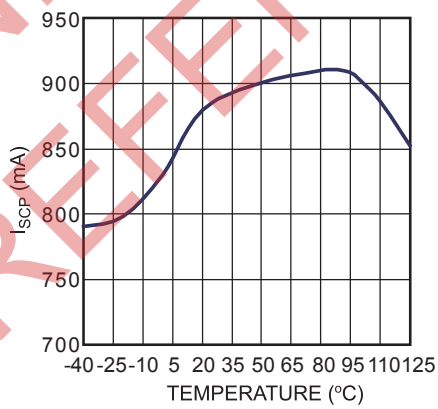
On State Resistance vs. Temperature



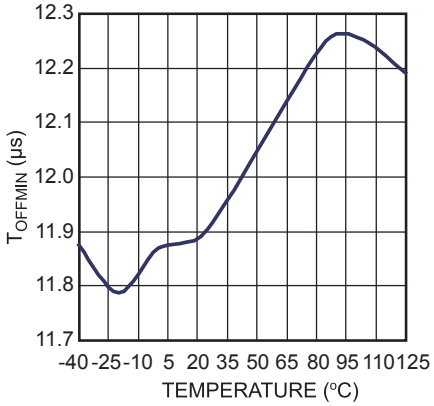
Peak Current Limit vs. Temperature



SCP Point vs. Temperature



Minimum Off Time vs. Temperature



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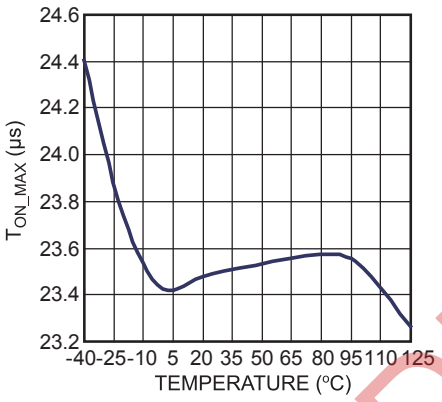
TYPICAL CHARACTERISTICS *(continued)*

Maximum On Time vs. Temperature



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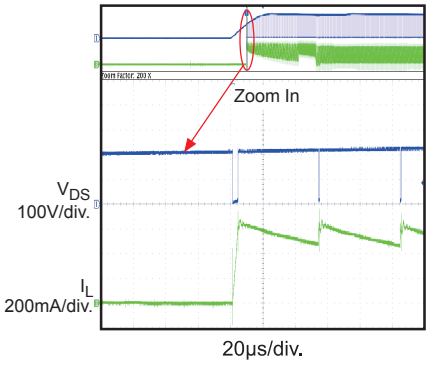
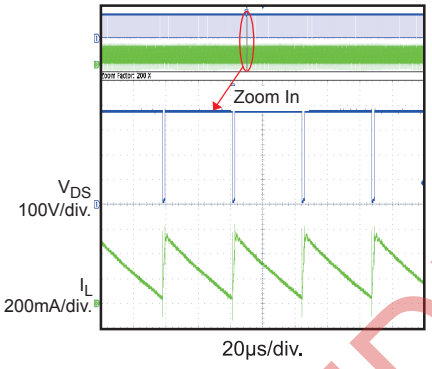
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 265VAC, V_{OUT} = 12V, I_{OUT} = 300mA, L = 1.2mH, C_{OUT} = 100µF, T_A = +25°C, unless otherwise noted.

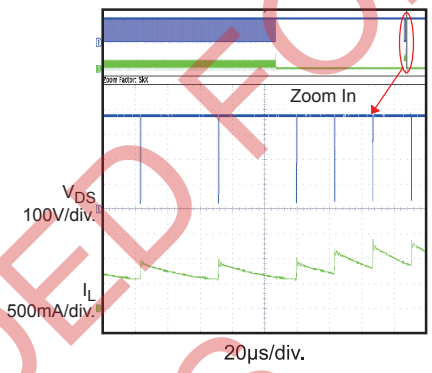
Start Up



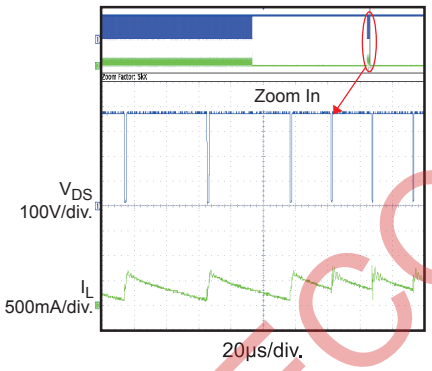
Normal Operation



SCP



Open Loop Detection



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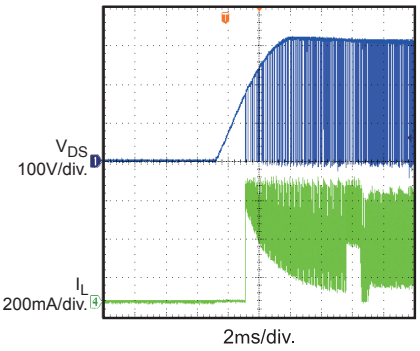
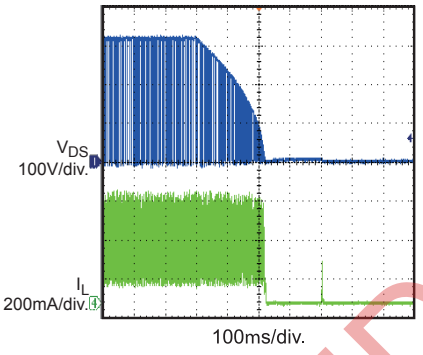
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 230VAC, V_{OUT} = 12V, I_{OUT} = 300mA, L = 1.2mH, C_{OUT} = 100µF, T_A = +25°C, unless otherwise noted.

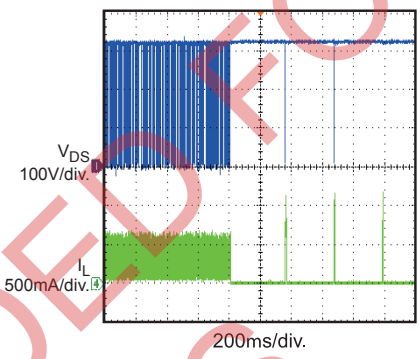
Input Power Startup



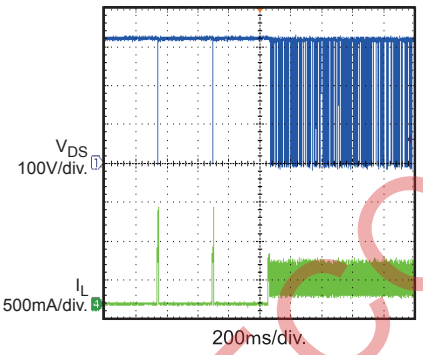
Input Power Shut Down



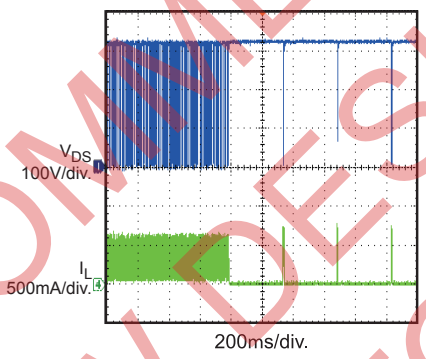
SCP Entry



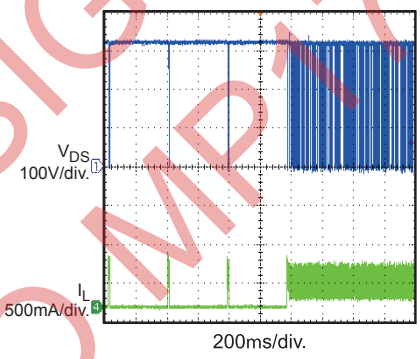
SCP Recovery



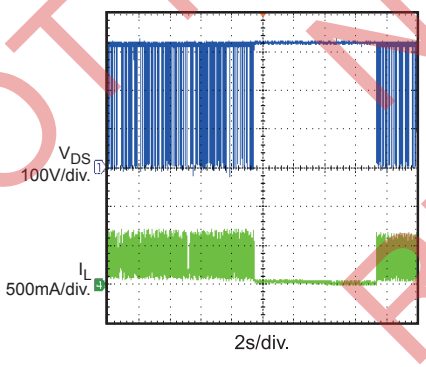
Open Loop Detection Entry



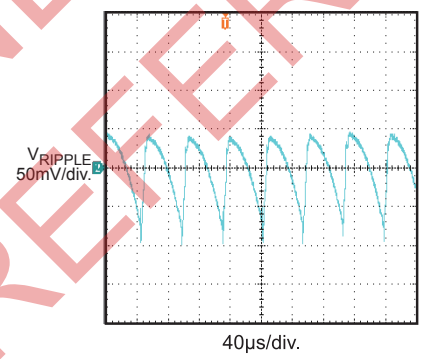
Open Loop Detection Recovery



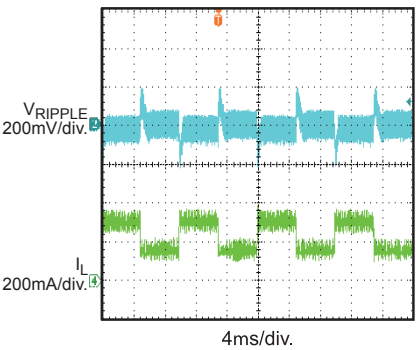
OTP



Output Ripple



Load Transient



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PIN FUNCTIONS

Pin # TSOT23-5	Pin # SOIC8	Name	Description
1	1	VCC	Control circuit power supply.
2	2	FB	Regulator feedback.
3,4	3,4	SOURCE	Internal power MOSFET source. Ground reference for VCC and FB pins.
5	7	DRAIN	Internal power MOSFET drain. High-voltage current source input.
	5,6,8	N/C	Not connected.

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FUNCTIONAL BLOCK DIAGRAM

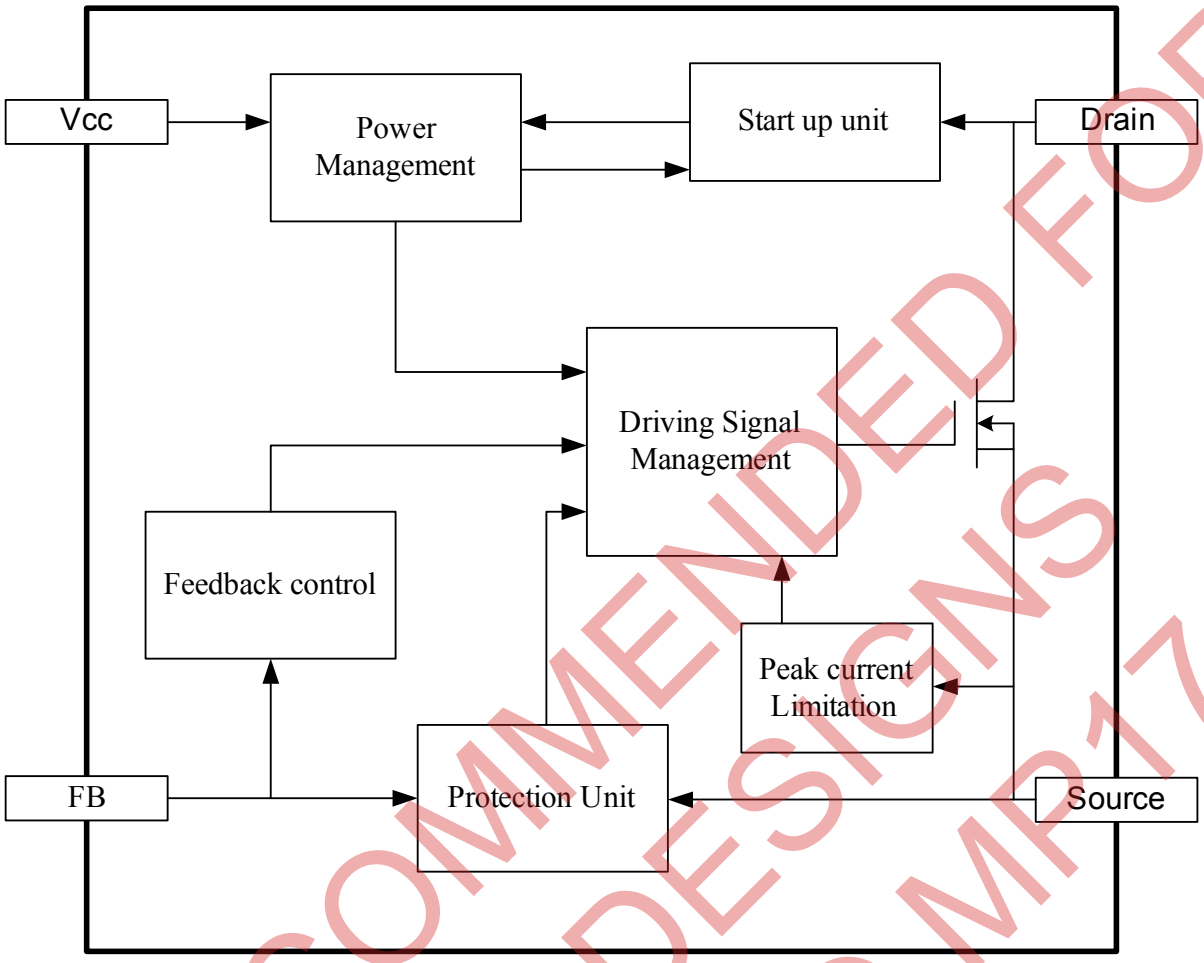

Figure 1: Functional Block Diagram

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OPERATION

MP174 is a green-mode-operation regulator: the peak current and the switching frequency both decrease with a decreasing load. As a result, it offers excellent light-load efficiency, and improves average efficiency. The typical application diagram shows the regulator operates with a minimum number of external components. It incorporates multiple features as described in the following sections.

Start-Up and Under-Voltage Lockout

The internal high-voltage regulator self-supplies the IC from the Drain pin. When VCC voltage reaches 5.6V, the IC starts switching and the internal high voltage regulator turns off. The internal high-voltage regulator turns on to charge the external VCC capacitor when the VCC voltage falls below 5.3V. A small capacitor (in the low μF range) can maintain the VCC voltage and thus lower the capacitor cost.

The IC stops switching when the VCC voltage drops blow 3.4V.

Under fault conditions—such as OLP, SCP, and OTP—the IC stops switching and an internal current source (~16μA) discharges the VCC capacitor. The internal high-voltage regulator will not charge the VCC capacitor until the VCC voltage drops below 2.4V. The restart time can be estimated using the following equation,

$$\tau_{restart} = C_{VCC} \times \frac{V_{CC} - 2.4V}{16\mu A} + C_{VCC} \times \frac{5.6V - 2.4V}{4.1mA}$$

Soft-Start

The IC stops operation when VCC voltage drops blow 3.4V and starts operation when VCC charges to 5.6V. Every time when the chip starts operation there is a Soft-Start period. The soft-start prevents the inductor current from overshooting by limiting the minimum off time.

MP174 adopts a 2 phase minimum off-time limit soft-start. Each Soft-Start phase retains 128 switching cycles. During soft-start, off time limit gradually shortens from 48μs to 24μs, and finally to the 12μs normal operation off-time limit (see Figure 2).

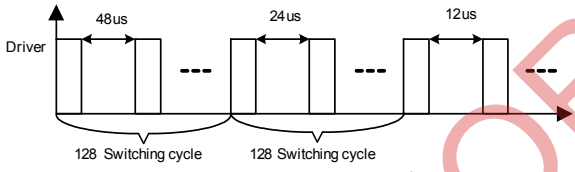

Figure 2: $\tau_{min\,off}$ at Start-Up

Constant Voltage Operation

MP174 acts as a fully-integrated regulator when used in the Buck topology, as shown in the typical application on page1.

It regulates the output voltage by monitoring the sampling capacitor.

At the beginning of each cycle, the integrated MOSFET turns on while the feedback voltage drops below the 2.55V reference voltage, which indicates insufficient output voltage. The peak current limitation determines the ON period. After the ON period elapses, the integrated MOSFET turns off. Sampling capacitor (C3) voltage is charged to the output voltage, when the freewheeling diode (D1) turns on. In this way, the sampling capacitor (C3) samples and holds the output voltage for output regulation. The sampling capacitor (C3) voltage decreases when the L1 inductor current falls below the output current. When the feedback voltage falls below the 2.55V reference voltage, a new switching cycle begins. Figure 3 shows this operation under CCM in detail.

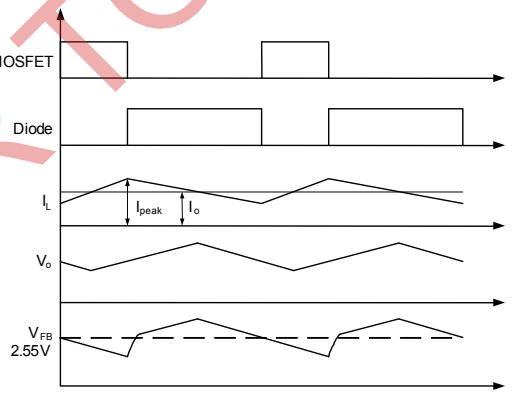

Figure 3: V_{FB} vs. V_O

Use the following equation to determine the output voltage:

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$$Vo = 2.55V \times \frac{R1+R2}{R2}$$

Frequency Foldback and Peak Current Compression

The MP174 remains highly efficient under light-load condition by reducing the switching frequency automatically.

Under light-load or no-load conditions, the output voltage drops very slowly, which increasing the MOSFET off time. Thus the frequency decreases as the load decreases.

Determine the switching frequency as:

$$f_s = \frac{(V_{in} - V_o)}{2L(I_{peak} - I_o)} \cdot \frac{V_o}{V_{in}}, \text{ for CCM}$$

$$f_s = \frac{2(V_{in} - V_O)}{LI^2_{peak}} \cdot \frac{I_o V_o}{V_{in}}, \text{ for DCM}$$

At the same time, the peak current limit decreases from 660mA as the off-time increases. In standby mode, the frequency and the peak current are both minimized, allowing for a smaller dummy load. As a result, peak-current compression helps further reduce no-load consumption. Peak current limit can be estimated from the following equation (τ_{off} is the power module's off time):

$$I_{Peak} = 660mA - (2.4mA/\mu s) \times (\tau_{off} - 12\mu s)$$

EA Compensation

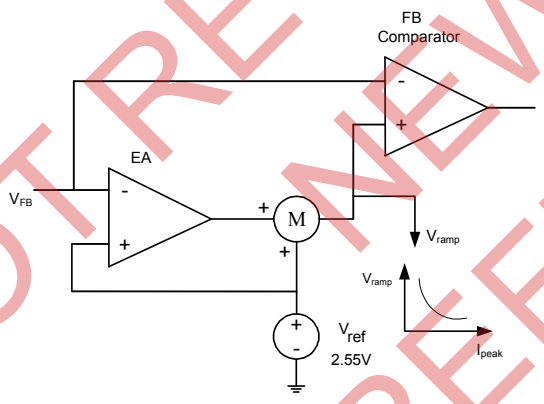

Figure 4: EA and Ramp Compensation

MP174 has internal error amplifier (EA) compensation loop. It samples the feedback voltage 6us after the MOSFET turns off, and regulates the output based on the 2.55V reference voltage.

Ramp Compensation

An internal ramp compensation circuit improves the load regulation. As shown in Figure 4, an exponential voltage signal added to pull down the reference voltage of the feedback comparator. The ramp compensation is a function of the load conditions: the compensation is about the 1mV/μs under full-load conditions compensation increases exponentially as the peak current decreases.

Over-Load Protection (OLP)

Maximum output power of MP174 is limited by maximum switching frequency and peak current limit. If the load current is too large, output voltage drops, so that the FB voltage drops.

When the FB voltage drops below 1.7V it is considered as an error flag and timer starts. If the timer reaches 220ms (f_S=28kHz), OLP occurs. This timer duration avoids triggering OLP when the power supply starts up or load transition. The power supply should start up in less than 220ms (f_S=28kHz). The OLP delay time is calculated as per the following equation:

$$\tau_{Delay} \approx 220ms \times \frac{28kHz}{fs}$$

Short-Circuit Protection (SCP)

The MP174 monitors the peak current, and shuts down when the peak current rises above SCP threshold through short-circuit protection. The power supply resumes operation with the removal of the fault.

Thermal Shutdown (OTP)

To prevent any thermal induced damage, the MP174 shuts down switching when the junction temperature exceeds 150°C. During the thermal shutdown (OTP), the VCC capacitor is discharged to 2.4V, and then the internal high voltage regulator re-charges. MP174 recovers when junction temperature drops below 120°C.

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Open-Loop Detection

If V_{FB} is less than 0.5V, the IC will stop switching and a re-start cycle will begin. During Soft-Start, the open loop detection is blanked.

Leading-Edge Blanking

An internal leading-edge blanking (LEB) unit avoids premature switching pulse termination due to turn on spike. Turn on spike is caused by parasitic capacitance and reverse recovery of freewheeling diode. During the blanking time, the current comparator is disabled and can not turn off the external MOSFET. Figure 5shows the leading-edge blanking.

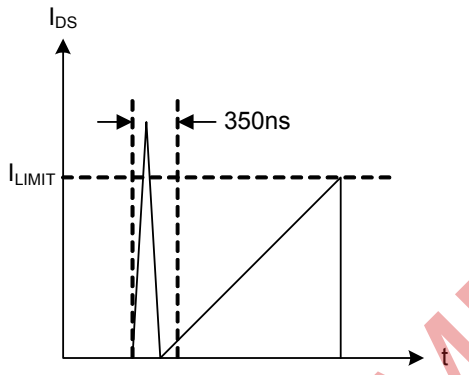

Figure 5: Leading-Edge Blanking

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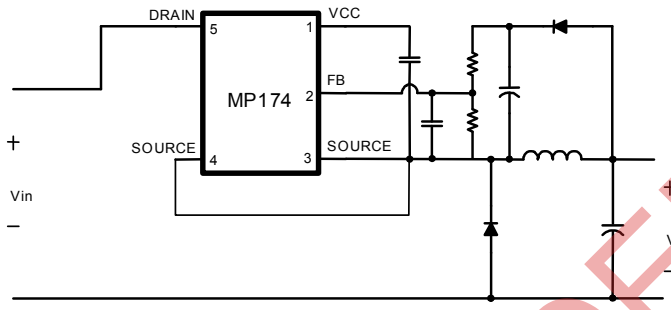
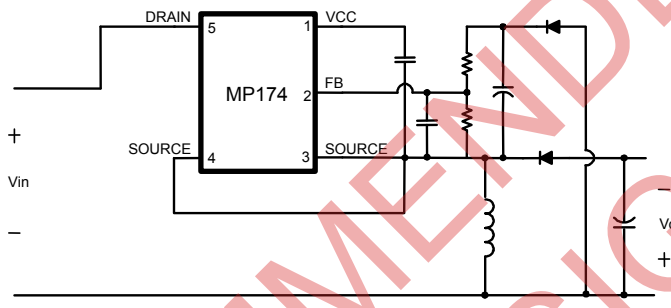
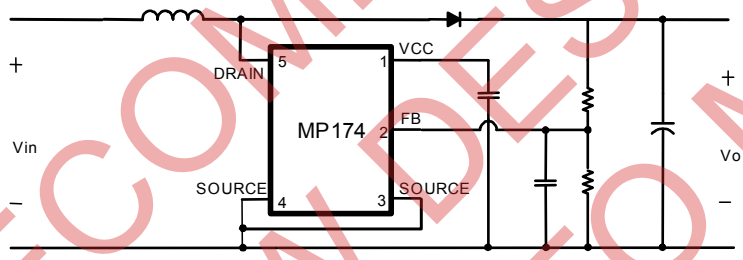
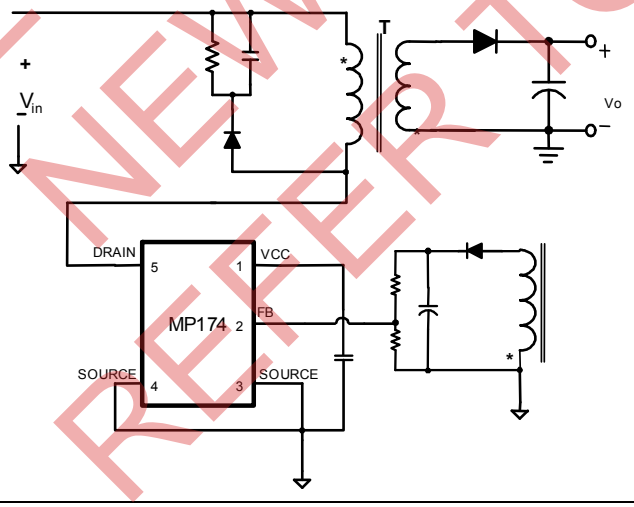
APPLICATION INFORMATION

Table 1: Common Topologies Using MP174

Topology	Circuit Schematic	Features
High-Side Buck		1. No-isolation, 2. Positive output 3. Low cost 4. Direct feedback
High-Side Buck-Boost		1. No-isolation, 2. Negative output 3. Low cost 4. Direct feedback
Boost		1. No-isolation, 2. Positive output 3. Low cost 4. Direct feedback
Flyback		1. Isolation, 2. Positive output 3. Low cost 4. Indirect feedback

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Topology Options

MP174 can be used in common topologies, such as Buck, Buck-Boost, Boost and Flyback. As illustrated in table 1.

Component Selection

Input Capacitor

The input capacitor supplies the DC input voltage for the converter. Figure 6 shows the typical DC bus voltage waveform of half-wave rectifier and full-wave rectifier.

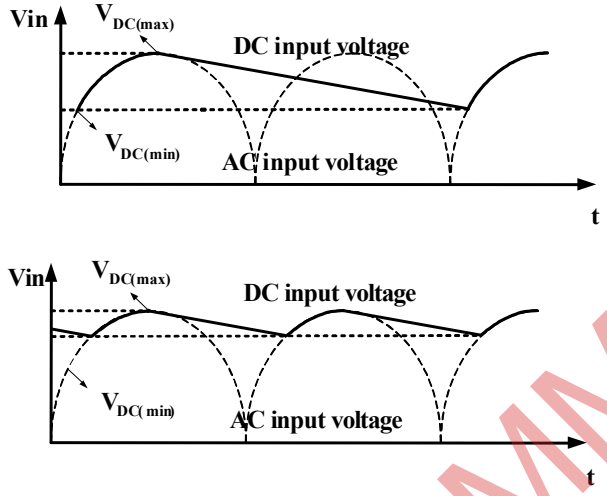

Figure 6: Input Voltage Waveform

Typically, the use of a half-wave rectifier requires an input capacitor rated at 3uF/W for the universal input condition. When using the full-wave rectifier, input capacitor is chosen as as 1.5~2uF/W for universal input condiont. Avoid a minimum DC voltage below 70V; a low DC input voltage can cause thermal issue. Half-wave rectifier is recommended for <2W output application and full-wave rectifier is recommended for >2W output application.

Inductor

The MP174 has a minimum off-time limit that determines the maximum power output. The maximum power increases as the inductor increases. Using a very small inductor may cause failure at full load, but a larger inductor means a higher OLP load. It is recommended to select an inductor with the minimum value that can supply the rated power. Estimate the maximum power with:

$$P_{omax} = V_o(I_{peak} - \frac{V_o \tau_{minoff}}{2L}), \text{ for CCM}$$

$$P_{omax} = \frac{1}{2} L I_{peak}^2 \cdot \frac{1}{\tau_{minoff}}, \text{ for DCM}$$

For mass production, tolerance on the parameters, such as peak current limitation, minimal off time, should be taken into consideration.

Figure 7 shows a example of a P_{min} curve with a 12V output. I_{peak}=0.6A and T_{minoff}=15μs is used as the worst case for P_{MIN} calculation.

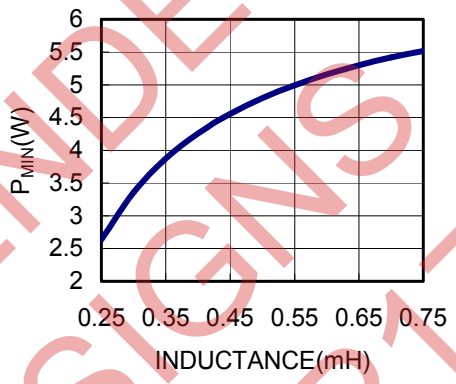

Figure 7: P_{min} vs. L at 12V

For a 3.6W output converter (12V, 0.3A), the minimum inductor value is about 0.36mH. But the switching frequency is too high using a 0.36mH inductor, which causes poor efficiency. Usually, it is recommended to use an inductor that make the switching frequency is higher than 20 kHz but not too high in large output current applications.

To reduce costs, use a standard off-the-shelf inductor no less than the calculated value.

Freewheeling Diode

The diode should be selected based on maximum input voltage and peak current.

The freewheeling diode's reverse recovery can affect efficiency and circuit operation for CCM condiotn, so use an ultra fast diode such as the EGC10JH.

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Output Capacitor

The output capacitor is required to maintain the DC output voltage. Estimate the output voltage ripple as:

$$V_{CCM_ripple} = \frac{\Delta i}{8 f_s C_o} + \Delta i \cdot R_{ESR}, \text{ for CCM}$$

$$V_{DCM_ripple} = \frac{I_o}{f_s C_o} \cdot \left(\frac{I_{pk} - I_o}{I_{pk}} \right)^2 + I_{pk} \cdot R_{ESR}, \text{ for DCM}$$

It is recommended to use ceramic, tantalum or low ESR electrolytic capacitors to reduce the output voltage ripple.

Feedback Resistors

The resistor divider determines the output voltage. Appropriate R1 and R2 values should be chosen to maintain V_{FB} at 2.55V. R2 is typically 5kΩ to 10kΩ, avoid large R2 value.

Feedback Capacitor

The feedback capacitor provides a sample and hold function. Small capacitors result in poor regulation at light loads, and large capacitors affect the circuit operation. Roughly estimate an optimal capacitor value using the following equation:

$$\frac{1}{2} \frac{V_o}{R_1 + R_2} \cdot \frac{C_o}{I_o} \le C_{FB} \le \frac{V_o}{R_1 + R_2} \cdot \frac{C_o}{I_o}$$

Dummy Load

A dummy load is required to maintain the load regulation. This ensures sufficient inductor energy to charge the sample and hold capacitor to detect the output voltage. Normally a 3mA dummy load is needed and can be adjusted according to the regulated voltage. It is a compromise between small no load consumption and good no load regulation, especially for applications require 30mW no load consumption. Use a zener to reduce no-load consumption if no-load regulation is not a concern.

Auxiliary VCC Supply

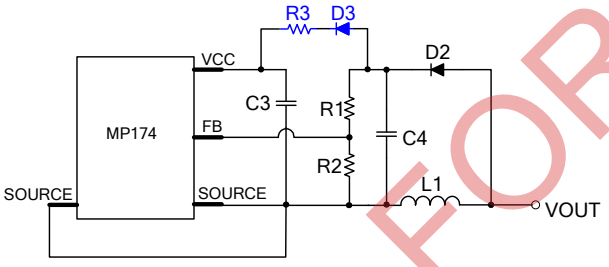

Figure 8: Auxiliary V_{CC} Supply Circuit

For V_O above 7V applications, MP174 can achieve the 30mW no-load power requirement. In order to do this, chip requires an external VCC supply to reduce overall power consumption.

This auxiliary VCC supply is derived from the resistor connected between C3 and C4. C4 should be set larger than recommendation above. D3 is used in case that VCC interfere with FB, R3 is determined per the formula below.

$$R \approx \frac{V_o - 5.8V}{I_S}$$

Where I_S is the VCC consumption under no load condition. R should be adjusted to meet the actual I_S, because it varies in different application. In a particular configuration, I_S is measured as about 250uA.

Surge Performance

Appropriate input capacitor value should be chosen to obtain a good surge performance. Figure 9 shows the half-wave rectifier. Table 2 shows the capacitance required under normal condition for different surge voltages. FR1 is 20Ω/2W fused resistor and L1 is 1mH for this recommendation.

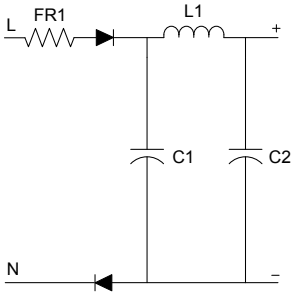

Figure 9: Half-Wave Rectifier

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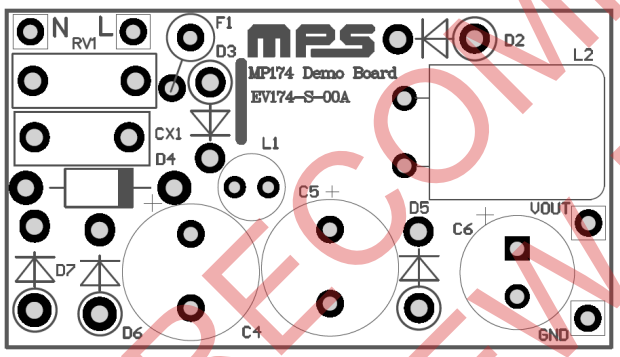
Table 2: Recommended Capacitance

Surge voltage	500V	1000V	2000V
C1	1μF	2.2μF	3.3μF
C2	1μF	2.2μF	3.3μF

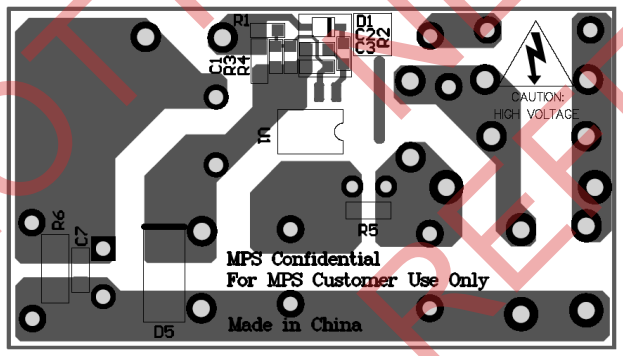
Layout Guide

PCB layout is very important for reliable operation, and good EMI and thermal performance. Please follow these guidelines to optimize performance.

1) Minimize the loop area formed by the input capacitor, IC, freewheeling diode, inductor and output capacitor.
2) Place the power inductor far away from the input filter while keeping the loop area to the inductor to a minimum, see example below.
3) Place a capacitor valued at several hundred pF between the FB pin and source as close the IC as possible.
4) Connect the exposed pads or large copper area with the DRAIN pin to improve thermal performance.



Top



Bottom Layer

Design Example

Below is a design example following the application guidelines for the specifications:

Table 3: Design Example

V_{IN}	85VAC to 265VAC
V_{OUT}	12V
I_{OUT}	300mA

The detailed application schematic is shown in Figure.10. The typical performance and circuit waveforms have been shown in the Typical Performance Characteristics section. For more device application, please refer to the related Evaluation Board Datasheets.

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TYPICAL APPLICATION CIRCUITS

Figure 10 shows a typical application example of a 12V, 300mA non-isolated power supply using MP174.

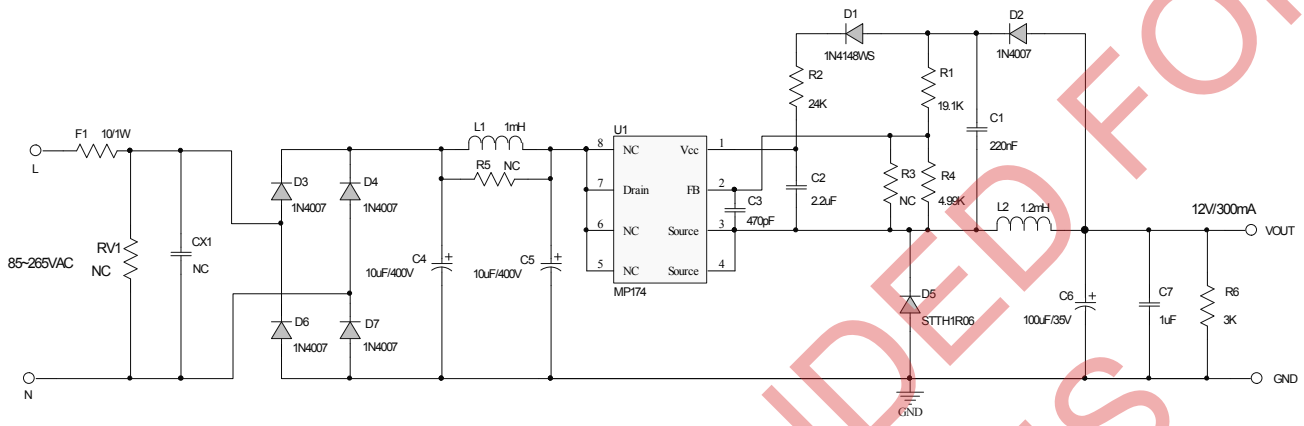

Figure 10: Typical Application at 12V, 300mA

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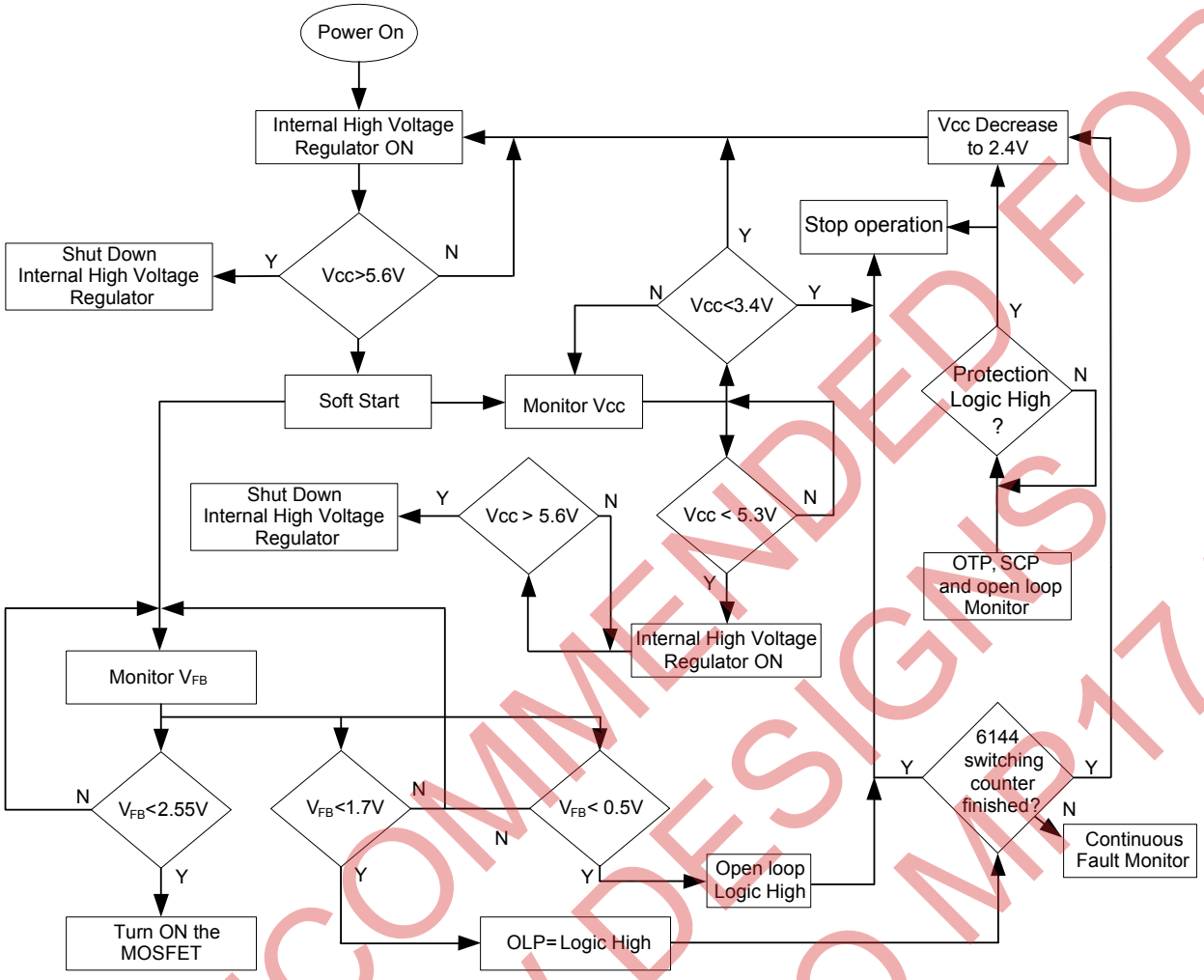
FLOW CHART



UVLO, SCP, OLP, OTP and Open loop protections are auto restart

Figure 11: Control Flow Chart

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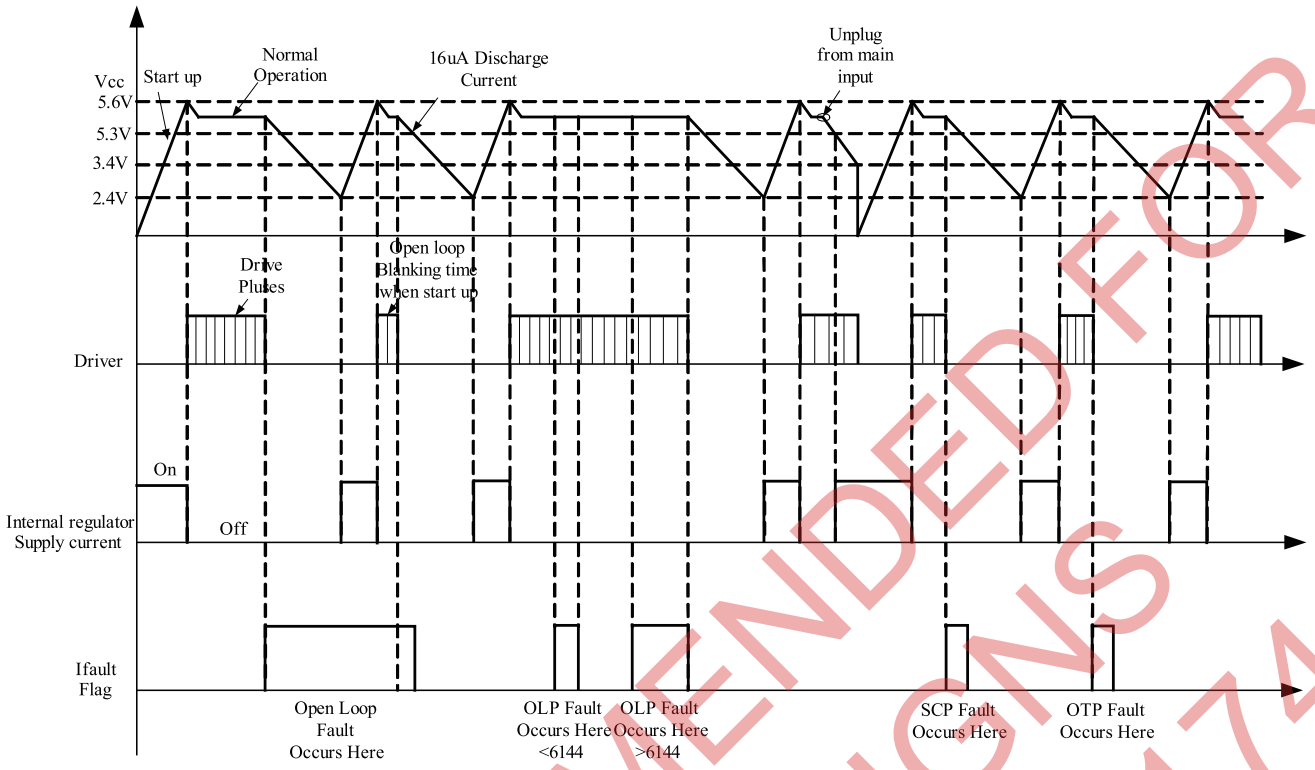

Figure 12: Signal Evolution in the Presence of a Fault

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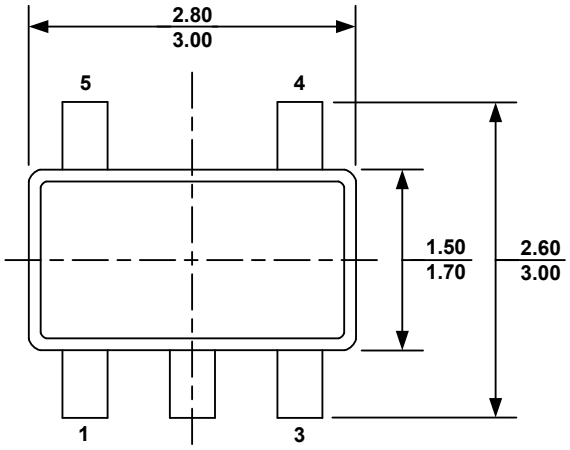
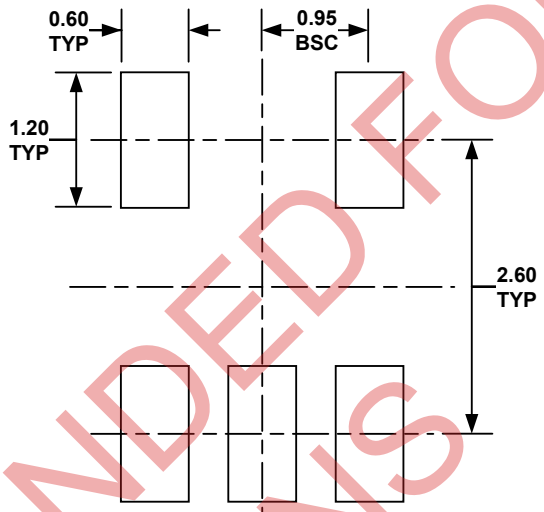
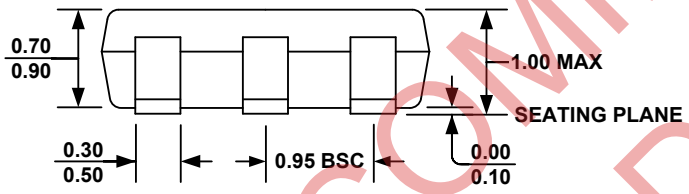


TOP VIEW



RECOMMENDED LAND PATTERN



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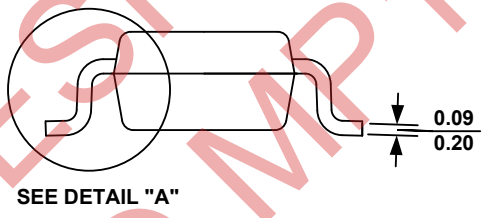
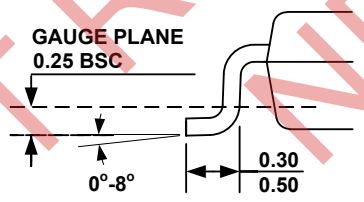


SIDE VIEW



DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-193, VARIATION AA.
6) DRAWING IS NOT TO SCALE.

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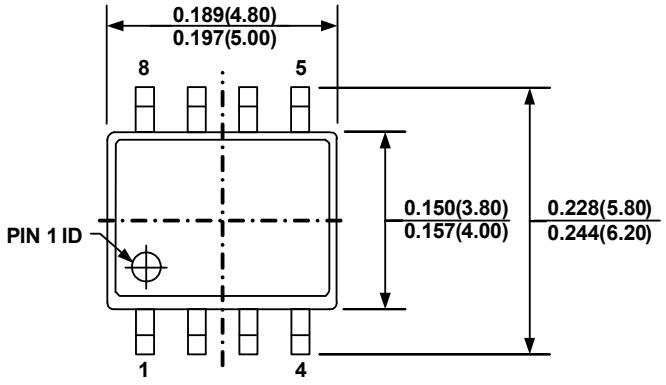
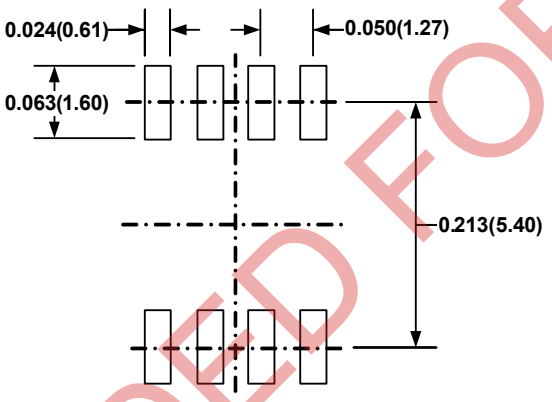


TOP VIEW



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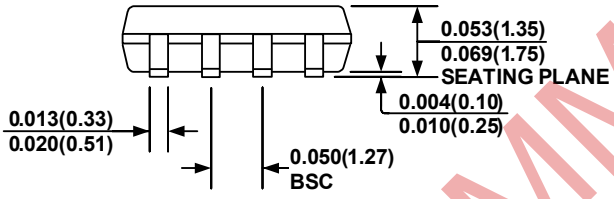
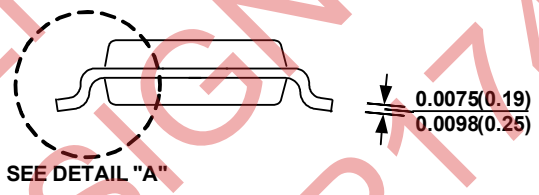
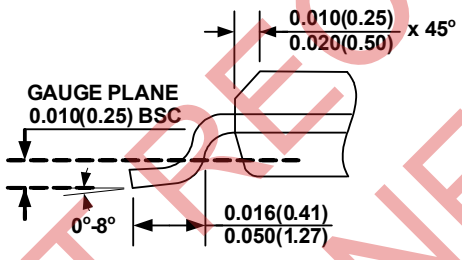


FRONT VIEW



SIDE VIEW



DETAIL "A"

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3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY(BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
6) DRAWING IS NOT TO SCALE

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