MP2796

7-Cell to 16-Cell Battery Monitor and Protector

DESCRIPTION

The MP2796 is a robust battery management device, providing a complete analog front-end (AFE) monitoring and protection solution. It is designed for multiple-cell series battery management systems (BMS). The device can support I²C or SPI communication. It supports connections for 7-cell to 16-cell series battery packs, with an absolute voltage exceeding 80V on particular pins.

The MP2796 integrates two separate analog-to-digital converters (ADCs). The first ADC measures each channel's differential cell voltages (up to 16 channels), die temperature, and 4-channel temperatures via external NTC thermistors. The second ADC measures the charge/discharge current via an external current-sense resistor.

When paired with an MPF4279x fuel gauge, the MP2796 can achieve a state-of-charge (SOC) error to within 2%.

The MP2796 includes high-side MOSFET (HS-FET) drivers for charge and discharge control. The discharge (DSG) MOSFET driver includes a configurable soft start (SS) that provides a controlled turn-on, eliminating the need for an external pre-charge circuit. The MOSFET drivers also incorporate over-current protection (OCP), short-circuit protection (SCP), battery under-voltage protection (UVP), battery over-voltage protection (OVP), and high-/low-temperature protection. All of these protections have configurable thresholds.

Internal passive balancing MOSFETs can be used to equalize mismatched cells, supporting up to 58mA. There is also the option to drive external balancing transistors (MOSFET or BJT).

The MP2796 is available in a TQFP-48 (7mmx7mm) package.

FEATURES

- **Incorporates Dual Analog-to-Digital Converter (ADC) Architecture:**
  - <±2% State-of-Charge (SOC) Error with MPF4279x Fuel Gauge
  - Cell Voltage Measurement Error <10mV
  - Current Error <±0.5%
- **Includes High-Side N-Channel MOSFET Drivers for Charge and Discharge Control:**
  - Supports MOSFET Soft-Start Discharge Control to Eliminate Pre-Charge Circuit
  - Drives Up to 100A DC with Parallel N-Channel MOSFETs
- **Hardware Configurable Protections:**
  - Charge/Discharge OCP and SCP
  - Cell UVP and OVP
  - Pack UVP and OVP
  - Cell Low-/High-Temperature Protection
  - Die High-Temperature Protection
- **Passive Cell Balancing up to 58mA per Cell:**
  - Can Drive External Balancing Transistors
  - Automatic or Manual Control
- **Additional Features:**
  - Integrated 3.3V and 5V LDOs
  - Reduced Current Standby Mode
  - High-Voltage and Low-Voltage GPIOs
  - Dedicated Thermistor Inputs
  - Open-Wire Detection
  - Persistent Dead Battery Flag
  - Lockable Multiple-Time Programmable (MTP) Memory for Key Thresholds
- I²C or SPI Interface with 8-Bit CRC
- Random Cell Connection Tolerant
- Available in a TQFP-48 (7mmx7mm) Package

APPLICATIONS

- E-Bikes, E-Scooters
- Battery Backup and UPSs
- Power and Gardening Tools
- Energy Storage Systems (ESSs)

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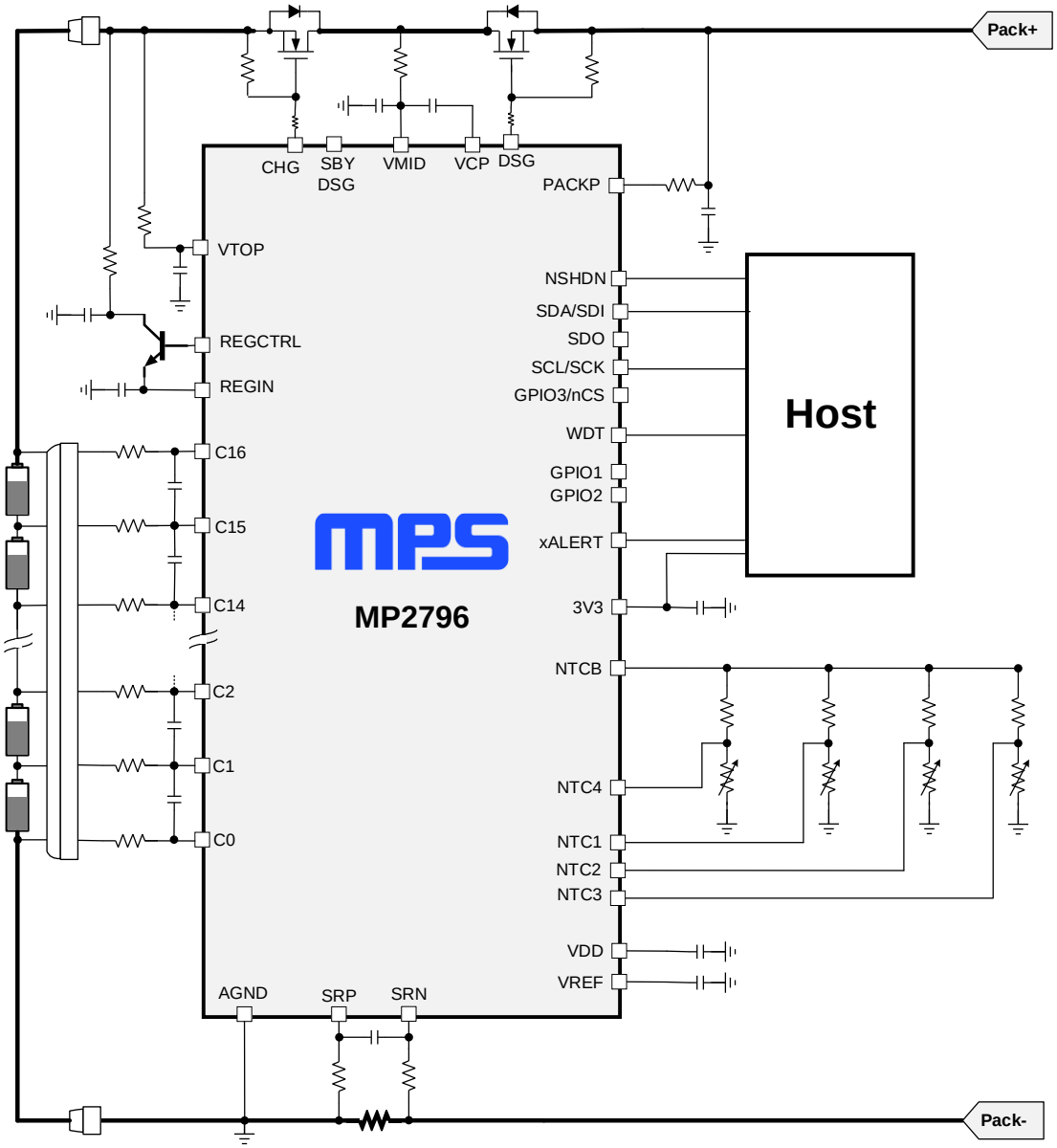
TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating	Communication
MP2796DFP-xxxx**	TQFP-48 (7mmx7mm)	*See Below*	3	
MP2796DFP-0000	TQFP-48 (7mmx7mm)	*See Below*	3	I^2C, CRC disabled
MP2796DFP-0001	TQFP-48 (7mmx7mm)	*See Below*	3	I^2C, CRC enabled
MP2796DFP-0002	TQFP-48 (7mmx7mm)	*See Below*	3	SPI, CRC disabled
EVKT-MP2796-0000	Evaluation kit	N/A	N/A	N/A
EVKT-MP2796-0002	Evaluation kit	N/A	N/A	N/A

* For Tray, add suffix -T (e.g. MP2796DFP-xxxx-T).

** "-xxxx" is the configuration code identifier for the register settings. Each "x" can be a hexadecimal value between 0 and F. The default codes are "0000", "0001", and "0002". Contact an MPS FAE to create this unique number.

TOP MARKING (MP2796)

MPSYYWW
MP2796
LLLLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP: MPS prefix
2796: Part number
LLLLLLLLL: Lot number

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EVALUATION KIT EVKT-MP2796-0000

EVKT-MP2796-0000 kit contents (items below can be ordered separately):

#	Part Number	Item	Quantity
1	EV2796-0000-FP-00A	MP2796DFP-0000 I^2C evaluation board	1
2	EVKT-USBI2C-02	Includes one USB-to-I^2C communication interface, one USB cable, and one ribbon cable	1
3	Online resources	Include datasheet, user guide, product brief, and GUI	1

Order directly from MonolithicPower.com or our distributors.

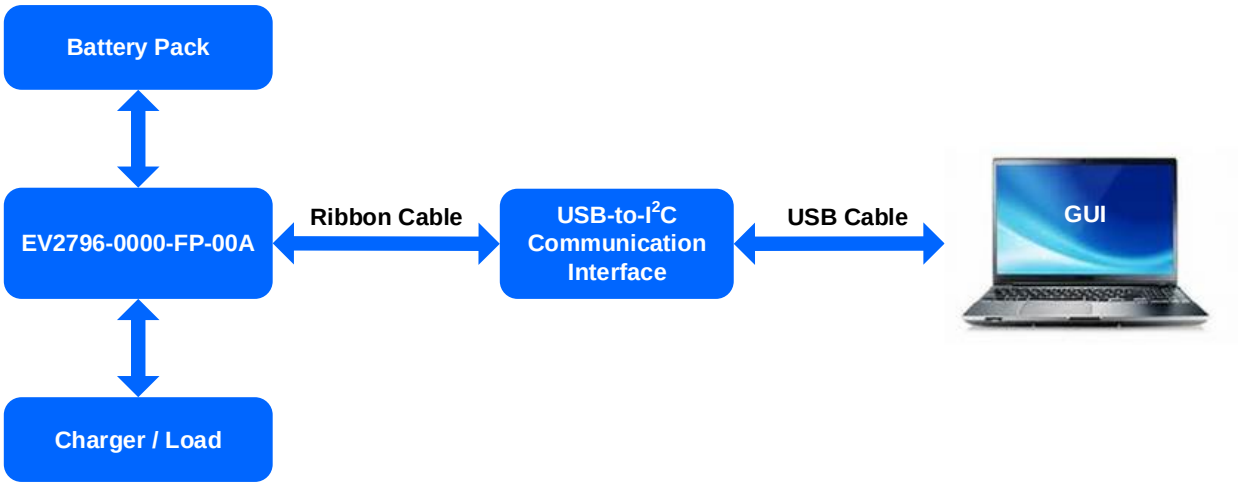

Figure 1: EV2796-0000-FP-00A Evaluation Kit Set-Up

EVALUATION KIT EVKT-MP2796-0002

EVKT-MP2796-0002 kit contents (items below can be ordered separately):

#	Part Number	Item	Quantity
1	EV2796-0002-FP-00A	MP2796DFP-0002 SPI evaluation board	1
2	EVKT-USBSPI-00	Includes one USB-to-SPI communication interface, one USB cable, and one ribbon cable	1
3	Online resources	Include datasheet, user guide, product brief, and GUI	1

Order directly from MonolithicPower.com or our distributors.

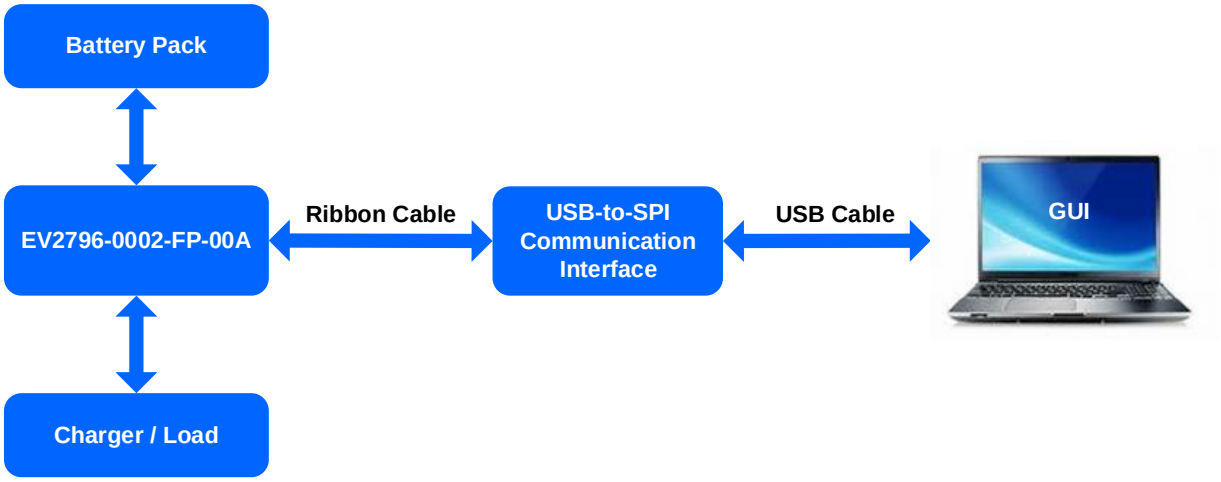

Figure 2: EV2796-0002-FP-00A Evaluation Kit Set-Up

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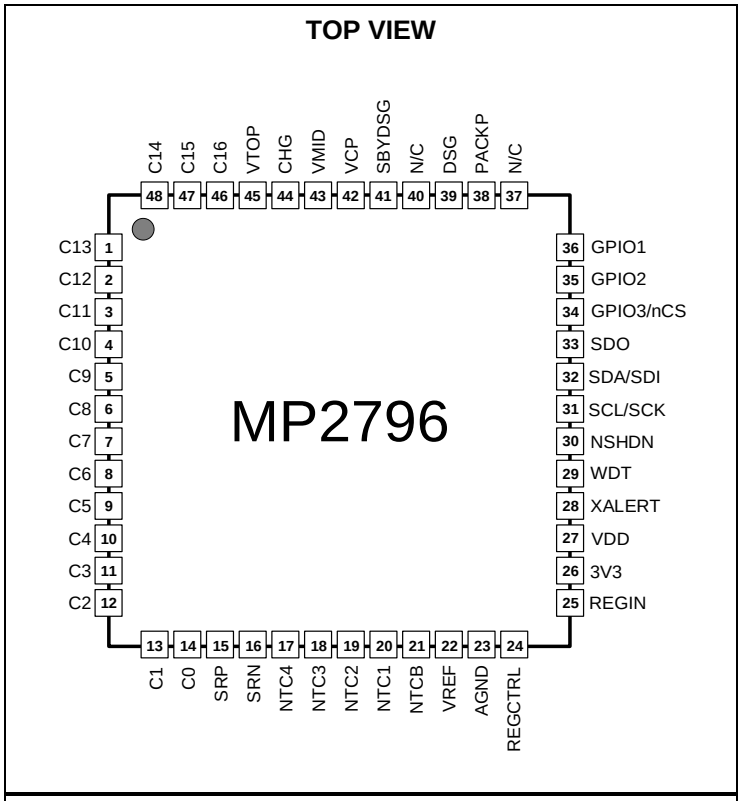
PACKAGE REFERENCE



TQFP-48 (7mmx7mm)

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PIN FUNCTIONS

Pin #	Name	Type	Description
26	3V3	P	**3.3V voltage output to drive external peripherals.** Bypass 3V3 with an external 1µF capacitor.
23	AGND	P	**Ground.** Connect AGND near the positive connection (SRP) of the low-side sense resistor.
45	VTOP	P	**Battery-side pack-sensing voltage and low-current positive supply pin.** VTOP must be connected to the top of the battery stack, which is the highest positive voltage in the battery pack.
46	C16	I	**Connect to the positive pin of cell 16.**
47	C15	I	**Connect to the positive pin of cell 15.**
48	C14	I	**Connect to the positive pin of cell 14.**
1	C13	I	**Connect to the positive pin of cell 13.**
2	C12	I	**Connect to the positive pin of cell 12.**
3	C11	I	**Connect to the positive pin of cell 11.**
4	C10	I	**Connect to the positive pin of cell 10.**
5	C9	I	**Connect to the positive pin of cell 9.**
6	C8	I	**Connect to the positive pin of cell 8.**
7	C7	I	**Connect to the positive pin of cell 7.**
8	C6	I	**Connect to the positive pin of cell 6.**
9	C5	I	**Connect to the positive pin of cell 5.**
10	C4	I	**Connect to the positive pin of cell 4.**
11	C3	I	**Connect to the positive pin of cell 3.**
12	C2	I	**Connect to the positive pin of cell 2.**
13	C1	I	**Connect to the positive pin of cell 1.**
14	C0	I	**Connect to the negative pin of cell 1.**
44	CHG	O	**Charge MOSFET driver.**
39	DSG	O	**Discharge MOSFET driver.**
36	GPIO1	I/O	**General-purpose pin 1.**
35	GPIO2	I/O	**General-purpose pin 2.**
37	N/C		**Not connected.**
30	NSHDN	I	**Active-low shutdown input signal.**
20	NTC1	I	**Thermistor 1 terminal.**
19	NTC2	I	**Thermistor 2 terminal.**
18	NTC3	I	**Thermistor 3 terminal.**
17	NTC4	I	**Thermistor 4 terminal.**
21	NTCB	O	**NTC bias.**
40	N/C		**Not connected.**
38	PACKP	I/O	**Pack sensing voltage (load side).**
24	REGCTRL	P	**Turn-on control for the external BJT low-dropout (LDO) regulator.**
25	REGIN	P	**Internal regulator input.** Connect an external 3.3µF bypass capacitor from REGIN to AGND.
41	SBYDSG	O	**Discharge bypass P-channel MOSFET driver.**
29	WDT	I/O	**Watchdog timer pin.**
28	xALERT	O	**Interrupt alert output.**
16	SRN	I	**Negative sense pin.**
15	SRP	I	**Positive sense pin.**
42	VCP	P	**Charge pump regulated voltage.** Connect a 47nF capacitor from VCP to VMID, then adjust the value based on the number of parallel DSG and CHG MOSFETs.
27	VDD	P	**1.8V rail for internal use.** Connect a 1µF bypass capacitor from VDD to AGND.
43	VMID	P	**Protection MOSFET middle point.**

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PIN FUNCTIONS *(continued)*

Pin #	Name	Type	Description
22	VREF	P	**Analog-to-digital converter (ADC) reference voltage.**
34	GPIO3/nCS	I/O	**Multi-function pin.** This pin can be set as GPIO3, or it can be set for SPI cable selection.
31	SCL/SCK	I	**Multi-function pin.** This pin can be set as the I^2C interface clock or the SPI interface clock.
32	SDA/SDI	I/O	**Multi-function pin.** This pin can be set as the I^2C interface data or the SPI serial data input.
33	SDO	O	**SPI serial data output.**

ABSOLUTE MAXIMUM RATINGS (1)

CHG, DSG, VCP to AGND .....-0.3V to +100V
SBYDSG to AGND.....-0.3V to +86V
VTOP to AGND.....-0.3V to +86V
PACKP to AGND .....-0.5V to +86V
VMID to AGND.....-0.3V to +86V
Cx - C(x - 1) (x: 1 to 16) .....-0.3V to +10V
C16 to AGND.....-0.3V to +86V
Cx to AGND (x: 1 to 15).....
..... -0.3V to (n - 1) x 5.375 + 7V
C0 to AGND .....-0.5V to +5.7V
SRP, SRN to AGND.....-0.5V to +6V
VCP to VMID.....-0.3V to +20V
REGCTRL to AGND .....-0.3V to +15V
NSHDN to AGND.....-0.3V to +9V
VDD to AGND.....-0.3V to +2V
All other pins to AGND.....-0.3V to +6V
Junction temperature .....150°C
Lead temperature.....260°C
Storage temperature..... - 65°C to +150°C

ESD Ratings

Human body model (HBM) (2)..... 1.5kV
Charged device model (CDM) (3)..... 500V

Recommended Operating Conditions (4)

VTOP voltage.....18V to 75.2V
Cx - C(x - 1) (x: 1 to 16) (5) .....1V to 5V
C0 to AGND..... -0.25V to +0.3V
REGIN voltage..... 4.5V to 5.5V
Operating temperature (T_J) ..... -40°C to +85°C
SRP to SRN .....-100mV to +100mV

Thermal Resistance (6)

Junction-to-ambient ($R_{\theta JA}$) ..... 46.6°C/W
Junction-to-case (top) ($R_{\theta JC(TOP)}$)..... 14.5°C/W
Junction-to-board (top) ($R_{\theta JB(TOP)}$) ..... 27.1°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) Tested per ANSI/ESDA/JEDEC JS-001.
3) Tested per ANSI/ESDA/JEDEC JS-002.
4) The device is not guaranteed to function outside of its operating conditions.
5) The stack voltage should exceed 18V.
6) Metrics provided using set-up conditions compliant with EIA/JESD51-2, 7, and 8.

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ELECTRICAL CHARACTERISTICS

Connected cells = 16, each cell voltage = 3.75V, V_{TOP} = 60V, T_A = 25°C, unless otherwise noted.

Parameter Name	Symbol	Condition	Min	Typ	Max	Units
Supply Current and Leakage						
Total shutdown current	I_{VTOP_SHDN}	VTOP + REGIN current, NSHDN pin low, 3.3V off, T_A = 25°C		1		µA
		VTOP + REGIN current, NSHDN pin low, 3.3V off, T_A = -40°C to +85°C			2.5	µA
		VTOP + REGIN current, 3.3V on, NSHDN pin low, T_A = 25°C		13.5		µA
		VTOP + REGIN current, 3.3V on, NSHDN pin low, T_A = -40°C to +85°C			20	µA
Total safe state current	I_{VTOP_SAFE}	VTOP + REGIN current, communication interface enabled, safe state (all MOSFETs off), hardware monitoring off, T_A = 25°C		23		µA
		VTOP + REGIN current, communication interface enabled, safe state (all MOSFETs off), hardware monitoring off, T_A = -40°C to +85°C			30	µA
Cell leakage	I_{Cx_LEAK}	T_A = 25°C	-200		+200	nA
		T_A = -40°C to +85°C	-600		+600	nA
Supported Series Cells						
Supported cell number (7)	N_{CELL}		7		16	
VTOP supply voltage range	V_{VTOP_SUPPLY}	T_A = -40°C to +85°C	18		75.2	V
VTOP under-voltage lockout (UVLO) threshold	V_{VTOP_UVLO}	Falling edge, T_A = -40°C to +85°C	14.6	15.8	17	V
VTOP under-voltage (UV) hysteresis	$V_{VTOP_UVLO_HYST}$	T_A = 25°C		1.15		V
		T_A = -40°C to +85°C	0.78		1.5	V
Current Sense						
Current analog-to-digital converter (ADC) conversion time	t_{IADC}	16 bits (15 bits + sign)		2		ms
Current ADC measurement range	V_{SRPN}	T_A = -40°C to +85°C	-100		+100	mV
Current ADC measurement gain error	$I_{ADC_GAIN_ERR}$	16-bit conversion, FSR = 100mV, SRP-N common mode: +300mV to -125mV from GND, T_A = 25°C	-0.5		+0.5	%
		16-bit conversion, FSR = 100mV, SRP-N common mode: +300mV to -125mV from GND, T_A = -40°C to 85°C	-1		+1	%

Note:

7) Guaranteed by design.

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ELECTRICAL CHARACTERISTICS *(continued)*

Connected cells = 16, each cell voltage = 3.75V, V_{TOP} = 60V, T_A = 25°C, unless otherwise noted.

Parameter Name	Symbol	Condition	Min	Typ	Max	Units
Current-sense offset (8)	$V_{IADC_ACC_OFFSET}$	SRP - SRN = 0V, SRP-N common mode: +300mV to -125mV from GND, T_A = -40°C to +85°C	-12		+12	µV
SRP and SRN leakage	I_{SRPN_LEAK}	IADC not running, T_A = -40°C to +85°C	-500		+500	nA
SRP and SRN differential input current	I_{SRPN_DIFF}	IADC running, |SPR - SRN| = 100mV, absolute value, T_A = -40°C to +85°C		0.5		µA
		IADC running, |SPR - SRN| < 5mV, T_A = -40°C to +85°C		50		nA
ADC Sigma Delta Voltage						
Voltage ADC conversion time	t_{VADC}	15 bits, T_A = 25°C		2		ms
Cell Voltage Measurement						
Cell ADC measurement range	V_{CELL}	T_A = -40°C to +85°C	1		5	V
Total cell measurement error	V_{CELL_ERR}	V_{CELL} = 2V to 4.5V, T_A = 25°C	-10		+10	mV
		V_{CELL} = 2V to 4.5V, T_A = -20°C to +65°C	-12.5		+12.5	mV
		V_{CELL} = 2V to 4.5V, T_A = -40°C to +85°C	-17.5		+17.5	mV
		V_{CELL} = 1V to 5V, T_A = -40°C to +85°C	-20		+20	mV
C0 to AGND voltage	$V_{C0_TO_AGND}$	C0 to AGND voltage drop resulting in less than 15mV error on cell 1, T_A = -40°C to +85°C	-0.25			V
Cell ADC input current	$I_{IN_CELL_CONV}$	Input current during ADC conversion when V_{CELL} = 5V, T_A = 25°C, cell 1 is measured by the C1 to C0 voltage		1.2		µA
Die Temperature						
Die temperature operating range	T_{DIE}		-40		+85	°C
Over-temperature (OT) analog shutdown threshold	T_{DIE_OTSD}			140	155	°C
Negative Temperature Coefficient (NTC) Temperature Measurement						
NTC voltage measurement range	V_{NTC}	Nominal NTC range within a percentage of NTCB, T_A = 25°C	0		100	%
NTC total measurement error	V_{NTC_ERR}	15-bit conversion, NTCB = 3.3V, T_A = -40°C to 85°C	-55		+55	LSB

Note:

8) Guaranteed by design. Cell current measurement offset error is specified after calibration. Contact an MPS FAE for the related application note.

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ELECTRICAL CHARACTERISTICS *(continued)*

Connected cells = 16, each cell voltage = 3.75V, V_{TOP} = 60V, T_A = 25°C, unless otherwise noted.

Parameter Name	Symbol	Condition	Min	Typ	Max	Units
NTCx input leakage	$I_{NTC_IN_LEAK}$	ADC off, on each NTC pin, T_A = -40°C to +85°C			250	nA
NTCx input leakage ADC on	$I_{NTC_LEAK_CONV}$	ADC converting NTCx, on each NTC pin, T_A = 25°C			250	nA
VTOP Measurement						
VTOP measurement range	V_{VTOP}	T_A = -40°C to +85°C	18		75.2	V
VTOP total measurement error	V_{VTOP_ERR}	15-bit conversion (positive range), T_A = -40°C to +85°C	-250		+250	mV
PACKP Measurement						
Pack measurement range	V_{PACKP}	T_A = -40°C to +85°C	2.5		75.2	V
Pack total measurement error	V_{PACKP_ERR}	15-bit conversion (positive range), T_A = -40°C to +85°C	-250		+250	mV
GPIO Measurement						
GPIO measurement range	V_{GPIO}	T_A = 25°C	0		3.3	V
GPIO total measurement error	V_{GPIO_ERR}	15-bit ADC reading, T_A = 25°C	-15		+15	mV
		15-bit ADC reading, T_A = -40°C to +85°C	-25		+25	mV
GPIO input current during ADC reading	$I_{GPIO_CONV_IN}$	GPIO pins input current during ADC conversion, T_A = -40°C to 85°C		1		µA
Regulators Measurements						
REGIN measurement error	V_{REGIN_ERR}	15-bit ADC reading, T_A = 25°C	-15		+15	mV
		15-bit ADC reading, T_A = -40°C to +85°C	-25		+25	mV
3V3 total measurement error	V_{3V3_ERR}	15-bit ADC reading, T_A = 25°C	-15		+15	mV
		15-bit ADC reading, T_A = -40°C to +85°C	-25		+25	mV
VDD total measurement error	V_{VDD_ERR}	15-bit ADC reading, T_A = 25°C	-15		+15	mV
		15-bit ADC reading, T_A = -40°C to +85°C	-25		+25	mV
Hardware Protection						
Cell over-voltage (OV) and UV steps	$V_{CELL_TH_STEP}$			19.5		mV
Cell OV/UV step accuracy	$V_{CELL_TH_ACC}$	V_{CELL} = 2V to 4.5V, T_A = 0°C to 60°C	-19.5		+19.5	mV
		V_{CELL} = 1V to 5V, T_A = -40°C to +85°C	-40		+40	mV

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ELECTRICAL CHARACTERISTICS *(continued)*

Connected cells = 16, each cell voltage = 3.75V, V_{TOP} = 60V, T_A = 25°C, unless otherwise noted.

Parameter Name	Symbol	Condition	Min	Typ	Max	Units
Pack OV/UV steps	$V_{PACK_TH_STEP}$			19.5		mV
Deep discharge steps	V_{DEEPTH_STEP}			19.5		mV
Deep discharge step accuracy	$V_{DEEPTH_STEP_ACC}$	V_{CELL} = 2V to 4.5V, T_A = 0°C to 60°C	-19.5		+19.5	mV
		V_{CELL} = 1V to 5V, T_A = -40°C to +85°C	-40		+40	mV
SC fastest detection time	$t_{SC_DGL_MIN}$	Fastest deglitch setting and latency, T_A = -40°C to +85°C			120	µs
OC1 discharge FSR value	$V_{OC1_DSG_FSR_1X}$	Range and LSB selector = 0 (1x), FSR (max setting), T_A = 25°C		80		mV
OC1 discharge full scale accuracy	$V_{OC1_DSG_FSR_1X_ACC}$	Range and LSB selector = 0 (1x), FSR (max setting), T_A = -40°C to +85°C	-15		+15	%
OC1 discharge offset	$V_{OC1_DSG_FSR_1X_OFF}$	Range and LSB selector = 0 (1x), offset on LSB, T_A = -40°C to +85°C	-1.5		+1.5	mV
OC1 discharge FSR value	$V_{OC1_DSG_FSR_3X}$	Range and LSB selector = 1 (3x), FSR (max setting), T_A = 25°C		240		mV
OC1 discharge full scale accuracy	$V_{OC1_DSG_FSR_3X_ACC}$	Range and LSB selector = 1 (3x), FSR (max setting), T_A = -40°C to +85°C	-15		+15	%
OC1 discharge offset	$V_{OC1_DSG_FSR_3X_OFF}$	Range and LSB selector = 1 (3x), offset on smallest setting, T_A = -40°C to +85°C	-1.5		+1.5	mV
OC2 discharge FSR value	$V_{OC2_DSG_FSR_1X}$	Range and LSB selector = 0 (1x), FSR (max setting), T_A = 25°C		80		mV
OC2 discharge full scale accuracy	$V_{OC2_DSG_FSR_1X_ACC}$	Range and LSB selector = 0 (1x), FSR (max setting), T_A = -40°C to +85°C	-15		+15	%
OC2 discharge offset	$V_{OC2_DSG_FSR_1X_OFF}$	Range and LSB selector = 0 (1x), offset on smallest setting, T_A = -40°C to 85°C	-1.5		+1.5	mV
OC2 discharge FSR value	$V_{OC2_DSG_FSR_3X}$	Range and LSB selector = 1 (3x), FSR (max setting), T_A = 25°C		240		mV
OC2 discharge full scale accuracy	$V_{OC2_DSG_FSR_3X_ACC}$	Range and LSB selector = 1 (3x), FSR (max setting), T_A = -40°C to 85°C	-15		+15	%
OC2 discharge offset	$V_{OC2_DSG_FSR_3X_OFF}$	Range and LSB selector = 1 (3x), offset on smallest setting, T_A = -40°C to +85°C	-1.5		+1.5	mV
OC charge FSR value	$V_{OC_CHG_FSR_1X}$	Range and LSB selector = 0 (1x), FSR (max setting), T_A = 25°C		51.2		mV

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ELECTRICAL CHARACTERISTICS *(continued)*

Connected cells = 16, each cell voltage = 3.75V, V_{TOP} = 60V, T_A = 25°C, unless otherwise noted.

Parameter Name	Symbol	Condition	Min	Typ	Max	Units
OC charge full scale accuracy	$V_{OC_CHG_FSR_1X_ACC}$	Range and LSB selector = 0 (1x), FSR (max setting), T_A = -40°C to +85°C	-15		+15	%
OC charge offset	$V_{OC_CHG_FSR_1X_OFF}$	Range and LSB selector = 0 (1x), offset on smallest setting, T_A = -40°C to +85°C	-1.5		+1.5	mV
OC charge FSR value	$V_{OC_CHG_FSR_3X}$	Range and LSB selector = 1 (3x), FSR (max setting), T_A = 25°C		153		mV
OC charge full scale accuracy	$V_{OC_CHG_FSR_3X_ACC}$	Range and LSB selector = 1 (3x), FSR (max setting), T_A = -40°C to +85°C	-15		+15	%
OC charge offset	$V_{OC_CHG_FSR_3X_OFF}$	Range and LSB selector = 1 (3x), offset on smallest setting, T_A = -40°C to +85°C	-1.5		+1.5	mV
SC discharge FSR value	$V_{SC_DSG_FSR_1X}$	Range and LSB selector = 0 (1x), FSR (max setting), T_A = 25°C		176		mV
SC discharge full scale accuracy	$V_{SC_DSG_FSR_1X_ACC}$	Range and LSB selector = 0 (1x), FSR (max setting), T_A = -40°C to +85°C	-15		+15	%
SC discharge offset	$V_{SC_DSG_FSR_1X_OFF}$	Range and LSB selector = 0 (1x), offset on smallest setting, T_A = -40°C to +85°C	-1.5		+1.5	mV
SC discharge FSR value	$V_{SC_DSG_FSR_3X}$	Range and LSB selector = 1 (3x), FSR (max setting), T_A = 25°C		528		mV
SC discharge full scale accuracy	$V_{SC_DSG_FSR_3X_ACC}$	Range and LSB selector = 1 (3x), FSR (max setting), T_A = -40°C to +85°C	-15		+15	%
SC discharge offset	$V_{SC_DSG_FSR_3X_OFF}$	Range and LSB selector = 1 (3x), offset on smallest setting, T_A = -40°C to +85°C	-2		+2	mV
SC charge FSR value	$V_{SC_CHG_FSR_1X}$	Range and LSB selector = 0 (1x), FSR (max setting), T_A = 25°C		80		mV
SC charge full scale accuracy	$V_{SC_CHG_FSR_1X_ACC}$	Range and LSB selector = 0 (1x), FSR (max setting), T_A = -40°C to +85°C	-15		+15	%
SC charge offset	$V_{SC_CHG_FSR_1X_OFF}$	Range and LSB selector = 0 (1x), offset on smallest setting, T_A = -40°C to +85°C	-1.5		+1.5	mV
SC charge FSR value	$V_{SC_CHG_FSR_3X}$	Range and LSB selector = 1 (3x), FSR (max setting), T_A = 25°C		240		mV
SC charge full scale accuracy	$V_{SC_CHG_FSR_3X_ACC}$	Range and LSB selector = 1 (3x), FSR (max setting), T_A = -40°C to +85°C	-15		+15	%

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ELECTRICAL CHARACTERISTICS *(continued)*

Connected cells = 16, each cell voltage = 3.75V, V_{TOP} = 60V, T_A = 25°C, unless otherwise noted.

Parameter Name	Symbol	Condition	Min	Typ	Max	Units
SC charge offset	$V_{SC_CHG_FSR_3X_OFF}$	Range and LSB selector = 1 (3x), offset on smallest setting, T_A = -40°C to +85°C	-1.5		+1.5	mV
Cell-Balancing						
On resistance ($R_{DS(ON)}$) for the balancing MOSFET	$R_{DS(ON)_BAL_FET}$	T_A = 25°C		28		Ω
		T_A = -40°C to +85°C	15		50	Ω
Open Wire						
Open-wire pull-up current	I_{OW_PUP}	T_A = 25°C		100		µA
Open-wire pull-down current	I_{OW_PD}	T_A = 25°C		100		µA
Low-Dropout Regulator (LDO) Supply and References						
REGCTRL output voltage	$V_{REGCTRL}$	V_{TOP} = 18V to 75.2V, with REGCTRL load current = 0mA and 1mA, T_A = -40°C to +85°C	5.45	5.6	5.75	V
REGIN voltage (9)	V_{REGIN}	With external REGIN BJT_FZT853TA, V_{TOP} = 18V to 75.2V, with load current = 1mA and 50mA, T_A = -40°C to +85°C	4.65	5.1	5.4	V
REGIN analog UV	V_{REGIN_UV}	External power to REGIN, falling edge, V_{TOP} = 18V to 75.2V, T_A = -40°C to +85°C	4.16	4.3	4.44	V
3V3 nominal voltage	V_{3V3}	T_A = 25°C		3.3		V
3V3 output accuracy	V_{3V3_ACC}	T_A = -40°C to +85°C	-5		+5	%
3V3 short-circuit current	I_{3V3_EFET}	External power to REGIN, T_A = -40°C to +85°C	55	68	80	mA
VDD output voltage	V_{DD}	T_A = 25°C		1.8		V
Reference voltage	V_{REF}	T_A = 25°C		3.3		V
NTCB pull-up voltage	V_{NTCB}	NTCB enabled, no load, T_A = 25°C		3.3		V
NTCB load	$I_{NTCB_MAXLOAD}$	NTCB enabled, max load, T_A = 25°C		4		mA
		NTCB enabled, max load, T_A = -40°C to +85°C	3.2		4.8	mA
3V3 analog UV	V_{3V3_UV}	Falling edge		2.85		V
GPIO						
GPIO input voltage (high)	V_{IH_GPIO}	Voltage high (V_H) = 3.3V or 5V, T_A = -40°C to +85°C	0.8 x V_H		V_H	V
GPIO input voltage (low)	V_{IL_GPIO}	V_H = 3.3V or 5V, T_A = -40°C to +85°C	0		0.2 x V_H	V
GPIO output voltage (high)	V_{OH_GPIO}	V_H = 3.3V or 5V, I_{SOURCE} = 1.5mA, T_A = -40°C to +85°C	V_H - 0.5		V_H	V

Note:

9) Guaranteed by design. The REGIN voltage is limited by the $V_{REGCTRL}$ and is equal to $V_{REGCTRL}$ - V_{BE_ON}.

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ELECTRICAL CHARACTERISTICS *(continued)*

Connected cells = 16, each cell voltage = 3.75V, V_{TOP} = 60V, T_A = 25°C, unless otherwise noted.

Parameter Name	Symbol	Condition	Min	Typ	Max	Units
GPIO output voltage (low)	$V_{OL-GPIO}$	V_H= 3.3V or 5V, I_{SINK} = 1.5mA, T_A = -40°C to +85°C	0		0.4	V
GPIO push-pull resistor (up)	R_{GPIO_PUP}	GPIO high voltage = 3.3V, external power to REGIN		430		Ω
GPIO push-pull resistor (down)	R_{GPIO_PDOWN}	GPIO low voltage = 0V		110	200	Ω
GPIO pull-up mode	$R_{GPIO_WEAK_PUP}$			17		kΩ
NSHDN Pin						
NSHDN internal pull down	R_{SHDN_PD}	NSHDN 0V to 5V		5		MΩ
NSHDN configuring voltage	V_{NSHDN_PROG}		7.5	7.6	7.7	V
NSHDN deglitch to enter shutdown	$t_{NSHDN_DGL_ENTER}$	T_A = 25°C, IC stays in safe mode for longer than $t_{NSHDN_DGL_ACTIVE}$		8		ms
NSHDN deglitch active time	$t_{NSHDN_DGL_ACTIVE}$	T_A = 25°C		4		ms
NSHDN falling threshold	V_{NSHDN_FALL}			1		V
NSHDN rising threshold	V_{NSHDN_RISE}	3V3 enabled at shutdown mode		2.65		V
		3V3 disabled at shutdown mode		2		V
WDT Pin						
Reset pulse length	$t_{WDT_RSTPULSE_LEN}$			10		ms
High-Side MOSFET (HS-FET) Drive						
CHG gate drive voltage	V_{CHG}	C_{LOAD} = 80nF, static value at transition completed, V_{TOP} = 18V to 75.2V, V_{GS} = 10V, T_A = 25°C		10		V
CHG gate drive voltage accuracy	V_{CHG_ACC}	C_{LOAD} = 80nF, static value at transition completed, V_{TOP} = 18V to 75.2V, 10V selected, T_A = -40°C to +85°C	9.3		10.7	V
CHG gate drive turn-on resistance	R_{CHG_ON}	MOSFET drive turned on, PACKP = V_{TOP}, T_A = 25°C		2600		Ω
CHG gate driver turn-off resistance	R_{CHG_OFF}	MOSFET driver turned off, PACKP = V_{TOP}, T_A = 25°C		840		Ω
DSG gate drive voltage	V_{DSG}	C_{LOAD} = 80nF, static value at transition completed, V_{TOP} = 18V to 75.2V, V_{GS} = 10V, T_A = 25°C		10		V
DSG gate driver voltage accuracy	V_{DSG_ACC}	C_{LOAD} = 80nF, static value at transition completed, V_{TOP} = 18V to 75.2V, 10V selected, T_A = -40°C to +85°C	9.3		10.7	V

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ELECTRICAL CHARACTERISTICS *(continued)*

Connected cells = 16, each cell voltage = 3.75V, V_{TOP} = 60V, T_A = 25°C, unless otherwise noted.

Parameter Name	Symbol	Condition	Min	Typ	Max	Units
DSG gate driver turn-on resistance	R_{DSG_ON}	MOSFET driver turned on, PACKP = V_{TOP}, T_A = 25°C		2600		Ω
DSG gate driver turn-off resistance	R_{DSG_OFF}	MOSFET driver turned off, PACKP = V_{TOP}, DSG = PACKP + 5V, T_A = 25°C		600		Ω
SBYDSG gate driver voltage	V_{SBYDSG}	C_{LOAD} = 10nF, static value at completed transition, V_{TOP} = 18V to 75.2V, V_{GS} = -10V, T_A = -40°C to +85°C	-12	-10	-9	V
SBYDSG gate driver on resistance	R_{SBYDSG_ON}	MOSFET driver turned on, T_A = -40°C to +85°C		14.3		kΩ
SBYDSG gate driver off resistance	R_{SBYDSG_OFF}	MOSFET driver turned off, T_A = -40°C to +85°C		2.7		kΩ
Charge Pump						
Charge pump output voltage	V_{CP}	Gate driver voltage = 10V, regular control mode, T_A = 25°C		14.7		V
Charge pump output voltage accuracy	V_{CP_ACC}	Accuracy of select VCP average value, T_A = -40°C to +85°C	-1		+1	V
Charge pump turn-on time	t_{CP_TON}	VCP - AGND transition from V_{TOP} to V_{TOP} + VCP, 10nF capacitor on VCP, V_{TOP} = 21V, for both low-power mode and regular control mode, T_A = -40 to +85°C			2	ms
Pull-Up Comparators						
PACKP charge	I_{PACKP_PUP}	V_{TOP} = 18V to 75.2V, T_A = 25°C		250		μA
PACKP discharge	I_{PACKP_PDOWN}	V_{TOP} = 18V to 75.2V, T_A = 25°C		250		μA
PACKP exceeds V_{TOP}	$V_{PACKP_HGR_VTOP}$	V_{TOP} = 18V to 75.2V, T_A = 25°C		280		mV
PACKP is below V_{TOP}	$V_{PACKP_LWR_VTOP}$	V_{TOP} = 18V to 75.2V, T_A = 25°C		-1.77		V
Standby comparator accuracy	$V_{SBY_COMP_ACCU}$	Offset on the smallest setting, T_A = 25°C	-125		+125	μV
PACKP short recovery threshold	$V_{PACKP_SCOC_REC_TH}$	T_A = 25°C		110		mV
Short recovery current-source accuracy	I_{SCOC_PUP}	Offset on the smallest setting, T_A = 25°C	-50		+50	μA
Internal Clock						
Internal clock frequency	f_{2M_CLOCK}	V_{TOP} = 18V to 75.2V, T_A = 25°C		2		MHz
		V_{TOP} = 18V to 75.2V, T_A = -40°C to +85°C	1.85	2	2.15	MHz
Low-frequency internal clock	f_{32K_CLOCK}	V_{TOP} = 18V to 75.2V, T_A = 25°C	31.2	32	32.8	kHz
		V_{TOP} = 18V to 75.2V, T_A = -40°C to +85°C	30.7		33.3	kHz

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ELECTRICAL CHARACTERISTICS *(continued)*

Connected cells = 16, each cell voltage = 3.75V, V_{TOP} = 60V, T_A = 25°C, unless otherwise noted.

Parameter Name	Symbol	Condition	Min	Typ	Max	Units
I²C Communication Interface						
I²C clock frequency	f_{I2C}	T_A = 25°C			400	kHz
SCL, SDA low input voltage	V_{ILOW}	T_A = -40°C to +85°C			0.25 x 3V3	V
SCL, SDA high input voltage	V_{IHIGH}	T_A = -40°C to +85°C	0.7 x 3V3			V
SCL, SDA input hysteresis	V_{IHYST}	T_A = -40°C to +85°C		0.2 x 3V3		V
SPI Communication Interface						
SPI clock frequency	f_{SPI}	T_A = 25°C			1.0	MHz
SPI input low	$V_{SPI_IN_LOW}$	SDI, CLK, T_A = -40°C to +85°C			0.25 x 3V3	V
SPI input high	$V_{SPI_IN_HIGH}$	SDI, CLK, T_A = -40°C to +85°C	0.7 x 3V3			V
SDO high-side (HS) on resistance	$R_{SDO_DRV_HI}$	I_{SOURCE} = 1.5mA, T_A = -40°C to +85°C	75	100	125	Ω
SDO low-side (LS) on resistance	$R_{SDO_DRV_LOW}$	I_{SINK} = 1.5mA, T_A = -40°C to +85°C	38	52	66	Ω

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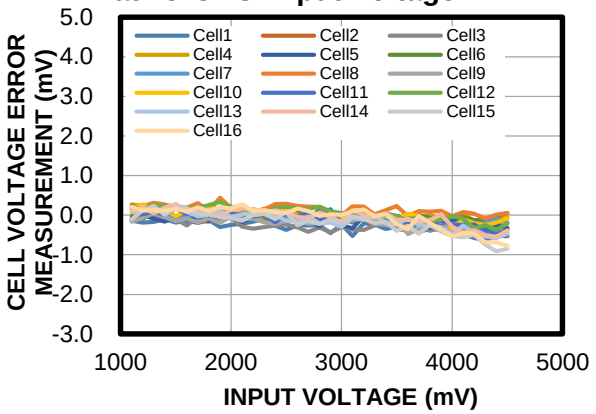
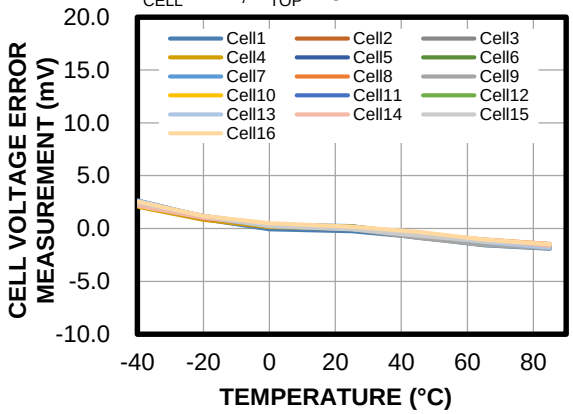
TYPICAL PERFORMANCE CHARACTERISTICS

Cell Voltage Error Measurement at 25°C vs. Input Voltage



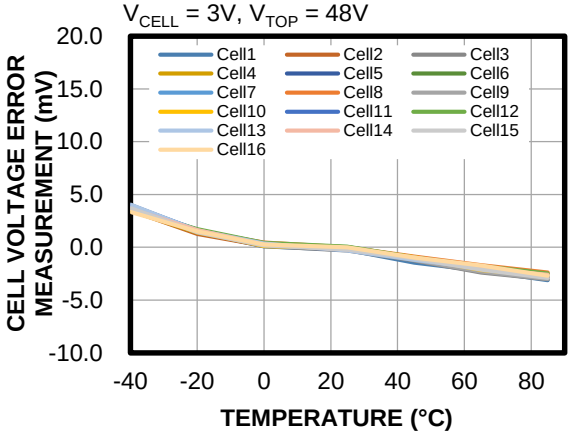
Cell Voltage Error Measurement vs. Temperature

V_{CELL} = 2V, V_{TOP} = 32V



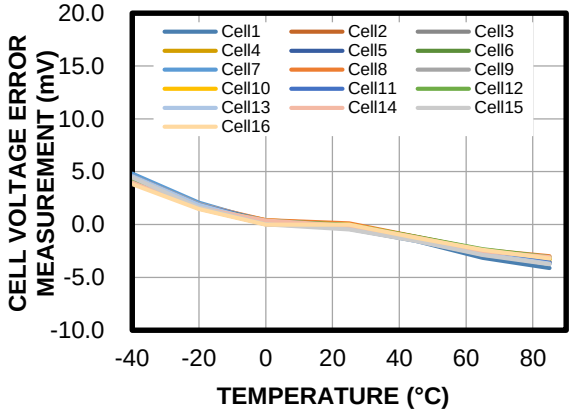
Cell Voltage Error Measurement vs. Temperature

V_{CELL} = 3V, V_{TOP} = 48V



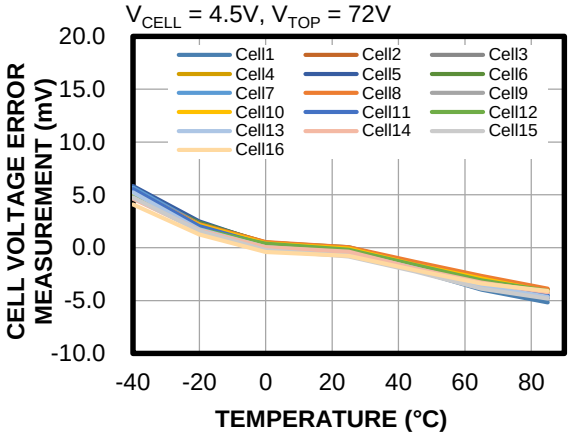
Cell Voltage Error Measurement vs. Temperature

V_{CELL} = 3.7V, V_{TOP} = 59.2V



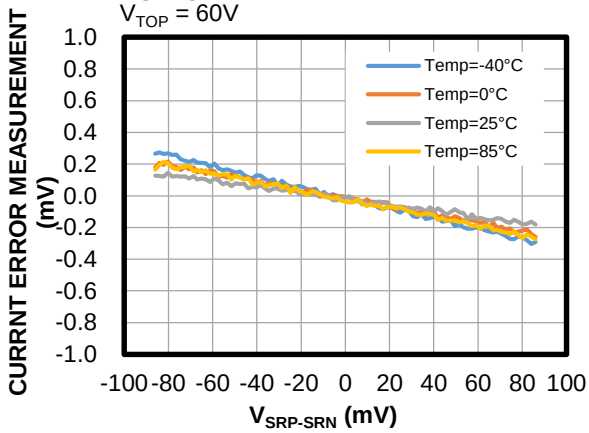
Cell Voltage Error Measurement vs. Temperature

V_{CELL} = 4.5V, V_{TOP} = 72V



Current Error Measurement vs. $V_{SRP-SRN}$

V_{TOP} = 60V



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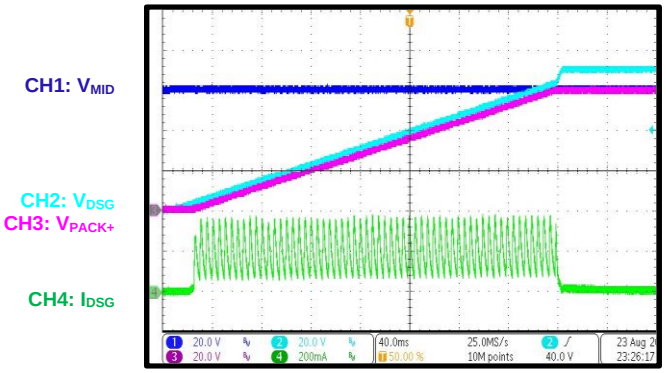
TYPICAL PERFORMANCE CHARACTERISTICS

Performance curves and waveforms are tested on the evaluation board. V_{TOP} = 60V, T_A = 25°C, unless otherwise noted.

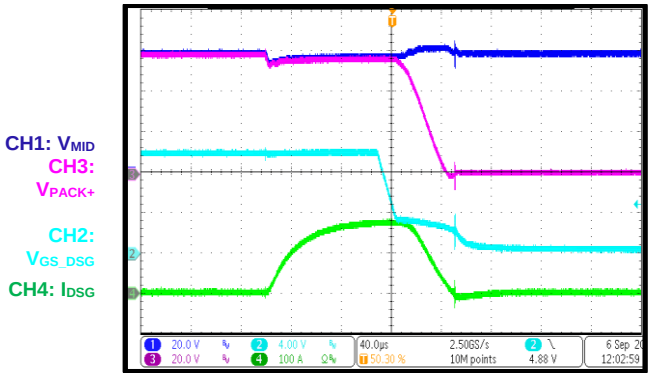
DSG Soft Start

PACK+ is connected to a 1mF capacitor, the DSG slope is 0.2V/ms



DSG Fast-Off in Short-Circuit

$R_{SRP-SRN}$ = 1mΩ, short-circuit threshold is 99mV, deglitch off, 4 paralleled AM90N08-04BA devices act as the DSG N-channel MOSFETs, which has a typical C_{ISS} of 9924pF



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TYPICAL PERFORMANCE WHEN PAIRED WITH MPF4279X FUEL GAUGE

The MP2796 battery monitor includes strictly synchronized cell and pack voltage and current measurements, for the purpose of maximizing state-of-charge (SOC) determination. MPS' MPF4279x family of fuel gauges are designed to take advantage of this feature. This section illustrates the SOC accuracy of the MP2796 battery monitor when combined with MPS' MPF4279x fuel gauge family.

Constant-Current/Constant-Voltage (CC/CV) Charge and Dynamic Discharge Cycle

The next scenarios consist of charging a 10S1P [10] battery using the typical CC/CV method, followed by a highly dynamic discharge at different ambient temperatures. The charge constant current rate is 1C, while the charge termination current in this example is 0.1C. The highly dynamic discharge corresponds to a typical e-bike's current profile, with an average current of 1C and maximum peak currents up to 2.8C. Figure 3 shows the current profile of the complete cycle at 25°C.

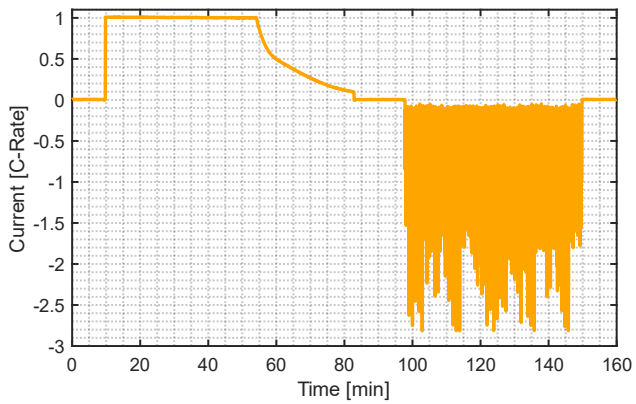

Figure 3: CC/CV Charge and Dynamic Discharge Current Profile

Figure 4 shows the performance of the combined MP2796 and MPF42791 for the CC/CV charge and dynamic discharge cycle at an ambient temperature of 25°C. During charge, the root-mean-squared (RMS) [11] and maximum pack SOC error are 0.61% and 1.03%, respectively. During discharge, the root-mean-squared and pack SOC error are 0.78% and 1.94%, respectively.

Notes:

10) 10S1P refers to the battery configuration. There are 10 groups of 1 parallel cell connected in series.

11) The RMS error is equal to $\sqrt{\frac{\sum_{n=1}^{N}(\theta_n-\hat{\theta}_n)^2}{N}}$, where θ is the actual SOC, $\hat{\theta}$ is the estimated SOC, and N is the number of samples.

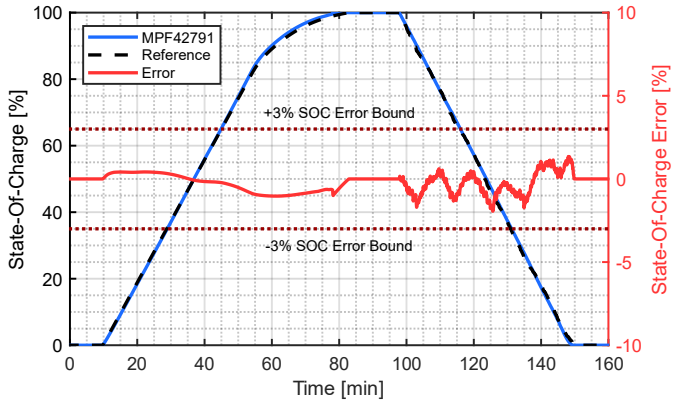

Figure 4: Combined MP2796 + MPF42791 Performance for a CC/CV Charge and Dynamic Discharge (Ambient Temperature = 25°C)

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Figure 5 shows the performance of the combined MP2796 and MPF42791 for the CC/CV charge and dynamic discharge cycle at an ambient temperature of 0°C. During charge, the root-mean-squared and maximum pack SOC error are 0.68% and 1.22%, respectively. During discharge, the root-mean-squared and pack SOC error are 1.15% and 2.97%, respectively.

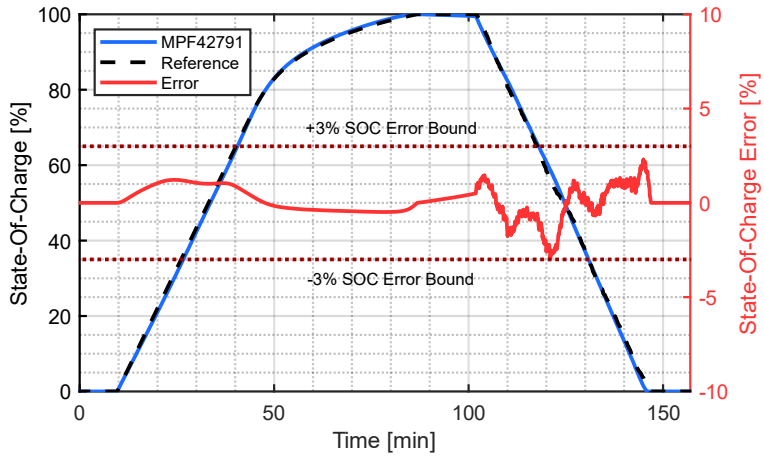

Figure 5: Combined MP2796 + MPF42791 Performance for a CC/CV Charge and Dynamic Discharge (Ambient Temperature = 0°C)

Figure 6 shows the performance of the combined MP2796 and MPF42791 for the CC/CV charge and dynamic discharge cycle at an ambient temperature of 40°C. During charge, the root-mean-squared and maximum pack SOC error are 0.40% and 0.60%, respectively. During discharge, the root-mean-squared and pack SOC error are 0.77% and 1.89%, respectively.

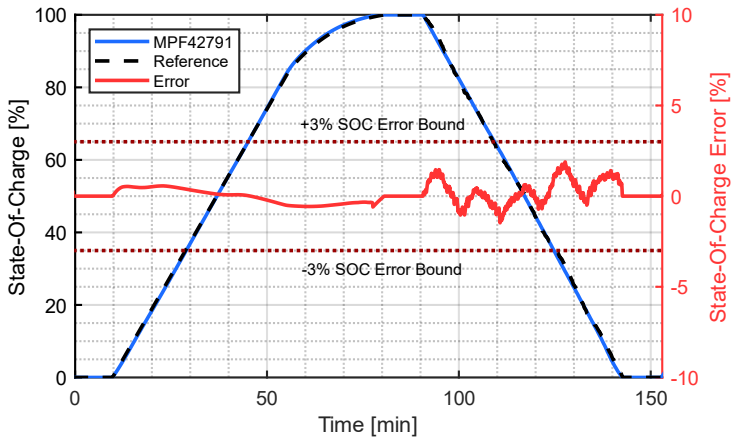

Figure 6: Combined MP2796 + MPF42791 Performance for a CC/CV Charge and Dynamic Discharge (Ambient Temperature = 40°C)

Performance Summary

This section provides a summary the combined MP2796 and MPF42791 real-world performance. Table 1 shows a summary of the pack SOC performance metrics for a 10S1P battery.

Table 1: MPF42791 SOC Root-Mean-Squared (and Maximum) Error

Test Case	0°C	25°C	40°C
CC/CV charge	0.68% (1.22%)	0.61% (1.03%)	0.40% (0.60%)
Dynamic discharge	1.15% (2.97%)	0.78% (1.94%)	0.77% (1.89%)

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FUNCTIONAL BLOCK DIAGRAM

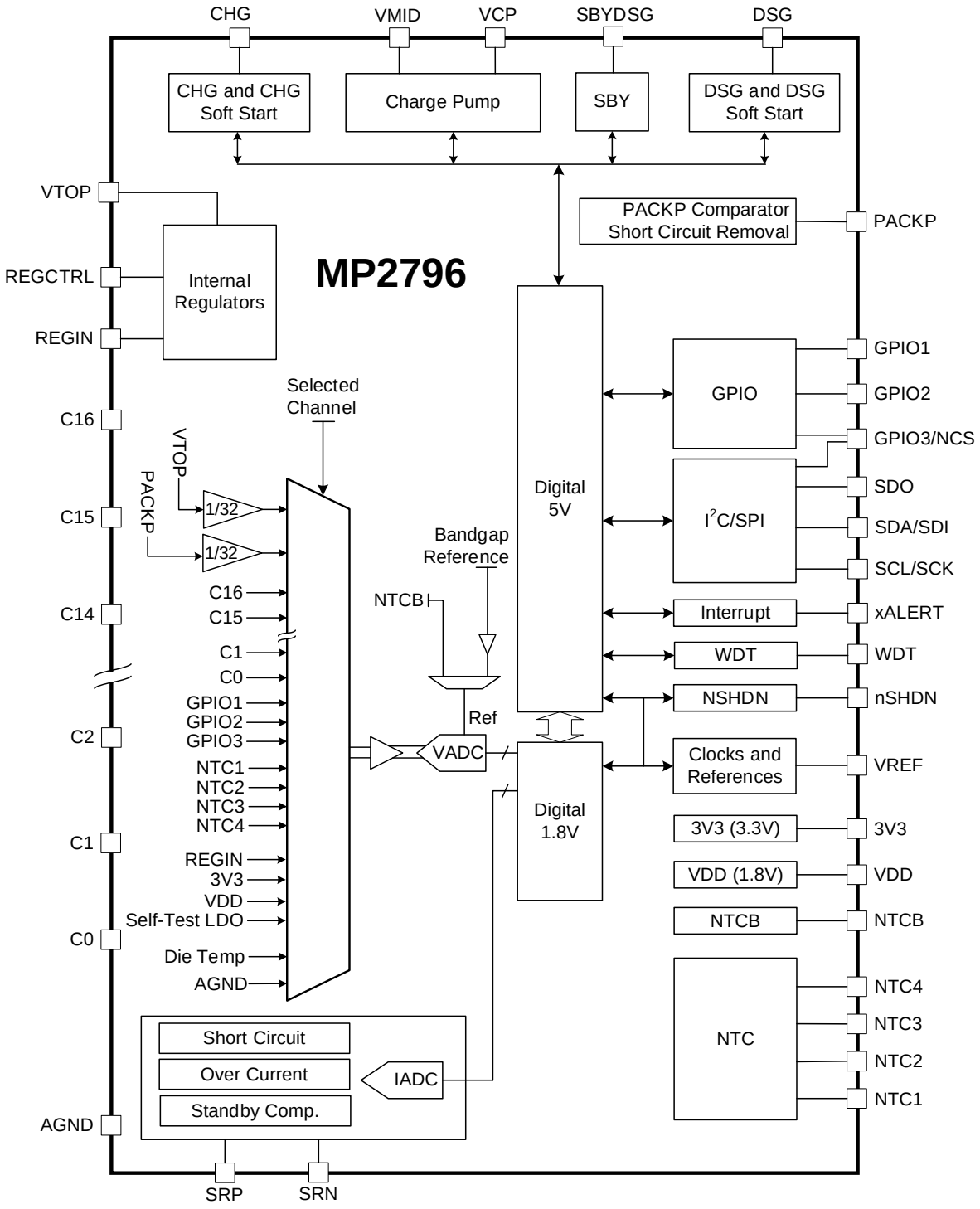

Figure 7: Functional Block Diagram

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OPERATION

Main Modes

The MP2796's main operation modes are listed and described below (see Figure 8).

Shutdown Mode

It is vital to preserve a battery's capacity. Shutdown mode minimizes the amount of leakage from the battery pack, which extends the battery pack's shelf storage life.

In shutdown mode, the communication interface is unavailable and REGIN is loosely regulated, which means its voltage is below the normal voltage without any load capacity. However, it is possible to keep 3.3V active in shutdown mode with a slight margin for current consumption.

Pull the NSHDN pin to ground to enter shutdown mode.

Safe Mode

To enter safe mode from shutdown mode, pull up the NSHDN pin and wait at least 5ms before issuing an I^2C or SPI command. If any functional commands are required in safe mode (e.g. high-resolution voltage scanning, Coulomb counting, MOSFETs turn-on, voltage protection monitoring, open wire, and cell-balancing), then the I^2C or SPI bus must be idle for at least 200µs after the functional command in enabled.

Safe mode is characterized by the following conditions:

- The protection MOSFETs turn off.
- The over-voltage (OV) and under-voltage (UV) hardware autonomous protection state machine is disabled, unless it is forcibly enabled.
- The communication interface is enabled.

To leave safe mode, see the Protection MOSFET Enable Control section on page 23.

In safe mode, it is possible enable protection monitoring (cell OV, cell UV, and current monitoring).

Active Mode

In active mode, the high-side drivers turn on, and the BMS can be powered or be charged by a downstream system through the CHG and DSG N-channel MOSFETs.

Standby Mode

Standby mode reduces current consumption by using a standby P-channel MOSFET to power the system (instead of DSG N-channel MOSFET), and conducts through the CHG N-channel MOSFET's body diode. To enter standby mode, standby mode must be enabled, and the current must be below the standby current threshold.

In standby mode, the time between ADC voltage conversions used for protection monitoring can be independently lengthened via the STBY_MONITOR_CFG register. This reduces the average current consumption.

Fault Mode

In fault mode, both the CHG and DSG MOSFET drivers turn off in response to a fault event. Protection monitoring is still enabled during a fault.

Fault mode can be cleared manually or through automatic fault recovery, depending on the configuration.

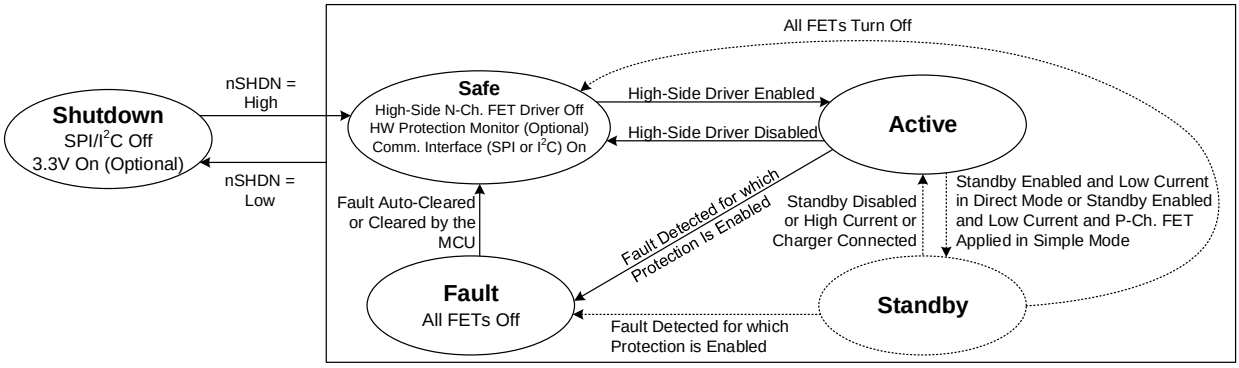

Figure 8: Main States Diagram

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Registers (Default and Lock)

Most of the configuration settings and options have a configurable default value. Certain registers can be configured independently, or they can be locked in read-only mode. This prevents critical safety features from being changed.

Protection MOSFET Enable Control

The MP2796 can leave safe mode and enter active mode via pin control or register control, though only one control method can be selected at a time. The FET_SRC register can be set using either the register (ACTIVE_CTRL register) or pin (GPIO1/2) to determine whether the device should remain in safe mode or active mode.

There are two control strategies that can be selected via the FET_CFG register: simple or direct. Table 2 lists the BMS behavior in simple mode, where a single control is offered for both the charge and the discharge driver. The system internally handles the MOSFETs' turn-on and turn-off sequences.

Table 2: Protection MOSFETs (Simple Mode)

Configuration: FET_SRC = GPIO, Standby P-Channel MOSFET Disabled			
MOSFET	**GPIO1 = Low**	**GPIO1 = High**	**GPIO1 = High**
		Fault	**No Fault**
CHG N-channel MOSFET	Off	Off	On
DSG N-channel MOSFET	Off	Off	On

Table 3 describes how the BMS behaves in direct mode, in which each driver (charge MOSFET driver and discharge MOSFET driver) can be directly controlled.

Table 3: Protection MOSFETs (Direct Mode)

Configuration: FET_SRC = GPIO, Standby P-Channel MOSFET Disabled					
MOSFET	**GPIO1 = Low GPIO2 = Low**	**Fault**	**No Fault**		
			GPIO1 = High GPIO2 = Low	**GPIO1 = Low GPIO2 = High**	**GPIO1 = High GPIO2 = High**
CHG N-channel MOSFET	Off	Off	Off	On	On
DSG N-channel MOSFET	Off	Off	On	Off	On

MOSFET Driving Ability

The high-side MOSFET (HS-FET) driver can drive multiple DSG/CHG FETs in parallel. The VCP capacitor value must be increased, depending on the number of parallel MOSFETs in the application.

DSG MOSFET Soft Start (SS) (12)

One of the biggest challenges when designing a BMS with HS-FETs is limiting the inrush current and protecting the DSG MOSFET from exceeding its safe operating area (SOA) while it turns on when a large capacitive load is present.

To address this issue, most system designers add what is commonly referred to as a pre-charge or pre-biased external circuit. This type of external circuit requires additional MOSFETs and physically large power resistors, which limit the discharge current while the load capacitance is charging. To reduce the significant size and cost of this circuit, the MP2796's DSG N-channel MOSFET driver includes an innovative soft start (SS) discharge MOSFET control circuit.

SS controls the rising slope of the DSG voltage by setting the DSG_SOFTON_DV bits, and thereby reducing the discharging current. To ensure that the DSG MOSFET's SOA is not exceeded during SS, the MP2796 uses 3 separate over-current (OC) comparators.

Note:

12) For detailed design guidelines on how to configure the DSG MOSFET SS settings, contact an MPS FAE for the related application note.

CHG MOSFET Soft Start (SS)

The CHG MOSFET driver supports a configurable SS via the CHG_SOFTON_PUP register to set the pull-up current values (ranging between 3μA and 10μA). When CHG_SOFTON_EN is enabled and V_{PACKP} exceeds V_{TOP}, the MOSFET drive circuit

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automatically uses CHG SS to control the CHG pin's output current, so that V_{GS} rises slowly.

GPIO Pins

The GPIO pins can be directly controlled by the MCU through registers, or they can be assigned to special functions. The GPIO pins have the following functions:

- Push-pull output: The pull-up voltage can be configured to REGIN or 3V3.
- Pull-up capability: Connect a 20kΩ pull-up resistor to REGIN or 3V3.
- Digital input.
- Analog input: Can act as a buffered ADC input with a 0V to 3.3V range.

In addition to the GPIO functions, the GPIO1 and GPIO2 pins can also enable certain protections (see the Protection MOSFET Enable Control section on page 23).

In addition to the GPIO capability, the GPIO3 pin can be configured to initiate automatic cell-balancing (as an input), or indicate fault status (as an output).

WDT Pin

The WDT pin is controlled by the watchdog timer (WDT), and provides the following functions:

- Toggles with a high pulse when a watchdog event occurs to reset an external IC (e.g. the host MCU).
- Triggers a self-reset to the IC by bringing the device back to its default values.
- Can be pulled high externally to reset the device.

Alert (xALERT)

The xALERT pin can be configured to be an active high (3.3V) or active low interrupt pin. When set to active low, xALERT goes low if there is a pending interrupt. When set to active high, this pin goes high if there is a pending interrupt.

Protections and other events trigger this pin, but certain bits must be enabled to ensure that only the relevant sources generate an interrupt.

Protections, Interrupts, and Faults

Hardware protections can trigger both interrupt and faults independently (see Figure 9).

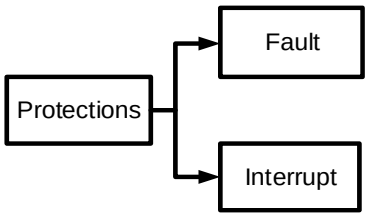

Figure 9: General Faults and Interrupts Architecture

Current Protections

Over-Current Protection (OCP)

All over-current protection (OCP) monitoring is performed with the same over-current (OC) analog comparator. Two possible range (RNG) levels are available for each threshold.

The threshold limit and deglitch are available with the multiple-time programmable (MTP) memory so that the value can be customized during battery pack assembly for different projects. OC1_DCHG_EN_CTRL, OC2_DCHG_EN_CTRL, and OC_CHG_EN_CTRL are the enable bits for discharge OC 1, discharge OC 2, and charge OC monitoring.

Once enabled, the monitoring function starts during the transition from safe mode to active mode, and keeps running in active mode. Use SAFE_SCOC_EN to enable monitoring in safe mode.

The enable bits for OC monitoring can be permanently locked in read-only mode, preventing the MCU from performing further changes. Once OC monitoring is enabled, the interrupt and fault polices can be set.

When only the CHG or DSG MOSFET turns on, the OC limits are set to whichever value is smaller between the configured value and 17.5mV. Meanwhile, the deglitch filter is the smaller value between the configured value and 16ms.

Discharge Over-Current Protection (OCP)

Two different, independent thresholds are available for discharge OCP: OC1 and OC2.

Table 4 on page 25 lists the resolution and ranges for discharge OC1 and OC2.

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Table 4: Discharge OC1 and OC2

Threshold	RNG = 0	RNG = 1 (3x)
LSB (mV)	2.5	7.5
FSR (mV)	80	240

Each limit has its own configurable deglitch time (OC1_DSG_DGL and OC2_DSG_DGL) with two configurable ranges (see Table 5). In standby mode, the discharge OC thresholds are set to 2.5mV, and the deglitch filter is the shorter value between the configured value and 1ms.

Table 5: OC1 and OC2 Deglitch Times

Deglitch Range	OCx_DSG_ DGL_RNG = 0	OCx_DSG_ DGL_RNG = 1
LSB (ms)	5	40
FSR (ms)	315	2520

Charge Over-Current Protection (OCP)

Table 6 lists the resolution and range for charge OCP.

Table 6: Charge OCP

Threshold	RNG = 0	RNG = 1 (3x)
LSB (mV)	1.6	4.8
FSR (mV)	51.2	153.6

The charge OC limit has its own configurable deglitch time with two configurable ranges (see Table 7).

Table 7: Charge OC Deglitch Time

Deglitch Range	OC_CHG_ DGL_RNG = 0	OC_CHG_ DGL_RNG = 1
LSB (ms)	5	40
FSR (ms)	315	2520

Short-Circuit Protections (SCP)

All short-circuit protection (SCP) monitoring is performed on a single short-circuit analog comparator. Each limit has a configurable deglitch time in the range of 100µs to 25.5ms.

SC_DCHG_EN_CTRL and SC_CHG_EN_CTRL are the enable bits for discharge short-circuit and charge short-circuit monitoring, respectively. Once monitoring is enabled and the MP2796 goes from safe mode to active mode, the IC begins monitoring.

The SAFE_SCOC_EN register can enable monitoring in safe mode.

Once short-circuit current monitoring is enabled, the interrupt and fault polices can be set.

Discharge Short-Circuit

Table 8 shows the resolution and range for the discharge short-circuit current limit.

Table 8: Discharge Short-Circuit Current Limit

	Limit		Deglitch Range
	RNG = 0	RNG = 1	
LSB	5.5mV	16.5mV	200µs
FSR	176mV	528mV	25.4ms

Charge Short-Circuit

Table 9 shows the resolution and range for the charge short-circuit current limit.

Table 9: Charge Short-Circuit Current Limit

	Limit		Deglitch Range
	RNG = 0	RNG = 1	
LSB	2.5mV	7.5mV	200µs
FSR	80mV	240mV	25.4ms

Voltage Protections

When enabled, all voltage protections are automatically monitored without needing an MCU to schedule ADC conversion.

An autonomous hardware state machine periodically schedules the conversion for all relevant channels, and the results are internally checked and compared to the limits.

The deglitch filters described refers to the number of consecutive readings during which the relevant channel exceeds its thresholds. The interval between readings is typically 254ms, though this value depends on the device's state (e.g. active mode or standby mode) and the configuration of the hardware monitoring (e.g. the ACTIVE_MONITOR_CFG register for active mode and STBY_MONITOR_CFG for standby mode).

Cell Under-Voltage (UV) and Over-Voltage (OV) Thresholds

When fewer than 16 cells are used, only the cells enabled by the CELL_S_CTRL register monitored for under-voltage (UV) and over-voltage (OV) conditions.

These thresholds are available in the MTP, which means they can be customized during battery pack assembly for different projects. Table 10 on page 26 lists the values for cell OV and UV thresholds.

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Table 10: Cell OV and UV Thresholds

Cell OV/UV	Limit	Hysteresis	Deglitch
LSB	19.5mV	19.5mV	1 reading
FSR	4.98V	292.5mV	16

Pack Under-Voltage (UV) and Over-Voltage (OV) Thresholds

The pack OV and UV thresholds are monitored by the VTOP pin. These thresholds are available in the MTP, which means they can be customized during battery pack assembly for different projects (see Table 11).

Table 11: Pack OV and UV Thresholds

Pack OV/UV	Limit	Hysteresis	Deglitch
LSB	19.5mV	78mV	1 reading
FSR	80V	4.922V	16

Negative Temperature Coefficient (NTC) Temperature

The negative temperature coefficient (NTC) voltages are checked during the automatic hardware monitoring sequence.

Figure 10 shows the block diagram of the NTC-sensing architecture.

All NTC channels are monitored in a ratiometric conversion. This means that the ADC reference is switched to NTCB for the NTC channels. In this scenario, all effects related to NTCB drifts due to the temperature and operating conditions are removed from the reading.

NTC1~4 have limits that can be set according to two modes:

- Cell monitor mode: The NTC monitors the temperature of the lithium cell in the pack. The MP2796 provides independent cell temperature limits (hot and cold) for the charging and discharging currents.

  These thresholds are available in the MTP, and can be customized during battery pack assembly for different projects.

- PCB monitor mode: The NTC monitors the PCB or the protection MOSFET's temperature. A standard hot temperature limit is provided for both the charge and discharge current.

Note that using NTCs results in a lower voltage threshold for OT (hot) conditions and a higher voltage threshold for under-temperature (cold) conditions.

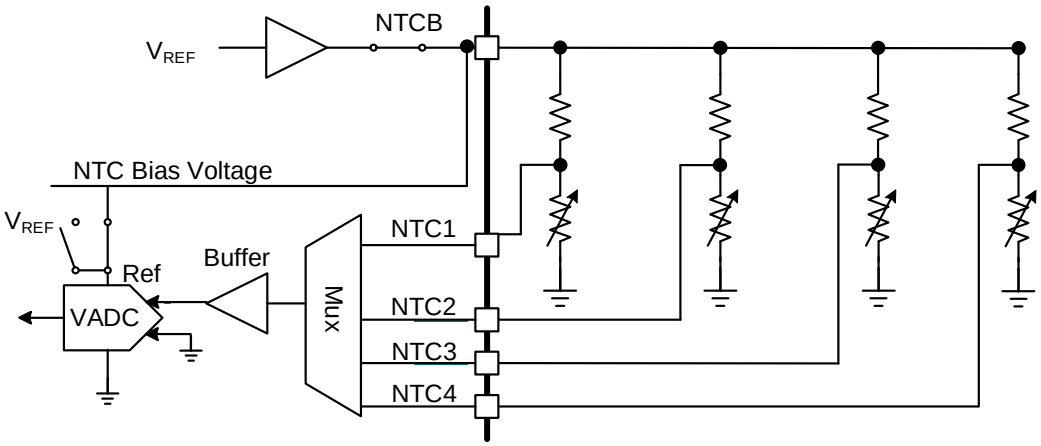

Figure 10: Architecture for NTC ADC Acquisition

Die Temperature

The die temperature alarm has two thresholds. The first is a digital threshold that can be configured between 70°C and 120°C. With this threshold, the comparator's output can put the IC in fault mode. The second is an analog threshold that forces the device to shut down at 140°C.

The digital die temperature threshold is typically used as an early warning, since the analog threshold forces the IC to shut down. Until the analog OT condition is resolved, the IC remains in a forced shutdown state, and the communication interface is unavailable.

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Dead Cells

The pack is monitored at a cell level for dead cells. A dead cell is defined as any cell whose voltage falls below the manufacturer's specified final discharge voltage, in which continued charging should be avoided. If dead cell detection is enabled, the MP2796 checks if any cell is below the configurable threshold (CELL_DEAD_LIMIT), which is typically much lower than the cell's UV threshold.

Once a dead cell condition is detected, the persistent dead cell flag (CELL_DEAD_LOG_STS) is set to 1. When the default values for CELL_DEAD_EN and CELL_DEAD_FAULT_EN are enabled via the OTP, this flag remains at 1 even if the device enters and exits shutdown mode. This flag can be cleared by the CELL_DEAD_DET_CLEAR command.

Mismatched Cells

Excessively mismatched or unbalanced cells can be detected by monitoring the maximum and minimum cell voltages.

If the difference between the maximum cell voltage and the minimum cell voltage exceeds a defined threshold, then a cell mismatch status is triggered. The mismatched cell with the higher voltage is reported as an individual flag. The cell with the minimum voltage is reported in the CELL_MSMT_LOWER register.

Diagnostics and Integrity

LDO (REGIN, 3.3V and 1.8V) Rail Monitoring

The LDO UV threshold is provided for the REGIN, 3.3V, and 1.8V rails. This UV threshold is compared to the ADC readings with the same refresh interval as the other voltage monitors, so it measures the nominal rail voltage rather than detecting deglitches.

ADC Self-Test Conversion

The ADC converts a known voltage value and ensures that the conversion result is within a predefined window that accounts for tolerance and temperature shifts.

One-Time Programmable (OTP) Cyclic Redundancy Check (CRC)

A one-time programmable (OTP) cyclic redundancy check (CRC) is executed when the device exits shutdown mode. If the CRC fails, the device can be configured to enter fault mode, preventing the BMS from turning on the protection MOSFETs.

Communication CRC

Typically, the CRC detects errors in exchanged data. The MP2796 supports CRC for exchanged data. When this functionality is enabled, the following is possible:

- Write a transaction to 1 register (2 bytes) to append a 1-byte CRC. A correct CRC is required for a successful write transaction.
- Read a transaction for 1 register (2 bytes) to append a 1-byte CRC.
- The read transaction length can be temporarily increased to 126 bytes using a dedicated register. The CRC is appended at the end of the transaction.

The communication CRC is implemented by the CRC-8 algorithm. The CRC can detect 1 incorrect bit. However, all CRC techniques encounter limitations when there are more incorrect bits.

If more than 1 bit is corrupted, the error detection depends on the specific pattern. Statistically, the detection can occur, but it is not guaranteed. In general, the ability to detect errors decreases when there is more data to check. For more details, see the I^{2}C Read section and SPI Read section on page 36 to page 41.

Watchdog Timer

The watchdog timer monitors communication with the I^{2}C or SPI interface. If there is no write to the WDT_RST register within a certain interval, the timer is triggered. The watchdog has a bark-bite style.

The bark notifies the device when the MCU has failed to clear the watchdog timer. This results in a bark timeout, which can be configured to trigger the alert pin. The WDT bark counter setting is 25ms per LSB, with up to 3.2 seconds maximum.

After a bite timeout, there is an optional feature to reset the device's registers to the default values. The WDT bite counter setting is 25ms per LSB, with up to 3.2 seconds maximum.

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Using the bidirectional, configurable WDT, it is possible to set up the IC to self-reset and/or to reset an external IC if its reset trigger is connected to the WDT pin.

Interrupts

Interrupt statuses are split between 2 register addresses (RD_INT0 and RD_INT1). Each interrupt source has a matching enable bit and a dedicated clear bit to clear the interrupt. Table 12 shows the main interrupts. Table 13 on page 29 shows additional interrupts.

Table 12: Main Interrupts (RD_INT0)

Condition	Flag	Description	Related Status Register(s)
Cell OV	CELL_OV_INT_STS	Unified flag for cell OV conditions. The related register reports each cell's OV flag, which is checked to determine which cell is generating the interrupt.	Flags in address, RD_CELL_OV
Cell UV	CELL_UV_INT_STS	Unified flag for cell UV conditions. The related register reports each cell's UV flag, which is checked to determine which cell is generating the interrupt.	Flags in address, RD_CELL_UV
VTOP pack OV	VTOP_OV_INT_ STS	Dedicated flag for battery pack OV conditions detected on the VTOP pin.	
VTOP pack UV	VTOP_UV_INT_STS	Dedicated flag for battery pack UV conditions detected on the VTOP pin. This is unrelated to the VTOP UV analog threshold.	
OC	OVER_CURR_ INT_STS	OC interrupt for charge, discharge 1, and discharge 2.	OC1_DCHG_STS, OC2_DCHG_STS, OC_CHG_STS
SCP	SHORT_CURR_ INT_STS	Short-circuit interrupt for both charge and discharge.	SC_CHG_STS, SC_DCHG_STS
NTC cold	NTC_COLD_ INT_STS	Unified flag for NTC cold conditions for all NTC channels configured in cell mode. To identify which NTC is the source of the interrupt, the additional individual flags should be checked.	NTC1_CELL_COLD_STS, NTC2_CELL_COLD_STS, NTC3_CELL_COLD_STS, NTC4_CELL_COLD_STS
NTC hot	NTC_HOT_INT_ STS	Unified flag for NTC hot conditions for all NTC channels configured in cell mode. To identify which NTC is the source of the interrupt, the additional individual flags should be checked.	NTC1_CELL_HOT_STS, NTC2_CELL_HOT_STS, NTC3_CELL_HOT_STS, NTC4_CELL_HOT_STS
Watchdog interrupt	WDT_INT_STS	Notification for either a bite or bark event from the communication watchdog timer.	WDT_BARKED, WDT_BITE
Fault recovered	RECOVERED_ INT_STS	Notification that the system recovers from a fault state, including both automatic fault recovery and a manual MCU clearing.	
AFE mode change	AFE_MODE_ CHANGE_INT_STS	The AFE has changed states (e.g. safe mode, active mode, fault mode, standby mode).	PWR_STATE
Scan complete	VSCAN_DONE_ INT_STS	Notification that the high-resolution voltage ADC scan has finished converting of all the channels on its list.	
Pack current	PACK_CURRENT_ INT_STS	Interrupt indicating a change in the battery pack current range (discharge, standby, or charge).	PACK_CURRENT_STATUS

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Table 13: Additional Interrupts (RD_INT1)

Name	Flag	Description	Related Status Register(s)
FET driver	FET_DRIVER_INT_STS	Reports a MOSFET driver issue such as the following: • FET timeout: the DSG or CHG driver did not reach its final voltage within the timeout interval • A lower level OC condition occurs during CHG or DSG soft start • A short-circuit is issued before DSG turns on	FET_TIMEOUT
PACKP voltage	PACKP_V_INT_STS	The voltage on PACKP node has changed compared to VTOP. Note that the PACKP comparator is invalid when disabled or during short-circuit removal, but still reports to the interrupt.	PACKP_COMP_STS
Balancing complete	BAL_DONE_INT_STS	Balancing has been completed.	Flags in address, BAL_STS
Self-test fail	SELF_TEST_INT_STS	The ADC is failing its self-diagnostic test and/or the conversion of this value is outside the specified boundaries.	SELF_TEST_STS_OV, SELF_TEST_STS_UV
Scheduler error	FSM_ERROR_INT_STS	The scheduler was busy when a new feature command was requested, and concurrent operation is not supported. For example, the device may report that an MCU conversion command is ignored since open-wire detection is running, or it may report that a cell-balancing command is ignored since open-wire detection is running.	
PCB temperature hot	PCB_MNTR_HOT_ INT_STS	Unified flag for NTC hot conditions for all NTC channels configured in PCB mode. To identify which NTC is the source of the interrupt, the individual flags should be checked.	NTC1_PCB_MNTR_HOT_STS, NTC2_PCB_MNTR_HOT_STS, NTC3_PCB_MNTR_HOT_STS, NTC4_PCB_MNTR_HOT_STS
Die temperature	DIE_TEMP_INT_STS	The die temperature is too high, reported by the digital die temperature check.	
Mismatched cells	CELL_MISMATCH_ INT_STS	The voltage difference between cells is too great.	Flags in address, RD_CELL_MSMT
Dead cell	CELL_DEAD_INT_STS	The dead cell threshold has been reached.	Flags in address, RD_CELL_DEAD
Open wire	OPEN_WIRE_INT_STS	Open-wire detection is complete. The open-wire interrupt status register must be checked to identify if there are any disconnected wires.	Flags in address, RD_OPENH, RD_OPENL
VDD	VDD_INT_STS	The VDD rail is below the defined UV threshold.	
3V3	3V3_INT_STS	The 3.3V rail is below the defined UV threshold.	
REGIN	REGIN_INT_STS	The REGIN rail is below the defined UV threshold.	
OTP CRC	OTP_CRC_EVENT_ INT_STS	The CRC stored in the OTP does not match the computed CRC value from OTP memory readback. The manual CRC check is completed.	

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The interrupt source can be configured using a TYPE selector. Depending on the interrupt, the TYPE selector provides a few options:

- Level (high)
- Rising edge
- Falling edge
- Rising and falling edge

Each interrupt that is related to a protection flag follows the processes described above.

Fault

In fault mode, both discharge (DSG N-channel MOSFETs and standby P-channel MOSFET) and charge (CHG N-channel MOSFETs) are turned off. Faults can be cleared either by an automatic recovery or manual MCU clearing. The fault enable control bit for each fault has a configurable default value, and the option to permanently lock the register in read-only mode. Table 14 lists certain faults and their recovery methods. Table 15 on page 31 lists additional faults and their recovery methods.

Table 14: Fault and Recovery Management (Part I)

Fault	Enable Control	Can Be Read-Only?	Recovery Method(s)
Cell OV	CELL_OV_ FAULT_EN	Yes	Configurable for manual or automatic recovery. • Manual recovery: The host MCU writes to the fault clear command (CELL_OV_FAULT_CLR) • Automatic recovery: This method is enabled with CELL_OV_REC. An additional recovery logic option is available via CELL_OV_LOGIC_SEL
Cell UV	CELL_UV_ FAULT_EN	Yes	Configurable for manual or automatic recovery. Note that if the battery pack's current status is charging, then the cell UV fault is blocked, but the status is still reported when V_{CELL} < (cell UV threshold). • Manual recovery: The host MCU writes to the fault clear command (CELL_UV_FAULT_CLR) • Automatic recovery: This method is enabled with CELL_UV_REC. An additional recovery logic option is available via CELL_UV_LOGIC_SEL
Dead cell	CELL_DEAD_ FAULT_EN	Yes	The host MCU writes to the fault clear command (CELL_DEAD_FAULT_CLR). CELL_DEAD_LOG_STS prevents the IC from entering active mode, which can only be cleared by CELL_DEAD_DET_CLEAR.
Cell mismatch	CELL_MSMT_ FAULT_EN	Yes	The host MCU writes to CELL_MSMT_FAULT_CLR.
Open wire	OPEN_WIRE_ FAULT_EN	Yes	The host MCU writes to OPEN_WIRE_FAULT_CLR.
VTOP OV	VTOP_OV_ FAULT_EN_ CTRL	Yes	The host MCU writes to VTOP_OV_FAULT_CLR.
VTOP UV	VTOP_UV_ FAULT_EN_ CTRL	Yes	The host MCU writes to VTOP_UV_FAULT_CLR.
Cell NTC too hot (discharge)	NTC_CELL_ HOT_FAULT_ EN	Yes	Configurable for manual or automatic recovery. • Manual recovery: The MCU writes to the clear bit (NTC_CELL_HOT_FAULT_CLR) • Automatic mode: The device recovers when the NTC voltage (V_{NTC}) exceeds (hot discharge threshold + hysteresis)). This method is enabled with NTC_CELL_DCHG_REC
Cell NTC too cold (discharge)	NTC_CELL_ COLD_FAULT_ EN	Yes	Configurable for manual or automatic recovery. • Manual recovery: The MCU writes to the clear bit (NTC_CELL_COLD_FAULT_CLR) • Automatic mode: The device recovers when V_{NTC} falls below (cold discharge threshold - hysteresis). This method is enabled with NTC_CELL_DCHG_REC

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Cell NTC too hot (charge)	NTC_CELL_ HOT_FAULT_ EN	Yes	Configurable for manual or automatic recovery. • Manual recovery: The MCU writes to the clear bit (NTC_CELL_HOT_FAULT_CLR) • Automatic recovery: The device recovers when V_{NTC} exceeds (hot charge threshold + hysteresis). This method is enabled with NTC_CELL_CHG_REC. An additional recovery logic option is available via NTC_CHG_REC_MODE
Cell NTC too cold (charge)	NTC_CELL_ COLD_FAULT_ EN	Yes	Configurable for manual or automatic recovery. • Manual recovery: The MCU writes to the clear bit (NTC_CELL_COLD_FAULT_CLR) • Automatic recovery: The device recovers when V_{NTC} falls below (cold charge threshold - hysteresis). This method is enabled via NTC_CELL_CHG_REC. An additional recovery logic option is available via NTC_CHG_REC_MODE

Table 15: Fault and Recovery Management (Part II)

Fault	Enable Control	Can be Read-Only?	Recovery Method(s)
Pack OC discharge 1	OC1_DCHG_ FAULT_EN	Yes	Configurable for manual or automatic recovery. This can only be manually cleared when OC_DCHG_RECOVERY_FAILED has issued a report. • Manual recovery: The host MCU writes to the fault clear command (OC1_DCHG_FAULT_CLR) • Automatic recovery: Enabled with OC1_DCHG_REC. This device tries to turn on the MOSFETs to check if the condition is removed. If removed, the device auto-clears the fault status and goes back to safe mode. If the condition is not removed within the time set by OC1_DCHG_RETRY, then the device reports to OC_DCHG_RECOVERY_FAILED. Once the pack drops below 110mV, the device reports to OC_DCHG_RECOVERY_FAILED directly.
Pack OC discharge 2	OC2_DCHG_ FAULT_EN	Yes	Configurable for manual or automatic recovery. This can only be manually cleared when OC_DCHG_RECOVERY_FAILED has issued a report. • Manual recovery: The host MCU writes to the fault clear command (OC2_DCHG_FAULT_CLR) • Automatic recovery: Enabled with OC2_DCHG_REC. This device tries to turn on the MOSFETs to check if the condition is removed. If removed, the device auto-clears the fault status and goes back to safe mode. If the condition is not removed within the time set by OC2_DCHG_RETRY, then the device reports to OC_DCHG_RECOVERY_FAILED. Once the pack drops below 110mV, the device reports to OC_DCHG_RECOVERY_FAILED directly.
Pack OC charge	OC_CHG_ FAULT_EN	Yes	Configurable for manual or automatic recovery. This can only be manually cleared when OC_CHG_RECOVERY_FAILED has issued a report. • Manual recovery: The host MCU writes to the fault clear command (OC_CHG_FAULT_CLR) • Automatic recovery: Enabled with OC_CHG_REC. This device tries to turn on the MOSFETs to check if the condition is removed. If removed, the device auto-clears the fault status and goes back to safe mode. If the condition is not removed within the time set by OC_CHG_RETRY, then the device reports to OC_CHG_RECOVERY_FAILED.

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Pack short-circuit current discharge	SC_DCHG_ FAULT_EN	Yes	Configurable for manual or automatic recovery. This can only be manually cleared when SC_DCHG_RECOVERY_FAILED has issued a report. • Manual recovery: The host MCU writes to the fault clear command (SC_DCHG_FAULT_CLR) • Automatic recovery: Enabled with SC_DCHG_REC. The device monitors the PACKP voltage to see if it rises to 110mV. If this condition is not removed by SC_PUP_RETRY_N, then the device reports to SC_DCHG_RECOVERY_FAILED.
Pack short-circuit current charge	SC_CHG_ FAULT_EN	Yes	Configurable for manual or automatic recovery. This can only be manually cleared when SC_CHG_RECOVERY_FAILED has issued a report. • Manual recovery: The host MCU writes to the fault clear command (SC_CHG_FAULT_CLR) • Automatic recovery: Enabled with SC_CHG_REC. The device monitors the PACKP voltage to see if it falls below (V_{TOP} + 270mV). If this condition is not removed within the time set by SC_PUP_RETRY_N, then the device reports to SC_CHG_RECOVERY_FAILED.
3.3V or VDD UV	3V3_VDD_ FAULT_EN	Yes	Manual recovery only. The host MCU writes to the fault clear command (3V3_VDD_FAULT_CLR).
PCB monitor too hot	PCB_MNTR_ FAULT_EN	Yes	Configurable for manual or automatic recovery. • Manual recovery: The host MCU writes to the fault clear command (PCB_MNTR _FAULT_CLR) • Automatic recovery: The device recovers when the NTC voltage exceeds (monitor hot threshold + hysteresis). This method is enabled with PCB_MNTR_REC.
Die too hot digital	DIE_TEMP_ DIG_FAULT_ EN	Yes	Configurable for manual or automatic recovery. • Manual recovery: The host MCU writes to the fault clear command (DIE_TEMP_FAULT_CLR) • Automatic recovery: The device waits for the die temperature to drop below (digital temperature threshold - hysteresis). This method is enabled with DIE_TEMP_FAULT_REC.
Die too hot analog	N/A; hardcoded enable	N/A	The IC returns to safe mode from shutdown mode once the die temperature drops below (analog temperature threshold - hysteresis).
Driver turn on fail	N/A; hardcoded enable	N/A	Manual recovery only. The host MCU writes to the fault clear command (DRIVER_FAULT_CLR).

Regulators and Power Domains

There are three main power rails:

- REGIN (5V): supplies power to the AFE analog circuitry
- 3V3 (3.3V): powers an external MCU
- VDD (1.8V): internal use only; powers the digital domain

The 3.3V rail can be configured to be on or off in shutdown mode.

Open-Wire Detection

The open wire state machine automatically controls the pull-up and pull-down currents sources during open-wire detection, and detects the voltage changes on each cell. The cells that are detected can be set by the CELLS_CTRL register.

The open-wire detection current uses a pair of 100µA pull-up/-down currents. The interval can be configured to be between 1ms and 16ms, with a 1ms resolution. The default is 8ms.

The threshold that determines how much change can be accepted for an open circuit is a configurable voltage threshold ranging between 39.06mV and 625mV, with 39.06mV steps. The default is 195mV. The host MCU can trigger open-wire detection with a dedicated command register. If multiple open wires are present simultaneously, then the detection logic reports at least one open wire, which tells the device to avoid using the overall battery pack (see Figure 11 on page 33).

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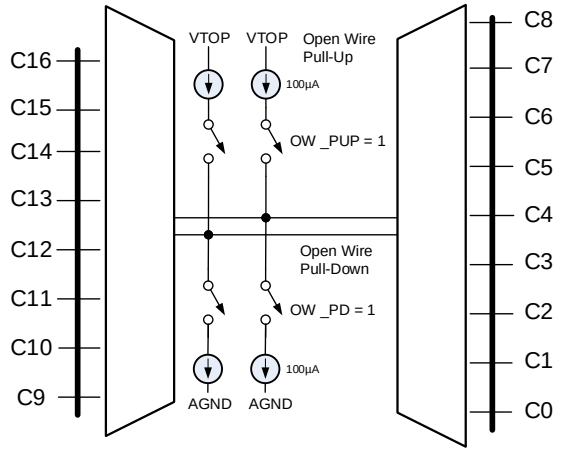

Figure 11: Open-Wire Detection Architecture

Cell-Balancing

The battery reaches its end of life (EOL) when the capacity of the weakest cell is too low to be usable. Unbalanced cells yield the same effect, with one cell at a higher SOC, and another at a lower SOC. To reduce the effects of the issue, it is critical to balance lithium cells.

Unbalanced cells can be caused by cell temperature differences, different self-discharge rates, and general production tolerances that affect cell chemistry and alter aging rates among strings of parallel cells.

Cell-balancing can extend the usable life of the battery pack by keeping the voltage of each cell within the defined safe operating area (SOA).

Internal MOSFET Balancing

The MP2796 supports direct cell balancing, without the use of external MOSFETs or BJTs, for currents up to about 58mA (with a 4V cell voltage). The balance current for each cell is dictated by the combined filter resistor and the on resistance of the internal balancing MOSFET ($R_{(DS)ON}$). The MP2796 can simultaneously balance only even or odd cells. Internal logic handles the sequencing between even and odd cells.

External Balancing

A balancing current exceeding 58mA can be achieved by adding external balancing MOSFETs or BJTs. This balancing current is limited by board thermals and the wiring resistance. For external MOSFETs, it is also limited by the MOSFETs' $R_{(DS)ON}$ at the appropriate gate voltage (V_{GS}). For external BJTs, it may be limited by the h_{FE}. For external MOSFETs, a minimum gate threshold voltage of 1.8V is required (assuming a 4.2V lithium cell) to turn on the balancing MOSFETs.

Manual Cell-Balancing

The cells that need to be balanced are manually marked by writing to the appropriate register (BAL_LIST).

The balancing time for marked cells can be configured via BAL_REPETITION, with 0 to 31 repetitions. When BAL_REPETITION is set to 0, there is only one 30ms execution.

The host MCU should periodically read the AFE die temperature to ensure it is within the operating range, as an excessive temperature can lead to over-temperature (OT) shutdown.

Automatic Cell-Balancing

Automatic cell-balancing offers the following configurations:

1. Enable automatic cell balancing by setting the register BALANCE_MODE_REG = 1.
2. Configure the method for initiating automatic cell-balancing via the register BALANCE_MODE_CTRL. The MP2796 can be configured to use register control (BALANCE_GO) or GPIO3 control to initiate automatic cell-balancing.
3. Disable constant automatic balancing by setting register AUTO_BAL_ALWAYS = 0. The register BAL_REPETITION sets the number of cell-balancing iterations. The cell-balancing repetition number is ignored if AUTO_BAL_ALWAYS = 1, and the device constantly balances the cells until the AUTO_BAL_ALWAYS is set to 0, or until the balancing list is empty.
4. Set the balancing threshold via the register BAL_MSM_TH. This is the minimum voltage difference between the current cell voltage and the lowest cell voltage to be eligible for cell balancing. This value ranges between 19.5mV and 87.855mV, with 9.765mV steps.
5. Set the minimum balancing voltage via the register CELL_BAL_MIN. This is the minimum cell voltage for a cell to be eligible for balancing. This value ranges from 2500mV to 4961mV with 39mV steps.

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6. Set ABAL_ON_CHARGE = 1 to enable automatic cell-balancing when the state of the current is in charge mode. Set ABAL_ON_STBY = 1 to enable automatic cell-balancing when the state of the current is in standby mode.

If the state of the current is in discharge mode, the automatic cell-balancing will be skipped.

The die temperature threshold can be used to prevent or suspend balancing. The MP2796 can be configured to suspend constant automatic cell-balancing (AUTO_BAL_ALWAYS = 1), when the die temperature threshold has been exceeded (see STOP_ON_HOT). Once the OT condition is removed, the constant automatic cell-balancing will resume

Figure 12 shows the cell-balancing list update for automatic cell-balancing. Figure 13 shows the cell-balancing sequence for the cell-balancing list.

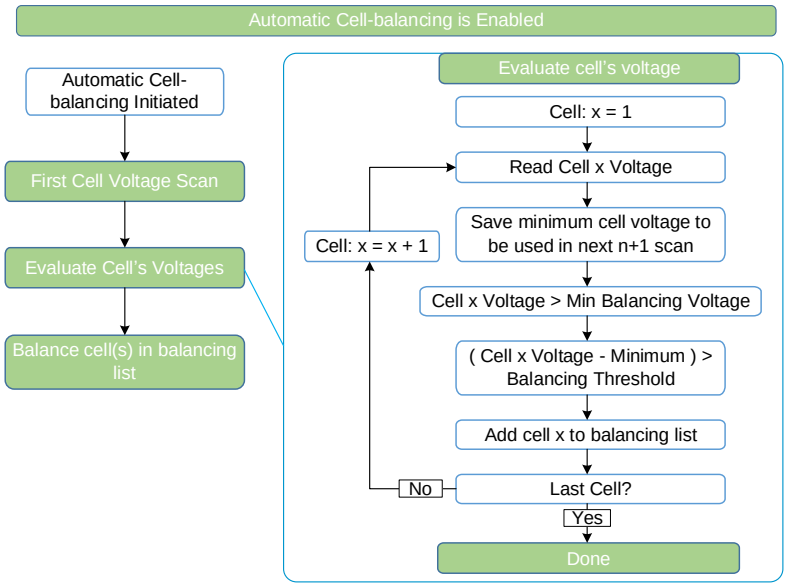

Figure 12: Automatic Cell-Balancing (Cell Voltage Evaluation)

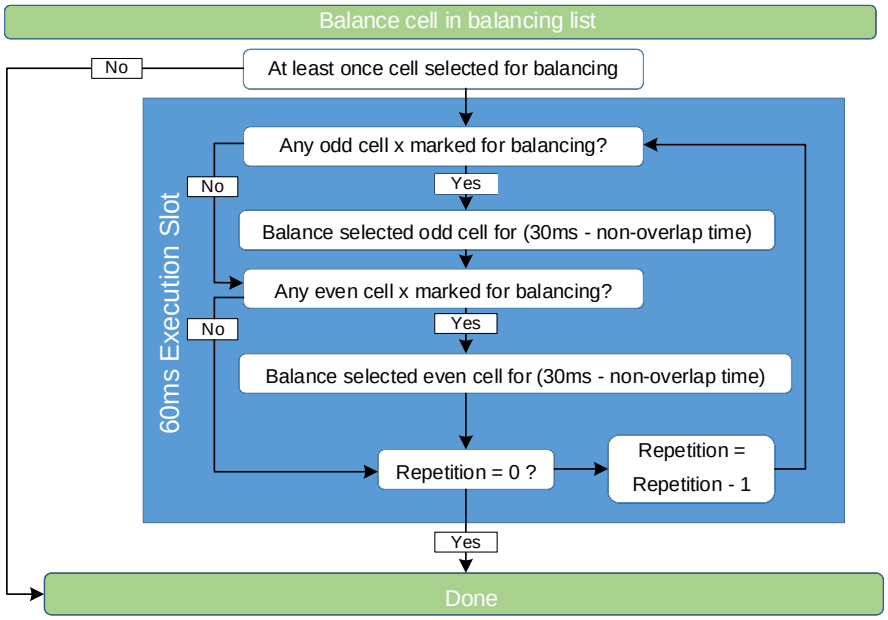

Figure 13: Executing Balancing for Cell in Balancing List

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Supported Concurrency

Table 16 shows which features can be enabled once a feature is active. When multiple features are enabled simultaneously, some remaining features can still be activated.

It is possible to use a high-resolution voltage scan during cell-balancing, but care should be taken, as voltage readings on the cell being balanced and adjacent cells are affected.

Table 16: Supported Concurrencies

Active Task	Triggered By	Concurrent Features
High-resolution voltage scan	ADC_SCAN_GO	Cell-balancing
Cell-balancing	BALANCE_GO	High-resolution voltage scan
Open wire	OPEN_WIRE_GO	N/A

The command sequence to the MP2796 should be controlled in the following manner:

- During high-resolution voltage scanning, wait to set ADC_SCAN_GO = 0 until SCAN_DONE_STS or SCAN_ERROR_STS updates to 1.
- During cell-balancing, wait to set BALANCE_GO = 0 until BAL_DONE_STS or BAL_ERROR_STS updates to 1. To stop automatic cell-balancing, set AUTO_BAL_ALWAYS = 0, wait until BAL_DONE_STS or BAL_ERROR_STS updates to 1, and then set BALANCE_GO = 0.
- When conducting open-wire checks, wait to set OPEN_WIRE_GO = 0 until OPEN_WIRE_DONE_STS or OPEN_WIRE_ERR_STS updates to 1.

For these command sequences, the status can be determined via polling or via interrupts (VSCAN_DONE_INT_STS, BAL_DONE_INT_STS, and OPEN_WIRE_INT_STS). See to the Interrupts section on page 28 for more details.

High-Resolution Voltage ADC Scan for the MCU

A voltage scan can convert the following classes of inputs:

- Die temperature voltage
- NTC1, NTC2, NTC3, and NTC4 voltages
- Cell voltages
- VTOP pin voltage
- PACKP pin voltage
- GPIO voltages (GPIO1, GPIO2, and GPIO3)
- Regulators (VDD [1.8V], 3V3, and REGIN)

If a class of inputs is not enabled, the scan skips to the next class. Control bits are provided to enable individual channels in each class. The device is notified when the scan is complete, and the results are available for readback.

High-Resolution Current Reading

The current is measured via an external current-sense resistor between SRP and SRN. It is synchronized with the VTOP channel conversion, which can be enabled using VTOP_SYNC_EN.

Non-Volatile Memory (NVM) Configuration

The default values of most registers can be configured through the non-volatile memory (NVM). Some registers are one-time programmable (OTP), while others are multiple-time programmable (MTP). The MTP registers can be programmed up to three times. These values can be locked, so that the same version of the IC can be adjusted for similar projects with minor differences.

To configure the MTP, apply 7.5V to the NSHDN pin and follow the steps below:

1. Ensure that the NSHDN pin is set to 7.5V.
2. Write the appropriate value to the register that allows MTP.
3. Write prior to the store command with the following command access code: 0xA5B6 (REG0xB9 = 0xA5B6).
4. Send the command to store the register's current value to the NVM by writing 1 to STORE_NVM_CMD (0xB8, bit[3]).
5. Wait for STORE_IN_PROGRESS to go back to 0.
6. Recover the NSHDN pin to 3.3V.

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I²C INTERFACE

The MP2796 can use an I²C interface to flexibly set parameters and report device statuses instantaneously. The I²C is a two-wire serial interface with two bus lines: a serial data line (SDA) and a serial clock line (SCL). Both SDA and SCL are open drains, and they must be connected to the positive supply voltage via a pull-up resistor.

The IC operates as a slave device that receives control inputs from the master device, such as a microcontroller (MCU). The SCL is always driven by the master device. The I²C interface supports both standard mode (up to 100kbit/s) and fast mode (up to 400kbit/s).

All transactions begin with a start (S) command and are terminated by a stop (P) command. Start and stop commands are always generated by the master. A start command is defined as a high-to-low transition on the SDA while the SCL is high. A stop command is defined as a low-to-high transition on the SDA while the SCL is high (see Figure 14).

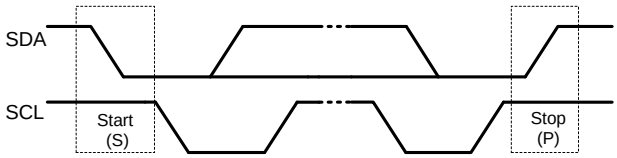

Figure 14: Start and Stop Commands

For data validity, the data on the SDA must be stable during the high period of the clock. The high or low state of the SDA can only change when the clock signal on the SCL is low (see Figure 15).

Every byte on the SDA must be 8 bits long. The number of bytes that can be transmitted per transfer is unrestricted. Data is transferred with the most significant bit (MSB) first.

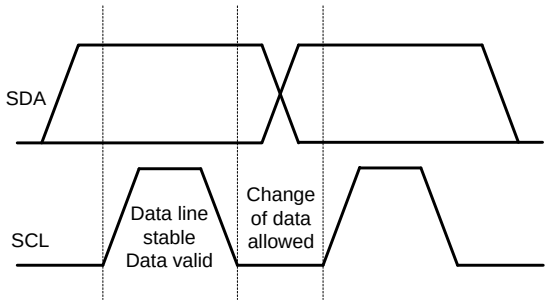

Figure 15: Bit Transfer on the I²C Bus

Each byte must be followed by an acknowledge (ACK) bit, which is generated by the receiver to signal to the transmitter that the byte was successfully received.

The ACK signal occurs when the transmitter releases the SDA line during the acknowledge clock pulse. This allows the receiver to pull the SDA line low. The SDA line stays low during the high period of the ninth clock.

If the SDA line is high during the 9th clock pulse, this is defined as a not acknowledge (NACK) signal. The master can then generate either a stop command to abort the transfer, or a repeated start (Sr) command to start a new transfer.

After the start command, a slave address is sent. This address is 7 bits long, followed by an 8th data direction bit (R/W). A 0 indicates a transmission (write), and a 1 indicates a request for data (read). Figure 16 shows the address bit arrangement.

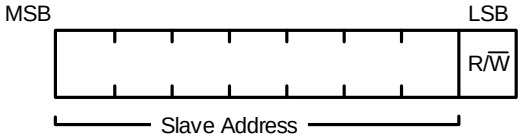

Figure 16: 7-Bit Address

Figure 17 shows a data transfer on the I²C bus.

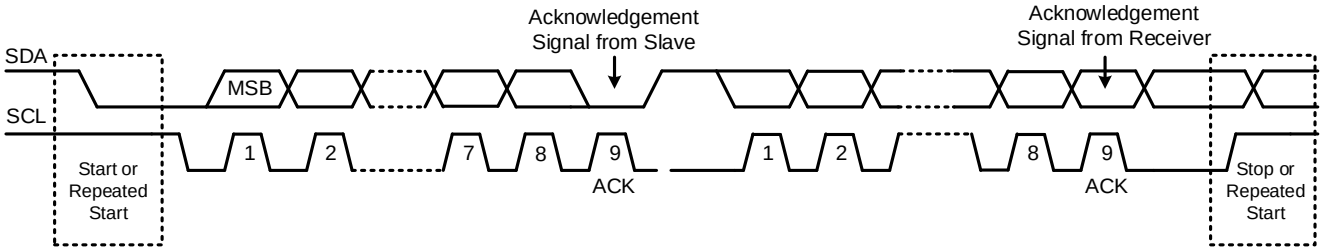

Figure 17: Data Transfer on the I²C Bus

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I²C Read

When CRC is enabled, the payload is limited to 2 bytes by default (see Figure 18 on page 38). This value can be increased to 63 words (126 bytes) using the XFR_NUM_RD_WORDS register. XFR_NUM_RD_WORDS retains the new value only for the next transaction, so ensure that the next transaction uses the increased payload count.

CRC in an I²C Read Transaction

After completing the request for a read transaction, the host MCU must ensure that the CRC matches the value provided in the read transaction to confirm that no bits were corrupted during the transmission.

The CRC-8 algorithm follows the polynomial ($1 + x^1 + x^2 + x^8$), and is applied byte-wise to the bytes, following the order in which the bytes are transmitted or received. If it were bit-wise, the MSB would be processed first in each byte. An example of this sequence is shown below:

1. Slave address byte + write (0x02)
2. Register address byte (0x00)
3. Slave address byte + read (0x03)
4. Register address byte (0x00)
5. Word 1 - byte 1 / bits[7:0] (0x7C)
6. Word 1 - byte 2 / bits[15:8] (0x00)

This sequence results in CRC = 0x36 being appended as the last CRC byte.

Although this byte of the fourth sequence does not exist in the actual read sequence, it must be added in the CRC calculation.

I²C Write

Figure 19 on page 38 shows how the byte is ordered in a write transaction. When CRC is enabled, the targeted register address is modified according to payload only if the CRC results match.

CRC in an I²C Write Transaction

The CRC-8 algorithm follows the polynomial ($1 + x^1 + x^2 + x^8$), and is applied byte-wise to the bytes following the order in which they are transmitted or received. If it were bit-wise, the MSB would first be processed in each byte. An example of this sequence is shown below:

1. Slave address byte + write (0x02)
2. Register address byte (0x00)
3. Word 1 - byte 1 / bits[7:0] (0x7C)
4. Word 1 - byte 2 / bits[15:8] (0x00)

This sequence results in CRC = 0x72, which the host MCU should append as the last CRC byte to ensure a successful transaction.

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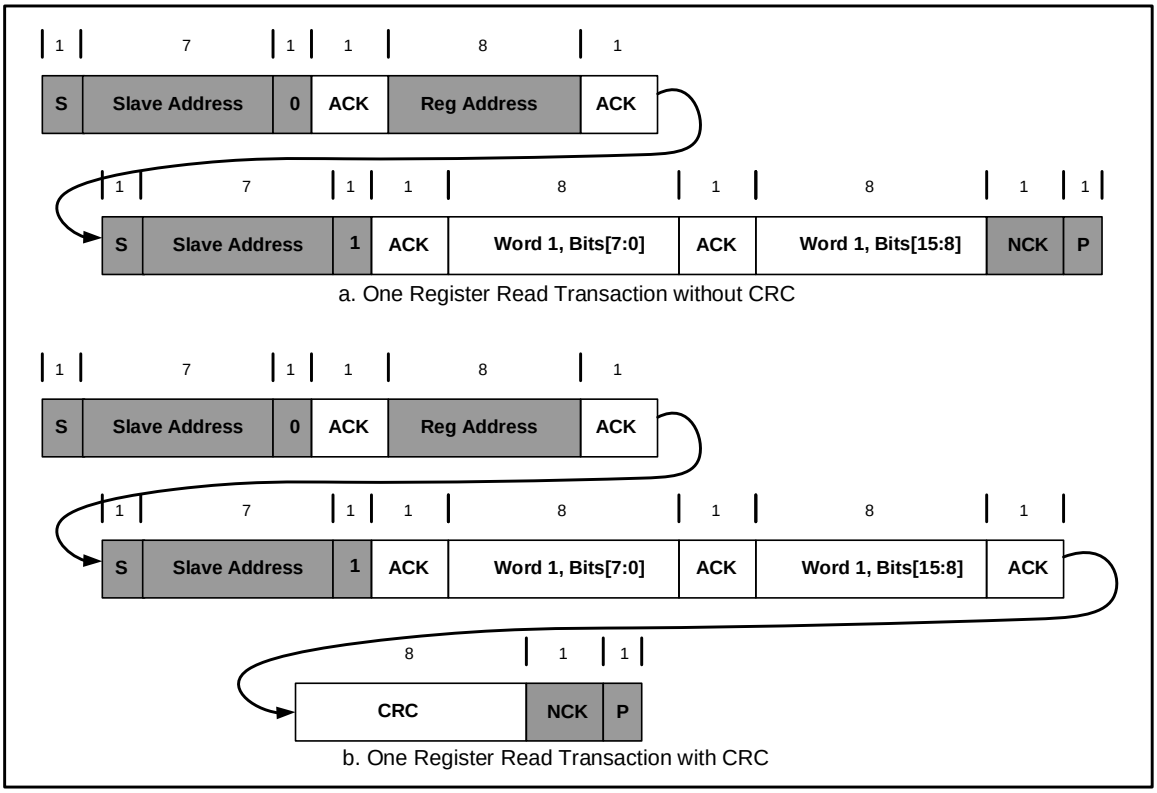

Figure 18: I²C Single Address Read

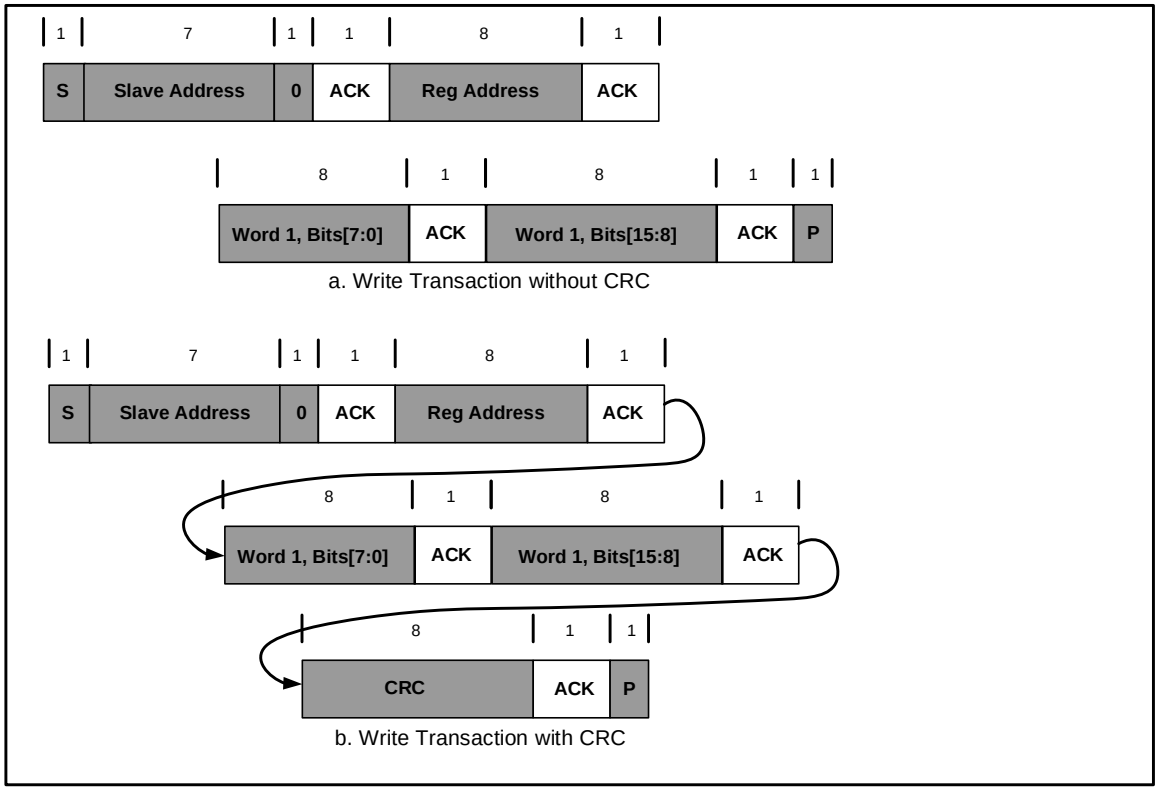

Figure 19: I²C Write Transaction

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Serial Peripheral Interface (SPI)

The MP2796 has an interface that is compatible with serial peripheral interfaces (SPIs). This interface is configured to operate using clock phase (CPHA) = 1 and clock polarity (CPOL) = 1. Consequently, data on SDI must be stable during SCK's rising edge. Words are transferred with most significant bit (MSB) first.

During a write transaction, the data value on SDI is latched to the device on SCK's rising edge. During a read transaction, the bit stream is presented on SDO with the MSB first, and is valid during SCK's rising edge, while the SDO transitions on SCK's falling edge.

nCS must remain low for the entire command sequence duration, including the time between the command byte and subsequent data. During a write command, data is latched on nCS's rising edge (see Figure 20 on page 40).

SPI Data Protocol

For a successful SPI transaction, nCS must go low and there must be a successful match between the transaction slave address and the internally configured slave address (located in register DEVICE_ADD). The MP2796's SPI requires a specific transaction structure.

SPI Read

Read transactions should have the fields arranged with a matching order for the slave address, read bit, register address, and data payload (see Figure 21 on page 40).

When CRC is enabled, the payload is limited to two bytes by default. This value can be increased to 63 words (126 bytes) using the XFR_NUM_RD_WORDS register. XFR_NUM_RD_WORDS retains the new value only for the next transaction, so ensure that the next transaction uses the increased payload count.

CRC in an SPI Read Transaction

After completing the request for a read transaction, the host MCU must ensure that the CRC matches the value provided in the read transaction to confirm that no bits were corrupted during the transmission.

The CRC-8 algorithm follows the polynomial ($1 + x^1 + x^2 + x^8$), and is applied byte-wise to the bytes, following the order in which bytes are transmitted or received. If it were bit-wise, the MSB would first be processed in each byte. An example of this sequence is shown below:

1. Slave address byte + read (0x03)
2. Register address byte (0x00)
3. Word 1 - byte 1 / bits[7:0] (0x7C)
4. Word 1 - byte 2 / bits[15:8] (0x00)

This sequence results in CRC = 0x64 being appended as the last CRC byte.

SPI Write

Write transactions should have the fields arranged with a slave address, write bit, register address, and data payload (see Figure 22 on page 41). When CRC is enabled, the SPI write payload is limited to 2 bytes and targeted register addresses are modified according to the payload only if the CRC matches.

CRC in an SPI Write Transaction

The CRC-8 algorithm follows the polynomial ($1 + x^1 + x^2 + x^8$), and is applied byte-wise to the bytes following the order in which they are transmitted or received. If it were bit-wise, the MSB would first be processed in each byte. An example of this sequence is shown below:

1. Slave address byte + write (0x02)
2. Register address byte (0x00)
3. Word 1 - byte 1 / bits[7:0] (0x7C)
4. Word 1 - byte 2 / bits[15:8] (0x00)

This sequence results in CRC = 0x72, which the host MCU should append as the last CRC byte to ensure a successful transaction.

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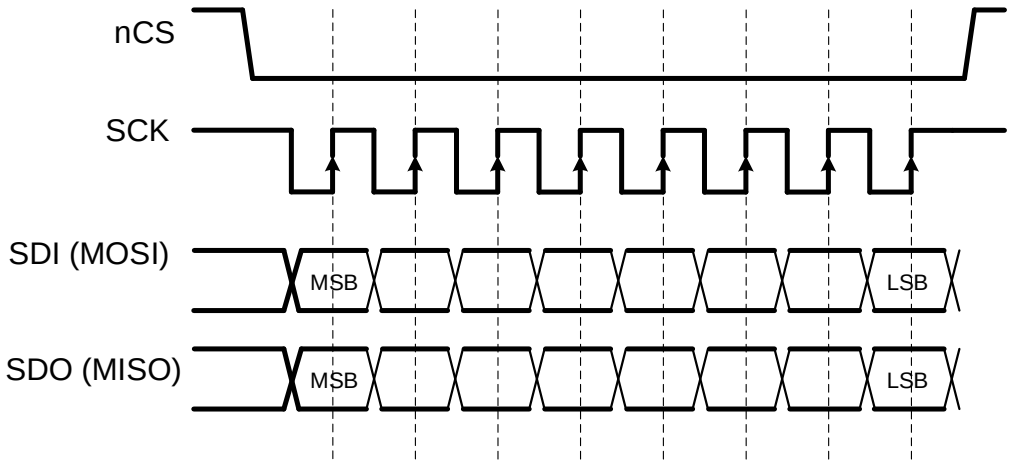
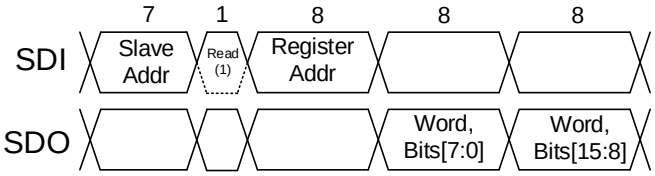
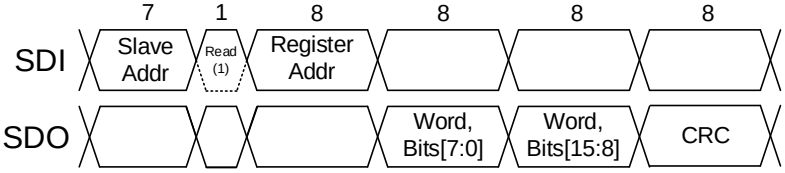


Figure 20: SPI Signal Sequencing

SPI Read without CRC: 1 Word (2 Bytes)



SPI Read with CRC: 1 Word (2 Bytes) Payload



SPI Read with CRC: 2 Words (4 Bytes) Payload

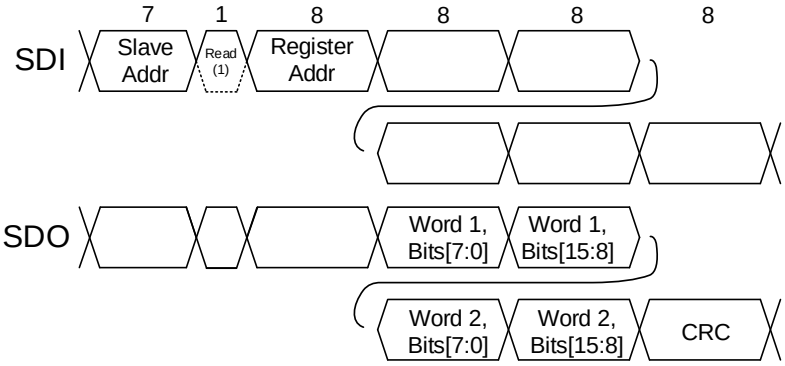


Figure 21: SPI Read Transaction

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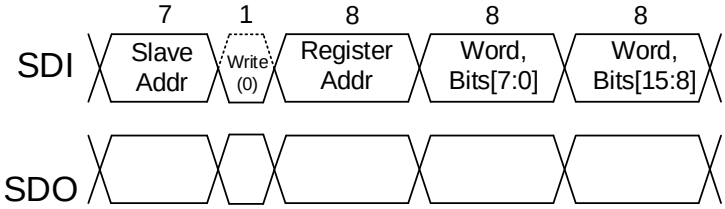
SPI Write without CRC: 1 Word (2 Bytes)



SPI Write with CRC: 1 Word (2 Bytes)

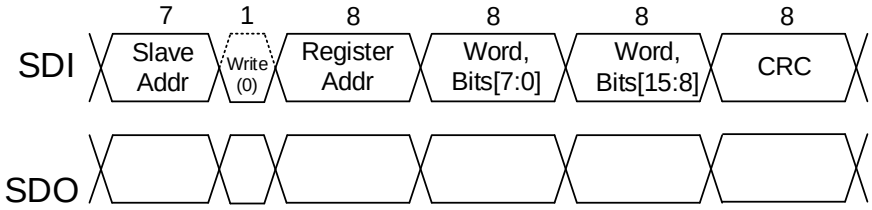


Figure 22: SPI Write Transaction

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REGISTER MAP

The default slave address is 01h. The address can be configured by modifying DEVICE_ADD (register 0xA3, bits[14:8]). Once the value has been changed, the next communication should use the new address. Note that the default address may be different for the chips with different “xxxx” suffixes.

All the bits in an address that are not populated by a register should be treated as reserved bits. Their values should not be modified during write operations that are meant to change bits in the same address.

This register map is organized by functions, which means registers that are located at the same address may be in different sections. However, the role of each bit in a given address can be used to learn more about other registers that are located in the same address.

Cell Configuration

Address Name and Location	Field Bit Position and Name	Description	Type	Reset Value (OTP/MTP)	Encoding, LSB, and Range
CELLS_CTRL: 0x00	Bits[3:0]: CELL_S_CTRL	Sets the number of stacked cells in use. 0x0: Cells 7~1 enabled 0x1: Cells 7~1 enabled 0x2: Cells 7~1 enabled 0x3: Cells 7~1 enabled 0x4: Cells 7~1 enabled 0x5: Cells 7~1 enabled 0x6: Cells 7~1 enabled 0x7: Cells 8~1 enabled 0x8: Cells 9~1 enabled 0x9: Cells 10~1 enabled 0xA: Cells 11~1 enabled 0xB: Cells 12~1 enabled 0xC: Cells 13~1 enabled 0xD: Cells 14~1 enabled 0xE: Cells 15~1 enabled 0xF: Cells 16~1 enabled	R/W (can lock to read-only)	0xF (MTP)	N/A

IC State Control

Address Name and Location	Field Bit Position and Name	Description	Type	Reset Value (OTP/MTP)	Encoding, LSB, and Range
PWR_STATUS: 0x01	Bits[4:0]: PWR_STATE	Returns the power state status. 0x01: Safe mode 0x02: Standby mode 0x04: Active mode 0x08: Fault mode 0x10: Recovery mode	Read-only	0x01	N/A
PWR_STATUS: 0x01	Bits[9:7]: PACK_ CURRENT_ STATUS	Returns the pack current status. 0x1: The battery pack current is discharging 0x2: The battery pack current is in standby range, meaning it is within ±STBY_CUR_TH 0x4: The battery pack current is charging	Read-only	0x2	N/A

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STB_STATUS: 0x02	Bit[0]: STBY_STATE	Reports the on/off setting for standby mode. If off, the AFE does not transition to standby mode from active mode, regardless of whether the current level is in the standby mode range.	Read-only	0x0	0: Off 1: On
STB_STATUS: 0x02	Bit[6]: DSG_PFET_ SYNC	Reports whether the SBYDSG driver is on or off.	Read-only	0x0	0: Off 1: On
STB_STATUS: 0x02	Bits[10:8]: PACKP_COMP_ STS	Reports the voltage comparison result between PACKP and VTOP. The exact voltage level for the transition can be slightly different based on the direction of the transition and the applied hysteresis. 0x4: $V_{PACKP} > V_{VTOP} + 270mV$ 0x3: The PACKP comparator is invalid 0x2: $V_{VTOP} + 160mV > V_{PACKP} > V_{VTOP} - 1V$ 0x1: $V_{PACKP} < V_{VTOP} - 1.6V$ 0x0: The comparison result is not available	Read-only	0x0	N/A
ACT_CFG: 0x05	Bit[0]: FET_SRC	Defines the source that enables the MOSFETs and switches to active mode. The CHG and DSG MOSFETs are controlled by the host MCU, via either register or pin. 0: Register control 1: GPIO (GPIO1 or GPIO1 and GPIO2 depending on FET_CFG)	R/W (can lock to read-only)	0x0 (OTP)	N/A
ACT_CFG: 0x05	Bit[1]: FET_CFG	Selects the CHG and DSG MOSFET control logic. 0: Simple mode. The internal logic automatically determines the turn-on/-off sequencing 1: Direct mode. In direct mode with pin control, GPIO1 controls the DSG MOSFET and GPIO2 controls the CHG MOSFET. When direct mode is selected and faults are enabled, the IC still uses the internal logic to turn off the MOSFETs	R/W (can lock to read-only)	0x0 (OTP)	N/A
ACT_CFG: 0x05	Bits[4:3]: ACTIVE_ CTRL	When FET_SRC = 0 and FET_CFG = 0: 0x0: All MOSFETs are off 0x1: CHG and DSG turn on 0x2: All MOSFETs are off 0x3: CHG and DSG turn on When FET_SRC = 0 and FET_CFG = 1: 0x0: All MOSFETs are off 0x1: DSG turns on 0x2: CHG turns on 0x3: CHG and DSG turn on	R/W	0x0 (OTP)	N/A

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ACT_CFG: 0x05	Bit[9]: FT_STATE_SEL	0: Rising edge 1: Level When this bit is set to 0, the MOSFETs transition to start-up via a control source (depending on FET_SRC), which is disabled then enabled. When this bit is set to 1, the MOSFETs start up depending on the control source status.	R/W (can lock to read-only)	0x0 (OTP)	N/A
STB_CFG: 0x06	Bit[0]: STBY_STATE_EN	Enables or disables standby mode. When disabled, the device cannot enter standby mode.	R/W (can lock to read-only)	0x0 (OTP)	0: Disabled 1: Enabled
STB_CFG: 0x06	Bits[2:1]: STBY_CUR_TH	Sets the standby comparator current threshold.	R/W	0x0 (OTP)	0x0: 250µV 0x1: 375µV 0x2: 500µV 0x3: 625µV
STB_CFG: 0x06	Bit[3]: STBY_HYS	Enables the digital hysteresis on the standby current comparator. 1: Enabled 0: Disabled	R/W	0x0 (OTP)	N/A
STB_CFG: 0x06	Bits[5:4]: STBY_MONITOR_CFG	Selects the interval used for voltage protection monitoring to refresh the ADC reading while in standby or safe mode: 0x0: Voltage protection readings are refreshed every 254ms 0x1: Voltage protection readings are refreshed every 492ms 0x2: Voltage protection readings are refreshed every 968ms 0x3: Not allowed	R/W (can lock to read-only)	0x2 (OTP)	N/A
STB_CFG: 0x06	Bit[6]: STBY_PFET_EN	Enables the P-channel MOSFET in standby mode when ENABLE_REG_CFG is set to simple mode. To control the standby MOSFET in direct mode, use P_FET_MANUAL setting together with P_FET_MAN_CTRL to turn the driver on and off.	R/W (can lock to read-only)	0x0 (OTP)	0: Disabled 1: Enabled
SAFE_CFG: 0x07	Bit[0]: PROTECT_IN_SAFE_CFG	1: Enables voltage protection monitoring in safe mode 0: Disables voltage protection monitoring in safe mode	R/W	0x0 (OTP)	0: Disabled 1: Enabled
SAFE_CFG: 0x07	Bit[1]: SAFE_SCOC_EN	Enables short-circuit (SC) and over-current (OC) monitoring, even in safe mode. This function is disabled by default, since the MOSFETs are disabled in safe mode. If enabled, current consumption increases.	R/W	0x0	0: Disabled 1: Enabled

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SAFE_CFG: 0x07	Bit[3]: ACTIVE_ MONITOR_CFG	Selects the interval used for voltage protection monitoring to refresh the ADC reading in active mode. 0x0: Voltage protection readings are refreshed every 254ms 0x1: Voltage protection readings are refreshed every 135ms	R/W	0x0	N/A
RGL_CFG: 0x08	Bit[2]: V3P3_SHDN_ EN	Enables the 3.3V regulator during shutdown mode.	R/W (can lock to read-only)	0x1 (OTP)	0: Disabled 1: Enabled
RGL_CFG: 0x08	Bit[3]: V3P3_SHOFF_ STS	Reports the internal enable/disable control for the 3.3V regulator during shutdown mode. When enabled, the 3.3V rails stay on even in shutdown mode.	Read-only	0x1	0: Disabled 1: Enabled
LOAD_ CHARGER_ CFG: 0x09	Bit[15]: PACKP_CMP_ EN	Enables the PACKP vs. VTOP comparator. When disabled, the comparator can still be internally enabled for other functions, such as short-circuit removal detection.	R/W	0x0 (OTP)	0: Disabled 1: Enabled

Pins and GPIO

Address Name and Location	Field Bit Position and Name	Description	Type	Value Reset (OTP/MTP)	Encoding, LSB and Range
GPIO_ STATUS: 0x0A	Bit[0]: GPIO1	Reports the GPIO1 pin status (high/low).	Read-only	0x1	0: Low 1: High
GPIO_ STATUS: 0x0A	Bit[1]: GPIO2	Reports the GPIO2 pin status (high/low).	Read-only	0x1	0: Low 1: High
GPIO_ STATUS: 0x0A	Bit[2]: GPIO3	Reports the GPIO3 pin status (high/low).	Read-only	0x1	0: Low 1: High
GPIO_OUT: 0x0B	Bit[0]: GPIO1_O	Sets the target output level for GPIO1 (high or low). This bit is effective only when GPIO1 is used as a digital output (GPIO1_IO is set to output).	R/W	0x0 (OTP)	0: Low 1: High
GPIO_OUT: 0x0B	Bit[1]: GPIO2_O	Sets the target output level for GPIO2 (high or low). This bit is effective only when GPIO2 is used as a digital output (GPIO2_IO is set to output).	R/W	0x0 (OTP)	0: Low 1: High
GPIO_OUT: 0x0B	Bit[2]: GPIO3_O	Sets the target output level for GPIO3 (high or low). This bit is effective only when GPIO3 is used as a digital output (GPIO3_IO is set to output).	R/W	0x0 (OTP)	0: Low 1: High
GPIO_CFG: 0x0C	Bit[0]: GPIO1_IO	Defines the direction for GPIO1. 0: Output 1: Input	R/W (can lock to read-only)	0x1 (OTP)	N/A
GPIO_CFG: 0x0C	Bit[1]: GPIO1_TYPE	Defines the type of input for GPIO1. 0: Digital input 1: Buffered ADC input, 3.3V range	R/W (can lock to read-only)	0x0 (OTP)	N/A

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GPIO_CFG: 0x0C	Bit[2]: GPIO1_PUP	Enables the GPIO1 pull-up capability. When enabled, a 20kΩ pull-up resistor is applied to GPIO1.	R/W (can lock to read-only)	0x1 (OTP)	0: Disabled 1: Enabled
GPIO_CFG: 0x0C	Bit[4]: GPIO2_IO	Defines the direction for GPIO2. 0: Output 1: Input	R/W (can lock to read-only)	0x1 (OTP)	N/A
GPIO_CFG: 0x0C	Bit[5]: GPIO2_TYPE	Defines the input type for GPIO2. 0: Digital input 1: Buffered ADC input, 3.3V range	R/W (can lock to read-only)	0x0 (OTP)	N/A
GPIO_CFG: 0x0C	Bit[6]: GPIO2_PUP	Enables the GPIO2 pull-up capability. When enabled, a 20kΩ pull-up resistor is applied to GPIO2.	R/W (can lock to read-only)	0x1 (OTP)	0: Disabled 1: Enabled
GPIO_CFG: 0x0C	Bit[8]: GPIO3_IO	Defines the direction for GPIO3. 0: Output 1: Input	R/W (can lock to read-only)	0x1 (OTP)	N/A
GPIO_CFG: 0x0C	Bit[9]: GPIO3_TYPE	Defines the input type for GPIO3. 0: Digital input 1: Buffered ADC input, 3.3V range	R/W (can lock to read-only)	0x0 (OTP)	N/A
GPIO_CFG: 0x0C	Bit[10]: GPIO3_PUP	Enables the GPIO3 pull-up capability. When enabled, a 20kΩ pull-up resistor is applied to GPIO3.	R/W (can lock to read-only)	0x1 (OTP)	0: Disabled 1: Enabled
GPIO_CFG: 0x0C	Bit[11]: GPIO3_FSEL	0: GPIO 1: Fault indicator. Valid when GPIO3 is set to be an output	R/W (can lock to read-only)	0x0 (OTP)	N/A
PINS_CFG: 0x0D	Bit[0]: ALERT_POL	0: Active low. xAlert goes low when an interrupt is pending 1: Active high. xAlert goes high when an interrupt is pending	R/W (can lock to read-only)	0x1 (OTP)	N/A
PINS_CFG: 0x0D	Bit[5]: WDT_RPT	When enabled, a bite event triggers the WDT pin to toggle a high pulse.	R/W (can lock to read-only)	0x1 (OTP)	0: Disabled 1: Enabled
PINS_CFG: 0x0D	Bit[6]: WDT_RST_EN	Enables the WDT pin to reset the MP2796 back to its factory settings. When disabled, a WDT pulse caused by a watchdog bite does not trigger a reset.	R/W (can lock to read-only)	0x1 (OTP)	0: Disabled 1: Enabled
PINS_CFG: 0x0D	Bit[8]: GPIO_LV_CFG	Sets the GPIO1~3 pull-up voltage. 0: 3V3 1: REGIN	R/W (can lock to read-only)	0x0 (OTP)	N/A

Watchdog Functions

Address Name and Location	Field Bit Position and Name	Description	Type	Value Reset (OTP/MTP)	Encoding, LSB and Range
WDT_STATUS: 0x0E	Bit[0]: WDT_BARKED	Indicates whether the bark timer has expired and a bark event has occurred.	Read-only	0x0	0: False 1: True
WDT_STATUS: 0x0E	Bit[1]: WDT_BITE	Indicates whether the bite timer has expired and a bite event has occurred. This event toggles the WDT pin, if WDT_RPT is set to enable.	Read-only	0x0	0: False 1: True

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WDT_RST: 0x0F	Bit[0]: WDT_RST	Writing 1 to this bit resets the watchdog timer counter, and clears WDT_BITE and WDT_BARKED. This is a self-clearing register.	Write-only	0x0	1: Reset the counter and clear the bits
WDT_CFG: 0x10	Bit[0]: WDT_COM_ CTRL	Enables watchdog communication.	R/W (can lock to read-only)	0x0 (OTP)	0: Disabled 1: Enabled
WDT_CFG: 0x10	Bits[8:2]: WDT_BARK_ CFG	Configures the watchdog bark timeout. The bark setting defines the delay from the last watchdog reset to the bark.	R/W (can lock to read-only)	0x4F (OTP)	LSB: 25ms RNG: 25ms to 3200ms 0x00: 25ms
WDT_CFG: 0x10	Bits[15:9]: WDT_BITE_CFG	Configures the watchdog bite timeout. The bite setting defines the delay from the bark to the bite.	R/W (can lock to read-only)	0x77 (OTP)	LSB: 25ms RNG: 25ms to 3200ms 0x00: 25ms

MOSFET Driver

Address Name and Location	Field Bit Position and Name	Description	Type	Value Reset (OTP/MTP)	Encoding, LSB and Range
FET_STATUS: 0x11	Bit[0]: CHG_DRV	Reports whether the CHG driver is on or off.	Read-only	0x0	0: Off 1: On
FET_STATUS: 0x11	Bit[1]: DSG_DRV	Reports whether the DSG driver is on or off.	Read-only	0x0	0: Off 1: On
FET_STATUS: 0x11	Bit[2]: SBYDSG_DRV	Reports whether the SBYDSG driver is on or off.	Read-only	0x0	0: Off 1: On
FET_STATUS: 0x11	Bit[3]: FET_TIMEOUT	When true, an issue was detected during the latest turn-on attempt.	Read-only	0x0	0: False 1: True
FET_STATUS: 0x11	Bit[8]: CHG_DRV_ TRANS	1: The CHG driver is changing states 0: The CHG driver is settled (off or at its target voltage)	Read-only	0x0	N/A
FET_STATUS: 0x11	Bit[9]: DSG_DRV_ TRANS	1: The DSG driver is changing states 0: The DSG driver is settled (off or at its target voltage)	Read-only	0x0	N/A
FET_STATUS: 0x11	Bit[10]: SBYDSG_DRV_ TRANS	1: The SBYDSG driver is changing states 0: The SBYDSG driver is settled (off or at its target voltage)	Read-only	0x0	N/A
FET_STATUS: 0x11	Bit[11]: CP_STS	Indicates the charge pump's status (on or off).	Read-only	0x0	0: Off 1: On
FET_CTRL: 0x12	Bit[0]: P_FET_MAN_ CTRL	Turns the SBYDSG MOSFET driver on and off. To use this bit, P_FET_MANUAL must be enabled, and the IC must be in direct mode.	R/W	0x0 (OTP)	0: Off 1: On
FET_MODE: 0x13	Bit[0]: DSG_SOFTON_ EN	Enables soft start for the DSG MOSFET driver.	R/W (can lock to read-only)	0x1 (OTP)	0: Disabled 1: Enabled

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FET_MODE: 0x13	Bit[3]: FET_ON_ RUN_SC_DET_ EN	Enables the short-circuit detection sequence prior to the MOSFET turning on. If detection is enabled and the device detects that PACKP is shorted to ground, then a MOSFET driver fault is generated. The associated MOSFET driver bit can be manually cleared with DRIVER_FAULT_CLR.	R/W (can lock to read-only)	0x1 (OTP)	0: Disabled 1: Enabled
FET_MODE: 0x13	Bit[4]: CHG_SOFTON_ EN	0: CHG soft start disabled 1: CHG soft start enabled	R/W (can lock to read-only)	0x1 (OTP)	0: Disabled 1: Enabled
FET_MODE: 0x13	Bits[7:5]: TURNON_ TIMEOUT	Sets the MOSFET turn-on timeout delay. Applies to both the CHG and DSG MOSFETs. This function is paused during soft start (SS).	R/W	0x0 (OTP)	LSB: 20ms RNG: 40ms to 180ms 0: 40ms
FET_MODE: 0x13	Bit[8]: CHG_TURNON_ TIMER	Changes the CHG SS timeout.	R/W (can lock to read-only)	0x1 (OTP)	0: 25ms 1: 50ms
FET_MODE: 0x13	Bit[9]: TURNON_ TIMEOUT_ FAULT	0: A fault is not triggered after turn-on timeout 1: A fault is triggered after turn-on timeout	R/W (can lock to read-only)	0x0 (OTP)	0: Disabled 1: Enabled
FET_MODE: 0x13	Bit[11]: CHG_SOFTON_ OC_LIM	Sets the over-current (OC) threshold that is only applicable when the CHG undergoes SS.	R/W (can lock to read-only)	0x0 (OTP)	0: 3.6mV 1: 4.8mV
FET_MODE: 0x13	Bit[12]: P_FET_ MANUAL	Enables the manual control of the P-channel MOSFET, only effective when direct mode is enabled (FET_CFG = 1). When this bit is enabled, P_FET_MAN_CTRL can be used to control the SBYDSG driver.	R/W (can lock to read-only)	0x0 (OTP)	0: Disabled 1: Enabled
FET_CFG: 0x14	Bits[2:0]: DSG_SOFTON_ DV	Sets the discharge MOSFET turn-on slope. 3’b000: 0.1V/ms 3’b001: 0.2V/ms 3’b010: 0.4V/ms 3’b011: 0.6V/ms 3’b100: 0.8V/ms 3’b101: 1.0V/ms 3’b110: 1.2V/ms 3’b111: 1.6V/ms	R/W (can lock to read-only)	0x0 (MTP)	N/A
FET_CFG: 0x14	Bits[5:4]: STBY_SC_ CUR_TH	Sets the standby comparator current threshold, which acts as a protection again excessive current while the DSG N-channel MOSFET ramps up during SS.	R/W	0x3 (OTP)	0x0: 250µV 0x1: 375µV 0x2: 500µV 0x3: 625µV

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FET_CFG: 0x14	Bits[8:6]: RAMP_UP_SC_GF	Deglitch filter for the standby comparator current threshold when DSG N-channel MOSFET is ramping up during SS. 3'b000: 100µs 3'b001: 200µs 3'b010: 400µs 3'b011: 800µs 3'b100: 1200µs 3'b101: 2400µs 3'b110: 2400µs 3'b111: 2400µs	R/W	0x3 (OTP)	N/A
FET_CFG: 0x14	Bits[11:9]: CHG_SOFTON_PUP	Sets the pull-up current values during CHG MOSFET SS.	R/W (can lock to read-only)	0x4 (MTP)	LSB: 1µA, RNG: 3µA to 10µA 0x0: 3µA
FET_CFG: 0x14	Bits[14:12]: FET_DRV_LVL	Defines V_{GS} for the CHG and DSG MOSFETs.	R/W (can lock to read-only)	0x3 (OTP)	0x0: 7V 0x1: 8V 0x2: 9V 0x3: 10V 0x4: 11V 0x5: 12V 0x6: 12V 0x7: 12V

Interrupt

Address Name and Location	Field Bit Position and Name	Description	Type	Value Reset (OTP/MTP)	Encoding, LSB and Range
RD_INT0: 0x15	Bit[0]: CELL_OV_INT_STS	Reports whether an interrupt related to a cell over-voltage (OV) event has been detected. The flags located in RD_CELL_OV should be checked to identify which cell caused the interrupt.	Read-only	0x0	0: Not detected 1: Detected
RD_INT0: 0x15	Bit[1]: CELL_UV_INT_STS	Reports whether an interrupt related to a cell under-voltage (UV) event has been detected. The flags located in RD_CELL_UV should be checked to identify which cell caused the interrupt.	Read-only	0x0	0: Not detected 1: Detected
RD_INT0: 0x15	Bit[2]: VTOP_UV_INT_STS	Reports whether a UV interrupt related to the battery stack positive terminal (VTOP) has been detected.	Read-only	0x0	0: Not detected 1: Detected
RD_INT0: 0x15	Bit[3]: VTOP_OV_INT_STS	Reports whether an OV interrupt related to the battery stack positive terminal (VTOP) has been detected.	Read-only	0x0	0: Not detected 1: Detected
RD_INT0: 0x15	Bit[4]: OVER_CURR_INT_STS	Reports whether an interrupt related to an over-current (OC) event has been detected. This signal is generated by combining the interrupt detection for discharge OC and charge OC. OC1_DCHG_STS, OC2_DCHG_STS, and OC_CHG_STS should be checked to identify the source of the interrupt.	Read-only	0x0	0: Not detected 1: Detected

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RD_INT0: 0x15	Bit[5]: SHORT_CURR_ INT_STS	Reports whether an interrupt related to a short-circuit event has been detected. This signal is generated by combining the interrupt detection for discharge short-circuit and charge short-circuit. SC_CHG_STS and SC_DCHG_STS should be checked to identify the source of the interrupt.	Read-only	0x0	0: Not detected 1: Detected
RD_INT0: 0x15	Bit[6]: NTC_COLD_ INT_STS	Reports whether an interrupt related to an NTC cold event has been detected. This signal is generated combining the interrupt detection for all 4 NTC channels. NTC1_CELL_COLD_STS, NTC2_CELL_COLD_STS, NTC3_CELL_COLD_STS, and NTC4_CELL_COLD_STS should be checked to identify the source of the interrupt.	Read-only	0x0	0: Not detected 1: Detected
RD_INT0: 0x15	Bit[7]: NTC_HOT_INT_ STS	Reports whether an interrupt related to an NTC hot event has been detected. This signal is generated by combining the interrupt detection for all 4 NTC channels. NTC1_CELL_HOT_STS, NTC2_CELL_HOT_STS, NTC3_CELL_HOT_STS, and NTC4_CELL_HOT_STS should be checked to identify the source of the interrupt.	Read-only	0x0	0: Not detected 1: Detected
RD_INT0: 0x15	Bit[8]: WDT_INT_STS	Reports whether an interrupt related to watchdog communication has been detected. A watchdog bark and a watchdog bite event can both trigger a watchdog event interrupt.	Read-only	0x0	0: Not detected 1: Detected
RD_INT0: 0x15	Bit[9]: RECOVERED_ INT_STS	Reports whether an interrupt related to fault recovery event has been detected.	Read-only	0x0	0: Not detected 1: Detected
RD_INT0: 0x15	Bit[10]: AFE_MODE_ CHANGE_ INT_STS	Reports whether an interrupt related to an AFE mode change has been detected. A mode change is a change between any of the operating modes (e.g. safe, fault, active, standby).	Read-only	0x0	0: Not detected 1: Detected
RD_INT0: 0x15	Bit[11]: VSCAN_DONE_ INT_STS	Reports whether an interrupt related to a high-resolution voltage scan has been detected.	Read-only	0x0	0: Not detected 1: Detected
RD_INT0: 0x15	Bit[14]: PACK_ CURRENT_INT_ STS	Reports whether an interrupt related to a battery pack current change has been detected. The pack current changes when switching between discharge, standby, and charge mode, which is reported in PACK_CURRENT_STATUS.	Read-only	0x0	0: Not detected 1: Detected

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RD_INT1: 0x16	Bit[0]: OTP_CRC_ EVENT_INT_ STS	Reports whether an interrupt related to a one-time-programmable (OTP) memory CRC fault has been detected. When enabled, this interrupt can be triggered by the following conditions: • The OTP CRC calculation fails while restoring the OTP • OTP CRC is manually triggered using OTP_CRC_DO. In this scenario, an interrupt event is generated when a CRC check is completed (for either passing or failing)	Read-only	0x0	0: Not detected 1: Detected
RD_INT1: 0x16	Bit[1]: REGIN_INT_ STS	Reports whether an interrupt related to a UV condition on REGIN has been detected.	Read-only	0x0	0: Not detected 1: Detected
RD_INT1: 0x16	Bit[2]: 3V3_INT_STS	Reports whether an interrupt related to a UV condition on 3V3 has been detected. This is triggered by monitoring the 3V3 ADC or the 3.3V analog comparator. The 3.3V UV analog comparator is always enabled, so when 3V3_INT_EN is enabled, it can trigger an interrupt even if 3V3_EN is disabled.	Read-only	0x0	0: Not detected 1: Detected
RD_INT1: 0x16	Bit[3]: VDD_INT_STS	Reports whether an interrupt related to a UV condition on VDD has been detected. A VDD UV event can be triggered by either ADC voltage monitoring or the VDD UV comparator. The VDD analog comparator is always enabled, so when VDD_INT_EN is enabled, it can trigger an interrupt even if VDD_EN is disabled.	Read-only	0x0	0: Not detected 1: Detected
RD_INT1: 0x16	Bit[4]: OPEN_WIRE_ INT_STS	Reports whether an interrupt related to an open-wire event has been detected. The open wire status registers (located at the RD_OPENH and RD_OPENL addresses) must be checked to determine whether there are disconnected wires.	Read-only	0x0	0: Not detected 1: Detected
RD_INT1: 0x16	Bit[5]: CELL_DEAD_ INT_STS	Reports whether an interrupt related to a dead cell has been detected.	Read-only	0x0	0: Not detected 1: Detected
RD_INT1: 0x16	Bit[6]: CELL_ MISMATCH_ INT_STS	Reports whether an interrupt related to a cell mismatch has been detected. Flags in the RD_CELL_MSMT and CELL_MSMT_LOWER registers should be read to identify the cells triggering the event.	Read-only	0x0	0: Not detected 1: Detected

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RD_INT1: 0x16	Bit[7]: DIE_TEMP_INT_STS	Reports whether an interrupt related to a digital die temperature event has been detected.	Read-only	0x0	0: Not detected 1: Detected
RD_INT1: 0x16	Bit[8]: PCB_MNTR_HOT_INT_STS	Reports whether an interrupt related to the NTC hot PCB monitor has been detected. NTC1_PCB_MNTR_HOT_STS, NTC2_PCB_MNTR_HOT_STS, NTC3_PCB_MNTR_HOT_STS, and NTC4_PCB_MNTR_HOT_STS should be checked to identify which NTC caused the interrupt.	Read-only	0x0	0: Not detected 1: Detected
RD_INT1: 0x16	Bit[9]: FSM_ERROR_INT_STS	Reports whether an interrupt related to a scheduler error event has been detected.	Read-only	0x0	0: Not detected 1: Detected
RD_INT1: 0x16	Bit[10]: SELF_TEST_INT_STS	Reports whether an interrupt related to an ADC self-diagnostic event has been detected. The SELF_TEST_STS_OV and SELF_TEST_STS_UV flags should be checked to identify the cause of the interrupt.	Read-only	0x0	0: Not detected 1: Detected
RD_INT1: 0x16	Bit[11]: BAL_DONE_INT_STS	Reports whether an interrupt related to a cell-balancing done event has been detected.	Read-only	0x0	0: Not detected 1: Detected
RD_INT1: 0x16	Bit[12]: PACKP_V_INT_STS	Reports whether an interrupt related to a PACKP voltage change event has been detected.	Read-only	0x0	0: Not detected 1: Detected
RD_INT1: 0x16	Bit[13]: FET_DRIVER_INT_STS	Reports whether an interrupt related to a MOSFET driver error has been detected. MOSFET driver errors cover the following conditions: • MOSFET timeout • An issue detected during a short-circuit or OC fault clearing sequence • An issue during CHG or DSG SS, such as a short-circuit or an OC condition	Read-only	0x0	0: Not detected 1: Detected
INT0_CLR: 0x17	Bit[0]: CELL_OV_INT_CLEAR	Write 1 to this bit to clear a cell OV interrupt. This is a self-clearing register.	Write-only	0x0	1: Clear the interrupt
INT0_CLR: 0x17	Bit[1]: CELL_UV_INT_CLEAR	Write 1 to this bit to clear a cell UV interrupt. This is a self-clearing register.	Write-only	0x0	1: Clear the interrupt
INT0_CLR: 0x17	Bit[2]: VTOP_UV_INT_CLEAR	Write 1 to this bit to clear a battery pack UV interrupt. This is a self-clearing register.	Write-only	0x0	1: Clear the interrupt
INT0_CLR: 0x17	Bit[3]: VTOP_OV_INT_CLEAR	Write 1 to this bit to clear a battery pack OV interrupt. This is a self-clearing register.	Write-only	0x0	1: Clear the interrupt
INT0_CLR: 0x17	Bit[4]: OVER_CURR_INT_CLEAR	Write 1 to this bit to clear an OC interrupt. This is a self-clearing register.	Write-only	0x0	1: Clear the interrupt

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INT0_CLR: 0x17	Bit[5]: SHORT_CURR_ INT_CLEAR	Write 1 to this bit to clear a short-circuit interrupt. This is a self-clearing register.	Write-only	0x0	1: Clear the interrupt
INT0_CLR: 0x17	Bit[6]: NTC_COLD_ INT_CLEAR	Write 1 to this bit to clear an NTC cold cell monitor interrupt. This is a self-clearing register.	Write-only	0x0	1: Clear the interrupt
INT0_CLR: 0x17	Bit[7]: NTC_HOT_INT_ CLEAR	Write 1 to this bit to clear an NTC hot cell monitor interrupt. This is a self-clearing register.	Write-only	0x0	1: Clear the interrupt
INT0_CLR: 0x17	Bit[8]: WDT_INT_ CLEAR	Write 1 to this bit to clear a watchdog event interrupt. This is a self-clearing register.	Write-only	0x0	1: Clear the interrupt
INT0_CLR: 0x17	Bit[9]: RECOVERED_ INT_CLEAR	Write 1 to this bit to clear a fault recovery interrupt. This is a self-clearing register.	Write-only	0x0	1: Clear the interrupt
INT0_CLR: 0x17	Bit[10]: AFE_MODE_ CHANGE_INT_ CLEAR	Write 1 to this bit to clear an AFE mode change interrupt. This is a self-clearing register.	Write-only	0x0	1: Clear the interrupt
INT0_CLR: 0x17	Bit[11]: VSCAN_DONE_ INT_CLEAR	Write 1 to this bit to clear a completed high-resolution voltage scan interrupt. This is a self-clearing register.	Write-only	0x0	1: Clear the interrupt
INT0_CLR: 0x17	Bit[14]: PACK_ CURRENT_INT_ CLEAR	Write 1 to this bit to clear a battery pack current change interrupt. This is a self-clearing register.	Write-only	0x0	1: Clear the interrupt
INT1_CLR: 0x18	Bit[0]: OTP_CRC_ EVENT_INT_ CLEAR	Write 1 to this bit to clear an OTP CRC interrupt. This is a self-clearing register.	Write-only	0x0	1: Clear the interrupt
INT1_CLR: 0x18	Bit[1]: REGIN_INT_ CLEAR	Write 1 to this bit to clear a REGIN interrupt. This is a self-clearing register.	Write-only	0x0	1: Clear the interrupt
INT1_CLR: 0x18	Bit[2]: 3V3_INT_ CLEAR	Write 1 to this bit to clear a 3V3 UV interrupt. This is a self-clearing register.	Write-only	0x0	1: Clear the interrupt
INT1_CLR: 0x18	Bit[3]: VDD_INT_ CLEAR	Write 1 to this bit to clear a VDD UV interrupt. This is a self-clearing register.	Write-only	0x0	1: Clear the interrupt
INT1_CLR: 0x18	Bit[4]: OPEN_WIRE_ INT_CLEAR	Write 1 to this bit to clear an open wire interrupt. This is a self-clearing register.	Write-only	0x0	1: Clear the interrupt
INT1_CLR: 0x18	Bit[5]: CELL_DEAD_ INT_CLEAR	Write 1 to this bit to clear a dead cell interrupt. This is a self-clearing register.	Write-only	0x0	1: Clear the interrupt
INT1_CLR: 0x18	Bit[6]: CELL_ MISMATCH_ INT_CLEAR	Write 1 to this bit to clear a mismatched cell interrupt. This is a self-clearing register.	Write-only	0x0	1: Clear the interrupt
INT1_CLR: 0x18	Bit[8]: PCB_MNTR_ TEMP_INT_ CLEAR	Write 1 to this bit to clear an NTC hot PCB monitor interrupt. This is a self-clearing register.	Write-only	0x0	1: Clear the interrupt

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INT1_CLR: 0x18	Bit[9]: FSM_ERROR_ INT_CLEAR	Write 1 to this bit to clear a schedule error interrupt. This is a self-clearing register.	Write-only	0x0	1: Clear the interrupt
INT1_CLR: 0x18	Bit[10]: SELF_TEST_ INT_CLEAR	Write 1 to this bit to clear a self-diagnostic interrupt. This is a self-clearing register.	Write-only	0x0	1: Clear the interrupt
INT1_CLR: 0x18	Bit[11]: BAL_DONE_ INT_CLEAR	Write 1 to this bit to clear a balancing complete interrupt. This is a self-clearing register.	Write-only	0x0	1: Clear the interrupt
INT1_CLR: 0x18	Bit[12]: PACKP_V_INT_ CLEAR	Write 1 to this bit to clear a PACKP voltage change interrupt. This is a self-clearing register.	Write-only	0x0	1: Clear the interrupt
INT1_CLR: 0x18	Bit[13]: FET_DRIVER_ INT_CLEAR	Write 1 to this bit to clear a MOSFET driver event interrupt. This is a self-clearing register.	Write-only	0x0	1: Clear the interrupt
INT0_EN: 0x19	Bit[0]: CELL_OV_INT_ EN	Enables interrupt reporting for cell OV conditions.	R/W	0x0	0: Disabled 1: Enabled
INT0_EN: 0x19	Bit[1]: CELL_UV_INT_ EN	Enables interrupt reporting for cell UV conditions.	R/W	0x0	0: Disabled 1: Enabled
INT0_EN: 0x19	Bit[2]: VTOP_UV_INT_ EN	Enables interrupt reporting for battery pack UV conditions.	R/W	0x0	0: Disabled 1: Enabled
INT0_EN: 0x19	Bit[3]: VTOP_OV_INT_ EN	Enables interrupt reporting for battery pack OV conditions.	R/W	0x0	0: Disabled 1: Enabled
INT0_EN: 0x19	Bit[4]: OVER_CURR_ INT_EN	Enables interrupt reporting for OC conditions. Note that there are individual enable/disable control bits: OC_CHG_INT_EN, OC2_DCHG_INT_EN, and OC1_DCHG_INT_EN. OVER_CURR_INT_EN acts as a master enabler, so it must be enabled for the charger and discharge interrupt to work.	R/W	0x0	0: Disabled 1: Enabled
INT0_EN: 0x19	Bit[5]: SHORT_CURR_ INT_EN	Enables interrupt reporting for short-circuit conditions. Note that there are individual enable/disable control bits: SC_CHG_INT_EN and SC_DCHG_INT_EN. SHORT_CURR_INT_EN acts as a master enabler, so it must be enabled for the charger and discharge interrupt to work.	R/W	0x0	0: Disabled 1: Enabled
INT0_EN: 0x19	Bit[6]: NTC_COLD_ INT_EN	Enables interrupt reporting for NTC cold cell monitoring conditions.	R/W	0x0	0: Disabled 1: Enabled
INT0_EN: 0x19	Bit[7]: NTC_HOT_INT_ EN	Enables interrupt reporting for NTC hot cell monitoring conditions.	R/W	0x0	0: Disabled 1: Enabled
INT0_EN: 0x19	Bit[8]: WDT_INT_EN	Enables interrupt reporting for watchdog communication.	R/W	0x0	0: Disabled 1: Enabled
INT0_EN: 0x19	Bit[9]: RECOVERED_ INT_EN	Enables interrupt reporting for fault recovery.	R/W	0x0	0: Disabled 1: Enabled

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INT0_EN: 0x19	Bit[10]: AFE_MODE_CHANGE_INT_EN	Enables interrupt reporting an AFE mode change.	R/W	0x0	0: Disabled 1: Enabled
INT0_EN: 0x19	Bit[11]: VSCAN_DONE_INT_EN	Enables interrupt reporting for high-resolution voltage ADC scan completion.	R/W	0x0	0: Disabled 1: Enabled
INT0_EN: 0x19	Bit[14]: PACK_CURRENT_INT_EN	Enables interrupt reporting for battery pack current direction changes.	R/W	0x0	0: Disabled 1: Enabled
INT0_EN: 0x19	Bit[15]: INT_ALERT_CTRL	Enables interrupt reporting to the xALERT pin.	R/W (can lock to read-only)	0x1 (OTP)	0: Disabled 1: Enabled
INT1_EN: 0x1A	Bit[0]: OTP_CRC_EVENT_INT_EN	Enables interrupt reporting for an OTP CRC event.	R/W	0x1	0: Disabled 1: Enabled
INT1_EN: 0x1A	Bit[1]: REGIN_INT_EN	Enables interrupt reporting for a REGIN UV event.	R/W	0x0	0: Disabled 1: Enabled
INT1_EN: 0x1A	Bit[2]: 3V3_INT_EN	Enables interrupt reporting for a 3V3 UV event.	R/W	0x0	0: Disabled 1: Enabled
INT1_EN: 0x1A	Bit[3]: VDD_INT_EN	Enables interrupt reporting for a VDD UV event.	R/W	0x0	0: Disabled 1: Enabled
INT1_EN: 0x1A	Bit[4]: OPEN_WIRE_INT_EN	Enables interrupt reporting for completed open-wire detection.	R/W	0x0	0: Disabled 1: Enabled
INT1_EN: 0x1A	Bit[5]: CELL_DEAD_INT_EN	Enables interrupt reporting for a dead cell condition.	R/W	0x0	0: Disabled 1: Enabled
INT1_EN: 0x1A	Bit[6]: CELL_MISMATCH_INT_EN	Enables interrupt reporting for a cell mismatch condition.	R/W	0x0	0: Disabled 1: Enabled
INT1_EN: 0x1A	Bit[7]: DIE_TEMP_INT_EN	Enables interrupt reporting for a die over-temperature (OT) event.	R/W	0x0	0: Disabled 1: Enabled
INT1_EN: 0x1A	Bit[8]: PCB_MNTR_TEMP_INT_EN	Enables interrupt reporting for an NTC hot PCB condition.	R/W	0x0	0: Disabled 1: Enabled
INT1_EN: 0x1A	Bit[9]: FSM_ERROR_INT_EN	Enables interrupt reporting for a scheduled error.	R/W	0x0	0: Disabled 1: Enabled
INT1_EN: 0x1A	Bit[10]: SELF_TEST_INT_EN	Enables interrupt reporting for an ADC self-diagnostics OV/UV conditions.	R/W	0x0	0: Disabled 1: Enabled
INT1_EN: 0x1A	Bit[11]: BAL_DONE_INT_EN	Enables interrupt reporting for completed cell-balancing.	R/W	0x0	0: Disabled 1: Enabled
INT1_EN: 0x1A	Bit[12]: PACKP_V_INT_EN	Enables interrupt reporting for PACKP voltage changes.	R/W	0x0	0: Disabled 1: Enabled
INT1_EN: 0x1A	Bit[13]: FET_DRIVER_INT_EN	Enables interrupt reporting for MOSFET driver issues.	R/W	0x0	0: Disabled 1: Enabled

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INT_TYPE0: 0x1B	Bits[1:0]: VTOP_UV_INT_TYPE	Controls the triggering logic for a battery pack UV interrupt. 0x0: Interrupt generated on input status signal high 0x1: Interrupt generated on the rising edge of the input status signal 0x2: Interrupt generated on the falling edge of the input status signal 0x3: Interrupt generated on the rising and falling edges of the input status signal	R/W	0x0	N/A
INT_TYPE0: 0x1B	Bits[3:2]: VTOP_OV_INT_TYPE	Controls the triggering logic for a battery pack OV interrupt. 0x0: Interrupt generated on input status signal high 0x1: Interrupt generated on the rising edge of the input status signal 0x2: Interrupt generated on the falling edge of the input status signal 0x3: Interrupt generated on the rising and falling edges of the input status signal	R/W	0x0	N/A
INT_TYPE0: 0x1B	Bits[5:4]: NTC_COLD_INT_TYPE	Controls the triggering logic for an NTC cold cell monitor interrupt. 0x0: Interrupt generated on input status signal high 0x1: Interrupt generated on the rising edge of the input status signal 0x2: Interrupt generated on the falling edge of the input status signal 0x3: Interrupt generated on the rising and falling edges of the input status signal	R/W	0x0	N/A
INT_TYPE0: 0x1B	Bits[7:6]: NTC_HOT_INT_TYPE	Controls the triggering logic for an NTC hot cell monitor interrupt. 0x0: Interrupt generated on input status signal high 0x1: Interrupt generated on the rising edge of the input status signal 0x2: Interrupt generated on the falling edge of the input status signal 0x3: Interrupt generated on the rising and falling edges of the input status signal	R/W	0x0	N/A
INT_TYPE1: 0x1C	Bits[9:8]: REGIN_INT_TYPE	Controls the triggering logic for a REGIN interrupt. 0x0: Interrupt generated on input status signal high 0x1: Interrupt generated on the rising edge of the input status signal 0x2: Interrupt generated on the falling edge of the input status signal 0x3: Interrupt generated on the rising and falling edges of the input status signal	R/W	0x0	N/A

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INT_TYPE1: 0x1C	Bits[11:10]: 3V3_INT_TYPE	Controls the triggering logic for a 3V3 interrupt. 0x0: Interrupt generated on input status signal high 0x1: Interrupt generated on the rising edge of the input status signal 0x2: Interrupt generated on the falling edge of the input status signal 0x3: Interrupt generated on the rising and falling edges of the input status signal	R/W	0x0	N/A
INT_TYPE1: 0x1C	Bits[13:12]: VDD_INT_TYPE	Controls the triggering logic for a VDD UV interrupt. 0x0: Interrupt generated on input status signal high 0x1: Interrupt generated on the rising edge of the input status signal 0x2: Interrupt generated on the falling edge of the input status signal 0x3: Interrupt generated on the rising and falling edges of the input status signal	R/W	0x0	N/A
INT_TYPE2: 0x1D	Bits[1:0]: CELL_DEAD_ INT_TYPE	Controls the triggering logic for a dead cell interrupt. 0x0: Interrupt generated on input status signal high 0x1: Interrupt generated on the rising edge of the input status signal 0x2: Interrupt generated on the falling edge of the input status signal 0x3: Interrupt generated on the rising and falling edges of the input status signal	R/W	0x0	N/A
INT_TYPE2: 0x1D	Bits[3:2]: CELL_ MISMATCH_ INT_TYPE	Controls the triggering logic for a mismatched cell interrupt. 0x0: Interrupt generated on input status signal high 0x1: Interrupt generated on the rising edge of the input status signal 0x2: Interrupt generated on the falling edge of the input status signal 0x3: Interrupt generated on the rising and falling edges of the input status signal	R/W	0x0	N/A
INT_TYPE2: 0x1D	Bits[5:4]: DIE_TEMP_INT_ TYPE	Controls the triggering logic for a die temperature interrupt. 0x0: Interrupt generated on input status signal high 0x1: Interrupt generated on the rising edge of the input status signal 0x2: Interrupt generated on the falling edge of the input status signal 0x3: Interrupt generated on the rising and falling edges of the input status signal	R/W	0x0	N/A

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INT_TYPE2: 0x1D	Bits[7:6]: PCB_MNTR_ TEMP_INT_ TYPE	Controls the triggering logic for an NTC hot PCB monitor interrupt. 0x0: Interrupt generated on input status signal high 0x1: Interrupt generated on the rising edge of the input status signal 0x2: Interrupt generated on the falling edge of the input status signal 0x3: Interrupt generated on the rising and falling edges of the input status signal	R/W	0x0	N/A
INT_TYPE2: 0x1D	Bits[11:10]: SELF_TEST_ INT_TYPE	Controls the triggering logic for a self-diagnostic interrupt. 0x0: Interrupt generated on input status signal high 0x1: Interrupt generated on the rising edge of the input status signal 0x2: Interrupt generated on the falling edge of the input status signal 0x3: Interrupt generated on the rising and falling edges of the input status signal	R/W	0x0	N/A
MASK_INT0: 0x1E	Bit[0]: CELL_OV_ MASK	Enables clearing the cell OV interrupt flag and pulls the interrupt pin low, unless there are other interrupts pending. When disabled, the interrupt process can set the interrupt flag again.	R/W	0x0	0: Disabled 1: Enabled
MASK_INT0: 0x1E	Bit[1]: CELL_UV_ MASK	Enables clearing the cell UV interrupt flag and pulls the interrupt pin low, unless there are other interrupts pending. When disabled, the interrupt process can set the interrupt flag again.	R/W	0x0	0: Disabled 1: Enabled
MASK_INT0: 0x1E	Bit[2]: VTOP_UV_ MASK	Enables clearing the VTOP UV interrupt flag and pulls the interrupt pin low, unless there are other interrupts pending. When disabled, the interrupt process can set the interrupt flag again.	R/W	0x0	0: Disabled 1: Enabled
MASK_INT0: 0x1E	Bit[3]: VTOP_OV_ MASK	Enables clearing the VTOP OV interrupt flag and pulls the interrupt pin low, unless there are other interrupts pending. When disabled, the interrupt process can set the interrupt flag again.	R/W	0x0	0: Disabled 1: Enabled
MASK_INT0: 0x1E	Bit[4]: OVER_CURR_ MASK	Enables clearing the OC interrupt flag and pulls the interrupt pin low, unless there are other interrupts pending. When disabled, the interrupt process can set the interrupt flag again.	R/W	0x0	0: Disabled 1: Enabled

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MASK_INT0: 0x1E	Bit[5]: SC_MASK	Enables clearing the short-circuit interrupt flag and pulls the interrupt pin low, unless there are other interrupts pending. When disabled, the interrupt process can set the interrupt flag again.	R/W	0x0	0: Disabled 1: Enabled
MASK_INT0: 0x1E	Bit[6]: NTCS_CELL_ COLD_MASK	Enables clearing the NTC cold cell interrupt flag and pulls the interrupt pin low, unless there are other interrupts pending. When disabled, the interrupt process can set the interrupt flag again.	R/W	0x0	0: Disabled 1: Enabled
MASK_INT0: 0x1E	Bit[7]: NTCS_CELL_ HOT_MASK	Enables clearing the NTC hot cell interrupt flag and pulls the interrupt pin low, unless there are other interrupts pending. When disabled, the interrupt process can set the interrupt flag again.	R/W	0x0	0: Disabled 1: Enabled
MASK_INT1: 0x1F	Bit[0]: SELF_TEST_ MASK	Enables clearing the self-test interrupt flag and pulls the interrupt pin low, unless there are other interrupts pending. When disabled, the interrupt process can set the interrupt flag again.	R/W	0x0	0: Disabled 1: Enabled
MASK_INT1: 0x1F	Bit[1]: REGIN_MASK	Enables clearing the REGIN interrupt flag and pulls the interrupt pin low, unless there are other interrupts pending. When disabled, the interrupt process can set the interrupt flag again.	R/W	0x0	0: Disabled 1: Enabled
MASK_INT1: 0x1F	Bit[2]: 3V3_MASK	Enables clearing the 3V3 interrupt flag and pulls the interrupt pin low, unless there are other interrupts pending. When disabled, the interrupt process can set the interrupt flag again.	R/W	0x0	0: Disabled 1: Enabled
MASK_INT1: 0x1F	Bit[3]: VDD_MASK	Enables clearing the VDD interrupt flag and pulls the interrupt pin low, unless there are other interrupts pending. When disabled, the interrupt process can set the interrupt flag again.	R/W	0x0	0: Disabled 1: Enabled
MASK_INT1: 0x1F	Bit[6]: CELL_MSMT_ MASK	Enables clearing the mismatched cell interrupt flag and pulls the interrupt pin low, unless there are other interrupts pending. When disabled, the interrupt process can set the interrupt flag again.	R/W	0x0	0: Disabled 1: Enabled
MASK_INT1: 0x1F	Bit[7]: DIE_TEMP_ DIG_MASK	Enables clearing the die temperature interrupt flag and pulls the interrupt pin low, unless there are other interrupts pending. When disabled, the interrupt process can set the interrupt flag again.	R/W	0x0	0: Disabled 1: Enabled

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MASK_INT1: 0x1F	Bit[8]: PCB_MNTR_ HOT_MASK	Enables clearing the NTC hot PCB monitor interrupt flag and pulls the interrupt pin low, unless there are other interrupts pending. When disabled, the interrupt process can set the interrupt flag again.	R/W	0x0	0: Disabled 1: Enabled

Over-Current

Address Name and Location	Field Bit Position and Name	Description	Type	Value Reset (OTP/MTP)	Encoding, LSB and Range
OC_STATUS: 0x20	Bit[0]: OC1_DCHG_ STS	Indicates the latched discharge over-current (OC) limit 1 interrupt status. 1: Interrupt detected 0: No interrupt detected The latched value depends on the selected interrupt type (e.g. rising, falling, or rising and falling). For a rising edge type, the bit is set to 1 if a rising edge is detected. For a falling edge type, the bit is set to 1 if a falling edge is detected. For a rising and falling edge type, the bit is set to 1 if either edge is detected. For a level, the bit is set to 1 if the source signal is high. The type is defined by OC_DCHG_INT_TYPE, with the type selection being common for both limit 1 and limit 2 interrupts. This status bit can be cleared with OVER_CURR_INT_CLEAR.	Read-only	0x0	0: Not detected 1: Detected
OC_STATUS: 0x20	Bit[1]: OC2_DCHG_ STS	Indicates the latched discharge OC limit 2 interrupt status. 1: Interrupt detected 0: No interrupt detected The latched value depends on the selected interrupt type (e.g. rising, falling, or rising and falling). For a rising edge type, the bit is set to 1 if a rising edge is detected. For a falling edge type, the bit is set to 1 if a falling edge is detected. For a rising and falling edge type, the bit is set to 1 if either edge is detected. For a level, the bit is set to 1 if the source signal is high. The type is defined by OC_DCHG_INT_TYPE, with the type selection being common for both limit 1 and limit 2 interrupts. This status bit can be cleared with OVER_CURR_INT_CLEAR.	Read-only	0x0	0: Not detected 1: Detected

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OC_STATUS: 0x20	Bit[2]: OC_CHG_STS	Indicates the latched charge OC limit interrupt status. 1: Interrupt detected 0: No interrupt detected The latched value depends on the selected interrupt type (e.g. rising, falling, or rising and falling). For a rising edge type, the bit is set to 1 if a rising edge is detected. For a falling edge type, the bit is set to 1 if a falling edge is detected. For a rising and falling edge type, the bit is set to 1 if either edge is detected. For a level, the bit is set to 1 if the source signal is high. The type is defined by OC_CHG_INT_TYPE. This status bit can be cleared with OVER_CURR_INT_CLEAR.	Read-only	0x0	0: Not detected 1: Detected
OC_STATUS: 0x20	Bit[8]: OC1_DCHG_ RT_STS	Reports in real time whether a discharge OC limit 1 is detected.	Read-only	0x0	0: Not detected 1: Detected
OC_STATUS: 0x20	Bit[9]: OC2_DCHG_ RT_STS	Reports in real time whether a discharge OC limit 2 is detected.	Read-only	0x0	0: Not detected 1: Detected
OC_STATUS: 0x20	Bit[10]: OC_CHG_RT_ STS	Reports in real time whether a charge OC limit is detected.	Read-only	0x0	0: Not detected 1: Detected
OCFT_CTRL: 0x23	Bit[0]: OC1_DCHG_ EN_CTRL	Enables discharge OC limit 1 monitoring. When disabled, a discharge OC limit 1 event does not trigger a fault or interrupt, regardless of whether the fault and interrupt bits are enabled.	R/W (can lock to read-only)	0x1 (MTP)	0: Disabled 1: Enabled
OCFT_CTRL: 0x23	Bit[1]: OC2_DCHG_ EN_CTRL	Enables discharge OC limit 2 monitoring. When disabled, a discharge OC limit 2 event does not trigger a fault or interrupt, regardless of whether the fault and interrupt bits are enabled.	R/W (can lock to read-only)	0x1 (MTP)	0: Disabled 1: Enabled
OCFT_CTRL: 0x23	Bit[2]: OC_CHG_EN_ CTRL	Enables charge OC limit monitoring. When disabled, a charge OC limit event does not trigger a fault or interrupt, regardless of whether the fault and interrupt bits are enabled.	R/W (can lock to read-only)	0x1 (MTP)	0: Disabled 1: Enabled
OCFT_CTRL: 0x23	Bit[3]: OC1_DCHG_ INT_EN	Enables bit-level control for a discharge OC 1 interrupt. OVER_CURR_INT_EN must be enabled for this bit to be effective.	R/W	0x0	0: Disabled 1: Enabled
OCFT_CTRL: 0x23	Bit[4]: OC2_DCHG_ INT_EN	Enables bit-level control for a discharge OC 2 interrupt. OVER_CURR_INT_EN must be enabled for this bit to be effective.	R/W	0x0	0: Disabled 1: Enabled
OCFT_CTRL: 0x23	Bit[5]: OC_CHG_INT_ EN	Enables bit-level control for a charge OC interrupt. OVER_CURR_INT_EN must be enabled for this bit to be effective.	R/W	0x0	0: Disabled 1: Enabled

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OCFT_CTRL: 0x23	Bit[6]: OC1_DCHG_ FAULT_EN	Enables a discharge OC 1 event to put the MP2796 in fault mode. When enabled, this OC event puts the AFE in a fault state.	R/W (can lock to read-only)	0x1 (OTP)	0: Disabled 1: Enabled
OCFT_CTRL: 0x23	Bit[7]: OC2_DCHG_ FAULT_EN	Enables a discharge OC 2 event to put the MP2796 in fault mode. When enabled, this OC event puts the AFE in a fault state.	R/W (can lock to read-only)	0x1 (OTP)	0: Disabled 1: Enabled
OCFT_CTRL: 0x23	Bit[8]: OC_CHG_ FAULT_EN	Enables a charge OC event to put the MP2796 in fault mode. When enabled, this OC event puts the AFE in a fault state.	R/W (can lock to read-only)	0x1 (OTP)	0: Disabled 1: Enabled
OCFT_CTRL: 0x23	Bits[13:12]: OC_DCHG_INT_ TYPE	Controls the triggering logic for discharge OC interrupt. 0x0: Interrupt generated on input status signal high 0x1: Interrupt generated on the rising edge of the input status signal 0x2: Interrupt generated on the falling edge of the input status signal 0x3: Interrupt generated on the rising and falling edges of the input status signal	R/W	0x0	N/A
OCFT_CTRL: 0x23	Bits[15:14]: OC_CHG_INT_ TYPE	Controls the triggering logic for charge OC interrupt. 0x0: Interrupt generated on input status signal high 0x1: Interrupt generated on the rising edge of the input status signal 0x2: Interrupt generated on the falling edge of the input status signal 0x3: Interrupt generated on the rising and falling edges of the input status signal	R/W	0x0	N/A
DSGOC_LIM: 0x24	Bits[4:0]: OC1_DCHG_LIM	Configures the discharge OC 1 threshold. With a 1x range (OC1_DCHG_RNG = 0), the smallest available code is 2.5mV. With a 3x range (OC1_DCHG_RNG = 1), the minimum code is 7.5mV. The limit has an offset equal to the LSB, so 0x00 = 2.5mV with a 1x range and 0x00 = 7.5mV with a 3x range. The full-scale range depends on OC1_DCHG_RNG (80mV for 1x, 240mV for 3x).	R/W (can lock to read-only)	0x10 (MTP)	N/A
DSGOC_LIM: 0x24	Bit[5]: OC1_DCHG_ RNG	Selects the range and LSB for the discharge OC level 1 threshold.	R/W (can lock to read-only)	0x0 (MTP)	0: 2.5mV/LSB, 80mV FSR 1: 7.5mV/LSB, 240mV FSR

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DSGOC_LIM: 0x24	Bits[12:8]: OC2_DCHG_ LIM	Configures the discharge OC 2 threshold. With a 1x range (OC2_DCHG_RNG = 0), the smallest available code is 2.5mV. With a 3x range (OC2_DCHG_RNG = 1), the minimum code is 7.5mV. The limit has an offset equal to the LSB, so 0x00 = 2.5mV with a 1x range and 0x00 = 7.5mV with a 3x range. The full-scale range depends on OC2_DCHG_RNG (80mV for 1x, 240mV for 3x).	R/W (can lock to read-only)	0x09 (MTP)	N/A
DSGOC_LIM: 0x24	Bit[13]: OC2_DCHG_ RNG	Selects the range and LSB for the discharge OC level 2 threshold.	R/W (can lock to read-only)	0x1 (MTP)	0: 2.5mV/LSB, 80mV FSR 1: 7.5mV/LSB, 240mV FSR
DSGOC_DEG: 0x25	Bits[5:0]: OC1_DCHG_ DGL	Sets the discharge OC 1 deglitch value. When OC1_DCHG_DGL_RNG = 0, the code LSB is 5ms. When OC1_DCHG_DGL_RNG = 1, the code LSB is 40ms. When OC1_DCHG_DGL = 0x00 there is no deglitch, regardless of the LSB. This means an OC event is flagged as soon as it is detected. The response time is about 100µs. The full-scale range depends on the OC1_DCHG_DGL_RNG setting (315ms or 2520ms).	R/W (can lock to read-only)	0x14 (MTP)	N/A
DSGOC_DEG: 0x25	Bit[6]: OC1_DCHG_ DGL_RNG	Sets the discharge OC 1 deglitch bit weight, and selects the range for OC1_DCHG_DGL. 0: 5ms LSB / 315ms FSR 1: 40ms LSB / 2520ms FSR	R/W (can lock to read-only)	0x0 (MTP)	N/A
DSGOC_DEG: 0x25	Bits[13:8]: OC2_DCHG_ DGL	Sets the discharge OC 2 deglitch value. When OC2_DCHG_DGL_RNG = 0, the code LSB is 5ms. When OC2_DCHG_DGL_RNG = 1, the code LSB is 40ms. When OC2_DCHG_DGL = 0x00 there is no deglitch, regardless of the LSB. This means an OC event is flagged as soon as it is detected. The response time is about 100µs. The full-scale range depends on the OC2_DCHG_DGL_RNG setting (315ms or 2520ms).	R/W (can lock to read-only)	0x04 (MTP)	N/A

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DSGOC_DEG: 0x25	Bit[14]: OC2_DCHG_DGL_RNG	Sets the discharge OC 2 deglitch bit weight, and selects the range for OC2_DCHG_DGL. 0x0: 5ms LSB / 315ms FSR 0x1: 40ms LSB / 2520ms FSR	R/W (can lock to read-only)	0x0 (MTP)	N/A
CHGOC_DEG: 0x26	Bits[4:0]: OC_CHG_LIM	Sets the charge OC threshold. With a 1x range (OC_CHG_RNG = 0), the smallest available code is 1.6mV. With a 3x range (OC_CHG_RNG = 1), the minimum code is 4.8mV. The limit has an offset equal to the LSB, so 0x00 = 1.6mV with a 1x range and 0x00 = 4.8mV with a 3x range. The full-scale range depends on OC_CHG_RNG as well (51.2mV for 1x and 153.6mV for 3x).	R/W (can lock to read-only)	0x10 (MTP)	N/A
CHGOC_DEG: 0x26	Bit[5]: OC_CHG_RNG	Selects the range and LSB selector for the charge OC threshold (OC_CHG_LIM).	R/W (can lock to read-only)	0x0 (MTP)	0: 1.6mV/LSB, 51.2mV FSR 1: 4.8mV/LSB, 153.6mV FSR
CHGOC_DEG: 0x26	Bits[13:8]: OC_CHG_DG	Sets the OC charge deglitch value. When OC_CHG_DGL_RNG = 0x0, the code LSB is 5ms. When OC_CHG_DGL_RNG = 0x1, the code LSB is 40ms. When OC_CHG_DG = 0x00, there is no deglitch, regardless of the LSB. This means an OC event is flagged as soon as it is detected. The response time is about 100µs. The full-scale range depends on the OC_CHG_DGL_RNG setting (315ms or 2520ms).	R/W (can lock to read-only)	0x04 (MTP)	N/A
CHGOC_DEG: 0x26	Bit[14]: OC_CHG_DGL_RNG	Sets the charge OC deglitch bit weight, and selects the range for OC_CHG_DG. 0x0: 5ms LSB / 315ms FSR 0x1: 40ms LSB / 2520ms FSR	R/W (can lock to read-only)	0x0 (MTP)	N/A

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Short-Circuit

Address Name and Location	Field Bit Position and Name	Description	Type	Value Reset (OTP/MTP)	Encoding, LSB and Range
SC_STATUS: 0x27	Bit[0]: SC_DCHG_STS	Reports whether a latched discharge short-circuit event has been detected. The latched value depends on the selected interrupt type (e.g. rising, falling, or rising and falling) selected by SC_DCHG_INT_TYPE. For a rising edge type, the bit is set to 1 if a rising edge is detected. For a falling edge type, the bit is set to 1 if a falling edge is detected. For a rising and falling edge type, the bit is set to 1 if either edge is detected. For a level, the bit is set to 1 if the source signal is high. This status bit can be cleared with SHORT_CURR_INT_CLEAR.	Read-only	0x0	0: Not detected 1: Detected
SC_STATUS: 0x27	Bit[1]: SC_CHG_STS	Reports whether a latched charge short-circuit event has been detected. The latched value depends on the selected interrupt type (e.g. rising, falling, or rising and falling) selected by SC_CHG_INT_TYPE. For a rising edge type, the bit is set to 1 if a rising edge is detected. For a falling edge type, the bit is set to 1 if a falling edge is detected. For a rising and falling edge type, the bit is set to 1 if either edge is detected. For a level, the bit is set to 1 if the source signal is high. This status bit can be cleared with SHORT_CURR_INT_CLEAR.	Read-only	0x0	0: Not detected 1: Detected
SC_STATUS: 0x27	Bit[8]: SC_DCHG_RT_STS	Reports whether a discharge short-circuit event has been detected in real time.	Read-only	0x0	0: Not detected 1: Detected
SC_STATUS: 0x27	Bit[9]: SC_CHG_RT_STS	Reports whether a charge short-circuit event has been detected in real time.	Read-only	0x0	0: Not detected 1: Detected
SCFT_CTRL: 0x2A	Bit[0]: SC_DCHG_EN_CTRL	Enables discharge short-circuit monitoring. When disabled, this fault does not trigger an interrupt or a fault, regardless of whether those bits are enabled.	R/W (can lock to read-only)	0x1 (MTP)	0: Disabled 1: Enabled
SCFT_CTRL: 0x2A	Bit[1]: SC_CHG_EN_CTRL	Enables charge short-circuit monitoring. When disabled, this fault does not trigger an interrupt or a fault, regardless of whether those bits are enabled.	R/W (can lock to read-only)	0x1 (MTP)	0: Disabled 1: Enabled

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SCFT_CTRL: 0x2A	Bit[2]: SC_DCHG_INT_EN	Enables the interrupt for a discharge short-circuit current. For this bit to be effective, SC_DCHG_EN_CTRL must be enabled.	R/W	0x0	0: Disabled 1: Enabled
SCFT_CTRL: 0x2A	Bit[3]: SC_CHG_INT_EN	Enables the interrupt for a charge short-circuit current. For this bit to be effective, SC_CHG_EN_CTRL must be enabled.	R/W	0x0	0: Disabled 1: Enabled
SCFT_CTRL: 0x2A	Bit[4]: SC_DCHG_FAULT_EN	Enables a discharge short-circuit event to force the MP2796 into fault mode. For this bit to be effective, SC_DCHG_EN_CTRL must be enabled.	R/W (can lock to read-only)	0x1 (OTP)	0: Disabled 1: Enabled
SCFT_CTRL: 0x2A	Bit[5]: SC_CHG_FAULT_EN	Enables a charge short-circuit event to force the MP2796 into fault mode. For this bit to be effective, SC_CHG_EN_CTRL must be enabled.	R/W (can lock to read-only)	0x1 (OTP)	0: Disabled 1: Enabled
SCFT_CTRL: 0x2A	Bits[13:12]: SC_DCHG_INT_TYPE	Controls the triggering logic for discharge short-circuit interrupt. 0x0: Interrupt generated on input status signal high 0x1: Interrupt generated on the rising edge of the input status signal 0x2: Interrupt generated on the falling edge of the input status signal 0x3: Interrupt generated on the rising and falling edges of the input status signal	R/W	0x0	N/A
SCFT_CTRL: 0x2A	Bits[15:14]: SC_CHG_INT_TYPE	Controls the triggering logic for charge short-circuit interrupt. 0x0: Interrupt generated on input status signal high 0x1: Interrupt generated on the rising edge of the input status signal 0x2: Interrupt generated on the falling edge of the input status signal 0x3: Interrupt generated on the rising and falling edges of the input status signal	R/W	0x0	N/A
DSGSC_CFG: 0x2B	Bits[4:0]: SC_DCHG_LIM	Configures the short-circuit discharge threshold. With a 1x range (SC_DCHG_RNG = 0), the smallest available code is 5.5mV. With a 3x range (SC_DCHG_RNG = 1), the minimum code is 16.5mV. This threshold has an offset equal to the LSB, so 0x00 = 5.5mV with a 1x range and 0x00 = 16.5mV with a 3x range. The full-scale range depends on the SC_DCHG_RNG (176mV for 1x and 528mV for 3x).	R/W (can lock to read-only)	0x11 (MTP)	N/A

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DSGSC_CFG: 0x2B	Bit[5]: SC_DCHG_RNG	Selects the range and LSB for the discharge short-circuit threshold (SC_DCHG_LIM).	R/W (can lock to read-only)	0x0 (MTP)	0: 5.5mV/LSB, 176mV FSR 1: 16.5mV/LSB, 528mV FSR
DSGSC_CFG: 0x2B	Bits[14:8]: SC_DCHG_DG	Configures the discharge short-circuit deglitch time. When SC_DCHG_DG = 0x00, there is no deglitch, so a short-circuit event is flagged as soon as it is detected. The response time is about 100µs.	R/W (can lock to read-only)	0x01 (MTP)	LSB: 200µs, RNG:100µs to 25500µs, 0x00: 100µs
CHGSC_CFG: 0x2C	Bits[4:0]: SC_CHG_LIM	Configures the charge short-circuit threshold. With a 1x range (SC_CHG_RNG = 0), the smallest available code is 2.5mV. With a 3x range (SC_CHG_RNG = 1), the minimum code is 7.5mV. The limit has an offset equal to the LSB, so 0x00 = 2.5mV with a 1x range and 0x00 = 7.5mV with a 3x range. The full-scale range depends on the SC_CHG_RNG (80mV for 1x and 240mV for 3x).	R/W (can lock to read-only)	0x11 (MTP)	N/A
CHGSC_CFG: 0x2C	Bit[5]: SC_CHG_RNG	Selects the range and LSB for the charge short-circuit threshold (SC_CHG_LIM).	R/W (can lock to read-only)	0x0 (MTP)	0: 2.5mV/LSB, 80mV FSR 1: 7.5mV/LSB, 240mV FSR
CHGSC_CFG: 0x2C	Bits[14:8]: SC_CHG_DG	Configures the charge short-circuit deglitch time. When SC_CHG_DG = 0x00, there is no deglitch, so a short-circuit event is flagged as soon as it is detected. The response time is about 100µs.	R/W (can lock to read-only)	0x08 (MTP)	LSB: 200µs, RNG: 100µs to 25500µs, 0x00:100µs

Over-Voltage (OV), Under-Voltage (UV), Dead Cell, and Mismatched Cell

Address Name and Location	Field Bit Position and Name	Description	Type	Value Reset (OTP/MTP)	Encoding, LSB and Range
RD_CELL_UV: 0x2D	Bit[0]: CELL_1_UV_ STS	Reports whether an under-voltage (UV) condition has been detected on cell 1. Send an interrupt UV clear to clear this bit. 0: No UV event has been detected 1: A UV event has been detected	Read-only	0x0	0: Not detected 1: Detected
RD_CELL_UV: 0x2D	Bit[1]: CELL_2_UV_ STS	Reports whether a UV condition has been detected on cell 2. Send an interrupt UV clear to clear this bit. 0: No UV event has been detected 1: A UV event has been detected	Read-only	0x0	0: Not detected 1: Detected

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RD_CELL_UV: 0x2D	Bit[2]: CELL_3_UV_ STS	Reports whether a UV condition has been detected on cell 3. Send an interrupt UV clear to clear this bit. 0: No UV event has been detected 1: A UV event has been detected	Read-only	0x0	0: Not detected 1: Detected
RD_CELL_UV: 0x2D	Bit[3]: CELL_4_UV_ STS	Reports whether a UV condition has been detected on cell 4. Send an interrupt UV clear to clear this bit. 0: No UV event has been detected 1: A UV event has been detected	Read-only	0x0	0: Not detected 1: Detected
RD_CELL_UV: 0x2D	Bit[4]: CELL_5_UV_ STS	Reports whether a UV condition has been detected on cell 5. Send an interrupt UV clear to clear this bit. 0: No UV event has been detected 1: A UV event has been detected	Read-only	0x0	0: Not detected 1: Detected
RD_CELL_UV: 0x2D	Bit[5]: CELL_6_UV_ STS	Reports whether a UV condition has been detected on cell 6. Send an interrupt UV clear to clear this bit. 0: No UV event has been detected 1: A UV event has been detected	Read-only	0x0	0: Not detected 1: Detected
RD_CELL_UV: 0x2D	Bit[6]: CELL_7_UV_ STS	Reports whether a UV condition has been detected on cell 7. Send an interrupt UV clear to clear this bit. 0: No UV event has been detected 1: A UV event has been detected	Read-only	0x0	0: Not detected 1: Detected
RD_CELL_UV: 0x2D	Bit[7]: CELL_8_UV_ STS	Reports whether a UV condition has been detected on cell 8. Send an interrupt UV clear to clear this bit. 0: No UV event has been detected 1: A UV event has been detected	Read-only	0x0	0: Not detected 1: Detected
RD_CELL_UV: 0x2D	Bit[8]: CELL_9_UV_ STS	Reports whether a UV condition has been detected on cell 9. Send an interrupt UV clear to clear this bit. 0: No UV event has been detected 1: A UV event has been detected	Read-only	0x0	0: Not detected 1: Detected
RD_CELL_UV: 0x2D	Bit[9]: CELL_10_UV_ STS	Reports whether a UV condition has been detected on cell 10. Send an interrupt UV clear to clear this bit. 0: No UV event has been detected 1: A UV event has been detected	Read-only	0x0	0: Not detected 1: Detected
RD_CELL_UV: 0x2D	Bit[10]: CELL_11_UV_ STS	Reports whether a UV condition has been detected on cell 11. Send an interrupt UV clear to clear this bit. 0: No UV event has been detected 1: A UV event has been detected	Read-only	0x0	0: Not detected 1: Detected
RD_CELL_UV: 0x2D	Bit[11]: CELL_12_UV_ STS	Reports whether a UV condition has been detected on cell 12. Send an interrupt UV clear to clear this bit. 0: No UV event has been detected 1: A UV event has been detected	Read-only	0x0	0: Not detected 1: Detected

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RD_CELL_UV: 0x2D	Bit[12]: CELL_13_UV_ STS	Reports whether a UV condition has been detected on cell 13. Send an interrupt UV clear to clear this bit. 0: No UV event has been detected 1: A UV event has been detected	Read-only	0x0	0: Not detected 1: Detected
RD_CELL_UV: 0x2D	Bit[13]: CELL_14_UV_ STS	Reports whether a UV condition has been detected on cell 14. Send an interrupt UV clear to clear this bit. 0: No UV event has been detected 1: A UV event has been detected	Read-only	0x0	0: Not detected 1: Detected
RD_CELL_UV: 0x2D	Bit[14]: CELL_15_UV_ STS	Reports whether a UV condition has been detected on cell 15. Send an interrupt UV clear to clear this bit. 0: No UV event has been detected 1: A UV event has been detected	Read-only	0x0	0: Not detected 1: Detected
RD_CELL_UV: 0x2D	Bit[15]: CELL_16_UV_ STS	Reports whether a UV condition has been detected on cell 16. Send an interrupt UV clear to clear this bit. 0: No UV event has been detected 1: A UV event has been detected	Read-only	0x0	0: Not detected 1: Detected
RD_CELL_OV: 0x2E	Bit[0]: CELL_1_OV_ STS	Reports whether an over-voltage (OV) condition has been detected on cell 1. Send an interrupt OV clear to clear this bit. 0: No OV event has been detected 1: An OV event has been detected	Read-only	0x0	0: Not detected 1: Detected
RD_CELL_OV: 0x2E	Bit[1]: CELL_2_OV_ STS	Reports whether an OV condition has been detected on cell 2. Send an interrupt OV clear to clear this bit. 0: No OV event has been detected 1: An OV event has been detected	Read-only	0x0	0: Not detected 1: Detected
RD_CELL_OV: 0x2E	Bit[2]: CELL_3_OV_ STS	Reports whether an OV condition has been detected on cell 3. Send an interrupt OV clear to clear this bit. 0: No OV event has been detected 1: An OV event has been detected	Read-only	0x0	0: Not detected 1: Detected
RD_CELL_OV: 0x2E	Bit[3]: CELL_4_OV_ STS	Reports whether an OV condition has been detected on cell 4. Send an interrupt OV clear to clear this bit. 0: No OV event has been detected 1: An OV event has been detected	Read-only	0x0	0: Not detected 1: Detected
RD_CELL_OV: 0x2E	Bit[4]: CELL_5_OV_ STS	Reports whether an OV condition has been detected on cell 5. Send an interrupt OV clear to clear this bit. 0: No OV event has been detected 1: An OV event has been detected	Read-only	0x0	0: Not detected 1: Detected
RD_CELL_OV: 0x2E	Bit[5]: CELL_6_OV_ STS	Reports whether an OV condition has been detected on cell 6. Send an interrupt OV clear to clear this bit. 0: No OV event has been detected 1: An OV event has been detected	Read-only	0x0	0: Not detected 1: Detected

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RD_CELL_OV: 0x2E	Bit[6]: CELL_7_OV_ STS	Reports whether an OV condition has been detected on cell 7. Send an interrupt OV clear to clear this bit. 0: No OV event has been detected 1: An OV event has been detected	Read-only	0x0	0: Not detected 1: Detected
RD_CELL_OV: 0x2E	Bit[7]: CELL_8_OV_ STS	Reports whether an OV condition has been detected on cell 8. Send an interrupt OV clear to clear this bit. 0: No OV event has been detected 1: An OV event has been detected	Read-only	0x0	0: Not detected 1: Detected
RD_CELL_OV: 0x2E	Bit[8]: CELL_9_OV_ STS	Reports whether an OV condition has been detected on cell 9. Send an interrupt OV clear to clear this bit. 0: No OV event has been detected 1: An OV event has been detected	Read-only	0x0	0: Not detected 1: Detected
RD_CELL_OV: 0x2E	Bit[9]: CELL_10_OV_ STS	Reports whether an OV condition has been detected on cell 10. Send an interrupt OV clear to clear this bit. 0: No OV event has been detected 1: An OV event has been detected	Read-only	0x0	0: Not detected 1: Detected
RD_CELL_OV: 0x2E	Bit[10]: CELL_11_OV_ STS	Reports whether an OV condition has been detected on cell 11. Send an interrupt OV clear to clear this bit. 0: No OV event has been detected 1: An OV event has been detected	Read-only	0x0	0: Not detected 1: Detected
RD_CELL_OV: 0x2E	Bit[11]: CELL_12_OV_ STS	Reports whether an OV condition has been detected on cell 12. Send an interrupt OV clear to clear this bit. 0: No OV event has been detected 1: An OV event has been detected	Read-only	0x0	0: Not detected 1: Detected
RD_CELL_OV: 0x2E	Bit[12]: CELL_13_OV_ STS	Reports whether an OV condition has been detected on cell 13. Send an interrupt OV clear to clear this bit. 0: No OV event has been detected 1: An OV event has been detected	Read-only	0x0	0: Not detected 1: Detected
RD_CELL_OV: 0x2E	Bit[13]: CELL_14_OV_ STS	Reports whether an OV condition has been detected on cell 14. Send an interrupt OV clear to clear this bit. 0: No OV event has been detected 1: An OV event has been detected	Read-only	0x0	0: Not detected 1: Detected
RD_CELL_OV: 0x2E	Bit[14]: CELL_15_OV_ STS	Reports whether an OV condition has been detected on cell 15. Send an interrupt OV clear to clear this bit. 0: No OV event has been detected 1: An OV event has been detected	Read-only	0x0	0: Not detected 1: Detected
RD_CELL_OV: 0x2E	Bit[15]: CELL_16_OV_ STS	Reports whether an OV condition has been detected on cell 16. Send an interrupt OV clear to clear this bit. 0: No OV event has been detected 1: An OV event has been detected	Read-only	0x0	0: Not detected 1: Detected

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RD_CELL_ MSMT: 0x2F	Bit[0]: CELL_1_MSMT_ STS	Reports the cell 1 mismatch interrupt status. Clear a mismatch with CELL_MISMATCH_INT_CLEAR. 0: No mismatch 1: A mismatch has been detected	Read-only	0x0	0: False 1: True
RD_CELL_ MSMT: 0x2F	Bit[1]: CELL_2_MSMT_ STS	Reports the cell 2 mismatch interrupt status. Clear a mismatch with CELL_MISMATCH_INT_CLEAR. 0: No mismatch 1: A mismatch has been detected	Read-only	0x0	0: False 1: True
RD_CELL_ MSMT: 0x2F	Bit[2]: CELL_3_MSMT_ STS	Reports the cell 3 mismatch interrupt status. Clear a mismatch with CELL_MISMATCH_INT_CLEAR. 0: No mismatch 1: A mismatch has been detected	Read-only	0x0	0: False 1: True
RD_CELL_ MSMT: 0x2F	Bit[3]: CELL_4_MSMT_ STS	Reports the cell 4 mismatch interrupt status. Clear a mismatch with CELL_MISMATCH_INT_CLEAR. 0: No mismatch 1: A mismatch has been detected	Read-only	0x0	0: False 1: True
RD_CELL_ MSMT: 0x2F	Bit[4]: CELL_5_MSMT_ STS	Reports the cell 5 mismatch interrupt status. Clear a mismatch with CELL_MISMATCH_INT_CLEAR. 0: No mismatch 1: A mismatch has been detected	Read-only	0x0	0: False 1: True
RD_CELL_ MSMT: 0x2F	Bit[5]: CELL_6_MSMT_ STS	Reports the cell 6 mismatch interrupt status. Clear a mismatch with CELL_MISMATCH_INT_CLEAR. 0: No mismatch 1: A mismatch has been detected	Read-only	0x0	0: False 1: True
RD_CELL_ MSMT: 0x2F	Bit[6]: CELL_7_MSMT_ STS	Reports the cell 7 mismatch interrupt status. Clear a mismatch with CELL_MISMATCH_INT_CLEAR. 0: No mismatch 1: A mismatch has been detected	Read-only	0x0	0: False 1: True
RD_CELL_ MSMT: 0x2F	Bit[7]: CELL_8_MSMT_ STS	Reports the cell 8 mismatch interrupt status. Clear a mismatch with CELL_MISMATCH_INT_CLEAR. 0: No mismatch 1: A mismatch has been detected	Read-only	0x0	0: False 1: True

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RD_CELL_ MSMT: 0x2F	Bit[8]: CELL_9_MSMT_ STS	Reports the cell 9 mismatch interrupt status. Clear a mismatch with CELL_MISMATCH_INT_CLEAR. 0: No mismatch 1: A mismatch has been detected	Read-only	0x0	0: False 1: True
RD_CELL_ MSMT: 0x2F	Bit[9]: CELL_10_ MSMT_STS	Reports the cell 10 mismatch interrupt status. Clear a mismatch with CELL_MISMATCH_INT_CLEAR. 0: No mismatch 1: A mismatch has been detected	Read-only	0x0	0: False 1: True
RD_CELL_ MSMT: 0x2F	Bit[10]: CELL_11_ MSMT_STS	Reports the cell 11 mismatch interrupt status. Clear a mismatch with CELL_MISMATCH_INT_CLEAR. 0: No mismatch 1: A mismatch has been detected	Read-only	0x0	0: False 1: True
RD_CELL_ MSMT: 0x2F	Bit[11]: CELL_12_ MSMT_STS	Reports the cell 12 mismatch interrupt status. Clear a mismatch with CELL_MISMATCH_INT_CLEAR. 0: No mismatch 1: A mismatch has been detected	Read-only	0x0	0: False 1: True
RD_CELL_ MSMT: 0x2F	Bit[12]: CELL_13_ MSMT_STS	Reports the cell 13 mismatch interrupt status. Clear a mismatch with CELL_MISMATCH_INT_CLEAR. 0: No mismatch 1: A mismatch has been detected	Read-only	0x0	0: False 1: True
RD_CELL_ MSMT: 0x2F	Bit[13]: CELL_14_ MSMT_STS	Reports the cell 14 mismatch interrupt status. Clear a mismatch with CELL_MISMATCH_INT_CLEAR. 0: No mismatch 1: A mismatch has been detected	Read-only	0x0	0: False 1: True
RD_CELL_ MSMT: 0x2F	Bit[14]: CELL_15_ MSMT_STS	Reports the cell 15 mismatch interrupt status. Clear a mismatch with CELL_MISMATCH_INT_CLEAR. 0: No mismatch 1: A mismatch has been detected	Read-only	0x0	0: False 1: True
RD_CELL_ MSMT: 0x2F	Bit[15]: CELL_16_ MSMT_STS	Reports the cell 16 mismatch interrupt status. Clear a mismatch with CELL_MISMATCH_INT_CLEAR. 0: No mismatch 1: A mismatch has been detected.	Read-only	0x0	0: False 1: True

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RD_CELL_ DEAD: 0x30	Bit[0]: CELL_1_DEAD_ STS	Reports cell 1's dead interrupt status. If CELL_DEAD_STS_SEL = 0, this bit indicates the interrupt status; if CELL_DEAD_STS_SEL = 1, this bit indicates the real-time status. 0: This cell is not dead 1: This cell is dead	Read-only	0x0	0: Not detected 1: Detected
RD_CELL_ DEAD: 0x30	Bit[1]: CELL_2_DEAD_ STS	Reports cell 2's dead interrupt status. If CELL_DEAD_STS_SEL = 0, this bit indicates the interrupt status; if CELL_DEAD_STS_SEL = 1, this bit indicates the real-time status. 0: This cell is not dead 1: This cell is dead	Read-only	0x0	0: Not detected 1: Detected
RD_CELL_ DEAD: 0x30	Bit[2]: CELL_3_DEAD_ STS	Reports cell 3's dead interrupt status. If CELL_DEAD_STS_SEL = 0, this bit indicates the interrupt status; if CELL_DEAD_STS_SEL = 1, this bit indicates the real-time status. 0: This cell is not dead 1: This cell is dead	Read-only	0x0	0: Not detected 1: Detected
RD_CELL_ DEAD: 0x30	Bit[3]: CELL_4_DEAD_ STS	Reports cell 4's dead interrupt status. If CELL_DEAD_STS_SEL = 0, this bit indicates the interrupt status; if CELL_DEAD_STS_SEL = 1, this bit indicates the real-time status. 0: This cell is not dead 1: This cell is dead	Read-only	0x0	0: Not detected 1: Detected
RD_CELL_ DEAD: 0x30	Bit[4]: CELL_5_DEAD_ STS	Reports cell 5's dead interrupt status. If CELL_DEAD_STS_SEL = 0, this bit indicates the interrupt status; if CELL_DEAD_STS_SEL = 1, this bit indicates the real-time status. 0: This cell is not dead 1: This cell is dead	Read-only	0x0	0: Not detected 1: Detected
RD_CELL_ DEAD: 0x30	Bit[5]: CELL_6_DEAD_ STS	Reports cell 6's dead interrupt status. If CELL_DEAD_STS_SEL = 0, this bit indicates the interrupt status; if CELL_DEAD_STS_SEL = 1, this bit indicates the real-time status. 0: This cell is not dead 1: This cell is dead	Read-only	0x0	0: Not detected 1: Detected

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RD_CELL_ DEAD: 0x30	Bit[6]: CELL_7_DEAD_ STS	Reports cell 7's dead interrupt status. If CELL_DEAD_STS_SEL = 0, this bit indicates the interrupt status; if CELL_DEAD_STS_SEL = 1, this bit indicates the real-time status. 0: This cell is not dead 1: This cell is dead	Read-only	0x0	0: Not detected 1: Detected
RD_CELL_ DEAD: 0x30	Bit[7]: CELL_8_DEAD_ STS	Reports cell 8's dead interrupt status. If CELL_DEAD_STS_SEL = 0, this bit indicates the interrupt status; if CELL_DEAD_STS_SEL = 1, this bit indicates the real-time status. 0: This cell is not dead 1: This cell is dead	Read-only	0x0	0: Not detected 1: Detected
RD_CELL_ DEAD: 0x30	Bit[8]: CELL_9_DEAD_ STS	Reports cell 9's dead interrupt status. If CELL_DEAD_STS_SEL = 0, this bit indicates the interrupt status; if CELL_DEAD_STS_SEL = 1, this bit indicates the real-time status. 0: This cell is not dead 1: This cell is dead	Read-only	0x0	0: Not detected 1: Detected
RD_CELL_ DEAD: 0x30	Bit[9]: CELL_10_ DEAD_STS	Reports cell 10's dead interrupt status. If CELL_DEAD_STS_SEL = 0, this bit indicates the interrupt status; if CELL_DEAD_STS_SEL = 1, this bit indicates the real-time status. 0: This cell is not dead 1: This cell is dead	Read-only	0x0	0: Not detected 1: Detected
RD_CELL_ DEAD: 0x30	Bit[10]: CELL_11_ DEAD_STS	Reports cell 11's dead interrupt status. If CELL_DEAD_STS_SEL = 0, this bit indicates the interrupt status; if CELL_DEAD_STS_SEL = 1, this bit indicates the real-time status. 0: This cell is not dead 1: This cell is dead	Read-only	0x0	0: Not detected 1: Detected
RD_CELL_ DEAD: 0x30	Bit[11]: CELL_12_ DEAD_STS	Reports cell 12's dead interrupt status. If CELL_DEAD_STS_SEL = 0, this bit indicates the interrupt status; if CELL_DEAD_STS_SEL = 1, this bit indicates the real-time status. 0: This cell is not dead 1: This cell is dead	Read-only	0x0	0: Not detected 1: Detected

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RD_CELL_ DEAD: 0x30	Bit[12]: CELL_13_ DEAD_STS	Reports cell 13's dead interrupt status. If CELL_DEAD_STS_SEL = 0, this bit indicates the interrupt status; if CELL_DEAD_STS_SEL = 1, this bit indicates the real-time status. 0: This cell is not dead 1: This cell is dead	Read-only	0x0	0: Not detected 1: Detected
RD_CELL_ DEAD: 0x30	Bit[13]: CELL_14_ DEAD_STS	Reports cell 14's dead interrupt status. If CELL_DEAD_STS_SEL = 0, this bit indicates the interrupt status; if CELL_DEAD_STS_SEL = 1, this bit indicates the real-time status. 0: This cell is not dead 1: This cell is dead	Read-only	0x0	0: Not detected 1: Detected
RD_CELL_ DEAD: 0x30	Bit[14]: CELL_15_ DEAD_STS	Reports cell 15's dead interrupt status. If CELL_DEAD_STS_SEL = 0, this bit indicates the interrupt status; if CELL_DEAD_STS_SEL = 1, this bit indicates the real-time status. 0: This cell is not dead 1: This cell is dead	Read-only	0x0	0: Not detected 1: Detected
RD_CELL_ DEAD: 0x30	Bit[15]: CELL_16_ DEAD_STS	Reports cell 16's dead interrupt status. If CELL_DEAD_STS_SEL = 0, this bit indicates the interrupt status; if CELL_DEAD_STS_SEL = 1, this bit indicates the real-time status. 0: This cell is not dead 1: This cell is dead	Read-only	0x0	0: Not detected 1: Detected
CELL_MSMT_ STS: 0x33	Bits[9:0]: CELL_MSMT_ DELTA	Reports the voltage difference between the cell with the lowest voltage and the cell with the highest voltage. If the interrupt is disabled, this bit indicates the real-time status; otherwise, this bit is latched at the interrupt and returns to the real-time status after being cleared.	Read-only	0x000	LSB: 4.88mV, RNG: 0mV to 4997.12mV, 0x000: 0mV
CELL_MSMT_ STS: 0x33	Bits[13:10]: CELL_MSMT_ LOWER	Reports the cell with the lowest voltage. If the interrupt is disabled, this bit indicates the real-time status; otherwise, this bit is latched at the interrupt and returns to the real-time status after being cleared. 0x0: Cell 1 … 0xF: Cell 16	Read-only	0x0	N/A
CELL_MSMT_ STS: 0x33	Bit[14]: CELL_MSMT_ RT_STS	Reports the real-time cell mismatch status. 0: There is no mismatch 1: A mismatch has been detected	Read-only	0x0	N/A

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PACKFT_ CTRL: 0x34	Bit[0]: VTOP_UV_EN_ CTRL	Enables the monitoring for battery pack (VTOP) under-voltage protection (UVP).	R/W	0x0 (OTP)	0: Disabled 1: Enabled
PACKFT_ CTRL: 0x34	Bit[1]: VTOP_UV_ FAULT_EN_ CTRL	Enables battery pack UVP to put the device in fault mode. 0: The device does not enter fault mode 1: The device enters fault mode	R/W (can lock to read-only)	0x0 (OTP)	0: Disabled 1: Enabled
PACKFT_ CTRL: 0x34	Bit[4]: VTOP_OV_EN_ CTRL	Enables the monitoring for battery pack (VTOP) over-voltage protection (OVP).	R/W	0x0 (OTP)	0: Disabled 1: Enabled
PACKFT_ CTRL: 0x34	Bit[5]: VTOP_OV_ FAULT_EN_ CTRL	Enables battery pack OVP to put the device in fault mode. 0: The device does not enter fault mode 1: The device enters fault mode	R/W (can lock to read-only)	0x0 (OTP)	0: Disabled 1: Enabled
PACKFT_ CTRL: 0x34	Bit[8]: CELL_DEAD_EN	Enables dead cell protection. This bit must be enabled to trigged dead cell faults or interrupts (which both have their own enable controls as well).	R/W (can lock to read-only)	0x0 (OTP)	0: Disabled 1: Enabled
PACKFT_ CTRL: 0x34	Bit[9]: CELL_DEAD_ FAULT_EN	0: A dead cell does not force the device into fault mode 1: A dead cell puts the device in fault mode	R/W (can lock to read-only)	0x0 (OTP)	0: Disabled 1: Enabled
PACKFT_ CTRL: 0x34	Bit[10]: CELL_DEAD_ STS_SEL	0: Show the latched dead cell status going to the interrupt controller 1: Show the real-time dead cell status	R/W	0x0	N/A
PACKFT_ CTRL: 0x34	Bit[11]: CELL_MSMT_ EN	0: Disable cell mismatch logic 1: Enable cell mismatch logic	R/W	0x0 (OTP)	0: Disabled 1: Enabled
PACKFT_ CTRL: 0x34	Bit[12]: CELL_MSMT_ FAULT_EN	0: A cell mismatch does not force the device into fault mode 1: A cell mismatch puts the device in fault mode	R/W (can lock to read-only)	0x0 (OTP)	0: Disabled 1: Enabled
PACKFT_ CTRL: 0x34	Bit[14]: CELL_DEAD_ LOG_STS	Reports whether a dead cell event has been detected. This status is not cleared by shutting down. It must be cleared with CELL_DEAD_DET_CLEAR.	Read-only	0x0	0: Not detected 1: Detected
PACKFT_ CTRL: 0x34	Bit[15]: CELL_DEAD_ DET_CLEAR	Set this bit to 1 to clear the dead cell status. This is a self-clearing bit.	Write-only	0x0	N/A
CELLFT_CTRL: 0x35	Bit[0]: SYNC_RT_ STATUS	When this bit is set to “on”, it synchronizes the status bit to allow the voltage ADC monitoring input status to be cleared after it has been disabled.	R/W	0x0	0: Off 1: On
CELLFT_CTRL: 0x35	Bit[1]: CELL_UV_EN_ CTRL	Enables cell UVP. This bit must be enabled for UV faults or interrupts to be triggered.	R/W (can lock to read-only)	0x0 (OTP)	0: Disabled 1: Enabled
CELLFT_CTRL: 0x35	Bit[2]: CELL_UV_ FAULT_EN	0: Cell UVP does not force the device into fault mode 1: Cell UVP puts the device in fault mode	R/W (can lock to read-only)	0x0 (OTP)	0: Disabled 1: Enabled

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CELLFT_CTRL: 0x35	Bit[4]: CELL_OV_EN_ CTRL	Enables cell OVP. This bit must be enabled for OV faults or interrupts to be triggered.	R/W (can lock to read-only)	0x0 (OTP)	0: Disabled 1: Enabled
CELLFT_CTRL: 0x35	Bit[5]: CELL_OV_ FAULT_EN	0: Cell OVP does not force the device into fault mode 1: Cell OVP puts the device in fault mode	R/W (can lock to read-only)	0x0 (OTP)	0: Disabled 1: Enabled
CELLFT_CTRL: 0x35	Bits[8:7]: CELL_UV_INT_ TYPE	Controls the triggering logic for cell UV interrupt. 0x0: Interrupt generated on input status signal high 0x1: Interrupt generated on the rising edge of the input status signal 0x2: Interrupt generated on the falling edge of the input status signal 0x3: Interrupt generated on the rising and falling edges of the input status signal	R/W	0x1	N/A
CELLFT_CTRL: 0x35	Bits[10:9]: CELL_OV_INT_ TYPE	Controls the triggering logic for cell OV interrupt. 0x0: Interrupt generated on input status signal high 0x1: Interrupt generated on the rising edge of the input status signal 0x2: Interrupt generated on the falling edge of the input status signal 0x3: Interrupt generated on the rising and falling edges of the input status signal	R/W	0x1	N/A
CELLFT_CTRL: 0x35	Bit[11]: CELL_UV_STS_ SEL	Selects what each of the CELL_x_UV_STS bits report. 0: Report the latched cell x status going to the interrupt controller 01: Report the latest outcome of the cell x UV check	R/W	0x0	N/A
CELLFT_CTRL: 0x35	Bit[12]: CELL_OV_STS_ SEL	Selects what each of the CELL_x_OV_STS bits report. 0: Report the latched cell x status going to the interrupt controller 1: Report the latest outcome of the cell x OV check	R/W	0x0	N/A
CELL_HYST: 0x36	Bits[7:4]: CELL_UV_HYST	Sets the cell UV threshold hysteresis.	R/W	0xA (OTP)	LSB: 19.5mV RNG: 0mV to 292.5mV 0: 0mV
CELL_HYST: 0x36	Bits[11:8]: CELL_OV_HYST	Sets the cell OV threshold hysteresis.	R/W	0xA (OTP)	LSB: 19.5mV RNG: 0mV to 292.5mV 0: 0mV

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PACK_UV_OV: 0x37	Bit[0]: VTOP_UV_RT_STS	Reports the real-time result of the VTOP vs. UV threshold comparison. Depending on the settings, a hysteresis may be applied to the threshold for comparison. 0: VTOP ≥ UV threshold 1: VTOP < UV threshold	Read-only	0x0	0: Not detected 1: Detected
PACK_UV_OV: 0x37	Bits[7:2]: VTOP_UV_HYST	Sets the battery pack UV threshold hysteresis.	R/W	0x20 (MTP)	LSB: 78.125mV RNG: 0mV to 4921.875mV 0x00: 0mV
PACK_UV_OV: 0x37	Bit[8]: VTOP_OV_RT_STS	Reports the real-time result of the VTOP vs. OV threshold comparison. Depending on the settings, a hysteresis may be applied to the threshold for comparison. 0: VTOP ≤ OV threshold 1: VTOP > OV threshold	Read-only	0x0	0: Not detected 1: Detected
PACK_UV_OV: 0x37	Bits[15:10]: VTOP_OV_HYST	Sets the battery pack OV threshold hysteresis.	R/W	0x20 (MTP)	LSB: 78.125mV RNG: 0mV to 4921.875mV 0x00: 0mV
CELL_UV: 0x38	Bits[7:0]: CELL_UV	Configures the cell UV threshold.	R/W (can lock to read-only)	0x98 (MTP)	LSB: 19.53mV RNG: 0mV to 4980.15mV 0x00: 0mV
CELL_UV: 0x38	Bits[11:8]: CELL_UV_DG	Sets the cell UV deglitch delay, which can be set between 1 reading (no deglitch) and 16 readings. 0x0: A UV condition is reported as soon as the UV threshold is reached 0x1: A UV condition is reported when the current and previous protection readings violate the cell UV threshold ... 0xF: A UV condition is reported when a total of 16 protection cycles violate the cell UV threshold	R/W (can lock to read-only)	0x0 (OTP)	LSB: 1 update RNG: 1 to 16 update(s) 0: 1 update
CELL_OV: 0x39	Bits[7:0]: CELL_OV	Configures the cell OV threshold.	R/W (can lock to read-only)	0xD7 (MTP)	LSB: 19.53mV RNG: 0mV to 4980.15mV 0x00: 0mV
CELL_OV: 0x39	Bits[11:8]: CELL_OV_DG	Sets the cell OV deglitch delay, which can be set between 1 reading (no deglitch) and 16 readings. 0x0: An OV condition is reported as soon as the OV threshold is reached 0x1: An OV condition is reported when the current and previous protection readings violate the cell OV threshold ... 0xF: An OV condition is reported when a total of 16 protection cycles violate the cell OV threshold	R/W (can lock to read-only)	0x0 (OTP)	LSB: 1 update RNG: 1 to 16 update(s) 0: 1 update

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PACK_UV: 0x3A	Bits[11:0]: VTOP_UV_LIMIT	Configures the battery pack UV threshold.	R/W	0x948 (MTP)	LSB: 19.531mV RNG: 0mV to 79979.5mV 0x000: 0mV
PACK_UV: 0x3A	Bits[15:12]: VTOP_UV_DG	Sets the VTOP UV deglitch delay, which can be set between 1 reading (no deglitch) and 16 readings. 0x0: A UV condition is reported as soon as the UV threshold is reached 0x1: A UV condition is reported when the current and previous protection readings violate the VTOP UV threshold ... 0xF: A UV condition is reported when a total of 16 protection cycles violate the VTOP UV threshold	R/W	0x0 (OTP)	LSB: 1 update RNG: 1 to 16 update(s) 0: 1 update
PACK_OV: 0x3B	Bits[11:0]: VTOP_OV_ LIMIT	Configures the battery pack OV threshold.	R/W	0xD71 (MTP)	LSB: 19.531mV RNG: 0mV to 79979.5mV, 0x000: 0mV
PACK_OV: 0x3B	Bits[15:12]: VTOP_OV_DG	Sets the VTOP OV deglitch delay, which can be set between 1 reading (no deglitch) and 16 readings. 0x0: An OV condition is reported as soon as the OV threshold is reached 0x1: An OV condition is reported when the current and previous protection readings violate the VTOP OV threshold ... 0xF: An OV condition is reported when a total of 16 protection cycles violate the VTOP OV threshold	R/W	0x0 (OTP)	LSB: 1 update RNG: 1 to 16 update(s) 0: 1 update
CELL_DEAD_ THR: 0x3C	Bits[6:0]: CELL_DEAD_ LIMIT	Configures the dead cell threshold.	R/W	0x68 (MTP)	LSB: 19.53mV RNG: 0mV to 2480.31mV 0x00: 0mV
CELL_DEAD_ THR: 0x3C	Bits[10:7]: CELL_DEAD_ DGL_N	Sets the dead cell deglitch delay, which can be set between 1 reading (no deglitch) and 16 readings. 0x0: A dead cell condition is reported as soon as the dead cell threshold is reached 0x1: A dead cell condition is reported when the current and previous protection readings violate the dead cell threshold ... 0xF: A dead cell condition is reported when a total of 16 protection cycles violate the dead cell threshold	R/W	0x0 (OTP)	LSB: 1 update RNG: 1 to 16 update(s) 0: 1 update

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CELL_MSMT: 0x3D	Bits[4:0]: MSMT_TH	Sets the mismatched cell threshold. The weight of each bit is below: Bit[4]: 625mV Bit[3]: 312.5mV Bit[2]: 156.25mV Bit[1]: 78.1mV Bit[0]: 39mV	R/W	0x02 (OTP)	N/A
CELL_MSMT: 0x3D	Bits[8:5]: CELL_MSMT_ DGL_N	Sets the mismatched cell deglitch delay, which can be set between 1 reading (no deglitch) and 16 readings. 0x0: A mismatched cell condition is reported as soon as the dead cell threshold is reached 0x1: A mismatched cell condition is reported when the current and previous protection readings violate the mismatched cell threshold ... 0xF: A mismatched cell condition is reported when a total of 16 protection cycles violate the mismatched cell threshold	R/W	0x0 (OTP)	LSB: 1 update RNG: 1 to 16 update(s) 0: 1 update

NTC Die Temperature

Address Name and Location	Field Bit Position and Name	Description	Type	Value Reset (OTP/MTP)	Encoding, LSB and Range
RD_NTC_DIE: 0x3E	Bit[0]: NTC1_CELL_ HOT_STS	Reports the NTC1 hot cell interrupt status. 0: No interrupt detected 1: An interrupt was detected The latched value depends on the selected interrupt type (e.g. rising, falling, or rising and falling). For a rising edge, the bit is set to 1 if a rising edge is detected. For a falling edge, the bit is set to 1 if a falling edge is detected. For a rising and falling edge, the bit is set to 1 if either edge is detected. For a level, the bit is set to 1 if the source signal is high.	Read-only	0x0	N/A

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RD_NTC_DIE: 0x3E	Bit[1]: NTC2_CELL_ HOT_STS	Reports the NTC2 hot cell interrupt status. 0: No interrupt detected 1: An interrupt was detected The latched value depends on the selected interrupt type (e.g. rising, falling, or rising and falling). For a rising edge, the bit is set to 1 if a rising edge is detected. For a falling edge, the bit is set to 1 if a falling edge is detected. For a rising and falling edge, the bit is set to 1 if either edge is detected. For a level, the bit is set to 1 if the source signal is high.	Read-only	0x0	N/A
RD_NTC_DIE: 0x3E	Bit[2]: NTC3_CELL_ HOT_STS	Reports the NTC3 hot cell interrupt status. 0: No interrupt detected 1: An interrupt was detected The latched value depends on the selected interrupt type (e.g. rising, falling, or rising and falling). For a rising edge, the bit is set to 1 if a rising edge is detected. For a falling edge, the bit is set to 1 if a falling edge is detected. For a rising and falling edge, the bit is set to 1 if either edge is detected. For a level, the bit is set to 1 if the source signal is high.	Read-only	0x0	N/A
RD_NTC_DIE: 0x3E	Bit[3]: NTC4_CELL_ HOT_STS	Reports the NTC4 hot cell interrupt status. 0: No interrupt detected 1: An interrupt was detected The latched value depends on the selected interrupt type (e.g. rising, falling, or rising and falling). For a rising edge, the bit is set to 1 if a rising edge is detected. For a falling edge, the bit is set to 1 if a falling edge is detected. For a rising and falling edge, the bit is set to 1 if either edge is detected. For a level, the bit is set to 1 if the source signal is high.	Read-only	0x0	N/A

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RD_NTC_DIE: 0x3E	Bit[4]: NTC1_CELL_ COLD_STS	Reports the NTC1 cold cell interrupt status. 0: No interrupt detected 1: An interrupt was detected The latched value depends on the selected interrupt type (e.g. rising, falling, or rising and falling). For a rising edge, the bit is set to 1 if a rising edge is detected. For a falling edge, the bit is set to 1 if a falling edge is detected. For a rising and falling edge, the bit is set to 1 if either edge is detected. For a level, the bit is set to 1 if the source signal is high.	Read-only	0x0	N/A
RD_NTC_DIE: 0x3E	Bit[5]: NTC2_CELL_ COLD_STS	Reports the NTC2 cold cell interrupt status. 0: No interrupt detected 1: An interrupt was detected The latched value depends on the selected interrupt type (e.g. rising, falling, or rising and falling). For a rising edge, the bit is set to 1 if a rising edge is detected. For a falling edge, the bit is set to 1 if a falling edge is detected. For a rising and falling edge, the bit is set to 1 if either edge is detected. For a level, the bit is set to 1 if the source signal is high.	Read-only	0x0	N/A
RD_NTC_DIE: 0x3E	Bit[6]: NTC3_CELL_ COLD_STS	Reports the NTC3 cold cell interrupt status. 0: No interrupt detected 1: An interrupt was detected The latched value depends on the selected interrupt type (e.g. rising, falling, or rising and falling). For a rising edge, the bit is set to 1 if a rising edge is detected. For a falling edge, the bit is set to 1 if a falling edge is detected. For a rising and falling edge, the bit is set to 1 if either edge is detected. For a level, the bit is set to 1 if the source signal is high.	Read-only	0x0	N/A

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RD_NTC_DIE: 0x3E	Bit[7]: NTC4_CELL_ COLD_STS	Reports the NTC4 cold cell interrupt status. 0: No interrupt detected 1: An interrupt was detected The latched value depends on the selected interrupt type (e.g. rising, falling, or rising and falling). For a rising edge, the bit is set to 1 if a rising edge is detected. For a falling edge, the bit is set to 1 if a falling edge is detected. For a rising and falling edge, the bit is set to 1 if either edge is detected. For a level, the bit is set to 1 if the source signal is high.	Read-only	0x0	N/A
RD_NTC_DIE: 0x3E	Bit[8]: NTC1_PCB_ MNTR_HOT_ STS	Reports the NTC1 hot PCB interrupt status. Depending on PCB_MNTR_STS_SEL, this bit may report the latched status or the real-time status. The latched value depends on the selected interrupt type (e.g. rising, falling, or rising and falling). For a rising edge, the bit is set to 1 if a rising edge is detected. For a falling edge, the bit is set to 1 if a falling edge is detected. For a rising and falling edge, the bit is set to 1 if either edge is detected. For a level, the bit is set to 1 if the source signal is high. If PCB_MNTR_STS_SEL reports the real-time status: 0: The NTC1 PCB temperature is within its normal range 1: The NTC1 PCB temperature is too hot If PCB_MNTR_STS_SEL reports the latched status: 0: No interrupt has been detected 1: An interrupt has been detected	Read-only	0x0	N/A

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RD_NTC_DIE: 0x3E	Bit[9]: NTC2_PCB_ MNTR_HOT_ STS	Reports the NTC2 hot PCB interrupt status. Depending on PCB_MNTR_STS_SEL, this bit may report the latched status or the real-time status. The latched value depends on the selected interrupt type (e.g. rising, falling, or rising and falling). For a rising edge, the bit is set to 1 if a rising edge is detected. For a falling edge, the bit is set to 1 if a falling edge is detected. For a rising and falling edge, the bit is set to 1 if either edge is detected. For a level, the bit is set to 1 if the source signal is high. If PCB_MNTR_STS_SEL reports the real-time status: 0: The NTC2 PCB temperature is within its normal range 1: The NTC2 PCB temperature is too hot If PCB_MNTR_STS_SEL reports the latched status: 0: No interrupt has been detected 1: An interrupt has been detected	Read-only	0x0	N/A
RD_NTC_DIE: 0x3E	Bit[10]: NTC3_PCB_ MNTR_HOT_ STS	Reports the NTC3 hot PCB interrupt status. Depending on PCB_MNTR_STS_SEL, this bit may report the latched status or the real-time status. The latched value depends on the selected interrupt type (e.g. rising, falling, or rising and falling). For a rising edge, the bit is set to 1 if a rising edge is detected. For a falling edge, the bit is set to 1 if a falling edge is detected. For a rising and falling edge, the bit is set to 1 if either edge is detected. For a level, the bit is set to 1 if the source signal is high. If PCB_MNTR_STS_SEL reports the real-time status: 0: The NTC3 PCB temperature is within its normal range 1: The NTC3 PCB temperature is too hot If PCB_MNTR_STS_SEL reports the latched status: 0: No interrupt has been detected 1: An interrupt has been detected	Read-only	0x0	N/A

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RD_NTC_DIE: 0x3E	Bit[11]: NTC4_PCB_ MNTR_HOT_ STS	Reports the NTC4 hot PCB interrupt status. Depending on PCB_MNTR_STS_SEL, this bit may report the latched status or the real-time status. The latched value depends on the selected interrupt type (e.g. rising, falling, or rising and falling). For a rising edge, the bit is set to 1 if a rising edge is detected. For a falling edge, the bit is set to 1 if a falling edge is detected. For a rising and falling edge, the bit is set to 1 if either edge is detected. For a level, the bit is set to 1 if the source signal is high. If PCB_MNTR_STS_SEL reports the real-time status: 0: The NTC4 PCB temperature is within its normal range 1: The NTC4 PCB temperature is too hot If PCB_MNTR_STS_SEL reports the latched status: 0: No interrupt has been detected 1: An interrupt has been detected	Read-only	0x0	N/A
RD_NTC_DIE: 0x3E	Bit[13]: DIE_TEMP_ DIG_RT_STS	Reports the real-time digital die temperature status, based on the result of the latest comparison between the digital die temperature reading and the associated hot threshold. 0: The die temperature is within its normal range 1: The digital die temperature is too hot	Read-only	0x0	N/A
RD_NTC_DIE: 0x3E	Bit[14]: DIE_TEMP_ DIG_STS	Reports the die temperature interrupt status. The latched value depends on the selected interrupt type (e.g. rising, falling, or rising and falling). For a rising edge, the bit is set to 1 if a rising edge is detected. For a falling edge, the bit is set to 1 if a falling edge is detected. For a rising and falling edge, the bit is set to 1 if either edge is detected. For a level, the bit is set to 1 if the source signal is high. This bit is cleared by DIE_TEMP_DIG_CLEAR. 0: No digital die temperature event has been detected 1: The digital die temperature event has been detected	Read-only	0x0	N/A

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RD_NTC_DIE: 0x3E	Bit[15]: DIE_TEMP_ ANA_EVENT	Obtains the status from analog circuit recordings after a hot die temperature event. This bit cannot be read in real time, since digital logic is shut down when this event occurs. This bit is cleared by DIE_TEMP_ANA_CLEAR. 0: The die temperature is within its normal range 1: The analog die temperature is too hot	Read-only	0x0	N/A
RD_V_NTC4_ LR: 0x3F	Bits[9:0]: NTC4_VALUE	Reports the NTC4 protection ADC reading. NTC4 monitoring is controlled by NTC4_EN, so this register updates when protection monitoring is requested and NTC4_EN is enabled.	Read-only	0x000	LSB: 0.09766% of NTCB RNG: 0% to 99.906% of NTCB 0x000: 0% of NTCB
RD_V_NTC4_ LR: 0x3F	Bit[12]: NTC1_CELL_ COLD_RT_STS	Reports the NTC1 cold cell real-time status. 0: The NTC1 temperature is within its normal range 1: The NTC1 temperature is too cold	Read-only	0x0	N/A
RD_V_NTC4_ LR: 0x3F	Bit[13]: NTC2_CELL_ COLD_RT_STS	Reports the NTC2 cold cell real-time status. 0: The NTC2 temperature is within its normal range 1: The NTC2 temperature is too cold	Read-only	0x0	N/A
RD_V_NTC4_ LR: 0x3F	Bit[14]: NTC3_CELL_ COLD_RT_STS	Reports the NTC3 cold cell real-time status. 0: The NTC3 temperature is within its normal range 1: The NTC3 temperature is too cold	Read-only	0x0	N/A
RD_V_NTC4_ LR: 0x3F	Bit[15]: NTC4_CELL_ COLD_RT_STS	Reports the NTC4 cold cell real-time status. 0: The NTC4 temperature is within its normal range 1: The NTC4 temperature is too cold	Read-only	0x0	N/A
RD_V_NTC3_ LR: 0x40	Bits[9:0]: NTC3_VALUE	Reports the NTC3 protection ADC reading. NTC3 monitoring is controlled by NTC3_EN, so this register updates when protection monitoring is requested and NTC3_EN is enabled.	Read-only	0x000	LSB: 0.09766% of NTCB RNG: 0% to 99.906% of NTCB 0x000: 0% of NTCB
RD_V_NTC3_ LR: 0x40	Bit[12]: NTC1_CELL_ HOT_RT_STS	Reports the NTC1 hot cell real-time status. 0: The NTC1 temperature is within its normal range 1: The NTC1 temperature is too hot	Read-only	0x0	N/A

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RD_V_NTC3_LR: 0x40	Bit[13]: NTC2_CELL_HOT_RT_STS	Reports the NTC2 hot cell real-time status. 0: The NTC2 temperature is within its normal range 1: The NTC2 temperature is too hot	Read-only	0x0	N/A
RD_V_NTC3_LR: 0x40	Bit[14]: NTC3_CELL_HOT_RT_STS	Reports the NTC3 hot cell real-time status. 0: The NTC3 temperature is within its normal range 1: The NTC3 temperature is too hot	Read-only	0x0	N/A
RD_V_NTC3_LR: 0x40	Bit[15]: NTC4_CELL_HOT_RT_STS	Reports the NTC4 hot cell real-time status. 0: The NTC4 temperature is within its normal range 1: The NTC4 temperature is too hot	Read-only	0x0	N/A
RD_V_NTC2_LR: 0x41	Bits[9:0]: NTC2_VALUE	Reports the NTC2 protection ADC reading. NTC2 monitoring is controlled by NTC2_EN, so this register updates when protection monitoring is requested and NTC2_EN is enabled.	Read-only	0x000	LSB: 0.09766% of NTCB RNG: 0% to 99.906% of NTCB 0x000: 0% of NTCB
RD_V_NTC1_LR: 0x42	Bits[9:0]: NTC1_VALUE	Reports the NTC1 protection ADC reading. NTC1 monitoring is controlled by NTC1_EN, so this register updates when protection monitoring is requested and NTC1_EN is enabled.	Read-only	0x000	LSB: 0.09766% of NTCB RNG: 0% to 99.906% of NTCB 0x000: 0% of NTCB
RD_T_DIE: 0x43	Bits[9:0]: DIE_TEMP_V	Reports the die temperature, which can be calculated with the following equation: T = Reading x 0.474 - 269.12°C	Read-only	0x000	LSB: 0.474°C RNG: -269.12°C to +215.78°C 0x2E3: 81.18°C
NTC_CLR: 0x44	Bit[2]: PCB_MNTR_STS_SEL	Controls the NTCx_PCB_MNTR_HOT_STS register. 0: Show the latched status going to the interrupt controller 1: Show the real-time status	R/W	0x0	N/A
NTC_CLR: 0x44	Bit[14]: DIE_TEMP_DIG_CLEAR	Write 1 to clear a digital die too hot event. This bit is a self-clearing register.	Write-only	0x0	N/A
NTC_CLR: 0x44	Bit[15]: DIE_TEMP_ANA_CLEAR	Write 1 to clear an analog die too hot event. This bit is a self-clearing register.	Write-only	0x0	N/A
DIE_CFG: 0x46	Bit[1]: DIE_TEMP_DIG_EN	0: Disabled 1: Enable digital die temperature sensor	R/W (can lock to read-only)	0x1 (OTP)	0: Disabled 1: Enabled
DIE_CFG: 0x46	Bit[3]: DIE_TEMP_DIG_FAULT_EN	0: A digital die temperature events does not trigger fault mode 1: A digital die temperature events triggers fault mode	R/W (can lock to read-only)	0x0 (OTP)	0: Disabled 1: Enabled

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NTC_CFG: 0x47	Bit[0]: NTC1_EN	Enables protection monitoring for NTC1 if monitoring is required. Monitoring is automatically required when the IC is not in safe mode, but this function can be enabled in safe mode with PROTECT_IN_SAFE_CFG.	R/W (can lock to read-only)	0x0 (OTP)	0: Disabled 1: Enabled
NTC_CFG: 0x47	Bit[1]: NTC1_TYPE_ SEL	Configures the NTC1 monitor type. 0: Cell monitor 1: PCB monitor	R/W (can lock to read-only)	0x0 (OTP)	N/A
NTC_CFG: 0x47	Bit[2]: NTC2_EN	Enables protection monitoring for NTC2 if monitoring is required. Monitoring is automatically required when the IC is not in safe mode, but this function can be enabled in safe mode with PROTECT_IN_SAFE_CFG.	R/W (can lock to read-only)	0x0 (OTP)	0: Disabled 1: Enabled
NTC_CFG: 0x47	Bit[3]: NTC2_TYPE_ SEL	Configures the NTC2 monitor type. 0: Cell monitor 1: PCB monitor	R/W (can lock to read-only)	0x0 (OTP)	N/A
NTC_CFG: 0x47	Bit[4]: NTC3_EN	Enables protection monitoring for NTC3 if monitoring is required. Monitoring is automatically required when the IC is not in safe mode, but this function can be enabled in safe mode with PROTECT_IN_SAFE_CFG.	R/W (can lock to read-only)	0x0 (OTP)	0: Disabled 1: Enabled
NTC_CFG: 0x47	Bit[5]: NTC3_TYPE_ SEL	Configures the NTC3 monitor type. 0: Cell monitor 1: PCB monitor	R/W (can lock to read-only)	0x0 (OTP)	N/A
NTC_CFG: 0x47	Bit[6]: NTC4_EN	Enables protection monitoring for NTC4 if monitoring is required. Monitoring is automatically required when the IC is not in safe mode, but this function can be enabled in safe mode with PROTECT_IN_SAFE_CFG.	R/W (can lock to read-only)	0x0 (OTP)	0: Disabled 1: Enabled
NTC_CFG: 0x47	Bit[7]: NTC4_TYPE_ SEL	Configures the NTC4 monitor type. 0: Cell monitor 1: PCB monitor	R/W (can lock to read-only)	0x1 (OTP)	N/A
NTC_CFG: 0x47	Bit[8]: NTC3_PD_EN	Enables the internal pull-down function on NTC3.	R/W (can lock to read-only)	0x0 (OTP)	0: Disabled 1: Enabled
NTC_CFG: 0x47	Bit[9]: NTC4_PD_EN	Enables the internal pull-down function on NTC4.	R/W (can lock to read-only)	0x0 (OTP)	0: Disabled 1: Enabled
NTC_CFG: 0x47	Bit[10]: NTCB_ DYNAMIC_ON	Enables dynamic bias on NTCB during ADC conversions of NTC channels. When disabled, NTCB is always enabled, which increases current consumption.	R/W (can lock to read-only)	0x1 (OTP)	N/A

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NTC_CFG: 0x47	Bit[13]: NTC_CELL_ HOT_FAULT_ EN	0: The system does not enter fault mode if the cell monitor hot limit is reached 1: The system enters fault mode if the cell monitor hot limit is reached	R/W (can lock to read-only)	0x0 (OTP)	0: Disabled 1: Enabled
NTC_CFG: 0x47	Bit[14]: NTC_CELL_ COLD_FAULT_ EN	0: The system does not enter fault mode if the cell monitor cold limit is reached 1: The system enters fault mode if the cell monitor cold limit is reached	R/W (can lock to read-only)	0x0 (OTP)	0: Disabled 1: Enabled
NTC_CFG: 0x47	Bit[15]: PCB_MNTR_ FAULT_EN	0: The system does not enter fault mode if the PCB monitor's hot limit is reached 1: The system enters fault mode if the PCB monitor's hot limit is reached	R/W (can lock to read-only)	0x0 (OTP)	0: Disabled 1: Enabled
NTCC_OTHR_ DSG: 0x48	Bits[9:0]: NTC_CELL_ HOT_DISCH	Sets the discharge NTC hot cell monitor voltage threshold. The limit is triggered if the value is equal to or below the set threshold.	R/W (can lock to read-only)	0x12E (MTP)	LSB: 0.09756% of NTCB RNG: 0% to 99.9% of NTCB 0x000: 0% of NTCB
NTCC_UTHR_ DSG: 0x49	Bits[9:0]: NTC_CELL_ COLD_DISCH	Sets the discharge NTC cold cell monitor voltage threshold. The limit is triggered if the value exceeds the set threshold.	R/W (can lock to read-only)	0x294 (MTP)	LSB: 0.09756% of NTCB RNG: 0% to 99.9% of NTCB 0x000: 0% of NTCB
NTCC_OTHR_ CHG: 0x4A	Bits[9:0]: NTC_CELL_ HOT_CHG	Sets the charge NTC hot cell monitor voltage threshold. The limit is triggered if the value is equal to or below the set threshold.	R/W (can lock to read-only)	0x12E (MTP)	LSB: 0.0975% of NTCB RNG: 0% to 99.9% of NTCB 0x000: 0% of NTCB
NTCC_UTHR_ CHG: 0x4B	Bits[9:0]: NTC_CELL_ COLD_CHG	Sets the charge NTC cold cell monitor voltage threshold. The limit is triggered if the value exceeds the set threshold.	R/W (can lock to read-only)	0x294 (MTP)	LSB: 0.09756% of NTCB RNG: 0% to 99.9% of NTCB 0x000: 0% of NTCB
NTCC_UTHR_ CHG: 0x4B	Bits[15:11]: NTC_CELL_ HYST	Sets the NTC cell monitor hysteresis.	R/W (can lock to read-only)	0x11 (OTP)	LSB: 0.1953% of NTCB RNG: 0% to 6.055% of NTCB, 0x00: 0% of NTCB
NTCM_OTHR: 0x4C	Bits[9:0]: PCB_MNTR_ HOT	Sets the NTC hot PCB monitor voltage threshold. The limit is triggered if the NTC reading is equal to or below the set threshold.	R/W	0x0EB (OTP)	LSB: 0.09756% of NTCB RNG: 0% to 99.9% of NTCB 0x000: 0% of NTCB

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NTCM_OTHR: 0x4C	Bits[15:11]: PCB_MNTR_ HYST	Sets the NTC hot PCB monitor hysteresis.	R/W	0x10 (OTP)	LSB: 0.1953% of NTCB RNG: 0% to 6.055% of NTCB, 0x00: 0% of NTCB
DIE_OT: 0x4D	Bits[9:0]: DIE_TEMP_HOT	Sets the digital die temperature threshold.	R/W	0x2E3 (OTP)	LSB: 0.474°C RNG: -269.12°C to +215.78°C 0x2E3: 81.18°C
DIE_OT: 0x4D	Bits[15:11]: DIE_TEMP_ HYST	Sets the digital die temperature hysteresis.	R/W	0x15 (OTP)	LSB: 0.474°C RNG: 0°C to 14.68°C, 0x15: 10°C

Diagnosis

Address Name and location	Field Bit Position and Name	Description	Type	Value Reset (OTP/MTP)	Encoding, LSB and Range
SELF_STS: 0x4E	Bit[0]: SELF_TEST_ STS_UV	0: No failure has been detected 1: A failure has been detected	Read-only	0x0	N/A
SELF_STS: 0x4E	Bit[1]: SELF_TEST_ STS_OV	0: No failure has been detected 1: A failure has been detected	Read-only	0x0	N/A
SELF_STS: 0x4E	Bit[2]: REGIN_STS	0: No failure has been detected 1: A failure has been detected	Read-only	0x0	N/A
SELF_STS: 0x4E	Bit[3]: 3V3_STS	0: No failure has been detected 1: A failure has been detected	Read-only	0x0	N/A
SELF_STS: 0x4E	Bit[4]: VDD_STS	0: No failure has been detected 1: A failure has been detected	Read-only	0x0	N/A
SELF_STS: 0x4E	Bit[5]: OTPCHK_ DONE_STS	When true, OTP CRC check is complete. This bit can be cleared by setting OTP_CRC_DO = 0.	Read-only	0x0	0: False 1: True
SELF_STS: 0x4E	Bit[6]: OTP_CRC_ OUTCOME	Reports the errors in the outcome CRC OTP check. 0: No errors detected 1: One or more error(s) detected The result of the previous check is retained until OTP_CRC_DO is set to 1 (from 0). Then OTP_CRC_OUTCOME remains at 0 until the check is completed and a new result is available.	Read-only	0x0	0: False 1: True
RD_VA1P8: 0x4F	Bits[9:0]: VDD_VALUE	Reports the latest ADC reading for the VDD regulator.	Read-only	0x000	LSB: 3.2227mV RNG: 0mV to 3296.82mV, 0x000: 0mV
RD_VA3P3: 0x50	Bits[9:0]: 3V3_VALUE	Reports the latest ADC reading for the 3V3 regulator.	Read-only	0x000	LSB: 6.4453mV RNG: 0mV to 6593.55mV, 0x000: 0mV

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RD_VA5: 0x51	Bits[9:0]: REGIN_VALUE	Reports the latest ADC reading for REGIN.	Read-only	0x000	LSB: 6.4453mV RNG: 0mV to 6593.55mV, 0x000: 0mV
RD_VASELF: 0x52	Bits[9:0]: SELF_TEST_ VALUE	Reports the latest 10-bit ADC reading for the internal fixed voltage reference, which acts as an ADC self-test.	Read-only	0x000	LSB: 3.2227mV RNG: 0mV to 3296.82mV, 0x000: 0mV
RD_OPENH: 0x53	Bit[0]: CELL_0_OPW_ STS	Reports whether C0 has as an open wire after a detection has been executed.	Read-only	0x0	0: Not detected 1: Detected
RD_OPENH: 0x53	Bit[1]: CELL_1_OPW_ STS	Reports whether C1 has as an open wire after a detection has been executed.	Read-only	0x0	0: Not detected 1: Detected
RD_OPENH: 0x53	Bit[2]: CELL_2_OPW_ STS	Reports whether C2 has as an open wire after a detection has been executed.	Read-only	0x0	0: Not detected 1: Detected
RD_OPENH: 0x53	Bit[3]: CELL_3_OPW_ STS	Reports whether C3 has as an open wire after a detection has been executed.	Read-only	0x0	0: Not detected 1: Detected
RD_OPENH: 0x53	Bit[4]: CELL_4_OPW_ STS	Reports whether C4 has as an open wire after a detection has been executed.	Read-only	0x0	0: Not detected 1: Detected
RD_OPENH: 0x53	Bit[5]: CELL_5_OPW_ STS	Reports whether C5 has as an open wire after a detection has been executed.	Read-only	0x0	0: Not detected 1: Detected
RD_OPENH: 0x53	Bit[6]: CELL_6_OPW_ STS	Reports whether C6 has as an open wire after a detection has been executed.	Read-only	0x0	0: Not detected 1: Detected
RD_OPENH: 0x53	Bit[7]: CELL_7_OPW_ STS	Reports whether C7 has as an open wire after a detection has been executed.	Read-only	0x0	0: Not detected 1: Detected
RD_OPENH: 0x53	Bit[8]: CELL_8_OPW_ STS	Reports whether C8 has as an open wire after a detection has been executed. The cell must be enabled from CELL_S_CTRL for this flag to function.	Read-only	0x0	0: Not detected 1: Detected
RD_OPENH: 0x53	Bit[9]: CELL_9_OPW_ STS	Reports whether C9 has as an open wire after a detection has been executed. The cell must be enabled from CELL_S_CTRL for this flag to function.	Read-only	0x0	0: Not detected 1: Detected
RD_OPENH: 0x53	Bit[10]: CELL_10_OPW_ STS	Reports whether C10 has as an open wire after a detection has been executed. The cell must be enabled from CELL_S_CTRL for this flag to function.	Read-only	0x0	0: Not detected 1: Detected
RD_OPENH: 0x53	Bit[11]: CELL_11_OPW_ STS	Reports whether C11 has as an open wire after a detection has been executed. The cell must be enabled from CELL_S_CTRL for this flag to function.	Read-only	0x0	0: Not detected 1: Detected

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RD_OPENH: 0x53	Bit[12]: CELL_12_OPW_STS	Reports whether C12 has as an open wire after a detection has been executed. The cell must be enabled from CELL_S_CTRL for this flag to function.	Read-only	0x0	0: Not detected 1: Detected
RD_OPENH: 0x53	Bit[13]: CELL_13_OPW_STS	Reports whether C13 has as an open wire after a detection has been executed. The cell must be enabled from CELL_S_CTRL for this flag to function.	Read-only	0x0	0: Not detected 1: Detected
RD_OPENH: 0x53	Bit[14]: CELL_14_OPW_STS	Reports whether C14 has as an open wire after a detection has been executed. The cell must be enabled from CELL_S_CTRL for this flag to function.	Read-only	0x0	0: Not detected 1: Detected
RD_OPENH: 0x53	Bit[15]: CELL_15_OPW_STS	Reports whether C15 has as an open wire after a detection has been executed. The cell must be enabled from CELL_S_CTRL for this flag to function.	Read-only	0x0	0: Not detected 1: Detected
RD_OPENL: 0x54	Bit[0]: CELL_16_OPW_STS	Reports whether C16 has as an open wire after a detection has been executed. The cell must be enabled from CELL_S_CTRL for this flag to function.	Read-only	0x0	0: Not detected 1: Detected
SFT_GO: 0x55	Bit[0]: OTP_CRC_DO	Write 0 to this bit to clear the results. Write 1 to this bit to schedule an OTP CRC.	R/W	0x0	N/A
SFT_GO: 0x55	Bit[8]: OPEN_WIRE_GO	Write 1 to this bit to schedule an open-wire check. Write 0 to this bit to clear the results of a completed open-wire detection.	R/W	0x0	1: Execute this function
SFT_GO: 0x55	Bit[9]: OPEN_WIRE_DONE_STS	Reports whether open-wire detection is complete. When true, open-wire detection is complete. Write 0 to OPEN_WIRE_GO to clear this flag.	Read-only	0x0	0: False 1: True
SFT_GO: 0x55	Bit[10]: OPEN_WIRE_ERR_STS	Reports whether an error has occurred during open-wire detection (e.g. cell-balancing is already operating).	Read-only	0x0	0: False 1: True
SELF_CFG: 0x56	Bit[0]: REGIN_EN	Enables ADC REGIN monitoring to ensure that the REGIN supply is above the defined UV level. 0: Disable REGIN check 1: Enable REGIN check	R/W (can lock to read-only)	0x1 (OTP)	0: Disabled 1: Enabled
SELF_CFG: 0x56	Bit[1]: 3V3_EN	Enables ADC 3V3 UV monitoring to ensure that the 3.3V supply is above the defined UV level.	R/W (can lock to read-only)	0x1 (OTP)	0: Disabled 1: Enabled

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SELF_CFG: 0x56	Bit[2]: VDD_EN	Enables the ADC VDD monitoring check to ensure that the digital 1.8V supply is above the defined UV level. 0: Disable VDD check 1: Enable VDD check	R/W (can lock to read-only)	0x1 (OTP)	0: Disabled 1: Enabled
SELF_CFG: 0x56	Bit[3]: ADC_SELF_ TEST_EN	Enables the ADC self-test check that indicates whether the applied voltage is within the allowed range. 0: Disabled 1: Enabled	R/W (can lock to read-only)	0x1 (OTP)	0: Disabled 1: Enabled
SELF_CFG: 0x56	Bit[6]: OTP_CRC_EN	Enables the OTP CRC.	R/W (can lock to read-only)	0x1 (OTP)	0: Disabled 1: Enabled
SELF_CFG: 0x56	Bit[9]: OPEN_WIRE_ FAULT_EN	0: An open-wire condition does not trigger fault mode 1: An open-wire condition triggers fault mode	R/W (can lock to read-only)	0x0 (OTP)	0: Disabled 1: Enabled
SELF_CFG: 0x56	Bit[10]: OPEN_WIRE_ PON	Enables open-wire detection when the device is powered on (leaving shutdown mode).	R/W (can lock to read-only)	0x0 (OTP)	0: Disabled 1: Enabled
SELF_CFG: 0x56	Bit[14]: 3V3_VDD_ FAULT_EN	Defines the reaction when a 3.3V UV or VDD UV condition is detected (analog comparator and ADC monitoring). 0: Disable fault mode 1: Enable fault mode	R/W (can lock to read-only)	0x0 (OTP)	0: Disabled 1: Enabled
SELF_CFG: 0x56	Bit[15]: OTP_FAULT_EN	0: An OTP CRC error does not trigger fault mode 1: An OTP CRC error triggers fault mode	R/W (can lock to read-only)	0x0 (OTP)	0: Disabled 1: Enabled
OPEN_CFG: 0x57	Bits[3:0]: OPW_CHECK_ LEN	Sets the length of each pull-up and pull-down phase.	R/W	0x7 (OTP)	LSB: 1ms RNG: 1ms to 16ms 0: 1ms
OPEN_CFG: 0x57	Bits[11:8]: OPW_CHECK_ TH	Sets the open-wire threshold used during the detection sequence.	R/W	0x4 (OTP)	LSB: 39.06mV RNG: 39.06mV to 624.96mV 0: 39.06mV
REGIN_UV: 0x58	Bits[8:0]: REGIN_UV_ LIMIT	Sets the REGIN UV threshold, which is applied to ADC readings.	Read-only	0x16D (OTP)	LSB: 12.891mV RNG: 0mV to 6587.1mV 0x000: 0mV
V3P3_UV: 0x59	Bits[7:0]: 3V3_UV_LIMIT	Sets the threshold for 3.3V UV conditions, which is applied to the ADC reading reported in 3V3_VALUE.	R/W	0xF0 (OTP)	LSB: 12.89mV RNG: 0mV to 3287.1mV 0x00: 0mV
VDD_UV: 0x5A	Bits[7:0]: VDD_UV_LIMIT	Sets the threshold for VDD 1.8V UV conditions, which is applied to the ADC reading reported in VDD_VALUE.	Read-only	0x84 (OTP)	LSB: 12.89mV RNG: 0mV to 3287.1mV 0x00: 0mV

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SELF_THR: 0x5B	Bits[7:0]: SELF_TEST_ UV_LIMIT	Sets the threshold for self-test UV conditions, which is applied to the SELF_TEST_VALUE ADC readings.	Read-only	0x55 (OTP)	LSB 12.89mV RNG: 0mV to 3287.1mV, 0x00: 0mV
SELF_THR: 0x5B	Bits[15:8]: SELF_TEST_ OV_LIMIT	Sets the threshold for self-test OV conditions, which is applied to SELF_TEST_VALUE ADC readings.	Read-only	0x65 (OTP)	LSB: 12.89mV RNG: 0mV to 3287.1mV 0x00: 0mV

Fault and Fault Recovery

Address Name and Location	Field Bit Position and Name	Description	Type	Value Reset (OTP/MTP)	Encoding, LSB and Range
FT_STS1: 0x5D	Bit[0]: CELL_UV_ FAULT_STS	Reports whether a cell UV condition is triggering a fault.	Read-only	0x0	0: False 1: True
FT_STS1: 0x5D	Bit[1]: CELL_OV_ FAULT_STS	Reports whether a cell OV condition is triggering a fault.	Read-only	0x0	0: False 1: True
FT_STS1: 0x5D	Bit[2]: CELL_DEAD_ FAULT_STS	Reports whether a dead cell condition is triggering a fault.	Read-only	0x0	0: False 1: True
FT_STS1: 0x5D	Bit[3]: CELL_MSMT_ FAULT_STS	Reports whether a cell mismatch condition is triggering a fault.	Read-only	0x0	0: False 1: True
FT_STS1: 0x5D	Bit[4]: OPEN_WIRE_ FAULT_STS	Reports whether an open-wire condition is triggering a fault.	Read-only	0x0	0: False 1: True
FT_STS1: 0x5D	Bit[5]: VTOP_UV_ FAULT_STS	Reports whether a VTOP UV condition is triggering a fault.	Read-only	0x0	0: False 1: True
FT_STS1: 0x5D	Bit[6]: VTOP_OV_ FAULT_STS	Reports whether a VTOP OV condition is triggering a fault.	Read-only	0x0	0: False 1: True
FT_STS1: 0x5D	Bit[7]: PCB_MNTR_ FAULT_STS	Reports whether an NTC PCB monitor condition is triggering a fault.	Read-only	0x0	0: False 1: True
FT_STS1: 0x5D	Bit[8]: NTC_CELL_ HOT_FAULT_ STS	Reports whether an NTC hot cell monitoring condition is triggering a fault.	Read-only	0x0	0: False 1: True
FT_STS1: 0x5D	Bit[9]: NTC_CELL_ COLD_FAULT_ STS	Reports whether an NTC cold cell monitoring condition is triggering a fault.	Read-only	0x0	0: False 1: True
FT_STS1: 0x5D	Bit[10]: OC1_DCHG_ FAULT_STS	Reports whether a discharge over-current (OC) 1 condition is triggering a fault.	Read-only	0x0	0: False 1: True
FT_STS1: 0x5D	Bit[11]: OC2_DCHG_ FAULT_STS	Reports whether a discharge OC 2 condition is triggering a fault.	Read-only	0x0	0: False 1: True
FT_STS1: 0x5D	Bit[12]: OC_CHG_ FAULT_STS	Reports whether a charge OC condition is triggering a fault.	Read-only	0x0	0: False 1: True
FT_STS1: 0x5D	Bit[13]: SC_DCHG_ FAULT_STS	Reports whether a discharge short-circuit condition is triggering a fault.	Read-only	0x0	0: False 1: True
FT_STS1: 0x5D	Bit[14]: SC_CHG_ FAULT_STS	Reports whether a charge short-circuit condition is triggering a fault.	Read-only	0x0	0: False 1: True

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FT_STS1: 0x5D	Bit[15]: DIE_TEMP_ FAULT_STS	Reports whether a die temperature condition is triggering a fault.	Read-only	0x0	0: False 1: True
FT_STS2: 0x5E	Bit[0]: OTP_CRC_ FAULT_STS	Reports whether an OTP CRC condition is triggering a fault. This bit can be cleared with OTP_CRC_CLR.	Read-only	0x0	0: False 1: True
FT_STS2: 0x5E	Bit[1]: 3V3_FAULT_STS	Reports whether a 3V3 UV is triggering a fault. A 3V3 fault can be triggered by ADC 3V3 UV monitoring or the 3.3V analog UV comparator. The 3.3V analog comparator is always enabled, so when 3V3_VDD_FAULT_EN is enabled, it can trigger a fault even when ADC 3V3 UV monitoring (3V3_EN) is disabled.	Read-only	0x0	0: False 1: True
FT_STS2: 0x5E	Bit[2]: VDD_FAULT_ STS	Reports whether a VDD UV is triggering a fault. A VDD fault can be triggered by ADC VDD UV monitoring or the VDD analog UV comparator. The VDD analog comparator is always enabled, so when 3V3_VDD_FAULT_EN is enabled, it can trigger a fault even when ADC VDD UV monitoring (VDD_EN) is disabled.	Read-only	0x0	0: False 1: True
FT_STS2: 0x5E	Bit[3]: DRIVER_ FAULT_STS	Reports whether a driver turn-on condition is triggering a fault.	Read-only	0x0	0: False 1: True
FT_STS2: 0x5E	Bit[9]: SC_CHG_ RECOVERY_ FAILED	When true, automatic recovery has failed. Use SC_CHG_FAULT_CLR to clear this bit.	Read-only	0x0	0: False 1: True
FT_STS2: 0x5E	Bit[10]: SC_DCHG_ RECOVERY_ FAILED	When true, automatic recovery has failed. Use SC_DCHG_FAULT_CLR to clear this bit.	Read-only	0x0	0: False 1: True
FT_STS2: 0x5E	Bit[11]: OC_CHG_ RECOVERY_ FAILED	When true, automatic recovery has failed. Use OC_CHG_FAULT_CLR to clear this bit.	Read-only	0x0	0: False 1: True
FT_STS2: 0x5E	Bit[12]: OC_DCHG_ RECOVERY_ FAILED	When true, automatic recovery has failed. Use OC1_DCHG_FAULT_CLR or OC2_DCHG_FAULT_CLR to clear this bit.	Read-only	0x0	0: False 1: True
FT_STS2: 0x5E	Bit[13]: RMVL_BUSY	When true, short-circuit removal detection is busy after an OC or SC protection has occurred.	Read-only	0x0	0: False 1: True
FT_CLR: 0x5F	Bit[0]: CELL_UV_ FAULT_CLR	Write 1 to this bit to manually clear a cell UV fault. This is a self-clearing register.	Write-only	0x0	1: Execute this function
FT_CLR: 0x5F	Bit[1]: CELL_OV_ FAULT_CLR	Write 1 to this bit to manually clear a cell OV fault. This is a self-clearing register.	Write-only	0x0	1: Execute this function

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FT_CLR: 0x5F	Bit[2]: CELL_DEAD_ FAULT_CLR	Write 1 to this bit to manually clear a dead cell fault. This is a self-clearing register.	Write-only	0x0	1: Execute this function
FT_CLR: 0x5F	Bit[3]: CELL_MSMT_ FAULT_CLR	Write 1 to this bit to manually clear a mismatched cell fault. This is a self-clearing register.	Write-only	0x0	1: Execute this function
FT_CLR: 0x5F	Bit[4]: OPEN_WIRE_ FAULT_CLR	Write 1 to this bit to manually clear a cell open wire fault. This is a self-clearing register.	Write-only	0x0	1: Execute this function
FT_CLR: 0x5F	Bit[5]: VTOP_UV_ FAULT_CLR	Write 1 to this bit to manually clear a battery pack UV fault. This is a self-clearing register.	Write-only	0x0	1: Execute this function
FT_CLR: 0x5F	Bit[6]: VTOP_OV_ FAULT_CLR	Write 1 to this bit to manually clear a battery pack OV fault. This is a self-clearing register.	Write-only	0x0	1: Execute this function
FT_CLR: 0x5F	Bit[7]: PCB_MNTR_ FAULT_CLR	Write 1 to this bit to manually clear an NTC PCB monitor fault. This is a self-clearing register.	Write-only	0x0	1: Execute this function
FT_CLR: 0x5F	Bit[8]: NTC_CELL_ HOT_FAULT_ CLR	Write 1 to this bit to manually clear a hot cell fault. This is a self-clearing register.	Write-only	0x0	1: Execute this function
FT_CLR: 0x5F	Bit[9]: NTC_CELL_ COLD_FAULT_ CLR	Write 1 to this bit to manually clear a cold cell fault. This is a self-clearing register.	Write-only	0x0	1: Execute this function
FT_CLR: 0x5F	Bit[10]: OC1_DCHG_ FAULT_CLR	Write 1 to this bit to manually clear a discharge OC 1 fault. This is a self-clearing register.	Write-only	0x0	1: Execute this function
FT_CLR: 0x5F	Bit[11]: OC2_DCHG_ FAULT_CLR	Write 1 to this bit to manually clear a discharge OC 2 fault. This is a self-clearing register.	Write-only	0x0	1: Execute this function
FT_CLR: 0x5F	Bit[12]: OC_CHG_FAULT _CLR	Write 1 to this bit to manually clear a charge OC fault. This is a self-clearing register.	Write-only	0x0	1: Execute this function
FT_CLR: 0x5F	Bit[13]: SC_DCHG_ FAULT_CLR	Write 1 to this bit to manually clear a discharge short-circuit fault. This is a self-clearing register.	Write-only	0x0	1: Execute this function
FT_CLR: 0x5F	Bit[14]: SC_CHG_ FAULT_CLR	Write 1 to this bit to manually clear a charge short-circuit fault. This is a self-clearing register.	Write-only	0x0	1: Execute this function
FT_CLR: 0x5F	Bit[15]: DIE_TEMP_ FAULT_CLR	Write 1 to this bit to manually clear a die temperature fault. This is a self-clearing register.	Write-only	0x0	1: Execute this function
FT_REC: 0x60	Bit[1]: NTC_CELL_ DCHG_REC	Enables auto-recovery from an NTC cell type fault (the temperature is back within the nominal range) in discharge mode or standby mode. Set this bit to 0 for manual recovery.	R/W (can lock to read-only)	0x0 (OTP)	0: Disabled 1: Enabled

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FT_REC: 0x60	Bit[2]: NTC_CELL_ CHG_REC	Enables auto-recovery from an NTC cell type fault (the temperature is back within the nominal range) in charge mode. Set this bit to 0 for manual recovery.	R/W (can lock to read-only)	0x0 (OTP)	0: Disabled 1: Enabled
FT_REC: 0x60	Bit[3]: NTC_CHG_REC_ MODE	Defines the recovery logic from an NTC hot/cold condition in charge mode. 0: NTC voltage [>/<] NTC_CELL_xxxx_CHG ± NTC_CELL_HYST 1: (NTC voltage [>/<] NTC_CELL_xxxx_CHG ± NTC_CELL_HYST) or if the charger is removed: (NTC voltage [>/<] NTC_CELL_xxxx_THR_IN_USE ± NTC_CELL_HYST) In this logic, NTC_CELL_xxxx_CHG is either NTC_CELL_HOT_CHG or NTC_CELL_COLD_CHG with comparison. The signs within the brackets are determined by the fault. When the current is within the standby boundaries in fault mode, NTC_CELL_xxxx_THR_IN_USE depends on CELL_HOT_STBY_MODE setting (available vs. conservative) or CELL_COLD_STBY_MODE (available vs conservative).	R/W	0x0 (OTP)	N/A
FT_REC: 0x60	Bit[4]: PCB_MNTR_REC	Enables automatic recovery from an NTC PCB monitor type fault. Set this bit to 0 for manual recovery.	R/W (can lock to read-only)	0x0 (OTP)	0: Disabled 1: Enabled
FT_REC: 0x60	Bit[6]: OC1_DCHG_REC	Enables an automatic recovery attempt for discharge OC 1 conditions. 0: Manual recovery 1: Automatic recovery attempt	R/W (can lock to read-only)	0x0 (OTP)	0: Disabled 1: Enabled
FT_REC: 0x60	Bit[7]: OC2_DCHG_REC	Enables an automatic recovery attempt for discharge OC 2 conditions. 0: Manual recovery 1: Automatic recovery attempt	R/W (can lock to read-only)	0x0 (OTP)	0: Disabled 1: Enabled
FT_REC: 0x60	Bit[8]: OC_CHG_REC	Enables an automatic recovery attempt for charge OC conditions. 0: Manual recovery 1: Automatic recovery attempt	R/W (can lock to read-only)	0x0 (OTP)	0: Disabled 1: Enabled
FT_REC: 0x60	Bit[9]: SC_DCHG_REC	Enables an automatic recovery attempt for discharge short-circuit conditions. 0: Manual recovery 1: Automatic recovery attempt	R/W (can lock to read-only)	0x0 (OTP)	0: Disabled 1: Enabled

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FT_REC: 0x60	Bit[10]: SC_CHG_REC	Enables an automatic recovery attempt for charge short-circuit conditions. 0: Manual recovery 1: Automatic recovery attempt	R/W (can lock to read-only)	0x0 (OTP)	0: Disabled 1: Enabled
FT_REC: 0x60	Bit[12]: DIE_TEMP_ FAULT_REC	Enables automatic recovery for die temperature conditions (when the temperature drops). 0: Manual recovery 1: Automatic recovery attempt	R/W (can lock to read-only)	0x0 (OTP)	0: Disabled 1: Enabled
FT_REC: 0x60	Bit[13]: DRIVER_FAULT_ CLR	Write 1 to this bit to manually clear a MOSFET driver fault. This is a self-clearing register.	Write-only	0x0	1: Execute this function
FT_REC: 0x60	Bit[14]: OTP_CRC_CLR	Write 1 to this bit to manually clear an OTP CRC fault. This is a self-clearing register.	Write-only	0x0	1: Execute this function
FT_REC: 0x60	Bit[15]: 3V3_VDD_ FAULT_CLR	Write 1 to this bit to manually clear 3.3V and 1.8V UV faults. This is a self-clearing register.	Write-only	0x0	1: Execute this function
FT0_CFG: 0x61	Bit[2]: CELL_HOT_ STBY_MODE	Defines the selection criteria for the NTC hot threshold when the battery pack current is within the STBY_CUR_TH range. 0: Available. The hotter threshold (and lower voltage) is selected between NTC_CELL_HOT_CHG and NTC_CELL_HOT_DISCH, and applied when the battery pack current is within the standby region 1: Conservative. The colder threshold (and higher voltage) is selected between NTC_CELL_HOT_CHG and NTC_CELL_HOT_DISCH, and applied when the battery pack current is within the standby region	R/W	0x0	N/A
FT0_CFG: 0x61	Bit[3]: CELL_COLD_ STBY_MODE	Defines the selection criteria for the NTC cold threshold when the battery pack current is within the STBY_CUR_TH range. 0: Available. The colder threshold (and higher voltage) is selected between NTC_CELL_COLD_DISCH and NTC_CELL_COLD_CHG, and applied when the battery pack current is within the standby region 1: Conservative. The hotter threshold (and lower voltage) is selected between NTC_CELL_COLD_DISCH and NTC_CELL_COLD_CHG, and applied when the battery pack current is within the standby region	R/W	0x0	N/A

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FT0_CFG: 0x61	Bit[5]: CELL_UV_ LOGIC_SEL	Selects which logic is used for status recovery from cell UV conditions. 0: The status recovers once the cell exceeds (UV threshold + hysteresis) 1: The status recovers by following either logic below: • The cell exceeds the UV threshold and the PACKP voltage exceeds (V_{TOP} + 270mV) • The cell exceeds (UV threshold + hysteresis)	R/W (can lock to read-only)	0x1 (OTP)	N/A
FT0_CFG: 0x61	Bit[7]: CELL_UV_REC	0: Manual recovery from cell UV fault 1: Automatic recovery from cell UV fault	R/W (can lock to read-only)	0x0 (OTP)	N/A
FT0_CFG: 0x61	Bit[9]: CELL_OV_ LOGIC_SEL	Selects which logic is used for status recovery from cell OV conditions. 0: The status recovers once the cell falls below (OV threshold - hysteresis) 1: The status recovers by following either logic below: • The cell falls below the OV threshold and the PACKP voltage falls below (VTOP – 1.6V) • The cell falls below (OV threshold – hysteresis)	R/W (can lock to read-only)	0x1 (OTP)	N/A
FT0_CFG: 0x61	Bit[11]: CELL_OV_REC	0: Manual recovery from cell OV fault 1: Automatic recovery from cell OV fault	R/W (can lock to read-only)	0x0 (OTP)	N/A
FT1_CFG: 0x62	Bits[1:0]: SCOC_PUP	Sets the battery pack pull-up current during short-circuit removal detection.	R/W	0x0 (MTP)	0x0: 250µA 0x1: 500µA 0x2: 750µA 0x3: 250µA
FT1_CFG: 0x62	Bits[3:2]: SCOC_DET_ TIME	Sets the time for SCOC_PUP.	R/W	0x0 (MTP)	0x0: 125ms 0x1: 250ms 0x2: 500ms 0x3: 1s
FT1_CFG: 0x62	Bits[6:4]: SCOC_RETRY_ DELAY	Sets the delay between short-circuit removal detection and a retry.	R/W	0x0 (MTP)	0x0: 1s 0x1: 2s 0x2: 4s 0x3: 6s 0x4: 10s 0x5: 15s 0x6: 20s 0x7: 25s
FT1_CFG: 0x62	Bits[14:13]: SC_PUP_ RETRY_N	Sets how many times short-circuit removal detection retries. 2'b00: Keep trying 2'b01: 1 try 2'b10: 2 tries 2'b11: 4 tries	R/W	0x0 (MTP)	N/A

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FT2_CFG: 0x63	Bits[1:0]: OC1_DCHG_ COOL	Sets the discharge OC 1 cool-down time. 2'b00: 100ms 2'b01: 200ms 2'b10: 500ms 2'b11: 1s	R/W	0x0 (MTP)	N/A
FT2_CFG: 0x63	Bits[3:2]: OC1_DCHG_ RETRY	Sets the number of discharge OC 1 reconnection attempts. 2'b00: 1 time 2'b01: 2 times 2'b10: 3 times 2'b11: Keep trying	R/W	0x0 (MTP)	LSB: 1 attempt 0x0: 1 attempt
FT2_CFG: 0x63	Bits[5:4]: OC2_DCHG_ COOL	Sets the discharge OC 2 cool-down time. 2'b00: 100ms 2'b01: 200ms 2'b10: 500ms 2'b11: 1s	R/W	0x0 (MTP)	N/A
FT2_CFG: 0x63	Bits[7:6]: OC2_DCHG_ RETRY	Sets the number of discharge OC 2 reconnection attempts. 2'b00: 1 time 2'b01: 2 times 2'b10: 3 times 2'b11: Keep trying	R/W	0x0 (MTP)	LSB: 1 attempt 0x0: 1 attempt
FT2_CFG: 0x63	Bits[9:8]: OC_CHG_COOL	Sets the charge OC cool-down time. 2'b00: 100ms 2'b01: 200ms 2'b10: 500ms 2'b11: 1s	R/W	0x0 (MTP)	N/A
FT2_CFG: 0x63	Bits[11:10]: OC_CHG_RETRY	Sets the number of charge OC reconnection attempts. 2'b00: 1 time 2'b01: 2 times 2'b10: 3 times 2'b11: Keep trying	R/W	0x0 (MTP)	N/A

ADC

Address Name and Location	Field Bit Position and Name	Description	Type	Value Reset (OTP/MTP)	Encoding, LSB and Range
RD_VPACKP: 0x69	Bits[14:0]: VPACK_V	Returns the PACKP high-resolution voltage reading.	Read-only	0x0000	LSB: 0.002441V RNG: 0V to 79.9976V 0x0000: 0V
RD_VTOP: 0x6A	Bits[14:0]: VTOP_V	Returns the VTOP high-resolution voltage reading.	Read-only	0x0000	LSB: 0.002441V RNG: 0V to 79.9976V 0x0000: 0V

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RD_ITOP: 0x6B	Bits[15:0]: VTOP_I	Returns the battery pack current reading (synchronous to VTOP_V). Signed short integer, and ranges from -32768 to +32767.	Read-only	0x0000	LSB: 0.00305176mV RNG: -100mV to +99.997mV 0x0000: 0mV
RD_VCELL1: 0x6C	Bits[14:0]: CELL_1_V	Returns the cell 1 high-resolution reading.	Read-only	0x0000	LSB: 0.15259mV RNG: 0mV to 4999.85mV 0x0000: 0mV
RD_VCELL2: 0x6E	Bits[14:0]: CELL_2_V	Returns the cell 2 high-resolution reading.	Read-only	0x0000	LSB: 0.15259mV RNG: 0mV to 4999.85mV 0x0000: 0mV
RD_VCELL3: 0x70	Bits[14:0]: CELL_3_V	Returns the cell 3 high-resolution reading.	Read-only	0x0000	LSB: 0.15259mV RNG: 0mV to 4999.85mV 0x0000: 0mV
RD_VCELL4: 0x72	Bits[14:0]: CELL_4_V	Returns the cell 4 high-resolution reading.	Read-only	0x0000	LSB: 0.15259mV RNG: 0mV to 4999.85mV 0x0000: 0mV
RD_VCELL5: 0x74	Bits[14:0]: CELL_5_V	Returns the cell 5 high-resolution reading.	Read-only	0x0000	LSB: 0.15259mV RNG: 0mV to 4999.85mV 0x0000: 0mV
RD_VCELL6: 0x76	Bits[14:0]: CELL_6_V	Returns the cell 6 high-resolution reading.	Read-only	0x0000	LSB: 0.15259mV RNG: 0mV to 4999.85mV 0x0000: 0mV
RD_VCELL7: 0x78	Bits[14:0]: CELL_7_V	Returns the cell 7 high-resolution reading.	Read-only	0x0000	LSB: 0.15259mV RNG: 0mV to 4999.85mV 0x0000: 0mV
RD_VCELL8: 0x7A	Bits[14:0]: CELL_8_V	Returns the cell 8 high-resolution reading.	Read-only	0x0000	LSB: 0.15259mV RNG: 0mV to 4999.85mV 0x0000: 0mV
RD_VCELL9: 0x7C	Bits[14:0]: CELL_9_V	Returns the cell 9 high-resolution reading.	Read-only	0x0000	LSB: 0.15259mV RNG: 0mV to 4999.85mV 0x0000: 0mV
RD_VCELL10: 0x7E	Bits[14:0]: CELL_10_V	Returns the cell 10 high-resolution reading.	Read-only	0x0000	LSB: 0.15259mV RNG: 0mV to 4999.85mV 0x0000: 0mV
RD_VCELL11: 0x80	Bits[14:0]: CELL_11_V	Returns the cell 11 high-resolution reading.	Read-only	0x0000	LSB: 0.15259mV RNG: 0mV to 4999.85mV 0x0000: 0mV

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RD_VCELL12: 0x82	Bits[14:0]: CELL_12_V	Returns the cell 12 high-resolution reading.	Read-only	0x0000	LSB: 0.15259mV RNG: 0mV to 4999.85mV 0x0000: 0mV
RD_VCELL13: 0x84	Bits[14:0]: CELL_13_V	Returns the cell 13 high-resolution reading.	Read-only	0x0000	LSB: 0.15259mV RNG: 0mV to 4999.85mV 0x0000: 0mV
RD_VCELL14: 0x86	Bits[14:0]: CELL_14_V	Returns the cell 14 high-resolution reading.	Read-only	0x0000	LSB: 0.15259mV RNG: 0mV to 4999.85mV 0x0000: 0mV
RD_VCELL15: 0x88	Bits[14:0]: CELL_15_V	Returns the cell 15 high-resolution reading.	Read-only	0x0000	LSB: 0.15259mV RNG: 0mV to 4999.85mV 0x0000: 0mV
RD_VCELL16: 0x8A	Bits[14:0]: CELL_16_V	Returns the cell 16 high-resolution reading.	Read-only	0x0000	LSB: 0.15259mV RNG: 0mV to 4999.85mV 0x0000: 0mV
RD_VNTC4: 0x8C	Bits[14:0]: NTC4_HIRES_V	Returns the NTC4 high-resolution voltage ADC reading. This reading is ratiometric to NTCB, which has a 3.3V nominal value.	Read-only	0x0000	LSB: 0.00305176% of NTCB RNG: 0% to 99.99695% of NTCB 0x0000: 0% of NTCB
RD_VNTC3: 0x8D	Bits[14:0]: NTC3_HIRES_V	Returns the NTC3 high-resolution voltage ADC reading. This reading is ratiometric to NTCB, which has a 3.3V nominal value.	Read-only	0x0000	LSB: 0.00305176% of NTCB RNG: 0% to 99.99695% of NTCB 0x0000: 0% of NTCB
RD_VNTC2: 0x8E	Bits[14:0]: NTC2_HIRES_V	Returns the NTC2 high-resolution voltage ADC reading. This reading is ratiometric to NTCB, which has a 3.3V nominal value.	Read-only	0x0000	LSB: 0.00305176% of NTCB RNG: 0% to 99.99695% of NTCB 0x0000: 0% of NTCB
RD_VNTC1: 0x8F	Bits[14:0]: NTC1_HIRES_V	Returns the NTC1 high-resolution voltage ADC reading. This reading is ratiometric to NTCB, which has a 3.3V nominal value.	Read-only	0x0000	LSB: 0.00305176% of NTCB RNG: 0% to 99.99695% of NTCB 0x0000: 0% of NTCB
RD_VGPIO3: 0x90	Bits[14:0]: GPIO3_ VOLTAGE	Returns the GPIO3 high-resolution voltage reading.	Read-only	0x0000	LSB: 0.1007mV RNG: 0mV to 3299.9mV 0x0000: 0mV

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RD_VGPIO2: 0x91	Bits[14:0]: GPIO2_ VOLTAGE	Returns the GPIO2 high-resolution voltage reading.	Read-only	0x0000	LSB: 0.1007mV RNG: 0mV to 3299.9mV 0x0000: 0mV
RD_VGPIO1: 0x92	Bits[14:0]: GPIO1_ VOLTAGE	Returns the GPIO1 high-resolution voltage reading.	Read-only	0x0000	LSB: 0.1007mV RNG: 0mV to 3299.9mV 0x0000: 0mV
RD_TDIE: 0x93	Bits[14:0]: DIE_T_ VOLTAGE	Returns the die temperature high-resolution reading, which is proportional to the internal die temperature. The temperature can be calculated with the following equation: T = Reading x 0.01481 - 269.12°C	Read-only	0x0000	LSB: 0.01481°C RNG: -269.12°C to +216.16°C 0x4D93: 25°C
ADC_STS: 0x98	Bits[9:8]: FSM_STS	This field reports the status of the feature command scheduler. 0x0: Free 0x1: Executing voltage ADC scan 0x2: Executing cell-balancing 0x3: Executing open-wire detection	Read-only	0x0	N/A
ADC_STS: 0x98	Bits[12:11]: INT_ SCHEDULER	This field reports the status of the internal scheduler. 0x0: Idle 0x1: Refreshing voltage protection reading 0x2: Ready for the feature command 0x3: Not allowed	Read-only	0x0	N/A
ADC_CTRL: 0x99	Bit[0]: ADC_SCAN_GO	Write 1 to this bit to start a high-resolution scan for all the selected channels.	R/W	0x0	1: Execute this function
ADC_CTRL: 0x99	Bit[1]: SCAN_DONE_ STS	Reports whether the high-resolution voltage scan status is complete (true) or not (false).	Read-only	0x0	0: False 1: True
ADC_CTRL: 0x99	Bit[2]: SCAN_ERROR_ STS	Reports whether an error has occurred when starting the high-resolution voltage scan (e.g. if open-wire detection is already running).	Read-only	0x0	0: False 1: True
TRIMG_IPCB: 0x9B	Bits[9:0]: I_PCB_GAIN_ VALUE	Current-sense PCB gain correction can compensate for sense resistors and SMT variation. The correction is applied to current ADC readings. It is not applied to short-circuit or OC detection. The encoding is in binary complement format, where LSB = 0.0244% and ranges between ±12.5%.	R/W (can lock to read-only)	0x000 (MTP)	LSB: 0.0244% RNG: -12.5% to +12.476%, 0x000: 0%
HR_SCAN0: 0x9C	Bit[0]: SCAN_VCELLS_ EN	Enables the cell readings to be updated during the high-resolution voltage ADC scan, according to the enable setting of each individual cell. When disabled, the cell readings are excluded from the high-resolution voltage ADC scan.	R/W (can lock to read-only)	0x1 (OTP)	0: Disabled 1: Enabled

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HR_SCAN0: 0x9C	Bit[1]: SCAN_VTOP_EN	Enables the VTOP reading to be updated during the high-resolution voltage ADC scan.	R/W (can lock to read-only)	0x1 (OTP)	0: Disabled 1: Enabled
HR_SCAN0: 0x9C	Bit[2]: SCAN_PACKP_EN	Enables the PACKP reading to be updated during the high-resolution voltage ADC scan.	R/W (can lock to read-only)	0x1 (OTP)	0: Disabled 1: Enabled
HR_SCAN0: 0x9C	Bit[3]: SCAN_GPIO_EN	Enables GPIO readings to be updated during the high-resolution voltage ADC scan, according to each individual GPIO enable setting.	R/W (can lock to read-only)	0x1 (OTP)	0: Disabled 1: Enabled
HR_SCAN0: 0x9C	Bit[4]: SCAN_NTCS_EN	Enables the NTCs scan to be updated during the high-resolution voltage ADC scan, according to the enable setting of each individual NTC channel.	R/W (can lock to read-only)	0x1 (OTP)	0: Disabled 1: Enabled
HR_SCAN0: 0x9C	Bit[5]: SCAN_DIE_T	Enables the die temperature to be updated during the high-resolution voltage ADC scan.	R/W (can lock to read-only)	0x1 (OTP)	0: Disabled 1: Enabled
HR_SCAN0: 0x9C	Bit[9]: VTOP_SYNC_EN	Enables the battery pack current reading that is synchronous with the VTOP reading to be updated during the high-resolution voltage ADC scan. When disabled, the synchronous VTOP current reading cannot be updated.	R/W (can lock to read-only)	0x1 (OTP)	0: Disabled 1: Enabled
HR_SCAN0: 0x9C	Bit[11]: CELL_1K_COMP	Enables ADC cell measurement compensation for the voltage drop caused by the cell input resistor, R_{CELL_FILTER}. This configuration should be enabled when the input filter resistor exceeds 500Ω. For R_{CELL_FILTER} values below 500Ω, this should be disabled.	R/W	0x0 (OTP)	0: Disabled 1: Enabled
HR_SCAN1: 0x9D	Bit[0]: CELL_1_V_READ_EN	Enables the cell 1 high-resolution voltage. Effective when SCAN_VCELLS_EN is enabled.	R/W	0x1 (OTP)	0: Disabled 1: Enabled
HR_SCAN1: 0x9D	Bit[1]: CELL_2_V_READ_EN	Enables the cell 2 high-resolution voltage. Effective when SCAN_VCELLS_EN is enabled.	R/W	0x1 (OTP)	0: Disabled 1: Enabled
HR_SCAN1: 0x9D	Bit[2]: CELL_3_V_READ_EN	Enables the cell 3 high-resolution voltage. Effective when SCAN_VCELLS_EN is enabled.	R/W	0x1 (OTP)	0: Disabled 1: Enabled
HR_SCAN1: 0x9D	Bit[3]: CELL_4_V_READ_EN	Enables the cell 4 high-resolution voltage. Effective when SCAN_VCELLS_EN is enabled.	R/W	0x1 (OTP)	0: Disabled 1: Enabled
HR_SCAN1: 0x9D	Bit[4]: CELL_5_V_READ_EN	Enables the cell 5 high-resolution voltage. Effective when SCAN_VCELLS_EN is enabled.	R/W	0x1 (OTP)	0: Disabled 1: Enabled
HR_SCAN1: 0x9D	Bit[5]: CELL_6_V_READ_EN	Enables the cell 6 high-resolution voltage. Effective when SCAN_VCELLS_EN is enabled.	R/W	0x1 (OTP)	0: Disabled 1: Enabled
HR_SCAN1: 0x9D	Bit[6]: CELL_7_V_READ_EN	Enables the cell 7 high-resolution voltage. Effective when SCAN_VCELLS_EN is enabled.	R/W	0x1 (OTP)	0: Disabled 1: Enabled

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HR_SCAN1: 0x9D	Bit[7]: CELL_8_V_ READ_EN	Enables the cell 8 high-resolution voltage. Effective when SCAN_VCELLS_EN is enabled.	R/W	0x1 (OTP)	0: Disabled 1: Enabled
HR_SCAN1: 0x9D	Bit[8]: CELL_9_V_ READ_EN	Enables the cell 9 high-resolution voltage. Effective when SCAN_VCELLS_EN is enabled.	R/W	0x1 (OTP)	0: Disabled 1: Enabled
HR_SCAN1: 0x9D	Bit[9]: CELL_10_V_ READ_EN	Enables the cell 10 high-resolution voltage. Effective when SCAN_VCELLS_EN is enabled.	R/W	0x1 (OTP)	0: Disabled 1: Enabled
HR_SCAN1: 0x9D	Bit[10]: CELL_11_V_ READ_EN	Enables the cell 11 high-resolution voltage. Effective when SCAN_VCELLS_EN is enabled.	R/W (can lock to read-only)	0x1 (OTP)	0: Disabled 1: Enabled
HR_SCAN1: 0x9D	Bit[11]: CELL_12_V_ READ_EN	Enables the cell 12 high-resolution voltage. Effective when SCAN_VCELLS_EN is enabled.	R/W (can lock to read-only)	0x1 (OTP)	0: Disabled 1: Enabled
HR_SCAN1: 0x9D	Bit[12]: CELL_13_V_ READ_EN	Enables the cell 13 high-resolution voltage. Effective when SCAN_VCELLS_EN is enabled.	R/W (can lock to read-only)	0x1 (OTP)	0: Disabled 1: Enabled
HR_SCAN1: 0x9D	Bit[13]: CELL_14_V_ READ_EN	Enables the cell 14 high-resolution voltage. Effective when SCAN_VCELLS_EN is enabled.	R/W (can lock to read-only)	0x1 (OTP)	0: Disabled 1: Enabled
HR_SCAN1: 0x9D	Bit[14]: CELL_15_V_ READ_EN	Enables the cell 15 high-resolution voltage. Effective when SCAN_VCELLS_EN is enabled.	R/W (can lock to read-only)	0x1 (OTP)	0: Disabled 1: Enabled
HR_SCAN1: 0x9D	Bit[15]: CELL_16_V_ READ_EN	Enables the cell 16 high-resolution voltage. Effective when SCAN_VCELLS_EN is enabled.	R/W (can lock to read-only)	0x1 (OTP)	0: Disabled 1: Enabled
HR_SCAN2: 0x9E	Bit[0]: GPIO1_READ_ EN	Enables the GPIO1 high-resolution voltage. Effective when SCAN_GPIO_EN is enabled.	R/W (can lock to read-only)	0x0 (OTP)	0: Disabled 1: Enabled
HR_SCAN2: 0x9E	Bit[1]: GPIO2_READ_ EN	Enables the GPIO2 high-resolution voltage. Effective when SCAN_GPIO_EN is enabled.	R/W (can lock to read-only)	0x0 (OTP)	0: Disabled 1: Enabled
HR_SCAN2: 0x9E	Bit[2]: GPIO3_READ_ EN	Enables the GPIO3 high-resolution voltage. Effective when SCAN_GPIO_EN is enabled.	R/W (can lock to read-only)	0x0 (OTP)	0: Disabled 1: Enabled
HR_SCAN2: 0x9E	Bit[5]: NTC1_READ_ EN	Enables the NTC1 high-resolution voltage scan. Effective when SCAN_NTCS_EN is enabled.	R/W (can lock to read-only)	0x0 (OTP)	0: Disabled 1: Enabled
HR_SCAN2: 0x9E	Bit[6]: NTC2_READ_ EN	Enables the NTC2 high-resolution voltage scan. Effective when SCAN_NTCS_EN is enabled.	R/W (can lock to read-only)	0x0 (OTP)	0: Disabled 1: Enabled
HR_SCAN2: 0x9E	Bit[7]: NTC3_READ_ EN	Enables the NTC3 high-resolution voltage scan. Effective when SCAN_NTCS_EN is enabled.	R/W (can lock to read-only)	0x0 (OTP)	0: Disabled 1: Enabled
HR_SCAN2: 0x9E	Bit[8]: NTC4_READ_ EN	Enables the NTC4 high-resolution voltage scan. Effective when SCAN_NTCS_EN is enabled.	R/W (can lock to read-only)	0x0 (OTP)	0: Disabled 1: Enabled

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Communication

Address Name and Location	Field Bit Position and Name	Description	Type	Value Reset (OTP/MTP)	Encoding, LSB and Range
SILC_INFO1: 0xA0	Bits[5:0]: XFR_NUM_RD_WORDS	When CRC is enabled, this register defines the size of the readback in words before appending a CRC. After each read transaction, this bit self-resets back to 2 bytes. 6'b000001: 1 word / 2 bytes 6'b111111: 63 words / 126 bytes	R/W	0x01	LSB: 1 word, RNG: 1 to 63 words 0x00: 0 words
COMM_CFG: 0xA3	Bit[2]: USE_COMM_CRC	Enables the use of CRC over the communication protocol.	R/W (can lock to Read-only)	0x0 (OTP)	0: Disabled 1: Enabled
COMM_CFG: 0xA3	Bits[14:8]: DEVICE_ADD	Sets the configurable device address.	R/W (can lock to read-only)	0x01 (MTP)	N/A

Cell-Balancing

Address Name and Location	Field Bit Position and Name	Description	Type	Value Reset (OTP/MTP)	Encoding, LSB and Range
BAL_STS: 0xA4	Bit[0]: BALANCING_ACTIVE	Reports whether cell-balancing is currently ongoing.	Read-only	0x0	0: False 1: True
BAL_STS: 0xA4	Bits[6:1]: AUTO_BALANCING_COUNT_STS	Shows the number of balancing cycles that are actually performed. To be valid, BAL_DONE must be set to true. If any balancing cycle is skipped, the reason can be verified by reading AUTO_BAL_SKIPPED_HOT, AUTO_BAL_SKIPPED_DISCHARGE, AUTO_BAL_SKIPPED_STANDBY, or AUTO_BAL_SKIPPED_CHARGE. This register is not updated when AUTO_BAL_ALWAYS is enabled.	Read-only	0x00	N/A
BAL_STS: 0xA4	Bit[7]: AUTO_BAL_SKIPPED_CHARGE	When true, balancing cycles were skipped due to a detected charge current.	Read-only	0x0	0: False 1: True
BAL_STS: 0xA4	Bit[8]: AUTO_BAL_SKIPPED_STANDBY	When true, balancing cycles were skipped due to a detected standby current.	Read-only	0x0	0: False 1: True
BAL_STS: 0xA4	Bit[9]: AUTO_BAL_SKIPPED_DISCHARGE	When true, balancing cycles were skipped due to a detected discharge current.	Read-only	0x0	0: False 1: True
BAL_STS: 0xA4	Bit[10]: AUTO_BAL_SKIPPED_HOT	When true, balancing cycles were skipped due to the die temperature being too hot.	Read-only	0x0	0: False 1: True
BAL_LIST: 0xA5	Bit[0]: CELL_1_TO_BALANCE	When true, cell 1 will be balanced during the next balancing session. When false, cell 1 is skipped.	R/W	0x0	0: False 1: True

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BAL_LIST: 0xA5	Bit[1]: CELL_2_TO_ BALANCE	When true, cell 2 will be balanced during the next balancing session. When false, cell 2 is skipped.	R/W	0x0	0: False 1: True
BAL_LIST: 0xA5	Bit[2]: CELL_3_TO_ BALANCE	When true, cell 3 will be balanced during the next balancing session. When false, cell 3 is skipped.	R/W	0x0	0: False 1: True
BAL_LIST: 0xA5	Bit[3]: CELL_4_TO_ BALANCE	When true, cell 4 will be balanced during the next balancing session. When false, cell 4 is skipped.	R/W	0x0	0: False 1: True
BAL_LIST: 0xA5	Bit[4]: CELL_5_TO_ BALANCE	When true, cell 5 will be balanced during the next balancing session. When false, cell 5 is skipped.	R/W	0x0	0: False 1: True
BAL_LIST: 0xA5	Bit[5]: CELL_6_TO_ BALANCE	When true, cell 6 will be balanced during the next balancing session. When false, cell 6 is skipped.	R/W	0x0	0: False 1: True
BAL_LIST: 0xA5	Bit[6]: CELL_7_TO_ BALANCE	When true, cell 7 will be balanced during the next balancing session. When false, cell 7 is skipped.	R/W	0x0	0: False 1: True
BAL_LIST: 0xA5	Bit[7]: CELL_8_TO_ BALANCE	When true, cell 8 will be balanced during the next balancing session. When false, cell 8 is skipped.	R/W	0x0	0: False 1: True
BAL_LIST: 0xA5	Bit[8]: CELL_9_TO_ BALANCE	When true, cell 9 will be balanced during the next balancing session. When false, cell 9 is skipped.	R/W	0x0	0: False 1: True
BAL_LIST: 0xA5	Bit[9]: CELL_10_TO_ BALANCE	When true, cell 10 will be balanced during the next balancing session. If false, cell 10 is skipped.	R/W	0x0	0: False 1: True
BAL_LIST: 0xA5	Bit[10]: CELL_11_TO_ BALANCE	When true, cell 11 will be balanced during the next balancing session. When false, cell 11 is skipped.	R/W	0x0	0: False 1: True
BAL_LIST: 0xA5	Bit[11]: CELL_12_TO_ BALANCE	When true, cell 12 will be balanced during the next balancing session. When false, cell 12 is skipped.	R/W	0x0	0: False 1: True
BAL_LIST: 0xA5	Bit[12]: CELL_13_TO_ BALANCE	When true, cell 13 will be balanced during the next balancing session. When false, cell 13 is skipped.	R/W	0x0	0: False 1: True
BAL_LIST: 0xA5	Bit[13]: CELL_14_TO_ BALANCE	When true, cell 14 will be balanced during the next balancing session. When false, cell 14 is skipped.	R/W	0x0	0: False 1: True
BAL_LIST: 0xA5	Bit[14]: CELL_15_TO_ BALANCE	When true, cell 15 will be balanced during the next balancing session. When false, cell 15 is skipped.	R/W	0x0	0: False 1: True
BAL_LIST: 0xA5	Bit[15]: CELL_16_TO_ BALANCE	When true, cell 16 will be balanced during the next balancing session. When false, cell 16 is skipped.	R/W	0x0	0: False 1: True
BAL_CTRL: 0xA6	Bit[0]: BALANCE_GO	Controls the start for both manual and automatic cell-balancing. When set to on, balancing begins.	R/W	0x0	0: Off 1: On
BAL_CTRL: 0xA6	Bit[1]: BAL_DONE_ STS	Reports whether cell-balancing is completed.	Read-only	0x0	0: False 1: True
BAL_CTRL: 0xA6	Bit[2]: BAL_ERROR_ STS	Reports whether an error occurs when balancing starts (e.g. if open-wire detection is already running).	Read-only	0x0	0: False 1: True

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BAL_CFG: 0xA7	Bit[0]: BALANCE_ MODE_CTRL	This register is used only when automatic cell-balancing is enabled. This feature is only available on I²C versions. 0: Register control (BALANCE_GO) 1: GPIO3 control (the direction of GPIO3 is set as input, and the input type is set as digital input). When set to high, balancing begins	R/W	0x0 (OTP)	N/A
BAL_CFG: 0xA7	Bit[1]: BALANCE_ MODE_REG	Controls the cell-balancing mode. 0: Manual cell-balancing 1: Automatic cell-balancing	R/W (can lock to read-only)	0x0 (OTP)	N/A
BAL_CFG: 0xA7	Bit[2]: AUTO_BAL_ ALWAYS	This register is used only when automatic cell-balancing is enabled. When disabled, automatic cell-balancing uses BAL_REPETITION to control how many iterations the device repeats. When enabled, balancing continues until the balancing list is empty. To stop constant automatic cell-balancing before the balancing list is empty, change this bit to disabled.	R/W (can lock to read-only)	0x0 (OTP)	0: Disabled 1: Enabled
BAL_CFG: 0xA7	Bits[7:3]: BAL_ REPETITION	Sets the number of repetitions for each execution of the balancing list. When set to 31 repetitions, 32 balancing cycles are executed.	R/W	0x1F (OTP)	LSB: 1 repetition RNG: 0 to 31 repetitions, 0x00: 0 repetitions
BAL_THR: 0xA8	Bits[5:0]: CELL_BAL_MIN	Sets the qualifying minimum cell voltage to run automatic cell-balancing. When a cell is below this level, it is excluded from the balancing list, while other qualifying cells could be balanced if they meet applicable criteria.	R/W	0x21 (OTP)	LSB: 39mV RNG: 2500mV to 4961mV 0x00: 2500mV
BAL_THR: 0xA8	Bit[6]: ABAL_ON_ CHARGE	This register is used only when automatic cell-balancing is enabled. 0: Automatic balancing does not run when there is a charge current that exceeds the charge standby threshold 1: Automatic balancing can run when there is a charge current that exceeds the charge standby threshold	R/W	0x0	0: Disabled 1: Enabled
BAL_THR: 0xA8	Bit[7]: ABAL_ON_STBY	This register is used only when automatic cell-balancing is enabled. 0: Automatic balancing does not run when the current is between 0 and the standby threshold 1: Automatic balancing can run when the current is between 0 and the standby threshold	R/W	0x0	N/A

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BAL_THR: 0xA8	Bit[9]: STOP_ON_HOT	0: Don't suspend automatic cell-balancing if the silicon digital die temperature is too hot 1: Suspend automatic cell-balancing if the silicon digital die temperature is too hot	R/W	0x0	N/A
BAL_THR: 0xA8	Bits[12:10]: BAL_MSM_TH	The cell-balancing threshold used by the automatic cell-balancing algorithm.	R/W	0x2 (OTP)	LSB: 9.765mV RNG: 19.5mV to 87.85mV 0: 19.5mV

Memory Control

Address Name and Location	Field Bit Position and Name	Description	Type	Value Reset (OTP/MTP)	Encoding, LSB and Range
MEM_STATUS: 0xB4	Bits[5:3]: NVM_STATUS	Returns the thermometer-coded confirmation status of the NVM: 3'bxx1: NVM Page 1 has been fully configured, and the NVM-backed registers can be loaded and use CRC if enabled 3'bx1x: NVM Page 2 has been fully configured, and the NVM-backed registers can be loaded and use CRC if enabled 3'b1xx: NVM Page 3 has been fully configured, and the NVM-backed registers can be loaded and use CRC if enabled	Read-only	0x1	N/A
OTP_CRC_ STATUS: 0xB6	Bit[15]: OTP_CRC_ ERROR	Reports whether an OTP CRC error has been detected. It is set by a CRC error during OTP restoration, and is reset by the restore command.	Read-only	0x0	0: Not detected 1: Detected
NVM_CRC_ STATUS: 0xB7	Bit[15]: NVM_CRC_ERR OR	Reports whether an NVM CRC error has been detected. It is set by a CRC error during NVM restoration, and it is reset by the restore command.	Read-only	0x0	0: Not detected 1: Detected
OTP_STORE_ CMD: 0xB8	Bit[0]: RESERVED	Reserved. Do not change this register value.	R/W	0x0	N/A
OTP_STORE_ CMD: 0xB8	Bit[1]: RESERVED	Reserved. Do not change this register value.	R/W	0x0	N/A
OTP_STORE_ CMD: 0xB8	Bit[2]: RESERVED	Reserved. Do not change this register value.	R/W	0x0	N/A
OTP_STORE_ CMD: 0xB8	Bit[3]: STORE_NVM_ CMD	Store all NVM registers and the NVM CRC code in the OTP if STORE_CMD_ACCESS_CODE has been configured with the correct code. 1: Store all NVM registers and the NVM CRC code in the OTP. This is a self-clearing register	R/W	0x0	N/A

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OTP_STORE_CMD: 0xB8	Bit[4]: RESERVED	Reserved. Do not change this register value.	R/W	0x0	N/A
OTP_STORE_CMD: 0xB8	Bit[15]: STORE_IN_PROGRESS	Reports whether the store function is in progress. 0: Storage of register data to the MTP memory is not in progress 1: Storage of register data to the MTP memory is in progress	Read-only	0x0	N/A
STORE_CMD_ACCESS_CODE: 0xB9	Bits[15:0]: STORE_CMD_ACCESS_CODE	Before enabling the STORE_NVM_CMD command, 0xA5B6 must be written to this register to allow for the store command. This bit should be cleared once storage is complete.	R/W	0x0000	N/A

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LOCK REGISTER MAP

The MP2796 supports the configuration register lock function. This prevents critical safety settings from changing due to unforeseen circumstances

All of the bits in an address that are not populated by a register should be treated as reserved. The value of these reserved bits may be 0 or 1, and should be set to 0 when there are write operations changing other bits in the same address. Setting these reserved bits to 0 does not change the value of the reserved bits.

Once the lock bit is set to 1, it cannot be set to 0 unless the MP2796 is reset.

All of the locking bits support the MTP, and the default value is 0. If the lock bit in the MTP is set to 1, the corresponding setting register cannot be modified anymore. Before setting the MTP command, carefully consider whether to set the locking bit to 1.

Table 17 shows the lock register map.

Table 17: Lock Register Map

Register Location and Bit Position for Locking	Locked Address Name and Location	Locked Field Bit Position and Name
0xAA: Bit[15]	FET_MODE: 0x13	Bit[11]: CHG_SOFTON_OC_LIM Bit[9]: TURNON_TIMEOUT_FAULT Bit[8]: CHG_TURNON_TIMER
	FET_CFG: 0x14	Bits[14:12]: FET_DRV_LVL Bits[11:9]: CHG_SOFTON_PUP Bits[2:0]: DSG_SOFTON_DV
0xAA: Bit[14]	FET_MODE: 0x13	Bit[12]: P_FET_MANUAL Bit[3]: FET_ON_RUN_SC_DET_EN
0xAA: Bit[13]	WDT_CFG: 0x10	Bits[15:9]: WDT_BITE_CFG Bits[8:2]: WDT_BARK_CFG Bit[0]: WDT_COM_CTRL
0xAA: Bit[12]	PINS_CFG: 0x0D	Bit[8]: GPIO_LV_CFG Bit[6]: WDT_RST_EN Bit[5]: WDT_RPT Bit[0]: ALERT_POL
0xAA: Bit[11]	GPIO_CFG: 0x0C	Bit[11]: GPIO3_FSEL Bit[10]: GPIO3_PUP Bit[9]: GPIO3_TYPE Bit[8]: GPIO3_IO Bit[6]: GPIO2_PUP Bit[5]: GPIO2_TYPE Bit[4]: GPIO2_IO Bit[2]: GPIO1_PUP Bit[1]: GPIO1_TYPE Bit[0]: GPIO1_IO
0xAA: Bit[8]	RGL_CFG: 0x08	Bit[2]: V3P3_SHDN_EN
0xAA: Bit[6]	STB_CFG: 0x06	Bits[5:4]: STBY_MONITOR_CFG

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0xAA: Bit[5]	STB_CFG: 0x06	Bit[6]: STBY_PFET_EN
0xAA: Bit[3]	ACT_CFG: 0x05	Bit[9]: FT_STATE_SEL
0xAA: Bit[2]	ACT_CFG: 0x05	Bit[1]: FET_CFG
0xAA: Bit[1]	ACT_CFG: 0x05	Bit[0]: FET_SRC
0xAB: Bit[14]	HR_SCAN2: 0x9E	Bit[8]: NTC4_READ_EN Bit[7]: NTC3_READ_EN Bit[6]: NTC2_READ_EN Bit[5]: NTC1_READ_EN
0xAB: Bit[13]	HR_SCAN2: 0x9E	Bit[2]: GPIO3_READ_EN Bit[1]: GPIO2_READ_EN Bit[0]: GPIO1_READ_EN
0xAB: Bit[12]	HR_SCAN1: 0x9D	Bit[15]: CELL_16_V_READ_EN Bit[14]: CELL_15_V_READ_EN Bit[13]: CELL_14_V_READ_EN Bit[12]: CELL_13_V_READ_EN
0xAB: Bit[11]	TRIMG_IPCB: 0x9B	Bits[9:0]: I_PCB_GAIN_VALUE
0xAB: Bit[7]	DIE_CFG: 0x46	Bit[3]: DIE_TEMP_DIG_FAULT_EN
0xAB: Bit[6]	DIE_CFG: 0x46	Bit[1]: DIE_TEMP_DIG_EN
0xAB: Bit[4]	CELLFT_CTRL: 0x35	Bit[5]: CELL_OV_FAULT_EN Bit[2]: CELL_UV_FAULT_EN
0xAB: Bit[3]	PACKFT_CTRL: 0x34	Bit[12]: CELL_MSMT_FAULT_EN Bit[9]: CELL_DEAD_FAULT_EN Bit[5]: VTOP_OV_FAULT_EN_CTRL Bit[1]: VTOP_UV_FAULT_EN_CTRL
0xAB: Bit[2]	SCFT_CTRL: 0x2A	Bit[5]: SC_CHG_FAULT_EN Bit[4]: SC_DCHG_FAULT_EN Bit[1]: SC_CHG_EN_CTRL Bit[0]: SC_DCHG_EN_CTRL
0xAB: Bit[1]	OCFT_CTRL: 0x23	Bit[8]: OC_CHG_FAULT_EN Bit[7]: OC2_DCHG_FAULT_EN Bit[6]: OC1_DCHG_FAULT_EN Bit[2]: OC_CHG_EN_CTRL Bit[1]: OC2_DCHG_EN_CTRL Bit[0]: OC1_DCHG_EN_CTRL
0xAB: Bit[0]	INT0_EN: 0x19	Bit[15]: INT_ALERT_CTRL
0xAC: Bit[15]	COMM_CFG: 0xA3	Bits[14:8]: DEVICE_ADD
0xAC: Bit[14]	COMM_CFG: 0xA3	Bit[2]: USE_COMM_CRC
0xAC: Bit[13]	HR_SCAN1: 0x9D	Bit[11]: CELL_12_V_READ_EN Bit[10]: CELL_11_V_READ_EN
0xAC: Bit[11]	FET_MODE: 0x13	Bit[4]: CHG_SOFTON_EN Bit[0]: DSG_SOFTON_EN

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0xAC: Bit[10]	NTC_CFG: 0x47	Bit[15]: PCB_MNTR_FAULT_EN
0xAC: Bit[9]	NTC_CFG: 0x47	Bit[14]: NTC_CELL_COLD_FAULT_EN Bit[13]: NTC_CELL_HOT_FAULT_EN
0xAC: Bit[8]	NTC_CFG: 0x47	Bit[10]: NTCB_DYNAMIC_ON
0xAC: Bit[7]	NTC_CFG: 0x47	Bit[7]: NTC4_TYPE_SEL
0xAC: Bit[6]	NTC_CFG: 0x47	Bit[6]: NTC4_EN
0xAC: Bit[5]	NTC_CFG: 0x47	Bit[5]: NTC3_TYPE_SEL
0xAC: Bit[4]	NTC_CFG: 0x47	Bit[4]: NTC3_EN
0xAC: Bit[3]	NTC_CFG: 0x47	Bit[3]: NTC2_TYPE_SEL
0xAC: Bit[2]	NTC_CFG: 0x47	Bit[2]: NTC2_EN
0xAC: Bit[1]	NTC_CFG: 0x47	Bit[1]: NTC1_TYPE_SEL
0xAC: Bit[0]	NTC_CFG: 0x47	Bit[0]: NTC1_EN
0xAD: Bit[15]	CELL_UV: 0x38	Bits[11:8]: CELL_UV_DG Bits[7:0]: CELL_UV
0xAD: Bit[14]	CELL_OV: 0x39	Bits[11:8]: CELL_OV_DG Bits[7:0]: CELL_OV
0xAD: Bit[13]	NTCC_OTHR_DSG: 0x48	Bits[9:0]: NTC_CELL_HOT_DISCH
	NTCC_UTHR_DSG: 0x49	Bits[9:0]: NTC_CELL_COLD_DISCH
	NTCC_OTHR_CHG: 0x4A	Bits[9:0]: NTC_CELL_HOT_CHG
	NTCC_UTHR_CHG: 0x4B	Bits[15:11]: NTC_CELL_HYST Bits[9:0]: NTC_CELL_COLD_CHG
0xAD: Bit[10]	CELLS_CTRL: 0x00	Bits[3:0]: CELL_S_CTRL
0xAD: Bit[9]	SELF_CFG: 0x56	Bit[15]: OTP_FAULT_EN
0xAD: Bit[8]	SELF_CFG: 0x56	Bit[14]: 3V3_VDD_FAULT_EN
0xAD: Bit[7]	SELF_CFG: 0x56	Bit[10]: OPEN_WIRE_PON
0xAD: Bit[6]	SELF_CFG: 0x56	Bit[9]: OPEN_WIRE_FAULT_EN
0xAD: Bit[4]	SELF_CFG: 0x56	Bit[6]: OTP_CRC_EN
0xAD: Bit[3]	SELF_CFG: 0x56	Bit[3]: ADC_SELF_TEST_EN
0xAD: Bit[2]	SELF_CFG: 0x56	Bit[2]: VDD_EN
0xAD: Bit[1]	SELF_CFG: 0x56	Bit[1]: 3V3_EN
0xAD: Bit[0]	SELF_CFG: 0x56	Bit[0]: REGIN_EN
0xAE: Bit[15]	DSGSC_CFG: 0x2B	Bits[14:8]: SC_DCHG_DG Bit[5]: SC_DCHG_RNG Bits[4:0]: SC_DCHG_LIM
0xAE: Bit[14]	CHGSC_CFG: 0x2C	Bits[14:8]: SC_CHG_DG Bit[5]: SC_CHG_RNG Bits[4:0]: SC_CHG_LIM
0xAE: Bit[13]	DSGOC_LIM: 0x24	Bit[13]: OC2_DCHG_RNG Bits[12:8]: OC2_DCHG_LIM

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	DSGOC_DEG: 0x25	Bit[14]: OC2_DCHG_DGL_RNG Bits[13:8]: OC2_DCHG_DGL
0xAE: Bit[12]	DSGOC_LIM: 0x24	Bit[5]: OC1_DCHG_RNG Bits[4:0]: OC1_DCHG_LIM
	DSGOC_DEG: 0x25	Bit[6]: OC1_DCHG_DGL_RNG Bits[5:0]: OC1_DCHG_DGL
0xAE: Bit[11]	CHGOC_DEG: 0x26	Bit[14]: OC_CHG_DGL_RNG Bits[13:8]: OC_CHG_DG Bit[5]: OC_CHG_RNG Bits[4:0]: OC_CHG_LIM
0xAE: Bit[9]	FT_REC: 0x60	Bit[12]: DIE_TEMP_FAULT_REC
0xAE: Bit[8]	FT_REC: 0x60	Bit[10]: SC_CHG_REC
0xAE: Bit[7]	FT_REC: 0x60	Bit[9]: SC_DCHG_REC
0xAE: Bit[6]	FT_REC: 0x60	Bit[8]: OC_CHG_REC
0xAE: Bit[5]	FT_REC: 0x60	Bit[7]: OC2_DCHG_REC
0xAE: Bit[4]	FT_REC: 0x60	Bit[6]: OC1_DCHG_REC
0xAE: Bit[2]	FT_REC: 0x60	Bit[4]: PCB_MNTR_REC
0xAE: Bit[1]	FT0_CFG: 0x61	Bit[11]: CELL_OV_REC Bit[7]: CELL_UV_REC
0xAE: Bit[0]	FT_REC: 0x60	Bit[2]: NTC_CELL_CHG_REC Bit[1]: NTC_CELL_DCHG_REC
0xAF: Bit[6]	FT0_CFG: 0x61	Bit[9]: CELL_OV_LOGIC_SEL
0xAF: Bit[3]	FT0_CFG: 0x61	Bit[5]: CELL_UV_LOGIC_SEL
0xB0: Bit[15]	PACKFT_CTRL: 0x34	Bit[8]: CELL_DEAD_EN
0xB0: Bit[13]	CELLFT_CTRL: 0x35	Bit[4]: CELL_OV_EN_CTRL Bit[1]: CELL_UV_EN_CTRL
0xB0: Bit[11]	BAL_CFG: 0xA7	Bit[2]: AUTO_BAL_ALWAYS
0xB0: Bit[10]	BAL_CFG: 0xA7	Bit[1]: BALANCE_MODE_REG
0xB0: Bit[9]	BAL_CFG: 0xA7	Bit[0]: BALANCE_MODE_CTRL (I^2C versions only)

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APPLICATION INFORMATION

PCB Layout Guidelines

Proper PCB layout is critical to reduce noise, and to optimize the device's accuracy and reliability. For the best results, refer to Figure 19, Figure 20, and Figure 21, and follow the guidelines below:

1. Route the ground plane such that it reduces ground noise and prevents stray current (see Figure 19).

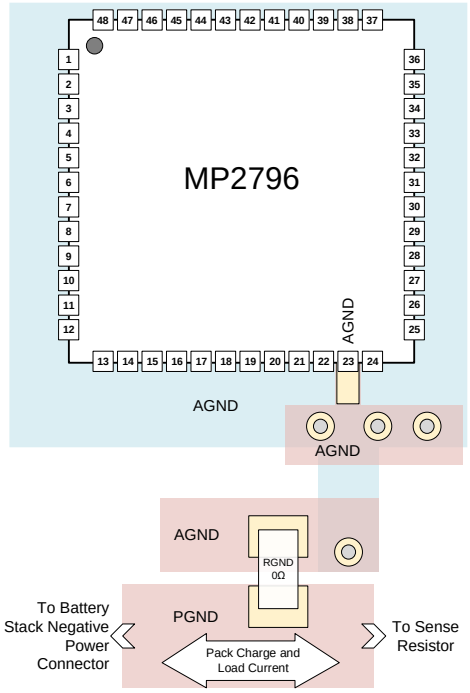

Figure 19: Recommended Layout for AGND

2. Connect the AGND pin to a dedicated ground plane. Then connect the AGND plane to the negative terminal of the battery stack via a 0Ω resistor.
3. Review the schematic and layout to ensure that each component is connected to the correct ground (power vs. signal). For example, the diodes protecting the different power terminals should be connected to PGND.
4. Consider the expected maximum peak load current, then check the PGND length, width, and thickness to ensure that there is an appropriate low-resistance path that prevents voltage drops.
5. The REGIN, VDD, VREF, 3V3, and NTCB pins require external decoupling capacitors, which should be placed as close as possible to each pin. Minimize the trace inductance from these pins to AGND (see Figure 20).

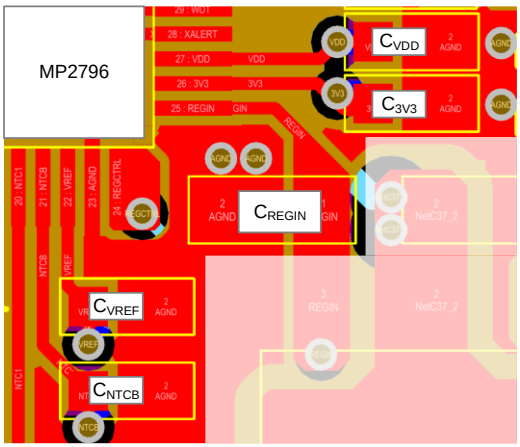

Figure 20: Recommended Layout for Decoupling Capacitors

6. Consider Kelvin connections at the sense resistor. A sense resistor with a dedicated sensing pad is ideal. A simple two-terminal sense resistor can be used in a 4-wire sensing configuration (see Figure 21).
7. Route the sensing signals to SRP and SRN in parallel to avoid coupling interfering signals.

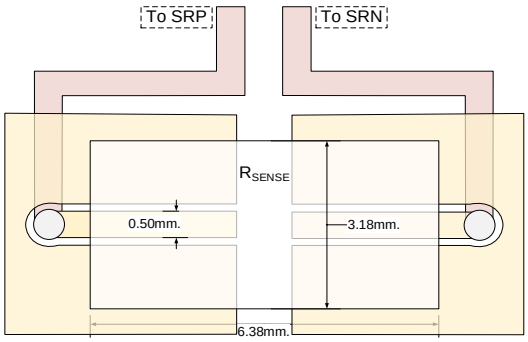

Figure 21: 2512 Sense Resistor using 4-Wire Footprint

8. Connect the temperature sensors (NTCx) to AGND using the star connection technique to avoid contaminating the voltage reading with the resistive voltage drop caused by the load or charging ground current.
9. Route the two wires connecting the NTCx pins together in twisted pairs to avoid coupling interfering signals. This is recommended if NTCx is located off-board.

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TYPICAL APPLICATION CIRCUIT

Figure 22 shows the typical external components and connections required to interface the MP2796 to the battery pack and the system.

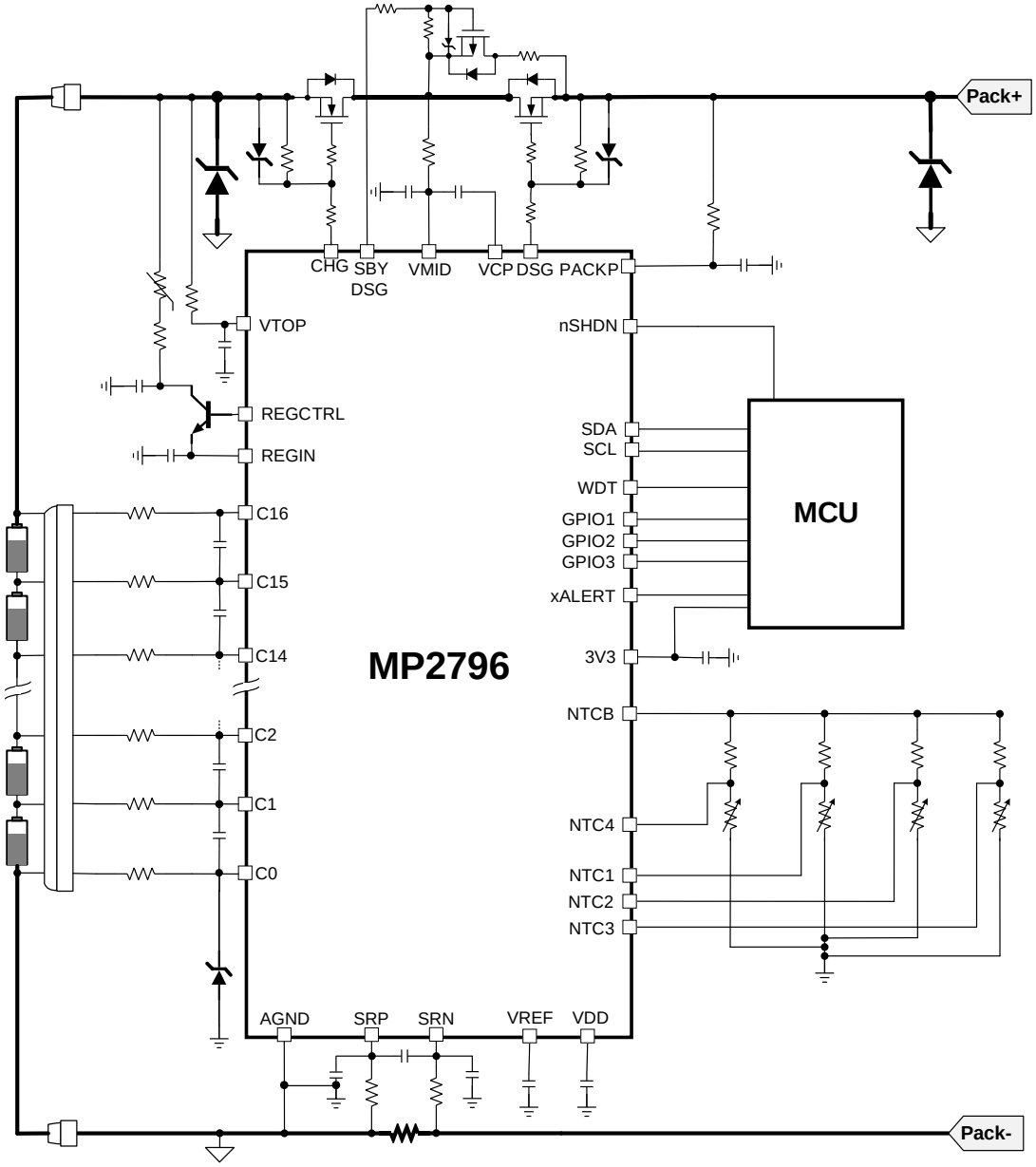

Figure 22: Typical Application Circuit for the MP2796

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Recommended External Components

Figure 23 shows a detailed view of all of the typical recommended external components.

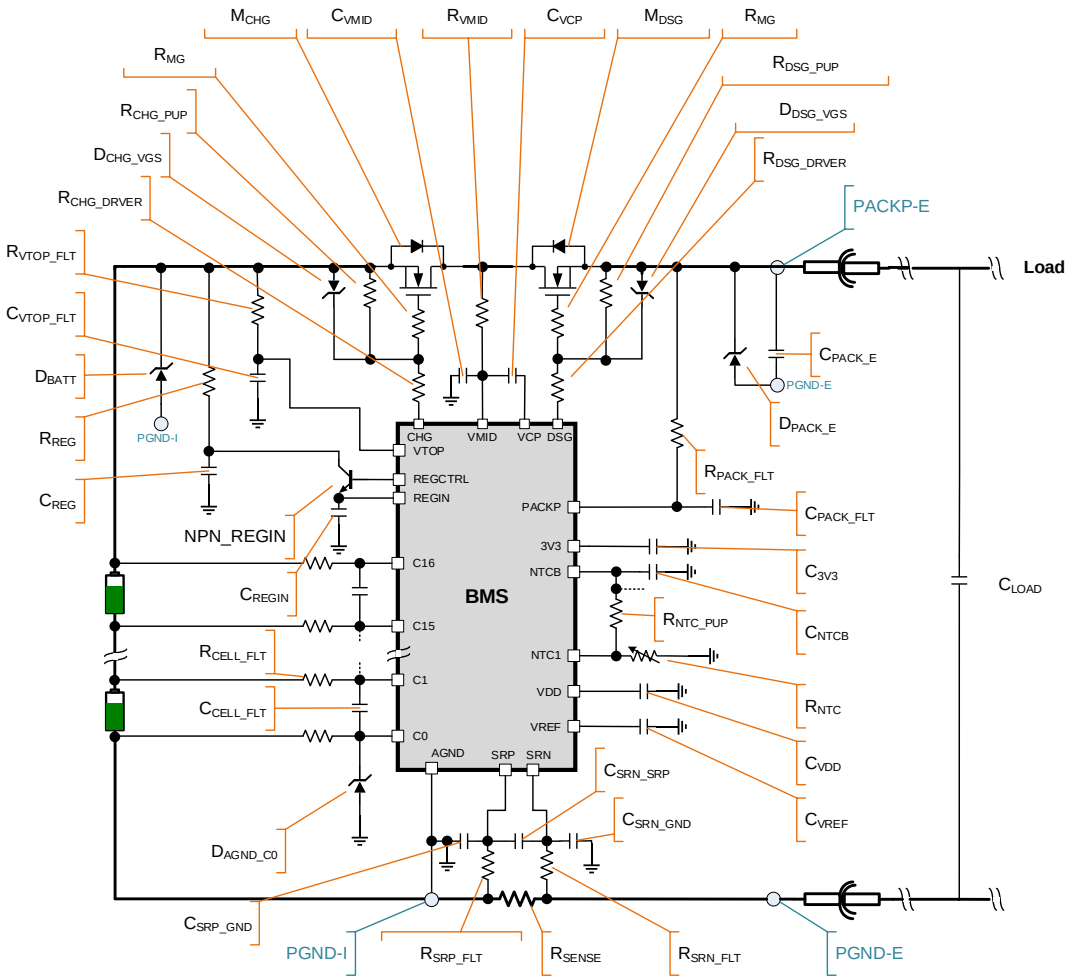

Figure 23: Recommended External Component Diagram

Table 18 on page 118 provides guidance regarding which parameters should be evaluated when selecting each BOM component (see the Configuration for External or Internal Cell-Balancing section on page 120 for more details on cell-balancing). Refer to the MP2796 evaluation board datasheet to see each BOM component.

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Table 18: Recommended Components

Parameter Identifier	Parameter Description	Component Description	Parameter Comments	Min	Typ	Max	Unit
General							
D_{AGND_C0}	Recommended Zener diode voltage rating	AGND-C0 Zener diode voltage			3.3		V
C_{PACK_E}	Capacitance value	External pack capacitor			47	200	µF
Pin Filtering							
C_{VTOP_FLT}	Required capacitance	VTOP-filtering capacitor			470		nF
R_{VTOP_FLT}	Required resistance	VTOP-filtering resistor			20		Ω
C_{PACK_FLT}	Required capacitance	PACKP-filtering capacitor	Do not use a capacitor larger or smaller than the recommended value		10		nF
R_{PACK_FLT}	Required resistance	PACKP-filtering resistor			100		Ω
R_{VMID}	Required resistance	VMID-filtering resistor			100		Ω
Cell Voltage Sensing							
C_{CELL_FLT}	Required capacitance	Cell-filtering capacitor			100		nF
R_{CELL_FLT}	Required resistance	Cell-filtering resistor		20	100		Ω
N-Channel MOSFET Driver							
$D_{CHG\text{-}VGS}$	Recommended Zener diode voltage rating	Diode CHG V_{GS} protection	For a CHG N-channel MOSFET with a ±20V maximum V_{GS}. If the CHG N-channel MOSFET has a smaller V_{GS}, decrease the Zener voltage value accordingly.		16		V
$D_{DSG\text{-}VGS}$	Recommended Zener diode voltage rating	Diode DSG V_{GS} protection	For a DSG N-channel MOSFET with a ±20V maximum V_{GS}. If the DSG N-channel MOSFET has a smaller V_{GS}, decrease the Zener voltage value accordingly.		16		V
R_{CHG_PUP}	Recommended resistance	Charge N-channel MOSFET pull-up resistor			10		MΩ
R_{DSG_PUP}	Recommended resistance	Discharge N-channel MOSFET pull-up resistor			10		MΩ
R_{CHG_DRVER}	Required resistance	N-channel MOSFET charge driver protection resistor			100		Ω
R_{DSG_DRVER}	Required resistance	N-channel MOSFET discharge driver protection resistor			100		Ω
R_{MG}	Required resistance	N-channel MOSFET gate protection resistor			100		Ω
Current Sensing							
R_{SRN_FLT}	Recommended resistance	SRN filtering resistor			100		Ω
C_{SRN_GND}	Recommended capacitance	SRN-GND filtering capacitor			100		nF

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C_{SRN_SRP}	Recommended capacitance	SRN/P differential filtering capacitor			100		nF
R_{SRP_FLT}	Recommended resistance	SRP filtering resistor			100		Ω
C_{SRP_GND}	Recommended capacitance	SRP-GND filtering capacitor			100		nF
R_{SENSE}	Recommended resistance	Pack current-sense resistor	The min and max values are recommended, and are based on the current-sense range.	0.2	2	5	mΩ
Regulators							
C_{3V3}	Required capacitance	3.3V capacitor		0.47	1	10	µF
C_{VCP}	Required capacitance	VCP-VMID capacitor			47		nF
	Required voltage rating		The rating can be proportionally reduced if fewer than 16 stacked cells are used.	80			V
C_{VDD}	Required capacitance	VDD bypass capacitor			1		µF
C_{VMID}	Required capacitance	VMID bypass capacitor			100		nF
C_{VREF}	Required capacitance	VREF bypass capacitor			1		µF
C_{REGIN}	Required capacitance	REGIN capacitor			3.3		µF
C_{REG}	Required capacitance	Regulator capacitor			1		µF
R_{REG}	Regulator-limiting resistor value	Regulator-limiting resistor value			500		Ω
Temperature Sensing							
R_{NTC_PUP}	Typical resistance	NTC pull-up	This is a typical value. Generally, the NTC pull-up value should match the NTC thermistor value at 25°C.		10		kΩ
R_{NTC}	Typical resistance	NTC thermistor	If a smaller resistance is used, the NTCB current limit should be evaluated and compared to the total resistance connected to the NTCB in the worst-case scenario (hot temperatures).		10		kΩ
C_{NTCB}	NTCB capacitance	NTCB capacitor				10	nF

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Configuration for External or Internal Cell-Balancing

Cell-balancing can be implemented via the internal balancing MOSFETs for up to 58mA. Higher cell-balancing current is possible with external MOSFETs or BJTs (see Figure 28).

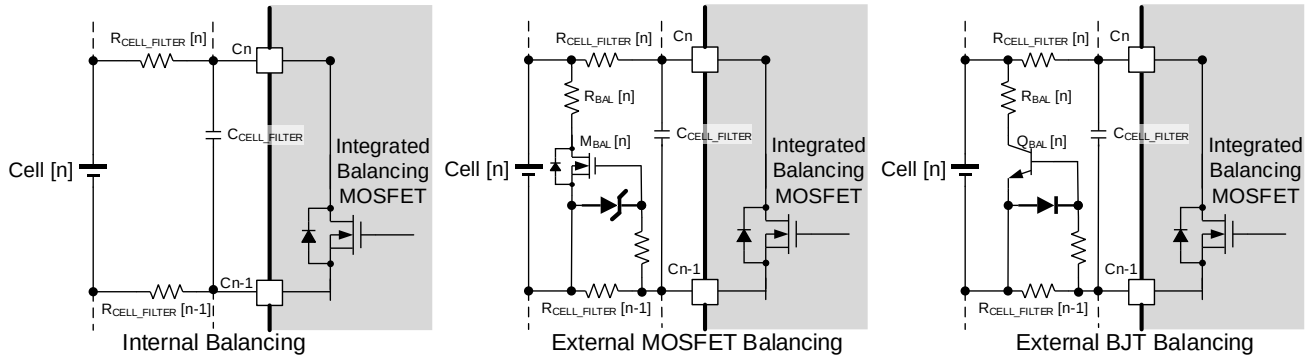

Figure 28: Typical Schematics Internal vs. External Balancing Configurations

The following section describes the recommended components for each of these 3 balancing configurations.

Table 19 recommends specific components for internal MOSFET balancing.

Table 19: Recommended Component Selection for Internal MOSFET Balancing

Parameter Identifier	Parameter Description	Component Description	Notes	Min	Typ	Max	Unit
C_{CELL_FILTER}	Required capacitance	Cell-filtering capacitor	Internal balancing configuration. If R_{CELL_FILTER} increases, C_{CELL_FILTER} should be proportionally decreased.		100		nF
R_{CELL_FILTER}	Required resistance	Cell-filtering resistor	Resistance for the internal balancing configuration.	20	100		Ω

The amount of current provided in an internal balancing configuration is easily derived by following the R_{CELL_FILTER} resistor value and considering the integrated MOSFET balancing resistance ($R_{DS(ON)_BAL_FET}$). For example, for a lithium cell at 4V where R_{CELL_FILTER} = 20Ω, the resistive path allows for 58mA once the integrated balancing resistor MOSFET is enabled.

For higher balancing current, Table 20 and Table 21 on page 121 provide guidance on selecting the MOSFET or BJT circuit components.

Table 20 recommends specific components for external MOSFET balancing.

Table 20: Recommended Component Selection for External MOSFET Balancing

Parameter Identifier	Parameter Description	Component Description	Notes	Min	Typ	Max	Unit
C_{CELL_FILTER}	Required capacitance	Cell-filtering capacitor	Capacitance for external balancing configuration. If R_{CELL_FILTER} increases, C_{CELL_FILTER} should be proportionally decreased.		10		nF
R_{CELL_FILTER}	Required resistance	Cell-filtering resistor	Resistance for external balancing configuration. If R_{CELL_FILTER} increases, C_{CELL_FILTER} should be proportionally decreased.	800	1000		Ω
R_{BAL}	Required resistance	Cell-balancing current-limiting resistor	Adjust this value to set the balancing current, and verify the power dissipation compared to package limit.		43		Ω
V_{TH_MBAL}	MOSFET V_{GS} threshold	External balancing MOSFET M_{BAL}	A higher voltage threshold may prevent the MOSFET from turning on.		1.5	1.8	V

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The external balancing MOSFETs should be selected using Table 19 on page 120. Choose a MOSFET with a sufficiently low V_{GS} threshold. For simplification, assume that the integrated MOSFET-balancing resistance can be ignored. The available V_{GS} that turns on the MOSFET is generated across R_{CELL_FILTER}, meaning its voltage is half of the lithium cell voltage (e.g. 4.2V / 2 = 2.1V). In this scenario, the V_{GS} threshold for M_{BAL} should be below 2.1V with an appropriate safety margin. The safety margin should allow for voltage drops on the integrated MOSFET balancing resistor. This drop can be caused by the following:

- Changes in the operating conditions
- Shifts in the M_{BAL} V_{GS} threshold across operating conditions
- Drops that develop across the sensing wires due to the balancing current

Table 21 recommends specific components for external BJT balancing.

Table 21: Recommended Component Selection for External BJT Balancing

Parameter Identifier	Parameter Description	Component Description	Notes	Min	Typ	Max	Unit
C_{CELL_FILTER}	Required capacitance	Cell-filtering capacitor	Capacitance for external balancing configuration. If R_{CELL_FILTER} increases, C_{CELL_FILTER} should be proportionally decreased.		100		nF
R_{CELL_FILTER}	Required resistance	Cell-filtering resistor	Resistance for external balancing configuration. If R_{CELL_FILTER} increases, C_{CELL_FILTER} should be proportionally decreased.	20	100	1000	Ω
R_{BAL}	Required resistance	Cell-balancing current-limiting resistor	Adjust this value to set the balancing current, and verify the power dissipation compared to package limit.		43		Ω
h_{FE_QBAL}	BJT DC current gain	External balancing BJT Q_{BAL}	A lower h_{EF} may limit the external balancing current.	50			

Because R_{BAL} sets the balancing current and dissipates most of the power, ensure that an appropriate resistor and resistor package are selected, especially for resistors below 100Ω. For example, if R_{BAL} = 43Ω, there is 410mW of power dissipation when the lithium cell voltage = 4.2V. This means that a package of at least 2512 (6432 Metric) should be used.

It is also important to consider the thermal design of the overall board and enclosure. The MP2796 can simultaneously balance only odd or even cells, meaning 8 cells in a 16-cell system. When balancing is run continuously on 8 cells, 3.28W is dissipated as heat with a 43Ω R_{BAL}. To keep the MP2796 in the allowed temperature range, consider how this additional heat can be dissipated, as it is added to the amount of heat generated by other components.

The MP2796 includes compensation for the voltage drop across the R_{CELL_FILTER} resistor via the OTP register CELL_1K_COMP. When enabled, this register compensates for an R_{CELL_FILTER} value of 1kΩ. Generally, CELL_1K_COMP should be enabled if R_{CELL_FILTER} is 500Ω or greater.

Selecting the VCP Capacitor

When multiple MOSFETs in parallel are used for DSG or CHG, the VCP capacitance should be selected to avoid causing an excessive voltage drop while the MOSFETs turn on. Table 22 on page 122 lists values for the VCP capacitor depending on the total C_{ISS} that the DSG or CHG MOSFET driver must drive. The total C_{ISS} was obtained from the MOSFET datasheets.

Design the number of parallel DSG MOSFETs to match the number of parallel CHG MOSFETs. If 4 parallel DSG MOSFETs are used, then the individual MOSFET's C_{ISS} should be multiplied by 4, and the resulting C_{ISS} value should be used.

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Table 22: VCP Capacitor Selection

C_{VCP}	Total C_{ISS}
47nF	47nF
68nF	68nF
100nF	100nF

Unused Pins

For a particular application, some pins may not be required. Table 23 shows how to connect these pins when they are not used.

Table 23: Unused Pins Connection

Pin #	Name	Recommendation
1, 2, 3, 4, 5, 6, 46, 47,48	C8,C9, C10, C11, C12, C13, C14, C15, C16	If fewer than 16 series cells are used, directly connect all unused cell channels to the practical maximum cell channel. For example, if only 10 cells are used, C16~C10 should be connected together.
15, 16	SRP, SRN	If the current-sense function is not required, connect these pins to AGND.
17, 18, 19, 20	NTC1, NTC2, NTC3, NTC4	Float the unused NTC channels.
21	NTCB	If NTC temperature monitoring is not used, float this pin.
28	XALERT	Float this pin if it is not used.
29	WDT	Float this pin if it is not used.
33	SDO	Float this pin if it is not used.
34	GPIO3/nCS	Float this pin if it is not used. Note that the GPIO3 should be set to 20kΩ pull-up mode via the GPIO_CFG register; otherwise there may be additional power consumption.
35, 36	GPIO1, GPIO2	Float this pin if it is not used. Note that the unused GPIO should be set to 20kΩ pull-up mode via the GPIO_CFG register; otherwise there may be additional power consumption.
38	PACKP	If the DSG MOSFET driver is not used, and the PACKP vs. VTOP comparator is not needed, connect this pin to VTOP.
39	DSG	If the HS-FET drivers are not used and active mode is required, connect this pin to PACKP via a 100Ω resistor and a 1nF capacitor. If active mode is not required, float this pin.
41	SBYDSG	Float this pin if it is not used.
42	VCP	If the HS-FET drivers are not used and active mode is required, connect this pin to VMID via a 47nF VCP capacitor. If active mode is not required, float this pin.
43	VMID	If the HS-FET drivers are not used, connect this pin to VTOP.
44	CHG	If the HS-FET drivers are not used and active mode is required, connect this pin to VTOP via a 100Ω resistor and a 1nF capacitor. If active mode is not required, float this pin.

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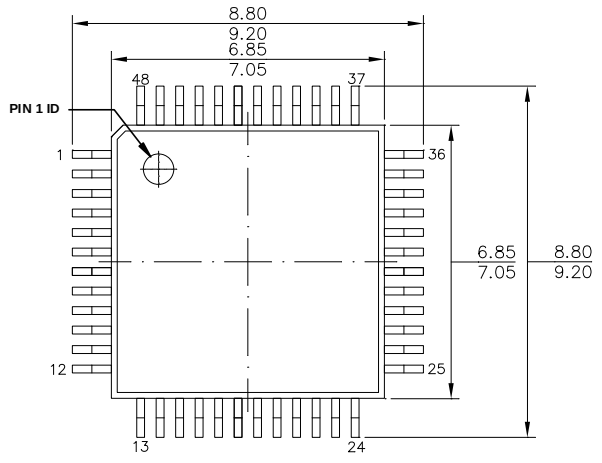
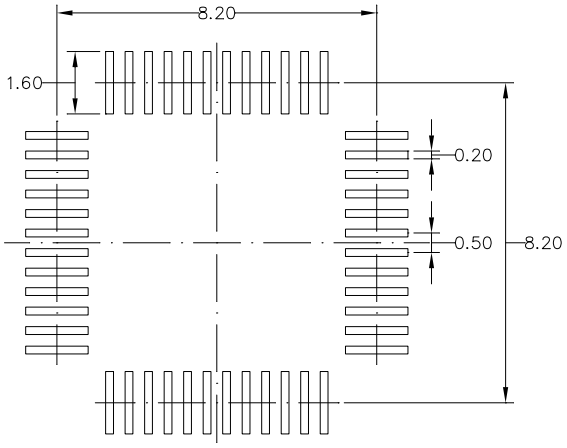
PACKAGE INFORMATION

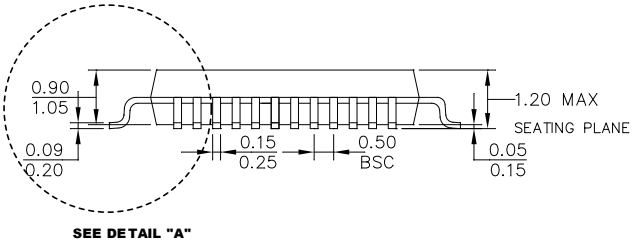
TQFP-48 (7mmx7mm)



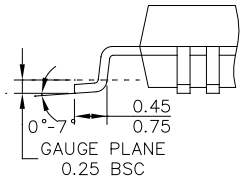
TOP VIEW



RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WITDH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO-143.
6) DRAWING IS NOT TO SCALE.

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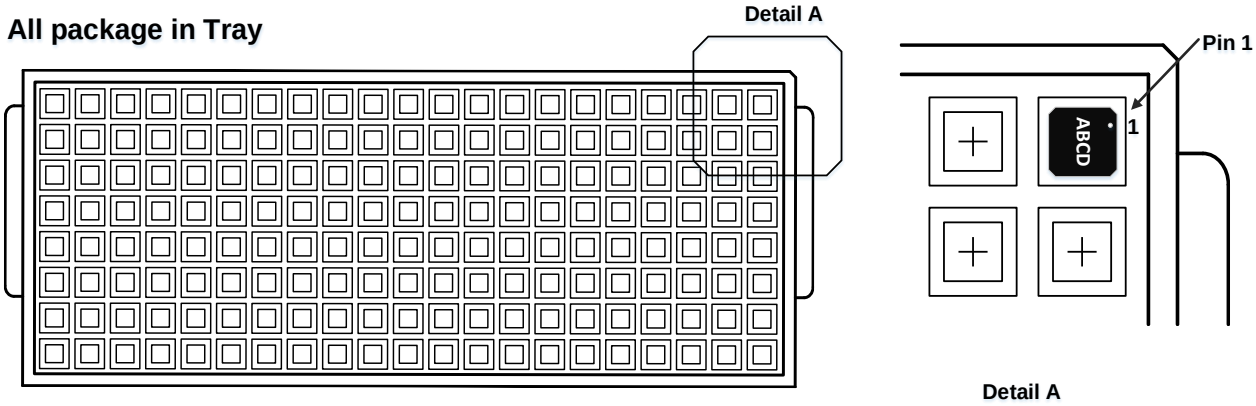
CARRIER INFORMATION

All package in Tray



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP2796DFP-xxxx-T	TQFP-48 (7mmx7mm)	N/A	N/A	250pcs	N/A	N/A	N/A

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	5/9/2023	Initial Release	-

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