MP2650

I²C-Controlled 5A Buck or Boost Charger with NVDC Power Management and USB OTG for 2-Cell to 4-Cell Battery Pack Applications

DESCRIPTION

The MP2650 is a highly integrated buck or boost charger IC with narrow-voltage DC (NVDC) power path management and USB On-The-Go (OTG) for battery packs with 2 cells to 4 cells in series. All power MOSFETs are integrated to provide a compact system solution size.

The IC can accept a wide input voltage (V_{IN}) range for charging, with a 21V maximum. The device has two operating modes during the charging process: boost charging mode and buck charging mode, depending on V_{IN} and the cell count.

With the I²C interface, the MP2650 can be flexibly configured to set the parameters in both charging mode and OTG mode. Parameters include the input current (I_{IN}) limit, V_{IN} limit, charging current, battery charge voltage regulation, and safety charge timer. It can also provide the operation statuses through status and fault registers.

To guarantee safe operation, the IC limits the die temperature to a preset value of 120°C. Other safety features include input over-voltage protection (OVP), battery OVP, system OVP, thermal shutdown, battery temperature protection, and a configured timer to prevent prolonged charging of a dead battery.

To comply with IMVP8 specifications, the IC provides three analog output pins for system power (PSYS), input current (IAM), and battery current (IBM). It also has a processor hot indication pin ($\overline{PROCHOT}$) for system power control.

NVDC power path management regulates the system voltage within a narrow DC range to provide an optimized system bus voltage for the rails at the system bus. With this feature, the system can continue operating even when the battery is completely depleted or removed.

The MP2650 is available in a QFN-30 (4mmx5mm) package.

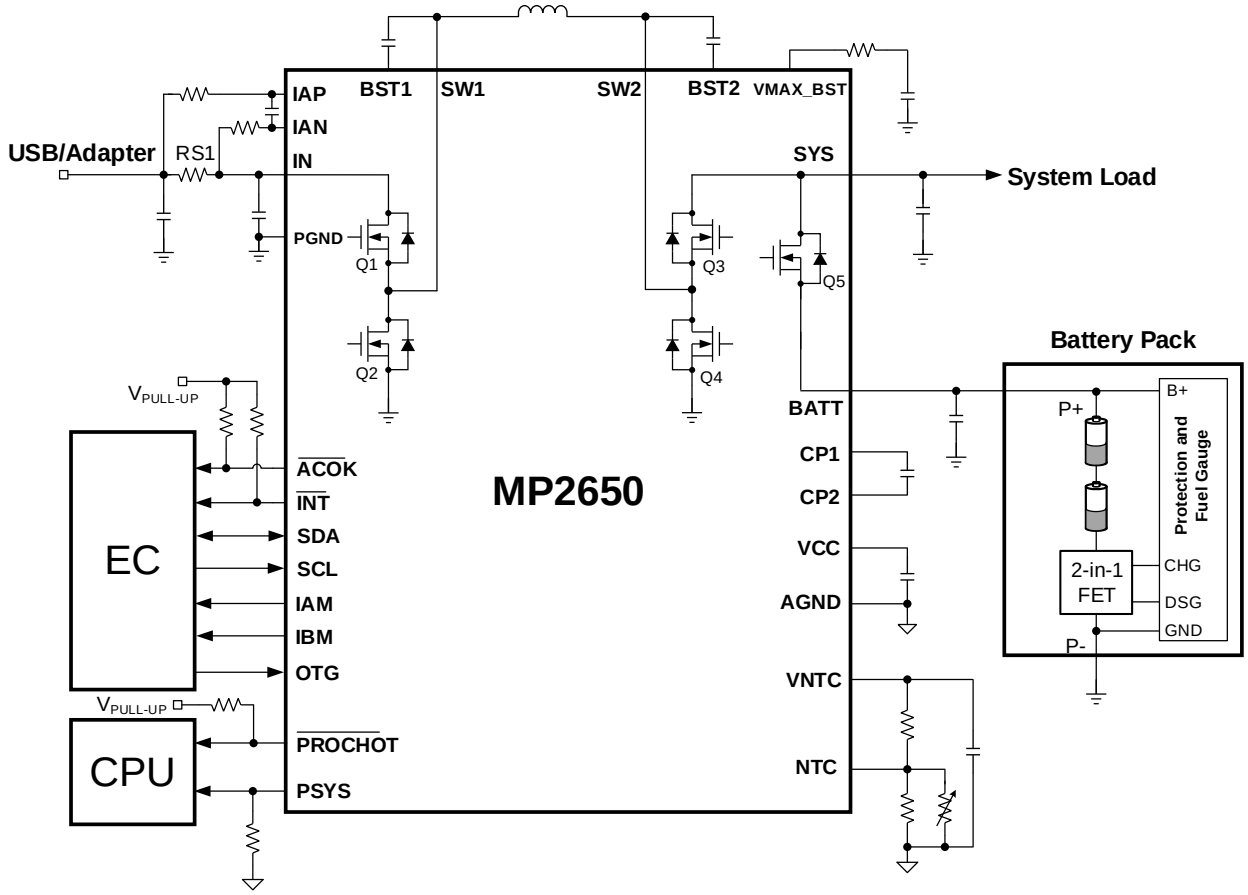
FEATURES

- Buck or Boost Charger for Battery Packs with 2 Cells to 4 Cells in Series
- All Switching MOSFETs are Integrated
- NVDC Power Management with an Integrated Battery FET
- 4V to 21V Operating Input Voltage (V_{IN}) Range
- Up to 28V (20ns) Sustainable V_{IN}
- Configurable V_{IN} Limit
- Up to 5A Configurable Input Current (I_{IN}) Limit (Up to 45W Total Power)
- Up to 5A Configurable Charge Current
- Configurable Battery Charge Voltage Regulation Up to 4.5V/Cell
- System Power Indication via the PSYS Pin
- I_{IN} and Battery Current Monitoring via the IAM and IBM Pins
- Input Over-Voltage Protection (OVP), Battery Temperature Protection, Battery OVP, System OVP
- Configurable Safety Charge Timer
- Thermal Regulation and Thermal Shutdown
- 600kHz, 800kHz, 1MHz, or 1.25MHz Configurable Switching Frequency (f_{SW})
- Input Power Source Status Indication Pin
- I²C Interface to Support Flexible Parameter Control
- Comprehensive Fault and Status Reporting in Register
- Up to 5V/3A USB On-The-Go (OTG)
- Configurable OTG Output Current (I_{OUT}) Limit
- Short-Circuit Protection (SCP) in OTG Mode
- Available in a QFN-30 (4mmx5mm) Package

APPLICATIONS

- Tablets and Notebooks
- Bluetooth Speakers
- Portable Gimbals

TYPICAL APPLICATION CIRCUIT



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP2650GV-xxxx**	QFN-30 (4mmx5mm)	*See Below*	1
MP2650GV-0200***			
MP2650GV-0300****			
MP2650GV-0400*****			
EVKT-MP2650	Evaluation Kit	N/A	N/A

* For Tape & Reel, add suffix -Z (e.g. MP2650GV-xxxx-Z).

** "xxxx" is the configuration code identifier for the register settings. For the default case, the number is "-0000." Each "x" can be a hexadecimal value between 0 and F. Work with an MPS FAE to create this unique number, even if ordering the "-0000" code.

*** "-0200" is configuration code for 2-cell applications.

**** "-0300" is configuration code for 3-cell applications.

***** "-0400" is configuration code for 4-cell applications.

TOP MARKING

MPSYWW

MP2650

LLLLLL

MPS: MPS prefix
Y: Year code
WW: Week code
MP2650: Part number
LLLLLL: Lot number

EVALUATION KIT EVKT-MP2650

EVKT-MP2650 kit contents (items below can be ordered separately):

#	Part Number	Item	Quantity
1	EV2650-V-01A	MP2650 evaluation board (MP2650GV-0200)	1
2	EVKT-USBI2C-02 bag	Includes one USB to I^2C communication interface, one USB cable, and one ribbon cable	1
3	Online resources	Include datasheet, user guide, product brief, and GUI	1

Order directly from MonolithicPower.com or our distributors.

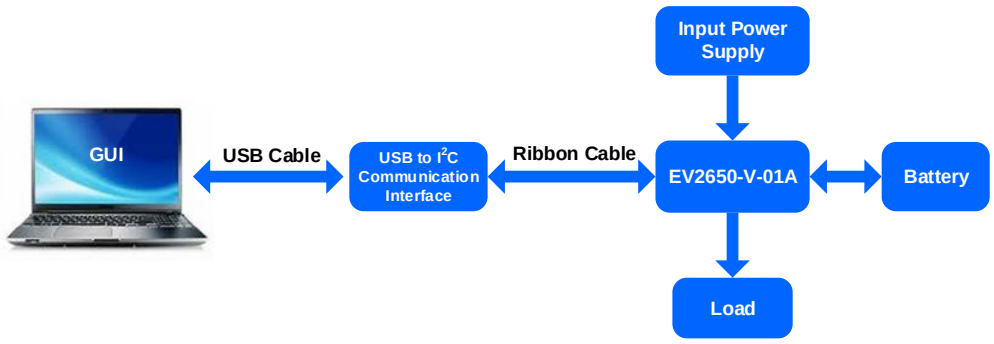
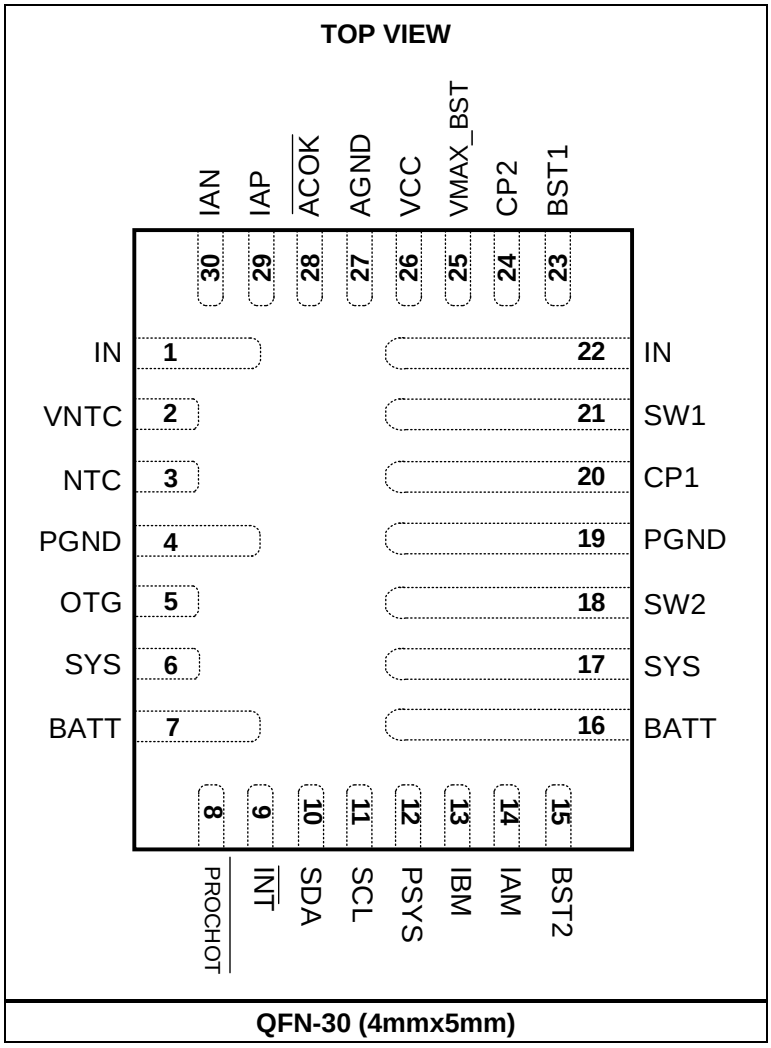


Figure 1: EVKT-MP2650 Evaluation Kit Set-Up

PACKAGE REFERENCE



QFN-30 (4mmx5mm)

PIN FUNCTIONS

Pin #	Name	Description
1, 22	IN	**Power input pin.** IN is the IC's power input from either an adapter or USB.
2	VNTC/ CMOUT	**Negative temperature coefficient (NTC) network pull-up voltage.** VNTC is the pull-up voltage of the NTC comparator resistor divider, which provides both the feedback and the reference. This pin can be also configured as an independent comparator output (CMOUT) via the I^2C interface.
3	NTC/ BATDET	**NTC thermistor input.** Connect an NTC thermistor from the NTC pin to AGND. Configure the hot and cold temperature windows with a resistor divider connected from VNTC to NTC to AGND. Charging is suspended when NTC is out of its range. This pin can also be configured as a battery detection terminal via the I^2C interface.
4, 19	PGND	**Power ground.**
5	OTG/ CMIN	**USB On-The-Go (OTG) enable control.** This pin can also be configured as the independent comparator input pin via the I^2C interface. When this pin is configured to be CMIN, OTG is enabled via the internal register bit.
6, 17	SYS	**System output.** Connect 5 x 22µF ceramic capacitors from SYS to PGND, and place them as close as possible to the IC.
7, 16	BATT	**Battery positive terminal.** Connect 2 x 22µF ceramic capacitors from BATT to PGND, and place them as close as possible to the IC.
8	$\overline{\text{PROCHOT}}$	**Processor hot interrupt output.** This pin is an open-drain structure. It is pulled to AGND when the PROCHOT signal asserts, and floats when a PROCHOT event is not occurring. This pin must be pulled up externally.
9	$\overline{\text{INT}}$	**Open-drain interrupt output.** The $\overline{\text{INT}}$ pin can send the charging status and fault interrupt signals to the host. It must be pulled up externally.
10	SDA	**I^2C interface data line**. Connect SDA to the logic rail through a 10kΩ resistor.
11	SCL	**I^2C interface clock line**. Connect SCL to the logic rail through a 10kΩ resistor.
12	PSYS	**System power indication pin.** This pin outputs a current source that is proportional to the total system power.
13	IBM	**Battery current-sense output.** IBM outputs a voltage that is proportional to the battery charge current or battery discharger current.
14	IAM	**Input current-sense output.** IAM outputs a voltage that is proportional to the input current.
15	BST2	**Bootstrap for boost phase**. Connect a 470nF bootstrap capacitor between the BST2 and SW2 pins to form a floating supply across the power MOSFET driver. This drives the power MOSFET's gate above the supply voltage.
18	SW2	**Boost phase switching node.**
20	CP1	**Charge pump node 1.** Place a 470nF capacitor between the CP1 and CP2 pins.
21	SW1	**Buck phase switching node.**
23	BST1	**Bootstrap for buck phase.** Connect a 470nF bootstrap capacitor between the BST1 and SW1 pins to form a floating supply across the power MOSFET driver. This drives the power MOSFET's gate above the supply voltage.
24	CP2	**Charge pump node 2.** Place a 470nF capacitor between the CP1 and CP2 pins.
25	VMAX_BST	**Charge pump output.** Connect a 100nF ceramic capacitor in series with a 100Ω resistor from VMAX_BST to PGND, and place the capacitor and resistor as close as possible to the IC.

PIN FUNCTIONS *(continued)*

Pin #	Name	Description
26	VCC	**VCC LDO output.** VCC can provide 3.6V/50mA for internal circuits, as well as the pull-up voltage for the open-drain pins ($\overline{\text{ACOK}}$, $\overline{\text{INT}}$, and $\overline{\text{PROCHOT}}$). Connect a 10μF ceramic capacitor from VCC to AGND, and place it as close as possible to the IC.
27	AGND	**Analog ground.**
28	$\overline{\text{ACOK}}$	**Input power present indication.** This pin is an open-drain structure, and must be pulled up externally.
29	IAP	**Input current-sense positive terminal.**
30	IAN	**Input current-sense negative terminal.**

ABSOLUTE MAXIMUM RATINGS (1)

IN, IAN, IAP to PGND (20ns).....-0.3V to +28V
IN, IAN, IAP to PGND (DC) .....-0.3V to +26V
SYS to PGND .....-0.3V to +24V
VMAX_BST to PGND .....0V to 26V
BATT to PGND .....-0.3V to +24V
SW1 to PGND (20ns).....-2V to +28V
SW1 to PGND (DC) .....-0.3V to +24V
SW2 to PGND .....-0.3V (-2V for 20ns) to +24V
CP1 to PGND (DC).....-0.3V to +24V
BST1 to PGND .....SW1 to SW1 + 5V
BST2 to PGND .....SW2 to SW2 + 5V
CP2 to PGND ..... CP1 to CP1 +5V
All other pins to AGND.....-0.3V to +5V
Continuous power dissipation (T_A = 25°C) (2)
..... 3.29W
Junction temperature .....150°C
Lead temperature (solder) .....260°C
Storage temperature ..... -65°C to +150°C

ESD Ratings

Human body model (HBM) 2000V
Charged device model (CDM).....750V

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) ..... 4V to 21V
Input current ..... Up to 5A
Charge current..... Up to 5A
Discharge current via battery FET (DC)……...
..... Up to 14A
Battery voltage..... Up to 18V
Operating junction temp (T_J).....-40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-30 (4mmx5mm)..... 38 ..... 8.... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS (5)

V_{IN} = 5V, V_{BATT} = 3.7V/cell, RS1 = 10mΩ, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Voltage (V_{IN}) Characteristics						
V_{IN} under-voltage lockout (UVLO) threshold	V_{IN_UVLO}	V_{IN} falling	3.45	3.68	3.87	V
V_{IN} UVLOhysteresis		V_{IN} rising		350		mV
V_{IN} UVLO recovery deglitch time		V_{IN} rising		30		ms
V_{IN} power-on reset (POR)	V_{IN_POR}	V_{IN} rising		3.17		V
V_{IN} POR hysteresis		V_{IN} falling		620		mV
V_{IN} over-voltage lockout (OVLO) threshold	V_{IN_OVLO}	V_{IN} rising	23	24	25	V
V_{IN} OVLO hysteresis		V_{IN} falling	1.55	1.66	1.78	V
DC/DC Converter						
Input shutdown current	I_{SHDN}	V_{IN} = 5V, Q1–Q4 are off			9.5	mA
		V_{IN} = 20V, Q1–Q4 are off			9.5	mA
VCC LDO output voltage	V_{VCC}	V_{IN} = 5V, I_{VCC} = 10mA	3.4	3.6	3.73	V
VCC LDO current limit	I_{VCC}	V_{IN} = 5V, V_{BATT} = 7.8V	50			mA
IN to SW1 N-channel MOSFET (Q1) on resistance	R_{ON_Q1}			16		mΩ
SW1 to PGND N-channel MOSFET (Q2) on resistance	R_{ON_Q2}			16		mΩ
SW2 to SYS N-channel MOSFET (Q3) on resistance	R_{ON_Q3}			6		mΩ
SW2 to PGND N-channel MOSFET (Q4) on resistance	R_{ON_Q4}			16		mΩ
SYS to BATT N-channel MOSFET (Q5) on resistance	R_{ON_Q5}			11		mΩ
Battery tracking regulation voltage	V_{TRACK}		5			mV
Minimum system regulation voltage	$V_{SYS\_REG\_MIN}$	2 cells, REG07h, bits[5:4] = 01, REG30h, bit[3] = 0	5.97	6.16	6.34	V
Operating frequency	f_{SW}	REG0Bh, bits[4:3] = 00		600		kHz
		REG0Bh, bits[4:3] = 01		800		
		REG0Bh, bits[4:3] = 10		1000		
		REG0Bh, bits[4:3] = 11		1250		
System short-circuit entry threshold		Boost charge, V_{SYS} falling, compare to V_{IN}	30	168	320	mV
System short-circuit exit threshold		Boost charge, V_{SYS} rising, compare to V_{IN}	110	314	500	

ELECTRICAL CHARACTERISTICS *(continued)* (5)

V_{IN} = 5V, V_{BATT} = 3.7V/cell, RS1 = 10mΩ, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Battery Charger						
Battery charge voltage regulation	V_{BATT_REG}	2 cells, default: 8.4V (REG04h, bits[6:1] = 100111, REG07h, bits[7:6] = 00)	8.337	8.40	8.463	V
		3 cells, default: 12.6V (REG04h, bits[6:1] = 100111, REG07h, bits[7:6] = 01)	12.465	12.59	12.715	V
		4 cells, default: 16.8V (REG04h, bits[6:1] = 100111, REG07h, bits[7:6] = 10/11)	16.613	16.78	16.947	V
Fast charge current	I_{CC}	I_{CC} = 3A, REG02h, bits[6:0] = 0111100	2.8	3	3.3	A
		I_{CC} = 2A, REG02h, bits[6:0] = 0101000	1.85	2	2.2	A
		I_{CC} = 1A, REG02h, bits[6:0] = 0010100	0.91	1	1.13	A
		I_{CC} = 0.5A, REG02h, bits[6:0] = 0001010	0.44	0.5	0.6	A
Trickle charge to pre-charge threshold	V_{BATT_TC}	2 cells, V_{BATT} rising	3.92	4	4.25	V
Trickle charge to pre-charge threshold hysteresis		2 cells, V_{BATT} falling	450	550	650	mV
Trickle charge current	I_{TC}	2 cells, V_{BATT} = 1V	60	100	190	mA
		2 cells, V_{BATT} = 3V	130	188	240	mA
Pre-charge to fast charge rising threshold	V_{BATT_PRE}	2 cells, REG07h, bits[5:4] = 01, REG30h, bit[3] = 0	6.04	6.2	6.32	V
		2 cells, REG07h, bits[5:4] = 11, REG30h, bit[3] = 0	6.42	6.6	6.71	V
Pre-charge to fast charge falling threshold		2 cells, REG07h, bits[5:4] = 01, REG30h, bit[3] = 0	5.85	6.025	6.15	V
		2 cells, REG07h, bits[5:4] = 11, REG30h, bit[3] = 0	6.25	6.42	6.54	V
Pre-charge current	I_{PRE}	2 cells, V_{BATT} = 5V, REG03h, bits[7:4] = 0010	120	180	240	mA
		2 cells, V_{BATT} = 5V, REG03h, bits[7:4] = 0101	170	240	310	mA
		2 cells, V_{BATT} = 5V, REG03h, bits[7:4] = 1010	400	540	720	mA
		2 cells, V_{BATT} = 5V, REG03h, bits[7:4] = 1100	480	660	920	mA
		2 cells, V_{BATT} = 5V, REG03h, bits[7:4] = 1111	600	840	1230	mA

ELECTRICAL CHARACTERISTICS *(continued)* (5)

V_{IN} = 5V, V_{BATT} = 3.7V/cell, RS1 = 10mΩ, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Termination current	I_{TERM}	REG03h, bits[3:0] = 0001	30	145	280	mA
		REG03h, bits[3:0] = 0100	280	435	600	mA
		REG03h, bits[3:0] = 1111	1.3	1.5	1.75	A
Auto-recharge battery voltage threshold	V_{RECH}	Below the battery-full voltage, 2 cells, REG04h, bit[0] = 1, REG07h, bits[7:6] = 00	150	210	270	mV /cell
Charge termination deglitch time	t_{TERM_DGL}			1.7		sec
Battery over-voltage (OV) threshold	V_{BATT_OVP}	2 cells, V_{BATT} rising, compare to V_{BATT_REG}	140	320	520	mV
Battery OV threshold hysteresis			130	210	290	mV
Virtual diode entry threshold		V_{SYS} falling, V_{BATT} - V_{SYS}		25		mV
Virtual diode quit threshold		V_{SYS} rising, V_{SYS} - V_{BATT}		30		mV
Ideal diode forward voltage in supplement mode	V_{FWD}	10mA discharge current		30		mV
V_{IN} and Input Current (I_{IN}) Regulation						
I_{IN} limit	I_{IN_LIM1}	REG00h, bits[6:0] = 0001010	410	470	530	mA
		REG00h, bits[6:0] = 0011110	1.4	1.49	1.57	A
		REG00h, bits[6:0] = 0111100	2.85	3	3.15	A
V_{IN} clamp limit threshold	V_{IN_MIN}	REG01h, bits[7:0] = 00101101	4.28	4.5	4.72	V
		REG01h, bits[7:0] = 01010101	8.25	8.5	8.73	
		REG01h, bits[7:0] = 10010001	14.1	14.5	14.9	
Battery Temperature Protection (NTC JEITA)						
NTC low-temp rising voltage threshold	V_{COLD}	NTC pin voltage rising as a percentage of V_{NTC}	69	71.1	73.5	%
NTC low-temp threshold hysteresis		NTC pin voltage falling		0.9		%
NTC cool-temp rising voltage threshold	V_{COOL}	NTC pin voltage rising as a percentage of V_{NTC}, REG0Ah, bits[1:0] = 01	66.5	68.9	71.5	%
NTC cool-temp threshold hysteresis		NTC pin voltage falling		1.3		%
NTC warm-temp falling voltage threshold	V_{WARM}	NTC pin voltage falling as a percentage of V_{NTC}, REG0Ah, bits[3:2] = 01	54	56.1	58.5	%
NTC warm-temp threshold hysteresis		NTC pin voltage rising		1.2		%
NTC hot-temp falling voltage threshold	V_{HOT}	NTC pin voltage falling as a percentage of V_{NTC}	46	48.3	50.5	%
NTC hot-temp threshold hysteresis		NTC pin voltage rising		1.4		%

ELECTRICAL CHARACTERISTICS *(continued)* (5)

V_{IN} = 5V, V_{BATT} = 3.7V/cell, RS1 = 10mΩ, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Thermal Regulation and Protection						
Thermal shutdown rising threshold (5)	T_{J_SHDN}	T_J rising		150		°C
Thermal shutdown hysteresis (5)		T_J falling		20		°C
Thermal regulation point (5)	T_{J_REG}	Pre-charge stage, REG05h, bits[1:0] = 11		120		°C
Battery-Only Mode						
Battery leakage current	I_{BATT_Q}	V_{IN} < V_{IN_UVLO}, V_{BATT} = 8.4V, BATTFET on, REG0Bh bits[1:0] = 00 to disable PROCHOT and PSYS/ADC functionality		40	60	µA
		V_{IN} < V_{IN_UVLO}, V_{BATT} = 8.4V, BATTFET on, REG0Bh bits[1:0] = 01 to disable PSYS /ADC but enable PROCHOT functionality			490	
		V_{IN} < V_{IN_UVLO}, V_{BATT} = 8.4V, BATTFET on, REG0Bh, bits[1:0] = 11 to enable both PSYS/ADC and PROCHOT functionality			2800	
Battery operation UVLO	V_{BATT_UVLO}	2 cells, V_{BATT} falling		5.2		V
Battery operation UVLO hysteresis		2 cells, V_{BATT} rising		560		mV
OTG Operation						
OTG short-circuit entry threshold		V_{IN} falling, compare to V_{SYS}	40	177	340	mV
OTG short-circuit exit threshold		V_{IN} rising, compare to V_{SYS}	160	335	520	mV
OTG over-voltage protection (OVP) threshold	V_{OTG_OVP}	V_{BATT} = 7.4V, V_{IN_OTG} rising, as a percentage of the OTG voltage setting, REG0Dh, bits[5:4] = 00		125		%
OTG OVP threshold hysteresis		V_{IN_OTG} falling, as a percentage of the OTG voltage setting		7.5		%
OTG output voltage	V_{IN_OTG}	I_{OTG} = 0A, REG06h, bits[6:0] = 000 0101	4.9	5	5.1	V
OTG output voltage accuracy		As a percentage of V_{IN_OTG}, I_{OTG} = 0A	-2		+2	%
OTG under-voltage protection (UVP) threshold	V_{OTG_UV}	V_{BATT} = 7.4V, V_{IN_OTG} falling, as a percentage of the OTG voltage setting, REG0Dh, bits[3:2] = 00		75		%
OTG UVP threshold hysteresis		V_{IN_OTG} rising, as a percentage of the OTG voltage setting		7.5		%
OTG output current limit	I_{OLIM}	REG07h, bits[3:0] = 0110, V_{BATT} = 7.4V	1.075	1.43	1.735	A
		REG07h, bits[3:0] = 1011, V_{BATT} = 7.4V	2.59	2.93	3.27	A

ELECTRICAL CHARACTERISTICS *(continued)* (5)

V_{IN} = 5V, V_{BATT} = 3.7V/cell, RS1 = 10mΩ, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
IMVP Requirements						
Monitoring Function						
I_{IN} indication gain	V_{IAM}	RS1 = 10mΩ		250		mV/A
I_{IN} indication offset				100		mV
Battery current indication gain	V_{IBM}	Charging		125		mV/A
		Discharging		62.5		mV/A
Battery current indication offset		Charging		50		mV
		Discharging, I_{BATT} = 200mA		6.5		mV
System Power Monitor						
System power indicator full scale		256 steps		100		µA
Processor Hot Interruption						
System under-voltage (UV) PROCHOT		REG0Dh, bits[1:0] = 01, V_{SYS} falling		5.84		V
System UV PROCHOT hysteresis				160		mV
Battery discharge over-current (OC) PROCHOT		REG0Ch, bits[7:5] = 110, I_{BATT} increasing		12		A
Discharge OC PROCHOT deglitch time				25		µs
Input current OC PROCHOT		REG12h, bits[6:3] = 1010, I_{IN} increasing		8.2		A
General Comparator						
General comparator reference		REG0Ch, bit[0] = 0		1.22		V
General comparator hysteresis			40	110	180	mV
General comparator output open-drain MOSFET resistance				200		Ω
Battery Missing Detection						
Battery absent threshold				1.6		V
Battery absent hysteresis				10		mV
Analog-to-Digital Converter (ADC) Performance						
Sample rate				50		kHz
ADC resolution				10		bits
ADC reference				1.6		V
Logic I/O Pin Characteristics						
Logic low voltage threshold	V_L				0.4	V
Logic high voltage threshold	V_H		1.3			V

ELECTRICAL CHARACTERISTICS *(continued)* (5)

V_{IN} = 5V, V_{BATT} = 3.7V/cell, RS1 = 10mΩ, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
I²C Interface (SDA, SCL)						
Input high threshold level		V_{PULL_UP} = 1.8V, SDA and SCL	1.3			V
Input low threshold level		V_{PULL_UP} = 1.8V, SDA and SCL			0.4	V
Output low threshold level		I_{SINK} = 5mA			0.4	V
I²C clock frequency	f_{SCL}				400	kHz
Timer Specifications						
Digital clock	f_{DIG}	VCC LDO enabled	4.5	5	5.5	MHz
Watchdog timer	t_{WDT}	REG09h, bits[5:4] = 11		160		sec
Short circuit recovery time				25.6		ms
Trickle charge and pre-charge timer				1		hrs
Total charger timer	t_{TMR}	REG09h, bits[2:1] = 10		12		hrs

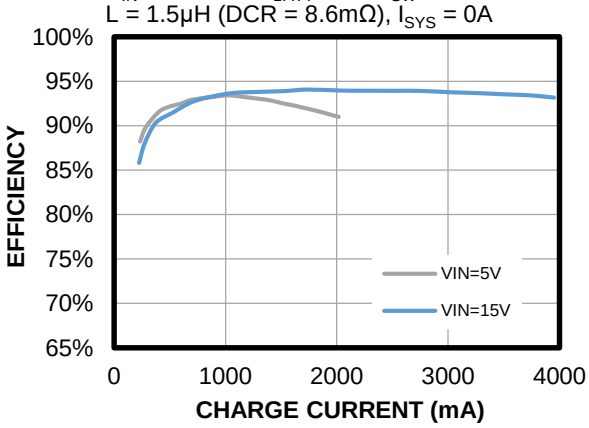
Note:

5) Guaranteed by design.

TYPICAL CHARACTERISTICS

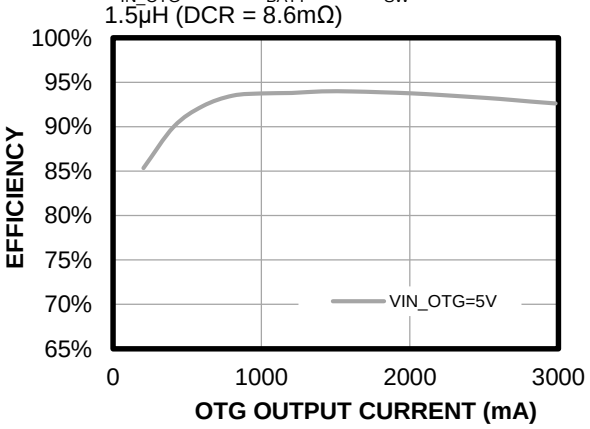
Charge Efficiency

V_{IN} = 5V/15V, V_{BATT} = 8V, f_{SW} = 600kHz, L = 1.5µH (DCR = 8.6mΩ), I_{SYS} = 0A



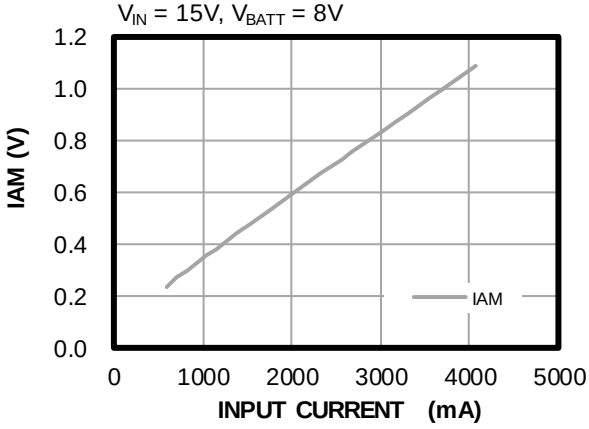
OTG Efficiency

V_{IN_OTG} = 5V, V_{BATT} = 8V, f_{SW} = 600kHz, L = 1.5µH (DCR = 8.6mΩ)



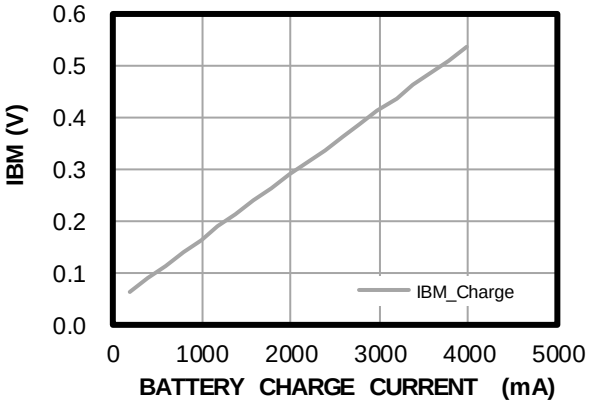
IAM vs. Input Current in Charge Mode

V_{IN} = 15V, V_{BATT} = 8V



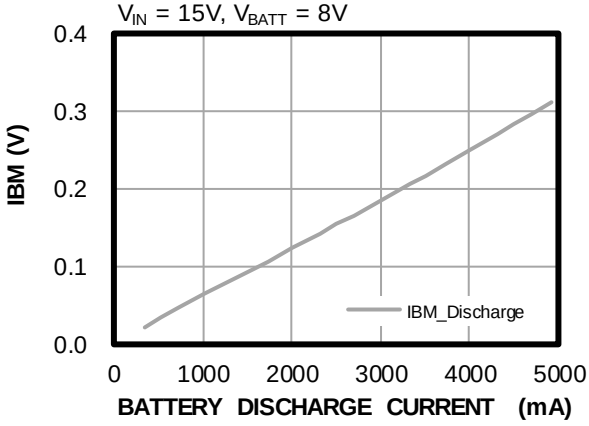
IBM vs. Battery Charge Current

V_{IN} = 15V, V_{BATT} = 8V



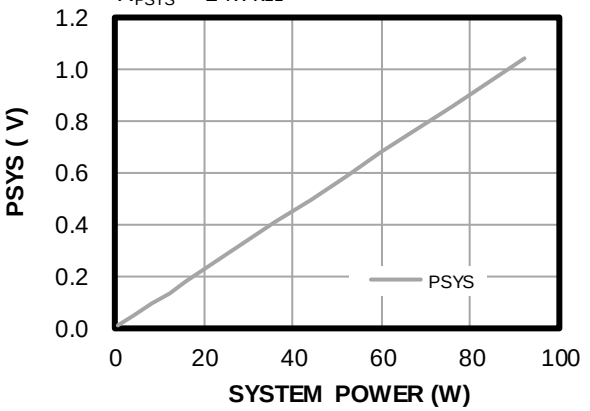
IBM vs. Battery Discharge Current

V_{IN} = 15V, V_{BATT} = 8V



PSYS vs. System Power

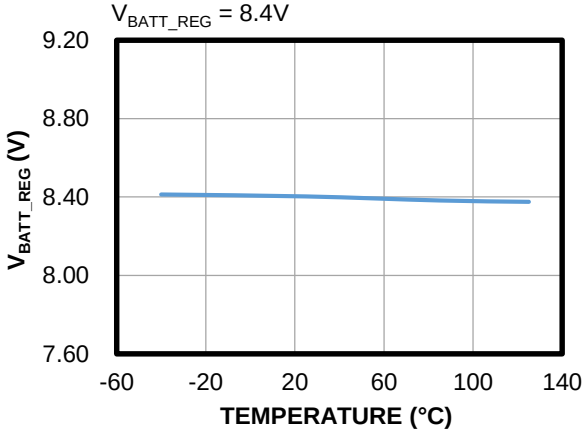
V_{IN} = 20V, V_{BATT} = 7.4V, I_{CHG} = 2A, R_{PSYS} = 14.7kΩ



TYPICAL CHARACTERISTICS *(continued)*

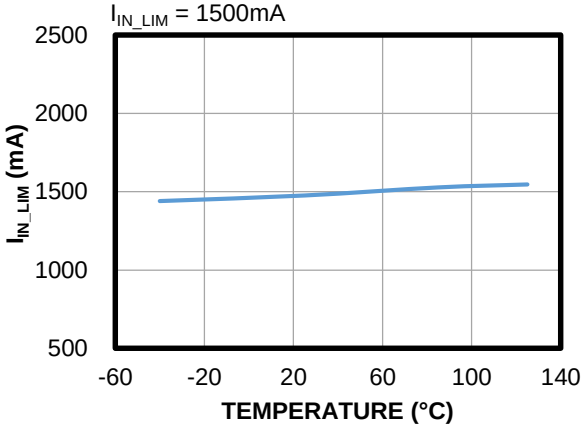
Battery Regulation Voltage vs. Temperature

V_{BATT_REG} = 8.4V



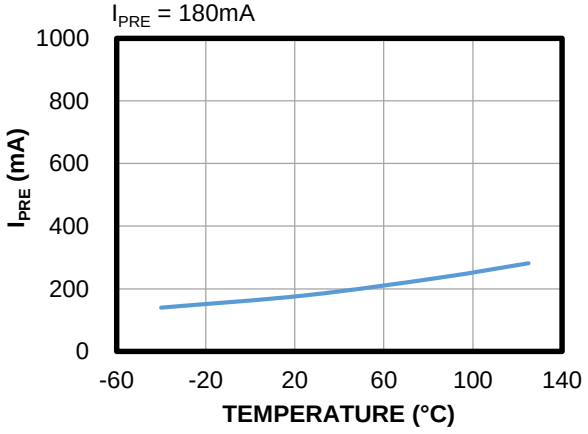
Input Current Limit vs. Temperature

I_{IN_LIM} = 1500mA



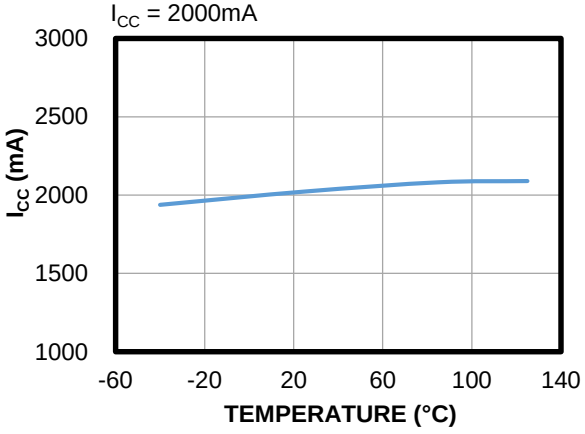
Pre-Charge Current vs. Temperature

I_{PRE} = 180mA



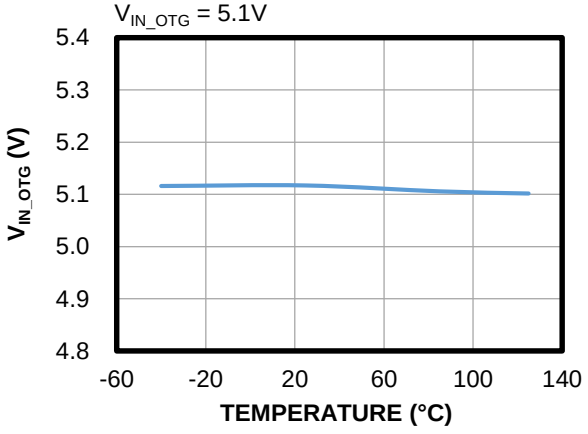
Fast Charge Current vs. Temperature

I_{CC} = 2000mA



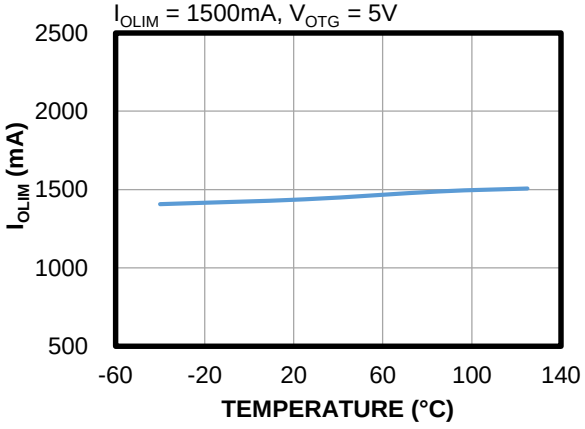
OTG Output Voltage vs. Temperature

V_{IN_OTG} = 5.1V



OTG Output Current Limit vs. Temperature

I_{OLIM} = 1500mA, V_{OTG} = 5V

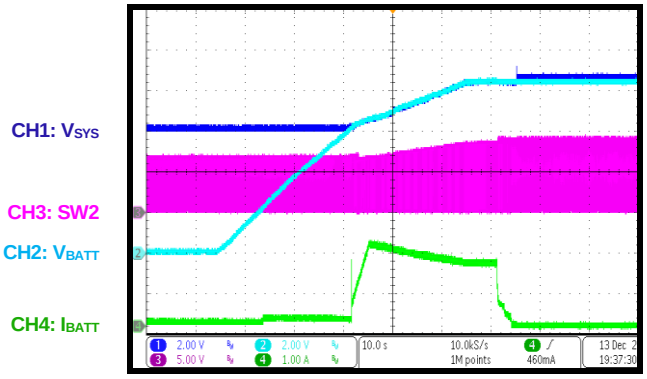


TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, V_{BATT} = 0V to 8.4V, I_{CC} = 2A, I_{IN_LIM1} = I_{IN_LIM2} = 3A, V_{IN_MIN} = 4.5V, f_{SW} = 600kHz, L = 1.5µH, T_A = 25°C, unless otherwise noted.

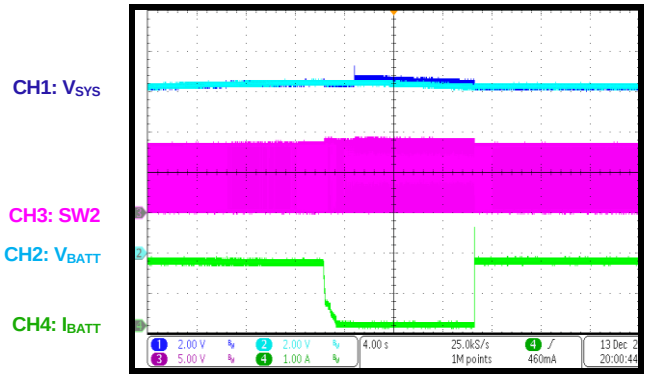
Battery Charge Curve

V_{IN} = 5V, V_{BATT_PRE} = 6V, V_{BATT_REG} = 8.4V



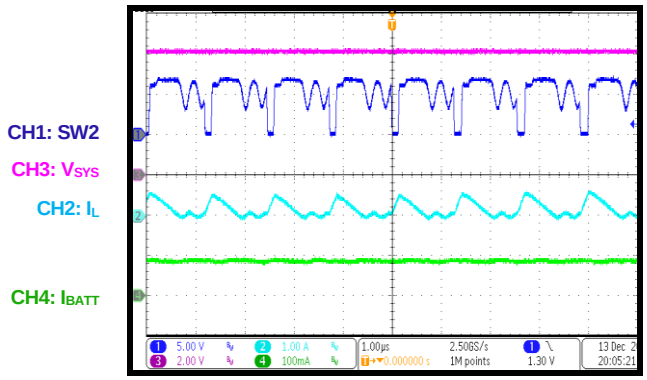
Auto-Recharge

V_{IN} = 5V, V_{BATT_PRE} = 6V, V_{BATT_REG} = 8.4V



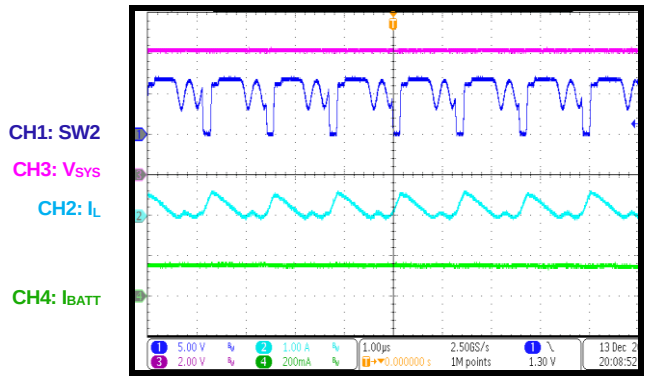
TC Charge Steady State

V_{IN} = 5V, V_{BATT} = 1V



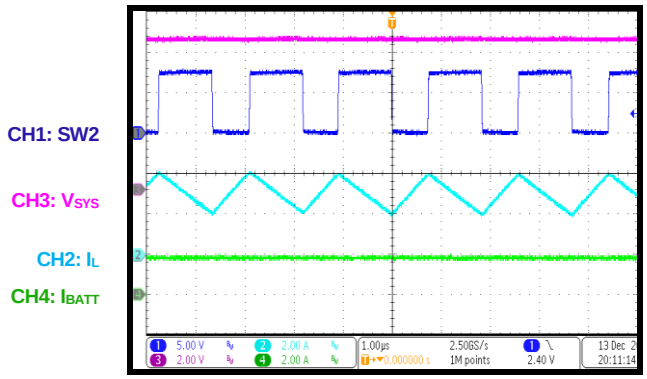
Pre-Charge Steady State

V_{IN} = 5V, V_{BATT} = 5.8V



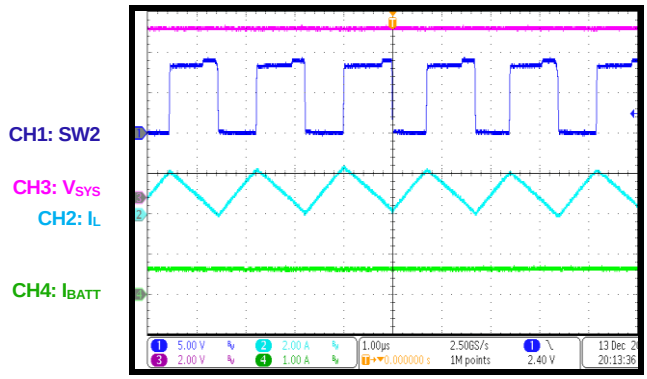
CC Charge Steady State

V_{IN} = 5V, V_{BATT} = 7.4V



CV Charge Steady State

V_{IN} = 5V, V_{BATT} = 8.4V

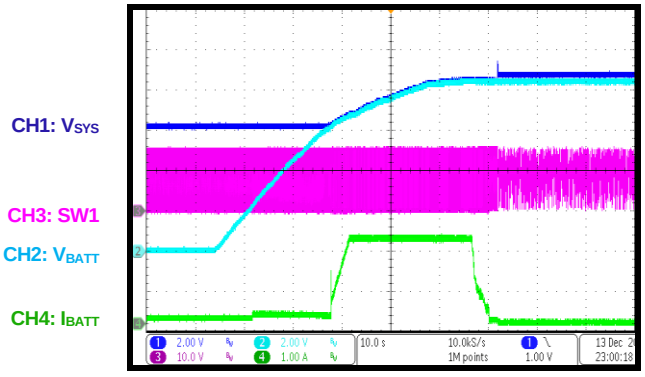


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 15V, V_{BATT} = 0V to 8.4V, I_{CC} = 2A, I_{IN_LIM1} = I_{IN_LIM2} = 3A, V_{IN_MIN} = 4.5V, f_{SW} = 600kHz, L = 1.5µH, T_A = 25°C, unless otherwise noted.

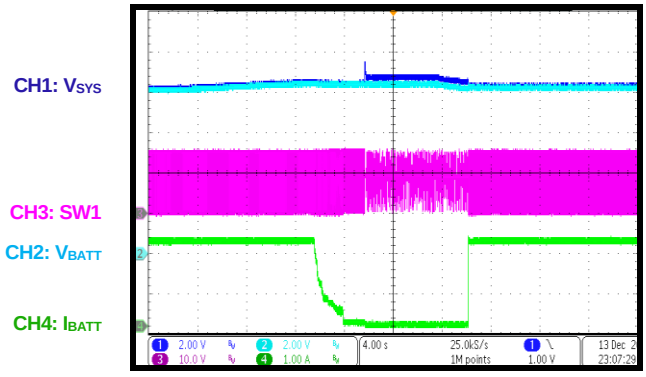
Battery Charge Curve

V_{IN} = 15V, V_{BATT_PRE} = 6V, V_{BATT_REG} = 8.4V



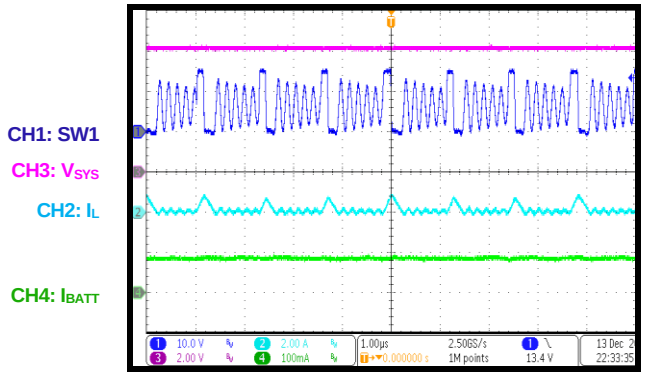
Auto-Recharge

V_{IN} = 15V, V_{BATT_PRE} = 6V, V_{BATT_REG} = 8.4V



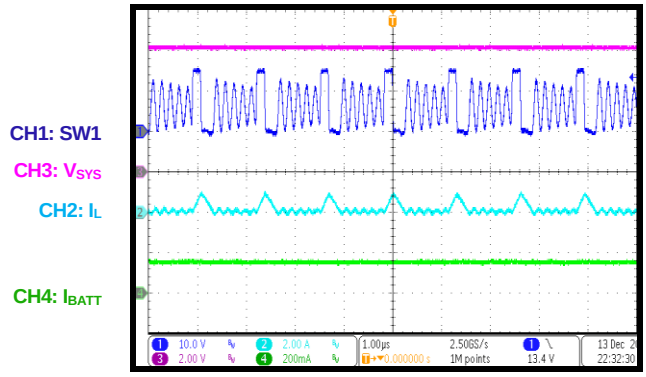
TC Charge Steady State

V_{IN} = 15V, V_{BATT} = 1V



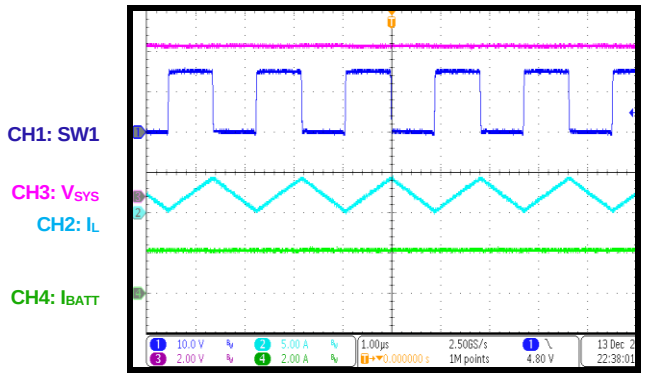
Pre-Charge Steady State

V_{IN} = 15V, V_{BATT} = 5.8V



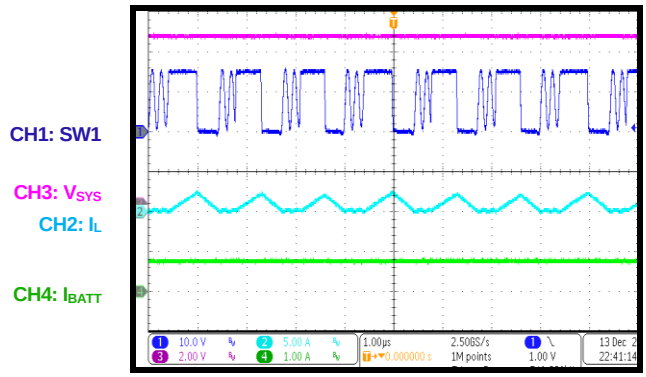
CC Charge Steady State

V_{IN} = 15V, V_{BATT} = 7.4V



CV Charge Steady State

V_{IN} = 15V, V_{BATT} = 8.4V

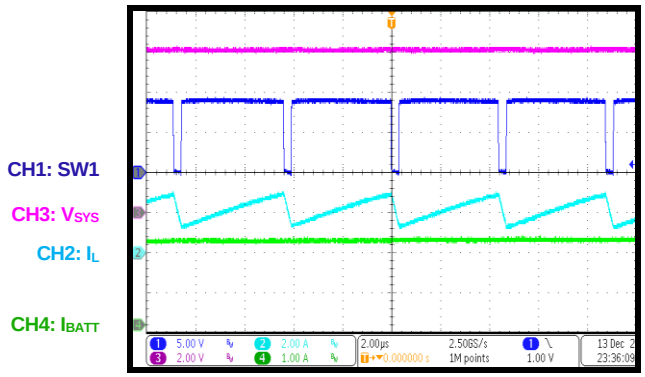


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{BATT} = 0V to 8.4V, I_{CC} = 2A, I_{IN_LIM1} = I_{IN_LIM2} = 3A, V_{IN_MIN} = 4.5V, f_{SW} = 600kHz, L = 1.5µH, T_A = 25°C, unless otherwise noted.

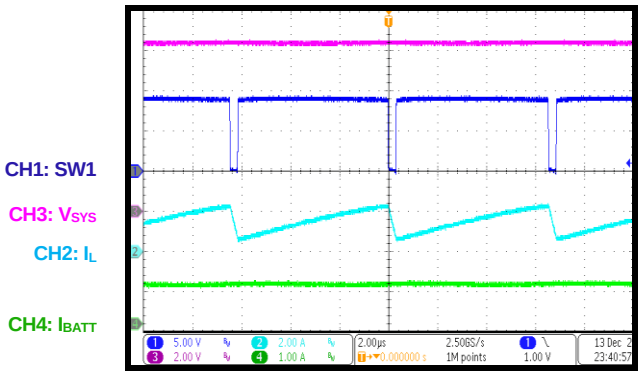
CC Charge Steady State

V_{IN} = 9V, V_{BATT} = 8V, I_{IN_LIM1} = I_{IN_LIM2} = 5A, I_{SYS} = 0A



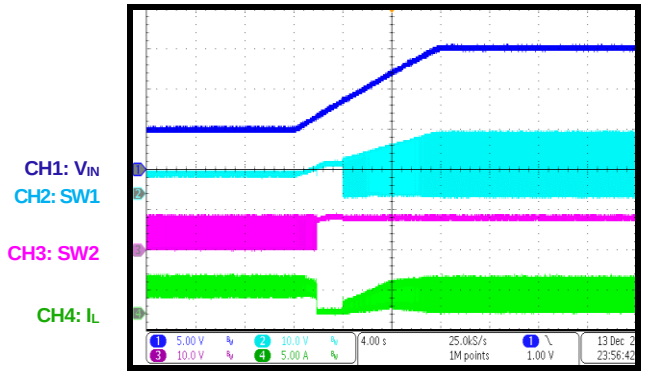
CV Charge Steady State

V_{IN} = 9V, V_{BATT} = 8.4V, I_{IN_LIM1}= I_{IN_LIM2} = 5A, I_{SYS} = 0.5A



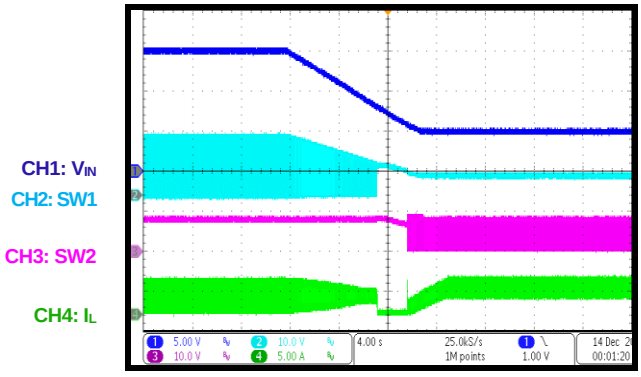
Boost-to-Buck Transition

V_{IN} = 5V to 15V, V_{BATT} = 7.4V



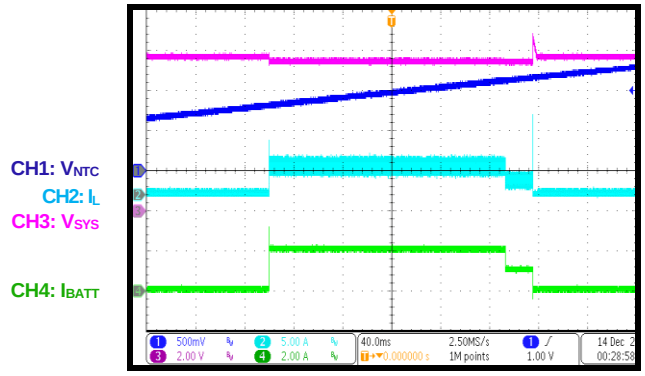
Buck-to-Boost Transition

V_{IN} = 15V to 5V, V_{BATT} = 7.4V



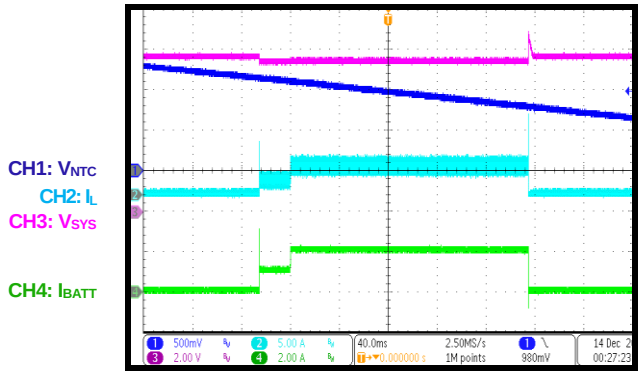
NTC

V_{IN} = 5V, V_{BATT} = 7.4V, temperature falling



NTC

V_{IN} = 5V, V_{BATT} = 7.4V, temperature rising

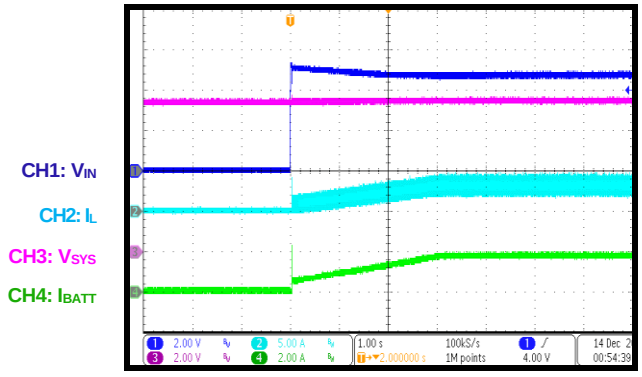


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{BATT} = 0V to 8.4V, I_{CC} = 2A, I_{IN_LIM1} = I_{IN_LIM2} = 3A, V_{IN_MIN} = 4.5V, f_{SW} = 600kHz, L = 1.5µH, T_A = 25°C, unless otherwise noted.

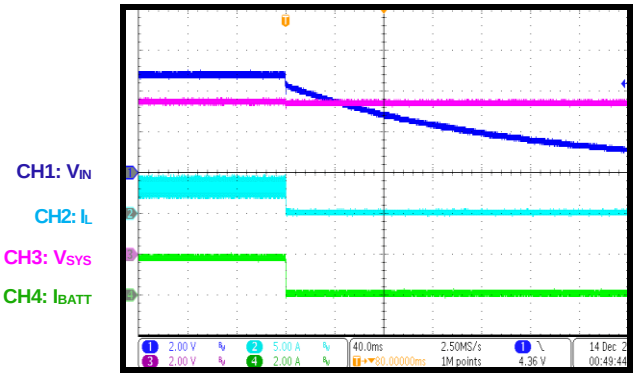
VIN Start-Up

V_{IN} = 5V, V_{BATT} = 7.4V



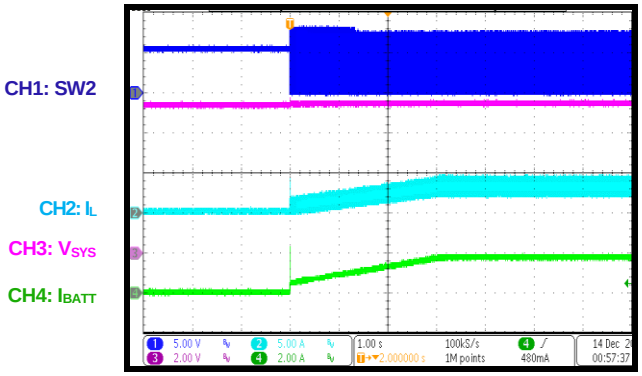
VIN Shutdown

V_{IN} = 5V, V_{BATT} = 7.4V



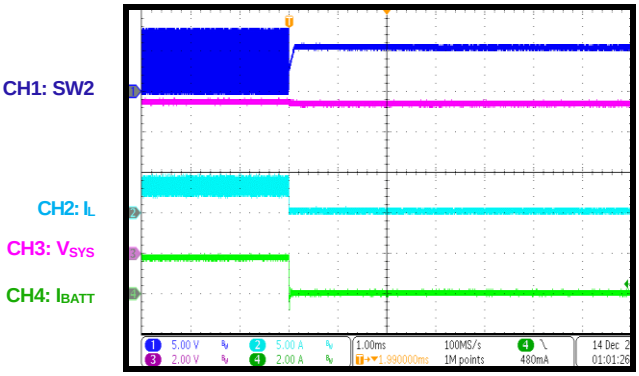
EN Start-Up

V_{IN} = 5V, V_{BATT} = 7.4V



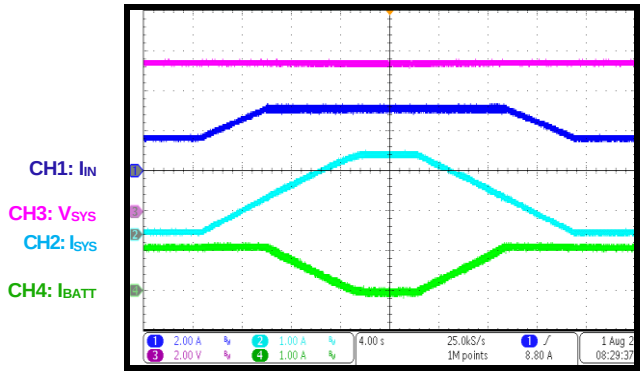
EN Shutdown

V_{IN} = 5V, V_{BATT} = 7.4V



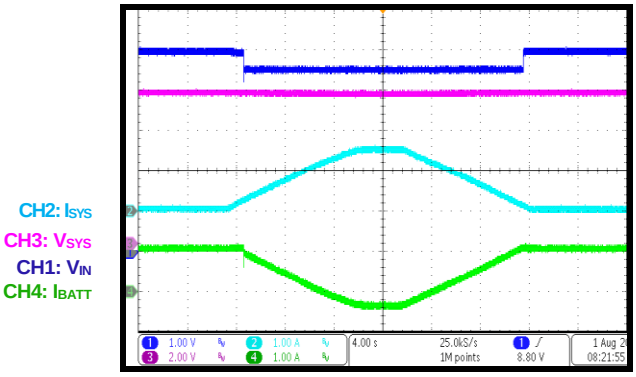
Input Current Limit

V_{IN} = 5V, V_{BATT} = 7.4V, I_{CC} = 1A



Input Voltage Limit

V_{IN} = 5V (2A), V_{BATT} = 7.4V, I_{CC} = 1A

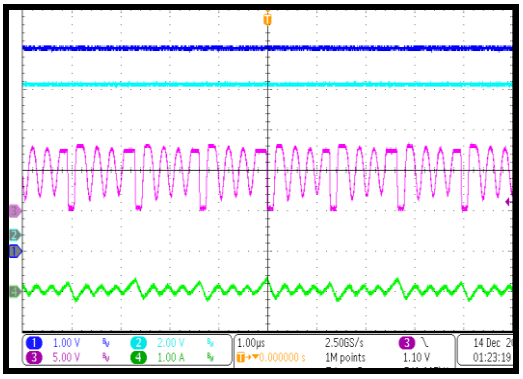


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN_OTG} = 5V, V_{BATT} = 0V to 8.4V, I_{OLIM} = 3A, f_{SW} = 600kHz, L = 1.5µH, T_A = 25°C, unless otherwise noted.

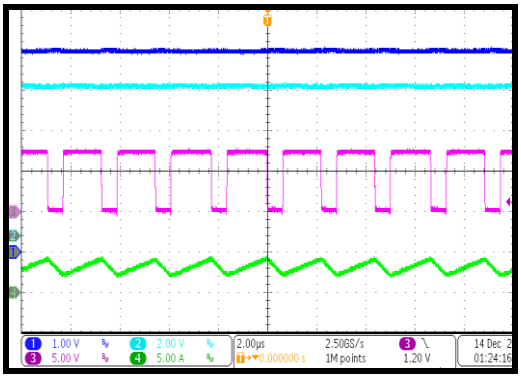
OTG Steady State

V_{BATT} = 7.4V, I_{OTG} = 0A



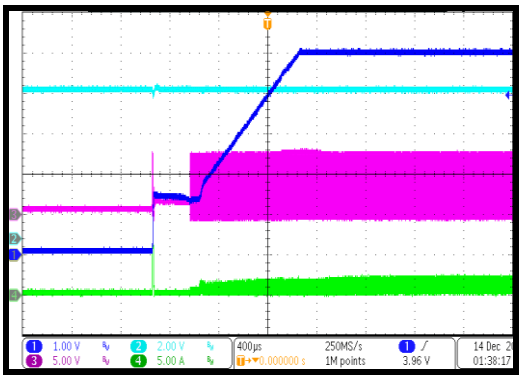
OTG Steady State

V_{BATT} = 7.4V, I_{OTG} = 3A



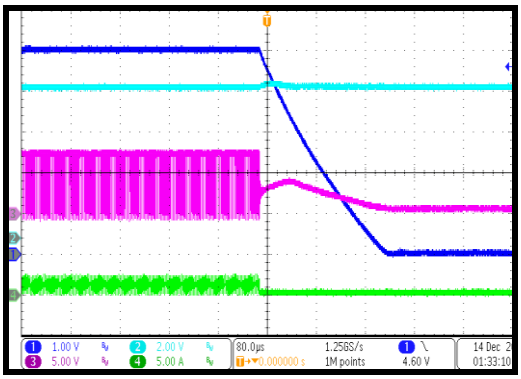
OTG EN Start-Up

V_{BATT} = 7.4V, I_{OTG} = 1A



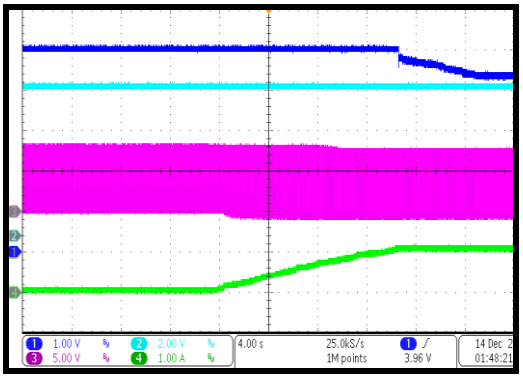
OTG EN Shutdown

V_{BATT} = 7.4V, I_{OTG} = 1A



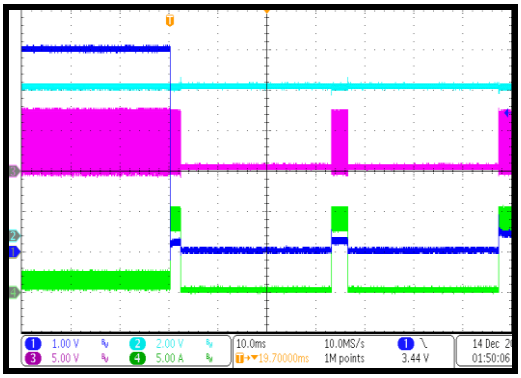
OTG Output Current Limit

V_{BATT} = 7.4V, I_{OLIM} = 1A



OTG SCP

V_{BATT} = 7.4V, I_{OTG} = 1A



FUNCTIONAL BLOCK DIAGRAM

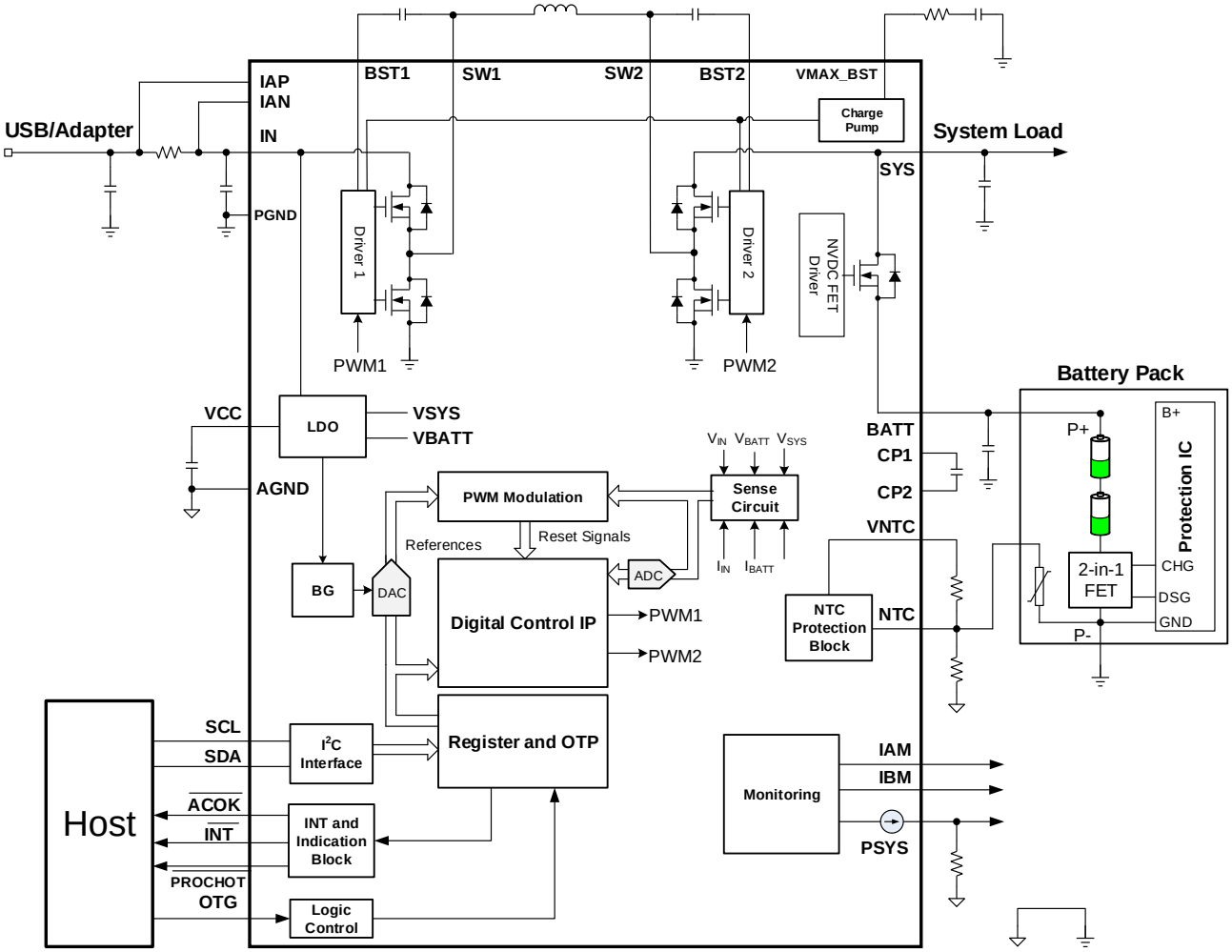


Figure 2: Functional Block Diagram

OPERATION

The MP2650 is a highly integrated buck or boost charger IC with narrow-voltage DC (NVDC) power path management and USB On-The-Go (OTG) charging for battery packs with 2 cells, 3 cells, or 4 cells in series. All power MOSFETs are integrated to provide a compact system solution size which is easy to use.

The IC can accept a wide input voltage (V_{IN}) range (up to 21V) for charging, and it has two operating modes during the charging process: boost charging mode and buck charging mode, depending on V_{IN} and the cell count. In buck charging mode, the buck phase (Q1/Q2) switches, while the high-side MOSFET (HS-FET) (Q3) of the boost phase is always on (see Figure 3).

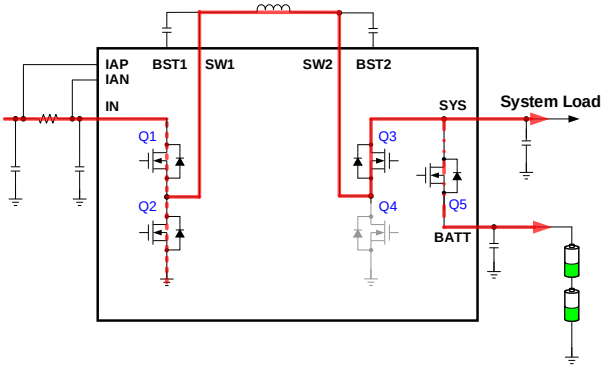


Figure 3: Power MOSFETs' State in Buck Charging Mode

In boost charge mode, the HS-FET (Q1) of the buck phase is always on, while the boost phase (Q3/Q4) switches (see Figure 4).

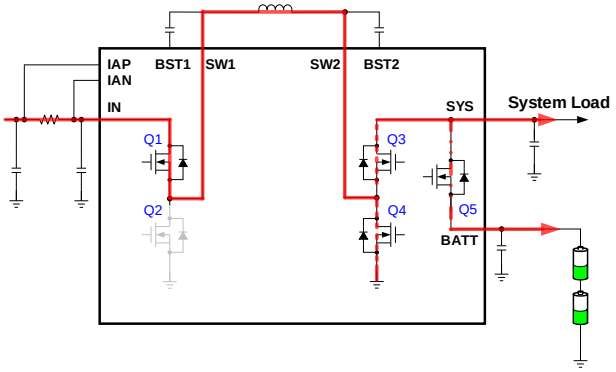


Figure 4: Power MOSFETs' State in Boost Charging Mode

The MP2650 can also provide a constant voltage (5V) at the input in USB OTG mode, and it utilizes a buck converter (Q3/Q4) to provide 5V/3A from the battery pack.

Operation Modes

The MP2650 offers bidirectional operation modes: charging mode and OTG mode.

When the input is present, the device operates in charging mode. The DC/DC stage in the MP2650 operates as a buck or boost charger depending on V_{IN} and the cell count. Table 1 lists the DC/DC operation modes.

Table 1: Operation Modes in Charging

Cell Count	V_{IN}	Boost Charge Threshold	Buck Charge Threshold
2	Rising	V_{IN} > 6.5V	V_{IN} > 8.5V
2	Falling	V_{IN} < 5.75V	V_{IN} < 8V
3	Rising	V_{IN} > 6.5V	V_{IN} > 15V
3	Falling	V_{IN} < 5.75V	V_{IN} < 14.5V
4	Rising	V_{IN} > 6.5V	V_{IN} > 18V
4	Falling	V_{IN} < 5.75V	V_{IN} < 17.5V

In charging mode, the MP2650 measures V_{IN} to automatically monitor the transition between buck and boost operation. When V_{IN} rises from 5V to 20V, the MP2650 charges the battery first in boost mode. Then the device stops switching, unless V_{IN} goes high enough for the device to operate in buck mode.

When the input is absent, the MP2650 powers the system from the battery through the integrated battery FET (BATTFET) (Q5). The MP2650 also provides a constant 5V voltage at the input terminal with I^2C control or hardware pin control, which is USB OTG mode (see Figure 5).

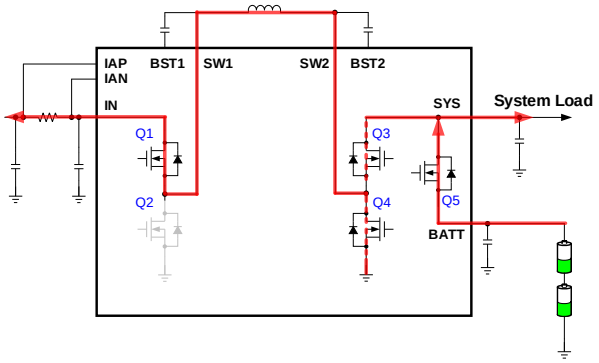


Figure 5: Power FETs' State in OTG Mode

If the IC is not working in charging mode or OTG mode, it enters battery-only mode. Several blocks can be disabled to optimize the battery's quiescent current (I_Q). The BATTFET can be turned off to further minimize the battery's I_Q.

VCC LDO Output

The VCC LDO supplies the internal bias circuits, as well as the DC/DC converter's drivers. The pull-up rail of the open-drain outputs can also be connected to VCC. VCC has a 3.6V output and a 50mA current capability.

VCC is supplied from either V_{IN} or V_{SYS}, depending on which has the higher value. When V_{IN} or V_{SYS} exceed their respective under-voltage lockout (UVLO) thresholds, the sleep comparator, battery depletion comparator, and BATTFET driver are active. In addition, the I^2C interface is ready for communication, and all registers are reset to their default values. The host can access all the registers.

In charging mode, the internal VCC LDO is enabled when the following conditions are valid:

- V_{IN} exceeds its UVLO threshold (V_{IN_UVLO})
- Thermal shutdown is not occurring

Particularly when V_{IN} exceeds V_{IN_UVLO} in 5V boost charge mode, VCC is powered by V_{SYS} after charge termination.

When the input is absent, the VCC LDO is powered by the battery.

Input Under-Voltage Lockout (UVLO) and Input Power-On Reset (POR)

The MP2650 has an input power-on reset (POR) voltage threshold. If V_{IN} drops below V_{IN_POR} and the battery is present, only the BATTFET block (charge pump, battery UVLO, battery over-current protection (OCP)) and the I^2C continue to operate.

The MP2650 also has an input UVLO threshold. If $V_{IN\_POR} < V_{IN} < V_{IN\_UVLO}$, then the internal control block reference, digital-to-analog converter (DAC), and analog-to-digital converter (ADC) start to operate. However, the power stage is not ready until $V_{IN} > V_{IN\_UVLO}$. Then the device can operate in buck or boost charging mode.

Input Power Status Reporting

The IC qualifies the voltage of the input source before start-up. The input source must meet the following requirements:

- $V_{IN\_UVLO} < V_{IN} < V_{IN\_OVLO}$

Once the input power source meets the above conditions, the system status register (REG13h, bit[1]) asserts that the input power is good, and the buck or boost converter is ready to operate.

ACOK Indication

ACOK is an open-drain output pin indicating the presence of an adapter. It indicates whether the charger is operating normally by pulling ACOK to AGND under the following conditions:

- $V_{IN} > V_{IN\_UVLO}$

NVDC Power Path Power Management

The MP2650 is designed as a charger with narrow-voltage DC (NVDC) power path power management, which guarantees the priority of the system power requirement under input plug-out or heavy-load conditions (see Figure 6).

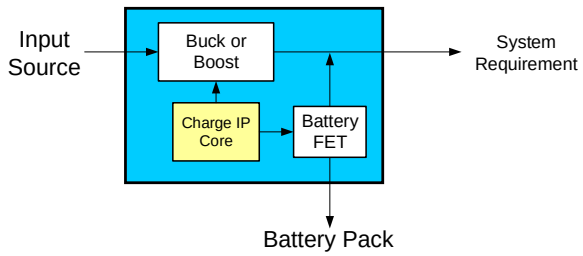


Figure 6: NVDC Power Path Management Structure

The NVDC power path regulates the system voltage (V_{SYS}) within a narrow DC range to provide an optimized system bus voltage for the rails at the system bus. This allows the system to operate even when the battery is completely depleted or removed. When the input source current or voltage limit is reached, power path management automatically reduces the charge current (I_{CHG}) to meet the priority of the system's power requirements. If the system current (I_{SYS}) increases after I_{CHG} is reduced to 0A, supplement mode allows the battery to power the system along with the input power supply. When the input is absent, the system

is powered by the battery via the integrated BATTFET.

When $V_{BATT} > V_{BATT\_UVLO}$ and $V_{IN} < V_{IN\_UVLO}$, the MP2650 operates in battery-only mode. In this mode, the battery FET fully turns on to power the system using the battery.

When OTG is enabled, the battery supplies power to the input side via the buck converter, as well as the system.

When $V_{IN\_OVLO} > V_{IN} > V_{IN\_UVLO}$, the input power supplies the system and charges the battery if charging is enabled. Due to the NVDC structure, when the battery FET is off, V_{SYS} is regulated above the maximum voltage between V_{BATT_PRE} and the battery voltage (V_{BATT}) via V_{TRACK} (see Figure 7). When $V_{BATT} > V_{BATT\_PRE}$, V_{SYS} tracks V_{BATT}.

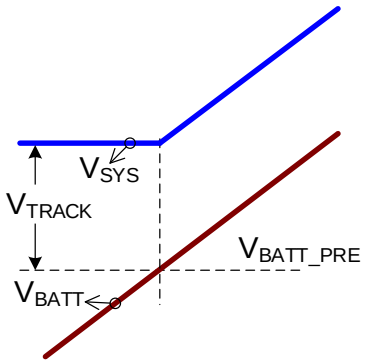


Figure 7: Battery Voltage Tracking

When charging is enabled and no charge fault occurs, BATTFET fully turns on once $V_{BATT} > V_{BATT\_PRE}$ + 140mV (see Figure 8).

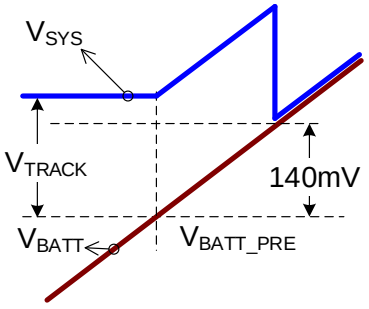


Figure 8: Switching Mode Fast Charging

Input Voltage Limit and Input Current Limit Regulation

To meet the maximum current limit for the USB specifications and avoid overloading the adapter, the MP2650 features both I_{IN} current limiting and V_{IN} limiting.

If the preset I_{IN} limit exceeds the adapter rating, the backup V_{IN} limit loop works to prevent the input source from being overloaded.

IC Thermal Regulation

The IC continuously monitors the internal junction temperature to maximize power delivery and avoid overheating the chip. If the internal junction temperature reaches the preset limit, the IC starts to reduce I_{CHG} to prevent higher power dissipation.

Battery Supplement Mode

When the I_{IN} or V_{IN} limit loop operates, PWM control limits the power from the input. As a result, V_{SYS} and I_{CHG} decrease.

If the system power exceeds the input power, V_{SYS} keeps falling. I_{CHG} drops to 0A or becomes negative, which means the battery must start to discharge and supplement the system. This is called battery supplement mode. In this mode, the system load is powered by the battery and DC/DC converter simultaneously.

Virtual Diode Mode

In battery supplement mode, a virtual diode mode is designed into the IC to optimize the control transition between BATTFET and DC/DC converter. BATTFET enters virtual diode mode under the following conditions:

- $V_{IN} > V_{IN\_UVLO}$
- $V_{SYS} < V_{BATT}$ - 25mV

In virtual diode mode, BATTFET operates as an ideal diode with a 30mV forward voltage (from the battery side to system side). When the system voltage is 25mV below the battery voltage, the gate drive of BATTFET is regulated to keep BATTFET's V_{DS} at about 30mV. As the discharge current increases, BATTFET obtains a stronger gate drive and a smaller $R_{DS(ON)}$ until BATTFET is fully on. The virtual diode exits when V_{SYS} exceeds V_{BATT} by 30mV due to the system's decreasing load current.

USB Suspended Mode

The IC has a USB suspended mode control bit to turn off the DC/DC converter and force the battery to power the system load, regardless of the V_{IN} status.

Charge Cycle

In charge mode, the IC has six control loops to regulate V_{IN}, I_{IN}, V_{SYS}, I_{CHG}, charge voltage, and device junction temperature.

The IC provides four main charging phases: constant current (CC) trickle charge, CC pre-charge, CC fast charge, and constant voltage (CV) charge. These phases are described below.

Constant Current Trickle Charge (Phase 1)

When the input power qualifies as a good power supply, the IC checks V_{BATT} to determine if trickle current charging is required. If V_{BATT} is below V_{BATT_TC}, a trickle charge current is applied to the battery.

Constant Current Pre-Charge (Phase 2)

When V_{BATT} exceeds V_{BATT_TC}, the IC starts to safely pre-charge the deeply depleted battery until V_{BATT} reaches the pre-charge to fast-charge threshold (V_{BATT_PRE}). If V_{BATT_PRE} is not reached before the pre-charge timer (1 hour) expires, then the charge cycle stops and a corresponding timeout fault signal is asserted. The pre-charge current can be configured via the I^2C (REG03h, bits[7:4]).

Constant Current Fast Charge (Phase 3)

If V_{BATT} exceeds V_{BATT_PRE} (set by REG07h, bits[5:4]), the IC enters the CC charge (fast charge) phase. The fast charge current can be configured up to 5A via REG02h, bits[6:0].

Constant Voltage Charge (Phase 4)

When V_{BATT} rises to the battery-full voltage (V_{BATT_REG}) set via REG04h, bits[6:1], I_{CHG} decreases due to battery voltage loop regulation.

The charge cycle is considered complete when I_{CHG} reaches the battery-full termination threshold (I_{TERM}) set via REG03h, bits[3:0], as long as the termination function is enabled. If I_{TERM} is not reached before the safety charge timer expires, then the charge cycle stops and the corresponding timeout fault signal is asserted (see the Safety Timer section on page 25).

Note that during the charging process, the actual I_{CHG} may be below the register setting due to the I_{IN} loop, V_{IN} loop, or thermal regulation. The thermal regulation loop reduces I_{CHG} when the junction temperature exceeds the preset limit. The limit can be configured to be between 60°C and 120°C. The junction temperature regulation threshold can be set via REG05h, bits[1:0].

A new charge cycle starts once all the following conditions are valid:

- The input power is re-plugged
- Battery charging is enabled by the I^2C
- No thermistor fault has occurred
- No battery over-voltage (OV) fault has occurred
- BATTFET is not forced to turn off

Re-plugging the input power or toggling the battery charging control bit can restart a charge cycle, even if a fault has not occurred. The new charge cycle can start with any phase, and the phase is determined by V_{BATT}.

Automatic Recharge

When charging is terminated, the battery may be discharged because of system consumption or the self-discharge function. When V_{BATT} is discharged below the configurable recharge threshold, the IC automatically starts a new charging cycle. If the input power is valid, a manual restart is not required. The charging safety timer resets when the auto-recharge cycle begins.

Battery Over-Voltage Protection (OVP)

The IC provides battery over-voltage protection (OVP). If the battery voltage exceeds the battery OV threshold, charging stops and BATTFET turns off immediately. V_{SYS} is regulated at a value above V_{BATT} via V_{TRACK}.

ADC Conversion and Multiplexer

The MP2650 integrates a 10-bit SAR ADC with 50ksps. In charge mode, the multiplexer measures V_{IN}, I_{IN}, V_{SYS}, V_{BATT}, and I_{CHG}. In OTG mode, the multiplexer measures the OTG output voltage, OTG output current, battery voltage, and current.

Safety Timer

The IC provides both a pre-charge and complete charge safety timer to prevent an extended charging cycle due to abnormal battery conditions. If V_{BATT} is below V_{BATT_PRE}, the total safety timer for both trickle charge and pre-charge is 1 hour. The complete charge safety timer includes a trickle charge and pre-charge timer. The user can configure the complete charge safety timer via the I²C. Note that the safety timer does not operate in discharge mode.

The safety timer is reset at the beginning of a new charging cycle. It can also be reset by sequentially writing 0 then 1 to REG08h, bit[4]. The following actions restart the safety timer:

- A new charge cycle begins
- Writing REG08h, bit[4] from 0 to 1 (charge enabled)
- Writing REG09h, bit[3] from 0 to 1 (safety timer enabled)

The IC can automatically adjust or suspend the timer if any fault occurs.

The timer is suspended if any of the following conditions occurs:

- The battery supplements the system
- System OVP
- An NTC hot or cold fault

If the I_{IN} limit, V_{IN} limit, or thermal regulation limit is reached, the remaining time for the timer can be doubled. Once the condition is removed, the timer returns to its normal value. This function can be enabled or disabled via the I²C.

Impedance Compensation to Accelerate Charging

In the charging cycle, the CV charging stage takes up a significant proportion of the total charging time. To accelerate the charging cycle, it is recommended to remain in the CC charging stage for as long as possible.

The IC allows the user to compensate the intrinsic resistance of the battery by adjusting the charge-full voltage threshold according to I_{CHG} and the internal resistance. In addition, a maximum allowed regulated voltage is also set for safety reasons.

The regulated voltage can be calculated with Equation (1):

$$V_{BATT\_REG}{}^{*} = V_{BATT\_REG} + \mathrm{Min}(I_{CHG} x R_{BATT\_CMP}, V_{CLAMP}) \quad (1)$$

Where V_{BATT_REG}* is the real battery regulation voltage, V_{BATT_REG} is the charge-full voltage set via REG04h, bits[6:1], I_{CHG} is the real-time charge current, and Min means the smaller value between (I_{CHG} x R_{BATT_CAMP}) and (V_{CLAMP}) should be used for the calculation.

Two-Level Input Current Limit

The I_{IN} limit has two thresholds: I_{IN_LIM1} for the lower limit, and I_{IN_LIM2} for the higher limit. I_{IN_LIM2} can only last for t_2, and repeat once in t_1. Figure 9 shows the two current limit levels, as well as the time durations for t_2 and t_1.

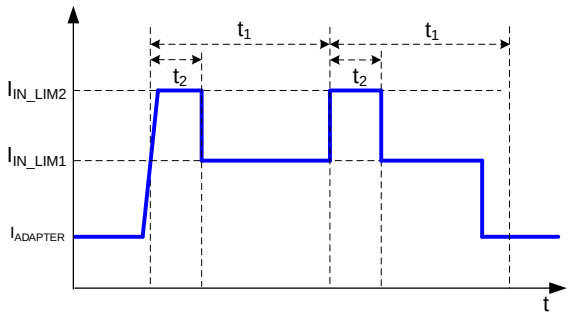


Figure 9: Two-Level Current Limit

The two-level current limit function is initiated when I_{IN} is close to 100mA and below I_{IN_LIM1}. It starts at I_{IN_LIM2} for t_2, and then changes to I_{IN_LIM1} for t_1 before repeating the pattern. This fully utilizes the input adapter surge capability to extend the battery life.

I_{IN_LMT1} and I_{IN_LMT2} can be configured through I²C registers REG00h and REG0Fh, respectively. t_2 and t_1 can be configured through I²C registers REG10h and REG11h, respectively.

System Power Monitor Analog Output (PSYS)

The IC has a PSYS pin to monitor the real-time system power in charging mode. The PSYS pin provides a current signal proportional to the total power consumed by the platform. Estimate the total system power (P_{SYS}) with Equation (2):

$$P_{SYS} = K_{PSYS} x \left(V_{IN} x I_{IN} + V_{BATT} x I_{BATT} \right) \quad (2)$$

Where V_{IN} is the adapter voltage, I_{IN} is the adapter current, V_{BATT} is the battery voltage, and I_{BATT} is the battery discharging current. When the battery is charged, I_{BATT} is a negative value.

PSYS is an analog-controlled current source output that is proportional to the system power, and has a 0.78μA/W gain. The MP2650 also has a 10-bit register that reports the system power, with a resolution of 0.125W/bits. The PSYS function can be enabled or disabled through REG0Bh, bits[1:0].

Current Monitoring (IAM/IBM)

The IC has an IBM pin to obtain the real-time battery current (I_{BATT}) in both charge mode and discharge mode. The IBM voltage (V_{IBM}) is a fraction of the charge current. It indicates the amount of charge current flowing into and out of the battery during charge and discharge mode, respectively. V_{IBM} can be estimated with Equation (3):

$$V_{IBM} = I_{BATT} \times 0.125(V) \quad (3)$$

The IBM pin can report the charge current or discharge current depending on the I²C register setting. Similarly, the MP2650 also monitors I_{IN} during the charging and discharging processes using the IAM pin. The IAM voltage (V_{IAM}) can be calculated with Equation (4):

$$V_{IAM} = I_{IN} \times 0.25(V) \quad (4)$$

The MP2650 also has registers to store I_{IN} (REG1E~1Fh), OTG current (REG22~23h), I_{CHG} (REG1A~1Bh), and discharge current (REG28~29h). When the battery is charged in charge mode, the results in the OTG current and discharge current registers are set to 0. In OTG mode or battery supplement mode, the results in the input current and charge current registers are set to 0.

Processor Hot Interrupt (PROCHOT)

The IC continuously monitors I_{IN}, V_{SYS}, the battery discharge current, input source presence, and whether the battery is present. The PROCHOT pin is pulled low if any of the following conditions occur:

- $I_{IN} > I_{IN\_OCP}$
- $I_{BATT} > I_{BAT\_DMAX}$
- $V_{SYS} < V_{SYS\_UV}$
- Adapter plug-out
- Battery plug-out
- An independent comparator has asserted

The thresholds for I_{IN_OCP}, I_{BAT_DMAX}, and V_{SYS_UV} are configurable via the I²C. To set the PROCHOT assertion threshold for adapter over-current (OC) conditions, write an I_{IN_OCP} command to REG12h. If the adapter current exceeds the I_{IN_OCP} threshold, the PROCHOT signal asserts after the debounce time. The signal latches on for a minimum time, which is configured via REG0Eh (see Figure 10).

V_{SYS_UV} has two optional debouncing times (10μs or 20μs), which can be set via REG0Ch, bit[4]. Other triggering events have the same debouncing time, which can also be set via REG0Eh.

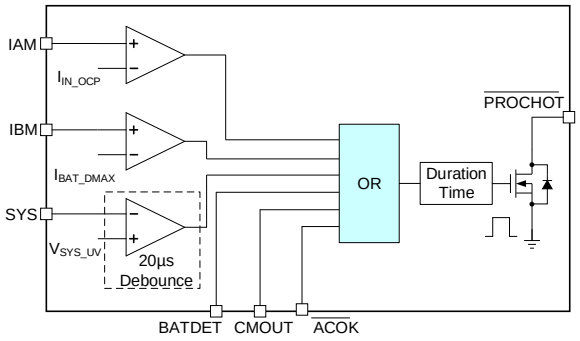


Figure 10: PROCHOT Events

Battery-Only Mode

If the input is absent, OTG mode is disabled, and V_{BATT} exceeds V_{BATT_UVLO}, then BATTFET fully turns on. The 10mΩ BATTFET minimizes the conduction loss. The IC's I_Q is as low as 30μA.

The low on resistance and low I_Q help to extend the battery's runtime.

Light-Load Operation

Under light loads in buck mode, one of the phases can be disabled manually or automatically via the I²C. Light-load operation is designed to optimize the switching frequency (f_{SW}).

When the system current decreases, V_{SYS} rises and t_{ON} shortens. Then t_{OFF} is extended to keep the frequency constant. Finally, t_{OFF} reaches its limit and t_{ON} reaches the minimum on time. If V_{SYS} still increases, the on time is skipped once V_{SYS} exceeds 102% of V_{SYS_REG}. The threshold can be adjusted via REG31h, bits[1:0].

USB On-The-Go (OTG) Mode

In discharge mode, the regulated 5V/3A power is delivered from the battery to the IN pin through a single-phase buck converter.

The IC does not enter OTG mode if the battery is below the configurable battery UVLO threshold. This ensures that the battery is not drained. To enable buck mode, the input voltage at the IN pin must be below 1V.

OTG operation can be enabled when REG08h, bit[5] = 1, and the OTG pin is high. The USB OTG output current can be set between 0A and 3.75A via the I²C (REG07h, bits[3:0]). Buck mode is enabled when all of the following conditions are met:

- $V_{BATT} > V_{BATT\_UVLO}$
- OTG REG08h, bit[5] = 1
- A 30ms delay has completed
- The OTG pin is high
- $V_{IN} < 1V$

If V_{IN} does not exceed V_{OTG_UV} (set by REG0Dh, bits[3:2]) within 30ms while OTG is enabled, a buck fault asserts, and buck mode is disabled until a command that enables OTG operation is reissued.

The IC also features output short-circuit protection (SCP) and output OVP. If the load current approaches the OTG current-limit threshold (set via the I²C) while the IC runs in buck mode, the OTG output current loop dominates, and the converter acts as a current source. If V_{BUS} falls below V_{OTG_UV} for more than 700µs, a buck fault is asserted. The buck is disabled and restarts after a 30ms delay time. Any fault during OTG buck operation sets the fault register (REG14h, bit[6]) to 1.

When both charging and OTG buck mode are enabled, OTG buck mode takes priority.

The IC continuously monitors the voltage at the IN pin in OTG buck mode. If V_{BUS} exceeds V_{OTG_OV} (set via REG0Dh, bits[5:4]), then the IC stops switching and the corresponding fault register is set high to indicate the fault.

Thermal Shutdown Protection

Thermal shutdown protection is also active in OTG mode. If the junction temperature exceeds 150°C, the MP2650 enters thermal shutdown. Once the junction temperature drops below 120°C, the device resumes normal operation.

Host Mode and Default Mode

The IC is a host-controlled device. After POR, the IC starts in the watchdog timer expiration state, or its default mode. All registers revert to their default settings.

Any write to the IC is transmitted to host mode. All of the device parameters can be configured by the host. To keep the device in host mode, the host must reset the watchdog timer regularly by writing 1 to REG08h, bit[6] before the watchdog timer expires. The IC goes back to default mode once the watchdog timer expires.

The MP2650 has a one-time programmable (OTP) memory to program the default value of certain registers after they are assembled.

I²C Interface

The IC uses an I²C-compatible interface that sets flexible charging parameters and reports device statuses instantaneously. The I²C is a bidirectional, two-wire serial interface. Only two bus lines are required: a serial data line (SDA) and a serial clock line (SCL). The device can be considered a master or a slave when performing data transfers. The master is the device that initiates a data transfer on the bus and generates the clock signals to permit the transfer. Any device addressed by the master is considered a slave.

The device operates as a slave device with address 5Ch, and receives control inputs from the master device, such as a microcontroller (MCU) or digital signal processor.

The I²C interface supports both standard mode (up to 100kbits), and fast mode (up to 400kbits). Both SDA and SCL are connected to the positive supply voltage via a current source or pull-up resistor.

When the bus is free, both lines are high. The SDA and SCL pins are open drains.

The data on SDA must be stable during the high period of the clock. The high or low state of the data line can only change when the clock signal on SCL is low. One clock pulse is generated for each data bit transferred (see Figure 11).

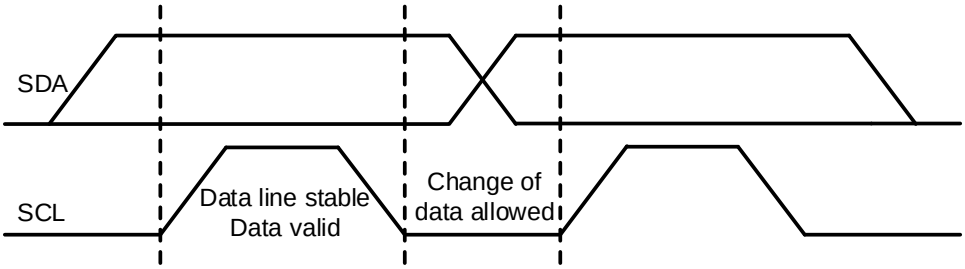


Figure 11: **Bit Transfer on the I²C Bus**

All the transactions begin with a start condition (S) and are terminated by a stop condition (P). A high-to-low transition on SDA while SCL is high defines a start condition. A low-to-high transition on SDA when SCL is high defines a stop condition. Start and stop conditions are always generated by the master. The bus is considered busy after the start condition, and is free after the stop condition (see Figure 12).

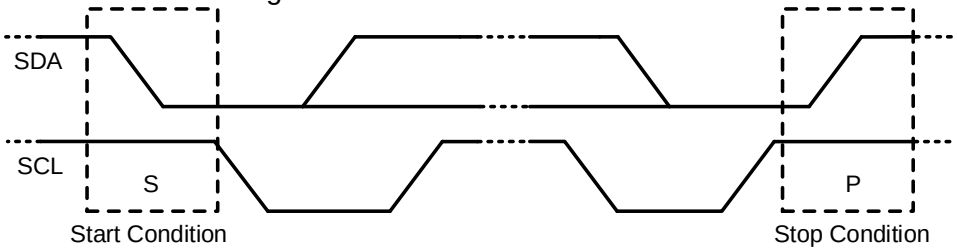


Figure 12: Start and Stop Conditions

Every byte on SDA must be 8 bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte must be followed by an acknowledge (ACK) bit. Data is transferred with the most significant bit (MSB) first (see Figure 13).

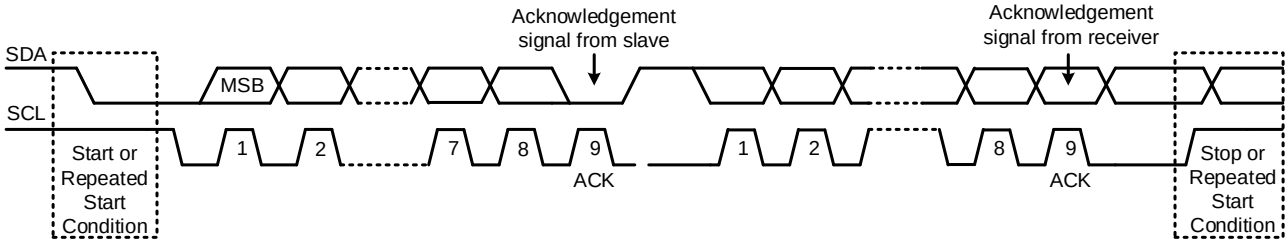


Figure 13: Data Transfer on the I²C Bus

The acknowledgement takes place after every byte. ACK bit allows the receiver to signal to the transmitter that the byte was successfully received and that another byte may be sent. All clock pulses, including the 9th (ACK) clock pulse, are generated by the master.

The transmitter releases SDA during the ACK clock pulse, so the receiver can pull SDA low. If SDA remains high during the 9th clock pulse, this is called a not acknowledge (NACK) signal. The master can then generate either a stop condition to abort the transfer, or a repeated start condition to start a new transfer.

After the process is initiated, a slave address is sent. This address is 7 bits long, followed by an 8th data direction bit (R/W). A 0 indicates a transmission (write), and a 1 indicates a request for data (read). Figure 14 shows the complete data transfer.

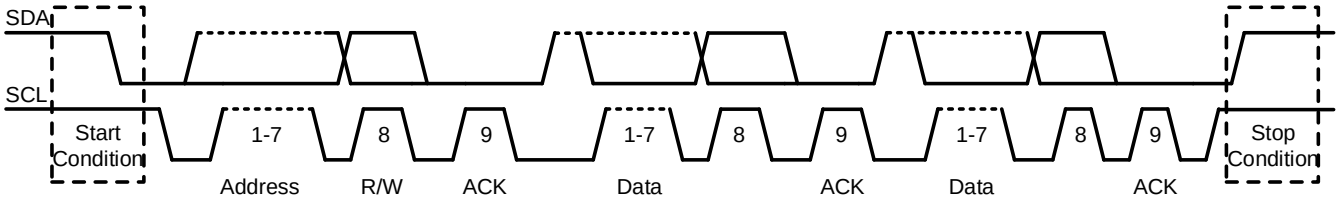


Figure 14: Complete Data Transfer

If the register address is not defined, then the charger IC sends back NACK and reverts to its idle state.

Figure 15, Figure 16, Figure 17, and Figure 18 show examples of I²C processes.

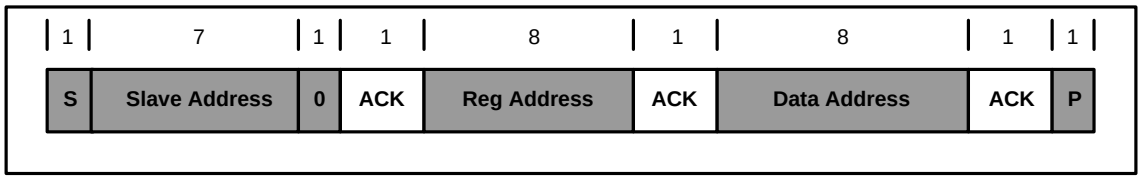


Figure 15: I²C Single Write

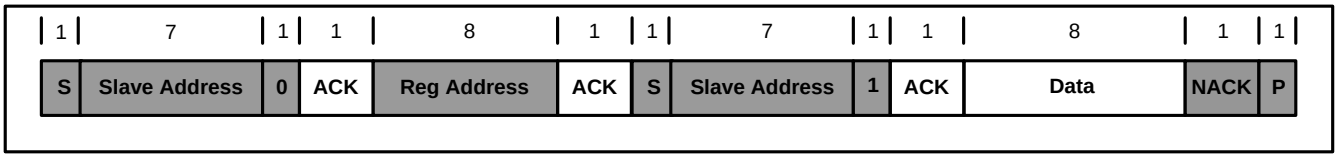


Figure 16: I²C Single Read

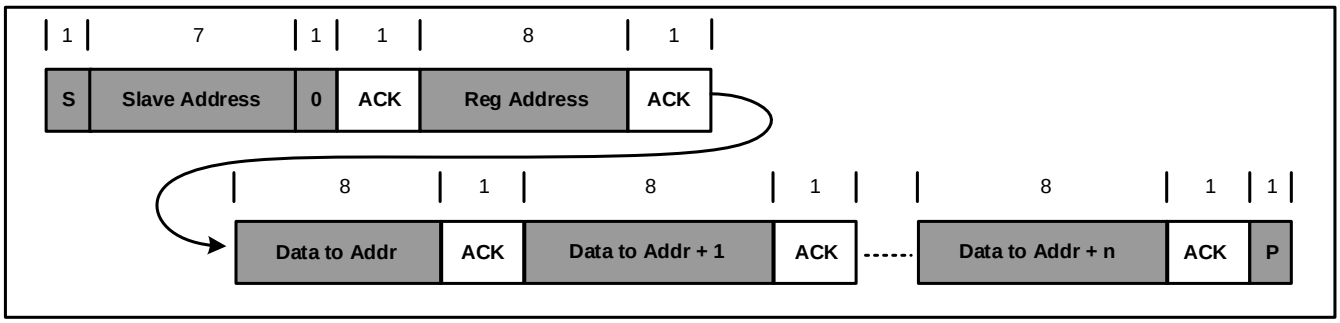


Figure 17: I²C Multi-Write

Figure 18: I²C Multi-Read

REGISTER MAP (Device Address: 5Ch)

Register Name	Register Address	OTP?	R/W	Description
REG00h	0x00	Yes	R/W	Input current limit 1 setting
REG01h	0x01	Yes	R/W	Input voltage limit setting
REG02h	0x02	Yes	R/W	Charge current setting
REG03h	0x03	Yes	R/W	Pre-charge and termination current setting
REG04h	0x04	Yes	R/W	Battery-full voltage and recharge threshold setting
REG05h	0x05	No	R/W	Battery impedance compensation and junction temperature regulation
REG06h	0x06	Yes	R/W	OTG voltage setting
REG07h	0x07	Yes	R/W	Pre-charge threshold and OTG output current limit setting
REG08h	0x08	Yes	R/W	Configuration register 0
REG09h	0x09	Yes	R/W	Configuration register 1
REG0Ah	0x0A	No	R/W	Configuration register 2
REG0Bh	0x0B	Yes	R/W	Configuration register 3
REG0Ch	0x0C	Yes	R/W	Configuration register 4
REG0Dh	0x0D	Yes	R/W	System/OTG under-voltage and over-voltage setting
REG0Eh	0x0E	Yes	R/W	PROCHOT interrupt debounce time and duration time setting
REG0Fh	0x0F	Yes	R/W	Input current limit 2 setting
REG10h	0x10	Yes	R/W	Input current limit 2 duration setting
REG11h	0x11	Yes	R/W	Two-level input current limit period setting
REG12h	0x12	Yes	R/W	Input OCP threshold for triggering PROCHOT
REG13h	0x13	No	R	Status register
REG14h	0x14	No	R	Fault register
REG16~17h	0x16	No	R	ADC result for the battery voltage
REG18~19h	0x18	No	R	ADC result for the system voltage
REG1A~1Bh	0x1A	No	R	ADC result for the battery charge current
REG1C~1Dh	0x1C	No	R	ADC result for the input voltage
REG1E~1Fh	0x1E	No	R	ADC result for the input current
REG20~21h	0x20	No	R	ADC result for the OTG output voltage
REG22~23h	0x22	No	R	ADC result for the OTG output current
REG24~25h	0x24	No	R	ADC result for the junction temperature
REG26~27h	0x26	No	R	ADC result for the system power
REG28~29h	0x28	No	R	ADC result for the battery discharge current
REG2Bh	0x2B	Yes	R/W	Battery OVP deglitch time
REG2Dh	0x2D	Yes	R/W	Battery voltage loop enable
REG30h	0x30	Yes	R/W	Battery pre-charge threshold option
REG31h	0x31	Yes	R/W	System voltage threshold for pulse skipping
REG33h	0x33	Yes	R/W	INT mask for Hi-Z mode entry and exit
REG36h	0x36	Yes	R/W	Analog frequency loop enable
REG40~41h	0x40	No	R	ADC result for NTC voltage
REG48h	0x48	No	R	Hi-Z mode indication

REG00h: Input Current Limit 1 Setting

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	RESERVED	0	N/A	N/A	N/A	Reserved.	Reserved.
6	I_{IN_LIM1}[6]	0	Y	Y	R/W	3200mA.	Default: 1.5A Range: 0mA to 5A Offset: 0mA These bits set the I_{IN} limit setting (RS = 10mΩ). These bits can be configured via the OTP.
5	I_{IN_LIM1}[5]	0	Y	Y	R/W	1600mA.	
4	I_{IN_LIM1}[4]	1	Y	Y	R/W	800mA.	
3	I_{IN_LIM1}[3]	1	Y	Y	R/W	400mA.	
2	I_{IN_LIM1}[2]	1	Y	Y	R/W	200mA.	
1	I_{IN_LIM1}[1]	1	Y	Y	R/W	100mA.	
0	I_{IN_LIM1}[0]	0	Y	Y	R/W	50mA.	

REG01h: Input Voltage Limit Setting

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	V_{IN_MIN}[7]	0	Y	Y	R/W	12800mV.	Default: 4.5V Range: 0V to 25.5V These bits set the V_{IN} limit threshold. These bits can be configured via the OTP.
6	V_{IN_MIN}[6]	0	Y	Y	R/W	6400mV.	
5	V_{IN_MIN}[5]	1	Y	Y	R/W	3200mV.	
4	V_{IN_MIN}[4]	0	Y	Y	R/W	1600mV.	
3	V_{IN_MIN}[3]	1	Y	Y	R/W	800mV.	
2	V_{IN_MIN}[2]	1	Y	Y	R/W	400mV.	
1	V_{IN_MIN}[1]	0	Y	Y	R/W	200mV.	
0	V_{IN_MIN}[0]	1	Y	Y	R/W	100mV.	

REG02h: Charge Current Setting

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	RESERVED	0	N/A	N/A	N/A	Reserved.	Internal use only. Do not change the value of this bit.
6	I_{CC}[6]	0	Y	Y	R/W	3200mA.	Default: 1A Range: 0A to 5A Offset: 0A These bits set I_{CHG}. These bits can be configured via the OTP.
5	I_{CC}[5]	0	Y	Y	R/W	1600mA.	
4	I_{CC}[4]	1	Y	Y	R/W	800mA.	
3	I_{CC}[3]	0	Y	Y	R/W	400mA.	
2	I_{CC}[2]	1	Y	Y	R/W	200mA.	
1	I_{CC}[1]	0	Y	Y	R/W	100mA.	
0	I_{CC}[0]	0	Y	Y	R/W	50mA.	

REG03h: Pre-Charge and Termination Current Setting

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	I_{PRE}[3]	0	Y	Y	R/W	0000: 180mA 0001: 180mA 0010: 180mA 0011: 180mA 0100: 180mA 0101: 240mA 0110: 300mA 0111: 360mA 1000: 420mA 1001: 480mA 1010: 540mA 1011: 600mA 1100: 660mA 1101: 720mA 1110: 780mA 1111: 840mA	Default: 180mA Offset: 0mA These bits set the pre-charge current limit. These bits can be configured via the OTP.
6	I_{PRE}[2]	0	Y	Y	R/W		
5	I_{PRE}[1]	1	Y	Y	R/W		
4	I_{PRE}[0]	1	Y	Y	R/W		
3	I_{TERM}[3]	0	Y	Y	R/W	800mA.	Default: 200mA Range: 0mA to 1500mA Offset: 0mA These bits set the termination current limit. These bits can be configured via the OTP.
2	I_{TERM}[2]	0	Y	Y	R/W	400mA.	
1	I_{TERM}[1]	1	Y	Y	R/W	200mA.	
0	I_{TERM}[0]	0	Y	Y	R/W	100mA.	

REG04h: Battery-Full Voltage and Recharge Threshold Setting

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	RESERVED	0	N/A	N/A	NA	Reserved.	Reserved.
6	V_{BATT_REG}[5]	1	Y	Y	R/W	400mV/cell.	Default: 4.2V/cell Range: 3.7125V/cell to 4.5V/cell Offset: 3.7125V/cell These bits set the charge-full voltage. These bits can be configured via the OTP.
5	V_{BATT_REG}[4]	0	Y	Y	R/W	200mV/cell.	
4	V_{BATT_REG}[3]	0	Y	Y	R/W	100mV/cell.	
3	V_{BATT_REG}[2]	1	Y	Y	R/W	50mV/cell.	
2	V_{BATT_REG}[1]	1	Y	Y	R/W	25mV/cell.	
1	V_{BATT_REG}[0]	1	Y	Y	R/W	12.5mV/cell.	
0	V_{RECH_OS}	0	Y	Y	R/W	0: 100mV/cell 1: 200mV/cell	Offset: 100mV/cell This bit sets the battery recharge threshold offset. This bit can be configured via the OTP.

REG05h: Battery Impedance Compensation and Junction Temperature Regulation

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	R_{BATT}[2]	0	Y	Y	R/W	100mΩ.	Default: 0mΩ Range: 0mΩ to 175mΩ These bits set the IR compensation resistor for each cell. These bits can be configured via the OTP.
6	R_{BATT}[1]	0	Y	Y	R/W	50mΩ.	
5	R_{BATT}[0]	0	Y	Y	R/W	25mΩ.	
4	V_{CLAMP}[2]	0	Y	Y	R/W	120mV.	Default: 0mV Range: 0mV to 210mV Offset: 0mV These bits set the IR compensation resistor clamp for each cell (above the charge voltage limit). These bits can be configured via the OTP.
3	V_{CLAMP}[1]	0	Y	Y	R/W	60mV.	
2	V_{CLAMP}[0]	0	Y	Y	R/W	30mV.	
1	T_{REG}[1]	1	Y	Y	R/W	00: 60°C 01: 80°C 10: 100°C 11: 120°C	Default: 11 These bits set the thermal regulation threshold. This is only for the BATTFET linear charge loop.
0	T_{REG}[0]	1	Y	Y	R/W		

REG06h: OTG Voltage Setting

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	RESERVED	0	N/A	N/A	N/A	Reserved.	Reserved.
6	V_{IN_OTG}[2]	0	Y	Y	R/W	000: 4.75V	Default: 000 These bits set the OTG voltage. These bits can be configured via the OTP.
5	V_{IN_OTG}[1]	0	Y	Y	R/W		
4	V_{IN_OTG}[0]	0	Y	Y	R/W		
3	$V_{IN\_OTG\_OS}$[3]	0	Y	Y	R/W	400mV.	Default: 250mV These bits set the secondary OTG voltage. These bits can be configured via the OTP.
2	$V_{IN\_OTG\_OS}$[2]	1	Y	Y	R/W	200mV.	
1	$V_{IN\_OTG\_OS}$[1]	0	Y	Y	R/W	100mV.	
0	$V_{IN\_OTG\_OS}$[0]	1	Y	Y	R/W	50mV.	

REG07h: Pre-Charge Threshold and OTG Output Current Limit Setting

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	BAT_NUM[1]	0	Y	Y	R/W	00: 2 cells 01: 3 cells 10/11: 4 cells	Default: 00 These bits set the battery cell count in series. These bits can be configured via the OTP.
6	BAT_NUM[0]	0	Y	Y	R/W		
5	V_{BATT_PRE}[1]	0	Y	Y	R/W	Option 1: 00: 2.9V/cell 01: 3V/cell 10: 3.1V/cell 11: 3.2V/cell Option 2: 00: 3.3V/cell 01: 3.4V/cell 10: 3.7V/cell 11: 3.6V/cell	Default: 3V/cell These bits set the battery pre-charge threshold. These bits can be configured via the OTP. The option is set by REG30h, bit[3].
4	V_{BATT_PRE}[0]	1	Y	Y	R/W		
3	I_{OTG}[3]	0	Y	Y	R/W	2000mA.	Default: 1A Range: 0mA to 3.75A Offset: 0mA These bits set the OTG current limit. These bits can be configured via the OTP.
2	I_{OTG}[2]	1	Y	Y	R/W	1000mA.	
1	I_{OTG}[1]	0	Y	Y	R/W	500mA.	
0	I_{OTG}[0]	0	Y	Y	R/W	250mA.	

REG08h: Configuration Register 0

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	REG_RST	0	Y	Y	R/W	0: Keep the current register setting 1: Reset to the default register value and reset the safety timer	Default: 0 This bit sets the register reset. It resets to 0 after the register is reset.
6	WTD_RST	0	Y	Y	R/W	0: Normal 1: Reset	Default: 0 This bit sets the I^2C watchdog timer reset. It resets to 0 after the register is reset.
5	OTG_EN	0	Y	Y	R/W	0: Disable OTG 1: Enable OTG	Default: 0 This bit configures the OTG mode configuration. OTG_EN overrides the charge enable function.
4	CHG_EN	1	Y	Y	R/W	0: Charge disabled (only turn off BATTFET) 1: Charge enabled	Default: 1 This bit configures the charge mode. OTG_EN overrides the CHG_EN enable function. This bit can be configured via the OTP.
3	SUSP_EN	0	Y	Y	R/W	0: Disable SUSP mode 1: Enable SUSP mode (only turn off the DC/DC stage)	Default: 0 This bit configures suspend mode.
2	NTC_ GCOMP_ SEL	1	Y	Y	R/W	0: The OTG/CMIN pin acts as CMIN, the VNTC/CMOUT pin acts as CMOUT, and the NTC/BATDET pin acts as BATDET 1: The OTG/CMIN pin acts as OTG, the VNTC/CMOUT pin acts as VNTC, and the NTC/BATDET pin acts as NTC	Default: 1 This bit selects the NTC and OTG pin functions. When the OTG pin is selected as the independent comparator input, the internal OTG pin is pulled high for OTG mode. This bit can be configured via the OTP.
1	BATTFET_EN	1	Y	Y	R/W	0: Disable charging or discharge 1: Enable charging or discharge	Default: 1 This bit configures the BATTFET.
0	RESERVED	0	N/A	N/A	N/A	Reserved.	Internal use only. Do not change the value of this bit.

REG09h: Configuration Register 1

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	RESERVED	0	N/A	N/A	N/A	Reserved.	Reserved.
6	EN_TERM	1	Y	Y	R/W	0: Disabled 1: Enabled	Default: 1 This bit enables charging termination.
5	WTD[1]	0	Y	Y	R/W	00: Disable the timer 01: 40s 10: 80s 11: 160s	Default: 00 This bit sets the I^2C watchdog timer. These bits can be configured via the OTP.
4	WTD[0]	0	Y	Y	R/W		
3	EN_TMR	1	Y	Y	R/W	0: Disabled 1: Enabled	Default: 1 This bit enables the charging safety timer (both the pre-charge timer and complete charge cycle timer). This bit can be configured via the OTP.
2	CHG_TMR [1]	1	Y	Y	R/W	00: 5 hours 01: 8 hours 10: 12 hours 11: 20 hours	Default: 10 This bit sets the fast-charge timer. These bits can be configured via the OTP.
1	CHG_TMR [0]	0	Y	Y	R/W		
0	TMR2X_EN	0	Y	Y	R/W	0: The safety timer is not doubled during input DPM or thermal regulation 1: The safety timer is doubled during input DPM and thermal regulation	Default: 0 This bit sets the safety timer during input DPM and thermal regulation.

REG0Ah: Configuration Register 2

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	JEITA_ISET	0	Y	Y	R/W	0: 50% 1: 20%	Default: 0 This bit sets the JEITA low-temperature current. It is a percentage of the value set by REG02h, bits[6:0]. This bit is only valid when REG0Ah, bits[5:4] = 00.
6	JEITA_ VSET	0	Y	Y	R/W	0: Set the charge voltage to V_{BATT_REG} - 75mV x cell count 1: Set the charge voltage to V_{BATT_REG} - 150mV x cell count	Default: 0 This bit sets the JEITA high-temperature voltage. It is only valid when REG0Ah, bits[5:4] = 00.
5	NTC_CTRL [1]	1	Y	Y	R/W	00: JEITA 01/10: Standard 11: Disabled	Default: 11 These bits set the NTC protection type.
4	NTC_CTRL [0]	1	Y	Y	R/W		
3	NTC_WARM [1]	0	Y	Y	R/W	00: 58.3% (40°C) 01: 56.1% (45°C) 10: 53.7% (50°C) 11: 51.3% (55°C)	Default: 01 These bits set the NTC warm temperature threshold (a percentage of VNTC).
2	NTC_WARM [0]	1	Y	Y	R/W		
1	NTC_COOL [1]	1	Y	Y	R/W	00: 70.7% (0°C) 01: 69.7% (5°C) 10: 68.6% (10°C) 11: 67.3% (15°C)	Default: 10 These bits set the NTC cool temperature threshold (a percentage of VNTC).
0	NTC_COOL [0]	0	Y	Y	R/W		

REG0Bh: Configuration Register 3

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	RESERVED	0	N/A	N/A	N/A	Reserved.	Reserved.
6	RESERVED	0	N/A	N/A	N/A	Reserved.	Internal use only. Do not change the value of this bit.
5	IBM_CFG	0	N	N	R/W	0: Reflect the battery discharge current 1: Reflect the battery charge current	Default: 0 This bit configures the battery current monitor.
4	SW_FREQ[1]	0	Y	Y	R/W	00: 600kHz 01: 800kHz 10: 1000kHz 11: 1250kHz	Default: 00 These bits set f_{SW}. These bits can be configured via the OTP.
3	SW_FREQ[0]	0	Y	Y	R/W		
2	RESERVED	0	N/A	N/A	N/A	Reserved.	Internal use only. Do not change the value of this bit.
1	PROCHOT/ PSYS_CFG[1]	0	Y	Y	R/W	00: Disable PROCHOT and PSYS functionality (lowest I_Q) 01: Enable PROCHOT and disable PSYS (middle I_Q, since part of the circuit is enabled) 10/11: Enable PROTHOT and PSYS	Default: 00 These bits set the function setting in battery-only mode. These bits can be configured via the OTP.
0	PROCHOT/ PSYS_CFG[0]	0	Y	Y	R/W		

REG0Ch: Configuration Register 4

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	DSCHG_OC_ PROCHOT[2]	1	Y	Y	R/W	000: 0A 001: 2A 010: 4A 011: 6A 100: 8A 101: 10A 110: 12A 111: 14A	Default: 110 These bits set the battery discharge over-current (OC) threshold for PROCHOT assertion. These bits can be configured via the OTP.
6	DSCHG_OC_ PROCHOT[1]	1	Y	Y	R/W		
5	DSCHG_OC_ PROCHOT[0]	0	Y	Y	R/W		
4	VSYS_ PROCHOT_ TDB	0	Y	Y	R/W	0: 10µs 1: 20µs	Default: 0 This bit sets the VSYS under-voltage (UV) trigger PROCHOT debounce time. This bit is set via the OTP.
3	VIRTUAL_ DIODE_EN	0	Y	Y	R/W	0: Disabled 1: Enabled	Default: 0 This bit sets the ideal diode mode when an adapter is absent. This bit can be configured via the OTP.
2	RESERVED	0	N/A	N/A	N/A	Reserved.	Internal use only. Do not change the value of this bit.
1	INDEPENDENT_ COMPARATOR_ CFG	0	Y	Y	R/W	0: PROCHOT does not assert 1: PROCHOT asserts	Default: 0 This bit sets the PROCHOT assertion when the independent comparator outputs low. This bit can be configured via the OTP.
0	INDEPENDENT_ COMPARATOR_ REFERENCE	0	Y	Y	R/W	0: 1.2V 1: 2.1V	Default: 0 This bit sets the independent comparator reference. This bit can be configured via the OTP.

REG0Dh: System/OTG Under-Voltage and Over-Voltage Setting

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	RESERVED	0	N/A	N/A	N/A	Reserved.	Reserved.
6	RESERVED	0	N/A	N/A	N/A	Reserved.	Reserved.
5	V_{OTG_OV}/ V_{SYS_OV}[1]	0	Y	Y	R/W	00: 125% 01: 120% 10: 115% 11: 110%	Default: 00 These bits set the OTG over-voltage (OV) and system OV threshold. It is a percentage of the OTG voltage and V_{SYS}. These bits can be configured via the OTP.
4	V_{OTG_OV}/ V_{SYS_OV}[0]	0	Y	Y	R/W		
3	V_{OTG_UV}/ V_{SYS_UV}[1]	0	Y	Y	R/W	00: 75% 01: 80% 10: 85% 11: 90%	Default: 00 These bits set the OTG under-voltage lockout (UVLO) voltage and system UVLO voltage. It is a percentage of the OTG voltage and V_{SYS}. These bits can be configured via the OTP.
2	V_{OTG_UV}/ V_{SYS_UV}[0]	0	Y	Y	R/W		
1	SYS_UV_ PROCHOT[1]	0	Y	Y	R/W	00: 5.6V 01: 5.8V 10: 6.0V 11: 6.2V	Default: 01 These bits set the low system voltage PROCHOT assertion threshold. These bits can be configured via the OTP.
0	SYS_UV_ PROCHOT[0]	1	Y	Y	R/W		

REG0Eh: PROCHOT Interrupt Debounce Time and Duration Time Setting

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	t_{DEB}[2]	0	Y	Y	R/W	000: 100µs 001: 200µs 010: 300µs 011: 400µs 100: 500µs 101: 600µs 110: 700µs 111: 800µs	Default: 001 These bits set the time before the following assertions are triggered via PROCHOT: ACProchot, DCProchot, absent input, absent battery, and independent comparator output. These bits can be configured via the OTP.
6	t_{DEB}[1]	0	Y	Y	R/W		
5	t_{DEB}[0]	1	Y	Y	R/W		
4	t_{DUR}[3]	0	Y	Y	R/W	1600µs.	Default: 400µs Offset: 200µs These bits set the duration time for the PROCHOT signal once it is asserted. These bits can be configured via the OTP.
3	t_{DUR}[2]	0	Y	Y	R/W	800µs.	
2	t_{DUR}[1]	0	Y	Y	R/W	400µs.	
1	t_{DUR}[0]	1	Y	Y	R/W	200µs.	
0	RESERVED	1	N/A	N/A	N/A	Reserved.	Internal use only. Do not change the value of this bit.

REG0Fh: Input Current Limit 2 Setting

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	RESERVED	0	N/A	N/A	N/A	Reserved.	Reserved.
6	I_{IN_LIM2}[6]	0	Y	Y	R/W	3200mA.	Default: 1.5A Range: 0mA to 5A Offset: 0mA These bits set the second I_{IN} limit (RS1 = 10mΩ). These bits can be configured via the OTP.
5	I_{IN_LIM2}[5]	0	Y	Y	R/W	1600mA.	
4	I_{IN_LIM2}[4]	1	Y	Y	R/W	800mA.	
3	I_{IN_LIM2}[3]	1	Y	Y	R/W	400mA.	
2	I_{IN_LIM2}[2]	1	Y	Y	R/W	200mA.	
1	I_{IN_LIM2}[1]	1	Y	Y	R/W	100mA.	
0	I_{IN_LIM2}[0]	0	Y	Y	R/W	50mA.	

REG10h: Input Current Limit 2 Duration Setting

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	t_{MAX}[6]	0	Y	Y	R/W	12800μs.	Default: 100μs Range: 100μs to 25.5ms Offset: 100μs These bits set the second I_{IN} limit duration (RS = 10mΩ). These bits can be configured via the OTP.
6	t_{MAX}[5]	0	Y	Y	R/W	6400μs.	
5	t_{MAX}[4]	0	Y	Y	R/W	3200μs.	
4	t_{MAX}[3]	0	Y	Y	R/W	1600μs.	
3	t_{MAX}[2]	0	Y	Y	R/W	800μs.	
2	t_{MAX}[1]	0	Y	Y	R/W	400μs.	
1	t_{MAX}[0]	0	Y	Y	R/W	200μs.	
0	RESERVED	1	N/A	N/A	N/A	Reserved.	Internal use only. Do not change the value of this bit.

REG11h: Two-Level Input Current Limit Period Setting

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	t_{PERIOD}[6]	1	Y	Y	R/W	12800µs.	Default: 1111 111 (25.5ms) Range: 100µs to 25.5ms Offset: 100µs These bits set the total time duration of for the second and first I_{IN} limit (RS1 = 10mΩ). These bits can be configured via the OTP.
6	t_{PERIOD}[5]	1	Y	Y	R/W	6400µs.	
5	t_{PERIOD}[4]	1	Y	Y	R/W	3200µs.	
4	t_{PERIOD}[3]	1	Y	Y	R/W	1600µs.	
3	t_{PERIOD}[2]	1	Y	Y	R/W	800µs.	
2	t_{PERIOD}[1]	1	Y	Y	R/W	400µs.	
1	t_{PERIOD}[0]	1	Y	Y	R/W	200µs.	
0	RESERVED	1	N/A	N/A	N/A	Reserved.	Internal use only. Do not change the value of this bit.

REG12h: Input OCP Threshold for Triggering PROCHOT

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	RESERVED	0	N/A	N/A	N/A	Reserved.	Reserved.
6	I_{IN_OCP}[3]	1	Y	Y	R/W	6400mA.	Default: 11.9A Offset: 700mA These bits set the input over-current (OC) threshold. PROCHOT is triggered when I_{IN} exceeds this threshold. These bits can be configured via the OTP.
5	I_{IN_OCP}[2]	1	Y	Y	R/W	3200mA.	
4	I_{IN_OCP}[1]	1	Y	Y	R/W	1600mA.	
3	I_{IN_OCP}[0]	0	Y	Y	R/W	800mA.	
2	RESERVED	1	N/A	N/A	N/A	Reserved.	Internal use only. Do not change the value of this bit.
1	DIG_SKIP_EN	1	Y	Y	R/W	0: Disabled 1: Enabled	When this bit is set to 1, digital skip mode is enabled to skip PWM when the load is light for all loops. This bit can be configured via the OTP.
0	RESERVED	1	N/A	N/A	N/A	Reserved.	Internal use only. Do not change the value of this bit.

REG13h: Status Register

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	BATT_UVLO	0	N/A	N/A	R	0: V_{BATT} UVLO has not occurred 1: V_{BATT} UVLO has occurred	Default: 0 This bit indicates the V_{BATT} under-voltage lockout (UVLO) status. It is set to 0 by default.
6	VSYS_UV	0	N/A	N/A	R	0: The system does not have a UV condition 1: The system has a UV condition	Default: 0 This bit indicates an under-voltage (UV) condition, which triggers short-circuit protection (SCP).
5	RESERVED	0	N/A	N/A	N/A	Reserved.	Reserved.
4	PPM_STAT	0	N/A	N/A	R	0: No DPM 1: VINDPM or IINDPM	Default: 0 This bit indicates the power path management status.
3	CHG_ STAT[1]	0	N/A	N/A	R	00: Not charging 01: Trickle charging or Pre-charging 10: Fast charging 11: Charge termination	Default: 00 These bits indicate the charging status.
2	CHG_ STAT[0]	0	N/A	N/A	R		
1	ACOK	0	N/A	N/A	R	0: V_{IN} not PG 1: V_{IN} PG	Default: 0 This bit indicates the power good (PG) status.
0	VSYS_STAT	0	N/A	N/A	R	0: In VSYSMIN regulation 1: Not in VSYSMIN regulation	Default: 0 This bit indicates the VSYS regulation status.

REG14h: Fault Register

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	WATCHDOG_FAULT	0	N/A	N/A	R	0: Normal operation 1: The watchdog timer has expired	Default: 0 This bit indicates whether a watchdog fault has occurred. It is set to 0 by default.
6	OTG_FAULT	0	N/A	N/A	R	0: Normal operation 1: VBUS is overloaded, or VBUS over-voltage protection (OVP) has occurred	Default: 0 This bit indicates whether an OTG mode fault has occurred. It is set to 0 by default.
5	CHG_FAULT [1]	0	N/A	N/A	R	00: Normal operation 01: Input OVP has occurred 10: Thermal shutdown has occurred 11: The safety timer has expired	Default: 00 These bits indicate whether a charge fault has occurred. They are set to 00 by default.
4	CHG_FAULT [0]	0	N/A	N/A	R		
3	BATT_FAULT	0	N/A	N/A	R	0: Normal operation 1: Battery OVP has occurred	Default: 0 This bit indicates whether a battery fault has occurred. It is set to 0 by default.
2	NTC_FAULT [2]	0	N/A	N/A	R	000: Normal 001: NTC cold 010: NTC cool 011: NTC warm 100: NTC hot	Default: 000 These bits indicate whether an NTC fault has occurred. They are set to 000 by default.
1	NTC_FAULT [1]	0	N/A	N/A	R		
0	NTC_FAULT [0]	0	N/A	N/A	R		

REG16~17h: ADC Battery Voltage Result

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
15	V_{BATT}[9]	N/A	N/A	N/A	R	6400mV.	These bits indicate the ADC conversion of V_{BATT}. For 2 cells: 12.5mV/LSB For 3 cells: 18.75mV/LSB For 4 cells: 25mV/LSB
14	V_{BATT}[8]	N/A	N/A	N/A	R	3200mV.	
13	V_{BATT}[7]	N/A	N/A	N/A	R	1600mV.	
12	V_{BATT}[6]	N/A	N/A	N/A	R	800mV.	
11	V_{BATT}[5]	N/A	N/A	N/A	R	400mV.	
10	V_{BATT}[4]	N/A	N/A	N/A	R	200mV.	
9	V_{BATT}[3]	N/A	N/A	N/A	R	100mV.	
8	V_{BATT}[2]	N/A	N/A	N/A	R	50mV.	
7	V_{BATT}[1]	N/A	N/A	N/A	R	25mV.	
6	V_{BATT}[0]	N/A	N/A	N/A	R	12.5mV.	
5	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
4	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
3	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
2	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
1	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
0	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.

REG18~19h: ADC System Voltage Result

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
15	V_{SYS}[9]	N/A	N/A	N/A	R	6400mV.	These bits indicate the ADC conversion of V_{SYS}. For 2 cells: 12.5mV/LSB For 3 cells: 18.75mV/LSB For 4 cells: 25mV/LSB
14	V_{SYS}[8]	N/A	N/A	N/A	R	3200mV.	
13	V_{SYS}[7]	N/A	N/A	N/A	R	1600mV.	
12	V_{SYS}[6]	N/A	N/A	N/A	R	800mV.	
11	V_{SYS}[5]	N/A	N/A	N/A	R	400mV.	
10	V_{SYS}[4]	N/A	N/A	N/A	R	200mV.	
9	V_{SYS}[3]	N/A	N/A	N/A	R	100mV.	
8	V_{SYS}[2]	N/A	N/A	N/A	R	50mV.	
7	V_{SYS}[1]	N/A	N/A	N/A	R	25mV.	
6	V_{SYS}[0]	N/A	N/A	N/A	R	12.5mV.	
5	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
4	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
3	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
2	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
1	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
0	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.

REG1A~1Bh: ADC Battery Charge Current Result

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
15	I_{CHG}[9]	N/A	N/A	N/A	R	6400mA.	These bits indicate the ADC conversion of I_{CHG}.
14	I_{CHG}[8]	N/A	N/A	N/A	R	3200mA.	
13	I_{CHG}[7]	N/A	N/A	N/A	R	1600mA.	
12	I_{CHG}[6]	N/A	N/A	N/A	R	800mA.	
11	I_{CHG}[5]	N/A	N/A	N/A	R	400mA.	
10	I_{CHG}[4]	N/A	N/A	N/A	R	200mA.	
9	I_{CHG}[3]	N/A	N/A	N/A	R	100mA.	
8	I_{CHG}[2]	N/A	N/A	N/A	R	50mA.	
7	I_{CHG}[1]	N/A	N/A	N/A	R	25mA.	
6	I_{CHG}[0]	N/A	N/A	N/A	R	12.5mA.	
5	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
4	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
3	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
2	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
1	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
0	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.

REG1C~1Dh: ADC Input Voltage Result

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
15	V_{IN}[9]	N/A	N/A	N/A	R	12800mV.	These bits indicate the ADC conversion of V_{IN}.
14	V_{IN}[8]	N/A	N/A	N/A	R	6400mV.	
13	V_{IN}[7]	N/A	N/A	N/A	R	3200mV.	
12	V_{IN}[6]	N/A	N/A	N/A	R	1600mV.	
11	V_{IN}[5]	N/A	N/A	N/A	R	800mV.	
10	V_{IN}[4]	N/A	N/A	N/A	R	400mV.	
9	V_{IN}[3]	N/A	N/A	N/A	R	200mV.	
8	V_{IN}[2]	N/A	N/A	N/A	R	100mV.	
7	V_{IN}[1]	N/A	N/A	N/A	R	50mV.	
6	V_{IN}[0]	N/A	N/A	N/A	R	25mV.	
5	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
4	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
3	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
2	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
1	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
0	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.

REG1E~1Fh: ADC Input Current Result

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
15	I_{IN}[9]	N/A	N/A	N/A	R	3200mA.	These bits indicate the ADC conversion of I_{IN}.
14	I_{IN}[8]	N/A	N/A	N/A	R	1600mA.	
13	I_{IN}[7]	N/A	N/A	N/A	R	800mA.	
12	I_{IN}[6]	N/A	N/A	N/A	R	400mA.	
11	I_{IN}[5]	N/A	N/A	N/A	R	200mA.	
10	I_{IN}[4]	N/A	N/A	N/A	R	100mA.	
9	I_{IN}[3]	N/A	N/A	N/A	R	50mA.	
8	I_{IN}[2]	N/A	N/A	N/A	R	25mA.	
7	I_{IN}[1]	N/A	N/A	N/A	R	12.5mA.	
6	I_{IN}[0]	N/A	N/A	N/A	R	6.25mA.	
5	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
4	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
3	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
2	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
1	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
0	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.

REG20~21h: ADC OTG Output Voltage Result

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
15	V_{IN_OTG}[9]	N/A	N/A	N/A	R	12800mV.	These bits indicate the ADC conversion of the OTG voltage.
14	V_{IN_OTG}[8]	N/A	N/A	N/A	R	6400mV.	
13	V_{IN_OTG}[7]	N/A	N/A	N/A	R	3200mV.	
12	V_{IN_OTG}[6]	N/A	N/A	N/A	R	1600mV.	
11	V_{IN_OTG}[5]	N/A	N/A	N/A	R	800mV.	
10	V_{IN_OTG}[4]	N/A	N/A	N/A	R	400mV.	
9	V_{IN_OTG}[3]	N/A	N/A	N/A	R	200mV.	
8	V_{IN_OTG}[2]	N/A	N/A	N/A	R	100mV.	
7	V_{IN_OTG}[1]	N/A	N/A	N/A	R	50mV.	
6	V_{IN_OTG}[0]	N/A	N/A	N/A	R	25mV.	
5	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
4	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
3	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
2	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
1	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
0	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.

REG22~23h: ADC OTG Output Current Result

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
15	I_{OTG}[9]	N/A	N/A	N/A	R	3200mA.	These bits indicate the ADC conversion of the OTG current.
14	I_{OTG}[8]	N/A	N/A	N/A	R	1600mA.	
13	I_{OTG}[7]	N/A	N/A	N/A	R	800mA.	
12	I_{OTG}[6]	N/A	N/A	N/A	R	400mA.	
11	I_{OTG}[5]	N/A	N/A	N/A	R	200mA.	
10	I_{OTG}[4]	N/A	N/A	N/A	R	100mA.	
9	I_{OTG}[3]	N/A	N/A	N/A	R	50mA.	
8	I_{OTG}[2]	N/A	N/A	N/A	R	25mA.	
7	I_{OTG}[1]	N/A	N/A	N/A	R	12.5mA.	
6	I_{OTG}[0]	N/A	N/A	N/A	R	6.25mA.	
5	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
4	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
3	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
2	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
1	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
0	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.

REG24~25h: ADC Junction Temperature Result

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
15	TJ[9]	N/A	N/A	N/A	R	512.	These bits indicate the ADC conversion of the IC's junction temperature (T_J). T_J can be calculated with the following equation: $T_J = 903 - 2.578 \times T$ (°C)
14	TJ[8]	N/A	N/A	N/A	R	256.	
13	TJ[7]	N/A	N/A	N/A	R	128.	
12	TJ[6]	N/A	N/A	N/A	R	64.	
11	TJ[5]	N/A	N/A	N/A	R	32.	
10	TJ[4]	N/A	N/A	N/A	R	16.	
9	TJ[3]	N/A	N/A	N/A	R	8.	
8	TJ[2]	N/A	N/A	N/A	R	4.	
7	TJ[1]	N/A	N/A	N/A	R	2.	
6	TJ[0]	N/A	N/A	N/A	R	1.	
5	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
4	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
3	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
2	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
1	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
0	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.

REG26~27h: ADC System Power Result

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
15	P_{SYS}[9]	N/A	N/A	N/A	R	64W.	These bits indicate the ADC conversion of the system power.
14	P_{SYS}[8]	N/A	N/A	N/A	R	32W.	
13	P_{SYS}[7]	N/A	N/A	N/A	R	16W.	
12	P_{SYS}[6]	N/A	N/A	N/A	R	8W.	
11	P_{SYS}[5]	N/A	N/A	N/A	R	4W.	
10	P_{SYS}[4]	N/A	N/A	N/A	R	2W.	
9	P_{SYS}[3]	N/A	N/A	N/A	R	1W.	
8	P_{SYS}[2]	N/A	N/A	N/A	R	0.5W.	
7	P_{SYS}[1]	N/A	N/A	N/A	R	0.25W.	
6	P_{SYS}[0]	N/A	N/A	N/A	R	0.125W.	
5	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
4	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
3	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
2	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
1	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
0	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.

REG28~29h: ADC Battery Discharge Current Result

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
15	I_{BATT_DSG}[9]	N/A	N/A	N/A	R	6400mA.	These bits indicate the ADC conversion of the battery discharge current.
14	I_{BATT_DSG}[8]	N/A	N/A	N/A	R	3200mA.	
13	I_{BATT_DSG}[7]	N/A	N/A	N/A	R	1600mA.	
12	I_{BATT_DSG}[6]	N/A	N/A	N/A	R	800mA.	
11	I_{BATT_DSG}[5]	N/A	N/A	N/A	R	400mA.	
10	I_{BATT_DSG}[4]	N/A	N/A	N/A	R	200mA.	
9	I_{BATT_DSG}[3]	N/A	N/A	N/A	R	100mA.	
8	I_{BATT_DSG}[2]	N/A	N/A	N/A	R	50mA.	
7	I_{BATT_DSG}[1]	N/A	N/A	N/A	R	25mA.	
6	I_{BATT_DSG}[0]	N/A	N/A	N/A	R	12.5mA.	
5	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
4	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
3	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
2	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
1	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
0	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.

REG2Bh: Battery OVP Deglitch Time

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	RESERVED	0	N/A	N/A	N/A	Reserved.	Internal use only. Do not change the value of this bit.
6	RESERVED	0	N/A	N/A	N/A	Reserved.	Internal use only. Do not change the value of this bit.
5	RESERVED	0	N/A	N/A	N/A	Reserved.	Internal use only. Do not change the value of this bit.
4	RESERVED	0	N/A	N/A	N/A	Reserved.	Internal use only. Do not change the value of this bit.
3	RESERVED	0	N/A	N/A	N/A	Reserved.	Internal use only. Do not change the value of this bit.
2	RESERVED	0	N/A	N/A	N/A	Reserved.	Internal use only. Do not change the value of this bit.
1	RESERVED	0	N/A	N/A	N/A	Reserved.	Internal use only. Do not change the value of this bit.
0	VBATT_OVP_DGL	1	Y	Y	R/W	0: 200µs 1: 1µs	Default: 1 This bit can be configured via the OTP.

REG2Dh: Battery Voltage Loop Enable

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
6	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
5	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
4	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
3	RESERVED	0	N/A	N/A	N/A	Reserved.	Internal use only. Do not change the value of this bit.
2	RESERVED	0	N/A	N/A	N/A	Reserved.	Internal use only. Do not change the value of this bit.
1	RESERVED	1	N/A	N/A	N/A	Reserved.	Internal use only. Do not change the value of this bit.
0	VBATT_LP_EN	1	Y	Y	R/W	0: Disabled 1: Enabled	This bit can be configured via the OTP.

REG30h: Battery Pre-Charge Threshold Option

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
6	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
5	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
4	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
3	VBATT_PRE_SEL	0	Y	Y	R/W	0: Option 1 1: Option 2	Default: 0 This bit can be configured via the OTP.
2	RESERVED	1	N/A	N/A	N/A	Reserved.	Internal use only. Do not change the value of this bit.
1	RESERVED	0	N/A	N/A	N/A	Reserved.	Internal use only. Do not change the value of this bit.
0	RESERVED	0	N/A	N/A	N/A	Reserved.	Internal use only. Do not change the value of this bit.

REG31h: System Voltage Threshold for Pulse Skipping

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
6	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
5	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
4	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
3	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
2	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
1	VSYS_SKIP [1]	0	Y	Y	R/W	00: 102% 01: 103% 10: 104% 11: 101%	Default: 00 These bits can be configured via the OTP.
0	VSYS_SKIP[0]	0	Y	Y	R/W		

REG33h: INT Mask for Hi-Z Mode Entry and Exit

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
6	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
5	RESERVED	0	N/A	N/A	N/A	Reserved.	Internal use only. Do not change the value of this bit.
4	RESERVED	1	N/A	N/A	N/A	Reserved.	Internal use only. Do not change the value of this bit.
3	RESERVED	0	N/A	N/A	N/A	Reserved.	Internal use only. Do not change the value of this bit.
2	HIZ_INT_MASK	1	Y	Y	R/W	0: Masked 1: Not masked	Default: 1 This bit configures the INT output for Hi-Z mode entry and exit. This bit can be configured via the OTP.
1	RESERVED	0	N/A	N/A	N/A	Reserved.	Internal use only. Do not change the value of this bit.
0	RESERVED	1	N/A	N/A	N/A	Reserved.	Internal use only. Do not change the value of this bit.

REG36h: Analog Frequency Loop Enable

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	RESERVED	1	N/A	N/A	N/A	Reserved.	Internal use only. Do not change the value of this bit.
6	RESERVED	1	N/A	N/A	N/A	Reserved.	Internal use only. Do not change the value of this bit.
5	RESERVED	0	N/A	N/A	N/A	Reserved.	Internal use only. Do not change the value of this bit.
4	RESERVED	1	N/A	N/A	N/A	Reserved.	Internal use only. Do not change the value of this bit.
3	RESERVED	0	N/A	N/A	N/A	Reserved.	Internal use only. Do not change the value of this bit.
2	RESERVED	1	N/A	N/A	N/A	Reserved.	Internal use only. Do not change the value of this bit.
1	FS_LOOP_EN	0	Y	Y	R/W	0: Disabled 1: Enabled	This bit enables the analog frequency loop. When the loop is disabled, an alternative t_{OFF} calculation calibrates f_{SW}. This bit can be configured via the OTP.
0	RESERVED	1	N/A	N/A	N/A	Reserved.	Internal use only. Do not change the value of this bit.

REG40~41h: ADC Result for NTC Voltage

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
15	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
14	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
13	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
12	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
11	NTC[11]	N/A	N/A	N/A	R	2048.	These bits indicate the ADC conversion of the NTC voltage vs. the reference voltage (1.6V). The real NTC voltage can be calculated with the following equation: NTC[11:0] x 1.6V / 4096
10	NTC[10]	N/A	N/A	N/A	R	1024.	
9	NTC[9]	N/A	N/A	N/A	R	512.	
8	NTC[8]	N/A	N/A	N/A	R	256.	
7	NTC[7]	N/A	N/A	N/A	R	128.	
6	NTC[6]	N/A	N/A	N/A	R	64.	
5	NTC[5]	N/A	N/A	N/A	R	32.	
4	NTC[4]	N/A	N/A	N/A	R	16.	
3	NTC[3]	N/A	N/A	N/A	R	8.	
2	NTC[2]	N/A	N/A	N/A	R	4.	
1	NTC[1]	N/A	N/A	N/A	R	2.	
0	NTC[0]	N/A	N/A	N/A	R	1.	

REG48h: Hi-Z Mode Indication (DC/DC Switcher is Off)

Bit	Name	Default	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
6	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
5	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
4	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
3	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
2	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
1	RESERVED	N/A	N/A	N/A	N/A	Reserved.	Reserved.
0	HI-Z_MODE	0	N/A	N/A	R	0: Buck charge or boost charge mode 1: Hi-Z mode	This bit indicates the status of the DC/DC stage.

APPLICATION INFORMATION

Selecting the Input Current-Sense Filter

The MP2650 has an I_{IN} loop that limits the output current drawn from the USB port. An external current-sense resistor is required to sense the average I_{IN}. The I_{IN} value sensed through IAP and IAN covers the ripple current and improves the I_{IN} accuracy and loop stability.

Figure 19 shows a recommended application that can filter noise.

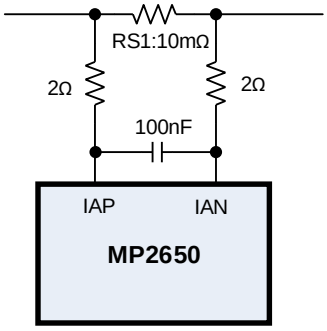


Figure 19: Input Current-Sense Filter

Selecting the Input Capacitor

The input capacitor from the typical application circuit absorbs the maximum ripple current from the PWM converter (see Figure 23 on page 63). The worst-case RMS ripple current is half of the output current when the duty cycle is 50% in buck mode. The RMS ripple current can be estimated with Equation (5):

$$I_{CIN\_RMS} = I_{SYS} x \frac{\sqrt{V_{SYS} x (V_{IN} - V_{SYS})}}{V_{IN}} \quad (5)$$

Low-ESR ceramic capacitors with X7R or X5R dielectrics are recommended to be the input decoupling capacitor, and should be placed as close as possible to IN and PGND. Their voltage rating must exceed the normal V_{IN} level. A capacitor with a minimum 25V rating is recommended for applications with a 20V V_{IN}.

Selecting the VMAX_BST Output Capacitor

The MP2650 has an integrated charge pump to power the HS-FET driver. An external output capacitor must be placed between the VMAX_BST pin and PGND to act as an output capacitor for the integrated charge pump. In addition to the charge pump output, several other paths can supplement the output capacitor (see Figure 20). To limit the inrush current flowing into the capacitor during input power or battery hot insertion, place an additional 100Ω resistor in series with the charge pump output capacitor.

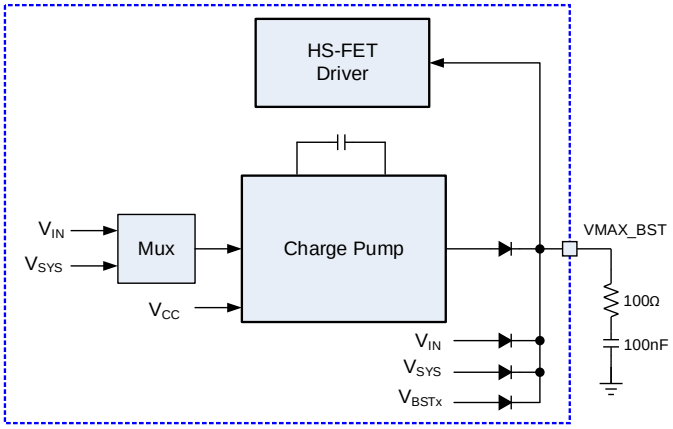


Figure 20: VMAX_BST Circuit Diagram

VCC Decoupling Capacitor

VCC is an internal LDO output. An external 10µF decoupling capacitor must be placed between VCC and AGND.

INT and PROCHOT Pull-Up

Both the $\overline{\text{INT}}$ and $\overline{\text{PROCHOT}}$ pins are open-drain outputs that interrupt operation if any status or faults occurs. To deliver high logic, these pins must be pulled up to an external power source with 10kΩ to 100kΩ resistors.

NTC Sense Resistor Divider

In real applications, an external NTC thermistor must be placed close to the battery to sense the battery's temperature. The MP2650 measures the battery temperature by monitoring the voltage ratio between the NTC and VNTC pins (see Figure 21). Every temperature corresponds to a voltage ratio. The MP2650 has four temperature thresholds to satisfy JEITA requirements.

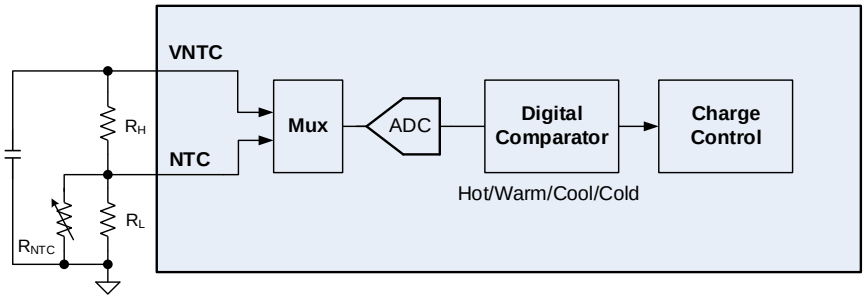


Figure 21: Temperature Sensing

For a given NTC thermistor, the NTC hot and cold temperature points can be calculated with Equation (6) and Equation (7), respectively:

$$\frac{\frac{R_L x R_{NTC\_HOT}}{R_L + R_{NTC\_HOT}}}{R_H + \frac{R_L x R_{NTC\_HOT}}{R_L + R_{NTC\_HOT}}} = \frac{V_{HOT}}{V_{VNTC}} \quad (6)$$

$$\frac{\frac{R_L x R_{NTC\_COLD}}{R_L + R_{NTC\_COLD}}}{R_H + \frac{R_L x R_{NTC\_COLD}}{R_L + R_{NTC\_COLD}}} = \frac{V_{COLD}}{V_{VNTC}} \quad (7)$$

Where R_{NTC_HOT} is the thermistor value at the expected hot temperature protection point, and R_{NTC_COLD} is the thermistor value at the expected cold temperature protection point.

V_{HOT} / V_{VNTC} and V_{COLD} / V_{VNTC} are 48.3% and 71.1%, respectively.

Assume the expected hot and cold temperature thresholds are 60°C and 0°C. Using a 104AT thermistor as an example, the thermistor values are:

- R_{NTC_COLD} = 390.3kΩ
- R_{NTC_HOT} = 19.72kΩ

R_H and R_L can be calculated with Equation (6) and Equation (7). In this scenario, R_H = 13.79kΩ and R_L = 37.15kΩ.

Selecting the Inductor

Inductor selection is a tradeoff between cost, size, and efficiency. A lower-value inductor offers a smaller size, but results in higher ripple current, magnetic hysteresis loss, and required output capacitance. The inductor ripple current should not exceed 30% of the maximum load current under the worst-case conditions.

The MP2650 has three options for f_{SW}. A higher f_{SW} allows for the use of lower-value inductors and capacitors. The inductor saturation current should exceed the load current plus half the ripple current. The recommended inductors are based on a 50% current ripple.

The inductor ripple current in buck operation depends on V_{IN}, f_{SW}, the duty cycle, and inductance. The inductance (L) can be estimated with Equation (8):

$$L = \frac{V_{IN} - V_{SYS}}{\Delta I_L} x \frac{V_{SYS}}{V_{IN} x f_{SW}} \quad (8)$$

The peak inductor current (I_{PEAK}) can be calculated with Equation (9):

$$I_{PEAK} = I_{LOAD(MAX)} + \frac{\Delta I_L}{2} \quad (9)$$

Where V_{IN} is the input voltage, V_{SYS} is the system voltage, f_{SW} is the switching frequency, and ΔI_L is the expected inductor current ripple.

Table 2 on page 61 lists how to select the inductance based on different voltages in buck mode.

Table 2: Inductances for Buck Mode

Specs	Inductance Selection				
V_{IN}	Calculations	L_{MIN}	L	I_{SAT}	DCR (mΩ)
9V	$L=\frac{V_{IN}-V_{SYS}}{\Delta I_L} \times \frac{V_{SYS}}{V_{IN} \times f_{SW}}$ ΔI_L = 0.5 x I_{SYS} = 3A f_{SW} = 800kHz	0.65µH	1.5µH	>6.7	<20
12V		1.2µH	1.5µH	>7.1	<20
15V		1.5µH	1.5µH	>7.5	<20
20V		2.0µH	2.2µH	>7.4	<20

When the MP2650 operates in boost mode, the required inductance (L) can be estimated with Equation (10):

$$L = \frac{V_{IN} \times (V_{SYS} - V_{IN})}{V_{SYS} \times f_{SW} \times \Delta I_L} \quad (10)$$

The peak inductor current (I_{PEAK}) can be estimated with Equation (11):

$$I_{PEAK} = I_{IN(MAX)} + \frac{\Delta I_L}{2} \quad (11)$$

Table 3 lists how to select the inductance based on different voltages in boost mode.

Table 3: Inductances for Boost Mode

Specs	Inductance Selection				
V_{IN}	Calculations	L_{MIN}	L	I_{SAT}	DCR (mΩ)
5V	$L = \frac{V_{IN} \times (V_{SYS} - V_{IN})}{V_{SYS} \times f_{SW} \times \Delta I_L}$ ΔI_L = 0.5 x I_{IN} = 2.5A f_{SW} = 800kHz	1.1µH	1.5µH	>7	<20

A 1.5µH inductor with a >7.5A saturation current is recommended for most specifications. However, for applications that allow for a higher ripple current, a lower-value inductor can be used to reduce PCB size.

Selecting the System Capacitor

The system output capacitor (C_{SYS}) from the typical application circuit is parallel to the SYS load (see Figure 23 on page 63). C_{SYS} absorbs the high-frequency switching ripple current and smooths the output voltage. Its impedance must be below that of the system load to ensure that it absorbs the ripple current.

Ceramic capacitors are recommended for their low ESR and small size, which allows the ESR of the output capacitor to be ignored.

The output voltage ripple can be estimated with Equation (12):

$$\frac{\Delta V_{SYS}}{V_{SYS}} = \frac{1 - \frac{V_{SYS}}{V_{IN}}}{8 \times C_{SYS} \times f_{SW}^2 \times L} \quad (12)$$

The maximum output voltage ripple occurs at the minimum V_{SYS} and the maximum V_{IN}. Assume that a ±0.2% output ripple voltage should be obtained in CCM.

C_{SYS} can be estimated with Equation (13):

$$C_{SYS} = \frac{1 - \frac{V_{SYS}}{V_{IN}}}{8 \times f_{SW}^2 \times L \times \frac{\Delta V_{SYS}}{V_{SYS}}} \quad (13)$$

Based on Equation (13), C_{SYS} must be 44µF.

To further improve loop stability, use a minimum 60µF capacitor. For an output capacitor, the recommended ceramic capacitor is 25V, with X7R or X5R dielectrics.

PCB Layout Guidelines

Efficient PCB layout is critical for specified noise, efficiency, and stability requirements. A minimum 4-layer PCB is recommended to improve thermal performance. For the best results, refer to Figure 22 and follow the guidelines below:

1. Connect the VMAX_BST capacitor to PGND. Place one 100Ω resistor in series with the VMAX_BST capacitor.
2. Connect AGND to PGND to each decoupling capacitor via a single-point connection.
3. Place a 470nF capacitor between the CP1 and CP2 pins.
4. Place the VCC capacitor close to the VCC and AGND pins.
5. Use a Kelvin connection for the input current-sense resistor.
6. Place capacitors between VIN and PGND as close as possible to the pins.
7. For the input current sense, use CM and DM filters.

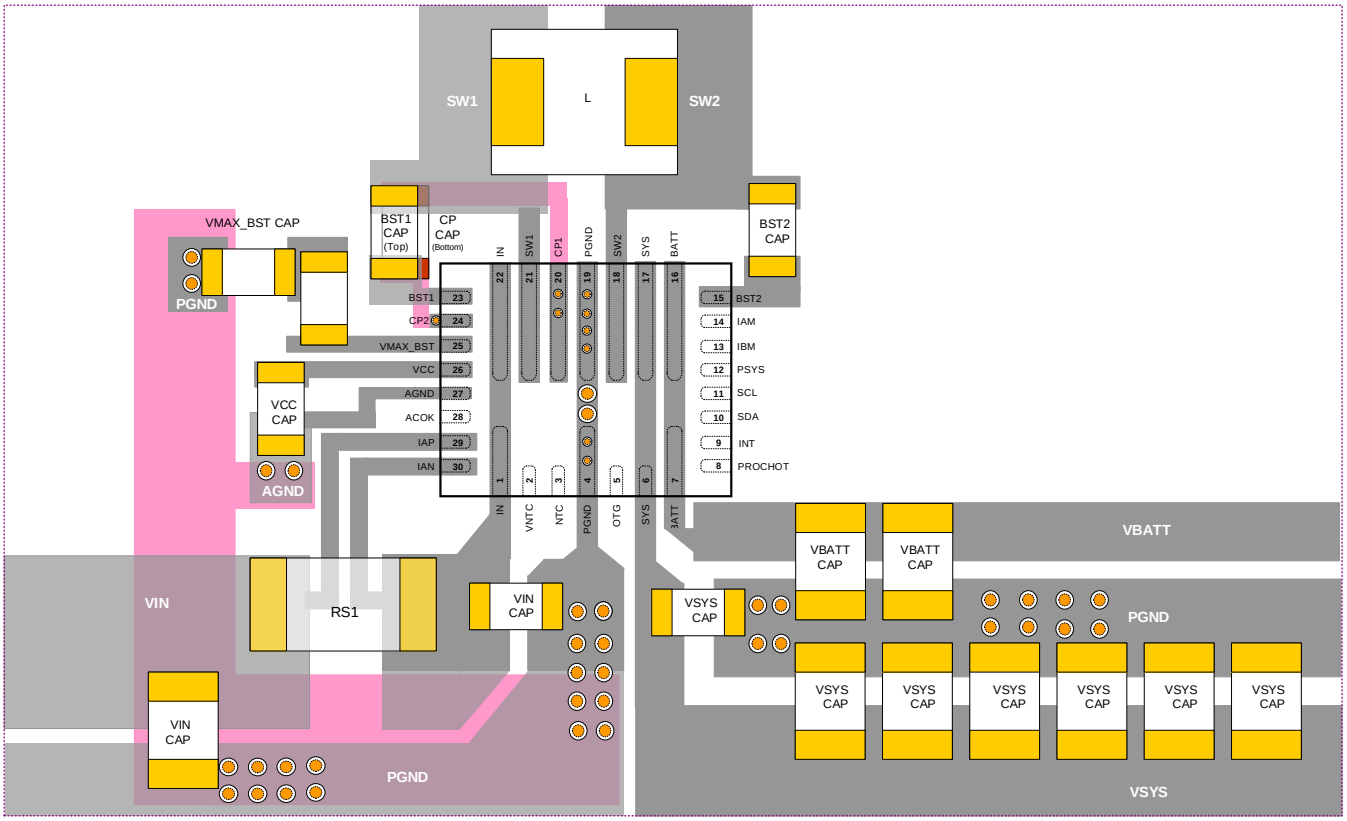


Figure 22: Recommended PCB Layout

TYPICAL APPLICATION CIRCUIT

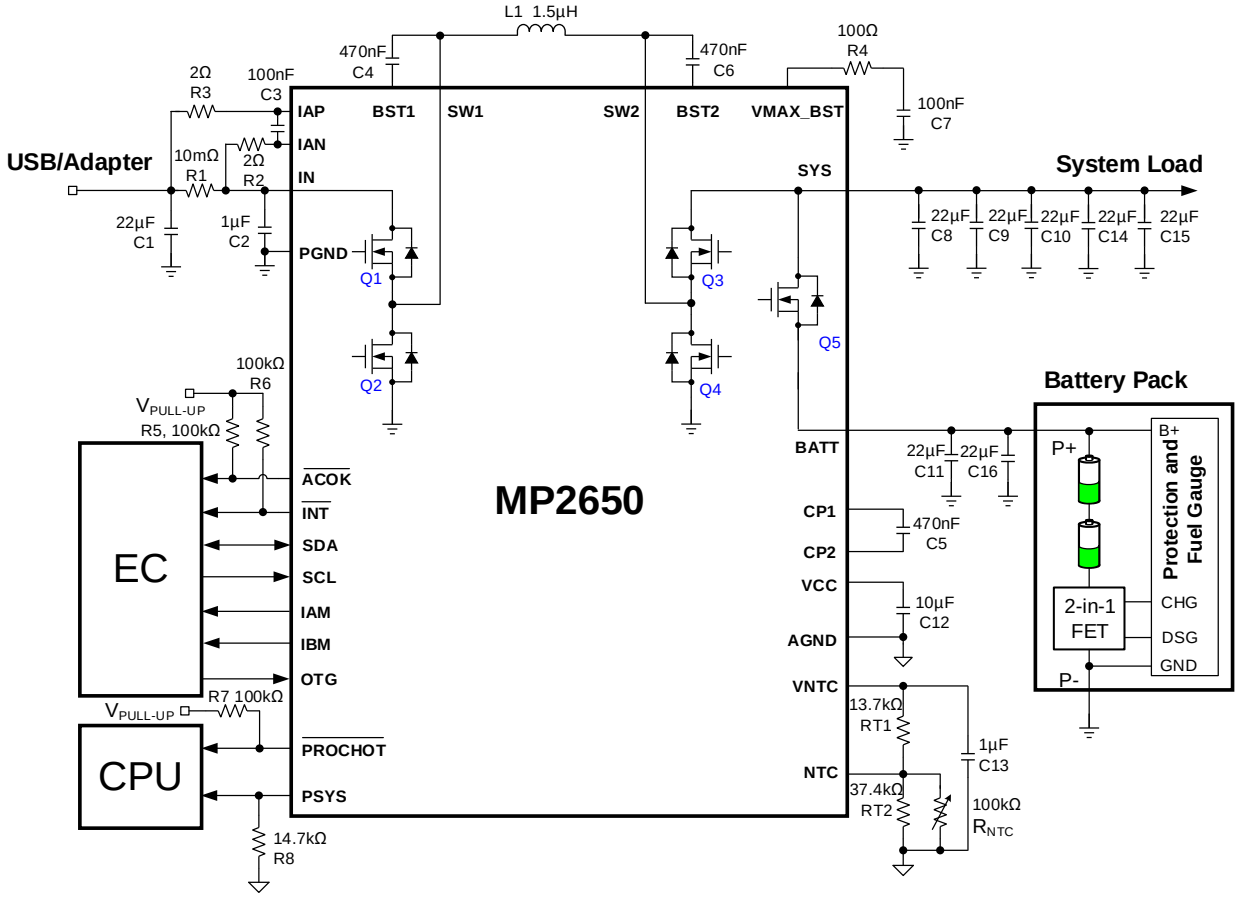


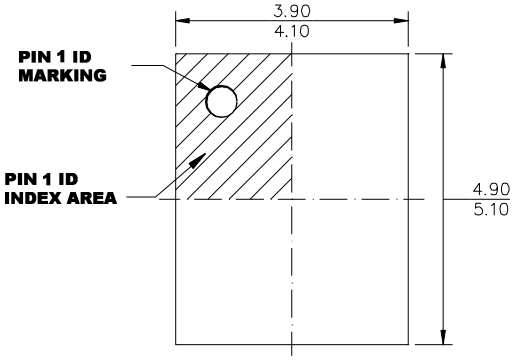
Figure 23: Typical Application Circuit

Table 4: Key BOM for Figure 23

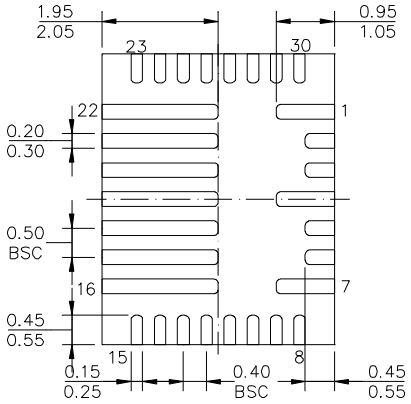
Qty	Ref	Value	Description	Package	Manufacturer
8	C1, C8, C9, C10, C11, C14, C15, C16	22µF	Ceramic capacitor, 25V, X5R or X7R	0805	Any
1	C2	1µF	Ceramic capacitor, 25V, X5R or X7R	0603	Any
1	C3	100nF	Ceramic capacitor, 25V, X5R or X7R	0603	Any
3	C4, C5, C6	470nF	Ceramic capacitor, 25V, X5R or X7R	0603	Any
1	C7	100nF	Ceramic capacitor, 50V, X5R or X7R	0603	Any
1	C12	10µF	Ceramic capacitor, 25V, X5R or X7R	0603	Any
1	R1	10mΩ	Film resistor, 1%	1206	Any
2	R2, R3	2Ω	Film resistor, 1%	0603	Any
1	R4	100Ω	Film resistor, 1%	0603	Any
1	RT1	13.7kΩ	Film resistor, 1%	0603	Any
1	RT2	37.4kΩ	Film resistor, 1%	0603	Any
1	L1	1.5µH	Inductor, 1.5µH, low DCR, I_{SAT} > 7A	SMD	Any

PACKAGE INFORMATION

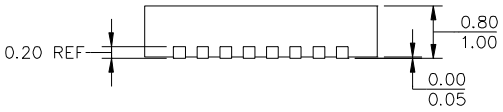
QFN-30 (4mmx5mm)



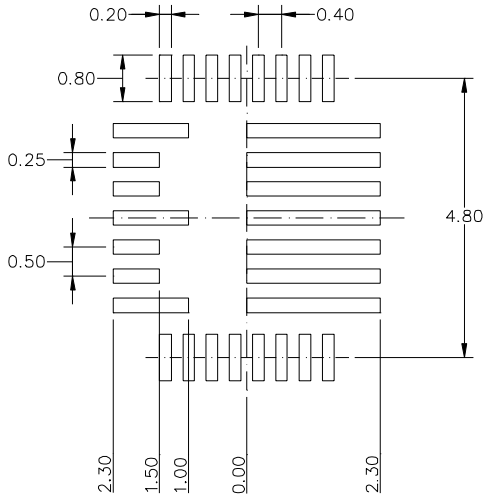
TOP VIEW



BOTTOM VIEW



SIDE VIEW

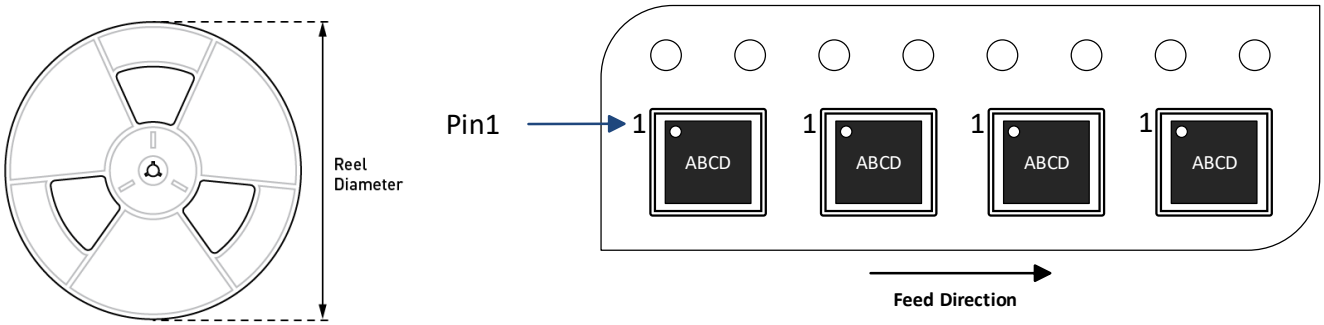


RECOMMENDED LAND PATTERN

NOTE:

1) LAND PATTERN OF PIN1,4 AND PIN7 HAVE THE SAME LENGTH AND WIDTH.
2) LAND PATTERN OF PIN16~22 HAVE THE SAME LENGTH AND WIDTH.
3) ALL DIMENSIONS ARE IN MILLIMETERS.
4) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO-220.
6) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP2650GV-xxxx-Z	QFN-30 (4mmx5mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	4/22/2022	Initial Release	-