MP8869W

3V - 18V, 12A, High-Efficiency, Wide-Input, Synchronous Step-Down Converter with Integrated Telemetry via I²C Interface

The Future of Analog IC Technology®

NOT RECOMMENDED FOR NEW DESIGNS, REFER TO MMP8869S

DESCRIPTION

The MP8869W is a high-frequency, synchronous, rectified, step-down, switch-mode converter with an I²C control interface. It offers a fully integrated solution that achieves 12A of continuous and 15A of peak output current with excellent load and line regulation over a wide input supply range.

In the I²C control loop, the output voltage level can be controlled on-the-fly through an I²C serial interface. The voltage range can be adjusted from 0.6V to 1.55V in 7.5mV steps. Voltage slew rate, frequency, current limit, hiccup/latch-off protection, enable, and power saving mode are also selectable through the I²C interface.

Constant-on-time (COT) control operation provides fast transient response. An open-drain power good (PG) pin indicates that the output voltage is in the nominal range. Full protection features include over-voltage protection (OVP), over-current protection (OCP), and thermal shutdown.

The MP8869W is available in a QFN-14 (3mmx4mm) package.

FEATURES

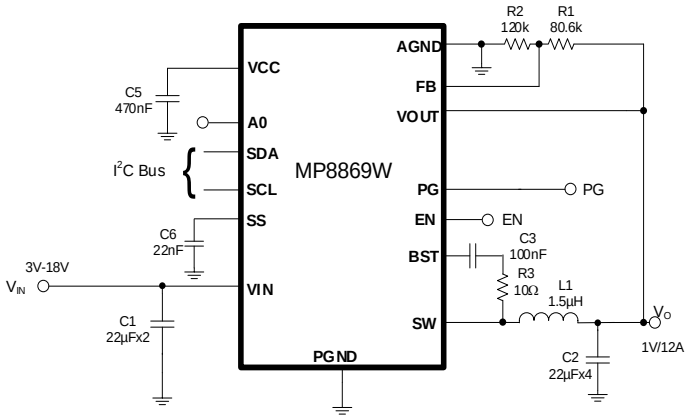
- Wide 3V to 18V Operating Input Range
- 12A Continuous/15A Peak Output Current
- 1% Internal Reference Accuracy
- I²C Programmable Output Range from 0.6V to 1.55V in 7.5mV Steps with Slew Rate Control
- 5% Accuracy Output Voltage and Output Current Monitoring via I²C
- Selectable PFM/PWM Mode, Adjustable Frequency and Current Limit through I²C
- 4 Different Selectable I²C Addresses
- External Soft Start
- Open-Drain Power Good Indication
- Output Over-Voltage Protection (OVP)
- Hiccup/Latch-Off OCP
- Available in a QFN-14 (3mmx4mm) Package

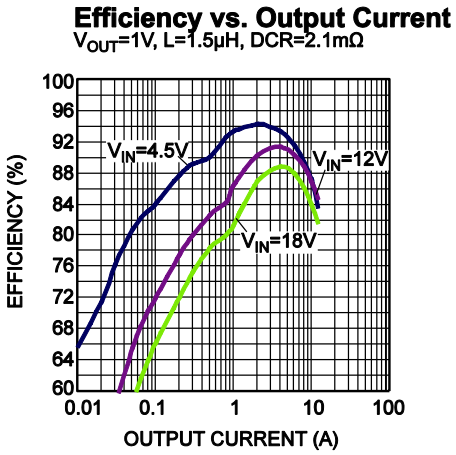
APPLICATIONS

- Solid-State Drive (SSD)
- Flat-Panel Television and Monitors
- Digital Set-Top Boxes
- Distributed Power Systems
- Networking/Server

All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance. "MPS" and "The Future of Analog IC Technology" are registered trademarks of Monolithic Power Systems, Inc.

TYPICAL APPLICATION





MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2023 MPS. All Rights Reserved.

NOT RECOMMENDED FOR NEW DESIGNS, REFER TO MMP8869S

ORDERING INFORMATION

Part Number	Package	Top Marking
MP8869WGL*	QFN-14 (3mmx4mm)	*See Below*
EVKT-8869W	Evaluation Kit	

* For Tape & Reel, add suffix –Z (e.g. MP8869WGL–Z)

TOP MARKING

MPYW
8869
WLLL

MP: MPS prefix
Y: Year code
W: Week code
8869W: First five digits of the part number
LLL: Lot number

EVALUATION KIT EVKT-8869W

EVKT-8869W Kit contents: (Items can be ordered separately).

#	Part Number	Item	Quantity
1	EV8869W-L-00A	MP8869WGL evaluation board	1
2	EVKT-USBI2C-02	Includes one USB to I2C dongle, one USB cable, and one ribbon cable	1
3	Tdrive-8869W	USB flash drive that stores the GUI installation file supplemental documents	1

Order direct from MonolithicPower.com or our distributors

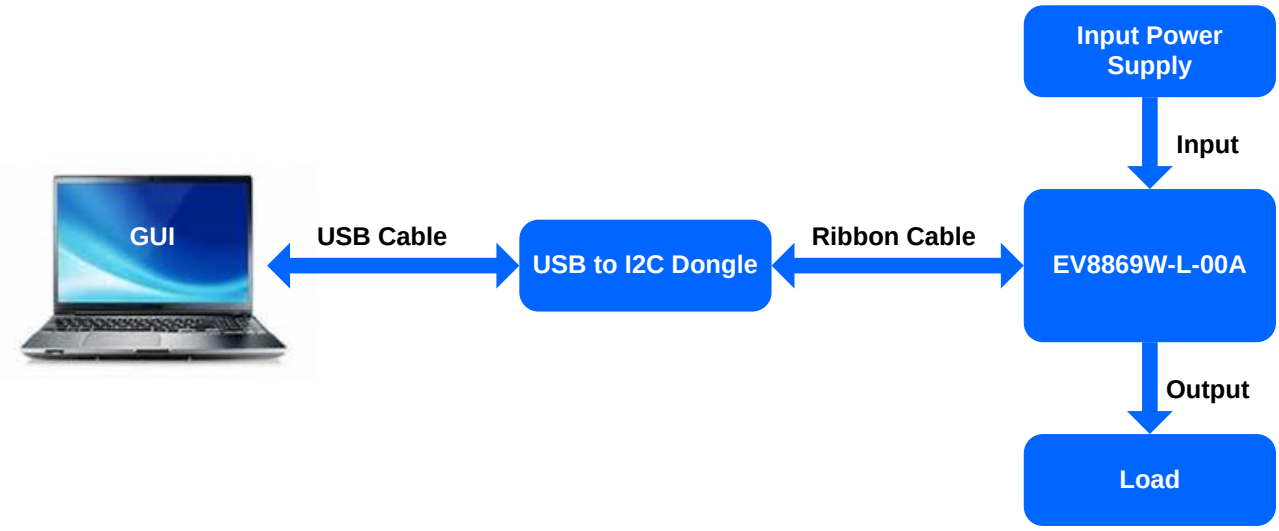
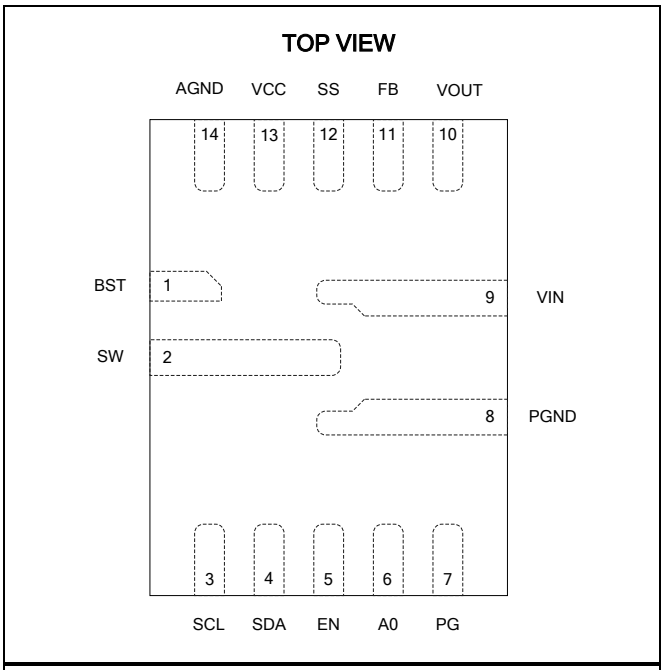


Figure 1: EVKT-8869W Evaluation Kit Set-Up

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2023 MPS. All Rights Reserved.

NOT RECOMMENDED FOR NEW DESIGNS, REFER TO MMP8869S

PACKAGE REFERENCE



QFN-14 (3mmx4mm)

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} ..... -0.3V to 19V
V_{SW} ..... -0.6V (-7V for <10ns) to V_{IN} + 0.7V (25V for <25ns)
V_{BST} ..... V_{SW} + 4V
V_{EN} 18V
V_{OUT} 7V
All other pins ..... -0.3V to 4V
Continuous power dissipation (T_A = +25°C) **(2)**
QFN-14 (3mmx4mm) 2.5W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to 150°C

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) ..... 3V to 18V
Output voltage (V_{OUT}) ... 0.6V to 5.5V for FB loop and 0.6V to 1.55V for I^2C loop
Operating junction temp. (T_J) ... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-14 (3mmx4mm) ..... 48 ..... 11 ... °C/W

NOTES:

1. Exceeding these ratings may damage the device.
2. The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3. The device is not guaranteed to function outside of its operating conditions.
4. Measured on JESD51-7, 4-layer PCB.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2023 MPS. All Rights Reserved.

NOT RECOMMENDED FOR NEW DESIGNS, REFER TO MMP8869S

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +125°C(5), typical value is tested at T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply current (shutdown)	I_{IN}	V_{EN} = 0V		2.1	4	μA
Supply current (quiescent)	I_q	No switching, FB = 105% Vref, PFM mode		420	600	μA
HS switch on resistance	$HS_{RDS(ON)}$	$V_{BST - SW}$ =3.3V		15		mΩ
LS switch on resistance	$LS_{RDS(ON)}$	V_{CC} = 3.3V		4.5		mΩ
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} =12V, T_J = +25°C			1	μA
Low-side valley current limit	I_{LIMIT_L}	Adjustable by I²C		14		A
Low-side negative current limit	I_{LIMIT_LN}	In forced PWM mode or OVP state		-3		A
Low-side ZCD threshold	I_{ZCD}	T_J = +25°C		200		mA
Switching frequency	f_{SW1}	V_{IN} = 12V, V_{OUT} = 1V	400	500	600	kHz
	f_{SW2}	V_{IN} = 12V, V_{OUT} = 5V	400	500	600	kHz
Minimum off time(6)	T_{OFF_MIN}			185		ns
Minimum on time(6)	T_{ON_MIN}	V_{OUT} = 0.6V		50		ns
Reference voltage	V_{ref}	T_J = 25°C	594	600	606	mV
		-40°C < T_J < 125°C (5)	591	600	609	
FB current	I_{FB}	V_{OUT} = 620mV		10	50	nA
A0 voltage threshold 1	V_{ADD_1}	Set I²C address 60H			0.24	VCC
A0 voltage threshold 2	V_{ADD_2}	Set I²C address 62H	0.28		0.49	VCC
A0 voltage threshold 3	V_{ADD_3}	Set I²C address 64H	0.53		0.72	VCC
A0 voltage threshold 4	V_{ADD_4}	Set I²C address 66H	0.77			VCC
A0 to GND pull-down resistor	R_{A0_PD}			2		MΩ
EN rising threshold	V_{EN_RISING}		1.1	1.2	1.3	V
EN threshold hysteresis	V_{EN_HYS}			110		mV
EN to GND pull-down resistor	R_{EN}			1.5		MΩ
VIN under-voltage lockout threshold rising	$INUV_{Vth}$		2.7	2.8	2.92	V
VIN under-voltage lockout threshold hysteresis	$INUV_{HYS}$			300		mV
Power good UV threshold rising	PGVth-Hi	Good	0.86	0.9	0.94	VOUT
Power good UV threshold falling	PGVth-Lo	Fault	0.81	0.85	0.89	VOUT
Power good OV threshold rising	PGVth-Hi	Fault	1.11	1.15	1.19	VOUT

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2023 MPS. All Rights Reserved.

NOT RECOMMENDED FOR NEW DESIGNS, REFER TO MMP8869S

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +125°C(5), typical value is tested at T_J=+25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power good OV threshold falling	PGVth-Lo	Good	1.01	1.05	1.09	VOUT
Power good deglitch time	PGTd	I^2C programmable		30		µs
Power good sink current capability	V_{PG}	Sink 4mA			0.4	V
OVP rising threshold	V_{OVP_Rise}	VOUT and FB	121%	125%	129%	V_{REF}
OVP falling threshold	$V_{OVP_Falling}$	VOUT and FB	106%	110%	114%	V_{REF}
OVP delay	T_{OVP}			3.7		µs
Output pin absolute OV	V_{OVP2}		6	6.5	7	V
UVP threshold	$V_{FB_UV_th}$	Hiccup entry	55%	60%	65%	V_{REF}
UVP delay (6)	T_{UVP}			10		µs
Soft-start current	I_{SS}		5	7	9	µA
VCC voltage	V_{CC}			3.5		V
VCC load regulation	V_{CC_reg}	I_{CC} = 20mA			3	%
Thermal shutdown (6)	T_{TSD}			160		°C
Thermal hysteresis (6)	T_{TSD_HYS}			20		°C

NOTES:
5) Not tested in production and guaranteed by over-temperature correlation.
6) Guaranteed by design and characterization test.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2023 MPS. All Rights Reserved.

NOT RECOMMENDED FOR NEW DESIGNS, REFER TO MMP8869S

I/O LEVEL CHARACTERISTICS

Parameter	Symbol	Condition	HS-Mode		LS-Mode		Units
			Min	Max	Min	Max	
Low-level input voltage	V_{IL}		-0.5	$0.3V_{CC}$	-0.5	$0.3V_{CC}$	V
High-level input voltage	V_{IH}		$0.7V_{CC}$	V_{CC} + 0.5	$0.7V_{CC}$	V_{CC} + 0.5	V
Hysteresis of Schmitt trigger inputs	V_{HYS}	V_{CC} > 2V	$0.05V_{CC}$	-	$0.05V_{CC}$	-	V
		V_{CC} < 2V	$0.1V_{CC}$	-	$0.1V_{CC}$	-	
Low-level output voltage (open drain) at 3mA sink current	V_{OL}	V_{CC} > 2V	0	0.4	0	0.4	V
		V_{CC} < 2V	0	$0.2V_{CC}$	0	$0.2V_{CC}$	
Low-level output current	I_{OL}		-	3	-	3	mA
Transfer gate on resistance for currents between SDA and SCAH, or SCL and SCLH	R_{onL}	VOL level, IOL = 3mA	-	50	-	50	Ω
Transfer gate on resistance between SDA and SCAH, or SCL and SCLH	R_{onH}	Both signals (SDA and SDAH, or SCL and SCLH) at V_{CC} level	50	-	50	-	kΩ
Pull-up current of the SCLH current source	I_{cs}	SCLH output levels between 0.3Vcc and $0.7V_{CC}$	2	6	2	6	mA
Rise time of the SCLH or SCL signal	T_{rCL}	Output rise time (current source enabled) with an external pull-up current source of 3mA					
		Capacitive load from 10pF to 100pF	10	40			ns
		Capacitive load of 400pF	20	80			ns
Fall time of the SCLH or SCL signal	T_{fCL}	Output fall time (current source enabled) with an external pull-up current source of 3mA					
		Capacitive load from 10pF to 100pF	10	40			ns
		Capacitive load of 400pF	20	80	20	250	ns
Rise time of SDAH signal	T_{rDA}	Capacitive load from 10pF to 100pF	10	80	-	-	ns
		Capacitive load of 400pF	20	160	20	250	ns
Fall time of SDAH signal	T_{fDA}	Capacitive load from 10pF to 100pF	10	80	-	-	ns
		Capacitive load of 400pF	20	160	20	250	ns

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2023 MPS. All Rights Reserved.

NOT RECOMMENDED FOR NEW DESIGNS, REFER TO MMP8869S

I/O LEVEL CHARACTERISTICS *(continued)*

Parameter	Symbol	Condition	HS-Mode		LS-Mode		Units
			Min	Max	Min	Max	
Pulse width of spikes that must be suppressed by the input filter	t_{SP}		0	10	0	50	ns
Input current each I/O pin	I_i	Input voltage between $0.1V_{CC}$ and $0.9V_{CC}$	-	10	-10	+10	µA
Capacitance for each I/O pin	C_i		-	10	-	10	pF

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2023 MPS. All Rights Reserved.

NOT RECOMMENDED FOR NEW DESIGNS, REFER TO MMP8869S

I²C PORT SIGNAL CHARACTERISTICS

Parameter	Symbol	Condition	Cb = 100pF		Cb = 400pF		Units
			Min	Max	Min	Max	
SCLH and SCL clock frequency	f_{SCHL}		0	3.4	0	0.4	MHz
Set-up time for a repeated start condition	$T_{SU;STA}$		160	-	600	-	ns
Hold time (repeated) start condition	$T_{HD;STA}$		160	-	600	-	ns
Low period of the SCL clock	T_{LOW}		160	-	1300	-	ns
High period of the SCL clock	T_{HIGH}		60	-	600	-	ns
Data set-up time	$T_{SU:DAT}$		10	-	100	-	ns
Data hold time	$T_{HD;DAT}$		0	70	0	-	ns
Rise time of SCLH signal	T_{rCL}		10	40	20*0.1Cb	300	ns
Rise time of SCLH signal after a repeated START condition and after an acknowledge bit	T_{fCL1}		10	80	20*0.1Cb	300	ns
Fall time of SCLH signal	T_{fCL}		10	40	20*0.1Cb	300	ns
Rise time of SDAH signal	T_{fDA}		10	80	20*0.1Cb	300	ns
Fall time of SDAH signal	T_{fDA}		10	80	20*0.1Cb	300	ns
Set-up time for stop condition	$T_{SU;STO}$		160	-	600	-	ns
Bus free time between a stop and start condition	T_{BUF}		160	-	1300	-	ns
Data valid time	$T_{VD;DAT}$		-	16	-	90	ns
Data valid acknowledge time	$T_{VD;ACK}$		-	160	-	900	ns
Capacitive load for each bus line	C_b	SDAH and SCLH line	-	100	-	400	pF
		SDAH + SDA line and SCLH + SCL line	-	400	-	400	pF
Noise margin at the low level	C_i	For each connected device	-	$0.1V_{CC}$	$0.1V_{CC}$	-	V
Noise margin at the high level	V_{nH}	For each connected device	-	$0.2V_{CC}$	$0.2V_{CC}$	-	V

NOTE:
V_{CC} is the I²C bus voltage, 1.8V to 3.6V range, and used for 1.8V, 2.5V, and 3.3V bus voltage.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2023 MPS. All Rights Reserved.

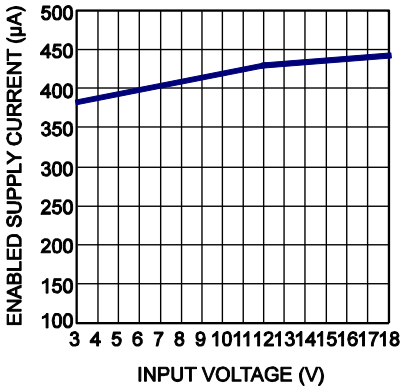
NOT RECOMMENDED FOR NEW DESIGNS, REFER TO MMP8869S

TYPICAL PERFORMANCE CHARACTERISTICS

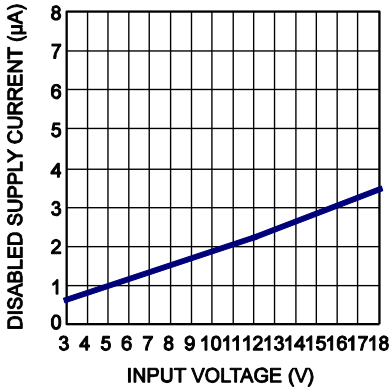
Performance waveforms are tested on the evaluation board.

V_{IN} = 12V, V_{OUT} = 1V, L = 1.5μH, F_S = 500kHz, auto PFM/PWM mode, T_A = 25°C, unless otherwise noted.

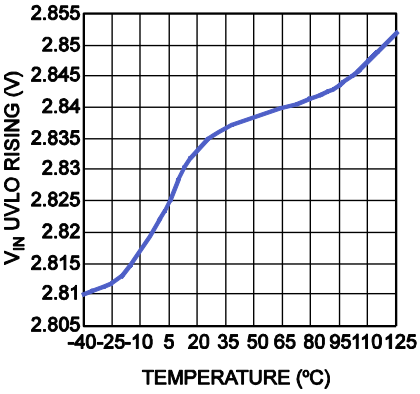
Enabled Supply Current vs. Input Voltage



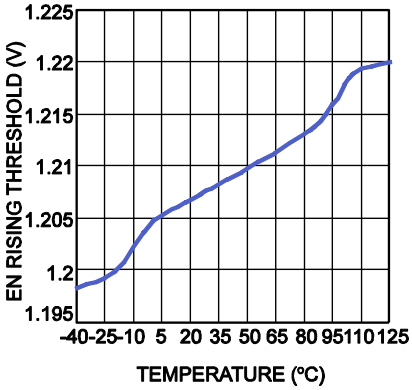
Disabled Supply Current vs. Input Voltage



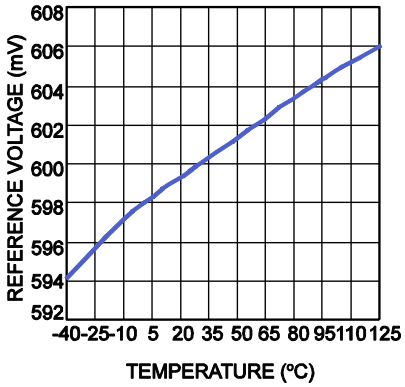
V_{IN} UVLO Rising vs. Temperature



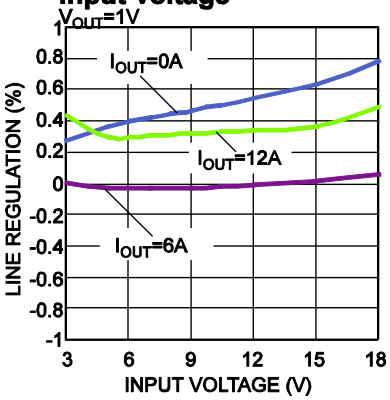
EN Rising Threshold vs. Temperature



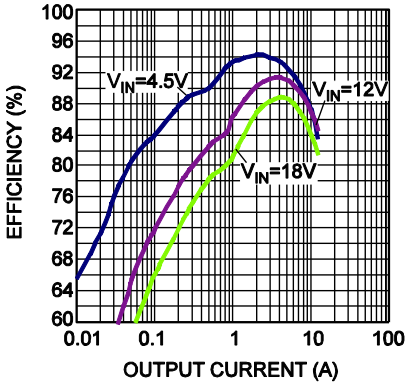
Reference Voltage vs. Temperature



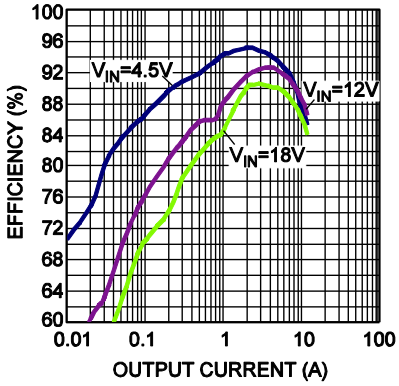
Line Regulation vs. Input Voltage



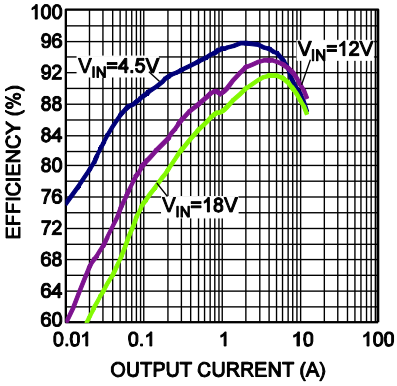
Efficiency vs. Output Current
V_{OUT}=1V, L=1.5μH, DCR=2.1mΩ



Efficiency vs. Output Current
V_{OUT}=1.2V, L=1.5μH, DCR=2.1mΩ



Efficiency vs. Output Current
V_{OUT}=1.5V, L=1.5μH, DCR=2.1mΩ



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2023 MPS. All Rights Reserved.

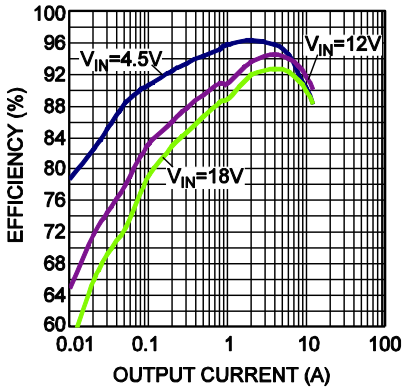
NOT RECOMMENDED FOR NEW DESIGNS, REFER TO MMP8869S

TYPICAL PERFORMANCE CHARACTERISTICS *(CONTINUED)*

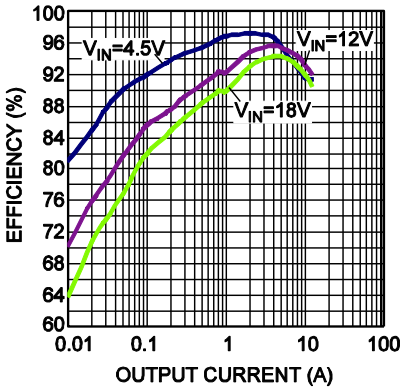
Performance waveforms are tested on the evaluation board.

V_{IN} = 12V, V_{OUT} = 1V, L = 1.5μH, F_S = 500kHz, auto PFM/PWM mode, T_A = 25°C, unless otherwise noted.

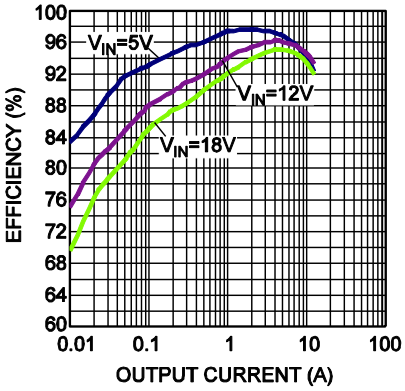
Efficiency vs. Output Current
V_{OUT}=1.8V, L=1.5μH, DCR=2.1mΩ



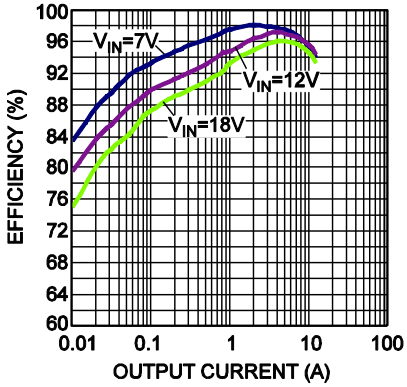
Efficiency vs. Output Current
V_{OUT}=2.5V, L=2.2μH, DCR=3mΩ



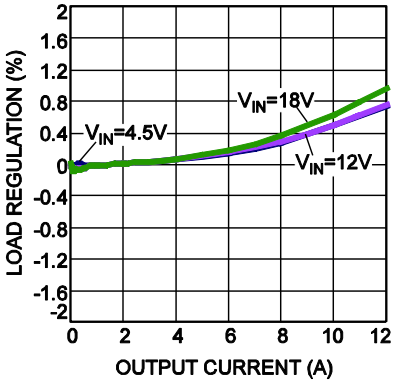
Efficiency vs. Output Current
V_{OUT}=3.3V, L=2.2μH, DCR=3mΩ



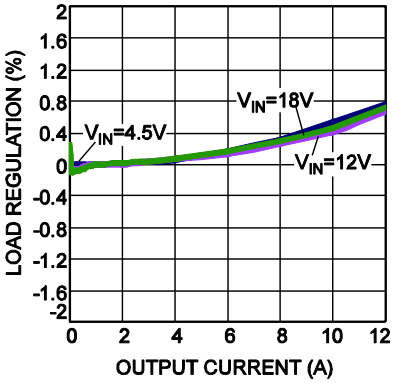
Efficiency vs. Output Current
V_{OUT}=5V, L=3.3μH, DCR=4.4mΩ



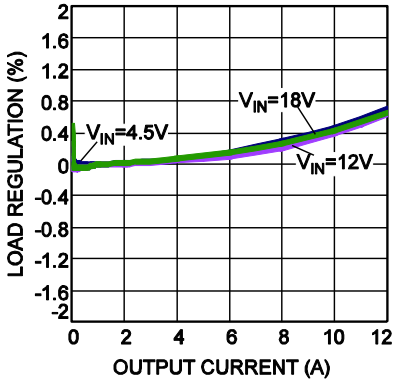
Load Regulation vs. Output Current
V_{OUT}=1V



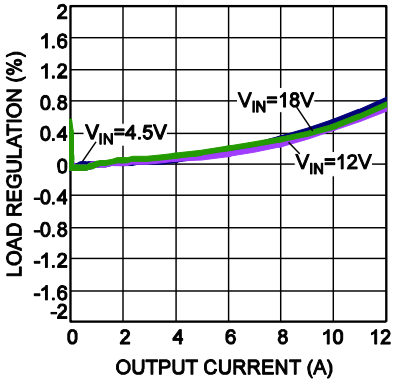
Load Regulation vs. Output Current
V_{OUT}=1.2V



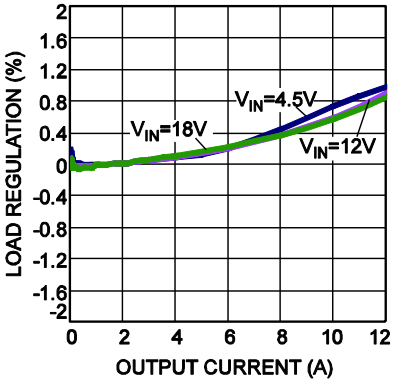
Load Regulation vs. Output Current
V_{OUT}=1.5V



Load Regulation vs. Output Current
V_{OUT}=1.8V



Load Regulation vs. Output Current
V_{OUT}=2.5V



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2023 MPS. All Rights Reserved.

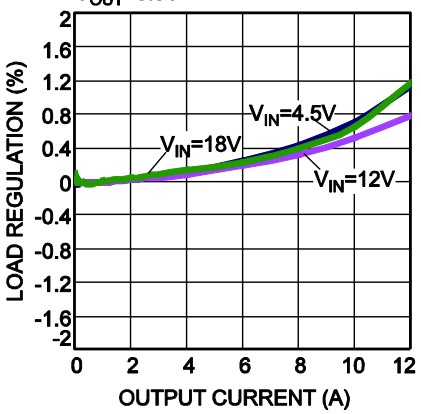
NOT RECOMMENDED FOR NEW DESIGNS, REFER TO MMP8869S

TYPICAL PERFORMANCE CHARACTERISTICS *(CONTINUED)*

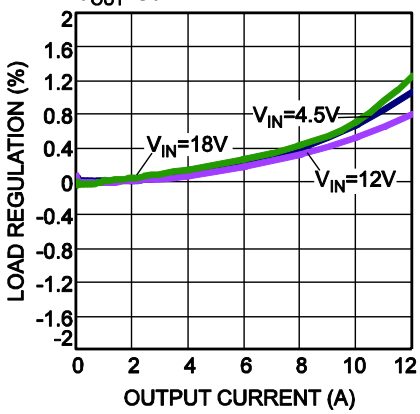
Performance waveforms are tested on the evaluation board.

V_{IN} = 12V, V_{OUT} = 1V, L = 1.5µH, F_S = 500kHz, auto PFM/PWM mode, T_A = 25°C, unless otherwise noted.

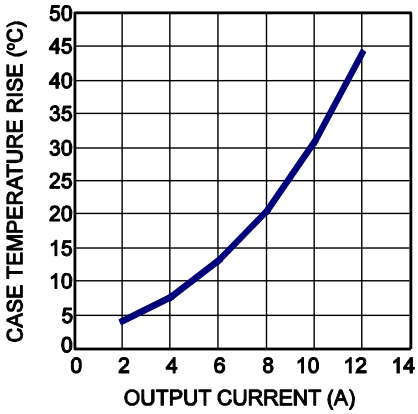
Load Regulation vs. Output Current
V_{OUT}=3.3V



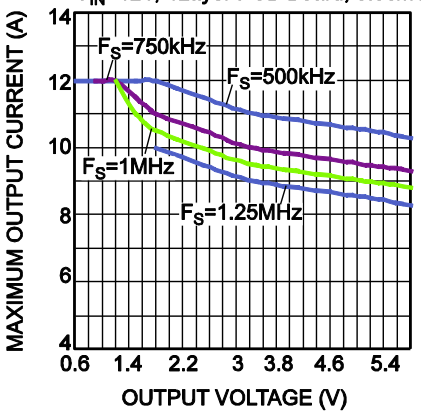
Load Regulation vs. Output Current
V_{OUT}=5V



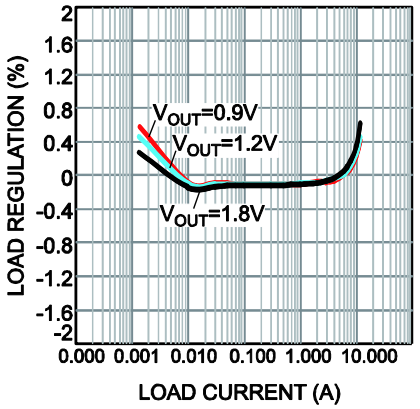
Case Temperature Rise vs. Output Current



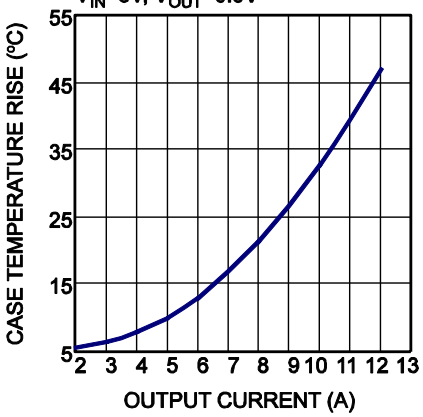
Output Current Derating vs. Frequency and Output Voltage
V_{IN}=12V, 4Layer PCB Board, 8.5cm x 8.5cm



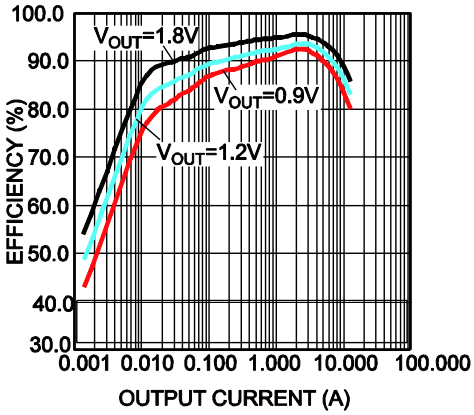
Load Regulation (%)
V_{IN}=3V, V_{OUT}=0.9V



Case Temperature Rise vs. Output Current
V_{IN}=3V, V_{OUT}=0.9V



Efficiency Curve
V_{IN}=3V, V_{OUT}=0.9V



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2023 MPS. All Rights Reserved.

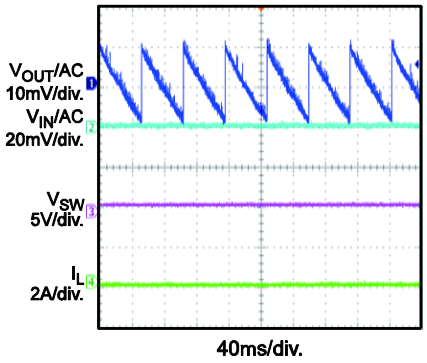
NOT RECOMMENDED FOR NEW DESIGNS, REFER TO MMP8869S

TYPICAL PERFORMANCE CHARACTERISTICS *(CONTINUED)*

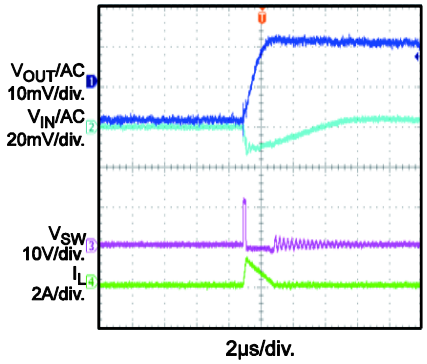
Performance waveforms are tested on the evaluation board.

V_{IN} = 12V, V_{OUT} = 1V, L = 1.5µH, F_S = 500kHz, auto PFM/PWM mode, T_A = 25°C, unless otherwise noted.

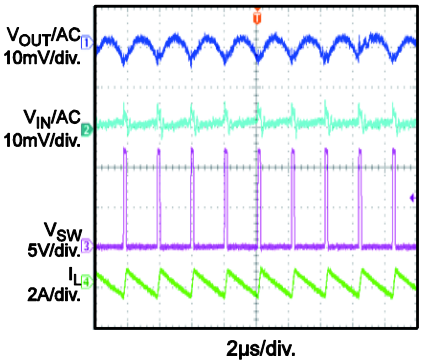
Input/Output Ripple
I_{OUT} = 0A



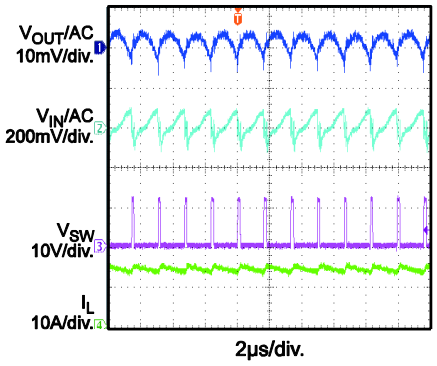
Input/Output Ripple
I_{OUT} = 0A



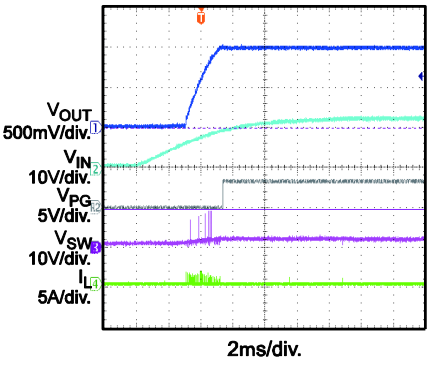
Input/Output Ripple
I_{OUT} = 0A, Forced PWM Mode



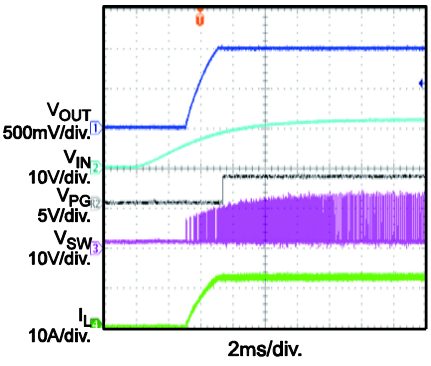
Input/Output Ripple
I_{OUT} = 12A



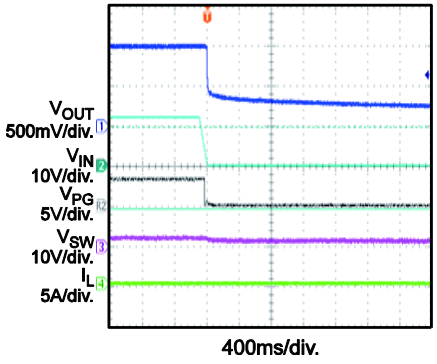
Start-Up through Input Voltage
I_{OUT} = 0A



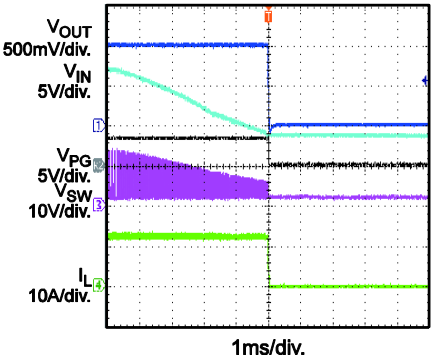
Start-Up through Input Voltage
I_{OUT} = 12A



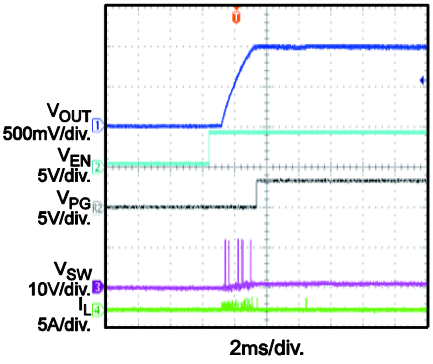
Shutdown through Input Voltage
I_{OUT} = 0A



Shutdown through Input Voltage
I_{OUT} = 12A



Start-Up through EN
I_{OUT} = 0A



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2023 MPS. All Rights Reserved.

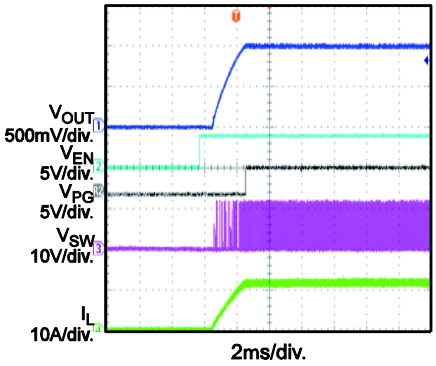
NOT RECOMMENDED FOR NEW DESIGNS, REFER TO MMP8869S

TYPICAL PERFORMANCE CHARACTERISTICS *(CONTINUED)*

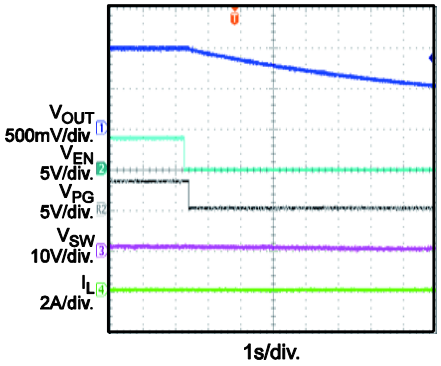
Performance waveforms are tested on the evaluation board.

V_{IN} = 12V, V_{OUT} = 1V, L = 1.5μH, F_S = 500kHz, auto PFM/PWM mode, T_A = 25°C, unless otherwise noted.

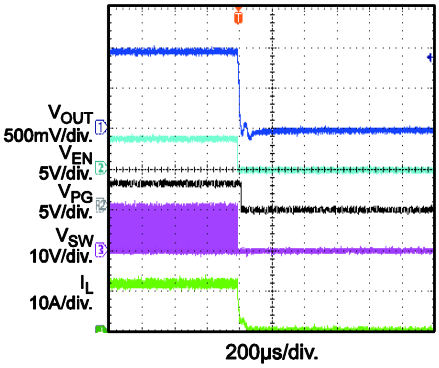
Start-Up through EN
I_{OUT} = 12A



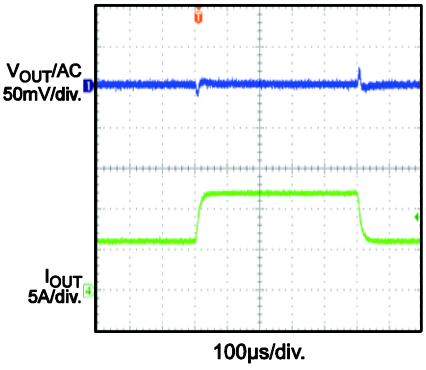
Shutdown through EN
I_{OUT} = 0A



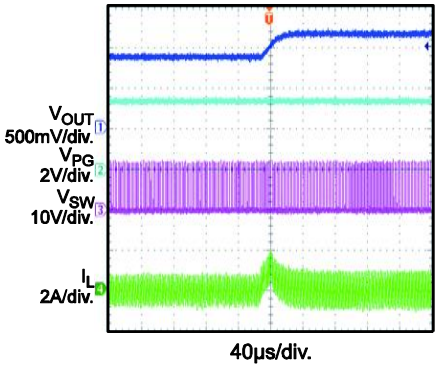
Shutdown through EN
I_{OUT} = 12A



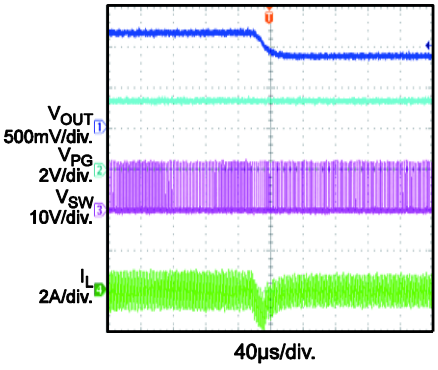
Load Transient
I_{OUT} = 6A-12A



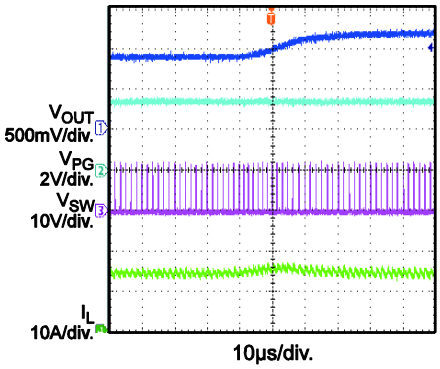
I^2C Control Slew Rate
I_{OUT}=0A, Slew Rate=20mV/μs,
PWM Mode, Output from 0.9V to 1.2V



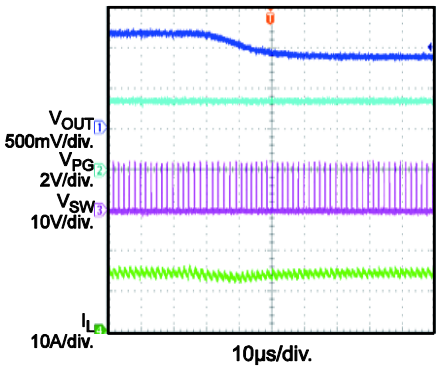
I^2C Control Slew Rate
I_{OUT}=0A, Slew Rate=20mV/μs,
PWM Mode, Output from 1.2V to 0.9V



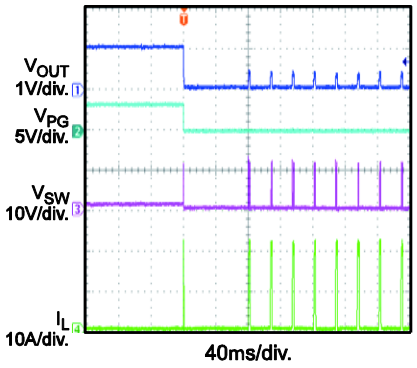
I^2C Control Slew Rate
I_{OUT}=12A, Slew Rate=20mV/μs,
PWM Mode, Output from 0.9V to 1.2V



I^2C Control Slew Rate
I_{OUT}=12A, Slew Rate=20mV/μs,
PWM Mode, Output from 1.2V to 0.9V



Short-Circuit Protection Entry
I_{OUT} = 0A



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2023 MPS. All Rights Reserved.

NOT RECOMMENDED FOR NEW DESIGNS, REFER TO MMP8869S

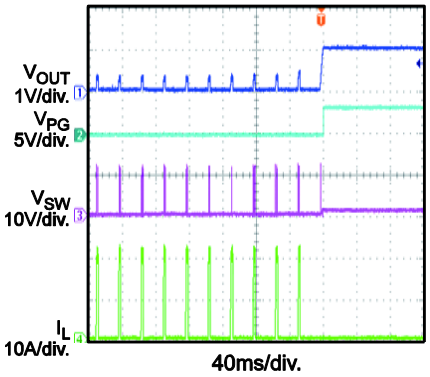
TYPICAL PERFORMANCE CHARACTERISTICS *(CONTINUED)*

Performance waveforms are tested on the evaluation board.

V_{IN} = 12V, V_{OUT} = 1V, L = 1.5µH, F_S = 500kHz, auto PFM/PWM mode, T_A = 25°C, unless otherwise noted.

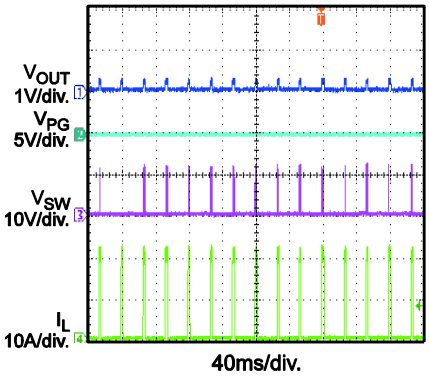
Short-Circuit Protection Recovery

I_{OUT} = 0A



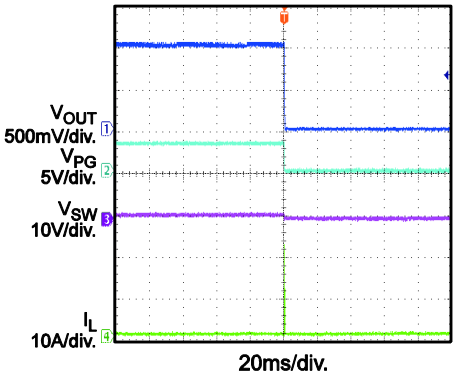
Short-Circuit Protection Steady State

Short Output to GND



Short-Circuit Protection Entry, Latch Off Mode

I_{OUT}=0A



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2023 MPS. All Rights Reserved.

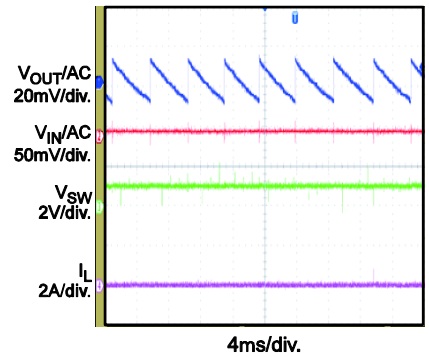
NOT RECOMMENDED FOR NEW DESIGNS, REFER TO MMP8869S

TYPICAL PERFORMANCE CHARACTERISTICS *(CONTINUED)*

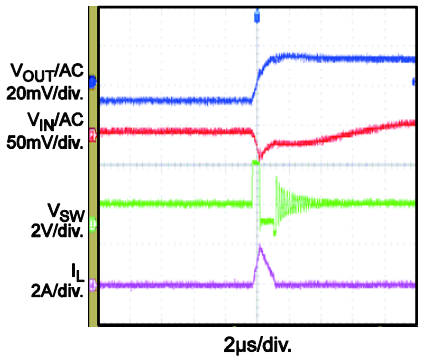
Performance waveforms are tested on the evaluation board.

V_{IN} = 3V, V_{OUT} = 0.9V, L = 0.47µH, F_S = 500kHz, auto PFM/PWM mode, T_A = 25°C, unless otherwise noted.

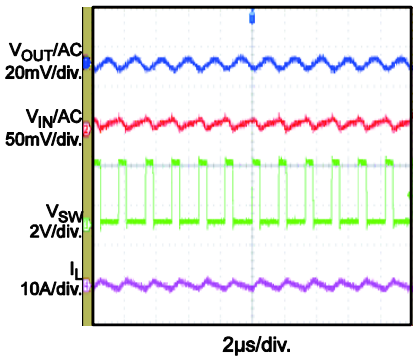
Input/Output Ripple
I_{OUT} = 0A



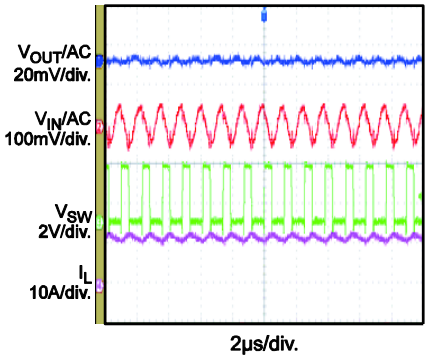
Input/Output Ripple
I_{OUT} = 0A



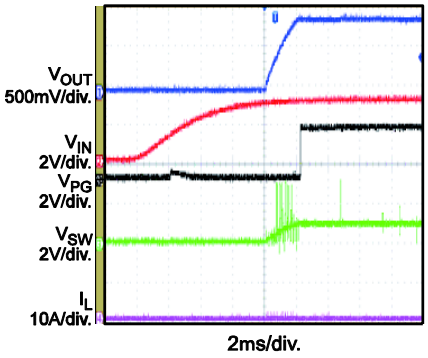
Input/Output Ripple
I_{OUT} = 0A, Forced PWM Mode



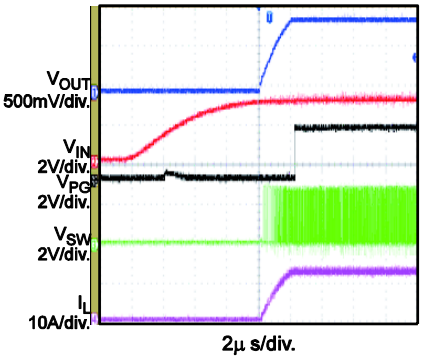
Input/Output Ripple
I_{OUT} = 12A



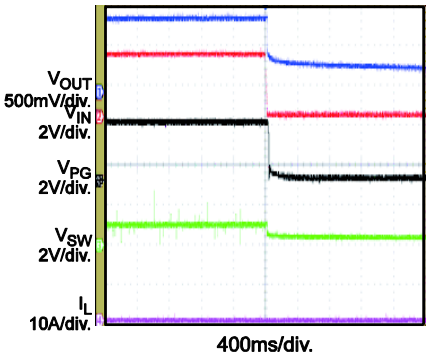
Start-Up through Input Voltage
I_{OUT} = 0A



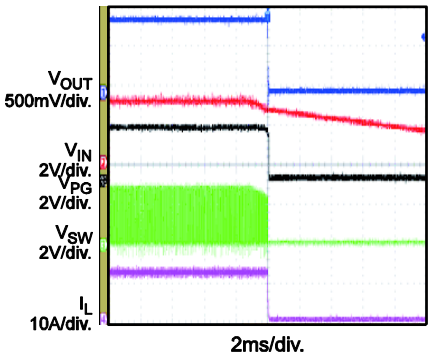
Start-Up through Input Voltage
I_{OUT} = 12A



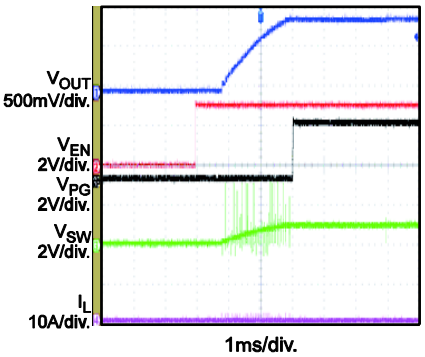
Shutdown through Input Voltage
I_{OUT} = 0A



Shutdown through Input Voltage
I_{OUT} = 12A



Start-Up through EN
I_{OUT} = 0A



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2023 MPS. All Rights Reserved.

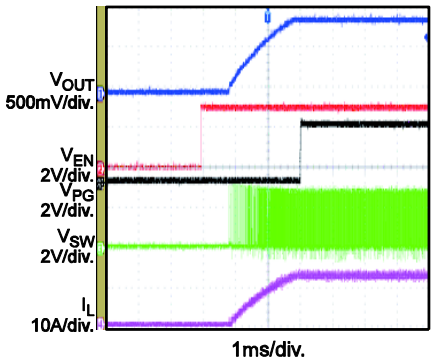
NOT RECOMMENDED FOR NEW DESIGNS, REFER TO MMP8869S

TYPICAL PERFORMANCE CHARACTERISTICS *(CONTINUED)*

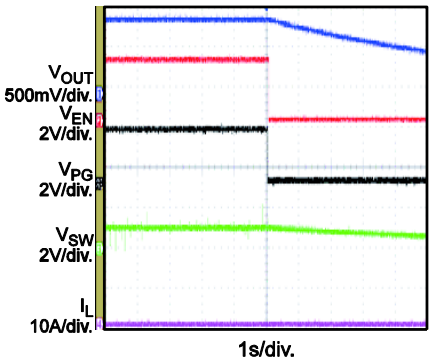
Performance waveforms are tested on the evaluation board.

V_{IN} = 3V, V_{OUT} = 0.9V, L = 0.47µH, F_S = 500kHz, auto PFM/PWM mode, T_A = 25°C, unless otherwise noted.

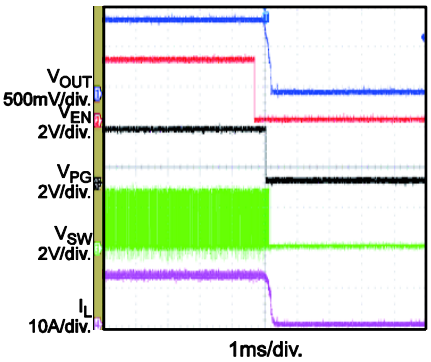
Start-Up through EN
I_{OUT} = 12A



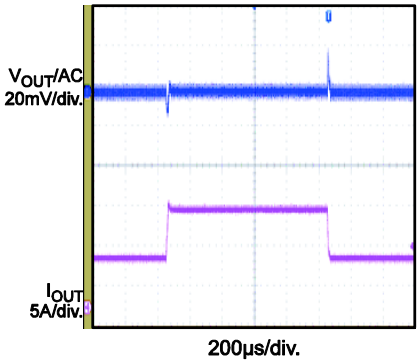
Shutdown through EN
I_{OUT} = 0A



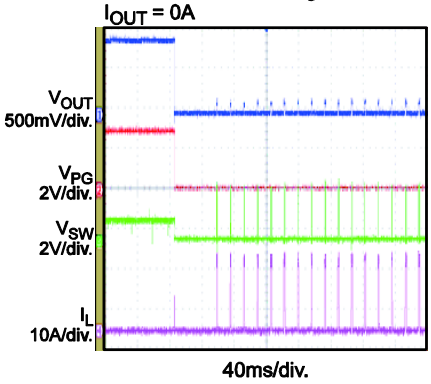
Shutdown through EN
I_{OUT} = 12A



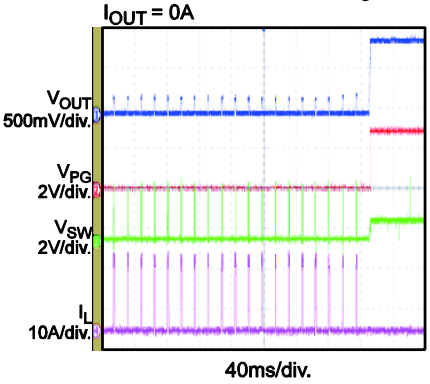
Load Transient
I_{OUT} = 6A-12A



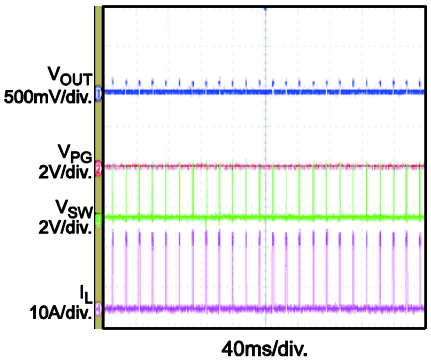
Short-Circuit Protection Entry
I_{OUT} = 0A



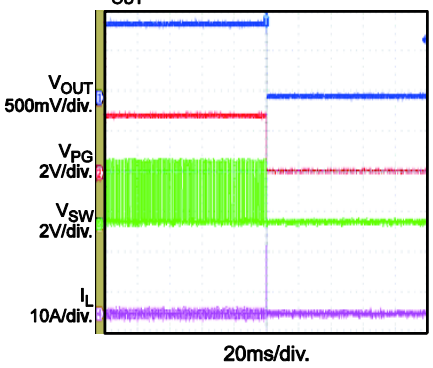
Short-Circuit Protection Recovery
I_{OUT} = 0A



Short-Circuit Protection Steady State
Short Output to GND



Short-Circuit Protection Entry, Latch Off Mode
I_{OUT}=0A



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2023 MPS. All Rights Reserved.

PIN FUNCTIONS

QFN-14 Pin#	Name	Description
1	BST	**Bootstrap**. A capacitor is required between SW and BST to form a floating supply across the high-side switch driver.
2	SW	**Switch output**. Connect SW using a wide PCB trace.
3	SCL	**I^2C serial clock**.
4	SDA	**I^2C serial data**.
5	EN	**Enable.** Set EN high to enable the MP8869W. EN has a 1.5MΩ internal pull-down resistor to GND. EN is a high-voltage pin, so it can be connected to VIN directly for auto start-up.
6	A0	**I^2C address set-up**. Connect a resistor divider from VCC to A0 to set different I^2C addresses.
7	PG	**Power good indication.** PG is an open-drain structure. PG is de-asserted if the output voltage is out of the regulation window.
8	PGND	**System power ground.** PGND is the reference ground of the regulated output voltage and requires special consideration during PCB layout. Connect PGND to the ground plane with copper traces and vias.
9	VIN	**Supply voltage.** The MP8869W operates from a 3V-to-18V input rail. Decouple the input rail with a ceramic capacitor. Connect VIN using a wide PCB trace.
10	VOUT	**Output voltage sense.** Connect VOUT to the positive terminal of the load.
11	FB	**Feedback.** Connect FB to the tap of an external resistor divider from the output to GND to set the output voltage before the I^2C takes control.
12	SS	**Soft-start set-up.** Connect a capacitor from SS to ground to set the soft-start time.
13	VCC	**Internal LDO regulator output.** Decouple VCC with a 0.47µF capacitor.
14	AGND	**Signal ground.** If AGND is not connected to PGND internally, ensure that AGND is connected to PGND during the PCB layout.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2023 MPS. All Rights Reserved.

NOT RECOMMENDED FOR NEW DESIGNS, REFER TO MMP8869S

BLOCK DIAGRAM

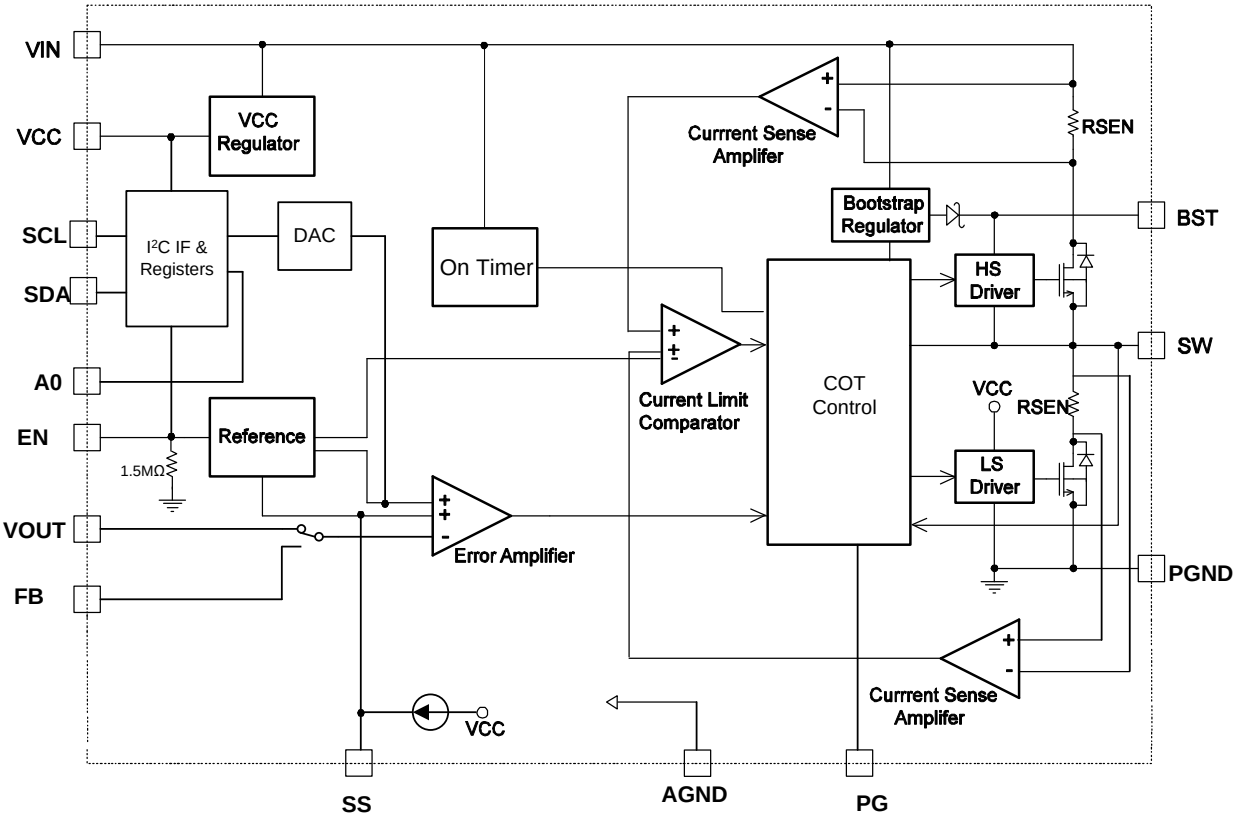


Figure 2: Functional Block Diagram

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2023 MPS. All Rights Reserved.

NOT RECOMMENDED FOR NEW DESIGNS, REFER TO MMP8869S

OPERATION

PWM Operation

The MP8869W is a fully-integrated, synchronous, rectified, step-down, switch-mode converter. The MP8869W uses constant-on-time (COT) control to provide fast transient response and easy loop stabilization. Figure 3 shows the simplified ramp compensation block. At the beginning of each cycle, the high-side MOSFET (HS-FET) turns on whenever the ramp voltage (V_{Ramp}) is lower than the error amplifier output voltage (V_{EAO}), which indicates an insufficient output voltage. The on period is determined by both the output voltage and input voltage to make the switching frequency fairly constant over the input voltage range.

After the on period elapses, the HS-FET enters the off state. By cycling the HS-FET between the on and off states, the converter regulates the output voltage. The integrated low-side MOSFET (LS-FET) turns on when the HS-FET is in its off state to minimize conduction loss.

Shoot-through occurs when both the HS-FET and LS-FET are turned on at the same time, causing a dead short between input and GND and reducing efficiency dramatically. The MP8869W prevents this by generating a dead-time (DT) internally between when the HS-FET is off and the LS-FET is on, and when the LS-FET is off and the HS-FET is on. The device enters either heavy-load operation or light-load operation depending on the amplitude of the output current.

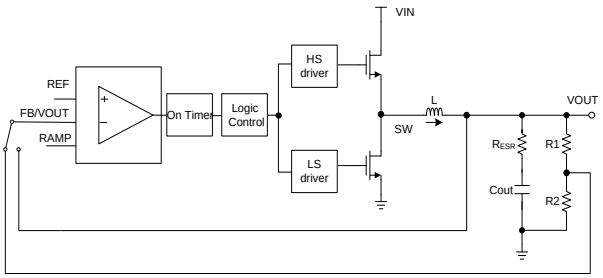


Figure 3: Simplified Compensation Block

Switching Frequency

The MP8869W uses constant-on-time (COT) control, so there is no dedicated oscillator in the IC. The input voltage is fed into the on-time one-shot timer through the internal frequency resistor. The duty ratio is VOUT/VIN, and the switching frequency is fairly constant over the input voltage range.

The MP8869W's switching frequency can be adjusted by setting the two bits D[5:4] in register 02 through I^2C communication. When the output voltage setting is low, and the input voltage is high, the switching on-time may be limited by the internal minimum on-time limit, and switching frequency decreases. Table 1 shows the maximum switching frequency vs. the output voltage when VIN = 12V and VIN = 5V.

Table 1: Maximum Frequency Selecting vs. Output Voltage

	Maximum Frequency Selecting	
Vo (V)	VIN = 12V	VIN = 5V
5	1.25MHz	/
3.3	1.25MHz	1.25MHz
2.5	1.25MHz	1.25MHz
1.8	1.25MHz	1.25MHz
1.5	1.25MHz	1.25MHz
1.2	1MHz	1.25MHz
1	750kHz	1.25MHz
0.9	750kHz	1.25MHz
0.6	500kHz	1.25MHz

Forced PWM Operation

When the MP8869W works in forced PWM mode, the MP8869W enters continuous conduction mode (CCM) where the HS-FET and LS-FET repeat the on/off operation, even if the inductor current is zero or a negative value. The switching frequency (F_{SW}) is fairly constant. Figure 4 shows the timing diagram during this operation.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2023 MPS. All Rights Reserved.

NOT RECOMMENDED FOR NEW DESIGNS, REFER TO MMP8869S

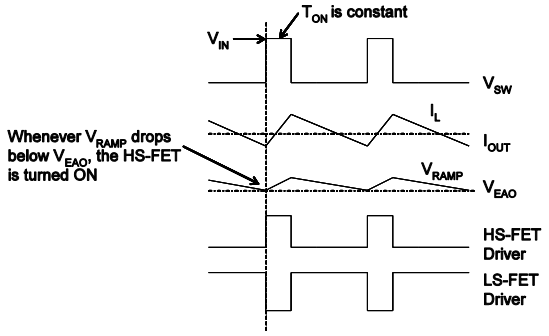


Figure 4: Forced PWM Operation

Light-Load Operation

When the MP8869W works in auto PFM/PWM mode or light-load operation, the MP8869W reduces the switching frequency automatically to maintain high efficiency, and the inductor current drops almost to zero. When the inductor current reaches zero, the LS-FET driver goes into tri-state (high-Z) (see Figure 5). The output capacitors discharge slowly to GND through R1 and R2. This operation improves device efficiency greatly when the output current is low.

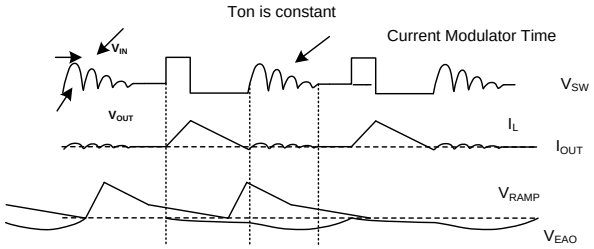


Figure 5: Light-Load Operation

Light-load operation is also called skip mode because the HS-FET does not turn on as frequently during heavy-load condition. The frequency at which the HS-FET turns on is a function of the output current. As the output current increases, the time period that the current modulator regulates becomes shorter, the HS-FET turns on more frequently, and the switching frequency increases. The output current reaches critical levels when the current modulator time is zero and can be determined with Equation (1):

$$I_{OUT} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times F_{SW} \times V_{IN}} \quad (1)$$

The device reverts to PWM mode once the output current exceeds the critical level. Afterward, the switching frequency remains fairly constant over the output current range.

The MP8869W can operate in pulse frequency modulation (PFM) mode under light load to improve efficiency (low-power mode). The MP8869W can also operate in forced PWM mode at any load condition. This mode is selectable through the I²C control. To enable low-power mode, set the Mode bit to 0. To disable low-power mode, set the mode bit to 1, and the converter will work in forced PWM mode. The Mode bit is set to 0 (PFM) by default.

Operating without an External Ramp

The traditional constant-on-time control scheme is unstable intrinsically if the output capacitor's ESR is not large enough to be an effective current-sense resistor. Ceramic capacitors cannot be used as output capacitors, usually. The MP8869W has built-in, internal ramp compensation to ensure that the system is stable, even without the help of the output capacitor's ESR. The pure ceramic capacitor solution can reduce the output ripple, total BOM cost, and board area significantly.

VCC Regulator

A 3.5V internal regulator powers most of the internal circuitries. A 470nF decoupling capacitor is needed to stabilize the regulator and reduce ripple. This regulator takes the VIN input and operates in the full VIN range. After EN is pulled high, and VIN is greater than 3.5V, the output of the regulator is in full regulation. When VIN is lower than 3.5V, the output voltage decreases and follows the input voltage. A 0.47μF ceramic capacitor is required for decoupling.

Error Amplifier (EA)

The error amplifier (EA) compares the FB voltage against the internal 0.6V reference (REF) for non-I²C mode and outputs a PWM modulation signal. In I²C mode, FB is opened, and VOUT is connected to the EA non-inverter input. The reference voltage can be programmed from 0.6V to 1.55V in the I²C control loop. The optimized internal ramp compensation minimizes the external component count and simplifies the control loop design.

Enable (EN)

EN is a digital control pin that turns the

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2023 MPS. All Rights Reserved.

regulator, including the I²C block, on and off. Drive EN high to turn on the regulator; drive EN low to turn off the regulator. An internal 1.5MΩ resistor is connected from EN to ground. EN can operate with an 18V input voltage, which allows EN to be directly connected to VIN for automatic start-up. When the external EN is high, set the EN bit to 0 in register 01 to stop the HS-FET and LS-FET from switching. The MP8869W resumes switching by setting the EN bit to 1.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The MP8869W UVLO comparator monitors the input voltage, VIN, and output voltage of the VCC regulator. The MP8869W is active when the voltages exceed the UVLO rising threshold.

Soft-Start (SS) and Pre-Bias Start-Up

The soft start (SS) prevents the converter output voltage from overshooting during start-up. When the chip starts up, the internal circuitry generates a soft-start voltage that ramps up from 0V to VCC. When SS is lower than REF, the error amplifier uses SS as the reference. When SS is higher than REF, the error amplifier uses REF as the reference.

The approximate typical soft-start time can be calculated with Equation (2):

$$t_{ss}(ms) = \frac{V_{ref}(V) \times C_{ss}(nF)}{7\mu A} \quad (2)$$

Where V_{ref} is reference voltage of the FB loop or I²C loop.

If the output of the MP8869W is pre-biased to a certain voltage during start-up, the IC disables the switching of both the HS-FET and LS-FET until the voltage on the internal SS capacitor exceeds the sensed output voltage at FB or VOUT(7).

NOTE:

V_BOOT = 1, sense FB voltage. V_BOOT = 0, sense VOUT voltage.

The MP8869W also provides a selectable soft-stop function which defines the output discharge behavior after EN shutdown. By default, the output is not controlled after EN shutdown. If setting the soft-stop control bit D[3] to 1 in register 02 via the I²C, the output is discharged linearly to zero in a quarter of the soft-start time.

Over-Current-Protection (OCP)

The MP8869W has a default, hiccup, cycle-by-cycle, over-current limiting control. The current-limit circuit employs both high-side current limit and a low-side "valley" current-sensing algorithm. The part uses the $R_{DS(ON)}$ of the LS-FET as a current-sensing element for the valley current limit. If the magnitude of the high-side current-sense signal is above the current-limit threshold, the PWM on pulse is terminated, and the LS-FET is turned on. Afterward, the inductor current is monitored by the voltage between GND and SW. GND is used as the positive current sensing node, so GND should be connected to the source terminal of the bottom MOSFET. PWM is not allowed to initiate a new cycle before the inductor current falls to the valley threshold.

After the cycle-by-cycle over-current limit occurs, the output voltage drops until VOUT is below the under-voltage (UV) threshold, typically 60% below the reference. Once UV is triggered, the MP8869W enters hiccup mode to restart the part periodically. This protection mode is especially useful when the output is dead shorted to ground. The average short-circuit current is greatly reduced to alleviate thermal issues and to protect the regulator. The MP8869W exits hiccup mode once the over-current condition is removed.

Short the output to ground first, and then power on the part. The MP8869W's I²C is disabled in this condition. The I²C resumes operation after the short circuit is removed. When hiccup OCP bit D[1] in register 01 is set to 0 by the I²C, a latch-off occurs if OCP is triggered, and FB UVP is triggered.

POWER GOOD (PG)

The power good (PG) indicates whether the output voltage is in the normal range compared to the internal reference voltage. PG is an open-drain structure. An external pull-up supply is required. During power-up, the PG output is pulled low. This indicates to the system to remain off and keep the load on the output to a minimum. This helps reduce in-rush current at start-up.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2023 MPS. All Rights Reserved.

When the output voltage is higher than 90% and lower than 115% of the internal reference voltage, and the soft start is finished, then the PG signal is pulled high. When the output voltage is lower than 85% after the soft start finishes, the PG signal remains low. When the output voltage is higher than 115% of the internal reference, PG is switched low; The PG signal rises back to high after the output voltage drops below 105% of the internal reference voltage.

PG implements an adjustable deglitch time via the I^2C whenever VOUT crosses the UV/OV rising and falling threshold. This guarantees the correct indication when the output voltage is scaled through the I^2C.

The PG output is pulled low immediately when EN UVLO, input UVLO, OCP, or OTP are triggered.

Input Over-Voltage Protection (VIN OVP)

The MP8869W monitors VIN to detect an input over-voltage event. This function is active only when the output is in OV or soft-stop condition. When the output is in OVP state, or soft stop is enabled, output discharge is enabled to charge the input voltage high. When the input voltage exceeds the input OVP threshold, both the HS-FET and LS-FET stop switching.

Output Over-Voltage Protection (OVP)

The MP8869W monitors both FB and VOUT to detect an over-voltage event. When setting the V_BOOT bit to 1, an internal comparator monitors FB. When setting the V_BOOT bit to 0, the internal comparator monitors VOUT. When the FB or VOUT voltage becomes higher than 125% of the internal reference voltage, the controller enters dynamic regulation mode, and the input voltage may be charged up during this time. When input OVP is triggered, the IC stops switching. If OVP mode is set to “Auto Retry” in the I^2C, the IC begins switching once the input voltage drops below the VIN OVP recover threshold. Otherwise, the MP8869W latches off. OVP auto-retry mode or latch-off mode occurs only if the soft start has finished.

Dynamic regulation mode can be operated by turning on the low side until the low-side negative current limit is triggered. Then the body diode of the HS-FET free-wheels the current. The output power charges the input, which may trigger the VIN OVP function. In VIN OVP, neither the HS-FET or LS-FET turn on and stop charging VIN. If the output is still over-voltage and the input voltage drops below the VIN OVP threshold, repeat the operation. If the output voltage is below 110% of the internal reference voltage, then output OVP is exited.

Output Absolute Over-Voltage Protection (OVP_ABS)

The MP8869W monitors the VOUT voltage to detect absolute over-voltage protection. When VOUT is larger than 6.5V, the controller enters dynamic regulation mode if the OVP retry bit is set to 1 in the I^2C register 01. Otherwise, the MP8869W latches off when output OVP and input OVP are both triggered. Absolute over-voltage protection works once both the input voltage and EN are higher than their rising thresholds. This means that this function can work even during a soft start.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die reaches temperatures that exceed 160°C, the entire chip shuts down. When the temperature is less than its lower threshold (typically 140°C), the chip is enabled again.

The D[1] and D[2] bits can be monitored in register 06 for more information about IC silicon temperature.

Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own UVLO protection. This UVLO’s rising threshold is 2.4V with a 150mV hysteresis. The bootstrap capacitor voltage is regulated by VIN internally through D1, M1, C4, L1, and C2 (see Figure 6). If V_{BST} - V_{SW} exceeds 3.3V, U1 regulates M1 to maintain a 3.3V BST voltage across C4.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2023 MPS. All Rights Reserved.

NOT RECOMMENDED FOR NEW DESIGNS, REFER TO MMP8869S

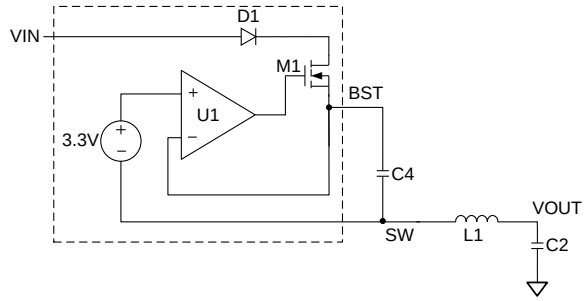


Figure 6: Internal Bootstrap Charging Circuit

START-UP AND SHUTDOWN

If VIN, VCC, and EN exceed their respective thresholds, the chip starts up. The reference block starts first, generating stable reference voltages and currents, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

Several events can shut down the chip: EN low, VIN low, VCC low, thermal shutdown, OVP latch, and OCP latch. In the shutdown procedure, the signaling path is first blocked to avoid any fault triggering. V_{EAO} and the internal supply rail are then pulled down.

I²C Control and Default Output Voltage

When the MP8869W is enabled, the output voltage is determined by the FB resistors with a programmed soft-start time. After that, the I²C bus can communicate with the master. If the chip does not receive I²C communication signal continuously, it can works well through FB and performs behavior similar to a traditional non-I²C part. The output voltage is determined by the resistor dividers R1, R2, and FB reference voltage. V_{OUT} can be calculated using Equation (3):

$$Vout(V) = 0.6 \times (1 + \frac{R1}{R2}) \quad (3)$$

The FB loop V_{REF} is 0.6V. The FB loop reference voltage is a fixed value that cannot be adjusted by the I²C.

Loop Switch

There is no output slew rate control during the FB loop to the I2C loop. When the output voltage setting is much larger or smaller than the present voltage, it is recommended to take two steps to finish the loop switch and output voltage setting. During the FB loop to the I²C loop, first set the output voltage in the I²C loop to the present output voltage, and then set V_BOOT = 0 to switch the FB loop to the I²C loop. Second, change the output voltage to the target with slew rate control in the I²C loop. Please refer to the Output Voltage Dynamic Scaling section on page 30 for details.

In the I²C control loop, the output voltage is determined by the I²C control, and the FB feedback loop is disabled. After the MP8869W receives a valid data byte of the output voltage setting, the MP8869W adjusts the DAC output as the reference voltage with a controlled slew rate. The slew rate is determined by three bits D[5:3] in register 01.

I²C Slave Address

To support multiple devices used on the same I²C bus, A0 can be used to select four different addresses. A resistor divider from VCC to GND can achieve an accurate reference voltage. Connect A0 to this reference voltage to set a different I²C slave address (see Figure 7). The internal circuit changes the I²C address accordingly. When the master sends an 8-bit address value, the 7-bit I²C address should be followed by 0/1 to indicate a write/read operation. Table 2 shows the recommended I²C address selection by the A0 voltage.

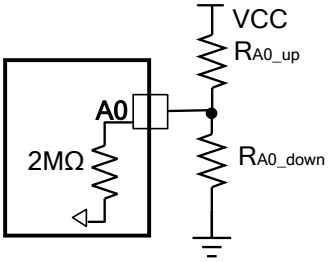


Figure 7: I²C Slave Address Selection Set-Up

Table 2: Recommended I²C Slave Address Selection by A0 Resistor Divider

A0 Upper Resistor R_{A0_up}(kΩ)	A0 Lower Resistor R_{A0_down}(kΩ)	I²C Slave Address	
		Binary	Hex
No connect	No connect	110 0000	60H
500	300	110 0010	62H
300	500	110 0100	64H
100	No connect	110 0110	66H

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2023 MPS. All Rights Reserved.

NOT RECOMMENDED FOR NEW DESIGNS, REFER TO MMP8869S

I²C INTERFACE

I²C Serial Interface Description

The I²C is a 2-wire, bidirectional, serial interface consisting of a data line (SDA) and a clock line (SCL). The lines are pulled to a bus voltage externally when they are idle. When connecting to the line, a master device generates the SCL signal and device address and arranges the communication sequence. The MP8869W interface is an I²C slave. The I²C interface adds flexibility to the power supply solution. The output voltage, transition slew rate, and other parameters can be controlled by the I²C interface instantaneously.

Data Validity

One clock pulse is generated for each data bit transferred. The data on the SDA line must be stable during the high period of the clock. The high or low state of the data line can only change when the clock signal on the SCL line is low (see Figure 8).

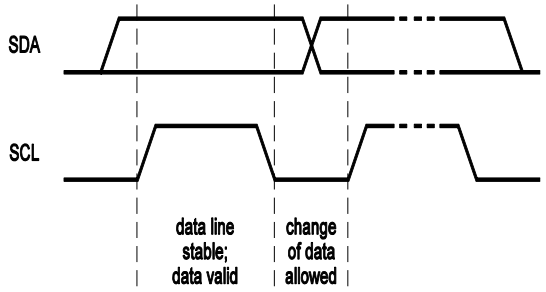


Figure 8: Bit Transfer on the I²C Bus

Start and stop are signaled by the master device, which signifies the beginning and the end of the I²C transfer. The start condition is defined as the SDA signal transitioning from high to low while the SCL is HIGH. The stop condition is defined as the SDA signal transitioning from low to high while the SCL is high (see Figure 9).

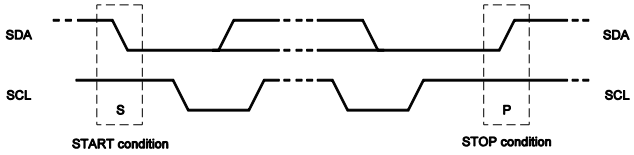


Figure 9: Start and Stop Conditions

Start and stop conditions are always generated by the master. The bus is considered to be busy after the start condition, and is considered to be free again after a minimum of 4.7µs after the stop condition. The bus remains busy if a repeated start (Sr) is generated instead of a stop condition. The start (S) and repeated start (Sr) conditions are functionally identical.

Transfer Data

Every byte put on the SDA line must be eight bits long. Each byte has to be followed by an acknowledge bit. The acknowledge-related clock pulse is generated by the master. The transmitter releases the SDA line (high) during the acknowledge clock pulse. The receiver must pull down the SDA line during the acknowledge clock pulse so that it remains stable low during the high period of this clock pulse.

Data transfers follow the format shown in Figure 10. After the start condition (S), a slave address is sent. This address is 7 bits long followed by an eighth bit data direction bit (R/W). A zero indicates a transmission (write), and a one indicates a request for data (read). A data transfer is always terminated by a stop condition (P) generated by the master. However, if a master still wishes to communicate on the bus, it can generate a repeated start condition (Sr) and address another slave without first generating a stop condition.

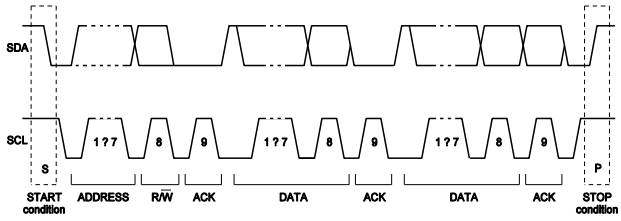


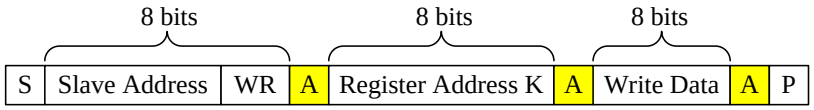
Figure 10: Complete Data Transfer

The MP8869W requires a start condition, a valid I²C address, a register address byte, and a data byte for a single data update. After receiving each byte, the MP8869W acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I²C address selects the MP8869W. The MP8869W performs an update on the falling edge of the LSB byte.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2023 MPS. All Rights Reserved.

NOT RECOMMENDED FOR NEW DESIGNS, REFER TO MMP8869S

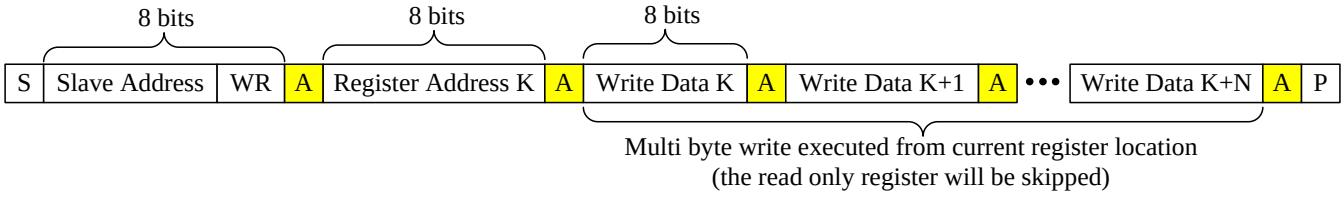
I²C Write and Read Sequence Example



Master to Slave — A = Acknowledge (SDA = LOW) — S = Start Condition — WR Write = 0

Slave to Master — NA = NOT Acknowledge (SDA = HIGH) — P = Stop Condition — RD Read = 1

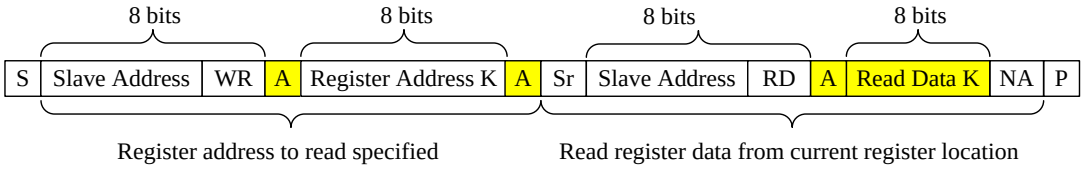
I²C Write Example --- Write Single Register



Master to Slave — A = Acknowledge (SDA = LOW) — S = Start Condition — WR Write = 0

Slave to Master — NA = NOT Acknowledge (SDA = HIGH) — P = Stop Condition — RD Read = 1

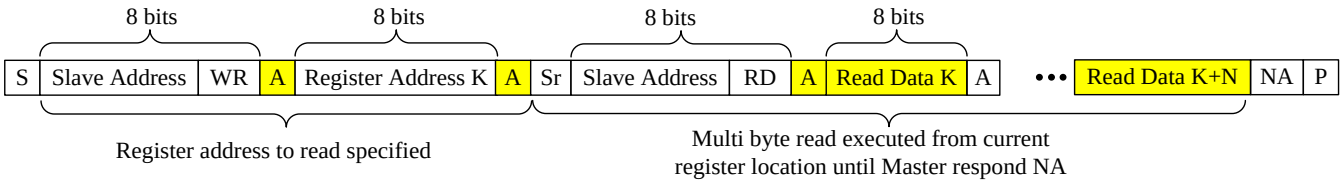
I²C Write Example --- Write Multi Register



Master to Slave — A = Acknowledge (SDA = LOW) — S = Start Condition — Sr = Repeat Start Condition — WR Write = 0

Slave to Master — NA = NOT Acknowledge (SDA = HIGH) — P = Stop Condition — RD Read = 1

I²C Read Example --- Read Single Register



Master to Slave — A = Acknowledge (SDA = LOW) — S = Start Condition — Sr = Repeat Start Condition — WR Write = 0

Slave to Master — NA = NOT Acknowledge (SDA = HIGH) — P = Stop Condition — RD Read = 1

I²C Read Example --- Read Multi Register

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2023 MPS. All Rights Reserved.

NOT RECOMMENDED FOR NEW DESIGNS, REFER TO MMP8869S

REGISER DESCRIPTION

Register Map

The MP8869W contains six write or read registers. Register 00 is the output voltage selection register. Register 01 is the first system control register, and users can use it to set the slew rate, hiccup OCP, etc. Register 02 is the second system control register, and users can use it to set the switching frequency, current limit, etc.

Register 03 and register 04 are output current and output voltage indicating registers. Register 05 is the IC ID register. Register 06 is the IC status indication register, and users can use it to check if the IC is in over-current protection, over-temperature protection status, etc. The register map is shown below.

ADD	NAME	R/W	D7	D6	D5	D4	D3	D2	D1	D0
00	VSEL	R/W	V_BOOT	Output Reference						
01	SysCntlreg1	R/W	EN	GO_BIT	Slew rate			Retry OVP	Hiccup OCP	Mode
02	SysCntlreg2	R/W	PG deglitch time		Switching frequency		Soft stop	Current limit adjust		
03	Output current	R	Output current							
04	Output voltage	R	Output voltage							
05	ID1	R	Vendor ID				Die ID			
06	Status	R	Reserved				OC	OTEW	OT	PG

Register Description

1) Reg00 VSEL

Register 00 is the output voltage selection register. The MP8869W default output voltage is determined by the FB resistor divider after the MP8869W power start-up or EN start-up. The reference voltage in the FB control loop is fixed at 0.6V.

After the MP8869W starts up, the output voltage can be controlled by the I^2C through setting the highest bit V_BOOT = 0. Before adjusting the output reference voltage, the bit GO_BIT of the first system control Register 01 should be set to 1, and then the output reference voltage can be adjusted by the lower seven bits of register 00 in the I^2C loop. When the output reference voltage setting command is finished, GO_BIT auto-resets to 0 to prevent false operation of the VOUT scaling. GO_BIT should be set to 1 before adjusting the output reference voltage in the I^2C loop.

Table 3 shows the output voltage selection chart from 0.6V to 1.55V in the I^2C control loop.

NAME	BITS	DEFAULT	DESCRIPTION
V_BOOT	D[7]	1	FB control loop enable bit. V_BOOT = 1 means the output voltage is determined by the resistor divider connecting to FB. The FB reference voltage is fixed at 0.6V. V_BOOT = 0 means the output voltage is controlled by I^2C through VOUT. This bit is helpful for the default output voltage setting before the I^2C signal is active. If the I^2C is not used, the part works well with FB.
Output reference	D[6:0]	001 1110	Set the output voltage from 0.6V to 1.55V (see Table 3). The default value is 0.825V.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2023 MPS. All Rights Reserved.

NOT RECOMMENDED FOR NEW DESIGNS, REFER TO MMP8869S

Table 3: Output Voltage Selection Chart

D[6:0]	VOUT(V)	D[6:0]	VOUT(V)	D[6:0]	VOUT(V)	D[6:0]	VOUT(V)
000 0000	0.6	010 0000	0.84	100 0000	1.08	110 0000	1.32
000 0001	0.6075	010 0001	0.8475	100 0001	1.0875	110 0001	1.3275
000 0010	0.615	010 0010	0.855	100 0010	1.095	110 0010	1.335
000 0011	0.6225	010 0011	0.8625	100 0011	1.1025	110 0011	1.3425
000 0100	0.63	010 0100	0.87	100 0100	1.11	110 0100	1.35
000 0101	0.6375	010 0101	0.8775	100 0101	1.1175	110 0101	1.3575
000 0110	0.645	010 0110	0.885	100 0110	1.125	110 0110	1.365
000 0111	0.6525	010 0111	0.8925	100 0111	1.1325	110 0111	1.3725
000 1000	0.66	010 1000	0.9	100 1000	1.14	110 1000	1.38
000 1001	0.6675	010 1001	0.9075	100 1001	1.1475	110 1001	1.3875
000 1010	0.675	010 1010	0.915	100 1010	1.155	110 1010	1.395
000 1011	0.6825	010 1011	0.9225	100 1011	1.1625	110 1011	1.4025
000 1100	0.69	010 1100	0.93	100 1100	1.17	110 1100	1.41
000 1101	0.6975	010 1101	0.9375	100 1101	1.1775	110 1101	1.4175
000 1110	0.705	010 1110	0.945	100 1110	1.185	110 1110	1.425
000 1111	0.7125	010 1111	0.9525	100 1111	1.1925	110 1111	1.4325
001 0000	0.72	011 0000	0.96	101 0000	1.2	111 0000	1.44
001 0001	0.7275	011 0001	0.9675	101 0001	1.2075	111 0001	1.4475
001 0010	0.735	011 0010	0.975	101 0010	1.215	111 0010	1.455
001 0011	0.7425	011 0011	0.9825	101 0011	1.2225	111 0011	1.4625
001 0100	0.75	011 0100	0.99	101 0100	1.23	111 0100	1.47
001 0101	0.7575	011 0101	0.9975	101 0101	1.2375	111 0101	1.4775
001 0110	0.765	011 0110	1.005	101 0110	1.245	111 0110	1.485
001 0111	0.7725	011 0111	1.0125	101 0111	1.2525	111 0111	1.4925
001 1000	0.78	011 1000	1.02	101 1000	1.26	111 1000	1.5
001 1001	0.7875	011 1001	1.0275	101 1001	1.2675	111 1001	1.5075
001 1010	0.795	011 1010	1.035	101 1010	1.275	111 1010	1.515
001 1011	0.8025	011 1011	1.0425	101 1011	1.2825	111 1011	1.5225
001 1100	0.81	011 1100	1.05	101 1100	1.29	111 1100	1.53
001 1101	0.8175	011 1101	1.0575	101 1101	1.2975	111 1101	1.5375
001 1110	0.825	011 1110	1.065	101 1110	1.305	111 1110	1.545
001 1111	0.8325	011 1111	1.0725	101 1111	1.3125	111 1111	1.5525

2) Reg01 SysCntlreg1

Register 01 is the first system control register.

The highest bit, EN, can be used to turn the part on or off when the external EN is high. When the external EN is high, after part shuts down by setting the EN bit to 0, and then the HS-FET and LS-FET stop switching. The part resumes switching by setting the EN bit to 1 again. When the external EN is low, the converter is off, and the I^2C shuts down.

The bit GO_BIT is only used for output reference setting in the I^2C loop. Set GO_BIT to 1 to enable the I^2C authority of writing the output reference. When the command is finished, GO_BIT auto-resets to 0 to prevent false operation of the VOUT scaling.

The IC switches to forced PWM mode when the GO_BIT is set to 1 to achieve a smooth output waveform during the output dynamic scaling. After the output scaling is complete, GO_BIT is set to 0 automatically, and the IC operation mode switches to the original mode set by the MODE bit.

The 3-bit slew rate D[5:3] is used for slew rate selection during the output voltage dynamic scaling when the output voltage is controlled by the I^2C loop. A proper slew rate reduces the inrush current, as well as voltage overshoot and undershoot. Eight different slew rate levels can be selected.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2023 MPS. All Rights Reserved.

The bit Retry OVP defines the protection mode when OVP is triggered. When Retry OVP is set to 1, the part enters auto-recovery when OVP is removed. When Retry OVP is set to the part latches off once output OVP occurs, and VIN OVP is triggered until VIN or EN are toggled.

The bit Hiccup OCP defines the over-current protection mode. When Hiccup OCP is set to 1, the part enters hiccup mode when OCP and UVP are both triggered. When Hiccup OCP is set to 0, the part enters latch-off when OCP and UVP are both triggered.

The lowest bit, Mode, is used for selecting forced PWM or auto PFM/PWM mode at light load. When Mode is set to 0, auto-PFM/PWM mode is enabled at light load. When Mode is set to 1, forced PWM mode is enabled at light load.

<table>
<tr><th>NAME</th><th>BITS</th><th>DEFAULT</th><th>DESCRIPTION</th></tr>
<tr><td>EN</td><td>D[7]</td><td>1</td><td>I²C controlled turn-on or turn-off of the part. When the external EN is low, the converter is off and I²C shuts down. When EN is high, the EN bit takes over. The default EN bit is 1.</td></tr>
<tr><td>GO_BIT</td><td>D[6]</td><td>0</td><td>Switch bit of the I²C writing authority for output reference command only. Set GO_BIT = 1 to enable the I²C authority of writing the output reference. When the command is finished, GO_BIT auto-resets to 0 to prevent false operation of the VOUT scaling. Write the GO_BIT = 1 first, then write the output reference voltage and change the V_BOOT status.
Voltage scaling examples:
1) Set GO_BIT = 1.
2) Write register 00: set V_BOOT = 0 and set the output reference.
3) Read back the GO_BIT value to see if the output scaling is finished. If GO_BIT = 0, the voltage scaling is done. Otherwise, VOUT is still in adjustment.
4) Set GO_BIT = 1 if output voltage scaling is needed a second time.
5) Write register 00: set V_BOOT = 0 and set the output reference.</td></tr>
<tr><td>Slew rate</td><td>D[5:3]</td><td>100</td><td>The slew rate during the I²C-controlled voltage changing is defined by three bits. The output voltage changes linearly from the previous voltage to the new set voltage with a below slew rate. This helps to reduce the inrush current, voltage overshoot, and voltage undershoot greatly.
<table>
<tr><th>D[5:3]</th><th>Slew Rate</th><th>D[5:3]</th><th>Slew Rate</th></tr>
<tr><td>000</td><td>40mV/μs</td><td>100</td><td>5mV/μs</td></tr>
<tr><td>001</td><td>30mV/μs</td><td>101</td><td>2.5mV/μs</td></tr>
<tr><td>010</td><td>20mV/μs</td><td>110</td><td>1.25mV/μs</td></tr>
<tr><td>011</td><td>10mV/μs</td><td>111</td><td>0.625mV/μs</td></tr>
</table></td></tr>
<tr><td>Retry OVP</td><td>D[2]</td><td>1</td><td>FB or VOUT over-voltage protection mode selection bit. 1 means the part auto-recovers when OVP is removed. 0 means the part latches off once output OVP and VIN OVP are both triggered until VIN or EN is power reset.</td></tr>
<tr><td>Hiccup OCP</td><td>D[1]</td><td>1</td><td>Over-current protection mode selection. 1 means hiccup mode OCP. 0 means latch-off type OCP.</td></tr>
<tr><td>Mode</td><td>D[0]</td><td>0</td><td>Set Mode to 0 to enable PFM mode; set Mode to 1 to disable auto-PFM/PWM mode. Default is auto-PFM/PWM mode for light load.</td></tr>
</table>

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2023 MPS. All Rights Reserved.

NOT RECOMMENDED FOR NEW DESIGNS, REFER TO MMP8869S

3) Reg02 SysCntlreg2

Register 02 is the second system control register.

The highest two bits of the PG deglitch time D[7:6] defines the power good signal rising and falling edge delay times. When output OVP or UVP is triggered, the PG signal turns low or high after a delay time. There are four levels of PG delay time that can be programmed by the I^2C in different conditions.

The two switching frequency bits D[5:4] are used for switching frequency selection. The MP8869W supports up to 1.25MHz of switching frequency by setting the two bits to 11. The MP8869W maximum programmable switching frequency is limited by internal minimum on-time (see Table 1).

The bit Soft Stop defines the output voltage discharge behavior after EN shutdown. When Soft Stop is set to 0, the output voltage is not controlled after EN shutdown. When Soft Stop is set to 1, the output voltage is discharged linearly to zero with the set soft-stop time.

The lowest three bits, Current Limit Adjust D[2:0], are used for peak and valley current-limit selection. There are eight levels of current limit that can be selected for different application conditions.

NAME	BITS	DEFAULT	DESCRIPTION			
PG deglitch time	D[7:6]	11	Power good signal rising and falling edges' delay time. When FB or VOUT is out of regulation window, the PG comparator is triggered, but needs a delay time before the PG signal can turn high or low.			
			D[7:6]	PG Deglitch	D[7:6]	PG Deglitch
			00	<1μs	10	12μs
			01	6μs	11	30μs
Switching frequency	D[5:4]	00	Switching frequency set bit. There is no dedicated frequency oscillator inside the part. The switching frequency is fairly fixed by controlling the T_{ON} timer.			
			D[5:4]	Frequency	D[5:4]	Frequency
			00	500kHz	10	1MHz
			01	750kHz	11	1.25MHz
Soft stop	D[3]	0	This bit defines the VOUT discharge behavior after EN shutdown. "0" means VOUT is not controlled after EN shutdown; "1" means VOUT is discharged linearly to zero with the set soft-stop time.			
Current limit adjust	D[2:0]	001	D[2:0]	Valley Current Limit (A)	D[2:0]	Valley Current Limit (A)
			000	16	100	8.5
			001	14	101	7
			010	12	110	6
			011	10	111	5

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2023 MPS. All Rights Reserved.

4) Reg03 Output Current

Register 03 is an output current-indicating register. After the part starts up, the DC output current information can be read through the I^2C communication.

When the inductor current is in DCM, the output current sense is not very accurate. The Mode bit can be set to 1 (PWM mode) for good current sensing accuracy at light load. When the inductor current enters CCM, the output current sense accuracy is excellent (typical accuracy is 5% when the output current is higher than 2A).

Table 4 shows the output current chart from 0A to 12.75A.

NAME	BITS	DEFAULT	DESCRIPTION
Output current	D[7:0]	0000 0000	Output current monitor bits. Table 4 shows the output current monitor chart.

Table 4: Output Current Chart

D[7:0]	I_{OUT}(A)	D[7:0]	I_{OUT}(A)	D[7:0]	I_{OUT}(A)	D[7:0]	I_{OUT}(A)	D[7:0]	I_{OUT}(A)	D[7:0]	I_{OUT}(A)
0000 0000	0	0010 1011	2.15	0101 0110	4.3	1000 0001	6.45	1010 1100	8.6	1101 0111	10.75
0000 0001	0.05	0010 1100	2.2	0101 0111	4.35	1000 0010	6.5	1010 1101	8.65	1101 1000	10.8
0000 0010	0.1	0010 1101	2.25	0101 1000	4.4	1000 0011	6.55	1010 1110	8.7	1101 1001	10.85
0000 0011	0.15	0010 1110	2.3	0101 1001	4.45	1000 0100	6.6	1010 1111	8.75	1101 1010	10.9
0000 0100	0.2	0010 1111	2.35	0101 1010	4.5	1000 0101	6.65	1011 0000	8.8	1101 1011	10.95
0000 0101	0.25	0011 0000	2.4	0101 1011	4.55	1000 0110	6.7	1011 0001	8.85	1101 1100	11
0000 0110	0.3	0011 0001	2.45	0101 1100	4.6	1000 0111	6.75	1011 0010	8.9	1101 1101	11.05
0000 0111	0.35	0011 0010	2.5	0101 1101	4.65	1000 1000	6.8	1011 0011	8.95	1101 1110	11.1
0000 1000	0.4	0011 0011	2.55	0101 1110	4.7	1000 1001	6.85	1011 0100	9	1101 1111	11.15
0000 1001	0.45	0011 0100	2.6	0101 1111	4.75	1000 1010	6.9	1011 0101	9.05	1110 0000	11.2
0000 1010	0.5	0011 0101	2.65	0110 0000	4.8	1000 1011	6.95	1011 0110	9.1	1110 0001	11.25
0000 1011	0.55	0011 0110	2.7	0110 0001	4.85	1000 1100	7	1011 0111	9.15	1110 0010	11.3
0000 1100	0.6	0011 0111	2.75	0110 0010	4.9	1000 1101	7.05	1011 1000	9.2	1110 0011	11.35
0000 1101	0.65	0011 1000	2.8	0110 0011	4.95	1000 1110	7.1	1011 1001	9.25	1110 0100	11.4
0000 1110	0.7	0011 1001	2.85	0110 0100	5	1000 1111	7.15	1011 1010	9.3	1110 0101	11.45
0000 1111	0.75	0011 1010	2.9	0110 0101	5.05	1001 0000	7.2	1011 1011	9.35	1110 0110	11.5
0001 0000	0.8	0011 1011	2.95	0110 0110	5.1	1001 0001	7.25	1011 1100	9.4	1110 0111	11.55
0001 0001	0.85	0011 1100	3	0110 0111	5.15	1001 0010	7.3	1011 1101	9.45	1110 1000	11.6
0001 0010	0.9	0011 1101	3.05	0110 1000	5.2	1001 0011	7.35	1011 1110	9.5	1110 1001	11.65
0001 0011	0.95	0011 1110	3.1	0110 1001	5.25	1001 0100	7.4	1011 1111	9.55	1110 1010	11.7
0001 0100	1	0011 1111	3.15	0110 1010	5.3	1001 0101	7.45	1100 0000	9.6	1110 1011	11.75
0001 0101	1.05	0100 0000	3.2	0110 1011	5.35	1001 0110	7.5	1100 0001	9.65	1110 1100	11.8
0001 0110	1.1	0100 0001	3.25	0110 1100	5.4	1001 0111	7.55	1100 0010	9.7	1110 1101	11.85
0001 0111	1.15	0100 0010	3.3	0110 1101	5.45	1001 1000	7.6	1100 0011	9.75	1110 1110	11.9
0001 1000	1.2	0100 0011	3.35	0110 1110	5.5	1001 1001	7.65	1100 0100	9.8	1110 1111	11.95
0001 1001	1.25	0100 0100	3.4	0110 1111	5.55	1001 1010	7.7	1100 0101	9.85	1111 0000	12
0001 1010	1.3	0100 0101	3.45	0111 0000	5.6	1001 1011	7.75	1100 0110	9.9	1111 0001	12.05
0001 1011	1.35	0100 0110	3.5	0111 0001	5.65	1001 1100	7.8	1100 0111	9.95	1111 0010	12.1
0001 1100	1.4	0100 0111	3.55	0111 0010	5.7	1001 1101	7.85	1100 1000	10	1111 0011	12.15
0001 1101	1.45	0100 1000	3.6	0111 0011	5.75	1001 1110	7.9	1100 1001	10.05	1111 0100	12.2
0001 1110	1.5	0100 1001	3.65	0111 0100	5.8	1001 1111	7.95	1100 1010	10.1	1111 0101	12.25
0001 1111	1.55	0100 1010	3.7	0111 0101	5.85	1010 0000	8	1100 1011	10.15	1111 0110	12.3
0010 0000	1.6	0100 1011	3.75	0111 0110	5.9	1010 0001	8.05	1100 1100	10.2	1111 0111	12.35
0010 0001	1.65	0100 1100	3.8	0111 0111	5.95	1010 0010	8.1	1100 1101	10.25	1111 1000	12.4
0010 0010	1.7	0100 1101	3.85	0111 1000	6	1010 0011	8.15	1100 1110	10.3	1111 1001	12.45
0010 0011	1.75	0100 1110	3.9	0111 1001	6.05	1010 0100	8.2	1100 1111	10.35	1111 1010	12.5
0010 0100	1.8	0100 1111	3.95	0111 1010	6.1	1010 0101	8.25	1101 0000	10.4	1111 1011	12.55
0010 0101	1.85	0101 0000	4	0111 1011	6.15	1010 0110	8.3	1101 0001	10.45	1111 1100	12.6
0010 0110	1.9	0101 0001	4.05	0111 1100	6.2	1010 0111	8.35	1101 0010	10.5	1111 1101	12.65
0010 0111	1.95	0101 0010	4.1	0111 1101	6.25	1010 1000	8.4	1101 0011	10.55	1111 1110	12.7
0010 1000	2	0101 0011	4.15	0111 1110	6.3	1010 1001	8.45	1101 0100	10.6	1111 1111	12.75
0010 1001	2.05	0101 0100	4.2	0111 1111	6.35	1010 1010	8.5	1101 0101	10.65		
0010 1010	2.1	0101 0101	4.25	1000 0000	6.4	1010 1011	8.55	1101 0110	10.7		

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2023 MPS. All Rights Reserved.

NOT RECOMMENDED FOR NEW DESIGNS, REFER TO MMP8869S

5) Reg04 Output Voltage

Register 04 is an output voltage-indicating register. After part starts up, the output voltage can be read through the I^2C communication.

Table 5 shows the output voltage chart from 0.35V to 2.52V.

NAME	BITS	DEFAULT	DESCRIPTION
Output voltage	D[7:0]	0000 0000	Output voltage monitor bits. Table 5 shows the output voltage monitor chart.

Table 5: Output Voltage Chart

D[7:0]	V_{OUT} (V)	D[7:0]	V_{OUT} (V)	D[7:0]	V_{OUT} (V)	D[7:0]	V_{OUT} (V)	D[7:0]	V_{OUT} (V)	D[7:0]	V_{OUT} (V)
0000 0000	0.35	0010 1011	0.7155	0101 0110	1.081	1000 0001	1.4465	1010 1100	1.812	1101 0111	2.1775
0000 0001	0.3585	0010 1100	0.724	0101 0111	1.0895	1000 0010	1.455	1010 1101	1.8205	1101 1000	2.186
0000 0010	0.367	0010 1101	0.7325	0101 1000	1.098	1000 0011	1.4635	1010 1110	1.829	1101 1001	2.1945
0000 0011	0.3755	0010 1110	0.741	0101 1001	1.1065	1000 0100	1.472	1010 1111	1.8375	1101 1010	2.203
0000 0100	0.384	0010 1111	0.7495	0101 1010	1.115	1000 0101	1.4805	1011 0000	1.846	1101 1011	2.2115
0000 0101	0.3925	0011 0000	0.758	0101 1011	1.1235	1000 0110	1.489	1011 0001	1.8545	1101 1100	2.22
0000 0110	0.401	0011 0001	0.7665	0101 1100	1.132	1000 0111	1.4975	1011 0010	1.863	1101 1101	2.2285
0000 0111	0.4095	0011 0010	0.775	0101 1101	1.1405	1000 1000	1.506	1011 0011	1.8715	1101 1110	2.237
0000 1000	0.418	0011 0011	0.7835	0101 1110	1.149	1000 1001	1.5145	1011 0100	1.88	1101 1111	2.2455
0000 1001	0.4265	0011 0100	0.792	0101 1111	1.1575	1000 1010	1.523	1011 0101	1.8885	1110 0000	2.254
0000 1010	0.435	0011 0101	0.8005	0110 0000	1.166	1000 1011	1.5315	1011 0110	1.897	1110 0001	2.2625
0000 1011	0.4435	0011 0110	0.809	0110 0001	1.1745	1000 1100	1.54	1011 0111	1.9055	1110 0010	2.271
0000 1100	0.452	0011 0111	0.8175	0110 0010	1.183	1000 1101	1.5485	1011 1000	1.914	1110 0011	2.2795
0000 1101	0.4605	0011 1000	0.826	0110 0011	1.1915	1000 1110	1.557	1011 1001	1.9225	1110 0100	2.288
0000 1110	0.469	0011 1001	0.8345	0110 0100	1.2	1000 1111	1.5655	1011 1010	1.931	1110 0101	2.2965
0000 1111	0.4775	0011 1010	0.843	0110 0101	1.2085	1001 0000	1.574	1011 1011	1.9395	1110 0110	2.305
0001 0000	0.486	0011 1011	0.8515	0110 0110	1.217	1001 0001	1.5825	1011 1100	1.948	1110 0111	2.3135
0001 0001	0.4945	0011 1100	0.86	0110 0111	1.2255	1001 0010	1.591	1011 1101	1.9565	1110 1000	2.322
0001 0010	0.503	0011 1101	0.8685	0110 1000	1.234	1001 0011	1.5995	1011 1110	1.965	1110 1001	2.3305
0001 0011	0.5115	0011 1110	0.877	0110 1001	1.2425	1001 0100	1.608	1011 1111	1.9735	1110 1010	2.339
0001 0100	0.52	0011 1111	0.8855	0110 1010	1.251	1001 0101	1.6165	1100 0000	1.982	1110 1011	2.3475
0001 0101	0.5285	0100 0000	0.894	0110 1011	1.2595	1001 0110	1.625	1100 0001	1.9905	1110 1100	2.356
0001 0110	0.537	0100 0001	0.9025	0110 1100	1.268	1001 0111	1.6335	1100 0010	1.999	1110 1101	2.3645
0001 0111	0.5455	0100 0010	0.911	0110 1101	1.2765	1001 1000	1.642	1100 0011	2.0075	1110 1110	2.373
0001 1000	0.554	0100 0011	0.9195	0110 1110	1.285	1001 1001	1.6505	1100 0100	2.016	1110 1111	2.3815
0001 1001	0.5625	0100 0100	0.928	0110 1111	1.2935	1001 1010	1.659	1100 0101	2.0245	1111 0000	2.39
0001 1010	0.571	0100 0101	0.9365	0111 0000	1.302	1001 1011	1.6675	1100 0110	2.033	1111 0001	2.3985
0001 1011	0.5795	0100 0110	0.945	0111 0001	1.3105	1001 1100	1.676	1100 0111	2.0415	1111 0010	2.407
0001 1100	0.588	0100 0111	0.9535	0111 0010	1.319	1001 1101	1.6845	1100 1000	2.05	1111 0011	2.4155
0001 1101	0.5965	0100 1000	0.962	0111 0011	1.3275	1001 1110	1.693	1100 1001	2.0585	1111 0100	2.424
0001 1110	0.605	0100 1001	0.9705	0111 0100	1.336	1001 1111	1.7015	1100 1010	2.067	1111 0101	2.4325
0001 1111	0.6135	0100 1010	0.979	0111 0101	1.3445	1010 0000	1.71	1100 1011	2.0755	1111 0110	2.441
0010 0000	0.622	0100 1011	0.9875	0111 0110	1.353	1010 0001	1.7185	1100 1100	2.084	1111 0111	2.4495
0010 0001	0.6305	0100 1100	0.996	0111 0111	1.3615	1010 0010	1.727	1100 1101	2.0925	1111 1000	2.458
0010 0010	0.639	0100 1101	1.0045	0111 1000	1.37	1010 0011	1.7355	1100 1110	2.101	1111 1001	2.4665
0010 0011	0.6475	0100 1110	1.013	0111 1001	1.3785	1010 0100	1.744	1100 1111	2.1095	1111 1010	2.475
0010 0100	0.656	0100 1111	1.0215	0111 1010	1.387	1010 0101	1.7525	1101 0000	2.118	1111 1011	2.4835
0010 0101	0.6645	0101 0000	1.03	0111 1011	1.3955	1010 0110	1.761	1101 0001	2.1265	1111 1100	2.492
0010 0110	0.673	0101 0001	1.0385	0111 1100	1.404	1010 0111	1.7695	1101 0010	2.135	1111 1101	2.5005
0010 0111	0.6815	0101 0010	1.047	0111 1101	1.4125	1010 1000	1.778	1101 0011	2.1435	1111 1110	2.509
0010 1000	0.69	0101 0011	1.0555	0111 1110	1.421	1010 1001	1.7865	1101 0100	2.152	1111 1111	2.5175
0010 1001	0.6985	0101 0100	1.064	0111 1111	1.4295	1010 1010	1.795	1101 0101	2.1605		
0010 1010	0.707	0101 0101	1.0725	1000 0000	1.438	1010 1011	1.8035	1101 0110	2.169		

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2023 MPS. All Rights Reserved.

6) Reg05 ID1

Register 05 is the IC information indicating register. The highest four bits, Vendor ID D[7:4], are set to 1000 internally.

The lowest four bits, IC Reversion ID D[3:0], indicates IC revision information.

NAME	BITS	DESCRIPTION
Vendor ID	D[7:4]	1000.
IC revision ID	D[3:0]	IC revision.

7) Reg06 Status

Register 06 is a fault condition-indicating register. The highest four bits, D[7:4], are reserved for future use.

The bit OC is the output over-current indication. When the bit is set to 1, the IC is in hiccup mode or OC latch-off.

The bit OTEW is the die temperature early warning indication. When the bit is set to 1, the IC die temperature is higher than 120°C.

The bit PG is output power good indication. When the bit is set to 1, the output power is normal.

NAME	BITS	DESCRIPTION
Reserved	D[7:4]	Reserved for future use.
OC	D[3]	Output over-current indication. When this bit is high, the IC is in hiccup mode or trips OC latch off.
OTEW	D[2]	Die temperature early warning bit. When the bit is high, the die temperature is higher than 120˚C.
OT	D[1]	Over temperature indication. When the bit is high the IC is in thermal shutdown
PG	D[0]	Output power good indication. When the bit is high the VOUT power is normal. This means VOUT is higher than 95% and lower than 115% of the designed regulation voltage. PG compares FB/VOUT with REF.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2023 MPS. All Rights Reserved.

NOT RECOMMENDED FOR NEW DESIGNS, REFER TO MMP8869S

APPLICATION INFORMATION

Setting the Output Voltage in a FB Control Loop

The MP8869W can be controlled by the FB loop or I²C loop. The FB loop is the default loop during power-up or EN on. In this case, the output voltage can be set by the external resistor dividers. The FB loop reference voltage is a fixed value (0.6V) and cannot be programmed by the I²C.

The FB loop network is shown in Figure 11.

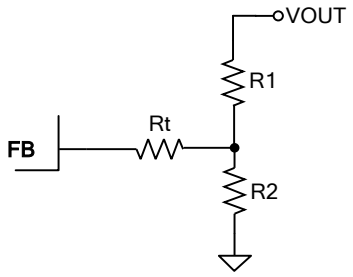


Figure 11: FB Loop Network

Choose R1 and R2 with Equation (4):

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.6V} - 1} \quad (4)$$

Table 6 lists the recommended feedback resistors value for common output voltages.

Table 6: Resistor Selection for Common Output Voltages (8)

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	Rt(kΩ)	L(μH)
1.0	80.6	120	10	1.5
1.2	80.6	80.6	10	1.5
1.5	80.6	53.6	10	1.5
1.8	80.6	40.2	10	1.5
2.5	80.6	25.5	10	2.2
3.3	80.6	17.8	10	2.2
5	80.6	11	10	3.3

NOTE:

6) The recommended parameters are based on a 12V input voltage and 22μFx4 output capacitor. Different input voltage and output capacitor values may affect the selection of R1 and R2. For other components' parameters, please refer to the Typical Application Circuits on page 34.

Setting the Output Voltage in an I²C control Loop

After the part powers up and EN turns on, the FB loop can be programmed to the I²C loop sensing (VOUT) by setting V_BOOT = 0. In this case, the output voltage can be set by the I²C from 0.6V to 1.55V. Please refer to Table 3 for more details about output voltage setting.

Output Voltage Dynamic Scale

The output voltage dynamic scaling can be done only in the I²C control loop. Refer to Figure 12 and follow the steps below.

1) Write GO_BIT (Reg01[6]) to 1.
2) Write Reg00 to select the feedback loop by setting V_BOOT (Reg00[7]) and setting the reference voltage by Output Reference (Reg00[6:0]) simultaneously. When the command is finished, GO_BIT auto-resets to 0 to prevent false operation of the VOUT scaling.

Repeat the above two steps if the output voltage needs to be changed to a different voltage.

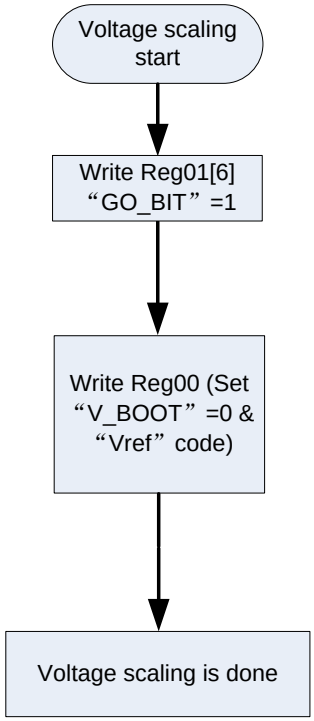


Figure 12: Loop Switch and Output Voltage Dynamic Scale Flow Chart

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2023 MPS. All Rights Reserved.

NOT RECOMMENDED FOR NEW DESIGNS, REFER TO MMP8869S

Selecting the Inductor

Use a 0.47µH-to-5µH inductor with a DC current rating at least 25% percent higher than the maximum load current for most applications. For highest efficiency, use an inductor with a DC resistance less than 5mΩ. For most designs, the inductance value can be derived from Equation (5):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \quad (5)$$

Where ΔIL is the inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current can be calculated with Equation (6):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (6)$$

Use a larger inductor for improved efficiency under light-load conditions below 100mA.

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are recommended because of their low ESR and small temperature coefficients. For most applications, use two 22µF capacitors.

Since C1 absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (7):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (7)$$

The worst-case condition occurs at VIN = 2VOUT, shown in Equation (8):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (8)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g.: 0.1µF) placed as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at input. The input voltage ripple caused by the capacitance can be estimated with Equation (9):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (9)$$

Selecting the Output Capacitor

The output capacitor (C2) maintains the DC output voltage. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For best results, use low ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right) \quad (10)$$

Where L_1 is the inductor value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes the majority of the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (11)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (12):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (12)$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MP8869W can be optimized for a wide range of capacitance and ESR values.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2023 MPS. All Rights Reserved.

NOT RECOMMENDED FOR NEW DESIGNS, REFER TO MMP8869S

External Bootstrap Diode

An external bootstrap diode can enhance the efficiency of the regulator given the following conditions:

- VOUT is 5V or 3.3V
- Duty cycle is high: D > 50%

In these cases, add an external BST diode from VCC to BST (see Figure 13).

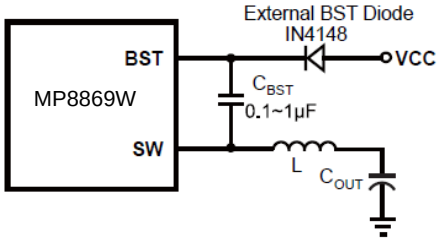


Figure 13: Optional External Bootstrap Diode to Enhance Efficiency

The recommended external BST diode is IN4148, and the recommended BST capacitor value is 0.1ST to 1cap

Connect VCC to VIN at a Low Input Voltage

VCC can be connected to VIN directly when VIN is lower than 3.5V. This helps improve the MP8869W's low input voltage efficiency performance. To use this application set-up, the VIN spike voltage must be limited below 4V, otherwise VCC may be damaged.

PCB Layout Guidelines [9]

Efficient PCB layout is critical for stable operation. For best results, refer to Figure 14 and follow the guidelines below. A four-layer layout is strongly recommended to achieve better thermal performance.

1. Place the high-current paths (PGND, VIN, and SW) very close to the device with short, direct, and wide traces.
2. Keep the VIN and PGND pads connected with large copper planes.
3. Use at least two layers for the IN and PGND trace to achieve better thermal performance.
4. Add several vias close to the IN and PGND pads to help with thermal dissipation. Place m than one via **adjacent to the inner edge of PGND pad** which connects to AGND pad through low impedance routing or ground plane.
5. Place the input capacitors as close to VIN and PGND as possible.
6. Place the decoupling capacitor as close to VCC and AGND as possible.
7. Add several vias close the the AGND pad, and connect to PGND plane with Kelvin connection.
8. Place the external feedback resistors next to FB.
9. Ensure that there is no via on the FB trace.
10. Keep the switching node SW short and away from the feedback network.
11. Keep the BST voltage path (BST, R3,C3, and SW) as short as possible.

NOTE:

9) The recommended layout is based on the Typical Application circuit on page 34.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2023 MPS. All Rights Reserved.

NOT RECOMMENDED FOR NEW DESIGNS, REFER TO MMP8869S

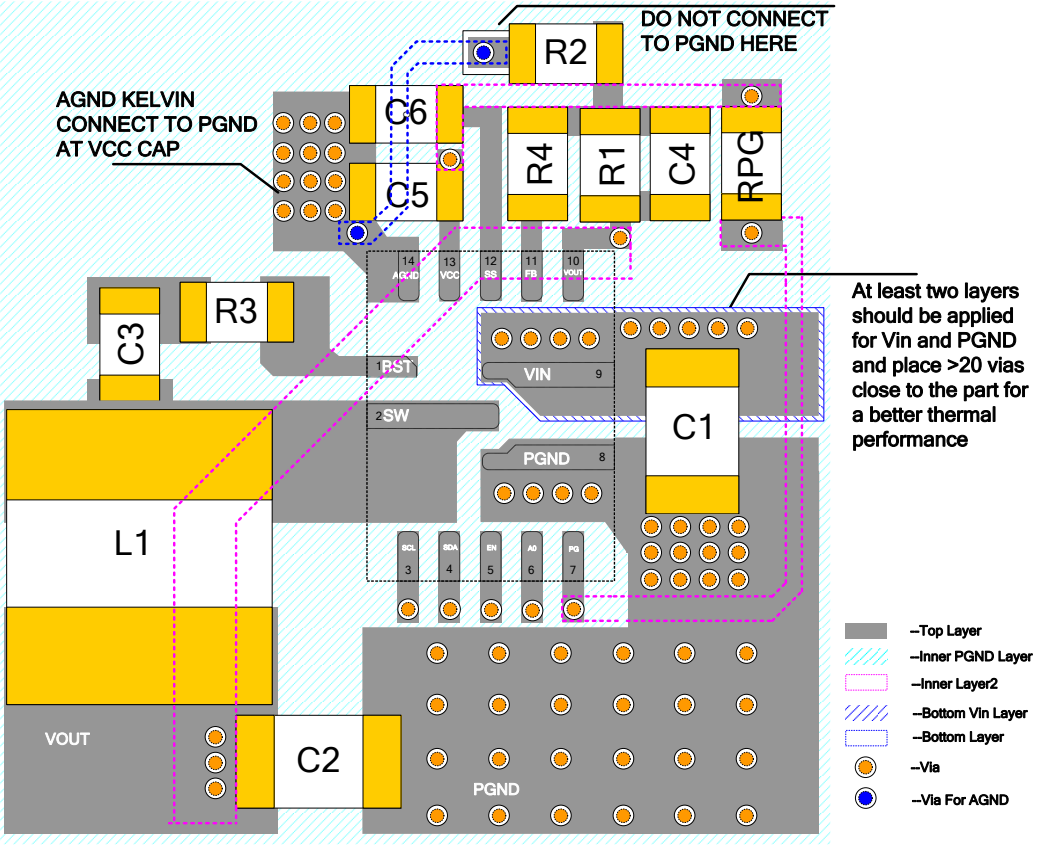


Figure 14: Recommend Layout

Design Example

Table 7 is a design example following the application guidelines for the specifications below.

Table 7: Design Example

V_{IN}	12V
V_{OUT}	1V
I_O	12A

The detailed application schematics are shown in Figure 15 through Figure 21. The typical performance and circuit waveforms are shown in the Typical Performance Characteristics section. For more device applications, please refer to the related evaluation board datasheets.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2023 MPS. All Rights Reserved.

NOT RECOMMENDED FOR NEW DESIGNS, REFER TO MMP8869S

TYPICAL APPLICATION CIRCUITS (10)

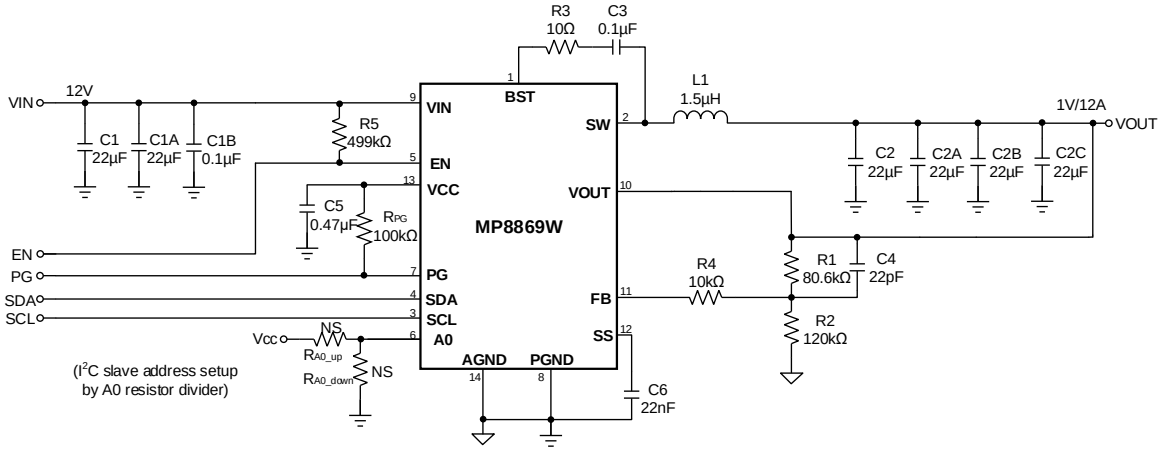


Figure 15: V_{IN} = 12V, V_{OUT} = 1V, I_{OUT} = 12A

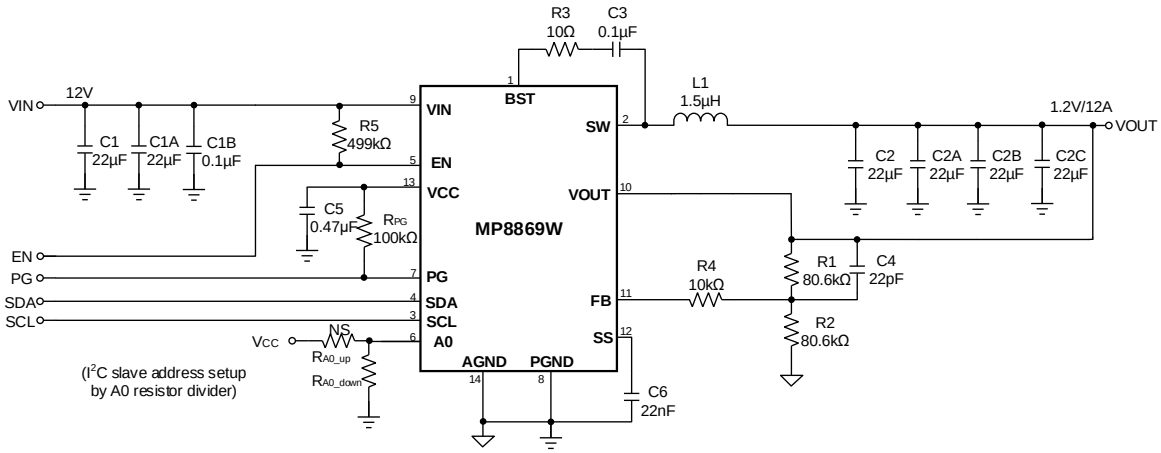


Figure 16: V_{IN} = 12V, V_{OUT} = 1.2V, I_{OUT} = 12A

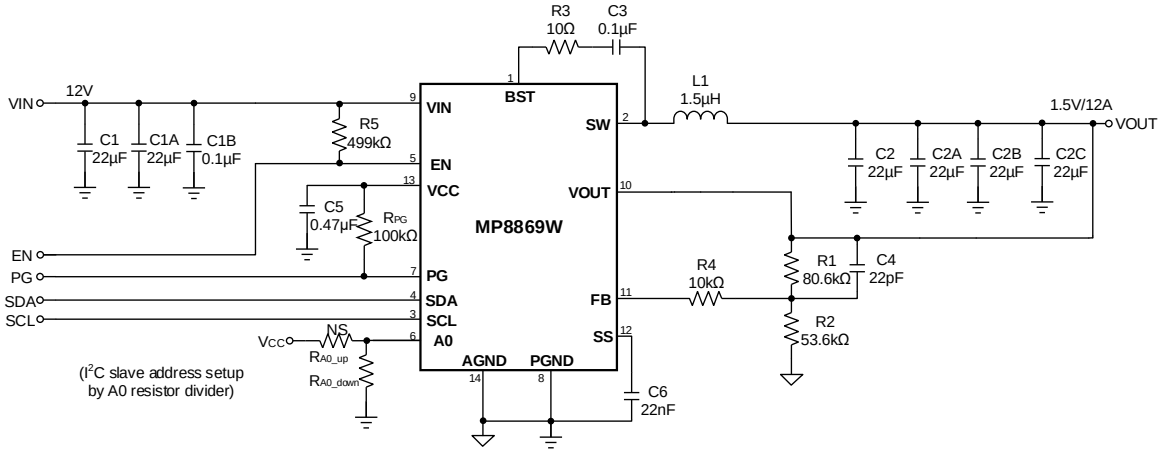


Figure 17: V_{IN} = 12V, V_{OUT} = 1.5V, I_{OUT} = 12A

NOTE:
10) All circuits are based on a 0.6V default reference voltage.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2023 MPS. All Rights Reserved.

NOT RECOMMENDED FOR NEW DESIGNS, REFER TO MMP8869S

TYPICAL APPLICATION CIRCUITS *(continued)*

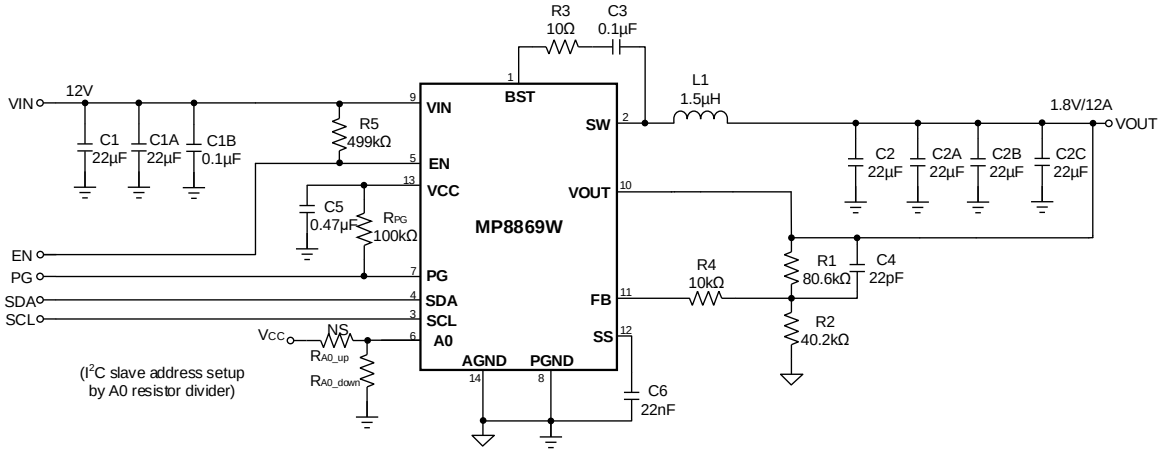


Figure 18: V_{IN} = 12V, V_{OUT} = 1.8V, I_{OUT} = 12A

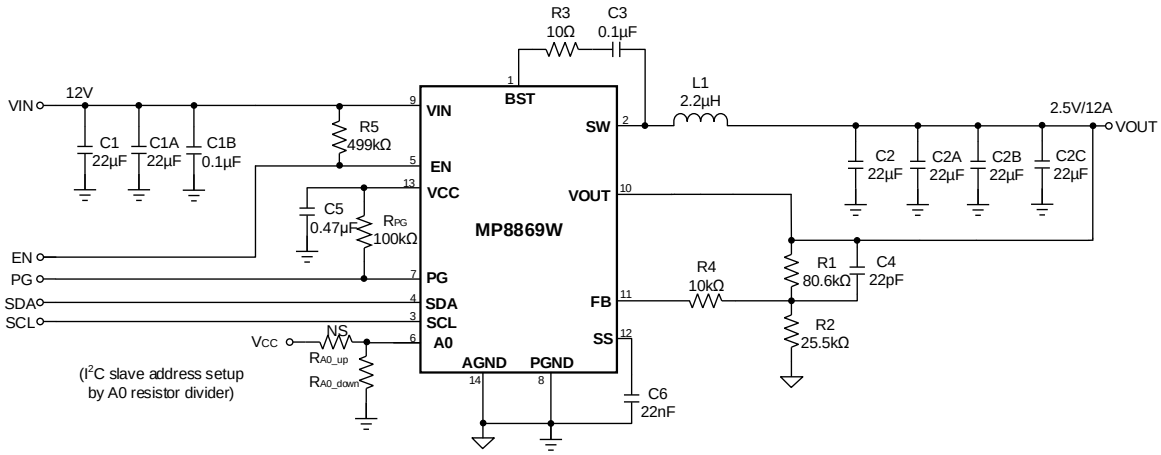


Figure 19: V_{IN} = 12V, V_{OUT} = 2.5V, I_{OUT} = 12A

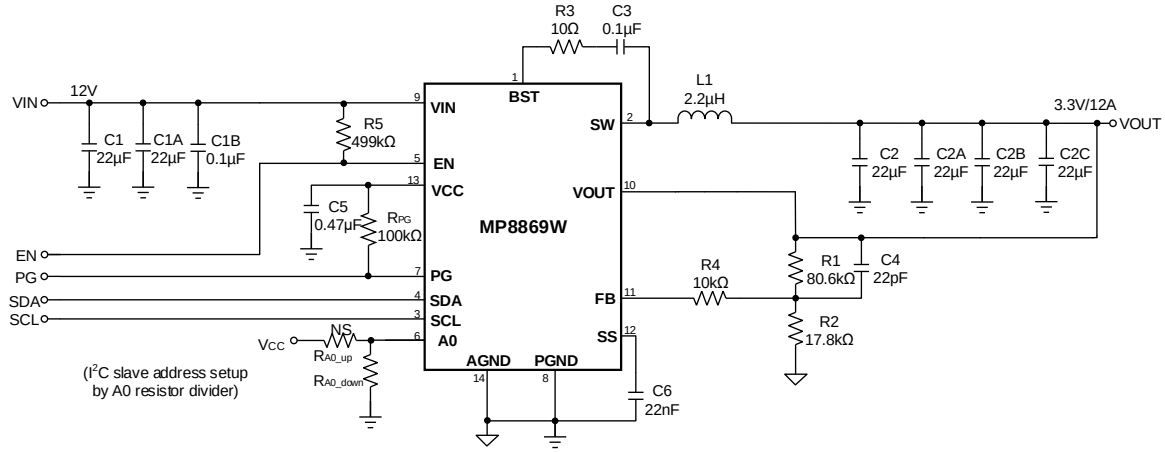


Figure 20: V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 12A

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2023 MPS. All Rights Reserved.

NOT RECOMMENDED FOR NEW DESIGNS, REFER TO MMP8869S

TYPICAL APPLICATION CIRCUITS *(continued)*

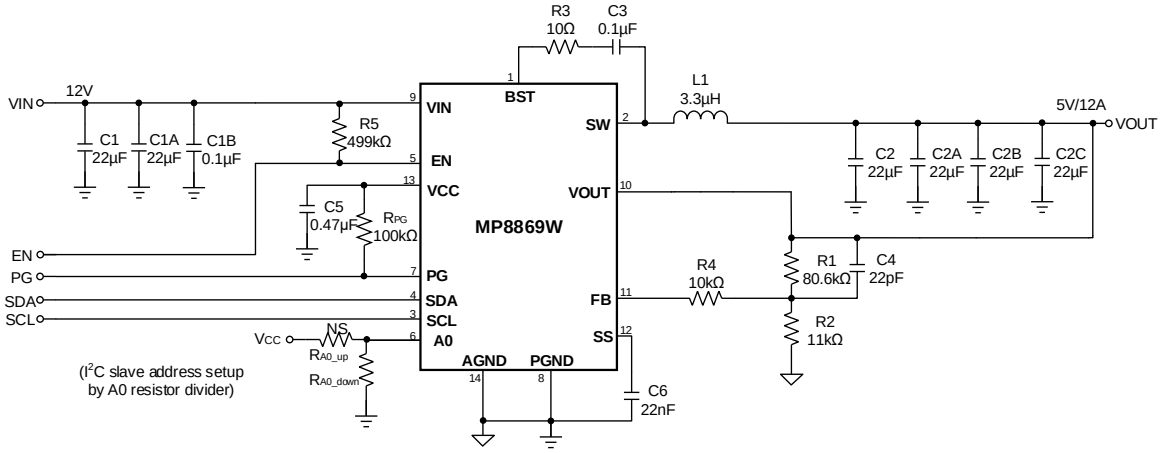


Figure 21: V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 12A(11)

NOTE:

11) Based on evaluation board test results at 25°C ambient temperature. A lower input voltage will trigger over-temperature protection with full load.

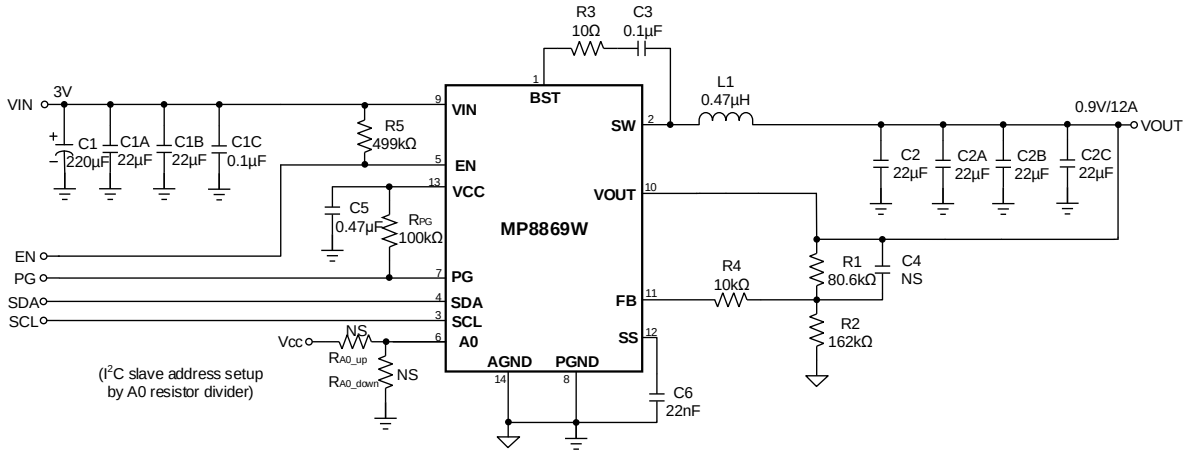


Figure 22: V_{IN} = 3V, V_{OUT} = 0.9V, I_{OUT} = 12A

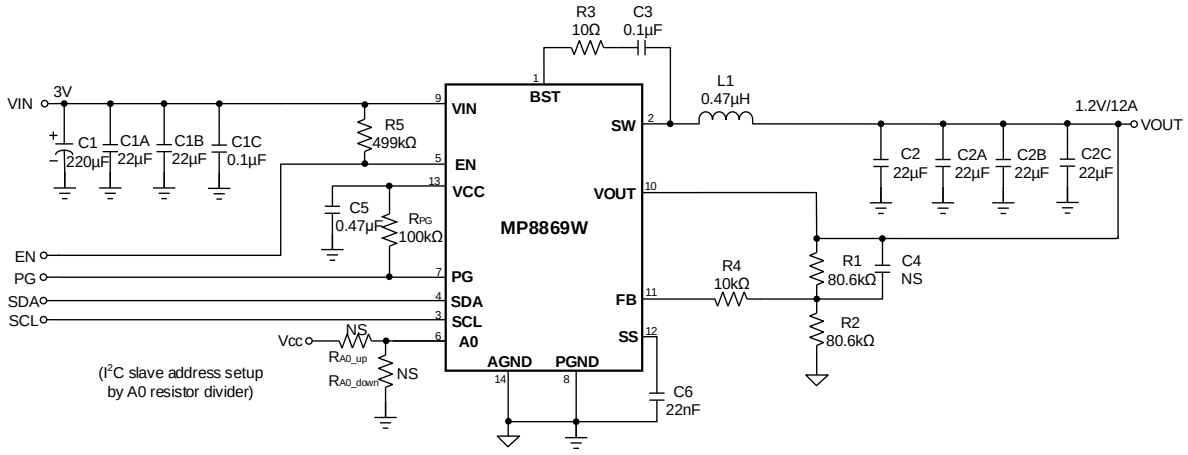


Figure 23: V_{IN} = 3V, V_{OUT} = 1.2V, I_{OUT} = 12A

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2023 MPS. All Rights Reserved.

NOT RECOMMENDED FOR NEW DESIGNS, REFER TO MMP8869S

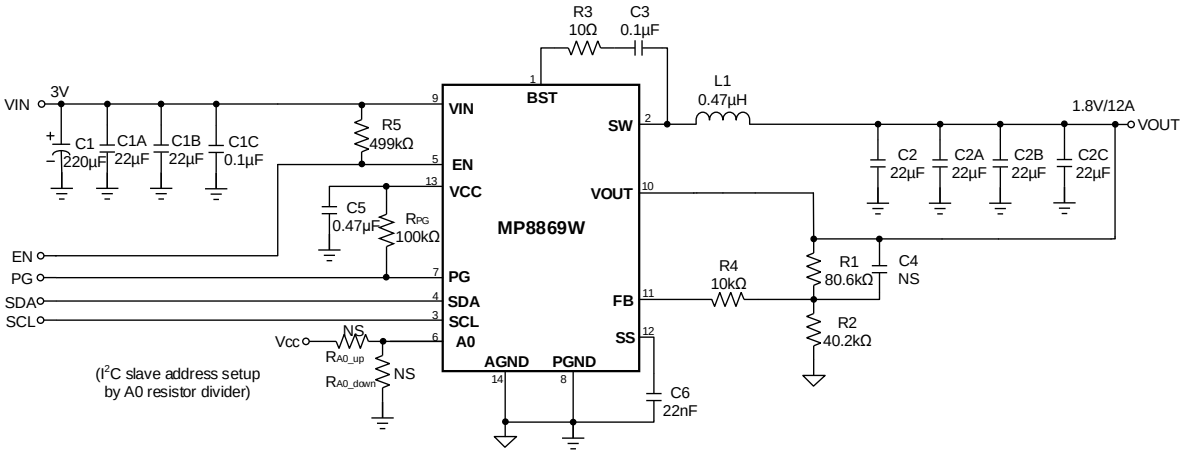


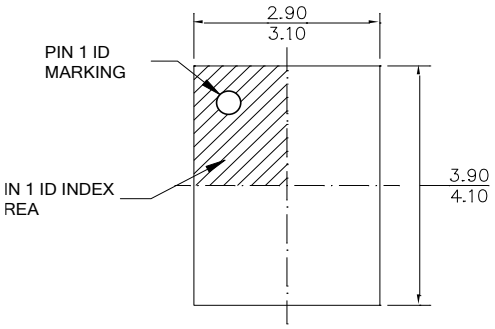
Figure 24: V_{IN} = 3V, V_{OUT} = 1.8V, I_{OUT} = 12A

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2023 MPS. All Rights Reserved.

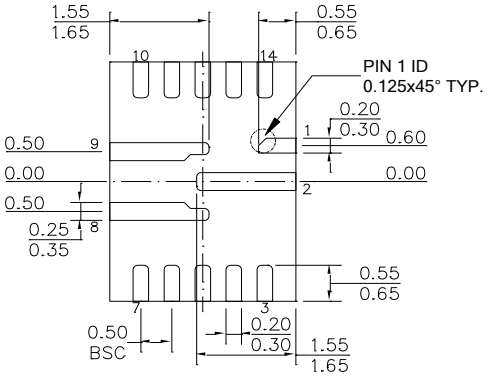
NOT RECOMMENDED FOR NEW DESIGNS, REFER TO MMP8869S

PACKAGE INFORMATION

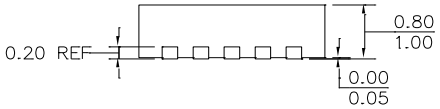
QFN-14 (3mmx4mm)



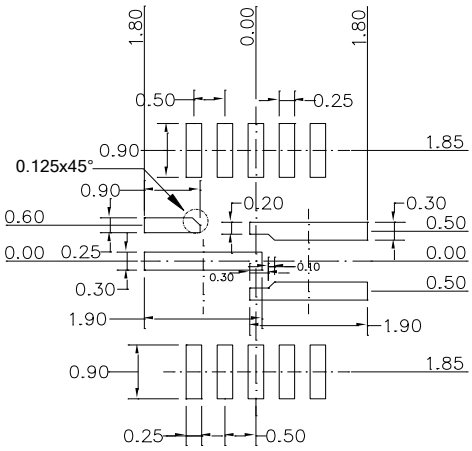
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMET MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2023 MPS. All Rights Reserved.

Revision History

Revision #	Revision Date	Description	Pages Updated
1.1	5/26/2020	Update typical application circuit and PCB layout guide line	1,35,37,38.39,40

NOTICE: The information in this document is subject to change without notice. Please contact MPS for current specifications. Users should warrant and guarantee that third party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2023 MPS. All Rights Reserved.