NB621

8A, 25V, 600kHz Synchronous Step-Down Converter with Integrated LDO

The Future of Analog IC Technology®

END OF LIFE, REFER TO NB700 OR NB693A

DESCRIPTION

The NB621 is a high frequency synchronous rectified step-down switch mode converter with a built in internal high side power MOSFET and integrated LDO. It offers a very compact solution to achieve 8A continuous output current over a wide input, load and line range.

Current mode operation provides fast transient response and eases loop stabilization.

Full protection features include OCP and thermal shut down.

The NB621 requires a minimum number of readily available standard external components and is available in a space saving 4mm x 5mm 28-pin QFN package.

FEATURES

- Wide 5.5V to 25V Operating Input Range
- 8A Output Current
- Internal Low R_{DSON} Power MOSFETs
- Fixed 600kHz switching frequency
- Sync from 300kHz to 2MHz External Clock
- Integrated 100mA LDO
- Internal Compensation
- Power Good Output
- Integrated Bootstrap Diode
- OCP Protection and Thermal Shutdown
- Output Adjustable from 0.8V to 15V
- Available in 4mm x 5mm 28-pin QFN package.

APPLICATIONS

- Notebook Systems and I/O Power
- Networking Systems
- Digital Set Top Boxes
- Personal Video Recorders
- Flat Panel Television and Monitors
- Distributed Power Systems

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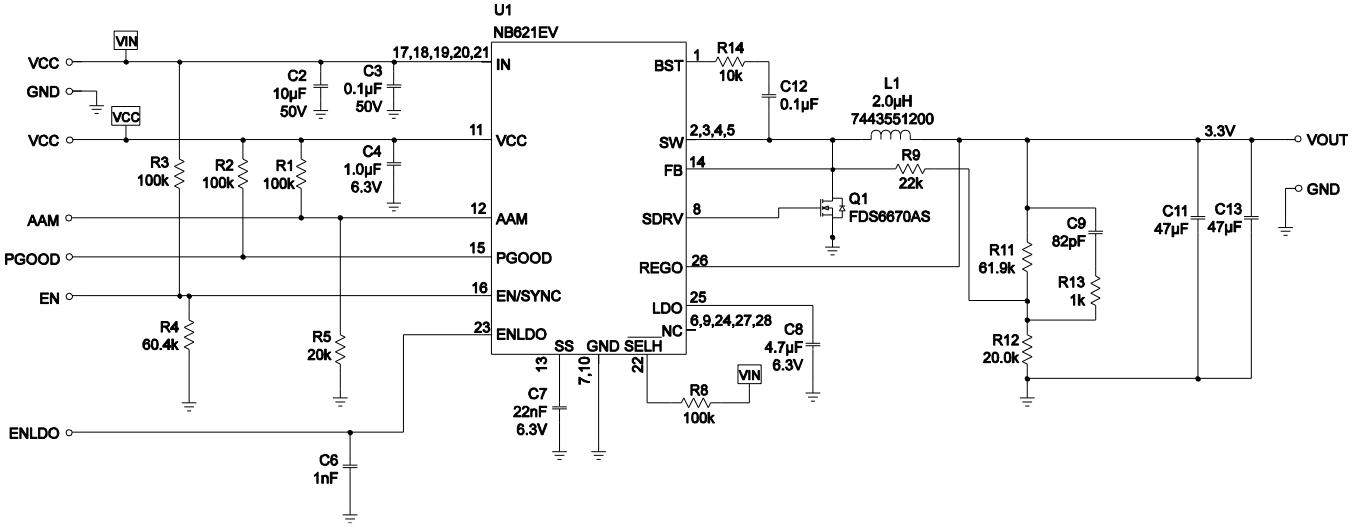
TYPICAL APPLICATION (FOR NOTEBOOK)



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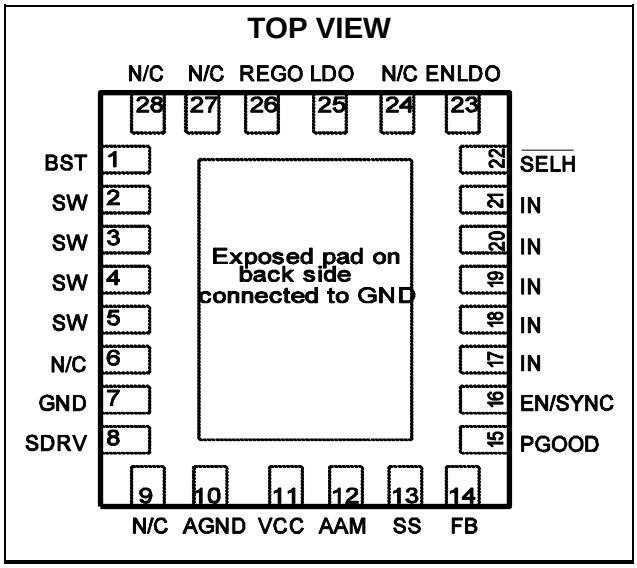
END OF LIFE, REFER TO NB700 OR NB693A

ORDERING INFORMATION

Part Number*	Package	Top Marking	Free Air Temperature (T_A)
NB621EV	QFN28 (4mmx5mm)	N621EV	–20°C to +85°C

***** For Tape & Reel, add suffix –Z (e.g. NB621EV–Z);
For RoHS compliant packaging, add suffix –LF (e.g. NB621EV–LF–Z).

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage V_{IN} 28V
V_{SW} .....–0.3V to V_{IN} + 0.3V
V_{BS} .....V_{SW} + 6V
$I_{VIN(RMS)}$ 3A
$I_{SW(RMS)}$ 3A
All Other Pins..... –0.3V to +6V
Continuous Power Dissipation (T_A=+25°C) (2)
.....3.1W
Junction Temperature..... 150°C
Lead Temperature ..... 260°C
Storage Temperature..... –65°C to +150°C

Recommended Operating Conditions (3)

Supply Voltage V_{IN} ..... 5.5V to 25V
Output Voltage V_{OUT}..... 0.8V to 15V
Operating Junct. Temp (T_J)..... –20°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

4x5 QFN28.....40.....9 °C/W

Notes:
1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D(MAX)=(T_J(MAX)-T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_A = +25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Current (Shutdown)	I_{IN}	V_{ENLDO} = 0V		30	TBD	μA
Supply Current (Quiescent)	I_{IN}	V_{EN} = 2V, V_{FB} = 1V		1.3	TBD	mA
High Side Switch On Resistance(5)	HSW_{RDS-ON}			50		mΩ
Switch Leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 0V		0	10	μA
Current Limit (5)	I_{LIMIT}		9.5			A
Oscillator Frequency	F_{SW}	V_{FB} = 0.75V		600		kHz
Fold-back Frequency	F_{FB}	V_{FB} = 100mV		0.25		f_{SW}
Maximum Duty Cycle	D_{MAX}	V_{FB} = 700mV	85	90		%
Sync Frequency Range	F_{SYNC}		0.3		2	MHz
Feedback Voltage	V_{FB}		788	808	828	mV
Feedback Current	I_{FB}	V_{FB} = 800mV		10	50	nA
Soft Start Charging Current	I_{SS}	V_{SS}=0V		10		μA
EN/SYNC Input Low Voltage	VIL_{EN}				0.4	V
EN/SYNC Input High Voltage	VIH_{EN}		2			V
EN Input Current	I_{EN}	V_{EN} = 2V		2		μA
		V_{EN} = 0V		0		
EN Turn Off Delay	EN_{Td-Off}			5		μsec
Power Good Threshold Rising	PG_{Vth-Hi}			0.9		V_{FB}
Power Good Threshold Falling	PG_{Vth-Lo}			0.7		V_{FB}
Power Good Delay (5)	PG_{Td}			0.42		Tss(6)
Power Good Sink Current Capability	V_{PG}	Sink 4mA			0.4	V
Power Good Leakage Current	I_{PG_LEAK}	V_{PG} = 3.3V			10	nA
VIN Under Voltage Lockout Threshold Rising	$INUV_{Vth}$	V_{ENLDO}=open		5.06		V
VIN Under Voltage Lockout Threshold Hysteresis	$INUV_{HYS}$	V_{ENLDO}=open		450		mV
VCC Under Voltage Lockout Threshold Rising	$VCCUV_{Vth}$	V_{ENLDO}=open	3.8	4.0	4.2	V
VCC Under Voltage Lockout Threshold Hysteresis	$VCCUV_{HYS}$	V_{ENLDO}=open		880		mV
VCC Regulator	V_{CC}		4.5	5		V
VCC Load Regulation		I_{CC}=20mA		5		%

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_A = +25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
LDD Switch On Resistance(5)	R_{LDO}	V_{LDO}=5V, I_{LDO}=100mA		5		Ω
LDO Output Voltage	V_{LDO}	SELH=0V, I_{LDO}<100mA	4.8	5	5.2	V
		SELH=0V, I_{LDO}<100mA, 6.5V<V_{IN}<25V	4.75	5	5.25	V
		V_{LDO}=0V, I_{LDO}<50mA, 5.5V<V_{IN}<25V	4.75	5	5.25	V
		SELH=5V, I_{LDO}<100mA	3.2	3.33	3.46	V
		SELH=5V, I_{LDO}<100mA, 6.5V<V_{IN}<25V	3.13	3.33	3.5	V
		SELH=5V, I_{LDO}<50mA, 5.5V<V_{IN}<25V	3.13	3.33	3.5	V
LDO Output Current	I_{LDO}	SELH=0V	100			mA
		SELH=5V	100			mA
Switch Over Threshold (Rising)	V_{SWO}	SELH=0V	4.55	4.7	4.85	V
		SELH=5V	3.05	3.15	3.25	V
Switch Over Hysteresis	$V_{SWO-HYS}$	SELH=0V	0.15	0.25	0.3	V
		SELH=5V	0.1	0.2	0.25	V
SELH Input Low Voltage	VIL_{SELH}				0.4	V
SELH Input High Voltage	VIH_{SELH}		2.5			V
ENLDO Input Low Voltage VIL_{ENLDO}					0.4	V
ENLDO Input High Voltage VIH_{ENLDO}			2			V
Thermal Shutdown	T_{SD}			150		°C

Note:

5) Guaranteed by design.

6) TSS—Soft startup time

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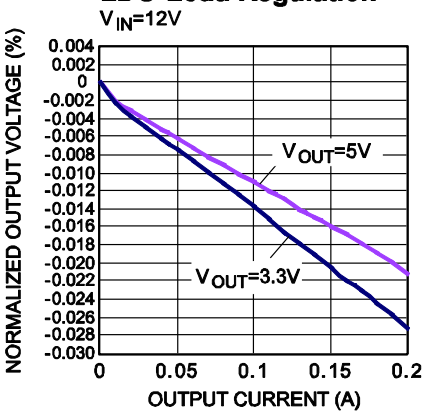
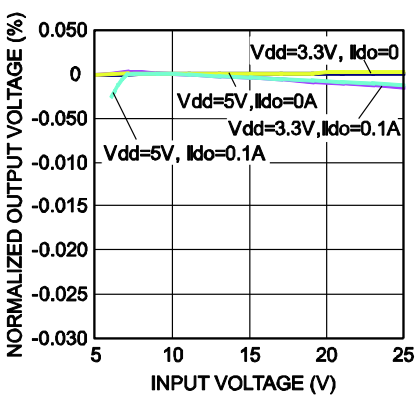
TYPICAL PERFORMANCE CHARACTERISTICS

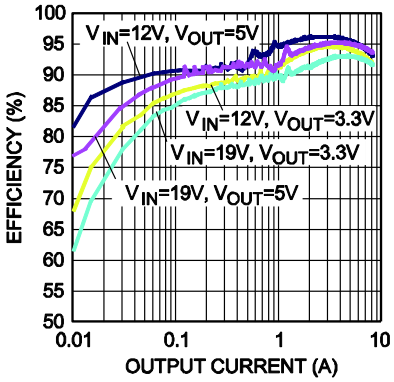
LDO-Load Regulation



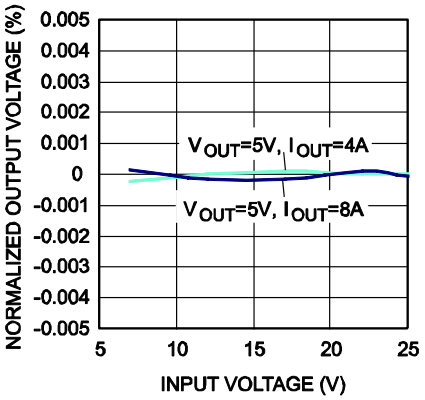
LDO- Line Regulation



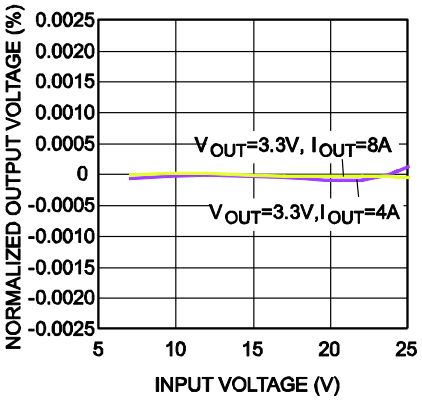
System Efficiency



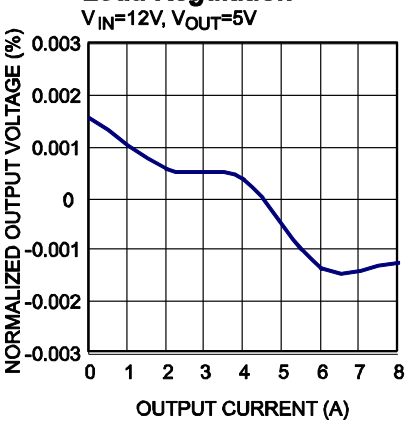
Line Regulation



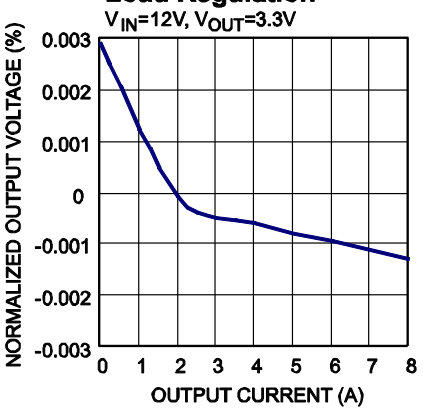
Line Regulation



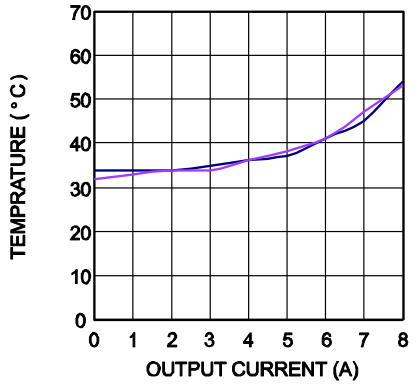
Load Regulation



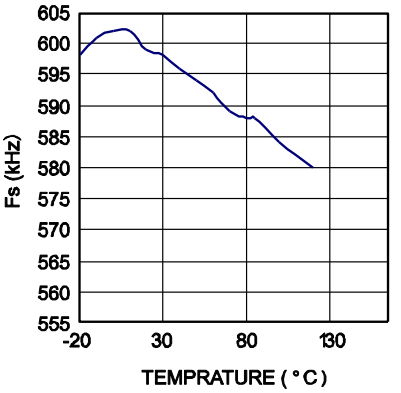
Load Regulation



Thermal Test



Frequency vs. Temperature



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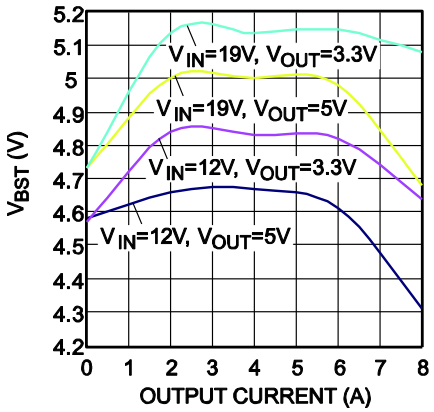
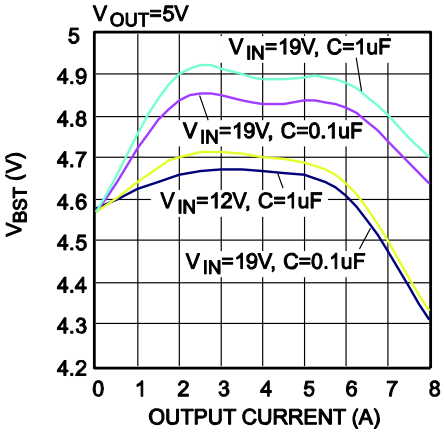
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

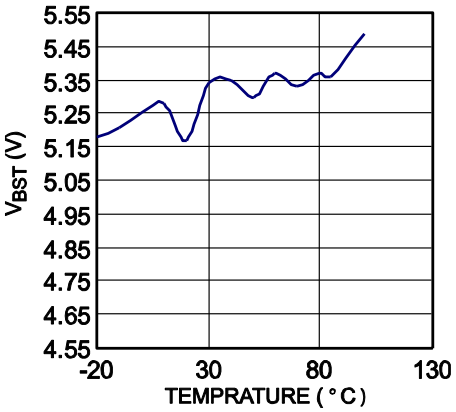
V_{BST} vs. I_{OUT} for V_{IN}=12V & 19V



V_{BST} vs. I_{OUT} for 0.1uF & 1uF



V_{BST} vs. Temperature



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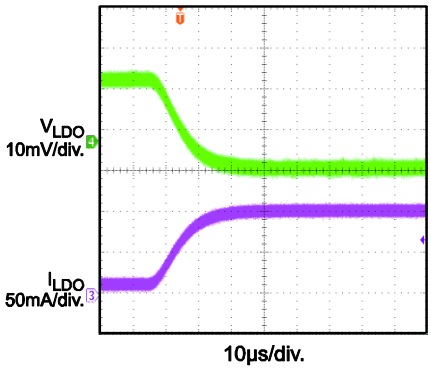
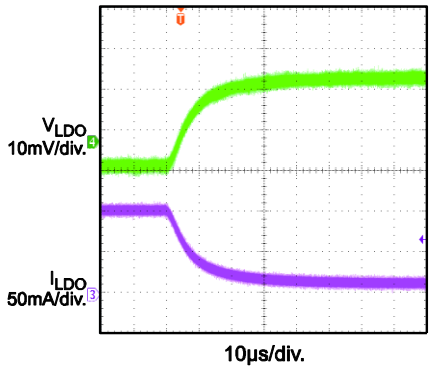
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

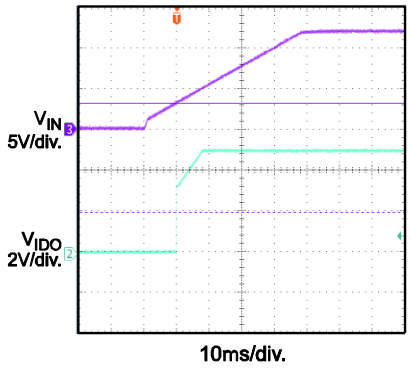
LDO-Transient Response
V_{IN} = 12V, EN = GND, V_{IDO}= 5V,
I_{IDO} = 10mA @ 250mA/µs



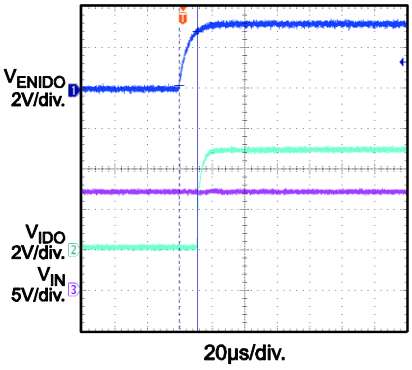
LDO-Transient Response
V_{IN} = 12V, EN = GND, V_{IDO} = 5V,
I_{IDO} = 100mA @ 250mA/µs



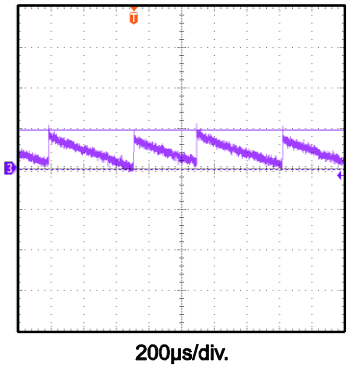
LDO Startup
V_{IN} = 12V, $V_{OUT.IDO}$ = 5V



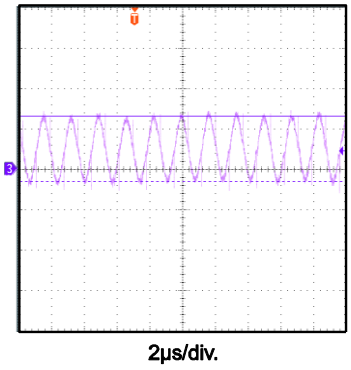
LDO-EN Startup
V_{IN} = 12V,V_{IDO} = 5V, I_{IDO} = 0.1A



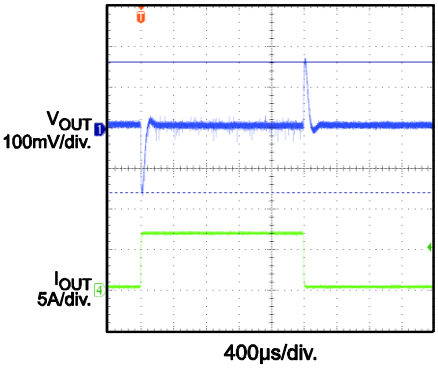
Switcher Output Voltage Ripple – No Current Load
V_{IN} = 12V, V_O= 5V, I_O = 0V
AAM Voltage=0.65V



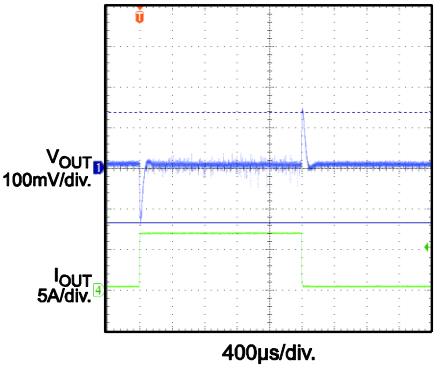
Switcher Output Voltage Ripple –Full Current Load
V_{IN} = 12V, V_O = 5V, I_O = 8A
AAM Voltage=0.65V



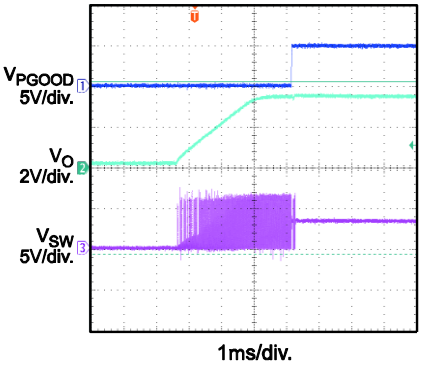
Transient Response
V_{IN} = 12V, V_O = 5V,
I_O from 0.5A to 7A @2.5A/µs
Add 330µF Poscon cap to Cout.



Transient Response
V_{IN} = 12V, V_O = 3.3V,
I_O from 0.5A to 7A @2.5A/µs
Add 330µF Poscon cap.



Power Startup – No Load
V_{IN} = 12V, V_O = 3.3V, I_O = 0A



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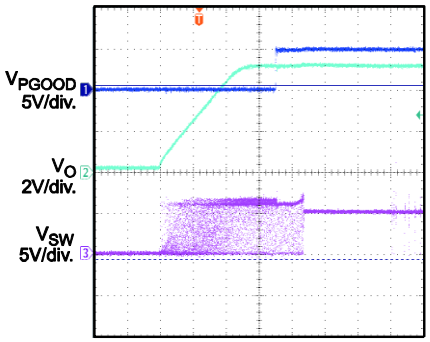
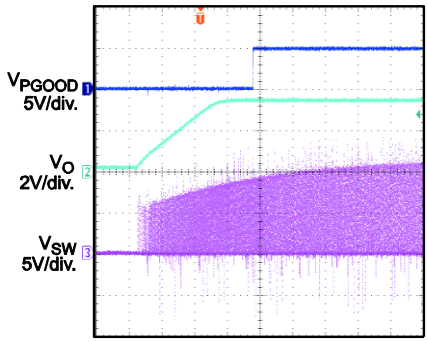
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

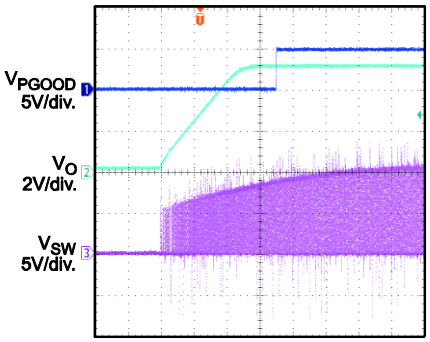
Power Startup – No Load
V_{IN} = 12V, V_O = 5V, I_O = 0A



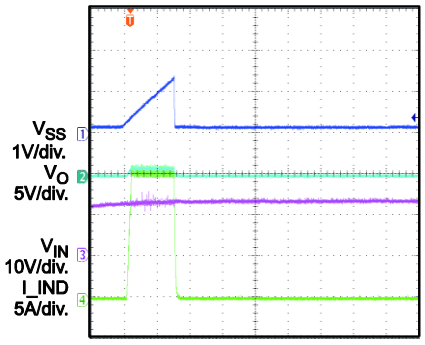
Power Startup – Full Load
V_{IN} = 12V, V_O = 3.3V, I_O = 8A



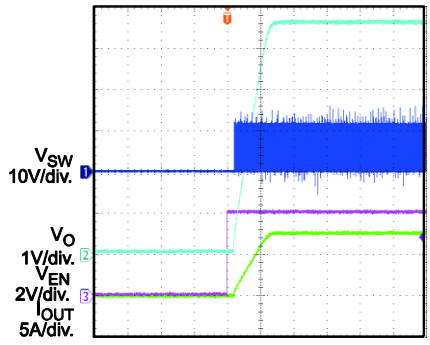
Power Startup – Full Load
V_{IN} = 12V, V_O = 5V, I_O = 8A



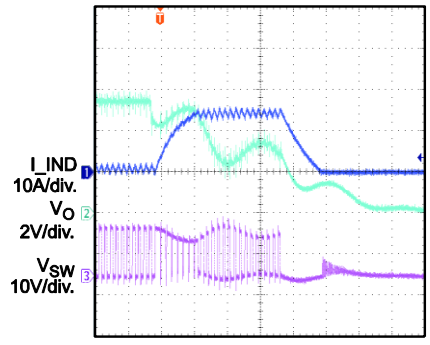
Power On with Shorted Vout
V_{IN} = 12V, V_O = 5V, I_O = 8A



EN Startup with Io=7A
V_{IN} = 12V, V_O = 5V



SCP Entry
V_{IN} = 12V, V_O = 5V, R_L = 7Ω



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PIN FUNCTIONS

Pin #	Name	Description
1	BST	Bootstrap. A capacitor connected between SW and BS pins is required to form a floating supply across the high-side switch driver.
2, 3, 4, 5	SW	Switch Output. Use wide PCB traces and multiple vias to make the connection.
6, 9, 24, 27, 28	N/C	No Connection.
7	GND	System Ground. This pin is the reference ground of the regulated output voltage. For this reason care must be taken in PCB layout.
8	SDRV	Low Side Gate Driver Output.
10	AGND	Analog Ground.
11	VCC	Bias Supply. Decouple with 1µF capacitor.
12	AAM	Connect to GND forces NB621 in synchronous mode. Connects to a voltage set by 2 resistor dividers forces NB621 into non-synchronous mode when load is small.
13	SS	Soft Start. Connect on external capacitor to program the soft start time for the switch mode regulator.
14	FB	Feedback. An external resistor divider from the output to GND, tapped to the FB pin, sets the output voltage. To prevent current limit run away during a short circuit fault condition the frequency fold-back comparator lowers the oscillator frequency when the FB voltage is below 400mV.
15	PG	Power good output, the output of this pin is an open drain and is high if the output voltage is higher than 90% of the nominal voltage. There is a 20µs delay to pull PG if the output voltage is lower than 10% of regulation value.
16	EN/SYNC	EN=1 to enable the NB621. External clock can be applied to EN pin for changing switching frequency. For automatic start-up, connect EN pin to VIN with 100KΩ resistor.
17,18,19,20,21	IN	Supply Voltage. The NB621 operates from a +4.5V to +25V input rail. C1 is needed to decouple the input rail. Use wide PCB traces and multiple vias to make the connection.
22	SELH	Internal LDO output voltage selection. When grounded, the LDO output will be regulated to 5V. When pulled high, the LDO output will be regulated to 3.3V.
23	ENLDO	Internal LDO regulator enable pin
25	LDO	Internal LDO regulator Output. Connect a 10uF decoupling capacitor to GND.
26	REGO	Switch Mode Regulator Output connection pin. This pin is used to switch the internal LDO output to the switch mode regulator output when it is available.

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BLOCK DIAGRAM

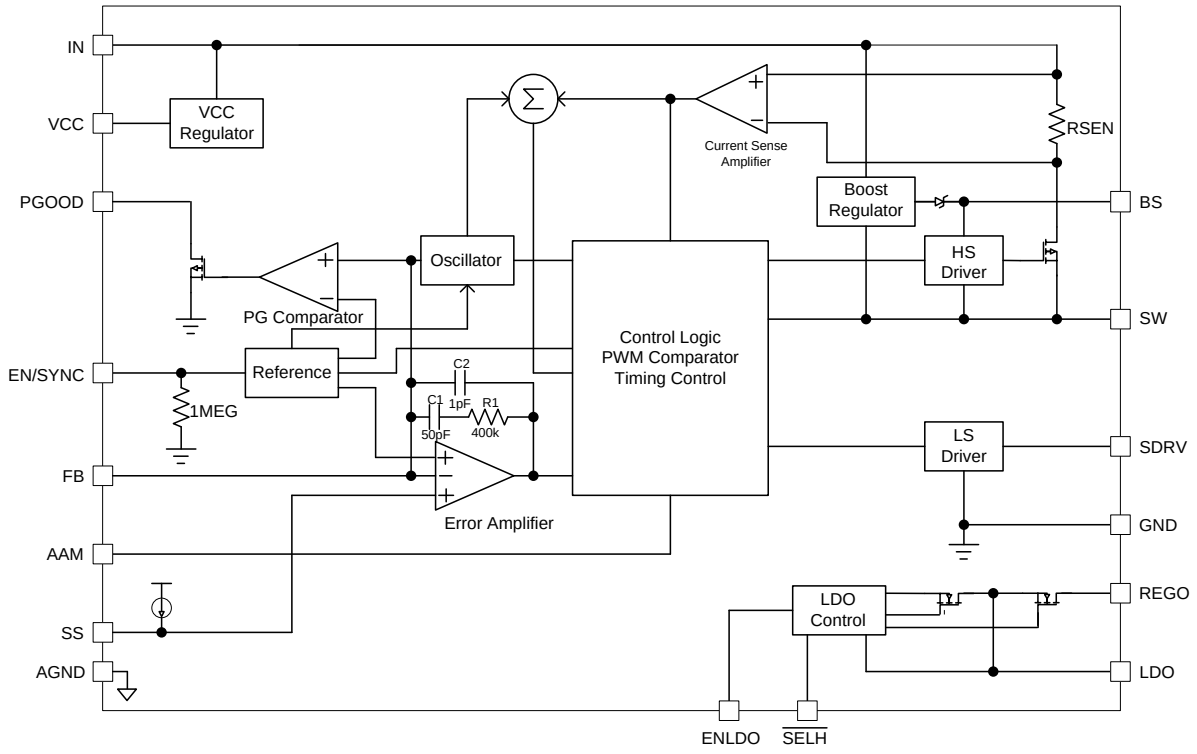

Figure 1—Function Block Diagram

OPERATION

The NB621 is a high frequency synchronous rectified step-down switch mode converter with a built in internal high side power MOSFET. It offers a very compact solution to achieve 8A continuous output current over a wide input supply range with excellent load and line regulation.

The NB621 operates in a fixed frequency, peak current control mode to regulate the output voltage. A PWM cycle is initiated by the internal clock. The integrated high-side power MOSFET is turned on and remains on until its current reaches the value set by the COMP voltage. When the power switch is off, it remains off until the next clock cycle starts. If, in 90% of one PWM period, the current in the power MOSFET does not reach the COMP set current value, the power MOSFET will be forced to turn off.

Error Amplifier

The error amplifier compares the FB pin voltage with the internal 0.8V reference (REF) and outputs a current proportional to the difference between the two. This output current is then used to charge or discharge the internal compensation network to form the COMP voltage, which is used to control the power MOSFET current. The optimized internal compensation network minimizes the external component counts and simplifies the control loop design.

Internal Regulator

Most of the internal circuitries are powered from the 5V internal regulator. This regulator takes the VIN input and operates in the full VIN range. When VIN is greater than 5.0V, the output of the

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regulator is in full regulation. When VIN is lower than 5.0 V, the output of the regulator decreases. Since this internal regulator provides the bias current for the bottom gate driver that requires significant amount of current depending upon the external MOSFET selection, a 1 µF ceramic capacitor for decoupling purpose is required.

Enable/Sync Control

The NB621 has a dedicated Enable/Sync control pin (EN/SYNC). By pulling it high or low, the IC can be enabled and disabled by EN. Tie EN to VIN for automatic start up. To disable the part, EN must be pulled low for at least 5µs.

The NB621 can be synchronized to external clock range from 300 kHz up to 2 MHz through the EN/SYNC pin. The internal clock rising edge is synchronized to the external clock rising edge.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) is implemented to protect the chip from operating at insufficient supply voltage. The NB621 UVLO comparator monitors the output voltage of the internal regulator, VCC. The UVLO rising threshold is about 4.0 V while its falling threshold is a consistent 3.2 V.

Soft-Start

The soft-start is implemented to prevent the converter output voltage from overshooting during startup. When the chip starts, the internal circuitry generates a soft-start voltage (SS) ramping up from 0 V to 1.2 V. When it is lower than the internal reference (REF), SS overrides REF so the error amplifier uses SS as the reference. When SS is higher than REF, REF regains control. The soft start time (T_{ss}) can be calculated by:

$$T_{ss} = \frac{1.2 \cdot C_{ss}}{10 \cdot 10^{-6}}$$

Over-Current-Protection and Hiccup

The NB621 has cycle-by-cycle over current limit when the inductor current peak value exceeds the set current limit threshold. Meanwhile, output voltage starts to drop until FB is below the Under-Voltage (UV) threshold, typically 30% below the reference. Once a UV is triggered, the NB621 enters hiccup mode to periodically restart the part. This protection mode is especially useful when the output is dead-short to ground. The average short circuit current is greatly reduced to alleviate the thermal issue and to protect the regulator. The NB621 exits the hiccup mode once the over current condition is removed.

Thermal Shutdown

Thermal shutdown is implemented to prevent the chip from operating at exceedingly high temperatures. When the silicon die temperature is higher than 150°C, it shuts down the whole chip. When the temperature is lower than its lower threshold, typically 140°C, the chip is enabled again.

Floating Driver and Bootstrap Charging

The floating power MOSFET driver is powered by an external bootstrap capacitor. This floating driver has its own UVLO protection. This UVLO's rising threshold is 2.2 V with a hysteresis of 150mV. The bootstrap capacitor voltage is regulated internally by VIN through D1, M3, C4, L1 and C2 (Figure 2). If (VIN-VSW) is more than 5 V, U2 will regulate M3 to maintain a 5V BST voltage across C4.

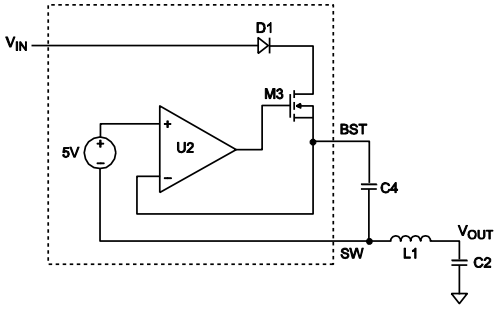

Figure 2—Internal Bootstrap Charging Circuit

Startup and Shutdown

If both VIN and EN are higher than their appropriate thresholds, the chip starts. The reference block starts first, generating stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides stable supply for the remaining circuitries.

Three events can shut down the chip: EN low, VIN low and thermal shutdown. In the shutdown procedure, the signaling path is first blocked to avoid any fault triggering. The COMP voltage and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

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APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider is used to set the output voltage (see the schematic on front page). The feedback resistor R1 also sets the feedback loop bandwidth with the internal compensation capacitor (see Figure 1). Choose R1 to be around 31.6kΩ for optimal transient response. R2 is then given by:

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.8V} - 1}$$

Table 1—Resistor Selection for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)
1.8	31.6 (1%)	25.5 (1%)
2.5	31.6 (1%)	14.7(1%)
3.3	31.6 (1%)	10(1%)
5	31.6 (1%)	6.04 (1%)

Selecting the Inductor

A 1µH to 10µH inductor with a DC current rating of at least 25% percent higher than the maximum load current is recommended for most applications. For highest efficiency, the inductor DC resistance should be less than 15mΩ. For most designs, the inductance value can be derived from the following equation.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}}$$

Where ΔI_L is the inductor ripple current.

Choose inductor current to be approximately 30% if the maximum load current, 8A. The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Under light load conditions below 100mA, larger inductance is recommended for improved efficiency.

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous, therefore a capacitor is required to supply the AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 22µF capacitor is sufficient.

Since the input capacitor (C1) absorbs the input switching current it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated by:

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The worse case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$I_{C1} = \frac{I_{LOAD}}{2}$$

For simplification, choose the input capacitor whose RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum or ceramic. When using electrolytic or tantalum capacitors, a small, high quality ceramic capacitor, i.e. 0.1µF, should be placed as close to the IC as possible. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at input. The input voltage ripple caused by capacitance can be estimated by:

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

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Selecting the Output Capacitor

The output capacitor (C2) is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right)$$

Where L is the inductor value and RESR is the equivalent series resistance (ESR) value of the output capacitor.

In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The NB621 can be optimized for a wide range of capacitance and ESR values.

PC Board Layout

The high current paths (GND, IN and SW) should be placed very close to the device with short, direct and wide traces. The input capacitor needs to be as close as possible to the IN and GND pins. The external feedback resistors should be placed next to the FB pin. Keep the switching node SW short and away from the feedback network.

External Bootstrap Diode

An external bootstrap diode may enhance the efficiency of the regulator, the applicable conditions of external BST diode are:

- V_{OUT} is 5V or 3.3V; and
- Duty cycle is high: $D = \frac{V_{OUT}}{V_{IN}} > 65\%$

In these cases, an external BST diode is recommended from the output of the voltage regulator to BST pin, as shown in Figure 3.

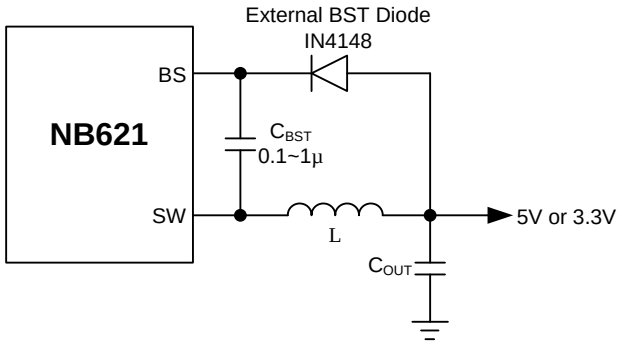

Figure 3—Add Optional External Bootstrap Diode to Enhance Efficiency

The recommended external BST diode is IN4148, and the BST cap is 0.1~1μF.

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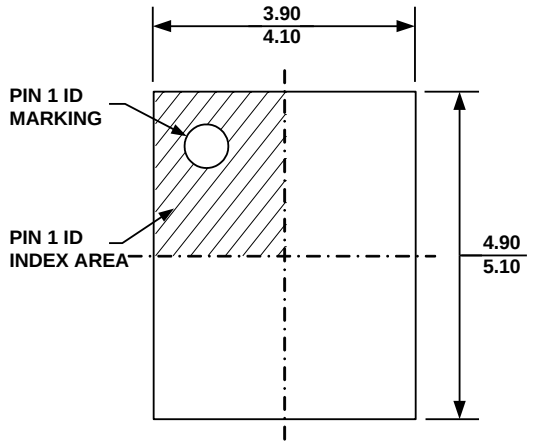
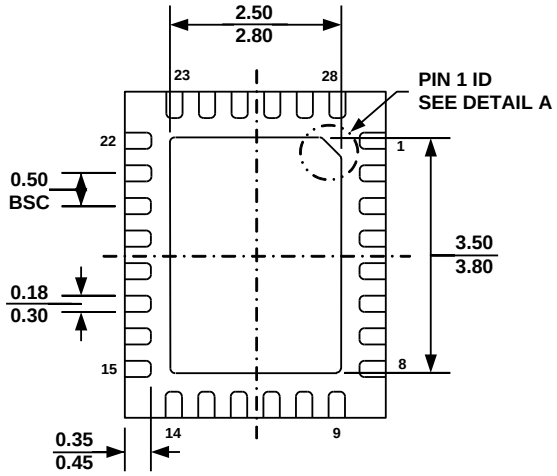
PACKAGE INFORMATION

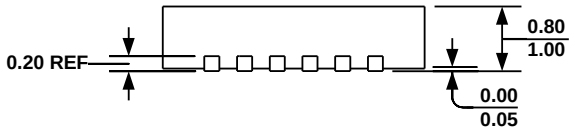
4mm x 5mm QFN28



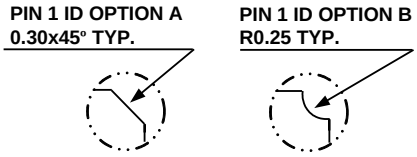
TOP VIEW



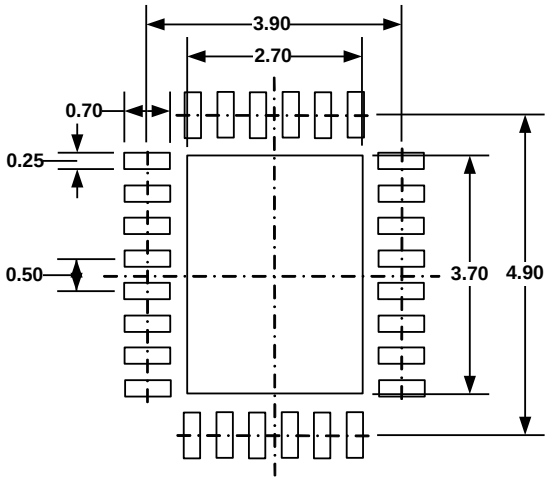
BOTTOM VIEW



SIDE VIEW



DETAIL A



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) DRAWING CONFORMS TO JEDEC MO-220, VARIATION VHGD-3.
5) DRAWING IS NOT TO SCALE.

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