# MP5403

## Configurable 2.7V-6V Mini PMIC with Dual 2.5A/3.5A Buck, One Load Switch, and Input Power Supervisory

The Future of Analog IC Technology®

***NOT RECOMMENDED FOR NEW DESIGNS, REFER TO MP5479 OR MP5417***

## DESCRIPTION

The MP5403 is a monolithic power management unit containing two high-efficiency, step-down, switching converters and a load switch. The two regulators supply current up to 3.5A and 2.5A separately, and the load switch supplies up to 3A of load current with an extremely low $R_{DS(ON)}$. With an input range of up to 6V, the MP5403 is ideal for powering ASIC and SOC for solid-state drives and other compact power systems.

The peak-current-mode control scheme with pulse-skip-mode operation provides the two switchers with fast transient response, high light-load efficiency, and minimum capacitance by using an interleaving PWM clock between the two switchers. The 3A load switch with a low 20mΩ on resistance provides flexible system configuration.

A full set of enable control pins and power good open-drain indicators allow for easy implementation of the start-up and shutdown sequences.

Full protection features include over-current protection (OCP) and thermal shutdown.

The MP5403 requires a minimal number of readily available, standard, external components and is available in a small UTQFN-20 (2.5mmx3mm) package.

## FEATURES

- Low $I_Q$: 85µA for Two Switchers Total
- Two Buck Converters
  - 3.5A with 55mΩ/20mΩ $R_{DS(ON)}$
  - 2.5A with 60mΩ/22mΩ $R_{DS(ON)}$
  - 1.5MHz Switching Frequency
  - 180° Interleaving Operation
  - 100% Duty Cycle
  - Load Switch Mode by Pulling FB Low
  - Latch-Off Short-Circuit Protection (SCP)
  - Parallel Capability by Connecting SW Nodes Together
  - Internal Soft Start and Output Discharge
  - Optimized Light-Load Efficiency
- Available Fixed Output Options via Package Trim:
  Ch1: 0.9V, 1.1V, 2.5V, 2.85V
  Ch2: 0.9V, 1.2V, 1.8V, 2.5V
- One Load Switch
  - 3A with 20mΩ $R_{DS(ON)}$
  - Soft Start and Output Discharge
  - Over-Current Protection (OCP)
- EN and Power Good for Power Sequencing
- Input Power Failure Indicator (PFL) with Adjustable Threshold and Delay
- Thermal Shutdown
- Available in Ultra-Thin UTQFN-20 (2.5mmx3mm) Package

## APPLICATIONS

- Solid-State Drives
- Hybrid Drives
- Low Voltage System Power

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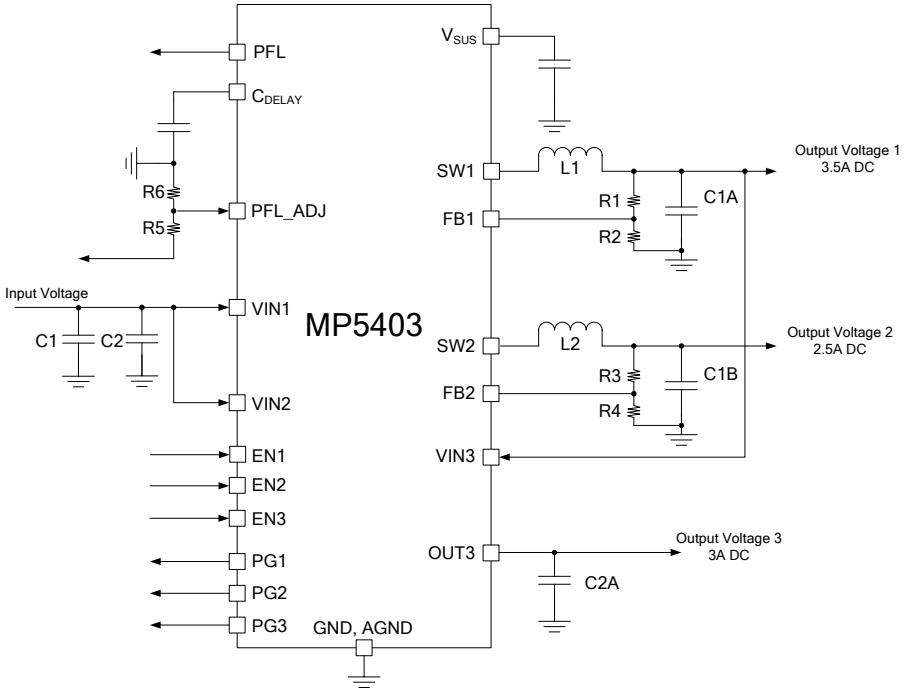
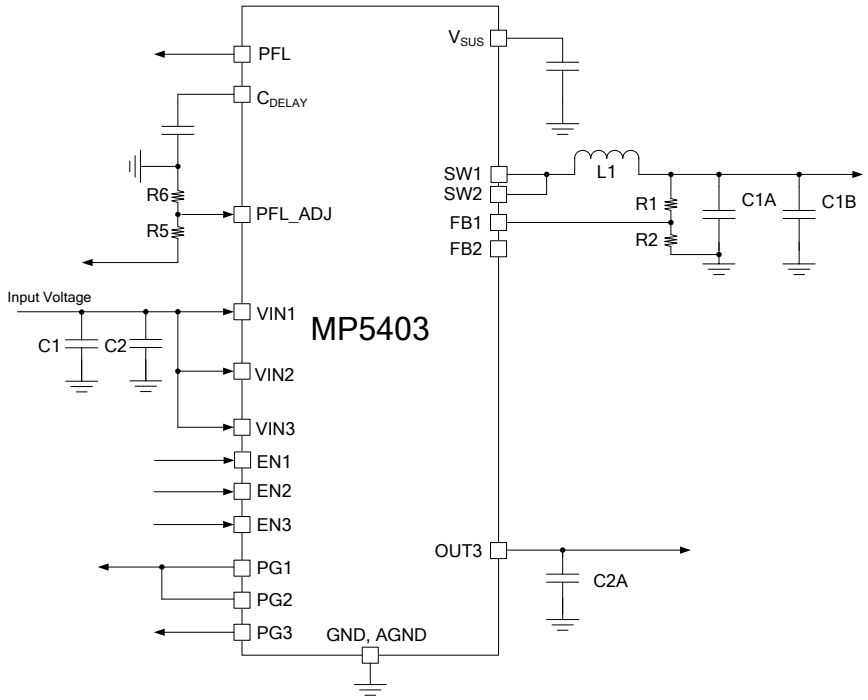
# TYPICAL APPLICATION




**Two Bucks and One Load Switch**




**One Parallel Buck and One Load Switch**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## ORDERING INFORMATION

| Part Number* | Package | Top Marking |
|---|---|---|
| MP5403GQBU | UTQFN-20 (2.5mmx3mm) | *See Below* |

* For Tape & Reel, add suffix –Z (e.g. MP5403GQBU–Z)

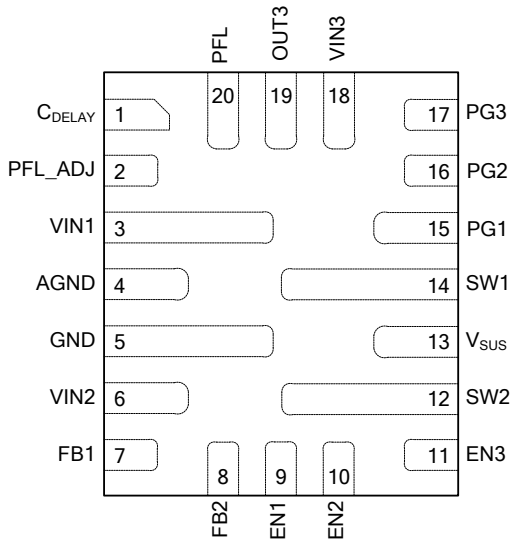
## TOP MARKING

APZ
YWW
LLL

APZ: Product code of MP5403GQBU
Y: Year code
WW: Week code
LLL: Lot number

## PACKAGE REFERENCE

**TOP VIEW**




**UTQFN-20 (2.5mmx3mm)**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## ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (VIN1/2/3) .....6.5V
$V_{SW1/2}$ .....-0.3V (-5V for <10ns) to 6.5V (10V for <10ns)
All other pins..... -0.3V to 6.5V
Continuous power dissipation ($T_A$ = +25°C) ……2.08W (2)
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature..... -65°C to +150°C

### *Recommended Operating Conditions* (3)

Supply voltage (VIN1) ..... 2.7V to 6V
If VIN1 > UVLO, supply voltage (VIN2) ..... ..... 2.0V to 6V
If VIN1 > UVLO, supply voltage (VIN3) ..... ..... 0.5V to 6V
If VIN1 < UVLO, supply voltage (VIN3) ..... ..... 2.7V to 6V
Output voltage ($V_{OUT1/2}$)..... 0.6V to VIN1/2
Output voltage ($V_{OUT3}$)..... VIN3
Operating junction temp. ($T_J$) ... -40°C to +125°C

| ***Thermal Resistance*** (4) | $\theta_{JA}$ | $\theta_{JC}$ |
|---|---|---|
| UTQFN-20 (2.5mmx3mm) | 60 | 13 |

**NOTES:**

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature $T_J$ (MAX), the junction-to-ambient thermal resistance $\theta_{JA}$, and the ambient temperature $T_A$. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D$ (MAX) = ($T_J$ (MAX)-$T_A$)/$\theta_{JA}$. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.


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## ELECTRICAL CHARACTERISTICS

**VIN1/2 = 3.6V, VIN3 = 3.6V, $T_J$ = -40°C to 125°C (7), typical value is tested at $T_J$ = 25°C unless otherwise noted.**

| Parameters | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Buck Regulators (5)** | | | | | | |
| Input voltage range | $V_{IN1}$ | For VIN1 | 2.7 | | 6 | V |
| Under-voltage lockout threshold rising | $V_{IN1_R}$ | For VIN1 | 2.3 | 2.5 | 2.65 | V |
| Under-voltage lockout threshold hysteresis | $V_{IN1_HYS}$ | For VIN1 | | 250 | | mV |
| Input voltage range for Rail2 | $V_{IN2}$ | VIN1 > $V_{IN1_R}$ | 2 | | 6 | V |
| VIN2 under-voltage lockout threshold rising | $V_{IN2_R}$ | For VIN2 | | 1.8 | 1.85 | V |
| VIN2 under-voltage lockout threshold hysteresis | $V_{IN2_HYS}$ | For VIN2 | | 300 | | mV |
| Supply current (shutdown) | $I_{SD}$ | $V_{EN1/2/3}$ = 0V, $T_J$ = 25°C | | | 1 | μA |
| Supply current (quiescent) | $I_{Q1+Q2}$ | $V_{EN1/2}$ = 2V, $V_{EN3}$ = 0V, $V_{FB1/2}$ = 1V | | 85 | 110 | μA |
| High-side switch on resistance for 3.5A switcher | $R_{DS(ON)1_H}$ | | | 55 | | mΩ |
| Low-side switch on resistance for 3.5A switcher | $R_{DS(ON)1_L}$ | | | 20 | | mΩ |
| High-side switch on resistance for 2.5A switcher | $R_{DS(ON)2_H}$ | | | 65 | | mΩ |
| Low-side switch on resistance for 2.5A switcher | $R_{DS(ON)2_L}$ | | | 22 | | mΩ |
| Switch leakage current | $I_{LK_SW1/2}$ | $V_{EN1/2}$ = 0V, VIN1/2 = 6V, $V_{SW1/2}$ = 0V and 6V, $T_J$ = 25°C | | 0 | 1 | μA |
| High-side current limit for 3.5A switcher | $I_{LIM1_H}$ | Duty = 33% | 4.5 | 5.6 | | A |
| High-side current limit for 2.5A switcher | $I_{LIM2_H}$ | Duty = 33% | 3.5 | 4.7 | | A |
| Low-side zero crossing current | $I_{ZCD1/2}$ | For both channels | | 0.1 | | A |
| Oscillator frequency | $F_{SW1/2}$ | CCM | 1.2 | 1.5 | 1.8 | MHz |
| Phase shift | PhS | CCM | | 180 | | degree |
| Minimum on time (6) | $T_{MIN_ON}$ | | | 70 | | ns |
| Minimum off time (6) | $T_{MIN_OFF}$ | | | 100 | | ns |
| Maximum duty cycle (6) | $D_{MAX}$ | | | 100 | | % |
| Feedback voltage | $V_{FB1/2}$ | $T_J$ = 25°C | 594 | 600 | 606 | mV |
| | | $T_J$ = -40°C to 125°C (7) | 591 | 600 | 609 | mV |
| Feedback currents | $I_{FB1/2}$ | FB1/2 = 0.65V | | 10 | 50 | nA |
| Internal soft-start time | $T_{SS1/2}$ | From 10% $V_{OUT}$ to 90% $V_{OUT}$ | | 0.35 | | ms |
| Output discharge resistor | $R_{DIS1/2}$ | | | 13 | | Ω |


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## ELECTRICAL CHARACTERISTICS *(continued)*

**VIN1/2 = 3.6V, VIN3 = 3.6V, $T_J$ = -40°C to 125°C [7], typical value is tested at $T_J$ = 25°C unless otherwise noted.**

| Parameters | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| EN high logic | $EN_{1/2_H}$ | | 1.05 | 1.3 | 1.5 | V |
| EN hysteresis | $EN_{1/2_HYS}$ | | | 150 | | mV |
| EN1/2 input current | $I_{EN1/2}$ | $V_{EN}$ = 2V | | 1 | | μA |
| | | $V_{EN}$ = 0V | | 0 | | |
| EN1 turn-on delay | $EN_{TD_1}$ | For channel 1 | | 100 | | μs |
| EN2 turn-on delay | $EN_{TD_2}$ | For channel 2, VIN1 > $V_{IN1_R}$ | | 100 | | μs |
| Power good upper trip threshold | $PG_{1/2_H}$ | FB with respect to the regulation | | +30 | | % |
| Power good lower trip threshold | $PG_{1/2_L}$ | FB with respect to the regulation | | -10 | | % |
| Power good hysteresis | $PG_{HY}$ | | | 5 | | % |
| Power good delay for rising | $PD_{TD_1/2\ H}$ | | | 20 | | μs |
| Power good delay for falling | $PD_{TD_1/2\ L}$ | | | 60 | | μs |
| Power good sink current capability | $V_{PG_LO_1/2}$ | Sink 1mA | | | 0.4 | V |
| Power good leakage current | $PG_{LK_1/2}$ | $V_{PG}$ = 1.8V | | 1 | | μA |
| **Load Switch** | | | | | | |
| Input voltage range | $V_{IN3}$ | VIN1 > $V_{IN1_R}$ | 0.6 | | 6 | V |
| | | VIN1 < $V_{IN1_R}$ | 2.7 | | 6 | V |
| Under-voltage lockout threshold rising | $V_{IN3_R}$ | For VIN3 | 2.3 | 2.5 | 2.65 | V |
| Under-voltage lockout threshold hysteresis | $V_{IN3_HYS}$ | For VIN3 | | 200 | | mV |
| Supply current (quiescent) | $I_{Q3}$ | From VIN3, $V_{EN1/2}$ = 0V, $V_{EN3}$ = 3.6V | | 160 | 250 | μA |
| On resistor | $R_{DSON}$ | | | 20 | | mΩ |
| EN3 high logic threshold | $EN_{3_H}$ | | 1.05 | 1.3 | 1.5 | V |
| EN3 hysteresis | $EN_{3_HYS}$ | | | 150 | | mV |
| EN3 turn-on delay | $EN_{TD_3}$ | VIN1 > $V_{IN1_R}$ | | 70 | | μs |
| | | VIN1 < $V_{IN1_R}$ | | 70 | | |
| EN3 input current | $I_{EN3}$ | $V_{EN3}$ = 2V | | 1 | | μA |
| | | $V_{EN3}$ = 0V | | 0 | | |
| PG3 high logic threshold | $PG_{3_H}$ | VIN3 - $V_{OUT3}$ is smaller than the range | 150 | 200 | | mV |
| PG3 low logic threshold | $PG_{3_L}$ | VIN3 - $V_{OUT3}$ is larger than the range | | 250 | | mV |
| Power good delay for rising | $PD_{TD_3}$ | | | 40 | | μs |
| Power good sink current capability | $V_{PG_LO_3}$ | Sink 1mA | | | 0.4 | V |
| Power good leakage current | $PG_{LK_3}$ | $V_{PG}$ = 1.8V | | 1 | | μA |
| Current limit | $I_{LIM3}$ | | | 5.6 | | A |


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## ELECTRICAL CHARACTERISTICS *(continued)*

**VIN1/2 = 3.6V, VIN3 = 3.6V, $T_J$ = -40°C to 125°C [7], typical value is tested at $T_J$ = 25°C unless otherwise noted.**

| Parameters | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Internal soft-start time | $T_{ss3}$ | From 10% $V_{OUT}$ to 90% $V_{OUT}$ | | 0.35 | | ms |
| Output resistor | $R_{DIS}$ | | | 13 | | Ω |
| **Power Failure Circuitry** | | | | | | |
| $V_{SUS}$ voltage | $V_{SUS}$ | | | 3.6 | | V |
| $V_{SUS}$ leakage current | $I_{SUS_LK}$ | $V_{SUS}$ = 3.6V, VIN1 = VIN3 = 3.6V, $T_J$ = 25°C | | 0 | 1 | μA |
| PFL_ADJ reference | PFL_ADJ | $T_A$ = 25°C | 594 | 600 | 606 | mV |
| | | $T_A$ = -40°C to 125°C [7] | 591 | 600 | 609 | |
| PFL hysteresis | PFL_HYS | | | 3 | | % |
| PFL high-to-low delay | $T_{PFL_HL}$ | | | 1 | | μs |
| $C_{DELAY}$ internal current source | $I_{DELAY}$ | | | 3.1 | | μA |
| Power good sink current capability | $V_{PFL_LO}$ | Sink 1mA | | | 0.4 | V |
| Power good leakage current | $PFL_{LK}$ | $V_{PFL}$ = 1.8V | | 1 | | μA |
| Thermal shutdown [6] | $T_{SD}$ | | | 160 | | °C |
| Thermal hysteresis [6] | $T_{HYS}$ | | | 30 | | °C |

**NOTES:**
5) VIN1 provides control voltage if VIN3 is lower than 2.7V.
6) Guaranteed by design.
7) Guaranteed by characterization test, not production tested.


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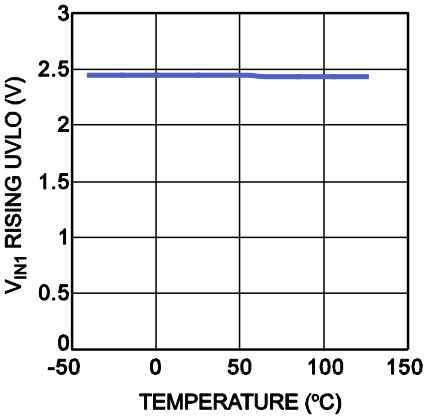
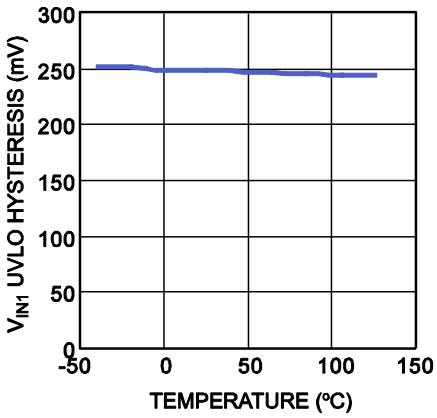
## TYPICAL PERFORMANCE CHARACTERISTICS

**VIN = 5V, $V_{OUT1}$ = 1.8V, $V_{OUT2}$ = 1.2V, L1 = 0.47µH, L2 = 0.47µH, $T_A$ = +25°C, unless otherwise noted.**

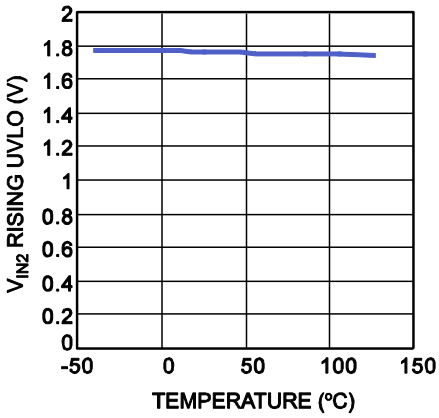
**$V_{IN1}$ Rising UVLO**



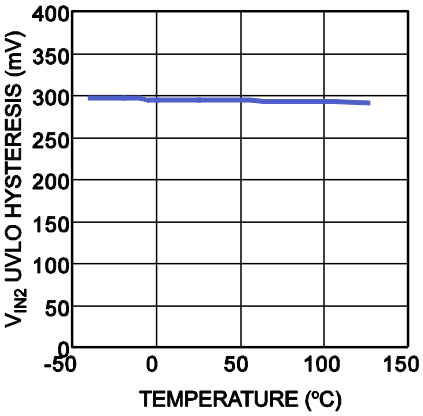

**$V_{IN1}$ UVLO Hysteresis**



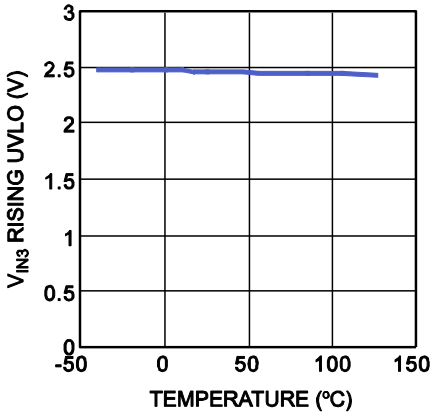

**$V_{IN2}$ Rising UVLO**



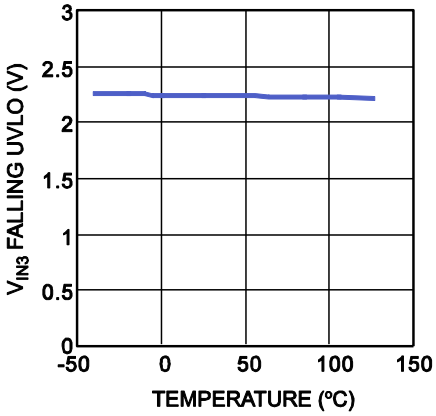

**$V_{IN2}$ UVLO Hysteresis**



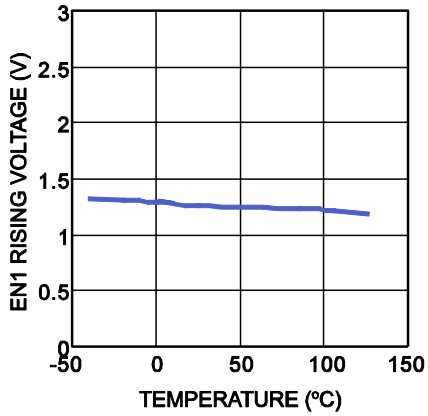

**$V_{IN3}$ Rising UVLO**



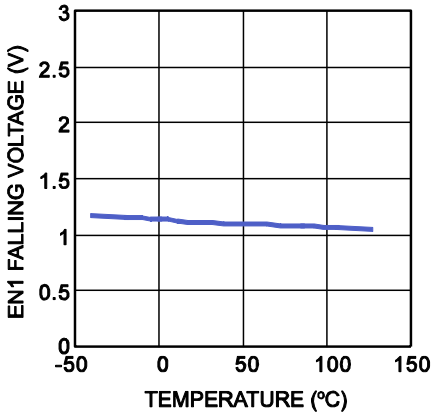

**$V_{IN3}$ Falling UVLO**



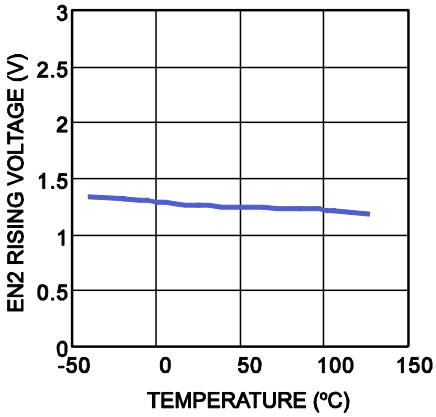

**EN1 Rising Voltage**




**EN1 Falling Voltage**




**EN2 Rising Voltage**





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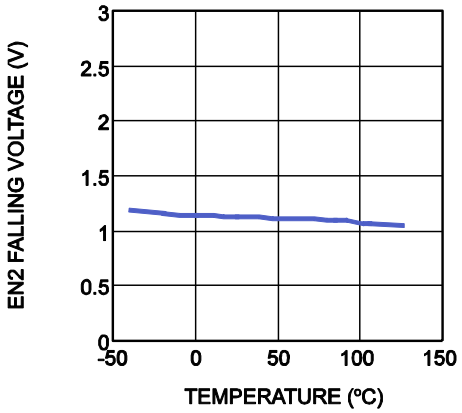
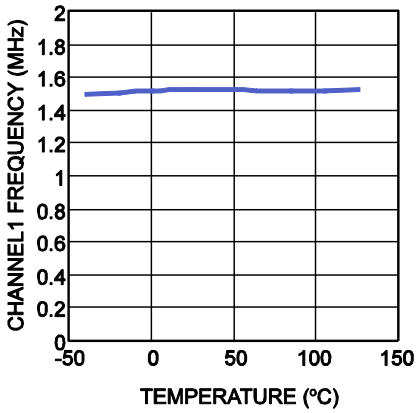
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**VIN = 5V, $V_{OUT1}$ = 1.8V, $V_{OUT2}$ = 1.2V, L1 = 0.47μH, L2 = 0.47μH, $T_A$ = +25°C, unless otherwise noted.**

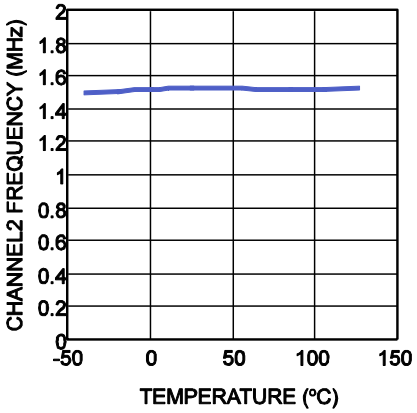
**EN2 Falling Voltage**



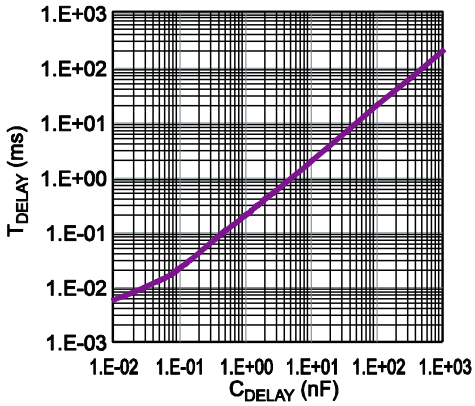

**Channel1 Frequency**



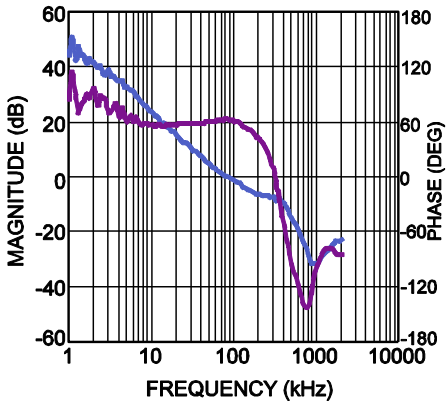

**Channel2 Frequency**



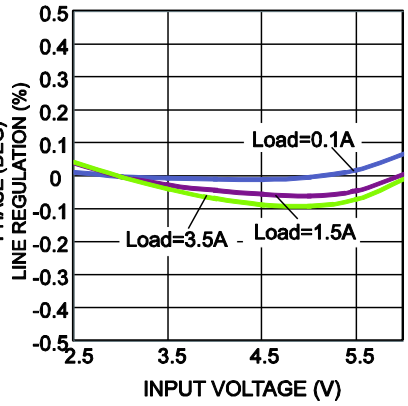

**$C_{DELAY}$ vs. $T_{DELAY}$**



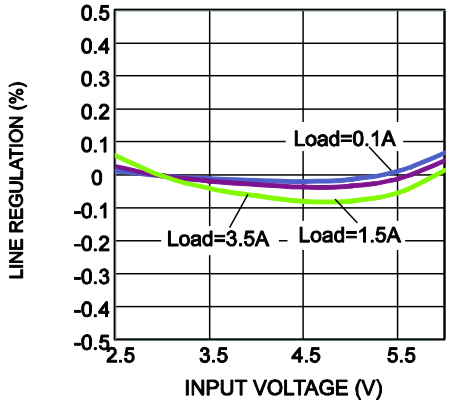

**Bode Plot**
$V_{OUT}$=3.3V



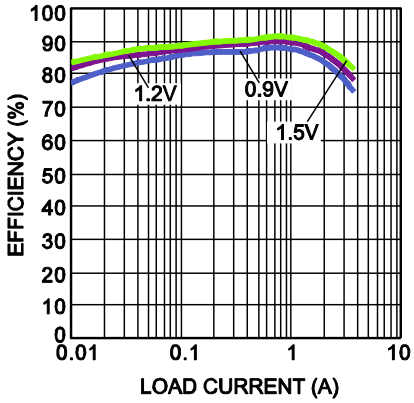

**Line Regulation**
CH1



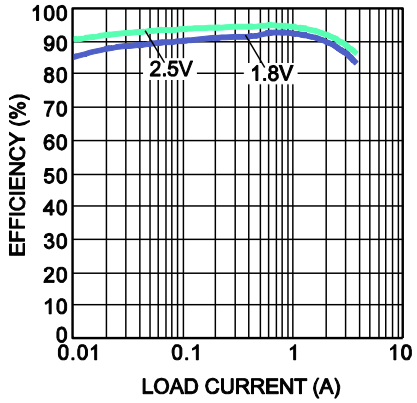

**Line Regulation**
CH2




**Efficiency**
CH1, $V_{IN}$ =3.3V




**Efficiency**
CH1, $V_{IN}$ =3.3V





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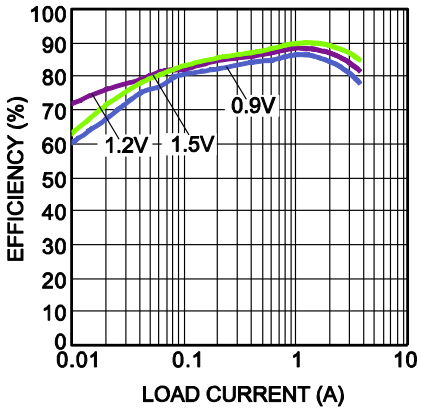
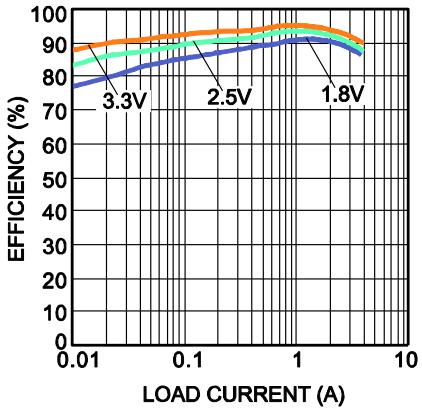
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**VIN = 5V, $V_{OUT1}$ = 1.8V, $V_{OUT2}$ = 1.2V, L1 = 0.47µH, L2 = 0.47µH, $T_A$ = +25°C, unless otherwise noted.**

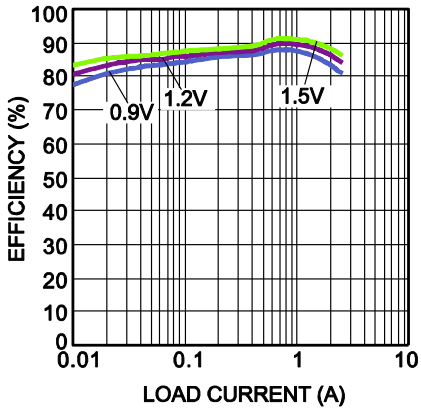
**Efficiency**
CH1



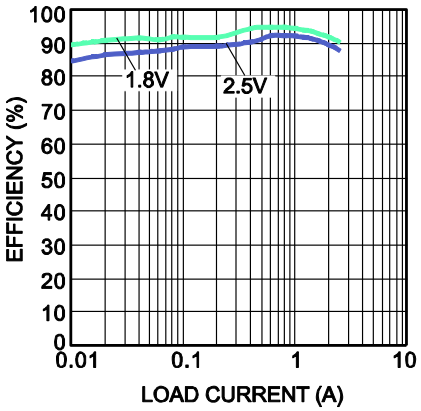

**Efficiency**
CH1



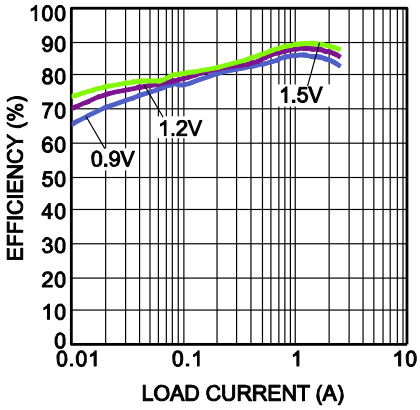

**Efficiency**
CH2, $V_{IN}$=3.3V



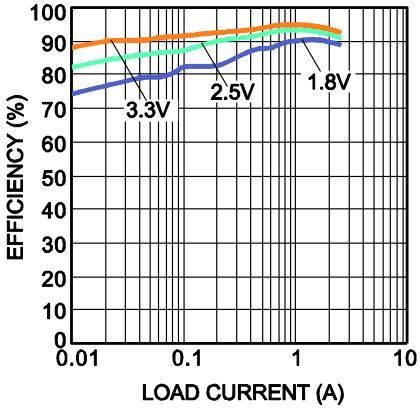

**Efficiency**
CH2, $V_{IN}$=3.3V




**Efficiency**
CH2




**Efficiency**
CH2





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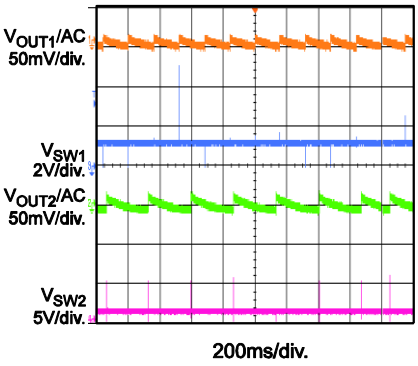
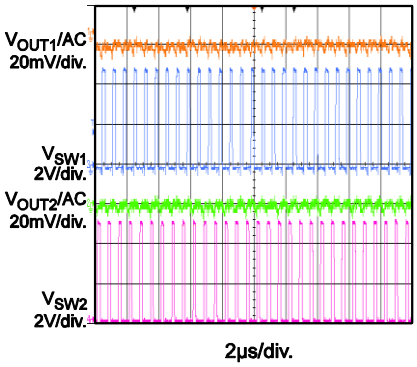
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**VIN = 5V, $V_{OUT1}$ = 1.2V, $V_{OUT2}$ = 1.2V, L1 = 0.47µH, L2 = 0.47µH, $T_A$ = +25°C, unless otherwise noted.**

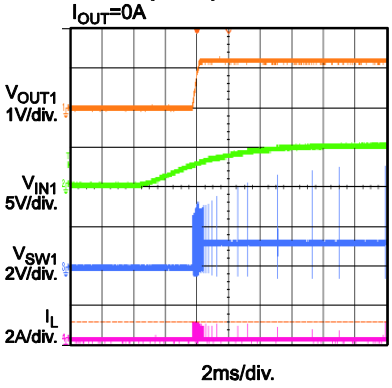
**Output Ripple**
$I_{OUT1}$=0A



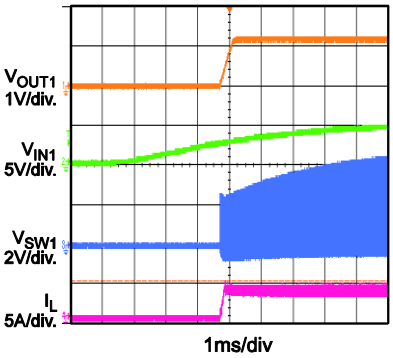

**Output Ripple**
$I_{OUT1}$=3.5A, $I_{OUT2}$=2.5A



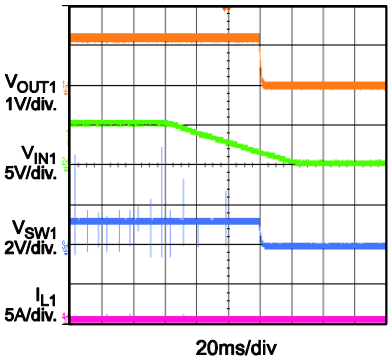

**VIN Power Up without Load (CH1)**
$I_{OUT}$=0A



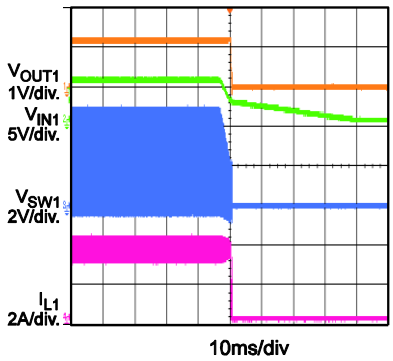

**VIN Power Up with 3.5A Load (CH1)**
$I_{OUT1}$=3.5A



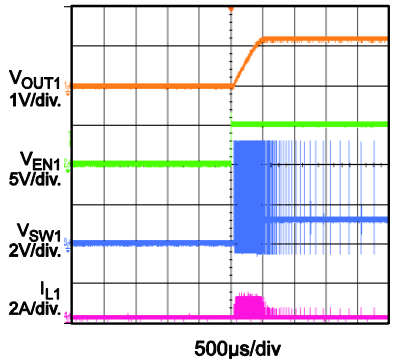

**VIN Power Down without Load (CH1)**
$I_{OUT1}$=0A



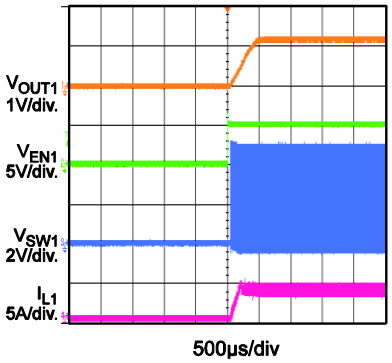

**VIN Power Down with 3.5A Load(CH1)**
$I_{OUT1}$=3.5A



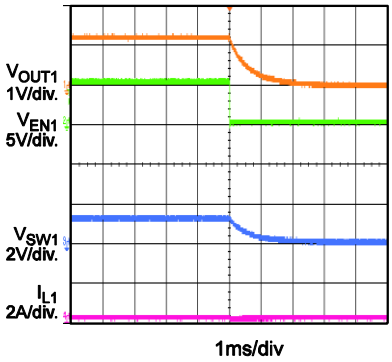

**EN On without Load (CH1)**
$I_{OUT1}$=0A




**EN On with 3.5A Load (CH1)**
$I_{OUT1}$=3.5A




**EN Down without Load (CH1)**
$I_{OUT1}$=0A





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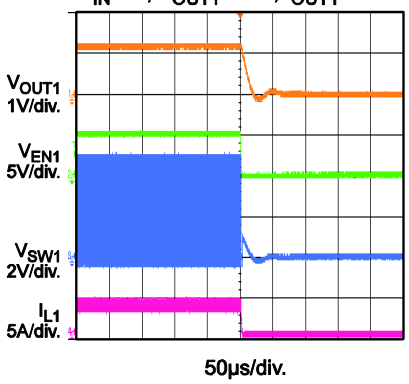
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**VIN = 5V, $V_{OUT1}$ = 1.2V, $V_{OUT2}$ = 1.2V, L1 = 0.47µH, L2 = 0.47µH, $T_A$ = +25°C, unless otherwise noted.**

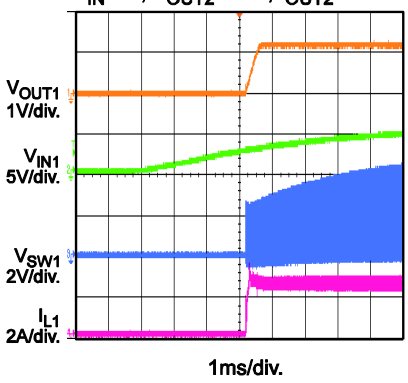
**EN Down with 3.5A Load (CH1)**

$V_{IN}$=5V, $V_{OUT1}$=1.2V, $I_{OUT1}$=3.5A



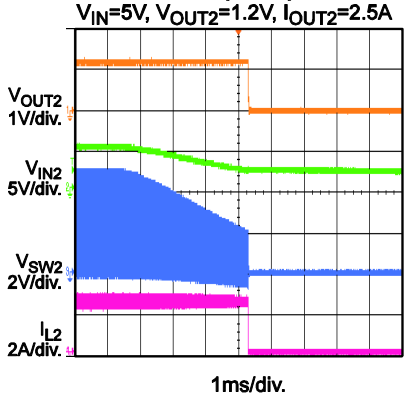

**VIN Power On with 2.5A Load (CH2)**

$V_{IN}$=5V, $V_{OUT2}$=1.2V, $I_{OUT2}$=2.5A



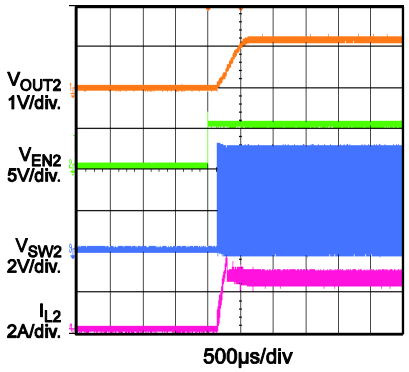

**VIN Power Down with 2.5A Load (CH2)**

$V_{IN}$=5V, $V_{OUT2}$=1.2V, $I_{OUT2}$=2.5A



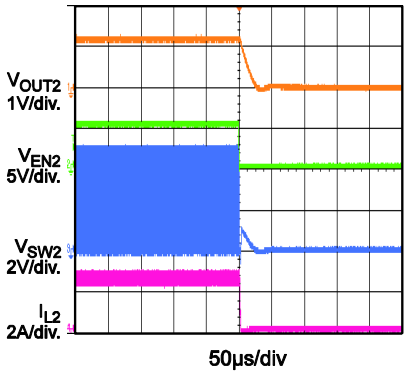

**Enable On with 2.5A Load (CH2)**

$V_{IN}$=5V, $V_{OUT2}$=1.2V, $I_{OUT2}$=2.5A



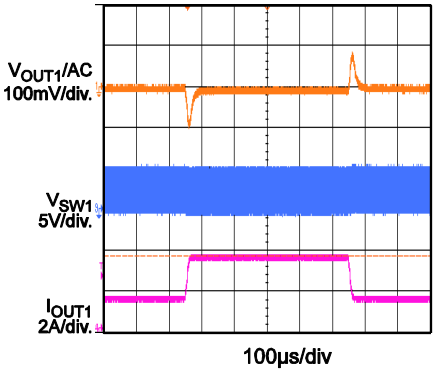

**Enable Down with 2.5A Load (CH2)**

$V_{IN}$=5V, $V_{OUT2}$=1.2V, $I_{OUT2}$=2.5A



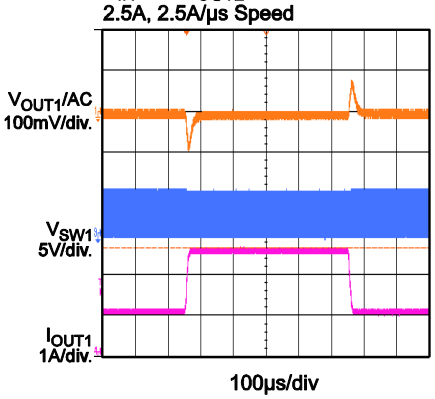

**CH1 Transient**

$V_{IN}$=5V, $V_{OUT1}$=1.2V, 1A Transient to 3.5A, 2.5A/µs Speed



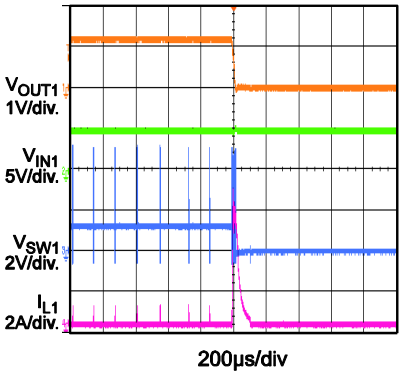

**CH2 Transient**

$V_{IN}$=5V, $V_{OUT2}$=1.2V, 1A Transient to 2.5A, 2.5A/µs Speed



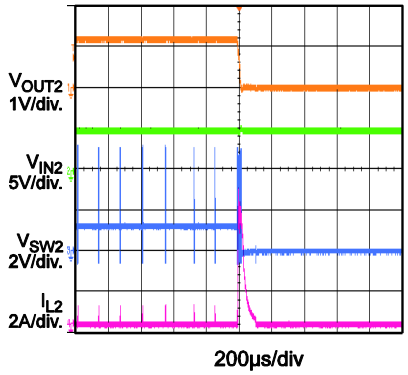

**CH1 Short Enter**

$V_{IN}$=5V, $V_{OUT1}$=1.2V, $I_{OUT1}$=0A




**CH2 Short Enter**

$V_{IN}$=5V, $V_{OUT2}$=1.2V, $I_{OUT2}$=0A





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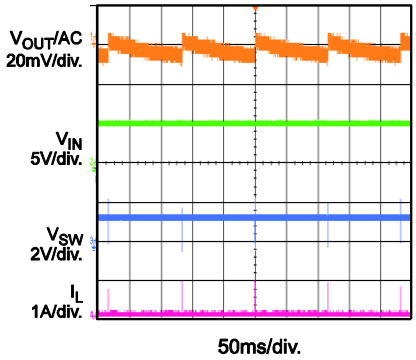
*NOT RECOMMENDED FOR NEW DESIGNS, REFER TO MP5479 OR MP5417*

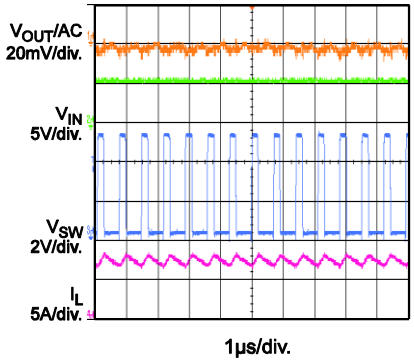
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**VIN = 5V, $V_{OUT1}$ = 1.2V, $V_{OUT2}$ = 1.2V, L1 = 0.47µH, L2 = 0.47µH, $T_A$ = +25°C, unless otherwise noted.**

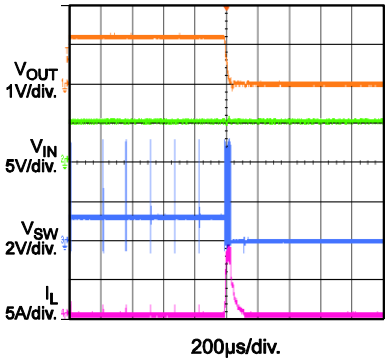
**Output Ripple (Parallel)**
$V_{IN}$=5V, $V_{OUT}$=1.2V, $I_{OUT}$=0A



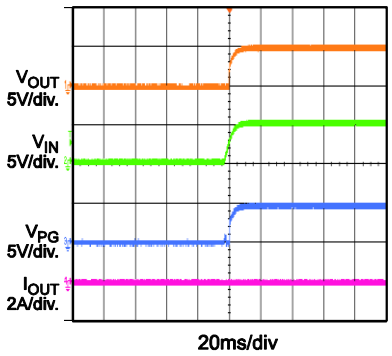

**Output Ripple (Parallel)**
$V_{IN}$=5V, $V_{OUT}$=1.2V, $I_{OUT}$=7A



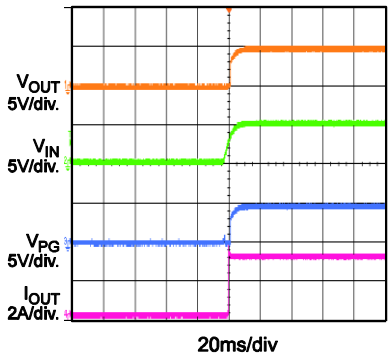

**Short Enter (Parallel)**
$V_{IN}$=5V, $V_{OUT}$=1.2V, $I_{OUT2}$=0A



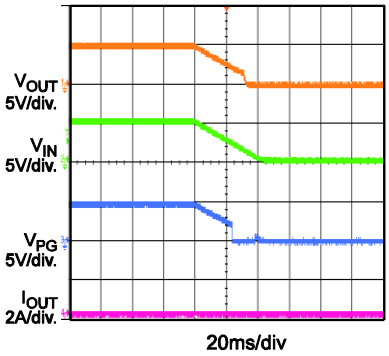

**VIN Start-Up (Load Switch)**
$V_{IN}$=5V, $V_{OUT}$=5V, $I_{OUT}$=0A



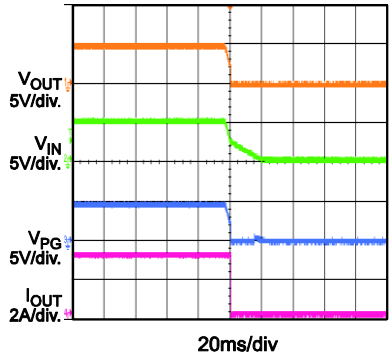

**VIN Start-Up (Load Switch)**
$V_{IN}$=5V, $V_{OUT}$=5V, $I_{OUT}$=3A



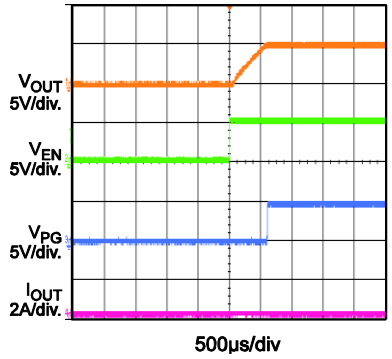

**VIN Shutdown (Load Switch)**
$V_{IN}$=5V, $V_{OUT}$=5V, $I_{OUT}$=0A



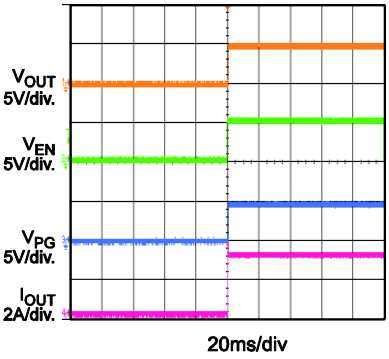

**VIN Shutdown (Load Switch)**
$V_{IN}$=5V, $V_{OUT}$=5V, $I_{OUT}$=3A




**EN Start-Up (Load Switch)**
$V_{IN}$=5V, $V_{OUT}$=5V, $I_{OUT}$=0A




**EN Start-Up (Load Switch)**
$V_{IN}$=5V, $V_{OUT}$=5V, $I_{OUT}$=3A





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## PIN FUNCTIONS

| Pin # | Name | Description |
|---|---|---|
| 1 | $C_{DELAY}$ | **Programmable PFL low-to-high delay time.** When $C_{DELAY}$ is floated, the delay time is minimized. |
| 2 | PFL_ADJ | **Power failure threshold adjust.** A resistor divider connected to the voltage rails is used to program the power failure threshold. The resistor divider needs to be monitored. |
| 3 | VIN1 | **Input supply voltage to the 3.5A switching regulators and internal logic module.** Place a small decoupling capacitor as close to VIN1 and GND as possible. |
| 4 | AGND | **Analog ground.** |
| 5 | GND | **Ground.** |
| 6 | VIN2 | **Input supply voltage to the 2.5A switching regulators.** Place a small decoupling capacitor as close to VIN2 and GND as possible. |
| 7 | FB1 | **Feedback voltage sensing for the 3.5A regulator.** Connect the output voltage of the 3.5A regulator through a resistor divider to FB1 to achieve output voltage regulation. Pull FB1 to ground to operate the 3.5A regulator in 100% duty cycle on mode. |
| 8 | FB2 | **Feedback voltage sensing for the 2.5A regulator.** Connect the output voltage of the 2.5A regulator through a resistor divider to FB2 to achieve output voltage regulation. Pull FB2 to ground to operate the 2.5A regulator in 100% duty cycle on mode. |
| 9 | EN1 | **Enable on/off control for the 3.5A regulator.** There is a 2MΩ resistor from EN1 to GND internally. Float or ground EN1 to turn off the 3.5A regulator. |
| 10 | EN2 | **Enable on/off control for the 2.5A regulator.** There is a 2MΩ resistor from EN2 to GND internally. Float or ground EN2 to turn off the 2.5A regulator. |
| 11 | EN3 | **Enable on/off control for the load switch.** There is a 2MΩ resistor from EN3 to GND internally. Float or ground EN3 to turn off the load switch. |
| 12 | SW2 | **Switch output for the 2.5A regulator.** A thick and wide power routing trace is recommended for SW2 to conduct current. |
| 13 | $V_{SUS}$ | **Sustain voltage.** Place a small decoupling capacitor as close to $V_{SUS}$ and GND as possible. |
| 14 | SW1 | **Switch output for the 3.5A regulator.** A thick and wide power routing trace is recommended for SW1 to conduct current. |
| 15 | PG1 | **Power good for the 3.5A regulator.** PG1 is an open-drain output. When the output voltage is between -10% to +30% of the regulation, PG1 is pulled high externally. When there is no supply, PG1 is pulled low internally. |
| 16 | PG2 | **Power good for the 2.5A regulator.** PG2 is an open-drain output. When the output voltage is between -10% to +30% of the regulation, PG2 is pulled high externally. When there is no supply, PG2 is pulled low internally. |
| 17 | PG3 | **Power good for the load switch.** PG3 is an open-drain output. When the output voltage is below 200mV compared with the input voltage, PG3 is pulled high externally. |
| 18 | VIN3 | **Input supply voltage for the load switch.** |
| 19 | OUT3 | **Output voltage for the load switch.** |
| 20 | PFL | **Power failure indicator.** PFL is an open-drain output. When the PFL_ADJ voltage is less than 0.6V, PFL is pulled low immediately. |


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## BLOCK DIAGRAM

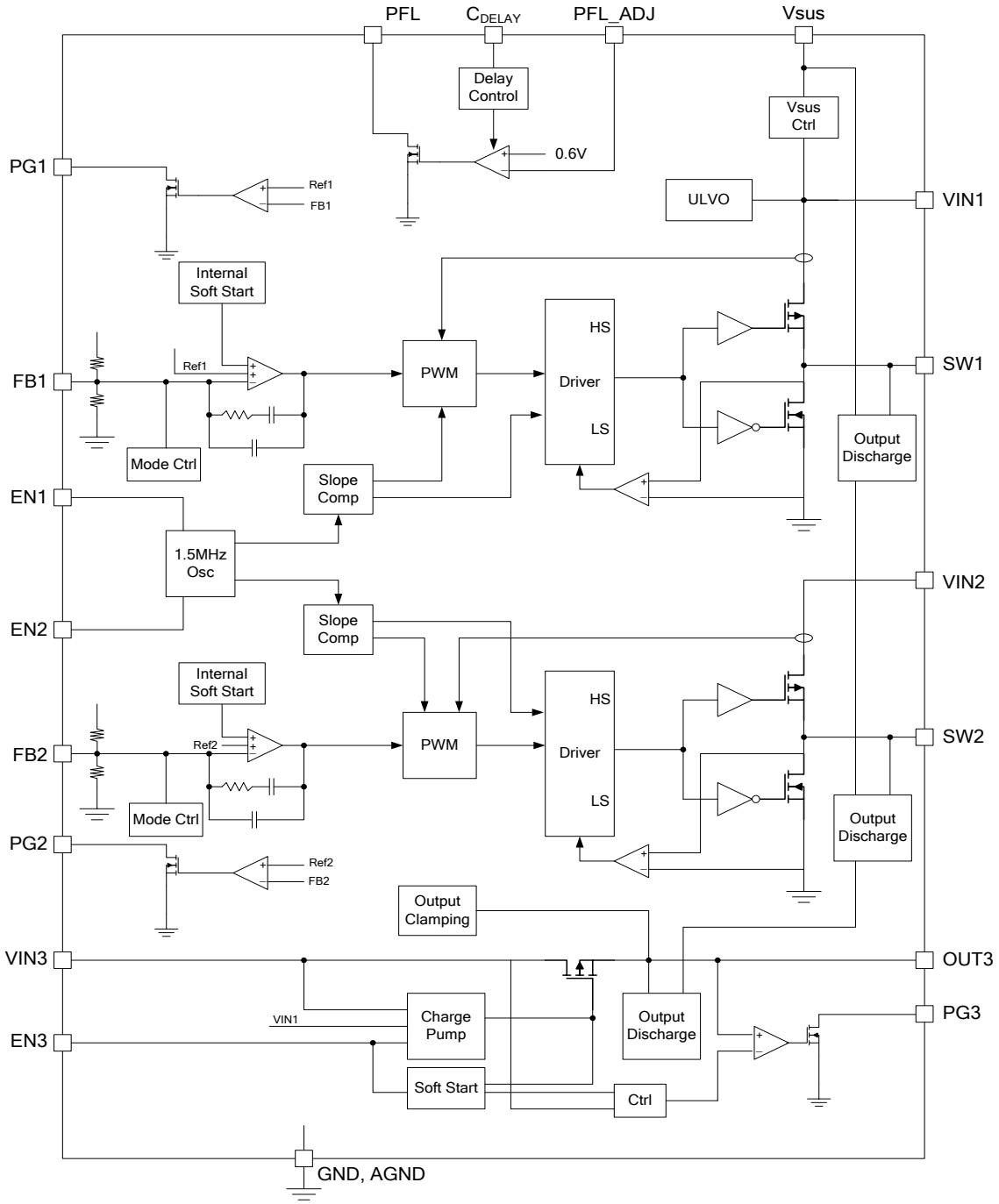


**Figure 1: Functional Block Diagram**


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# OPERATION

The MP5403 has two step-down regulators and one load switch integrated into an ultra-small UTQFN-20 package. The two buck regulators are able to run up to 3.5A and 2.5A of load current, respectively. With a peak current mode control scheme and an interleaving PWM clock, the MP5403 minimizes the input voltage ripple and achieves a fast dynamic load response. The load switch has 3A and only 20mΩ of $R_{DS(ON)}$, achieves extremely small conduction loss, and provides tight regulation with a high load current. The load switch can also clamp $V_{OUT}$ to 5.5V. The MP5403 can be used in compact solid-state drives (SSD), portable instruments, and battery-powered devices.

## Peak-Current Mode Control

The two buck regulators of the MP5403 operate at an 180° phase shift to reduce the input current ripple and the required input capacitor. In continuous conduction mode (CCM), two internal clocks control the switching behavior. The high-side MOSFET (HS-FET) turns on at the corresponding clock's rising edge. The two clocks are at an 180° phase shift. When the high-side switch current increases and reaches the internal compensation voltage, the high-side switch is turned off, and the low-side switch is turned on to conduct current.

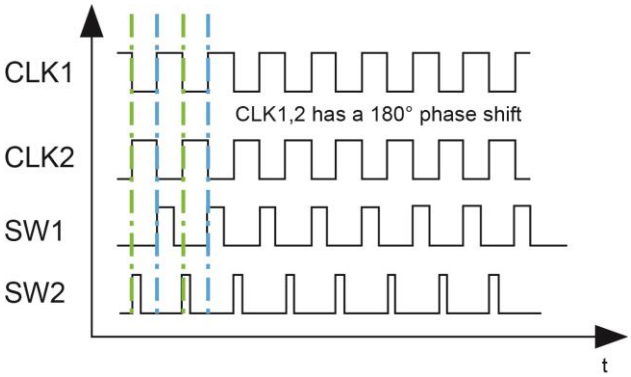


**Figure 2: Phase Shift**

The switching frequency is 1.5MHz, typically, running in CCM. With a lower input voltage, the switching frequency falls and works with a large duty cycle and a fixed off-time mode.

## Light-Load Operation

In light load mode, the MP5403 uses a proprietary control scheme to save power and improve efficiency. The MP5403 turns off the low-side switch when the inductor current begins reversing. The MP5403 then works in discontinuous conduction mode (DCM) operation. With light-load mode control, the switching loss can be greatly reduced due to the lower switching frequency.

A zero-current cross detection (ZCD) circuit is used to detect if the inductor current begins reversing. Considering the internal circuit propagation time, the typical delay is 50ns. This means that the inductor current continues falling after ZCD is triggered in this delay. If the inductor current falling slew rate is fast ($V_{OUT}$ is high or close to VIN), the low-side MOSFET (LS-FET) is turned off, and the inductor current may be negative. This prevents the MP5403 from entering DCM operation. If DCM operation is required, the off time of the LS-FET in CCM should be longer than 100ns. For example, if VIN is 3.6V and $V_{OUT}$ is 3.4V, then the off time in CCM is 37ns. It is difficult to enter DCM at light load. Using a smaller inductor can improve this and make it easier to enter DCM.

## Enable (EN)

When VIN1 is greater than the under-voltage lockout (UVLO) threshold (typically 2.5V), the regulators or the load switch can be enabled by pulling its EN pins above the EN UVLO threshold. Leave the EN pins floating or pull the EN pins down to ground to disable the corresponding channel. There is an internal 2MΩ resistor from the EN pins to ground. There is a delay of about 100µs for the VIN1 and VIN2 enable start-up. The VIN3 enable start-up delay is shorter (around 70µs).

## Soft Start (SS) and Output Discharge

The MP5403 has a built-in soft start (SS) that ramps up the output voltage at a controlled slew rate to prevent overshooting at start-up for both step-down regulators and the load switch. For the step-down regulator, the soft-start time is about 500µs, typically. For the load switch, the soft-start time is set to around 350µs. When the regulators are disabled, the internal discharge


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resistor discharges $V_{OUT}$. The discharge resistor is biased by $V_{SUS}$ (see Table 1).

**Table 1: Output Discharge Conditions**

| Output Discharge | VIN | EN |
|---|---|---|
| No | >UVLO | High |
| Yes | >UVLO | Low |
| Yes | <UVLO | High |
| Yes | <UVLO | Low |

### Power Good (PG) Indicators

The MP5403 has three separate power good (PG), open-drain, output indicators for the regulators and load switch. For the two step-down regulators, when FB is in the regulation window (between 90% to 130% of the reference voltage, 0.6V), PG1 and PG2 are pulled up to the external bus voltage through external resistors. The pull-up resistors are recommend not to be too low to ensure that the leakage current is small when the PG pins are low and not too high if the PG pins are used to drive the downstream signals. Normally, pull-up resistors between 10kΩ to 400kΩ are sufficient. The PG rising delay is around 20µs. If the FB voltage drops below 90% or above 130% of the reference voltage, the PG pins are pulled down to ground by an internal MOSFET. The MOSFET has a maximum $R_{DS(ON)}$ of less than 400Ω. There is also a 60µs delay for the PG falling threshold trigger.

The power good pin for the load switch (PG3) is pulled high when the input voltage of the load switch (VIN3) is higher than its UVLO threshold, the output voltage (VOUT3) is less than 200mV compared with the input voltage of the load switch, and there is around 40µs of rising delay for the PG3 indicator. If any of these three conditions are not met, PG3 is pulled low.

The PG indicators are pulled low when VIN1 is below UVLO. In this condition, the PG pins are self-driven low (around 0.6V).

There is another important feature on PG to detect the parallel capability usage (see Figure 3). After VIN rises above ULVO and either EN1 or EN2 is high, the MP5403 uses an internal 50µs detection time window to determine if the buck regulator is entering parallel mode. The schematic in Figure 3 is only active in the 50µs detection window.

During this 50µs time window, the PG1 (M2) switch is turned off, and an internal 5µA pulled high current is applied on PG1. The PG2 (M3) switch (<400Ω) is turned on. If the PG1 voltage is <150mV, the MP5403 enters parallel mode (EN1 controls the parallel mode on/off). If the PG1 voltage is >150mV, the MP5403 enters independent working mode (EN1 and EN2 control separately).

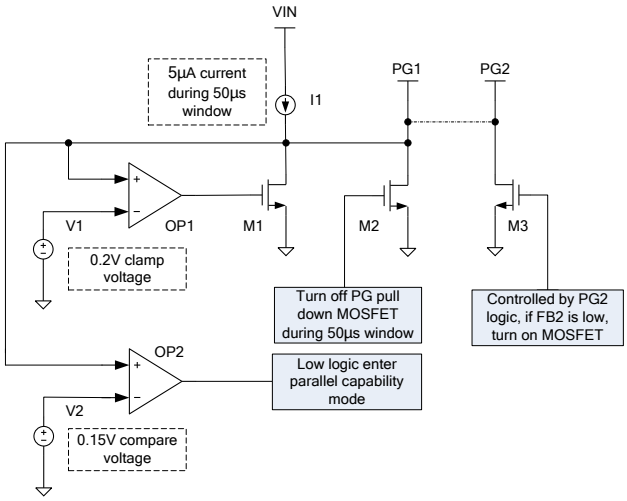


**Figure 3: PG Functional Schematic**

If PG1 is connected to PG2 externally, the PG1 voltage is pulled below 150mV to make the MP5403 enter parallel mode.

The PG1 connection requires special consideration (see Figure 4). If PG1 is connected to another IC's PG to control the other device together, a resistor (RT) is required to prevent the MP5403 from entering parallel mode. RT is suggested to be 50kΩ.

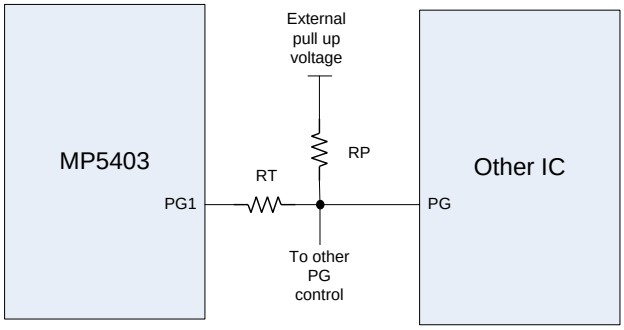


**Figure 4: PG Connection Example**


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### Power Failure Indicator (PFL)

The power failure indicator (PFL) senses the external voltage rails. When the input voltage is below the programmed threshold, the PFL open-drain output is pulled low immediately to indicate the monitored power failure. This function is enabled by pulling any of the EN pins (EN1, EN2, or EN3) high and disabled by pulling all of the EN pins low. For example, if all EN pins are low, PFL is zero, even if VIN is above the UVLO threshold and PFL_ADJ is higher than 0.6V. Ensure that there is at least one EN pin that is high before using it to control the other pins.

PFL_ADJ is used to adjust the power failure threshold voltage. A resistor divider is used to monitor the voltage rail. When the PFL_ADJ voltage is lower than 0.6V, PFL is pulled down to indicate the sense power failure. When the PFL_ADJ voltage is higher than the 0.6V reference voltage, PFL is pulled high with the delay, which is set by $C_{DELAY}$.

Choose $C_{DELAY}$ using Equation (1):

$$T_{DELAY}(\mu s) = \frac{C_{DELAY}(pF) \times 0.62}{I_{DELAY}(\mu A)} + 3.5\mu s \qquad (1)$$

Where $T_{DELAY}$ is the PFL delay time, and $I_{DELAY}$ is the $C_{DELAY}$ internal current source (typically 3.1µA).

### Current Limit

The MP5403 has a high-side 5.6A current limit for the first regulator and a 4.7A current limit for the second regulator. When the high-side switch reaches the current limit threshold, the regulators shut down the high-side switch and force the low-side switch on until the low-side current drops to the low-side valley current threshold (5A and 4A for the two regulators). After the low-side current reaches the valley current threshold, the high-side switch is allowed to turn on again. If the high load current persists, the high side turns on again, and the current limit mechanism repeats until the output voltage drops to the short-circuit threshold. If the high-load current does not persist, then the regulator runs back to normal condition.

For the load switch, the current limit begins working when the load switch current reaches the current limit threshold. The gate is pulled low to regulate the load switch current to the current limit. The output voltage drops until thermal shutdown occurs.

### Short Circuit and Recovery

When CH1 or CH2 is in buck mode, the MP5403 enters short-circuit protection (SCP) mode when the inductor current reaches the current limit for 300µs continuously or the output voltage drops below 50% of the regulation voltage. In SCP mode, the MP5403 disables the output power stage, discharges the soft-start capacitor, and enters latch-off protection mode. The MP5403 restarts by recycling the power.

### Parallel Capability

By connecting SW1 and SW2 together and connecting PG1 and PG2 together, the two step-down regulators can run in parallel mode to increase the output power capability. In this mode, only FB1 is used to program the output voltage. Keep FB2 floating.

### Load-Switch Mode of Buck1/2

By pulling FB1 or FB2 to ground, the step-down regulator 1 or 2 can enter load-switch mode without having to install an inductor. The MP5403 pulses a smaller current to the FB pins before the system starts up. If a low impedance is connected to the FB pins, the MP5403 enters load-switch mode, where the high-side switch is turned on gradually to achieve a soft start, and short-circuit protection is equipped.


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# APPLICATION INFORMATION

## Output Voltage Setting

The output voltage of the two switchers can be adjusted with external resistor dividers (see Figure 5). The typical reference voltage of both FB1 and FB2 is 600mV. The maximum allowed voltage for the outputs is close to the input voltage minus the voltage drop when the high-side switch is 100% turned on.

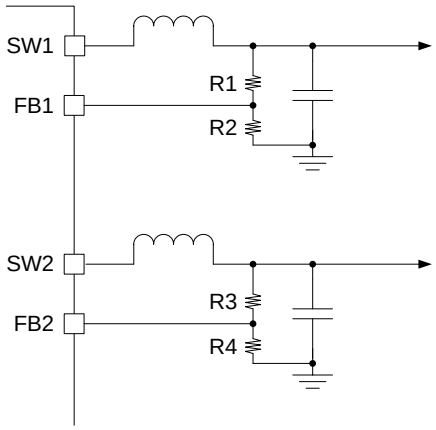


**Figure 5: Feedback Resistor Dividers to Set the Output Voltages**

The divider current is recommended to be higher than 500nA to avoid influence from the feedback node leakage current (which is in the 10nA level). Additionally, considering control loop optimization, the pull-up resistor is recommended to be between 100kΩ to 500kΩ. Then, the pull-down resistor can be calculated with Equation (2):

$$R2(\text{or}R4) = \frac{R1(\text{or}R3)}{\frac{V_{OUT}}{0.6V} - 1} \quad (2)$$

Table 2 shows some typical output voltages and their corresponding recommended resistor divider values.

**Table 2: Output Voltage vs. Resistor Values**

| $V_{OUT}$ | R1 | R2 |
|---|---|---|
| 1.2V | 300kΩ | 300kΩ |
| 1.5V | 300kΩ | 200kΩ |
| 1.8V | 300kΩ | 150kΩ |
| 2.5V | 300kΩ | 95.3kΩ |
| 3.3V | 300kΩ | 66.5kΩ |

**NOTE:** $C_{OUT}$ is 22µF for each channel.

## Inductor Selection

The inductor has a great impact on several key performances for the step-down switcher, such as inductor current ripple, output voltage ripple, efficiency, and load transient response.

Calculate the inductor current ripple with Equation (3):

$$\Delta I_L = \frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN} \cdot L \cdot f_{SW}} \quad (3)$$

Calculate the inductor peak current with Equation (4):

$$I_{Lpk} = I_{Load} + \frac{\Delta I_L}{2} \quad (4)$$

Choosing the inductance is a trade-off between the output ripple, efficiency, and transient response. The larger the inductance is, the smaller the output ripple, but the slower the response. Choose an inductance to make the ripple current 30% to 40% of the max load current.

The inductor saturation current must be higher than the inductor peak current.

The inductor also impacts the solution efficiency in terms of conduction loss and coil-related loss. Generally, the DC resistance provides DC conduction loss information. For AC conduction loss and coil-related loss, please refer to the vendor datasheet for more detailed information.

### Input Capacitor Selection

The input capacitor reduces the surge current drawn from the input and the switching noise from the device. Select an input capacitor with a switching frequency impedance less than the input source impedance to prevent high-frequency switching current from passing to the input source. Use low ESR ceramic capacitors with X5R or X7R dielectrics and small temperature coefficients. For most applications, a 22µF capacitor is sufficient.


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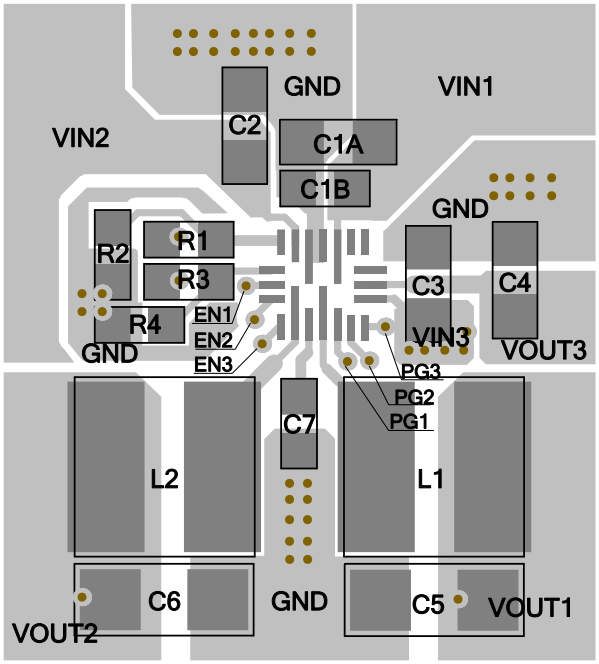
### Output Capacitor Selection

The output capacitor limits the output voltage ripple and ensures a stable regulation loop. Select an output capacitor with low impedance at the switching frequency. Use ceramic capacitors with X5R or X7R dielectrics. Using an electrolytic capacitor may result in additional output voltage ripple, thermal issues, and require additional care in selecting the feedback resistor (R1) due to the large ESR. For most applications, a 22µF capacitor is sufficient.

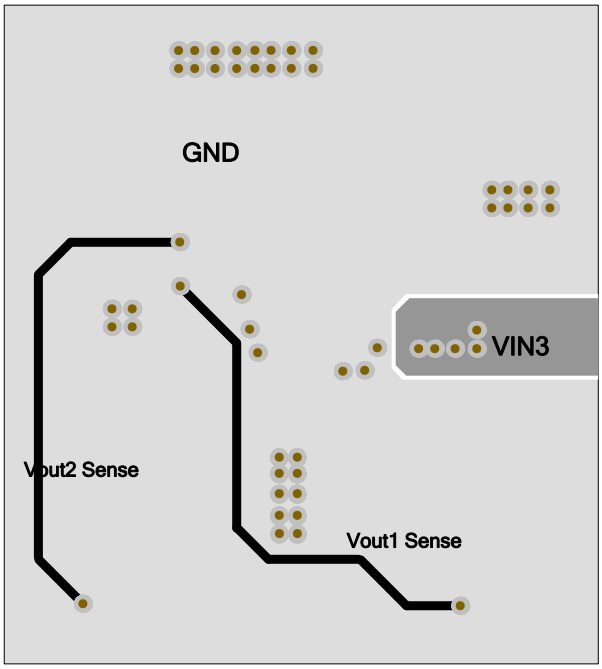
## PCB Layout Guidelines

Efficient PCB layout of the switching power supplies is critical for stable operation. If the layout is not done carefully, regarding the high switching frequency converter especially, the regulator could show poor line or load regulation and stability issues. For best results, refer to Figure 6 and follow the guideline below.

1. Place the input capacitor as close to the IC pins as possible for the high-speed step-down regulator to provide clean control voltage.




**Top Layer**




**Bottom Layer**

**Figure 6: Recommended PCB Layout**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# TYPICAL APPLICATION CIRCUITS

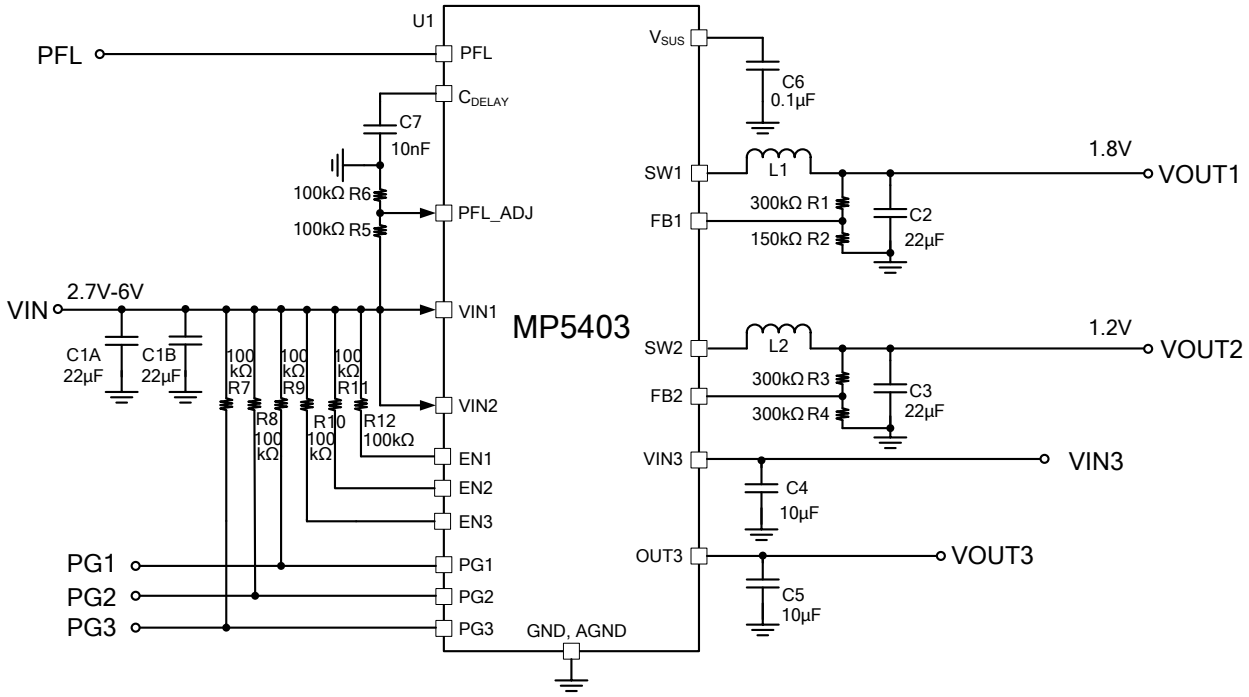


**Figure 7: Typical System Architecture Using 2 Units**

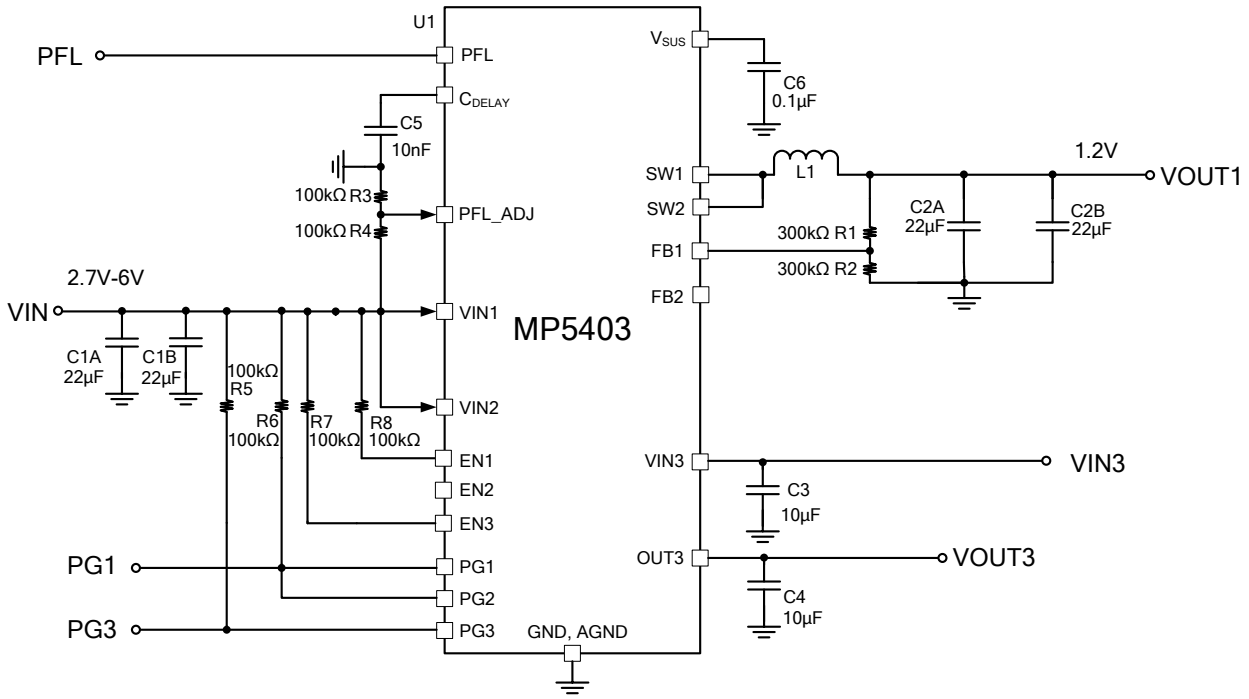


**Figure 8: Typical System Architecture Using Parallel**


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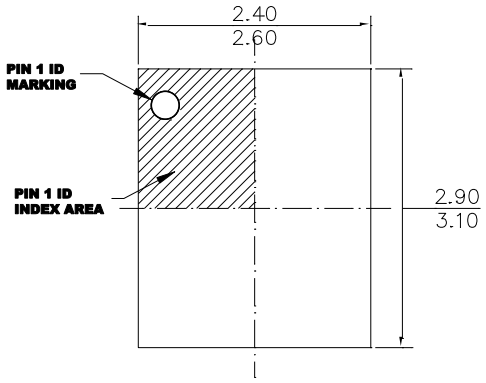
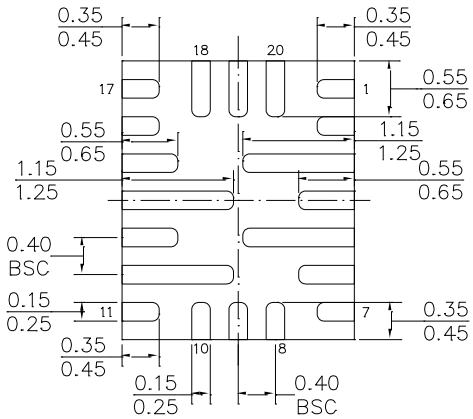
# PACKAGE INFORMATION

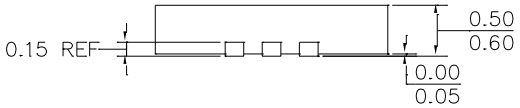
## UTQFN-20 (2.5mmx3mm)



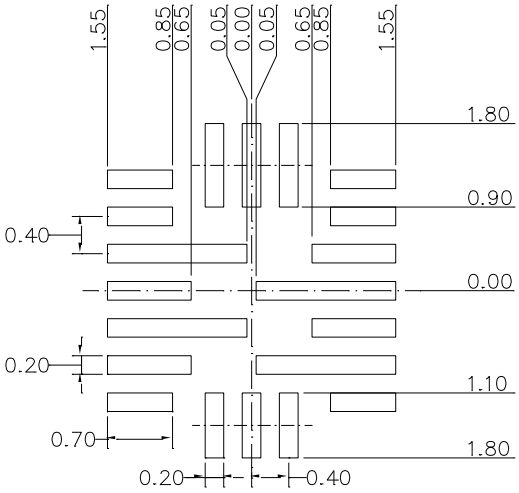

**TOP VIEW**




**BOTTOM VIEW**




**SIDE VIEW**




**RECOMMENDED LAND PATTERN**

**NOTE:**

**1) LAND PATTERN OF PIN3,5,12 AND 14 HAVE THE SAME LENGTH AND WIDTH.**
**2) LAND PATTERN OF PIN4,6,13 AND 15 HAVE THE SAME LENGTH AND WIDTH.**
**3)ALL DIMENSIONS ARE IN MILLIMETERS.**
**4) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.**
**5) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.**
**6) DRAWING CONFIRMS TO JEDEC MO-220.**
**7) DRAWING IS NOT TO SCALE.**

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