MP020A-5

Offline, Primary-Side Regulator with CC/CV Control and a 700V MOSFET

The Future of Analog IC Technology®

DESCRIPTION

The MP020A-5 is an offline, primary-side regulator that provides accurate constant voltage and constant current regulation without an optocoupler or a secondary feedback circuit. The MP020A-5 has an integrated 700V MOSFET.

The MP020A-5's variable off-time control allows a flyback converter to operate in discontinuous conduction mode (DCM). The MP020A-5 also features protection functions such as VCC under-voltage lockout (UVLO), over-current protection (OCP), over-temperature protection (OTP), open-circuit protection (OCkP), and over-voltage protection (OVP). Its internal high-voltage start-up current source and power-saving technologies limit the no-load power consumption to less than 30mW.

The MP020A-5's variable switching frequency technology provides natural spectrum shaping to smooth the EMI signature, making it suitable for offline, low-power battery chargers and adapters.

The MP020A-5 is available in a SOIC8-7A package.

Part Number	$R_{DS(ON)}$	Maximum Output Power (85 - 265V_{AC})	
		Adapter	Open Frame
MP020A-5GS	10Ω	5W	8W

FEATURES

- Primary-Side Control without Optocoupler or Secondary Feedback Circuit
- Precise Constant Current and Constant Voltage Control (CC/CV)
- Integrated 700V MOSFET with Minimal External Components
- Variable Off Time, Peak-Current Control
- 550µA High-Voltage Current Source
- 30mW No-Load Power Consumption
- Programmable Cable Compensation
- OVP, OCP, OCkP, OTP, and VCC UVLO
- Natural Spectrum Shaping for Improved EMI Signature
- Low Cost and Simple External Circuit
- Available in a SOIC8-7A Package

APPLICATIONS

- Cell Phone Chargers
- Adapters for Handheld Electronics
- Standby and Auxiliary Power Supplies
- Small Appliances

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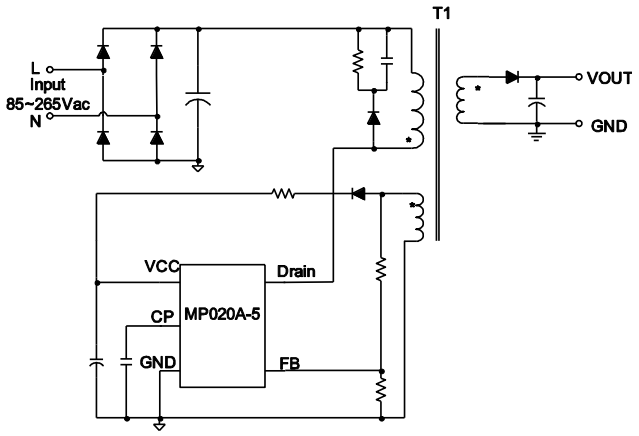
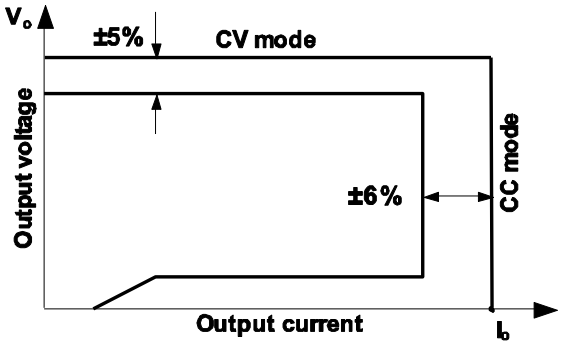
TYPICAL APPLICATION





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ORDERING INFORMATION

Part Number*	Package	Top Marking
MP020A-5GS	SOIC8-7A	*See Below*

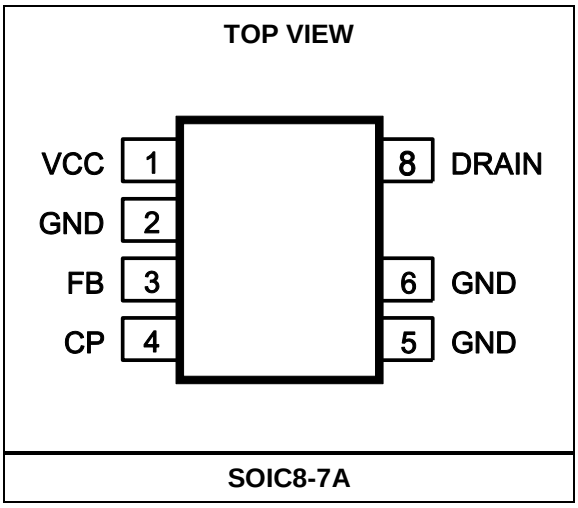
* For Tape & Reel, add suffix –Z (e.g. MP020A-5GS–Z)

TOP MARKING

MP020A-5
LLLLLLLL
MPSYWW

MP020A-5: Product code of MP020A-5GS
LLLLLLLL: Lot number
MPS: MPS prefix
Y: Year code
WW: Week code

PACKAGE REFERENCE



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ABSOLUTE MAXIMUM RATINGS (1)

DRAIN to GND..... -0.7V to 700V
VCC to GND ..... -0.3V to 30V
CP to GND..... -0.3V to 7V
FB input ..... -0.7V to 10V
Continuous power dissipation (T_A = +25°C) (2)
SOIC8-7A 1.3W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature.....-60°C to +150°C
ESD capability human body mode 2.0kV
ESD capability machine mode 200V

Recommended Operating Conditions (3)

Operating junction temp. (T_J). .. -40°C to +125°C
Operating VCC range ..... 6.6V to 28V

Thermal Resistance (4)

	θ_{JA}	θ_{JC}	
SOIC8-7A	76	45	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

VCC = 15V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply Voltage Management (VCC)						
VCC on threshold	V_{CCH}		16.8	17.3	17.8	V
VCC off threshold	V_{CCL}		6	6.3	6.6	V
VCC operating voltage			6.6		28	V
Quiescent current	I_Q	At no load condition, VCC = 20V		360	410	μA
Operating current	I_{OP}	60kHz, VCC = 20V		500		μA
Leakage current from VCC	I_{Leak_VCC}	VCC = 0 → 16V, DRAIN floating		0.1	1	μA
Internal MOSFET (DRAIN)						
Break-down voltage	V_{BRDSS}	VCC = 20V, V_{FB} = 7V	700			V
Supply current from DRAIN	I_{Charge}	VCC = 4V, V_{DRAIN} = 100V	450	550	750	μA
Leakage current from DRAIN	I_{Leak_Drain}	V_{DS} = 500V_{DC}		1	10	μA
On-state resistance	R_{ON}	I_D = 10mA, T_J = 20°C		10	13	Ω
Minimum switching frequency	f_{MIN}	At no load condition		120		Hz
Internal Current Sense						
Current limit	I_{Limit}	V_{FB} = -0.5V	365	380	395	mA
Leading-edge blanking	t_{LEB}		230	300	370	ns
Feedback Input (FB)						
FB input current	I_{FB}	V_{FB} = 4V, V_{CP} = 3V	10	14	18	μA
FB threshold	V_{FB}		3.93	4	4.07	V
DCM detect threshold	V_{DCM}		80	120	160	mV
FB open-circuit threshold	V_{FBOPEN}		-0.22	-0.15	-0.08	V
FB OVP threshold	V_{FBOVP}		6.2	6.35	6.5	V
OVP sample delay	t_{OVP}			3.5		μs
Output Cable Compensation (CP)						
Cable compensation voltage	V_{CP}	Full load		2		V
Thermal Shutdown						
Thermal shutdown threshold				150		°C
Thermal shutdown recovery threshold				120		°C

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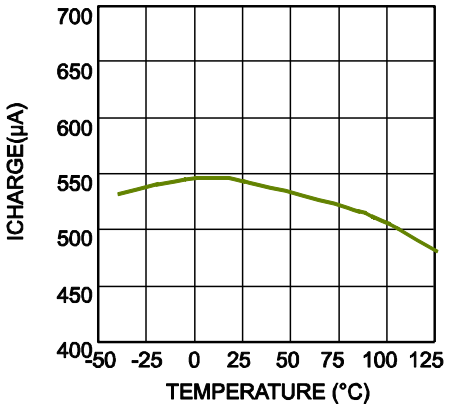
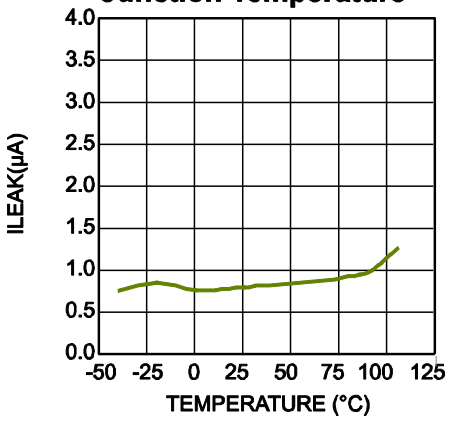
TYPICAL CHARACTERISTICS

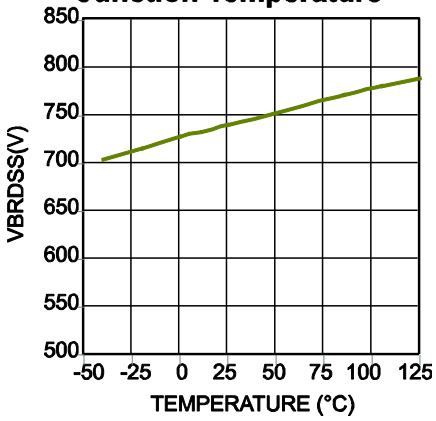
Charge Current vs. Junction Temperature



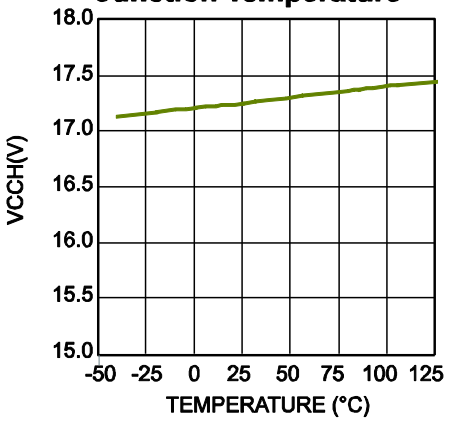
Leakage Current vs. Junction Temperature



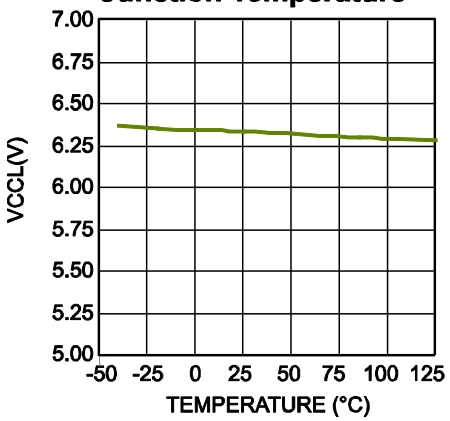
Breakdown Voltage vs. Junction Temperature



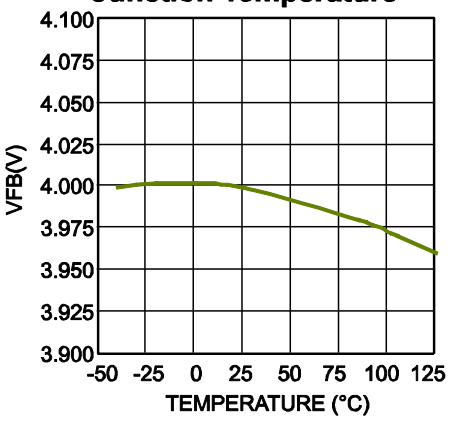
VCC ON Threshold vs. Junction Temperature



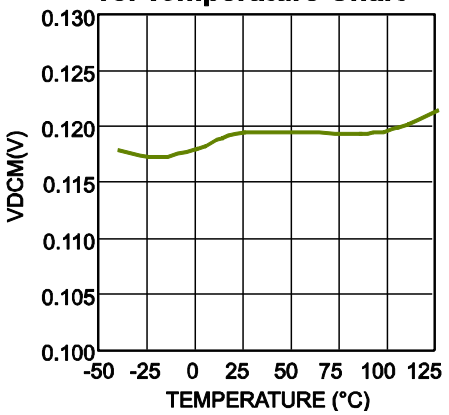
VCC OFF Threshold vs. Junction Temperature



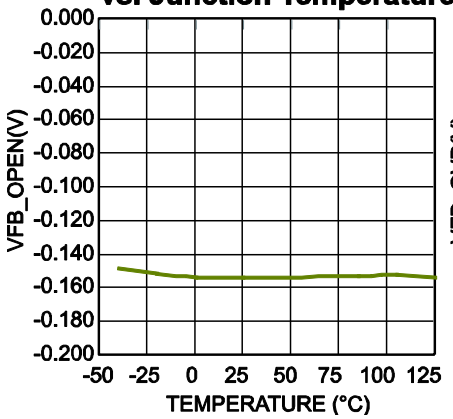
Feedback Threshold vs. Junction Temperature



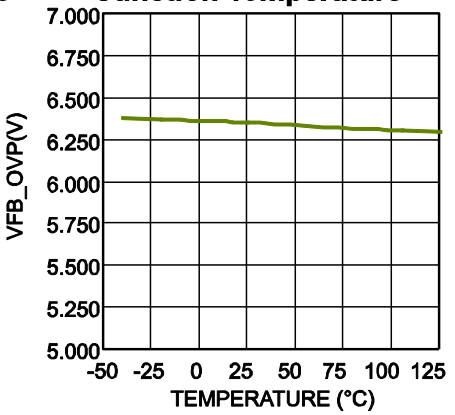
DCM Detect Threshold vs. Temperature Chart



FB Open Circuit Threshold vs. Junction Temperature



FB OVP Threshold vs. Junction Temperature



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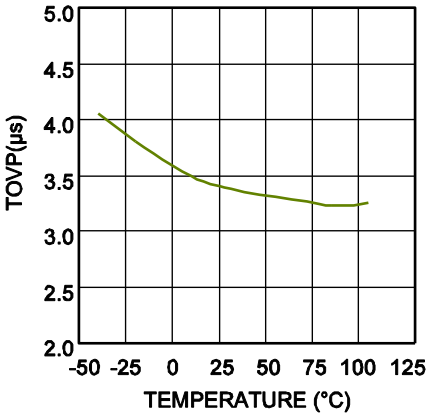
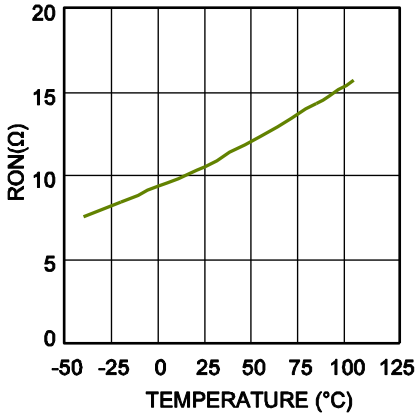
TYPICAL CHARACTERISTICS *(continued)*

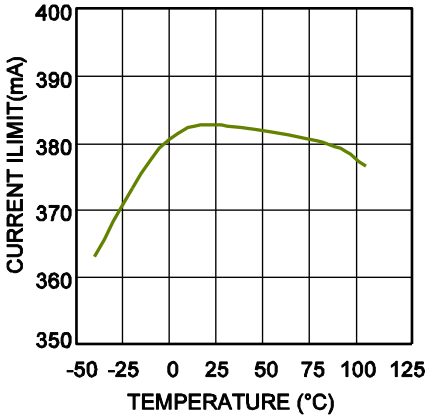
OVP Sample Delay vs. Junction Temperature



On State Resistance vs. Junction Temperature



Current I_{Limit} vs. Junction Temperature



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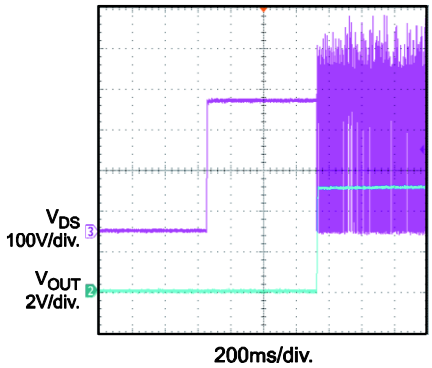
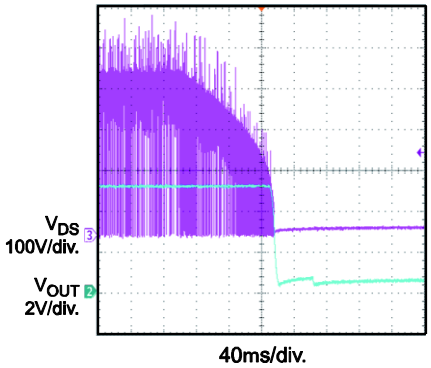
TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board in the Design Example section.
V_{IN} = 230V_{AC}, V_{OUT} = 5V, I_{OUT} = 1A, L = 1.6mH, T_A = 25°C, unless otherwise noted.

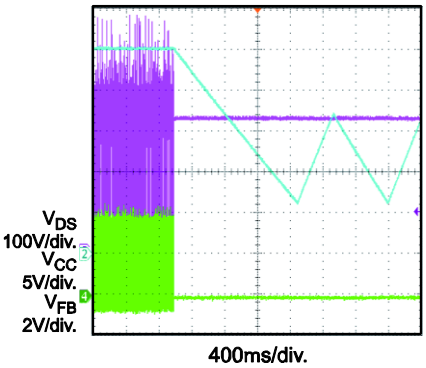
Input Power Start-Up



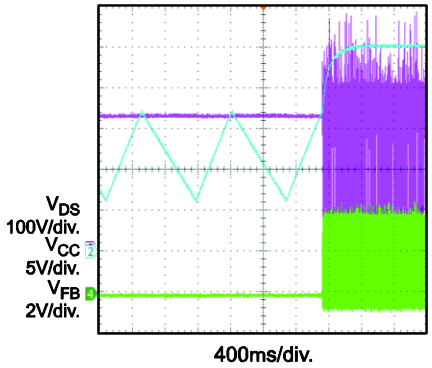
Input Power Shutdown



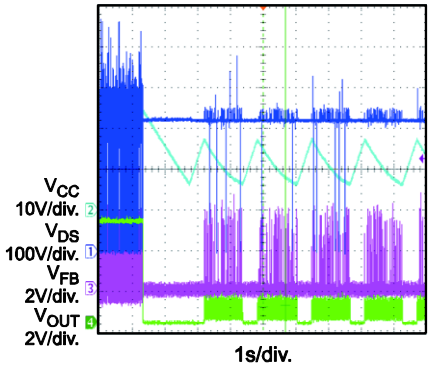
OCkP Entry



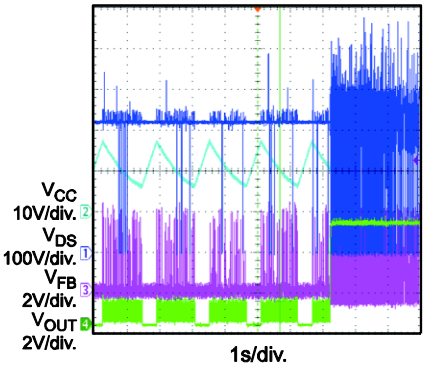
OCkP Recovery



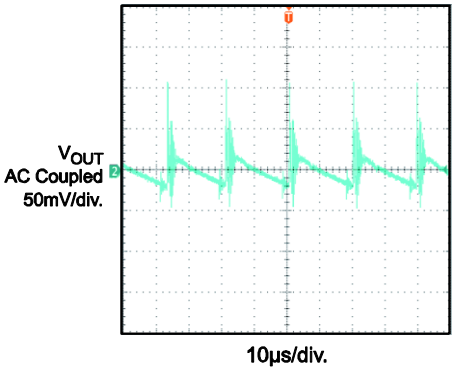
OVP Entry



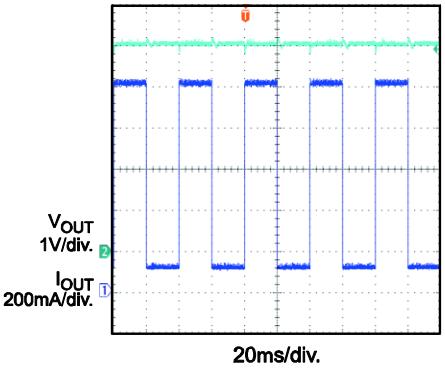
OVP Recovery



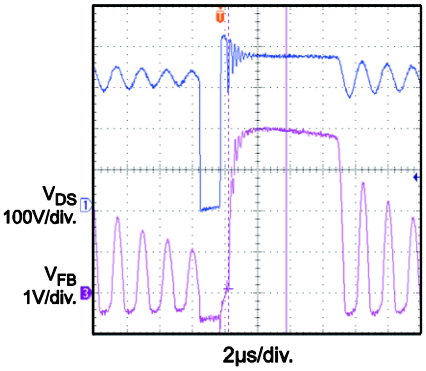
Output Voltage Ripple



Load Transient



Normal Operation



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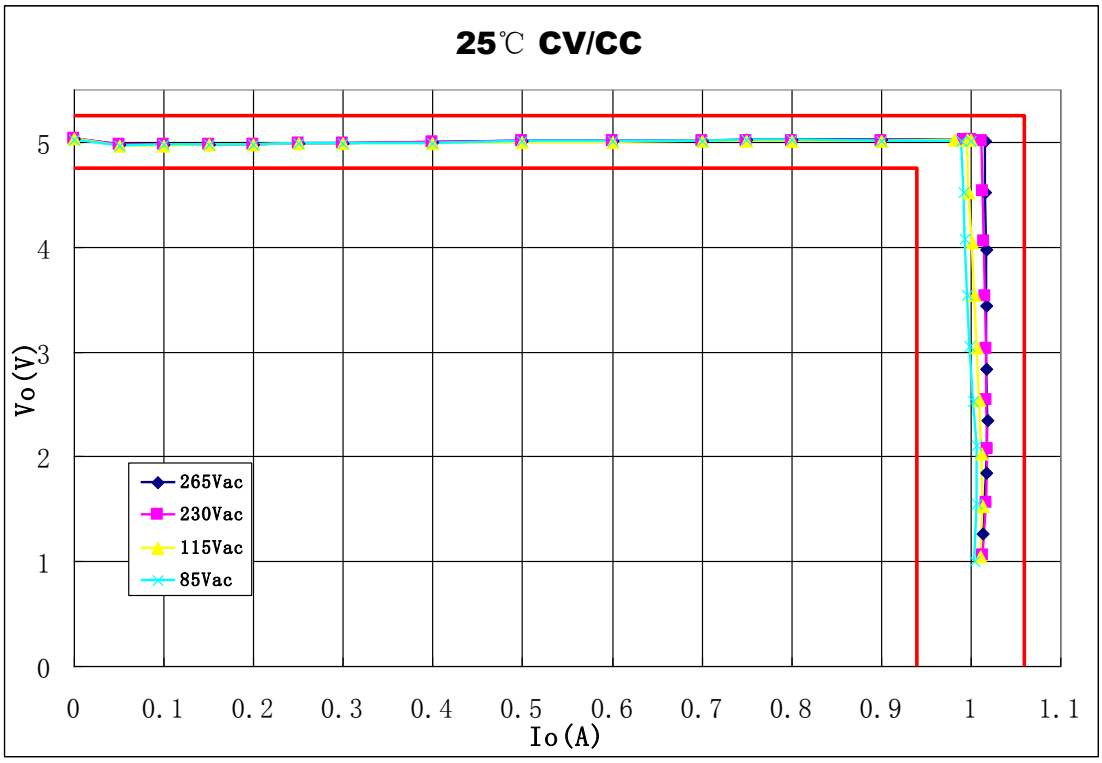
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board in the Design Example section.
V_{IN} = 230V_{AC}, V_{OUT} = 5V, I_{OUT} = 1A, L = 1.6mH, T_A = 25°C, unless otherwise noted.

MP020A-5 CV/CC Characteristics



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PIN FUNCTIONS

SOIC8-7A Pin #	Name	Description
1	VCC	**Supply.** The IC begins functioning when VCC charges to the on threshold (V_{CCH}) through an internal high-voltage current source. When VCC falls below the off threshold (V_{CCL}), the internal high-voltage current source turns on to charge VCC. Connect a 0.1µF decoupling ceramic capacitor for most applications.
2, 5, 6	GND	**Ground.**
3	FB	**Feedback.** FB provides the output reference voltage and detects the falling voltage edges to determine the operation mode (CV mode or CC mode).
4	CP	**Output cable compensation.** Connect a 1µF ceramic capacitor as a low pass filter. The upper resistor of the resistor divider connected to FB adjusts the compensation voltage.
8	DRAIN	**Internal MOSFET drain.** DRAIN is the input for the high-voltage start-up current source.

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BLOCK DIAGRAM

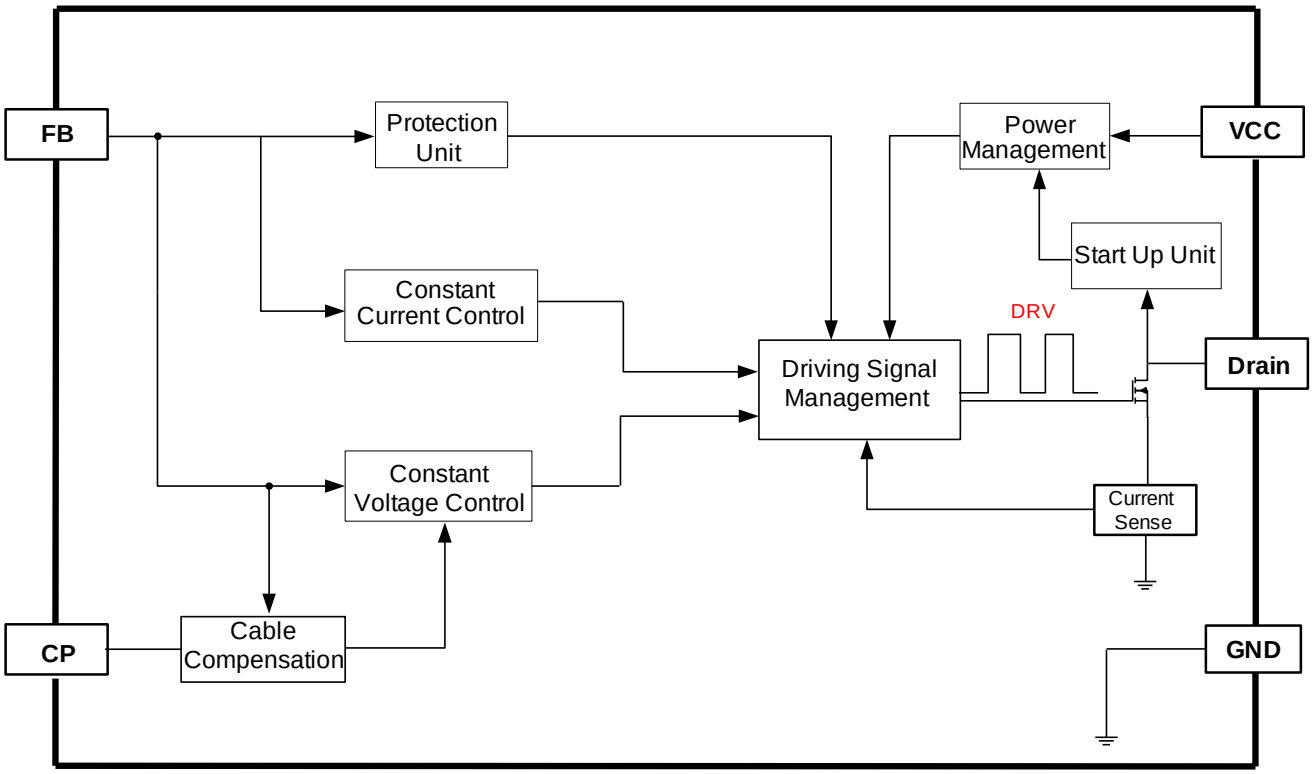

Figure 1: Functional Block Diagram

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OPERATION

Start-Up

Initially, the IC is self-supplying through an internal high-voltage current source, which is drawn from DRAIN. The internal high-voltage current source turns off for better efficiency when VCC reaches its on threshold (V_{CCH}). Then the transformer's auxiliary winding takes over as the power source. When VCC falls below its off threshold (V_{CCL}), the IC stops switching, and the internal high-voltage current source turns on again (see Figure).

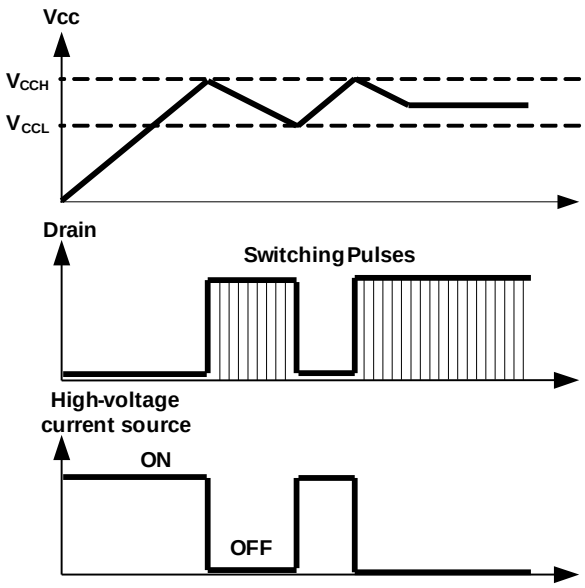

Figure 2: VCC UVLO

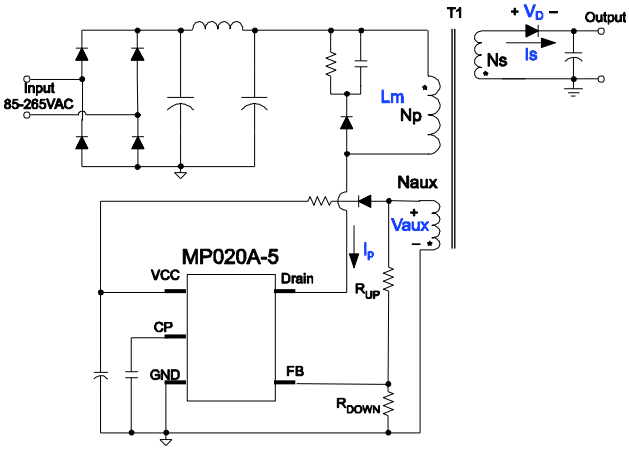

Figure 3: Simplified Flyback Converter

Working Principle

After start-up, the internal MOSFET turns on, and the current sense resistor (R_{CS}) senses the primary current ($i_P(t)$) internally (see Figure 3). The current rises linearly at a rate that can be calculated with Equation (1):

$$\frac{di_P(t)}{dt} = \frac{V_{IN}}{L_M} \quad (1)$$

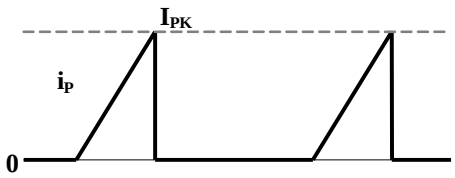

Figure 1: Primary Current Waveform

When $i_P(t)$ rises up to I_{PK}, the internal MOSFET turns off (see Figure 4). Then the energy stored in the inductor transfers to the secondary side through the transformer.

The inductor (L_M) stores energy with each cycle as a function shown in Equation (2):

$$E = \frac{1}{2} L_M \times I_{PK}^2 \quad (2)$$

The power transferred from the input to the output can be determined with Equation (3):

$$P = \frac{1}{2} L_M \times I_{PK}^2 \times f_S \quad (3)$$

Where f_S is the switching frequency. When I_{PK} is constant, the output power depends on f_S.

Constant Voltage (CV) Operation

The MP020A-5 detects the auxiliary winding voltage from FB and operates in constant voltage (CV) mode to regulate the output voltage. Assume the secondary winding is the master and the auxiliary winding is the slave. When the secondary-side diode turns on, the FB voltage can be calculated with Equation (4):

$$V_{FB} = \frac{N_{P_AU}}{N_S} \times (V_O + V_D) \times \frac{R_{DOWN}}{R_{UP} + R_{DOWN}} \quad (4)$$

Where V_D is the secondary-side diode forward-drop voltage, Vo is the output voltage, N_{P_AU} is the number of auxiliary winding turns, N_S is the number of secondary side winding turns, and R_{UP} and R_{DOWN} are the resistor divider for sampling.

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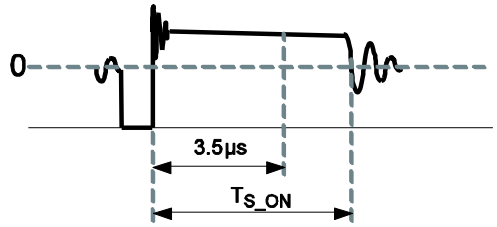

Figure 2: Auxiliary Voltage Waveform

The output voltage differs from the secondary voltage due to the current-dependent forward-diode voltage drop. If the secondary voltage is always detected at a fixed secondary current, the difference between the output voltage and the secondary voltage is a fixed V_D. The MP020A-5 samples the auxiliary winding voltage 3.5µs after the primary switch turns off (see Figure 5). The CV loop control function turns the secondary-side diode off to regulate the output voltage.

Constant Current (CC) Operation

Figure 3 shows the constant-current operation.

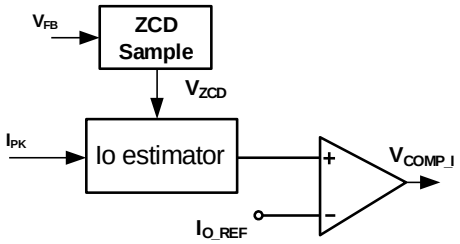

Figure 3: CC Control Loop

The flyback always works in discontinuous conduction mode (DCM), and the zero-current detection (ZCD) sample block can detect the duty cycle of the secondary-side diode.

In constant current (CC) operation, the product of V_{ZCD} times I_{pk} approximately equals I_{O_REF}, as shown in Equation (5):

$$I_{O_REF} = V_{ZCD} \times I_{PK} \quad (5)$$

The calculated output current from the I_O estimator block is compared with the reference value (I_{O_REF}), and the error signal (V_{COMP_I}) controls the turn-on signal of the integral MOSFET. I_O can be calculated with Equation (6):

$$I_O = \frac{1}{2} \times \frac{N_P}{N_S} \times I_{O_REF} \quad (6)$$

The MP020A-5 maintains I_{O_REF} at 0.152A.

Leading-Edge Blanking

The parasitic capacitances induce a spike on the sense resistor when the power switch turns on. The MP020A-5 includes a 300ns leading-edge blanking period to avoid falsely terminating the switching pulse. During this blanking period, the current sense comparator is disabled, and the gate driver cannot switch off (see Figure 4).

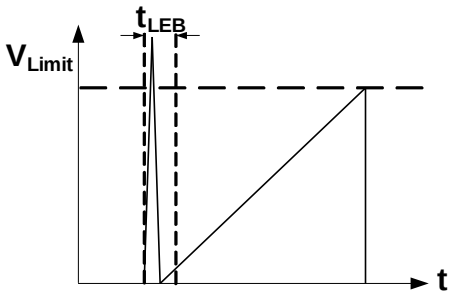

Figure 4: Leading-Edge Blanking

DCM Detection

The MP020A-5 operates in DCM in both CV and CC modes. To avoid operating in continuous conduction mode (CCM), the MP020A-5 detects the falling edge of the FB input voltage with each cycle. If the chip does not detect a 120mV falling edge, it stops switching.

OVP and OCkP

The MP020A-5 includes over-voltage protection (OVP) and open-circuit protection (OCkP). If the voltage at FB exceeds 6.35V for 3.5µs, or the FB input's 0.15V falling edge cannot be monitored, the MP020A-5 immediately shuts off the driving signals and enters hiccup mode. The MP020A-5 resumes normal operation when the fault has been removed.

Thermal Shutdown

When the temperature of the IC exceeds 150°C, over-temperature protection (OTP) is triggered, and the IC enters auto-recovery mode. When the temperature falls below 120°C, the IC recovers.

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Output Cable Compensation

To compensate for the secondary-side cable voltage drop for a more precise output voltage, the MP020A-5 has an internal output cable compensation circuit (see Figure 5). The internal ZCD sample can detect the duty of the secondary-side diode. A low-pass filter converts the duty signal to a DC voltage (V_{CP}) that changes as the load current varies.

V_{CP} can be converted to a current signal drawn from FB. The voltage drop on R_{UP} helps the output cable compensation. When the system operates in the maximum load, the CP voltage reaches a maximum of 2V.

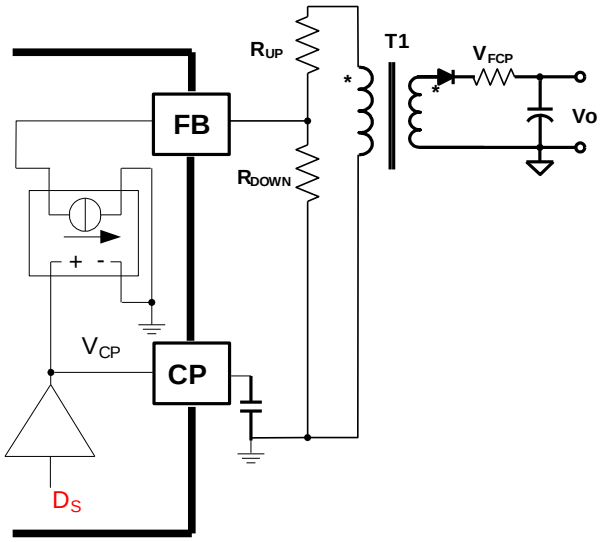

Figure 5: Output Cable Compensator

Determine the compensation voltage with Equation (7):

$$V_{FCP} = \frac{5.6 \times D_S}{360 \times 10^3} \times 2 \times R_{UP} \times \frac{N_S}{N_{P_AU}} \quad (7)$$

Where V_{FCP} is the secondary-side compensation voltage drop, D_S is the secondary-diode duty cycle in CC mode (0.4 for the MP020A-5), R_{UP} is the upper resistor of the resistor divider, N_S is the number of turns for the secondary-side transformer windings, and N_{P_AU} is the number of transformer auxiliary winding turns.

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APPLICATION INFORMATION

Input Filter

The input filter helps convert the AC input to a DC source through the rectifier. Figure 6 shows the input filter, and Figure 7 shows the typical DC bus voltage waveform.

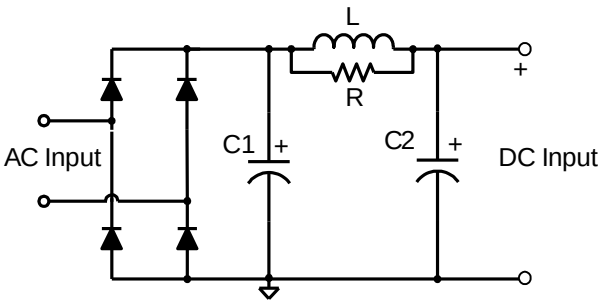

Figure 6: Input Filter

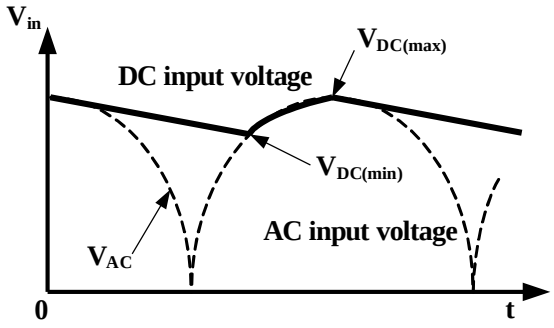

Figure 7: DC Input Voltage Waveform

Bulk capacitors (C1 and C2) filter the rectified AC input. The inductor (L) forms a π filter with C1 and C2 to restrain the differential mode EMI noise. The resistor (R) parallel with L restrains the mid-frequency band EMI noise. Normally, R is 1 - 10kΩ.

C1 and C2 are usually set as 2µF/W to 3µF/W for the universal input condition. For $230V_{AC}$ single-range applications, halve the capacitor values. Avoid using very low minimum DC voltages to ensure that the converter can supply the maximum power load, which can be calculated with Equation (8):

$$V_{DC(min)} \geq \frac{N_P}{N_S} \cdot (V_O + V_D) \cdot \frac{D_S}{1 - D_S} \qquad (8)$$

If $V_{DC(min)}$ cannot satisfy this expression, increase the value of the input capacitors to increase $V_{DC(min)}$.

Output Capacitor

Use low ESR or very low ESR output capacitors to meet the output voltage ripple requirement without using an LC post filter. Using low ESR capacitors improves output voltage regulation and feedback voltage sampling at high temperatures or low temperatures. Use an output capacitor with an ESR below 100mΩ for better efficiency over high ESR output capacitors.

Output Diode

Use a Schottky diode because of its fast switching speed and low forward-voltage drop for better high- or low-temperature CV regulation and efficiency.

If the lower average efficiency (3% to 4%) is sufficient, replace the output diode with a fast or ultra-fast diode to reduce costs. Be sure to readjust the resistor divider values to the correct output voltage because the forward voltage drop is higher than the Schottky diode's.

Leakage Inductance

The transformer's leakage inductance decreases the system efficiency and affects the output current or voltage constant precision. Optimize the transformer structure to minimize the leakage inductance. Aim for a leakage inductance less than 5% of the primary inductance.

RCD Snubber

The transformer's leakage inductance causes the MOSFET drain voltage to spike and excessive ringing on the drain voltage waveform, which affects the output voltage sampling 3.5µs after the MOSFET turns off.

The RCD snubber circuit can limit the DRAIN voltage spike. Figure 8 shows the RCD snubber circuit.

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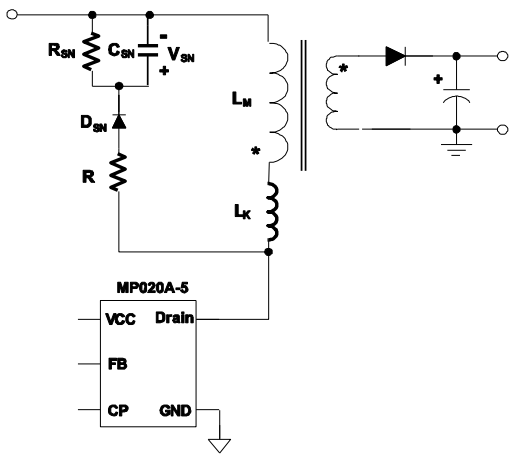

Figure 8: RCD Snubber

Select R_{SN} and C_{SN} to meet the voltage spike requirements and improve system operation.

The power dissipated in the snubber circuit can be approximated with Equation (9):

$$P_{SN} = \frac{1}{2} \cdot L_K \cdot I_{PK}^2 \cdot \frac{V_{SN}}{V_{SN} - N_{PS} \times V_O} \times f_S \qquad (9)$$

Where L_K is the leakage inductance, V_{SN} is the clamp voltage, and N_{PS} is the turn ratio of primary and secondary side.

Since R_{SN} consumes the majority of the power, R_{SN} is approximated with Equation (10):

$$R_{SN} = \frac{V_{SN}^2}{P_{SN}} \qquad (10)$$

The maximum ripple of the snubber capacitor voltage can then be calculated with Equation (11):

$$\Delta V_{SN} = \frac{V_{SN}}{C_{SN} \cdot R_{SN} \cdot f_S} \qquad (11)$$

Generally, a 15% ripple is reasonable, so C_{SN} can be estimated with Equation (11) as well.

Normally, select a time constant ($\tau = R_{SN} \times C_{SN}$) below 0.1ms for better CV sampling. Adjust the resistor based on the power loss and the acceptable clamp voltage in practical applications.

The damping resistor in series with the RCD has a relatively large value to prevent any excessive voltage ringing that can affect the CV sampling and increase the output ripple. Use a 200 - 500Ω damping resistor to restrain the drain-voltage ringing.

Divided Resistor

For better application performance, select the resistor divider's total value to be between 40 - 100kΩ. Smaller resistors draw larger currents from the auxiliary winding, which increases the no-load consumption. Larger resistors may also pick up noise from adjacent components.

If necessary, use a resistor between 1kΩ and 2kΩ connected between the FB and resistor divider. R_{FB} can also limit substrate injection current effects (see Figure 9).

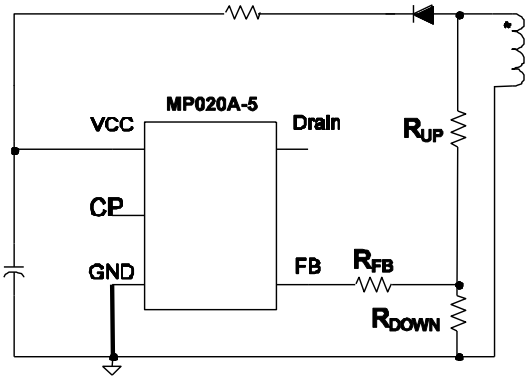

Figure 9: Feedback Resistor Divider Circuit

For more accurate CV regulation, the accuracy of these feedback resistors should be at least 1%.

Dummy Load

When the system operates without a load and no dummy load, the output voltage rises above the normal operation because of the minimum switching frequency limitation. Use a dummy load for good load regulation. However, a large dummy load deteriorates efficiency and no-load consumption, so selecting the dummy load is tradeoff between efficiency and load regulation. For most applications, use a dummy load around 10mW, which satisfies the 30mW requirement.

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Maximum Switching Frequency

Use a secondary-side diode conduction time that exceeds 5.4µs, as shown in Equation (12):

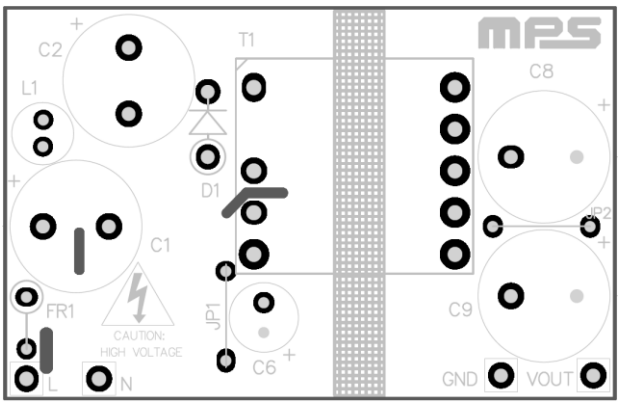
$$T_{S_ON} = I_{PK} \cdot \frac{N_S \cdot L_M}{N_P \cdot (V_O + V_D)} > 5.4\mu s \quad (12)$$

For high- or low-temperature applications, select a maximum switching frequency below 75kHz.

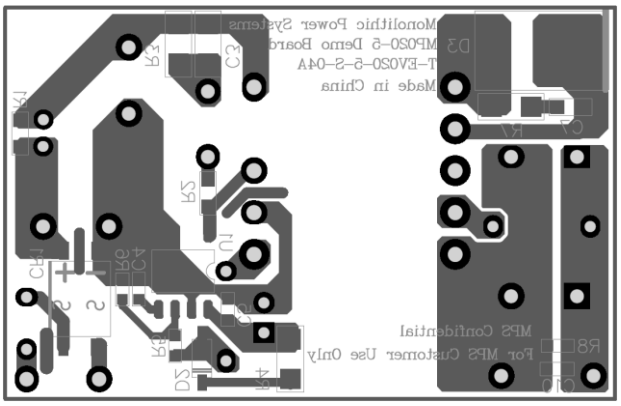
PCB Layout Guide

Efficient PCB layout is critical for reliable operation, good EMI, and good thermal performance. For best results, refer to Figure 10 and follow the guidelines below.

1. Minimize the loop area formed by the input capacitor, the MP020A-5 drain-source, and the primary winding to reduce EMI noise.
2. Provide at least 1in^2 of top-side copper for adequate heat-sinking.
3. The copper area connected to GND is the heat conduction path for the MP020A-5.
4. Minimize the clamp circuit loop to reduce EMI.
5. Minimize the secondary loop area of the output diode and output filter to reduce EMI noise.
6. Provide sufficient copper area at the anode and cathode terminal of the output diode to act as a heat sink.
7. Place the AC input away from the switching nodes to minimize the noise coupling that may bypass the input filter.
8. Place the bypass capacitor as close as possible to the IC and source.
9. Place the feedback resistors next to FB.
10. Minimize the feedback sampling loop to minimize noise coupling.
11. Use a single-point connection at the negative terminal of the input filter capacitor for the MP020A-5 source pin and bias winding return.



Top Layer



Bottom Layer

Figure 10: Recommended Layout

Design Example

Table 1 shows a design example following the application guidelines based the specifications below.

Table 1: Design Example

V_{IN}	85 ~ 265V_{AC}
V_{OUT}	5V
I_{OUT}	1A
f_S	60kHz

Figure 14 through Figure 16 show the detailed application schematic. This circuit was used for the typical performance and circuit waveforms. For more device applications, please refer to the related evaluation board datasheets.

The transformer structure used in Figure 14 can benefit from passing the 3-wire conducted EMI test (output GND connect to earth) without the Y-cap. The Y-cap results in leakage current, which is prohibited in some cell phone charger applications. Figure 15 illustrates how the common noise of the secondary-side diode is restrained. The secondary-side winding splits to two separate windings (N_{SEC1} and N_{SEC2}), which

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have the same turns and approximate parasitic capacitors (C_{SP1} and C_{SP2}), but their hot spot is opposite (Point 9 and Point 10 in Figure 15). Therefore, the common mode noise current produced at the secondary-side windings can counteract each other.

The transformer structure is simple if the application does not need to pass the 3-wire conducted EMI or uses a Y-cap. Figure 16 shows a schematic with a simple transformer structure.

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TYPICAL APPLICATION CIRCUITS

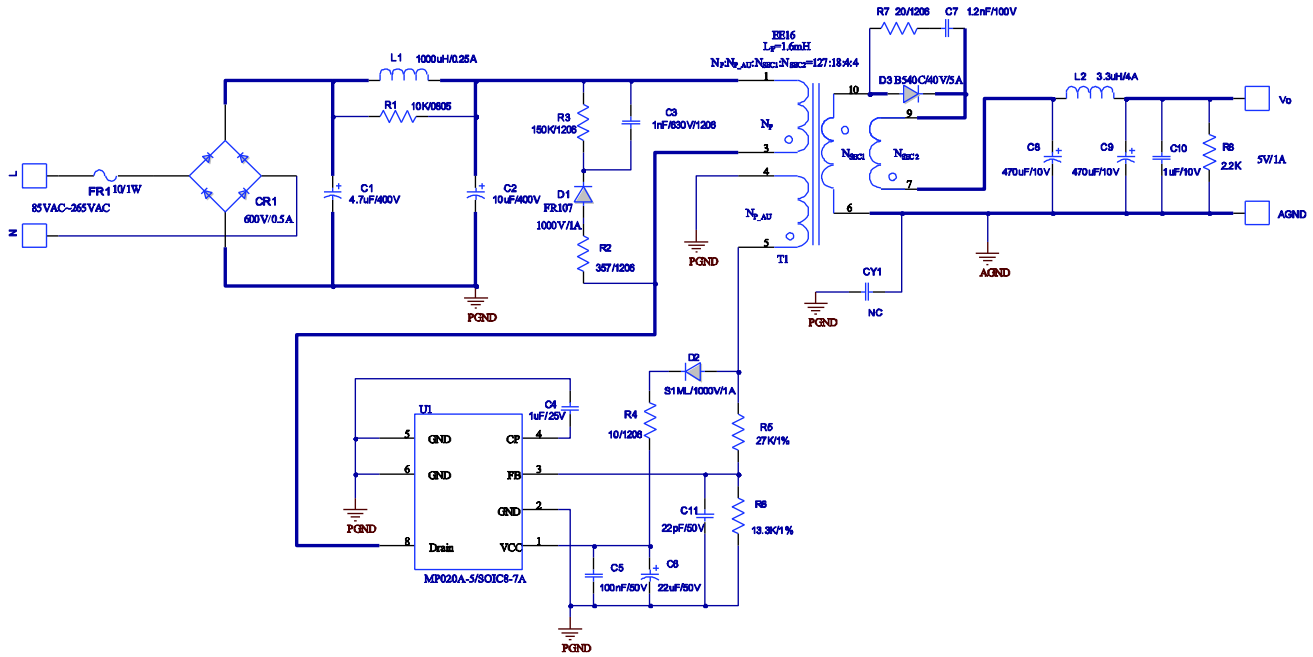

Figure 11: 5V/1A with Complicated Transformer Structure

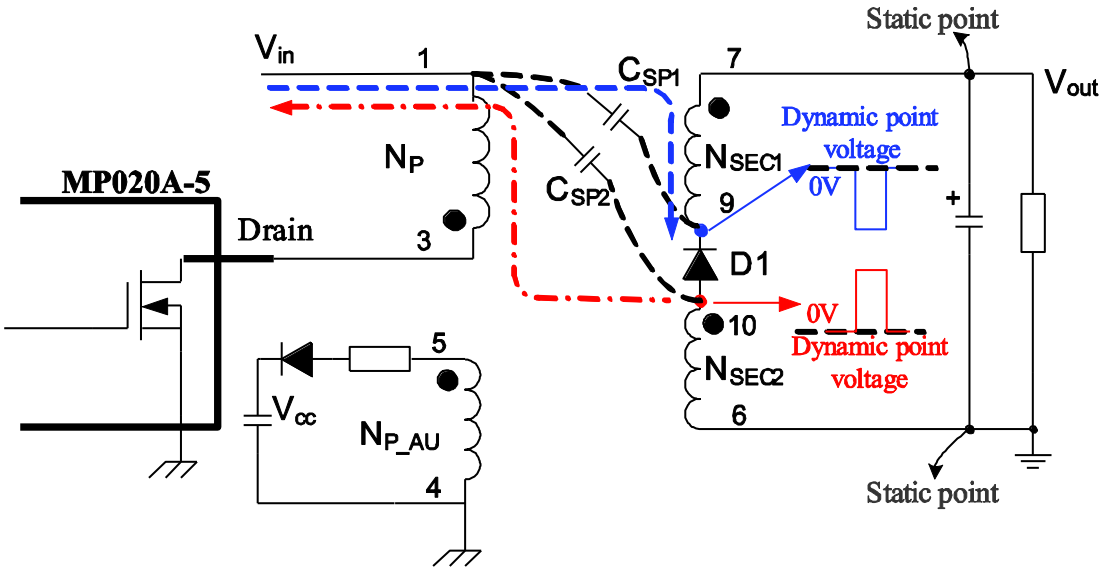

Figure 15: Secondary Side Windings Structure to Restrain the Common Mode Noise

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TYPICAL APPLICATION CIRCUITS

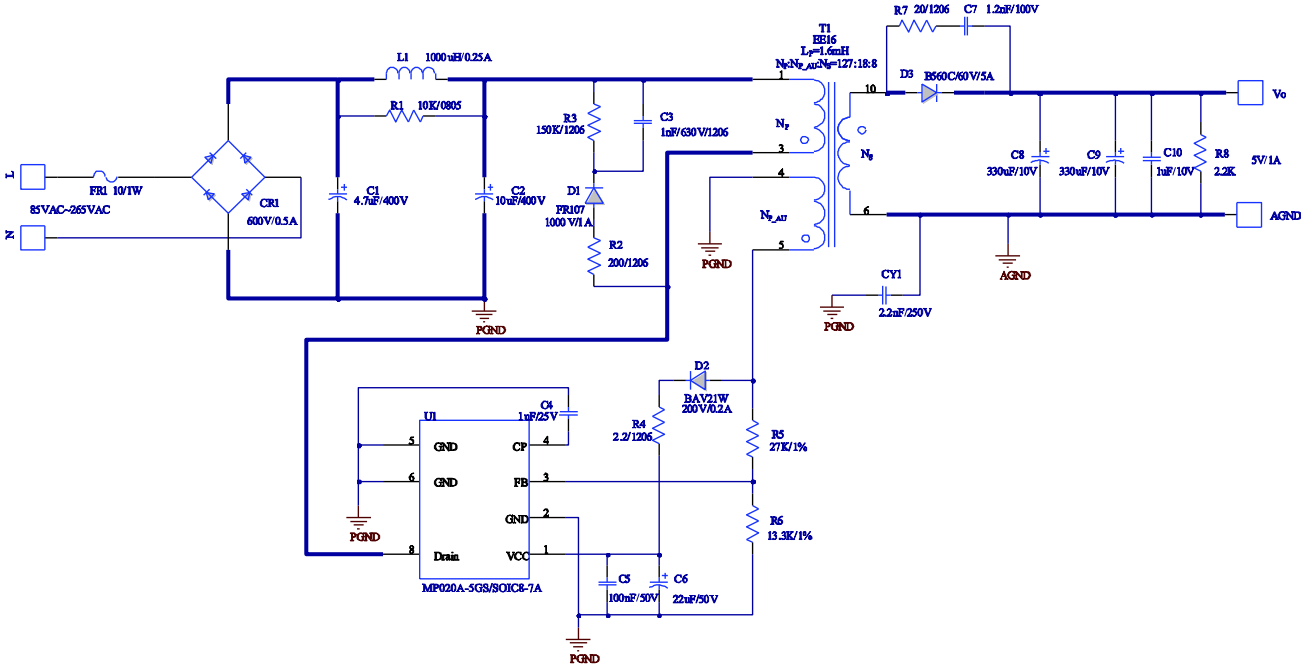

Figure 16: 5V/1A with Simple Transformer Structure

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FLOW CHART

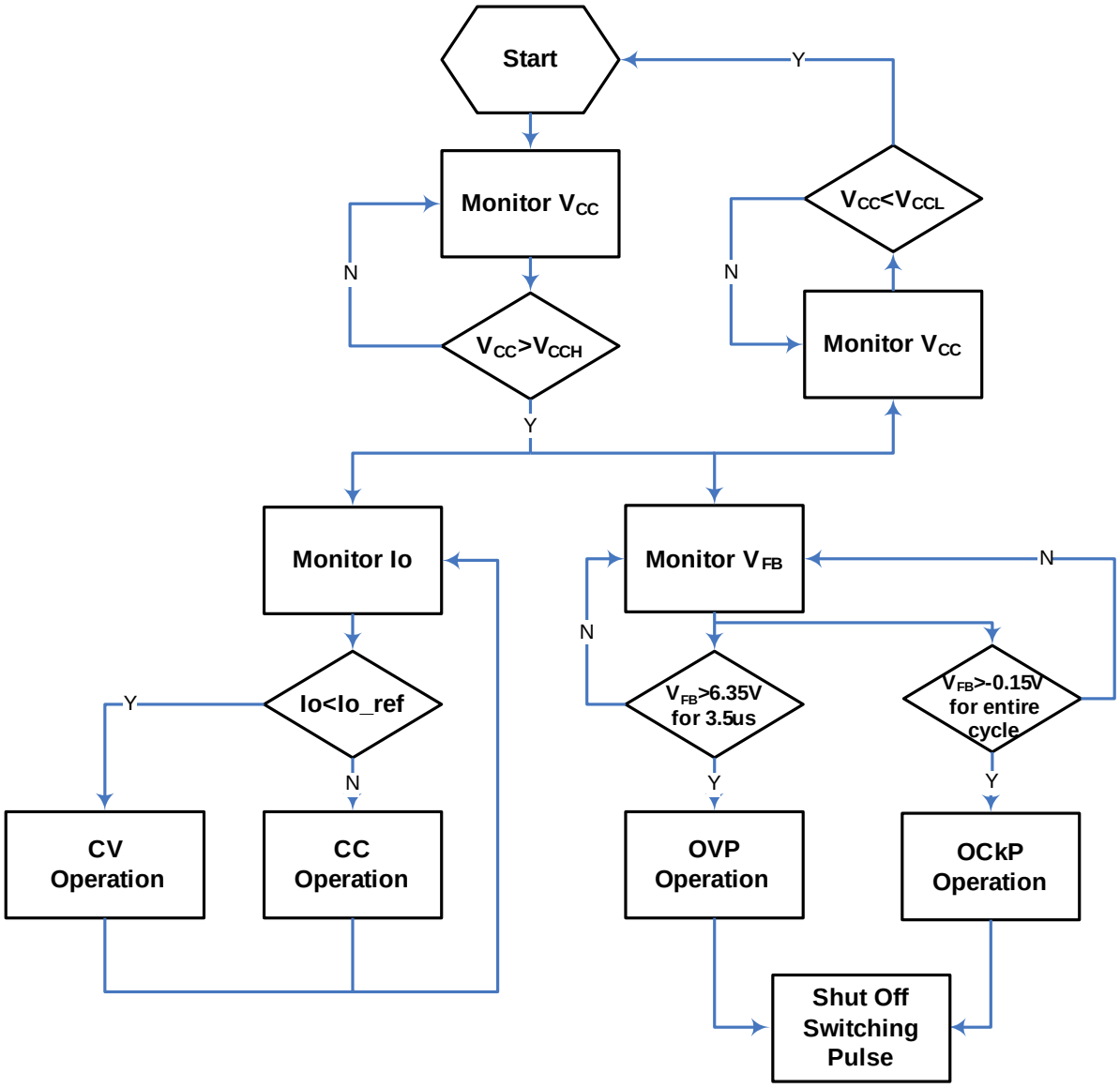

Figure 17: Flow Chart

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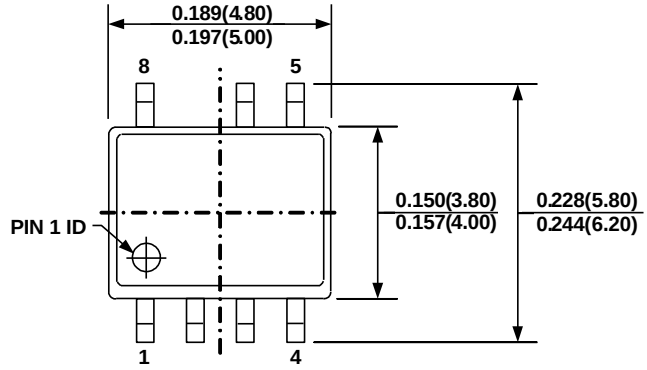
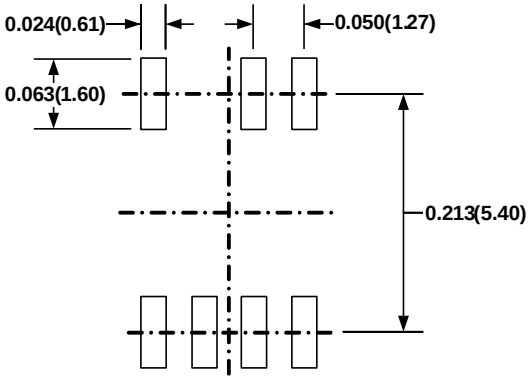
PACKAGE INFORMATION

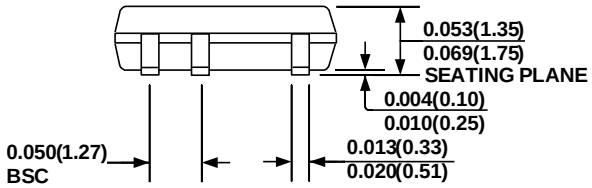
SOIC8-7A



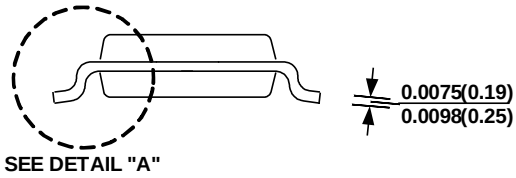
TOP VIEW



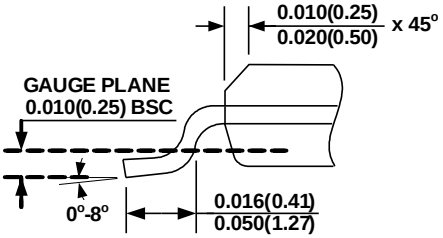
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) JEDEC REFERENCE IS MS-012.
6) DRAWING IS NOT TO SCALE.

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