Freescale Semiconductor
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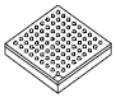
P4080/P4081 QorIQ Integrated Processor Hardware Specifications



FC-PBGA–1295
37.5 mm x 37.5 mm

The P4080/P4081 QorIQ integrated communication processor combines eight Power Architecture® processor cores with high-performance data path acceleration logic and network and peripheral bus interfaces required for networking, telecom/datacom, wireless infrastructure, and mil/aerospace applications.

This chip can be used for combined control, data path, and application layer processing in routers, switches, base station controllers, and general-purpose embedded computing. Its high level of integration offers significant performance benefits compared to multiple discrete devices, while also greatly simplifying board design.

This chip includes the following function and features:

- Eight e500-mc Power Architecture cores, each with a backside 128 KB L2 cache with ECC
  - Three levels of instructions: user, supervisor, and hypervisor
  - Independent boot and reset
  - Secure boot capability
- CoreNet fabric supporting coherent and non-coherent transactions amongst CoreNet end-points
- A frontside 2 MB L3 Cache with ECC
- CoreNet bridges between the CoreNet fabric the I/Os, data path accelerators, and high and low speed peripheral interfaces
- Two 10-Gigabit Ethernet (XAUI) controllers
- One 10-Gigabit Ethernet (XAUI) controller on P4081
- Eight 1-Gigabit Ethernet controllers
- Two 64-bit DDR2/DDR3 SDRAM memory controllers with ECC
- Multicore programmable interrupt controller (MPIC)
- Four I^2C controllers
- Four 2-pin UARTs or two 4-pin UARTs
- Two 4-channel DMA engines
- Enhanced local bus controller (eLBC)
- Three PCI Express 2.0 controllers/ports
- Two serial RapidIO® 1.2 controllers/ports
- Enhanced secure digital host controller (SD/MMC)
- Enhanced serial peripheral interfaces (eSPI)
- High-speed USB controller (USB 2.0)
  - Host and device support
  - Enhanced host controller interface (EHCI)
  - ULPI interface to PHY
- Data Path Acceleration Architecture (DPAA) incorporating acceleration for the following functions:
  - Frame manager (FMan) for packet parsing, classification, and distribution
  - Queue manager (QMan) for scheduling, packet sequencing, and congestion management
  - Hardware buffer manager (BMan) for buffer allocation and de-allocation
  - Encryption/decryption (SEC 4.0)
  - Regex pattern matching (PME 2.0)
- 1295 FC-PBGA package

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Table of Contents

1 Pin Assignments and Reset States 3
1.1 1295 FC-PBGA Ball Layout Diagrams 3
1.2 Pinout List 9
2 Electrical Characteristics 52
2.1 Overall DC Electrical Characteristics 52
2.2 Power Sequencing 57
2.3 Power Down Requirements. 59
2.4 Power Characteristics 59
2.5 Thermal. 62
2.6 Input Clocks 63
2.7 RESET Initialization 65
2.8 Power-on Ramp Rate 66
2.9 DDR2 and DDR3 SDRAM Controller 66
2.10 eSPI 74
2.11 DUART 76
2.12 Ethernet: Data Path Three-Speed Ethernet (dTSEC), Management Interface 1 and 2, IEEE Std 1588™ 77
2.13 USB. 84
2.14 Enhanced Local Bus Interface 87
2.15 Enhanced Secure Digital Host Controller (eSDHC) . . .92
2.16 Programmable Interrupt Controller (PIC) Specifications94
2.17 JTAG Controller. 95
2.18 I^2C. 97
2.19 GPIO 100
2.20 High-Speed Serial Interfaces (HSSI). 101
3 Hardware Design Considerations 129
3.1 System Clocking 129
3.2 Supply Power Setting 137
3.3 Power Supply Design 139
3.4 Decoupling Recommendations 140
3.5 SerDes Block Power Supply Decoupling Recommendations. 140
3.6 Connection Recommendations 141
3.7 Recommended Thermal Model 149
3.8 Thermal Management Information 149
4 Package Information 151
4.1 Package Parameters for the P4080/P4081 FC-PBGA 151
4.2 Mechanical Dimensions of the P4080/P4081 FC-PBGA 152
5 Security Fuse Processor. 153
6 Ordering Information 153
6.1 Part Numbering Nomenclature 153
6.2 Orderable Part Numbers Addressed by This Document 154
7 Revision History 156

This figure shows the major functional units within the chip.

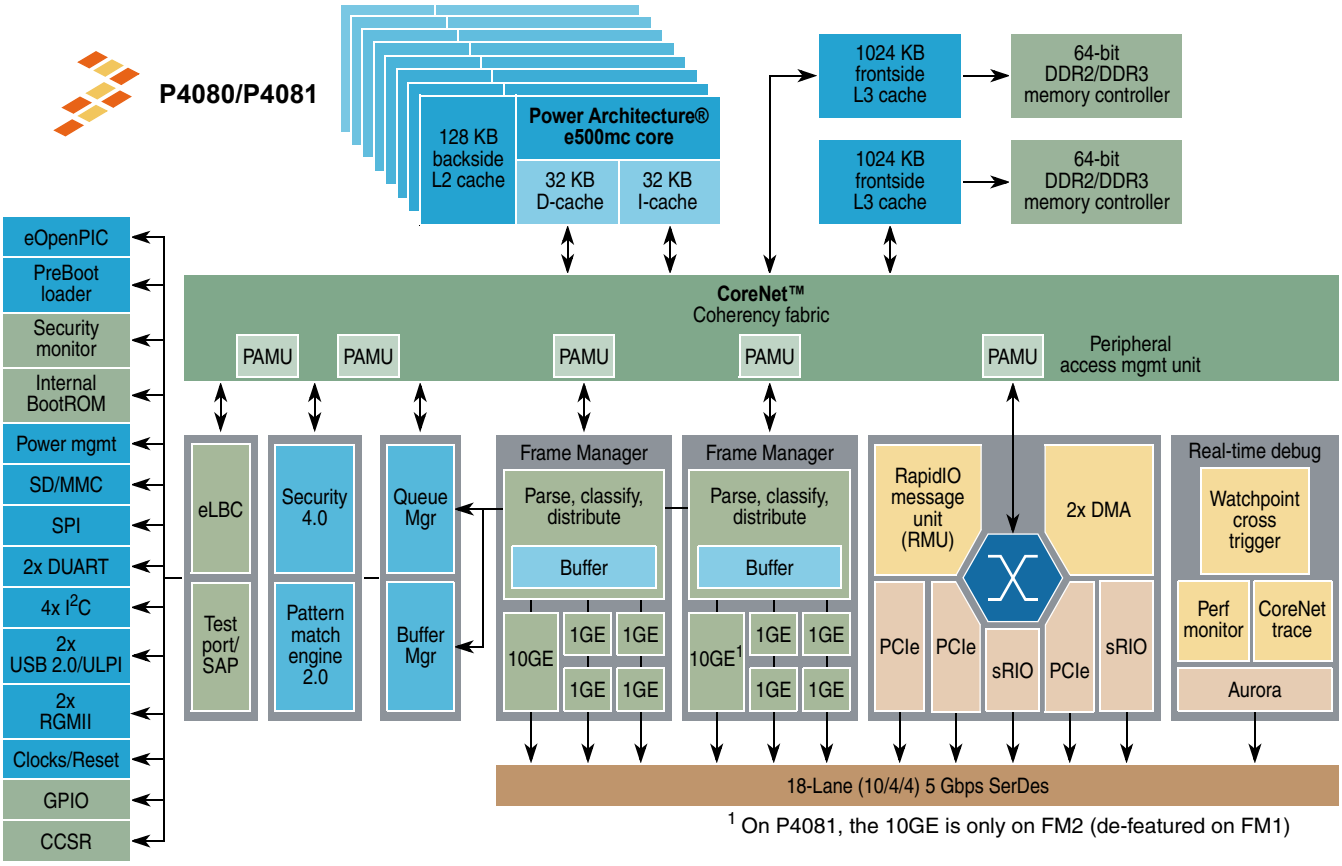
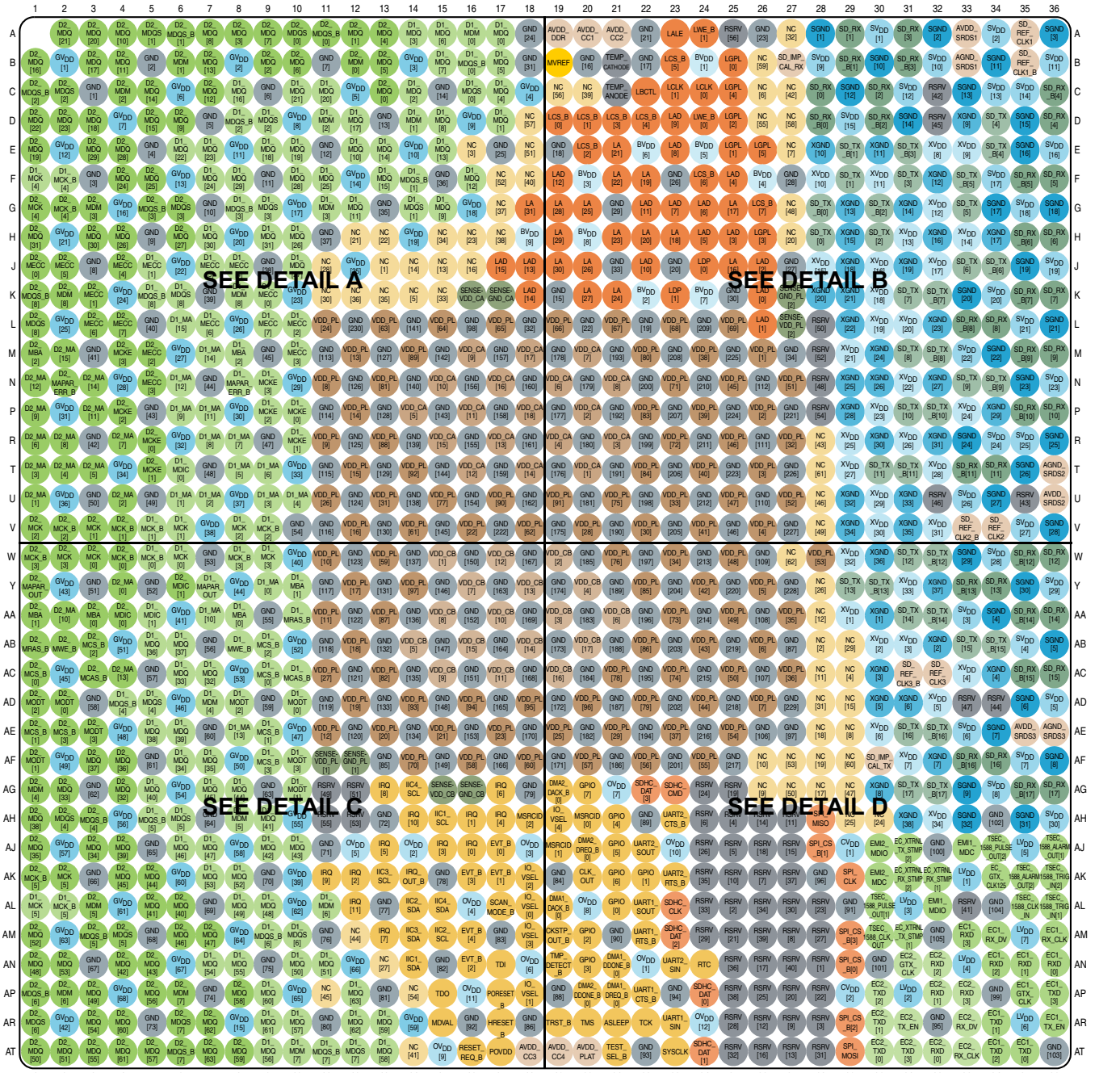


Figure 1. P4080/P4081 QorIQ Preliminary Block Diagram

1 Pin Assignments and Reset States

1.1 1295 FC-PBGA Ball Layout Diagrams

These figures show the FC-PBGA ball map.



Signal Groups

OV_{DD}	I/O Supply Voltage	SV_{DD}	SerDes Core Power Supply	AVDD_SRDS1	SerDes 1 PLL Supply Voltage	SENSE-VDD_CA	Core Group A Voltage Sense
LV_{DD}	I/O Supply Voltage	XV_{DD}	SerDes Transcvr Pad Supply	AVDD_SRDS2	SerDes 2 PLL Supply Voltage	SENSE-VDD_CB	Core Group B Voltage Sense
GV_{DD}	DDR DRAM I/O Supply	VDD_PL	Platform Supply Voltage	AVDD_PLAT	Platform PLL Supply Voltage	RSRV	Reserved
CV_{DD}	SPI Voltage Supply	VDD_CA	Core Group A Supply Voltage	AVDD_CC	Core PLL Supply Voltage	POVDD	Fuse Programming Override Supply
BV_{DD}	Local Bus I/O Supply	VDD_CB	Core Group B Supply Voltage	SENSE-VDD_PL	Platform Voltage Sense		

Figure 2. 1295 BGA Ball Map Diagram (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
A		D2_MDQ [21]	D2_MDQ [20]	D2_MDQ [10]	D2_MDQS [1]	D2_MDQS_B [1]	D2_MDQ [8]	D2_MDQ [3]	D2_MDQ [7]	D2_MDQS [0]	D2_MDQS_B [0]	D2_MDQ [1]	D2_MDQ [4]	D1_MDQ [3]	D1_MDQ [6]	D1_MDM [0]	D1_MDQ [0]	GND [24]
B	D2_MDQ [16]	GV_{DD} [1]	D2_MDQ [17]	D2_MDQ [11]	GND [2]	D2_MDM [1]	D2_MDQ [13]	GV_{DD} [2]	D2_MDQ [2]	D2_MDQ [6]	GND [7]	D2_MDM [0]	D2_MDQ [5]	GV_{DD} [3]	D1_MDQ [7]	D1_MDQS_B [0]	D1_MDQ [5]	GND [31]
C	D2_MDQS_B [2]	D2_MDQS [2]	GND [1]	D2_MDM [2]	D2_MDQ [14]	GV_{DD} [6]	D2_MDQ [12]	D1_MDQ [16]	GND [6]	D1_MDQ [21]	D1_MDQ [20]	GV_{DD} [5]	D2_MDQ [0]	D1_MDQ [2]	GND [14]	D1_MDQS [0]	D1_MDQ [4]	GV_{DD} [4]
D	D2_MDQ [22]	D2_MDQ [23]	D2_MDQ [18]	GV_{DD} [7]	D2_MDQ [15]	D2_MDQ [9]	GND [5]	D1_MDQS_B [2]	D1_MDQS [2]	GV_{DD} [8]	D1_MDM [2]	D1_MDQ [17]	GND [13]	D1_MDM [1]	D1_MDQ [8]	GV_{DD} [9]	D1_MDQ [1]	NC [57]
E	D2_MDQ [19]	GV_{DD} [12]	D2_MDQ [29]	D2_MDQ [28]	GND [4]	D1_MDQ [22]	D1_MDQ [23]	GV_{DD} [11]	D1_MDQ [18]	D1_MDQ [19]	GND [12]	D1_MDQ [10]	D1_MDQ [14]	GV_{DD} [10]	D1_MDQ [13]	NC [3]	GND [25]	NC [51]
F	D1_MCK [4]	D1_MCK_B [4]	GND [3]	D2_MDQ [24]	D2_MDQ [25]	GV_{DD} [13]	D1_MDQ [24]	D1_MDQ [29]	GND [11]	D1_MDQ [28]	D1_MDQ [25]	GV_{DD} [14]	D1_MDQ [15]	D1_MDQS_B [1]	GND [36]	D1_MDQ [12]	NC [52]	NC [40]
G	D2_MCK [4]	D2_MCK_B [4]	D2_MDM [3]	GV_{DD} [16]	D2_MDQS_B [3]	D2_MDQS [3]	GND [10]	D1_MDQS_B [3]	D1_MDQS [3]	GV_{DD} [17]	D1_MDM [3]	D1_MDQ [11]	GND [35]	D1_MDQS [1]	D1_MDQ [9]	GV_{DD} [18]	NC [37]	LA [31]
H	D2_MDQ [31]	GV_{DD} [21]	D2_MDQ [30]	D2_MDQ [26]	GND [9]	D2_MDQ [27]	D1_MDQ [30]	GV_{DD} [20]	D1_MDQ [31]	D1_MDQ [26]	GND [37]	NC [21]	NC [22]	GV_{DD} [19]	NC [34]	NC [23]	NC [38]	BV_{DD} [9]
J	D2_MECC [0]	D2_MECC [5]	GND [8]	D2_MECC [4]	D1_MECC [1]	GV_{DD} [22]	D1_MECC [5]	D1_MECC [4]	GND [38]	D1_MDQ [27]	NC [28]	GV_{DD} [35]	NC [1]	NC [14]	NC [13]	NC [16]	LAD [15]	LAD [13]
K	D2_MDQS_B [8]	D2_MDM [8]	D2_MECC [1]	GV_{DD} [24]	D1_MDQS_B [8]	D1_MDQS [8]	GND [39]	D1_MDM [8]	D1_MECC [0]	GV_{DD} [23]	NC [30]	NC [36]	NC [35]	NC [5]	NC [33]	SENSE-VDD_CA	SENSE-GND_CA	LAD [14]
L	D2_MDQS [8]	GV_{DD} [25]	D2_MECC [6]	D2_MECC [7]	GND [40]	D1_MA [15]	D1_MECC [6]	GV_{DD} [26]	D1_MECC [7]	D1_MECC [2]	VDD_PL [24]	GND [230]	VDD_PL [63]	GND [141]	VDD_PL [64]	GND [98]	VDD_PL [65]	GND [32]
M	D2_MBA [2]	D2_MA [15]	GND [41]	D2_MCKE [3]	D2_MECC [2]	GV_{DD} [27]	D1_MA [14]	D1_MBA [2]	GND [45]	D1_MECC [3]	GND [113]	VDD_PL [13]	GND [127]	VDD_PL [89]	GND [142]	VDD_CA [9]	GND [157]	VDD_CA [17]
N	D2_MA [12]	D2_MAPAR_ERR_B	D2_MA [14]	GV_{DD} [28]	D2_MECC [3]	D1_MA [12]	GND [44]	D1_MAPAR_ERR_B	D1_MCKE [3]	GV_{DD} [29]	VDD_PL [8]	GND [126]	VDD_PL [81]	GND [140]	VDD_CA [10]	GND [156]	VDD_CA [16]	GND [160]
P	D2_MA [9]	GV_{DD} [31]	D2_MA [11]	D2_MCKE [2]	GND [43]	D1_MA [9]	D1_MA [11]	GV_{DD} [30]	D1_MCKE [2]	D1_MCKE [0]	GND [114]	VDD_PL [14]	GND [128]	VDD_CA [5]	GND [143]	VDD_CA [11]	GND [158]	VDD_CA [18]
R	D2_MA [6]	D2_MA [8]	GND [42]	D2_MA [7]	D2_MCKE [0]	GV_{DD} [32]	D1_MA [8]	D1_MA [7]	GND [47]	D1_MCKE [1]	VDD_PL [9]	GND [125]	VDD_PL [88]	GND [139]	VDD_CA [15]	GND [155]	VDD_CA [13]	GND [161]
T	D2_MA [3]	D2_MA [4]	D2_MA [5]	GV_{DD} [34]	D2_MCKE [1]	D1_MDIC [0]	GND [48]	D1_MA [5]	D1_MA [6]	GV_{DD} [33]	GND [115]	VDD_PL [15]	GND [129]	VDD_PL [92]	GND [144]	VDD_CA [12]	GND [159]	VDD_CA [14]
U	D2_MA [1]	GV_{DD} [36]	GND [50]	D2_MA [2]	GND [49]	D1_MA [1]	D1_MA [2]	GV_{DD} [37]	D1_MA [3]	D1_MA [4]	VDD_PL [26]	GND [124]	VDD_PL [31]	GND [138]	VDD_PL [77]	GND [154]	VDD_PL [90]	GND [162]
V	D2_MCK [2]	D2_MCK_B [2]	D2_MCK [1]	D2_MCK [1]	D1_MCK_B [1]	D1_MCK [1]	GV_{DD} [38]	D1_MCK [2]	D1_MCK_B [2]	GND [54]	GND [116]	VDD_PL [16]	GND [130]	VDD_PL [61]	GND [145]	VDD_PL [22]	GND [222]	VDD_PL [62]

DETAIL A

Figure 3. 1295 BGA Ball Map Diagram (Detail View A)

	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36
A	AVDD_ DDR	AVDD_ CC1	AVDD_ CC2	GND [21]	LALE	LWE [1]	RSRV [56]	GND [23]	NC [32]	SGND [1]	SD_RX [1]	SV_{DD} [1]	SD_RX [3]	SGND [2]	AVDD_ SRDS1	SV_{DD} [2]	SD_ REF_ CLK1	SGND [3]
B	MVREF	GND [16]	TEMP_ CATHODE	GND [17]	LCS [5]	BV_{DD} [1]	LGPL [0]	NC [59]	SD_IMP_ CAL_RX	SV_{DD} [9]	SD_RX _B[1]	SGND [10]	SD_RX _B[3]	SV_{DD} [10]	AGND_ SRDS1	SGND [11]	SD_ REF_ CLK1_B	SV_{DD} [11]
C	NC [56]	NC [39]	TEMP_ ANODE	LBCTL	LCLK [1]	LCLK [0]	LGPL [4]	NC [6]	NC [42]	SD_RX [0]	SGND [12]	SD_RX [2]	SV_{DD} [12]	RSRV [42]	SGND [13]	SV_{DD} [13]	SV_{DD} [14]	SD_RX _B[4]
D	LCS_B [0]	LCS_B [1]	LCS_B [3]	LCS_B [4]	LAD [9]	LWE_B [0]	LGPL [2]	NC [55]	NC [58]	SD_RX _B[0]	SV_{DD} [15]	SD_RX _B[2]	SGND [14]	RSRV [45]	XGND [9]	SD_TX [4]	SGND [15]	SD_RX [4]
E	GND [18]	LCS_B [2]	LA [21]	BV_{DD} [6]	LAD [8]	BV_{DD} [5]	LGPL [1]	LGPL [5]	NC [7]	XGND [10]	SD_TX _B[1]	XGND [11]	SD_TX _B[3]	XV_{DD} [8]	XV_{DD} [9]	SD_TX _B[4]	SGND [16]	SV_{DD} [16]
F	LAD [12]	BV_{DD} [3]	LA [22]	LA [19]	GND [26]	LCS_B [6]	LAD [4]	BV_{DD} [4]	GND [28]	XV_{DD} [10]	SD_TX [1]	XV_{DD} [11]	SD_TX [3]	XGND [12]	SD_TX _B[5]	SV_{DD} [17]	SD_RX [_B5]	SD_RX [5]
G	LA [28]	LA [25]	GND [29]	LAD [11]	LAD [7]	LAD [6]	LA [17]	LCS_B [7]	NC [48]	SD_TX _B[0]	XGND [13]	SD_TX _B[2]	XGND [14]	XV_{DD} [12]	SD_TX [5]	SGND [17]	SV_{DD} [18]	SGND [18]
H	LA [29]	BV_{DD} [8]	LA [23]	LA [20]	LA [18]	LAD [5]	LAD [3]	LGPL [3]	NC [20]	SD_TX [0]	XGND [15]	SD_TX [2]	XV_{DD} [13]	XGND [16]	XV_{DD} [14]	XGND [17]	SD_RX _B[6]	SD_RX [6]
J	LA [30]	LA [26]	GND [33]	LAD [10]	GND [20]	LDP [0]	LA [16]	LAD [2]	GND [27]	XV_{DD} [15]	XGND [18]	XV_{DD} [16]	XGND [19]	XV_{DD} [17]	SD_TX [6]	SD_TX _B[6]	SGND [19]	SV_{DD} [19]
K	GND [15]	LA [27]	LA [24]	BV_{DD} [2]	LDP [1]	BV_{DD} [7]	GND [30]	LAD [0]	SENSE-GND_PL [2]	XGND [20]	XGND [21]	XV_{DD} [18]	SD_TX [7]	SD_TX _B[7]	SGND [20]	SV_{DD} [20]	SD_RX _B[7]	SD_RX [7]
L	VDD_PL [66]	GND [22]	VDD_PL [67]	GND [19]	VDD_PL [68]	GND [209]	VDD_PL [69]	LAD [1]	SENSE-VDD_PL [2]	RSRV [50]	XGND [22]	XV_{DD} [19]	XV_{DD} [20]	XGND [23]	SD_RX _B[8]	SD_RX [8]	SV_{DD} [21]	SGND [21]
M	GND [178]	VDD_CA [7]	GND [193]	VDD_PL [80]	GND [208]	VDD_PL [38]	GND [225]	VDD_PL [1]	GND [34]	RSRV [52]	XV_{DD} [21]	XGND [24]	SD_TX [8]	SD_TX _B[8]	SV_{DD} [22]	SGND [22]	SD_RX _B[9]	SD_RX [9]
N	VDD_CA [6]	GND [179]	VDD_CA [8]	GND [200]	VDD_PL [71]	GND [210]	VDD_PL [45]	GND [112]	VDD_PL [51]	RSRV [48]	XGND [25]	XGND [26]	XV_{DD} [22]	XGND [27]	SD_TX [9]	SD_TX _B[9]	SGND [23]	SV_{DD} [23]
P	GND [177]	VDD_CA [2]	GND [192]	VDD_PL [83]	GND [207]	VDD_PL [39]	GND [224]	VDD_PL [2]	GND [221]	RSRV [54]	XGND [28]	XV_{DD} [23]	SD_TX [10]	SD_TX _B[10]	XV_{DD} [24]	XGND [29]	SD_RX _B[10]	SD_RX [10]
R	VDD_CA [4]	GND [180]	VDD_CA [3]	GND [199]	VDD_PL [72]	GND [211]	VDD_PL [46]	GND [111]	VDD_PL [32]	NC [43]	XV_{DD} [25]	XGND [30]	XV_{DD} [26]	XGND [31]	SGND [24]	SV_{DD} [24]	SV_{DD} [25]	SGND [25]
T	GND [176]	VDD_CA [1]	GND [191]	VDD_PL [84]	GND [206]	VDD_PL [40]	GND [223]	VDD_PL [3]	GND [226]	NC [61]	XV_{DD} [27]	SD_TX [11]	SD_TX _B[11]	XV_{DD} [28]	SD_RX _B[11]	SD_RX [11]	SGND [26]	AGND_ SRDS2
U	VDD_PL [91]	GND [181]	VDD_PL [75]	GND [198]	VDD_PL [33]	GND [212]	VDD_PL [47]	GND [110]	VDD_PL [52]	NC [46]	XGND [32]	XV_{DD} [29]	XGND [33]	RSRV [46]	SV_{DD} [26]	SGND [27]	RSRV [43]	AVDD_ SRDS2
V	GND [175]	VDD_PL [28]	GND [190]	VDD_PL [30]	GND [205]	VDD_PL [41]	GND [46]	VDD_PL [4]	GND [227]	NC [49]	XGND [34]	XV_{DD} [30]	XGND [35]	XV_{DD} [31]	SD_ REF_ CLK2_B	SD_ REF_ CLK2	SV_{DD} [27]	SGND [28]

DETAIL B

Figure 4. 1295 BGA Ball Map Diagram (Detail View B)

DETAIL C

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
W	D2_ MCK_B [3]	D2_ MCK [3]	D2_ MCK [0]	D2_ MCK_B [0]	D1_ MCK_B [0]	D1_ MCK [0]	GND [53]	D1_ MCK_B [3]	D1_ MCK [3]	GV_{DD} [40]	VDD_PL [10]	GND [123]	VDD_PL [59]	GND [137]	VDD_CB [1]	GND [150]	VDD_CB [12]	GND [167]
Y	D2_ MAPAR_ OUT	GV_{DD} [43]	GND [51]	D2_MA [0]	GND [52]	D2_ MDIC [1]	D1_ MAPAR_ OUT	GV_{DD} [44]	D1_MA [0]	D1_ MBA [1]	GND [117]	VDD_PL [17]	GND [131]	VDD_PL [97]	GND [146]	VDD_CB [7]	GND [163]	VDD_CB [13]
AA	D2_ MBA [1]	D2_MA [10]	D2_ MBA [0]	D2_ MDIC [0]	D1_ MDIC [1]	GV_{DD} [41]	D1_MA [10]	D1_ MBA [0]	GND [55]	D1_ MRAS_B	VDD_PL [11]	GND [122]	VDD_PL [87]	GND [136]	VDD_CB [8]	GND [152]	VDD_CB [10]	GND [169]
AB	D2_ MRAS_B	D2_ MWE_B	D2_ MCS_B [2]	GV_{DD} [51]	D1_ MDQ [36]	D1_ MDQ [37]	GND [56]	D1_ MWE_B	D1_ MCS_B [2]	GV_{DD} [52]	GND [118]	VDD_PL [18]	GND [132]	VDD_CB [5]	GND [147]	VDD_CB [15]	GND [164]	VDD_CB [14]
AC	D2_ MCS_B [0]	GV_{DD} [45]	D2_ MCAS _B	D2_MA [13]	GND [57]	D1_ MDQ [33]	D1_ MDQ [32]	GV_{DD} [53]	D1_ MCS_B [0]	D1_ MCAS_B	VDD_PL [27]	GND [121]	VDD_PL [82]	GND [135]	VDD_CB [9]	GND [151]	VDD_CB [11]	GND [168]
AD	D2_ MODT [2]	D2_ MODT [0]	GND [58]	D1_ MDQS_B [4]	D1_ MDQS [4]	GV_{DD} [46]	D1_ MDM [4]	D1_ MODT [2]	GND [59]	D1_ MODT [0]	GND [119]	VDD_PL [19]	GND [133]	VDD_PL [93]	GND [148]	VDD_PL [94]	GND [165]	VDD_PL [95]
AE	D2_ MCS_B [1]	D2_ MCS_B [3]	D2_ MODT [3]	GV_{DD} [48]	D1_ MDQ [38]	D1_ MDQ [39]	GND [60]	D1_MA [13]	D1_ MCS_B [1]	GV_{DD} [47]	VDD_PL [12]	GND [120]	VDD_PL [20]	GND [134]	VDD_PL [21]	GND [153]	VDD_PL [23]	GND [170]
AF	D2_ MODT [1]	GV_{DD} [49]	D2_ MDQ [37]	D2_ MDQ [36]	GND [61]	D1_ MDQ [34]	D1_ MDQ [35]	GV_{DD} [50]	D1_ MCS_B [3]	D1_ MODT [3]	SENSE- VDD_PL [1]	SENSE- GND_PL [1]	GND [85]	VDD_PL [70]	GND [149]	VDD_PL [58]	GND [166]	VDD_PL [60]
AG	D2_ MDM [4]	D2_ MDQ [33]	GND [62]	D2_ MDQ [32]	D1_ MDQ [40]	GV_{DD} [54]	D1_ MDQ [45]	D1_ MDQ [44]	GND [63]	D1_ MODT [1]	RSRV [49]	RSRV [51]	IRQ [8]	IIC4_ SCL	SENSE- VDD_CB	SENSE- GND_CB	IRQ [6]	GND [79]
AH	D2_ MDQ [38]	D2_ MDQS [4]	D2_ MDQS_B [4]	GV_{DD} [56]	D1_ MDQS_B [5]	D1_ MDQS [5]	GND [64]	D1_ MDM [5]	D1_ MDQ [41]	GV_{DD} [55]	RSRV [55]	RSRV [53]	GND [72]	IRQ [10]	IIC1_ SCL	IRQ [1]	IRQ [4]	MSRCID [2]
AJ	D2_ MDQ [35]	GV_{DD} [57]	D2_ MDQ [34]	D2_ MDQ [39]	GND [65]	D1_ MDQ [46]	D1_ MDQ [47]	GV_{DD} [58]	D1_ MDQ [42]	D1_ MDQ [43]	GND [71]	OV_{DD} [5]	IRQ [5]	OV_{DD} [2]	IRQ [3]	IRQ [0]	EVT_B [0]	OV_{DD} [3]
AK	D2_ MCK_B [5]	D2_ MCK [5]	GND [66]	D2_ MDQ [45]	D2_ MDQ [44]	GV_{DD} [60]	D1_ MDQ [53]	D1_ MDQ [52]	GND [70]	GV_{DD} [39]	IRQ [9]	IRQ [2]	IIC3_ SCL	IRQ_ OUT_B	GND [78]	EVT_B [3]	EVT_B [1]	IO_ VSEL [2]
AL	D1_ MCK [5]	D1_ MCK_B [5]	D2_ MDM [5]	GV_{DD} [61]	D2_ MDQ [41]	D2_ MDQ [40]	GND [69]	D1_ MDQ [49]	D1_ MDQ [48]	GV_{DD} [62]	D1_ MDM [6]	IRQ [11]	GND [77]	IIC2_ SDA	IIC4_ SDA	OV_{DD} [4]	SCAN_ MODE _B	IO_ VSEL [0]
AM	D2_ MDQ [52]	GV_{DD} [63]	D2_ MDQS_B [5]	D2_ MDQS [5]	GND [68]	D2_ MDQ [46]	D2_ MDQ [47]	GV_{DD} [64]	D1_ MDQS_B [6]	D1_ MDQS [6]	GND [76]	NC [44]	IRQ [7]	IIC3_ SDA	IIC2_ SCL	EVT_B [4]	GND [83]	IO_ VSEL [3]
AN	D2_ MDQ [48]	D2_ MDQ [53]	GND [67]	D2_ MDQ [42]	D2_ MDQ [43]	GV_{DD} [67]	D1_ MDQ [54]	D1_ MDQ [55]	GND [75]	D1_ MDQ [50]	D1_ MDQ [51]	GV_{DD} [66]	NC [27]	IIC1_ SDA	GND [82]	EVT_B [2]	TDI	OV_{DD} [6]
AP	D2_ MDQS_B [6]	D2_ MDM [6]	D2_ MDQ [49]	GV_{DD} [68]	D2_ MDQ [56]	D2_ MDM [7]	GND [74]	D2_ MDQ [58]	D1_ MDQ [60]	GV_{DD} [65]	NC [45]	D1_ MDQ [63]	GND [81]	NC [54]	TDO	OV_{DD} [11]	PORESET _B	IO_ VSEL [1]
AR	D2_ MDQS [6]	GV_{DD} [42]	D2_ MDQ [54]	D2_ MDQ [60]	GND [73]	D2_ MDQS [7]	D2_ MDQ [62]	GV_{DD} [15]	D1_ MDQ [61]	D1_ MDQ [57]	GND [80]	D1_ MDQ [62]	D1_ MDQ [59]	GV_{DD} [59]	MDVAL	GND [92]	HRESET _B	GND [86]
AT	D2_ MDQ [50]	D2_ MDQ [51]	D2_ MDQ [55]	D2_ MDQ [61]	D2_ MDQ [57]	D2_ MDQS_B [7]	D2_ MDQ [63]	D2_ MDQ [59]	D1_ MDQ [56]	D1_ MDM [7]	D1_ MDQS_B [7]	D1_ MDQS [7]	D1_ MDQ [58]	NC [41]	OV_{DD} [9]	RESET_ REQ_B	POVDD	AVDD_ CC3

Figure 5. 1295 BGA Ball Map Diagram (Detail View C)

DETAIL D

	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36
W	VDD_CB [2]	GND [185]	VDD_PL [76]	GND [197]	VDD_PL [34]	GND [213]	VDD_PL [48]	GND [109]	NC [62]	VDD_PL [53]	XV_{DD} [32]	XGND [36]	SD_TX [12]	SD_TX _B[12]	SGND [29]	SV_{DD} [28]	SD_RX _B[12]	SD_RX [12]
Y	GND [174]	VDD_CB [4]	GND [189]	VDD_PL [85]	GND [204]	VDD_PL [42]	GND [220]	VDD_PL [5]	GND [228]	NC [26]	SD_TX [13]	SD_TX _B[13]	XV_{DD} [33]	XGND [37]	SD_RX _B[13]	SD_RX [13]	SGND [30]	SV_{DD} [29]
AA	VDD_CB [3]	GND [183]	VDD_CB [6]	GND [196]	VDD_PL [73]	GND [214]	VDD_PL [49]	GND [108]	VDD_PL [35]	NC [12]	XV_{DD} [1]	XGND [1]	SD_TX [14]	SD_TX _B[14]	SV_{DD} [3]	SGND [4]	SD_RX _B[14]	SD_RX [14]
AB	GND [173]	VDD_CB [17]	GND [188]	VDD_PL [86]	GND [203]	VDD_PL [43]	GND [219]	VDD_PL [6]	GND [87]	NC [2]	NC [29]	XV_{DD} [2]	XV_{DD} [3]	XGND [2]	SD_TX [15]	SD_TX _B[15]	SV_{DD} [4]	SGND [5]
AC	VDD_CB [16]	GND [184]	VDD_PL [78]	GND [195]	VDD_PL [74]	GND [215]	VDD_PL [50]	GND [107]	VDD_PL [36]	NC [11]	NC [4]	XGND [3]	SD_ REF_ CLK3_B	SD_ REF_ CLK3	XV_{DD} [4]	XGND [4]	SD_RX _B[15]	SD_RX [15]
AD	GND [172]	VDD_PL [96]	GND [187]	VDD_PL [79]	GND [202]	VDD_PL [44]	GND [218]	VDD_PL [7]	GND [229]	NC [31]	NC [15]	XGND [5]	XGND [6]	XV_{DD} [5]	RSRV [47]	RSRV [44]	SGND [6]	SV_{DD} [5]
AE	VDD_PL [25]	GND [182]	VDD_PL [29]	GND [194]	VDD_PL [37]	GND [216]	VDD_PL [54]	GND [106]	GND [97]	NC [18]	NC [8]	XV_{DD} [6]	SD_TX [16]	SD_TX _B[16]	SV_{DD} [6]	SGND [7]	AVDD_ SRDS3	AGND_ SRDS3
AF	GND [171]	VDD_PL [57]	GND [186]	VDD_PL [56]	GND [201]	VDD_PL [55]	GND [217]	NC [10]	NC [53]	NC [19]	NC [60]	SD_IMP_ CAL_TX	XV_{DD} [7]	XGND [7]	SD_RX _B[16]	SD_RX [16]	SV_{DD} [7]	SGND [8]
AG	DMA2_ DACK_B [0]	GPIO [7]	OV_{DD} [7]	SDHC_ DAT [3]	SDHC_ CMD	RSRV [24]	RSRV [19]	NC [9]	NC [50]	NC [17]	NC [47]	XGND [8]	SD_TX [17]	SD_TX _B[17]	SGND [9]	SV_{DD} [8]	SD_RX _B[17]	SD_RX [17]
AH	IO_ VSEL [4]	MSRCID [0]	GPIO [4]	GND [89]	UART2_ CTS_B	RSRV [6]	RSRV [4]	RSRV [14]	RSRV [11]	SPI_ MISO	NC [25]	NC [24]	XGND [38]	XV_{DD} [34]	SGND [32]	GND [102]	SGND [31]	SV_{DD} [30]
AJ	MSRCID [1]	DMA2_ DREQ_B [0]	GPIO [5]	UART2_ SOUT	OV_{DD} [10]	RSRV [26]	RSRV [5]	RSRV [18]	RSRV [15]	SPI_CS _B[1]	CV_{DD} [1]	EMI2_ MDIO	EC_XTRNL _TX_STMP [2]	GND [100]	EMI1_ MDC	TSEC_ 1588_PULSE _OUT[2]	LV_{DD} [5]	TSEC_ 1588_ALARM _OUT[1]
AK	GND [84]	CLK_ OUT	GPIO [6]	GPIO [1]	UART2_ RTS_B	RSRV [35]	RSRV [10]	RSRV [7]	RSRV [37]	GND [96]	SPI_ CLK	EMI2_ MDC	EC_XTRNL _RX_STMP [2]	EC_XTRNL _RX_STMP [1]	LV_{DD} [1]	EC_ GTX_ CLK125	TSEC_ 1588_ALARM _OUT[2]	TSEC_ 1588_TRIG _IN[2]
AL	DMA1_ DACK_B [0]	OV_{DD} [8]	GPIO [0]	UART1_ SOUT	SDHC_ CLK	RSRV [33]	RSRV [2]	RSRV [34]	RSRV [30]	RSRV [23]	GND [91]	TSEC_ 1588_PULSE _OUT[1]	LV_{DD} [3]	EMI1_ MDIO	RSRV [41]	GND [104]	TSEC_ 1588_CLK _IN	TSEC_ 1588_TRIG _IN[1]
AM	CKSTP_ OUT_B	GPIO [2]	GND [90]	UART1_ RTS_B	SDHC_ DAT [2]	RSRV [29]	RSRV [21]	RSRV [39]	RSRV [8]	RSRV [27]	SPI_CS _B[3]	TSEC_ 1588_CLK_ OUT	EC_XTRNL _TX_STMP [1]	GND [105]	EC1_ RXD [3]	EC1_ RX_DV	LV_{DD} [7]	EC1_ RX_CLK
AN	TMP_ DETECT _B	GPIO [3]	DMA1_ DDONE_B [0]	OV_{DD} [1]	UART2_ SIN	RTC	RSRV [36]	RSRV [17]	RSRV [40]	RSRV [1]	SPI_CS _B[0]	GND [101]	EC2_ GTX_ CLK	EC2_ RXD [2]	LV_{DD} [4]	EC1_ RXD [2]	EC1_ RXD [1]	EC1_ RXD [0]
AP	GND [88]	DMA2_ DDONE_B [0]	DMA1_ DREQ_B [0]	UART1_ CTS_B	GND [94]	SDHC_ DAT [0]	RSRV [38]	RSRV [25]	RSRV [20]	RSRV [22]	CV_{DD} [2]	EC2_ TXD [2]	LV_{DD} [2]	EC2_ RXD [1]	EC2_ RXD [3]	GND [99]	EC1_ GTX_ CLK	EC1_ TXD [3]
AR	TRST_B	TMS	ASLEEP	TCK	UART1_ SIN	OV_{DD} [12]	RSRV [28]	RSRV [12]	RSRV [9]	RSRV [3]	SPI_CS _B[2]	EC2_ TXD [1]	EC2_ TX_EN	GND [95]	EC2_ RX_DV	EC1_ TXD [1]	LV_{DD} [6]	EC1_ TX_EN
AT	AVDD_ CC4	AVDD_ PLAT	TEST_ SEL_B	GND [93]	SYSCLK	SDHC_ DAT [1]	RSRV [32]	RSRV [16]	RSRV [13]	RSRV [31]	SPI_ MOSI	EC2_ TXD [0]	EC2_ TXD [3]	EC2_ RXD [0]	EC2_ RX_CLK	EC1_ TXD [2]	EC1_ TXD [0]	GND [103]

Figure 6. 1295 BGA Ball Map Diagram (Detail View D)

1.2 Pinout List

This table provides the pinout listing for the chipby bus.

Table 1. Pins List by Bus

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
DDR SDRAM Memory Interface 1					
D1_MDQ00	Data	A17	I/O	GV_{DD}	—
D1_MDQ01	Data	D17	I/O	GV_{DD}	—
D1_MDQ02	Data	C14	I/O	GV_{DD}	—
D1_MDQ03	Data	A14	I/O	GV_{DD}	—
D1_MDQ04	Data	C17	I/O	GV_{DD}	—
D1_MDQ05	Data	B17	I/O	GV_{DD}	—
D1_MDQ06	Data	A15	I/O	GV_{DD}	—
D1_MDQ07	Data	B15	I/O	GV_{DD}	—
D1_MDQ08	Data	D15	I/O	GV_{DD}	—
D1_MDQ09	Data	G15	I/O	GV_{DD}	—
D1_MDQ10	Data	E12	I/O	GV_{DD}	—
D1_MDQ11	Data	G12	I/O	GV_{DD}	—
D1_MDQ12	Data	F16	I/O	GV_{DD}	—
D1_MDQ13	Data	E15	I/O	GV_{DD}	—
D1_MDQ14	Data	E13	I/O	GV_{DD}	—
D1_MDQ15	Data	F13	I/O	GV_{DD}	—
D1_MDQ16	Data	C8	I/O	GV_{DD}	—
D1_MDQ17	Data	D12	I/O	GV_{DD}	—
D1_MDQ18	Data	E9	I/O	GV_{DD}	—
D1_MDQ19	Data	E10	I/O	GV_{DD}	—
D1_MDQ20	Data	C11	I/O	GV_{DD}	—
D1_MDQ21	Data	C10	I/O	GV_{DD}	—
D1_MDQ22	Data	E6	I/O	GV_{DD}	—
D1_MDQ23	Data	E7	I/O	GV_{DD}	—
D1_MDQ24	Data	F7	I/O	GV_{DD}	—
D1_MDQ25	Data	F11	I/O	GV_{DD}	—
D1_MDQ26	Data	H10	I/O	GV_{DD}	—
D1_MDQ27	Data	J10	I/O	GV_{DD}	—
D1_MDQ28	Data	F10	I/O	GV_{DD}	—
D1_MDQ29	Data	F8	I/O	GV_{DD}	—
D1_MDQ30	Data	H7	I/O	GV_{DD}	—

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
D1_MDQ31	Data	H9	I/O	GV_{DD}	—
D1_MDQ32	Data	AC7	I/O	GV_{DD}	—
D1_MDQ33	Data	AC6	I/O	GV_{DD}	—
D1_MDQ34	Data	AF6	I/O	GV_{DD}	—
D1_MDQ35	Data	AF7	I/O	GV_{DD}	—
D1_MDQ36	Data	AB5	I/O	GV_{DD}	—
D1_MDQ37	Data	AB6	I/O	GV_{DD}	—
D1_MDQ38	Data	AE5	I/O	GV_{DD}	—
D1_MDQ39	Data	AE6	I/O	GV_{DD}	—
D1_MDQ40	Data	AG5	I/O	GV_{DD}	—
D1_MDQ41	Data	AH9	I/O	GV_{DD}	—
D1_MDQ42	Data	AJ9	I/O	GV_{DD}	—
D1_MDQ43	Data	AJ10	I/O	GV_{DD}	—
D1_MDQ44	Data	AG8	I/O	GV_{DD}	—
D1_MDQ45	Data	AG7	I/O	GV_{DD}	—
D1_MDQ46	Data	AJ6	I/O	GV_{DD}	—
D1_MDQ47	Data	AJ7	I/O	GV_{DD}	—
D1_MDQ48	Data	AL9	I/O	GV_{DD}	—
D1_MDQ49	Data	AL8	I/O	GV_{DD}	—
D1_MDQ50	Data	AN10	I/O	GV_{DD}	—
D1_MDQ51	Data	AN11	I/O	GV_{DD}	—
D1_MDQ52	Data	AK8	I/O	GV_{DD}	—
D1_MDQ53	Data	AK7	I/O	GV_{DD}	—
D1_MDQ54	Data	AN7	I/O	GV_{DD}	—
D1_MDQ55	Data	AN8	I/O	GV_{DD}	—
D1_MDQ56	Data	AT9	I/O	GV_{DD}	—
D1_MDQ57	Data	AR10	I/O	GV_{DD}	—
D1_MDQ58	Data	AT13	I/O	GV_{DD}	—
D1_MDQ59	Data	AR13	I/O	GV_{DD}	—
D1_MDQ60	Data	AP9	I/O	GV_{DD}	—
D1_MDQ61	Data	AR9	I/O	GV_{DD}	—
D1_MDQ62	Data	AR12	I/O	GV_{DD}	—
D1_MDQ63	Data	AP12	I/O	GV_{DD}	—
D1_MECC0	Error Correcting Code	K9	I/O	GV_{DD}	—

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
D1_MECC1	Error Correcting Code	J5	I/O	GV_{DD}	—
D1_MECC2	Error Correcting Code	L10	I/O	GV_{DD}	—
D1_MECC3	Error Correcting Code	M10	I/O	GV_{DD}	—
D1_MECC4	Error Correcting Code	J8	I/O	GV_{DD}	—
D1_MECC5	Error Correcting Code	J7	I/O	GV_{DD}	—
D1_MECC6	Error Correcting Code	L7	I/O	GV_{DD}	—
D1_MECC7	Error Correcting Code	L9	I/O	GV_{DD}	—
$\overline{\text{D1_MAPAR_ERR}}$	Address Parity Error	N8	I	GV_{DD}	4
D1_MAPAR_OUT	Address Parity Out	Y7	O	GV_{DD}	—
D1_MDM0	Data Mask	A16	O	GV_{DD}	—
D1_MDM1	Data Mask	D14	O	GV_{DD}	—
D1_MDM2	Data Mask	D11	O	GV_{DD}	—
D1_MDM3	Data Mask	G11	O	GV_{DD}	—
D1_MDM4	Data Mask	AD7	O	GV_{DD}	—
D1_MDM5	Data Mask	AH8	O	GV_{DD}	—
D1_MDM6	Data Mask	AL11	O	GV_{DD}	—
D1_MDM7	Data Mask	AT10	O	GV_{DD}	—
D1_MDM8	Data Mask	K8	O	GV_{DD}	—
D1_MDQS0	Data Strobe	C16	I/O	GV_{DD}	—
D1_MDQS1	Data Strobe	G14	I/O	GV_{DD}	—
D1_MDQS2	Data Strobe	D9	I/O	GV_{DD}	—
D1_MDQS3	Data Strobe	G9	I/O	GV_{DD}	—
D1_MDQS4	Data Strobe	AD5	I/O	GV_{DD}	—
D1_MDQS5	Data Strobe	AH6	I/O	GV_{DD}	—
D1_MDQS6	Data Strobe	AM10	I/O	GV_{DD}	—
D1_MDQS7	Data Strobe	AT12	I/O	GV_{DD}	—
D1_MDQS8	Data Strobe	K6	I/O	GV_{DD}	—
D1_MDQS0_B	Data Strobe	B16	I/O	GV_{DD}	—
D1_MDQS1_B	Data Strobe	F14	I/O	GV_{DD}	—
D1_MDQS2_B	Data Strobe	D8	I/O	GV_{DD}	—
D1_MDQS3_B	Data Strobe	G8	I/O	GV_{DD}	—
D1_MDQS4_B	Data Strobe	AD4	I/O	GV_{DD}	—
D1_MDQS5_B	Data Strobe	AH5	I/O	GV_{DD}	—
D1_MDQS6_B	Data Strobe	AM9	I/O	GV_{DD}	—

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
D1_MDQS7_B	Data Strobe	AT11	I/O	GV_{DD}	—
D1_MDQS8_B	Data Strobe	K5	I/O	GV_{DD}	—
D1_MBA0	Bank Select	AA8	O	GV_{DD}	—
D1_MBA1	Bank Select	Y10	O	GV_{DD}	—
D1_MBA2	Bank Select	M8	O	GV_{DD}	—
D1_MA00	Address	Y9	O	GV_{DD}	—
D1_MA01	Address	U6	O	GV_{DD}	—
D1_MA02	Address	U7	O	GV_{DD}	—
D1_MA03	Address	U9	O	GV_{DD}	—
D1_MA04	Address	U10	O	GV_{DD}	—
D1_MA05	Address	T8	O	GV_{DD}	—
D1_MA06	Address	T9	O	GV_{DD}	—
D1_MA07	Address	R8	O	GV_{DD}	—
D1_MA08	Address	R7	O	GV_{DD}	—
D1_MA09	Address	P6	O	GV_{DD}	—
D1_MA10	Address	AA7	O	GV_{DD}	—
D1_MA11	Address	P7	O	GV_{DD}	—
D1_MA12	Address	N6	O	GV_{DD}	—
D1_MA13	Address	AE8	O	GV_{DD}	—
D1_MA14	Address	M7	O	GV_{DD}	—
D1_MA15	Address	L6	O	GV_{DD}	—
D1_MWE_B	Write Enable	AB8	O	GV_{DD}	—
D1_MRAS_B	Row Address Strobe	AA10	O	GV_{DD}	—
D1_MCAS_B	Column Address Strobe	AC10	O	GV_{DD}	—
D1_MCS0_B	Chip Select	AC9	O	GV_{DD}	—
D1_MCS1_B	Chip Select	AE9	O	GV_{DD}	—
D1_MCS2_B	Chip Select	AB9	O	GV_{DD}	—
D1_MCS3_B	Chip Select	AF9	O	GV_{DD}	—
D1_MCKE0	Clock Enable	P10	O	GV_{DD}	—
D1_MCKE1	Clock Enable	R10	O	GV_{DD}	—
D1_MCKE2	Clock Enable	P9	O	GV_{DD}	—
D1_MCKE3	Clock Enable	N9	O	GV_{DD}	—
D1_MCK0	Clock	W6	O	GV_{DD}	—
D1_MCK1	Clock	V6	O	GV_{DD}	—

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
D1_MCK2	Clock	V8	O	GV_{DD}	—
D1_MCK3	Clock	W9	O	GV_{DD}	—
D1_MCK4	Clock	F1	O	GV_{DD}	—
D1_MCK5	Clock	AL1	O	GV_{DD}	—
D1_MCK0_B	Clock Complements	W5	O	GV_{DD}	—
D1_MCK1_B	Clock Complements	V5	O	GV_{DD}	—
D1_MCK2_B	Clock Complements	V9	O	GV_{DD}	—
D1_MCK3_B	Clock Complements	W8	O	GV_{DD}	—
D1_MCK4_B	Clock Complements	F2	O	GV_{DD}	—
D1_MCK5_B	Clock Complements	AL2	O	GV_{DD}	—
D1_MODT0	On Die Termination	AD10	O	GV_{DD}	—
D1_MODT1	On Die Termination	AG10	O	GV_{DD}	—
D1_MODT2	On Die Termination	AD8	O	GV_{DD}	—
D1_MODT3	On Die Termination	AF10	O	GV_{DD}	—
D1_MDIC0	Driver Impedance Calibration	T6	I/O	GV_{DD}	16
D1_MDIC1	Driver Impedance Calibration	AA5	I/O	GV_{DD}	16
DDR SDRAM Memory Interface 2					
D2_MDQ00	Data	C13	I/O	GV_{DD}	—
D2_MDQ01	Data	A12	I/O	GV_{DD}	—
D2_MDQ02	Data	B9	I/O	GV_{DD}	—
D2_MDQ03	Data	A8	I/O	GV_{DD}	—
D2_MDQ04	Data	A13	I/O	GV_{DD}	—
D2_MDQ05	Data	B13	I/O	GV_{DD}	—
D2_MDQ06	Data	B10	I/O	GV_{DD}	—
D2_MDQ07	Data	A9	I/O	GV_{DD}	—
D2_MDQ08	Data	A7	I/O	GV_{DD}	—
D2_MDQ09	Data	D6	I/O	GV_{DD}	—
D2_MDQ10	Data	A4	I/O	GV_{DD}	—
D2_MDQ11	Data	B4	I/O	GV_{DD}	—
D2_MDQ12	Data	C7	I/O	GV_{DD}	—
D2_MDQ13	Data	B7	I/O	GV_{DD}	—
D2_MDQ14	Data	C5	I/O	GV_{DD}	—
D2_MDQ15	Data	D5	I/O	GV_{DD}	—
D2_MDQ16	Data	B1	I/O	GV_{DD}	—

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
D2_MDQ17	Data	B3	I/O	GV_{DD}	—
D2_MDQ18	Data	D3	I/O	GV_{DD}	—
D2_MDQ19	Data	E1	I/O	GV_{DD}	—
D2_MDQ20	Data	A3	I/O	GV_{DD}	—
D2_MDQ21	Data	A2	I/O	GV_{DD}	—
D2_MDQ22	Data	D1	I/O	GV_{DD}	—
D2_MDQ23	Data	D2	I/O	GV_{DD}	—
D2_MDQ24	Data	F4	I/O	GV_{DD}	—
D2_MDQ25	Data	F5	I/O	GV_{DD}	—
D2_MDQ26	Data	H4	I/O	GV_{DD}	—
D2_MDQ27	Data	H6	I/O	GV_{DD}	—
D2_MDQ28	Data	E4	I/O	GV_{DD}	—
D2_MDQ29	Data	E3	I/O	GV_{DD}	—
D2_MDQ30	Data	H3	I/O	GV_{DD}	—
D2_MDQ31	Data	H1	I/O	GV_{DD}	—
D2_MDQ32	Data	AG4	I/O	GV_{DD}	—
D2_MDQ33	Data	AG2	I/O	GV_{DD}	—
D2_MDQ34	Data	AJ3	I/O	GV_{DD}	—
D2_MDQ35	Data	AJ1	I/O	GV_{DD}	—
D2_MDQ36	Data	AF4	I/O	GV_{DD}	—
D2_MDQ37	Data	AF3	I/O	GV_{DD}	—
D2_MDQ38	Data	AH1	I/O	GV_{DD}	—
D2_MDQ39	Data	AJ4	I/O	GV_{DD}	—
D2_MDQ40	Data	AL6	I/O	GV_{DD}	—
D2_MDQ41	Data	AL5	I/O	GV_{DD}	—
D2_MDQ42	Data	AN4	I/O	GV_{DD}	—
D2_MDQ43	Data	AN5	I/O	GV_{DD}	—
D2_MDQ44	Data	AK5	I/O	GV_{DD}	—
D2_MDQ45	Data	AK4	I/O	GV_{DD}	—
D2_MDQ46	Data	AM6	I/O	GV_{DD}	—
D2_MDQ47	Data	AM7	I/O	GV_{DD}	—
D2_MDQ48	Data	AN1	I/O	GV_{DD}	—
D2_MDQ49	Data	AP3	I/O	GV_{DD}	—
D2_MDQ50	Data	AT1	I/O	GV_{DD}	—

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
D2_MDQ51	Data	AT2	I/O	GV_{DD}	—
D2_MDQ52	Data	AM1	I/O	GV_{DD}	—
D2_MDQ53	Data	AN2	I/O	GV_{DD}	—
D2_MDQ54	Data	AR3	I/O	GV_{DD}	—
D2_MDQ55	Data	AT3	I/O	GV_{DD}	—
D2_MDQ56	Data	AP5	I/O	GV_{DD}	—
D2_MDQ57	Data	AT5	I/O	GV_{DD}	—
D2_MDQ58	Data	AP8	I/O	GV_{DD}	—
D2_MDQ59	Data	AT8	I/O	GV_{DD}	—
D2_MDQ60	Data	AR4	I/O	GV_{DD}	—
D2_MDQ61	Data	AT4	I/O	GV_{DD}	—
D2_MDQ62	Data	AR7	I/O	GV_{DD}	—
D2_MDQ63	Data	AT7	I/O	GV_{DD}	—
D2_MECC0	Error Correcting Code	J1	I/O	GV_{DD}	—
D2_MECC1	Error Correcting Code	K3	I/O	GV_{DD}	—
D2_MECC2	Error Correcting Code	M5	I/O	GV_{DD}	—
D2_MECC3	Error Correcting Code	N5	I/O	GV_{DD}	—
D2_MECC4	Error Correcting Code	J4	I/O	GV_{DD}	—
D2_MECC5	Error Correcting Code	J2	I/O	GV_{DD}	—
D2_MECC6	Error Correcting Code	L3	I/O	GV_{DD}	—
D2_MECC7	Error Correcting Code	L4	I/O	GV_{DD}	—
D2_MAPAR_ERR_B	Address Parity Error	N2	I	GV_{DD}	4
D2_MAPAR_OUT	Address Parity Out	Y1	O	GV_{DD}	—
D2_MDM0	Data Mask	B12	O	GV_{DD}	—
D2_MDM1	Data Mask	B6	O	GV_{DD}	—
D2_MDM2	Data Mask	C4	O	GV_{DD}	—
D2_MDM3	Data Mask	G3	O	GV_{DD}	—
D2_MDM4	Data Mask	AG1	O	GV_{DD}	—
D2_MDM5	Data Mask	AL3	O	GV_{DD}	—
D2_MDM6	Data Mask	AP2	O	GV_{DD}	—
D2_MDM7	Data Mask	AP6	O	GV_{DD}	—
D2_MDM8	Data Mask	K2	O	GV_{DD}	—
D2_MDQS0	Data Strobe	A10	I/O	GV_{DD}	—
D2_MDQS1	Data Strobe	A5	I/O	GV_{DD}	—

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
D2_MDQS2	Data Strobe	C2	I/O	GV_{DD}	—
D2_MDQS3	Data Strobe	G6	I/O	GV_{DD}	—
D2_MDQS4	Data Strobe	AH2	I/O	GV_{DD}	—
D2_MDQS5	Data Strobe	AM4	I/O	GV_{DD}	—
D2_MDQS6	Data Strobe	AR1	I/O	GV_{DD}	—
D2_MDQS7	Data Strobe	AR6	I/O	GV_{DD}	—
D2_MDQS8	Data Strobe	L1	I/O	GV_{DD}	—
D2_MDQS0_B	Data Strobe	A11	I/O	GV_{DD}	—
D2_MDQS1_B	Data Strobe	A6	I/O	GV_{DD}	—
D2_MDQS2_B	Data Strobe	C1	I/O	GV_{DD}	—
D2_MDQS3_B	Data Strobe	G5	I/O	GV_{DD}	—
D2_MDQS4_B	Data Strobe	AH3	I/O	GV_{DD}	—
D2_MDQS5_B	Data Strobe	AM3	I/O	GV_{DD}	—
D2_MDQS6_B	Data Strobe	AP1	I/O	GV_{DD}	—
D2_MDQS7_B	Data Strobe	AT6	I/O	GV_{DD}	—
D2_MDQS8_B	Data Strobe	K1	I/O	GV_{DD}	—
D2_MBA0	Bank Select	AA3	O	GV_{DD}	—
D2_MBA1	Bank Select	AA1	O	GV_{DD}	—
D2_MBA2	Bank Select	M1	O	GV_{DD}	—
D2_MA00	Address	Y4	O	GV_{DD}	—
D2_MA01	Address	U1	O	GV_{DD}	—
D2_MA02	Address	U4	O	GV_{DD}	—
D2_MA03	Address	T1	O	GV_{DD}	—
D2_MA04	Address	T2	O	GV_{DD}	—
D2_MA05	Address	T3	O	GV_{DD}	—
D2_MA06	Address	R1	O	GV_{DD}	—
D2_MA07	Address	R4	O	GV_{DD}	—
D2_MA08	Address	R2	O	GV_{DD}	—
D2_MA09	Address	P1	O	GV_{DD}	—
D2_MA10	Address	AA2	O	GV_{DD}	—
D2_MA11	Address	P3	O	GV_{DD}	—
D2_MA12	Address	N1	O	GV_{DD}	—
D2_MA13	Address	AC4	O	GV_{DD}	—
D2_MA14	Address	N3	O	GV_{DD}	—

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
D2_MA15	Address	M2	O	GV_{DD}	—
D2_MWE_B	Write Enable	AB2	O	GV_{DD}	—
D2_MRAS_B	Row Address Strobe	AB1	O	GV_{DD}	—
D2_MCAS_B	Column Address Strobe	AC3	O	GV_{DD}	—
D2_MCS0_B	Chip Select	AC1	O	GV_{DD}	—
D2_MCS1_B	Chip Select	AE1	O	GV_{DD}	—
D2_MCS2_B	Chip Select	AB3	O	GV_{DD}	—
D2_MCS3_B	Chip Select	AE2	O	GV_{DD}	—
D2_MCKE0	Clock Enable	R5	O	GV_{DD}	—
D2_MCKE1	Clock Enable	T5	O	GV_{DD}	—
D2_MCKE2	Clock Enable	P4	O	GV_{DD}	—
D2_MCKE3	Clock Enable	M4	O	GV_{DD}	—
D2_MCK0	Clock	W3	O	GV_{DD}	—
D2_MCK1	Clock	V3	O	GV_{DD}	—
D2_MCK2	Clock	V1	O	GV_{DD}	—
D2_MCK3	Clock	W2	O	GV_{DD}	—
D2_MCK4	Clock	G1	O	GV_{DD}	—
D2_MCK5	Clock	AK2	O	GV_{DD}	—
D2_MCK0_B	Clock Complements	W4	O	GV_{DD}	—
D2_MCK1_B	Clock Complements	V4	O	GV_{DD}	—
D2_MCK2_B	Clock Complements	V2	O	GV_{DD}	—
D2_MCK3_B	Clock Complements	W1	O	GV_{DD}	—
D2_MCK4_B	Clock Complements	G2	O	GV_{DD}	—
D2_MCK5_B	Clock Complements	AK1	O	GV_{DD}	—
D2_MODT0	On Die Termination	AD2	O	GV_{DD}	—
D2_MODT1	On Die Termination	AF1	O	GV_{DD}	—
D2_MODT2	On Die Termination	AD1	O	GV_{DD}	—
D2_MODT3	On Die Termination	AE3	O	GV_{DD}	—
D2_MDIC0	Driver Impedance Calibration	AA4	I/O	GV_{DD}	16
D2_MDIC1	Driver Impedance Calibration	Y6	I/O	GV_{DD}	16
Local Bus Controller Interface					
LAD00	Muxed Data/Address	K26	I/O	BV_{DD}	3
LAD01	Muxed Data/Address	L26	I/O	BV_{DD}	3
LAD02	Muxed Data/Address	J26	I/O	BV_{DD}	3

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
LAD03	Muxed Data/Address	H25	I/O	BV_{DD}	3
LAD04	Muxed Data/Address	F25	I/O	BV_{DD}	3
LAD05	Muxed Data/Address	H24	I/O	BV_{DD}	3
LAD06	Muxed Data/Address	G24	I/O	BV_{DD}	3
LAD07	Muxed Data/Address	G23	I/O	BV_{DD}	3
LAD08	Muxed Data/Address	E23	I/O	BV_{DD}	3
LAD09	Muxed Data/Address	D23	I/O	BV_{DD}	3
LAD10	Muxed Data/Address	J22	I/O	BV_{DD}	3
LAD11	Muxed Data/Address	G22	I/O	BV_{DD}	3
LAD12	Muxed Data/Address	F19	I/O	BV_{DD}	3
LAD13	Muxed Data/Address	J18	I/O	BV_{DD}	3
LAD14	Muxed Data/Address	K18	I/O	BV_{DD}	3
LAD15	Muxed Data/Address	J17	I/O	BV_{DD}	3
LDP0	Data Parity	J24	I/O	BV_{DD}	—
LDP1	Data Parity	K23	I/O	BV_{DD}	—
LA16	Address	J25	O	BV_{DD}	3, 30
LA17	Address	G25	O	BV_{DD}	3, 30
LA18	Address	H23	O	BV_{DD}	3, 30
LA19	Address	F22	O	BV_{DD}	3, 30
LA20	Address	H22	O	BV_{DD}	3, 30
LA21	Address	E21	O	BV_{DD}	3, 30
LA22	Address	F21	O	BV_{DD}	3, 30
LA23	Address	H21	O	BV_{DD}	3, 4
LA24	Address	K21	O	BV_{DD}	3, 4, 33
LA25	Address	G20	O	BV_{DD}	3, 30
LA26	Address	J20	O	BV_{DD}	—
LA27	Address	K20	O	BV_{DD}	—
LA28	Address	G19	O	BV_{DD}	—
LA29	Address	H19	O	BV_{DD}	—
LA30	Address	J19	O	BV_{DD}	—
LA31	Address	G18	O	BV_{DD}	—
LCS0_B	Chip Selects	D19	O	BV_{DD}	5
LCS1_B	Chip Selects	D20	O	BV_{DD}	5
LCS2_B	Chip Selects	E20	O	BV_{DD}	5

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
LCS3_B	Chip Selects	D21	O	BV_{DD}	5
LCS4_B	Chip Selects	D22	O	BV_{DD}	5
LCS5_B	Chip Selects	B23	O	BV_{DD}	5
LCS6_B	Chip Selects	F24	O	BV_{DD}	5
LCS7_B	Chip Selects	G26	O	BV_{DD}	5
LWE0_B	Write Enable	D24	O	BV_{DD}	—
LWE1_B	Write Enable	A24	O	BV_{DD}	—
LBCTL	Buffer Control	C22	O	BV_{DD}	—
LALE	Address Latch Enable	A23	I/O	BV_{DD}	—
LGPL0	UPM General Purpose Line 0/ LFCLE—FCM	B25	O	BV_{DD}	3, 4
LGPL1	UPM General Purpose Line 1/ LFALE—FCM	E25	O	BV_{DD}	3, 4
LGPL2	UPM General Purpose Line 2/ $\overline{\text{LOE}}$—Output Enable	D25	O	BV_{DD}	3, 4
LGPL3	UPM General Purpose LIne 3/ $\overline{\text{LFWP}}$—FCM	H26	O	BV_{DD}	3, 4
LGPL4	UPM General Purpose Line 4/ $\overline{\text{LGTA}}$—FCM	C25	I/O	BV_{DD}	35
LGPL5	UPM General Purpose Line 5 / Amux	E26	O	BV_{DD}	3, 4
LCLK0	Local Bus Clock	C24	O	BV_{DD}	—
LCLK1	Local Bus Clock	C23	O	BV_{DD}	—
DMA					
DMA1_DREQ0_B/GPIO18	DMA1 Channel 0 Request	AP21	I	OV_{DD}	25
DMA1_DACK0_B/GPIO19	DMA1 Channel 0 Acknowledge	AL19	O	OV_{DD}	25
DMA1_DDONE0_B	DMA1 Channel 0 Done	AN21	O	OV_{DD}	4, 26
DMA2_DREQ0_B/GPIO20/ALT_MDVAL	DMA2 Channel 0 Request	AJ20	I	OV_{DD}	25
DMA2_DACK0_B/EVT7_B/ ALT_MDSRCID0	DMA2 Channel 0 Acknowledge	AG19	O	OV_{DD}	25
DMA2_DDONE0_B/EVT8_B/ ALT_MDSRCID1	DMA2 Channel 0 Done	AP20	O	OV_{DD}	25
USB Host Port 1					
USB1_D7/EC1_TXD3	USB1 Data bits	AP36	I/O	LV_{DD}	3, 30
USB1_D6/EC1_TXD2	USB1 Data bits	AT34	I/O	LV_{DD}	3, 30
USB1_D5/EC1_TXD1	USB1 Data bits	AR34	I/O	LV_{DD}	3, 30
USB1_D4/EC1_TXD0	USB1 Data bits	AT35	I/O	LV_{DD}	3, 30

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
USB1_D3/EC1_RXD3	USB1 Data bits	AM33	I/O	LV_{DD}	26
USB1_D2/EC1_RXD2	USB1 Data bits	AN34	I/O	LV_{DD}	26
USB1_D1/EC1_RXD1	USB1 Data bits	AN35	I/O	LV_{DD}	26
USB1_D0/EC1_RXD0	USB1 Data bits	AN36	I/O	LV_{DD}	26
USB1_STP/EC1_TX_EN	USB1 Stop	AR36	O	LV_{DD}	—
USB1_NXT/EC1_RX_DV	USB1 Next data	AM34	I	LV_{DD}	26
USB1_DIR/EC1_RX_CLK	USB1 Data Direction	AM36	I	LV_{DD}	26
USB1_CLK/EC1_GTX_CLK	USB1 bus clock	AP35	I	LV_{DD}	25
USB Host Port 2					
USB2_D7/EC2_TXD3	USB2 Data bits	AT31	I/O	LV_{DD}	3, 30
USB2_D6/EC2_TXD2	USB2 Data bits	AP30	I/O	LV_{DD}	3, 30
USB2_D5/EC2_TXD1	USB2 Data bits	AR30	I/O	LV_{DD}	3, 30
USB2_D4/EC2_TXD0	USB2 Data bits	AT30	I/O	LV_{DD}	3, 30
USB2_D3/EC2_RXD3	USB2 Data bits	AP33	I/O	LV_{DD}	26
USB2_D2/EC2_RXD2	USB2 Data bits	AN32	I/O	LV_{DD}	26
USB2_D1/EC2_RXD1	USB2 Data bits	AP32	I/O	LV_{DD}	26
USB2_D0/EC2_RXD0	USB2 Data bits	AT32	I/O	LV_{DD}	26
USB2_STP/EC2_TX_EN	USB2 Stop	AR31	O	LV_{DD}	—
USB2_NXT/EC2_RX_DV	USB2 Next data	AR33	I	LV_{DD}	26
USB2_DIR/EC2_RX_CLK	USB2 Data Direction	AT33	I	LV_{DD}	26
USB2_CLK/EC2_GTX_CLK	USB2 bus clock	AN31	I	LV_{DD}	25
Programmable Interrupt Controller					
IRQ00	External Interrupts	AJ16	I	OV_{DD}	—
IRQ01	External Interrupts	AH16	I	OV_{DD}	—
IRQ02	External Interrupts	AK12	I	OV_{DD}	—
IRQ03/GPIO21	External Interrupts	AJ15	I	OV_{DD}	25
IRQ04/GPIO22	External Interrupts	AH17	I	OV_{DD}	25
IRQ05/GPIO23	External Interrupts	AJ13	I	OV_{DD}	25
IRQ06/GPIO24	External Interrupts	AG17	I	OV_{DD}	25
IRQ07/GPIO25	External Interrupts	AM13	I	OV_{DD}	25
IRQ08/GPIO26	External Interrupts	AG13	I	OV_{DD}	25
IRQ09/GPIO27	External Interrupts	AK11	I	OV_{DD}	25
IRQ10/GPIO28	External Interrupts	AH14	I	OV_{DD}	25
IRQ11/GPIO29	External Interrupts	AL12	I	OV_{DD}	25

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
IRQ_OUT_B/EVT9_B	Interrupt Output	AK14	O	OV_{DD}	1, 2, 25
TMP_DETECT_B	Tamper Detect	AN19	I	OV_{DD}	26
eSDHC					
SDHC_CMD	Command/Response	AG23	I/O	OV_{DD}	—
SDHC_DAT0	Data	AP24	I/O	OV_{DD}	—
SDHC_DAT1	Data	AT24	I/O	OV_{DD}	—
SDHC_DAT2	Data	AM23	I/O	OV_{DD}	—
SDHC_DAT3	Data	AG22	I/O	OV_{DD}	—
SDHC_DAT4/SPI_CS0_B	Data	AN29	I/O	CV_{DD}	25, 32
SDHC_DAT5/SPI_CS1_B	Data	AJ28	I/O	CV_{DD}	25, 32
SDHC_DAT6/SPI_CS2_B	Data	AR29	I/O	CV_{DD}	25, 32
SDHC_DAT7/SPI_CS3_B	Data	AM29	I/O	CV_{DD}	25, 32
SDHC_CLK	Host to Card Clock	AL23	O	OV_{DD}	—
SDHC_CD_B/IIC3_SCL/GPIO16	Card Detection	AK13	I	OV_{DD}	25, 26
SDHC_WP/IIC3_SDA/GPIO17	Card Write Protection	AM14	I	OV_{DD}	25, 26
eSPI					
SPI_MOSI	Master Out Slave In	AT29	I/O	CV_{DD}	—
SPI_MISO	Master In Slave Out	AH28	I	CV_{DD}	—
SPI_CLK	eSPI clock	AK29	O	CV_{DD}	—
SPI_CS0_B/SDHC_DAT4	eSPI chip select	AN29	O	CV_{DD}	25
SPI_CS1_B/SDHC_DAT5	eSPI chip select	AJ28	O	CV_{DD}	25
SPI_CS2_B/SDHC_DAT6	eSPI chip select	AR29	O	CV_{DD}	25
SPI_CS3_B/SDHC_DAT7	eSPI chip select	AM29	O	CV_{DD}	25
IEEE 1588					
TSEC_1588_CLK_IN	Clock In	AL35	I	LV_{DD}	—
TSEC_1588_TRIG_IN1	Trigger In 1	AL36	I	LV_{DD}	—
TSEC_1588_TRIG_IN2	Trigger In 2	AK36	I	LV_{DD}	—
TSEC_1588_ALARM_OUT1	Alarm Out 1	AJ36	O	LV_{DD}	—
TSEC_1588_ALARM_OUT2/GPIO30	Alarm Out 2	AK35	O	LV_{DD}	25
TSEC_1588_CLK_OUT	Clock Out	AM30	O	LV_{DD}	—
TSEC_1588_PULSE_OUT1	Pulse Out1	AL30	O	LV_{DD}	—
TSEC_1588_PULSE_OUT2/GPIO31	Pulse Out2	AJ34	O	LV_{DD}	25
Ethernet MII Management Interface 1					

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
EMI1_MDC	Management Data Clock	AJ33	O	LV_{DD}	—
EMI1_MDIO	Management Data In/Out	AL32	I/O	LV_{DD}	—
Ethernet MII Management Interface 2					
EMI2_MDC	Management Data Clock	AK30	O	1.2 V	2, 18, 21
EMI2_MDIO	Management Data In/Out	AJ30	I/O	1.2 V	2, 18, 21
Ethernet Reference Clock					
EC_GTX_CLK125	Reference Clock	AK34	I	LV_{DD}	26
Ethernet External Timestamping					
EC_XTRNL_TX_STMP1	External Timestamp Transmit 1	AM31	I	LV_{DD}	—
EC_XTRNL_RX_STMP1	External Timestamp Receive 1	AK32	I	LV_{DD}	—
EC_XTRNL_TX_STMP2	External Timestamp Transmit 2	AJ31	I	LV_{DD}	—
EC_XTRNL_RX_STMP2	External Timestamp Receive 2	AK31	I	LV_{DD}	—
Three-Speed Ethernet Controller 1					
EC1_TXD3/USB1_D7	Transmit Data	AP36	O	LV_{DD}	3, 25, 30
EC1_TXD2/USB1_D6	Transmit Data	AT34	O	LV_{DD}	3, 25, 30
EC1_TXD1/USB1_D5	Transmit Data	AR34	O	LV_{DD}	3, 25, 30
EC1_TXD0/USB1_D4	Transmit Data	AT35	O	LV_{DD}	3, 25, 30
EC1_TX_EN/USB1_STP	Transmit Enable	AR36	O	LV_{DD}	15
EC1_GTX_CLK/USB1_CLK	Transmit Clock Out	AP35	O	LV_{DD}	25
EC1_RXD3/USB1_D3	Receive Data	AM33	I	LV_{DD}	25, 26
EC1_RXD2/USB1_D2	Receive Data	AN34	I	LV_{DD}	25, 26
EC1_RXD1/USB1_D1	Receive Data	AN35	I	LV_{DD}	25, 26
EC1_RXD0/USB1_D0	Receive Data	AN36	I	LV_{DD}	25, 26
EC1_RX_DV/USB1_NXT	Receive Data Valid	AM34	I	LV_{DD}	26
EC1_RX_CLK/USB1_DIR	Receive Clock	AM36	I	LV_{DD}	26
Three-Speed Ethernet Controller 2					
EC2_TXD3/USB2_D7	Transmit Data	AT31	O	LV_{DD}	3, 25, 30
EC2_TXD2/USB2_D6	Transmit Data	AP30	O	LV_{DD}	3, 25, 30

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
EC2_TXD1/USB2_D5	Transmit Data	AR30	O	LV_{DD}	3, 25, 30
EC2_TXD0/USB2_D4	Transmit Data	AT30	O	LV_{DD}	3, 25, 30
EC2_TX_EN/USB2_STP	Transmit Enable	AR31	O	LV_{DD}	15
EC2_GTX_CLK/USB2_CLK	Transmit Clock Out	AN31	O	LV_{DD}	25
EC2_RXD3/USB2_D3	Receive Data	AP33	I	LV_{DD}	25, 26
EC2_RXD2/USB2_D2	Receive Data	AN32	I	LV_{DD}	25, 26
EC2_RXD1/USB2_D1	Receive Data	AP32	I	LV_{DD}	25, 26
EC2_RXD0/USB2_D0	Receive Data	AT32	I	LV_{DD}	25, 26
EC2_RX_DV/USB2_NXT	Receive Data Valid	AR33	I	LV_{DD}	26
EC2_RX_CLK/USB2_DIR	Receive Clock	AT33	I	LV_{DD}	26
DUART					
UART1_SOUT/GPIO8	Transmit Data	AL22	O	OV_{DD}	25
UART2_SOUT/GPIO9	Transmit Data	AJ22	O	OV_{DD}	25
UART1_SIN/GPIO10	Receive Data	AR23	I	OV_{DD}	25
UART2_SIN/GPIO11	Receive Data	AN23	I	OV_{DD}	25
UART1_RTS_B/UART3_SOUT/GPIO12	Ready to Send	AM22	O	OV_{DD}	25
UART2_RTS_B/UART4_SOUT/GPIO13	Ready to Send	AK23	O	OV_{DD}	25
UART1_CTS_B/UART3_SIN/GPIO14	Clear to Send	AP22	I	OV_{DD}	25
UART2_CTS_B/UART4_SIN/GPIO15	Clear to Send	AH23	I	OV_{DD}	25
I^2C Interface					
IIC1_SCL	Serial Clock	AH15	I/O	OV_{DD}	2, 14
IIC1_SDA	Serial Data	AN14	I/O	OV_{DD}	2, 14
IIC2_SCL	Serial Clock	AM15	I/O	OV_{DD}	2, 14
IIC2_SDA	Serial Data	AL14	I/O	OV_{DD}	2, 14
IIC3_SCL/GPIO16/SDHC_CD_B	Serial Clock	AK13	I/O	OV_{DD}	2, 14
IIC3_SDA/GPIO17/SDHC_WP	Serial Data	AM14	I/O	OV_{DD}	2, 14
IIC4_SCL/EVT5_B	Serial Clock	AG14	I/O	OV_{DD}	2, 14
IIC4_SDA/EVT6_B	Serial Data	AL15	I/O	OV_{DD}	2, 14
SerDes (x18) PCIe, sRIO, Aurora, 10GE, 1GE					
SD_TX17	Transmit Data (positive)	AG31	O	XV_{DD}	—
SD_TX16	Transmit Data (positive)	AE31	O	XV_{DD}	—
SD_TX15	Transmit Data (positive)	AB33	O	XV_{DD}	—

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
SD_TX14	Transmit Data (positive)	AA31	O	XV_{DD}	—
SD_TX13	Transmit Data (positive)	Y29	O	XV_{DD}	—
SD_TX12	Transmit Data (positive)	W31	O	XV_{DD}	—
SD_TX11	Transmit Data (positive)	T30	O	XV_{DD}	—
SD_TX10	Transmit Data (positive)	P31	O	XV_{DD}	—
SD_TX09	Transmit Data (positive)	N33	O	XV_{DD}	—
SD_TX08	Transmit Data (positive)	M31	O	XV_{DD}	—
SD_TX07	Transmit Data (positive)	K31	O	XV_{DD}	—
SD_TX06	Transmit Data (positive)	J33	O	XV_{DD}	—
SD_TX05	Transmit Data (positive)	G33	O	XV_{DD}	—
SD_TX04	Transmit Data (positive)	D34	O	XV_{DD}	—
SD_TX03	Transmit Data (positive)	F31	O	XV_{DD}	—
SD_TX02	Transmit Data (positive)	H30	O	XV_{DD}	—
SD_TX01	Transmit Data (positive)	F29	O	XV_{DD}	—
SD_TX00	Transmit Data (positive)	H28	O	XV_{DD}	—
SD_TX17_B	Transmit Data (negative)	AG32	O	XV_{DD}	—
SD_TX16_B	Transmit Data (negative)	AE32	O	XV_{DD}	—
SD_TX15_B	Transmit Data (negative)	AB34	O	XV_{DD}	—
SD_TX14_B	Transmit Data (negative)	AA32	O	XV_{DD}	—
SD_TX13_B	Transmit Data (negative)	Y30	O	XV_{DD}	—
SD_TX12_B	Transmit Data (negative)	W32	O	XV_{DD}	—
SD_TX11_B	Transmit Data (negative)	T31	O	XV_{DD}	—
SD_TX10_B	Transmit Data (negative)	P32	O	XV_{DD}	—
SD_TX09_B	Transmit Data (negative)	N34	O	XV_{DD}	—
SD_TX08_B	Transmit Data (negative)	M32	O	XV_{DD}	—
SD_TX07_B	Transmit Data (negative)	K32	O	XV_{DD}	—
SD_TX06_B	Transmit Data (negative)	J34	O	XV_{DD}	—
SD_TX05_B	Transmit Data (negative)	F33	O	XV_{DD}	—
SD_TX04_B	Transmit Data (negative)	E34	O	XV_{DD}	—
SD_TX03_B	Transmit Data (negative)	E31	O	XV_{DD}	—
SD_TX02_B	Transmit Data (negative)	G30	O	XV_{DD}	—
SD_TX01_B	Transmit Data (negative)	E29	O	XV_{DD}	—
SD_TX00_B	Transmit Data (negative)	G28	O	XV_{DD}	—
SD_RX17	Receive Data (positive)	AG36	I	SV_{DD}	—

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
SD_RX16	Receive Data (positive)	AF34	I	SV_{DD}	—
SD_RX15	Receive Data (positive)	AC36	I	SV_{DD}	—
SD_RX14	Receive Data (positive)	AA36	I	SV_{DD}	—
SD_RX13	Receive Data (positive)	Y34	I	SV_{DD}	—
SD_RX12	Receive Data (positive)	W36	I	SV_{DD}	—
SD_RX11	Receive Data (positive)	T34	I	SV_{DD}	—
SD_RX10	Receive Data (positive)	P36	I	SV_{DD}	—
SD_RX09	Receive Data (positive)	M36	I	SV_{DD}	—
SD_RX08	Receive Data (positive)	L34	I	SV_{DD}	—
SD_RX07	Receive Data (positive)	K36	I	SV_{DD}	—
SD_RX06	Receive Data (positive)	H36	I	SV_{DD}	—
SD_RX05	Receive Data (positive)	F36	I	SV_{DD}	—
SD_RX04	Receive Data (positive)	D36	I	SV_{DD}	—
SD_RX03	Receive Data (positive)	A31	I	SV_{DD}	—
SD_RX02	Receive Data (positive)	C30	I	SV_{DD}	—
SD_RX01	Receive Data (positive)	A29	I	SV_{DD}	—
SD_RX00	Receive Data (positive)	C28	I	SV_{DD}	—
SD_RX17_B	Receive Data (negative)	AG35	I	SV_{DD}	—
SD_RX16_B	Receive Data (negative)	AF33	I	SV_{DD}	—
SD_RX15_B	Receive Data (negative)	AC35	I	SV_{DD}	—
SD_RX14_B	Receive Data (negative)	AA35	I	SV_{DD}	—
SD_RX13_B	Receive Data (negative)	Y33	I	SV_{DD}	—
SD_RX12_B	Receive Data (negative)	W35	I	SV_{DD}	—
SD_RX11_B	Receive Data (negative)	T33	I	SV_{DD}	—
SD_RX10_B	Receive Data (negative)	P35	I	SV_{DD}	—
SD_RX09_B	Receive Data (negative)	M35	I	SV_{DD}	—
SD_RX08_B	Receive Data (negative)	L33	I	SV_{DD}	—
SD_RX07_B	Receive Data (negative)	K35	I	SV_{DD}	—
SD_RX06_B	Receive Data (negative)	H35	I	SV_{DD}	—
SD_RX05_B	Receive Data (negative)	F35	I	SV_{DD}	—
SD_RX04_B	Receive Data (negative)	C36	I	SV_{DD}	—
SD_RX03_B	Receive Data (negative)	B31	I	SV_{DD}	—
SD_RX02_B	Receive Data (negative)	D30	I	SV_{DD}	—
SD_RX01_B	Receive Data (negative)	B29	I	SV_{DD}	—

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
SD_RX00_B	Receive Data (negative)	D28	I	SV_{DD}	—
SD_REF_CLK1	SerDes Bank 1 PLL Reference Clock	A35	I	XV_{DD}	—
SD_REF_CLK1_B	SerDes Bank 1 PLL Reference Clock Complement	B35	I	XV_{DD}	—
SD_REF_CLK2	SerDes Bank 2Reference Clock	V34	I	XV_{DD}	—
SD_REF_CLK2_B	SerDes Bank 2 Reference Clock Complement	V33	I	XV_{DD}	—
SD_REF_CLK3	SerDes Bank 2 and 3 PLL Reference Clock	AC32	I	XV_{DD}	31
SD_REF_CLK3_B	SerDes Bank 2 and 3 PLL Reference Clock Complement	AC31	I	XV_{DD}	31
General-Purpose Input/Output					
GPIO00	General Purpose Input / Output	AL21	I/O	OV_{DD}	—
GPIO01	General Purpose Input / Output	AK22	I/O	OV_{DD}	—
GPIO02	General Purpose Input / Output	AM20	I/O	OV_{DD}	—
GPIO03	General Purpose Input / Output	AN20	I/O	OV_{DD}	—
GPIO04	General Purpose Input / Output	AH21	I/O	OV_{DD}	—
GPIO05	General Purpose Input / Output	AJ21	I/O	OV_{DD}	—
GPIO06	General Purpose Input / Output	AK21	I/O	OV_{DD}	—
GPIO07	General Purpose Input / Output	AG20	I/O	OV_{DD}	—
GPIO08/UART1_SOUT	General Purpose Input / Output	AL22	I/O	OV_{DD}	—
GPIO09/UART2_SOUT	General Purpose Input / Output	AJ22	I/O	OV_{DD}	—
GPIO10/UART1_SIN	General Purpose Input / Output	AR23	I/O	OV_{DD}	—
GPIO11/UART2_SIN	General Purpose Input / Output	AN23	I/O	OV_{DD}	—
GPIO12/UART1_RTS_B/UART3_SOUT	General Purpose Input / Output	AM22	I/O	OV_{DD}	—
GPIO13 /UART2_RTS_B/UART4_SOUT	General Purpose Input / Output	AK23	I/O	OV_{DD}	—
GPIO14/UART1_CTS_B/UART3_SIN	General Purpose Input / Output	AP22	I/O	OV_{DD}	—
GPIO15/UART2_CTS_B/UART4_SIN	General Purpose Input / Output	AH23	I/O	OV_{DD}	—
GPIO16/IIC3_SCL/SDHC_CD_B	General Purpose Input / Output	AK13	I/O	OV_{DD}	—
GPIO17/IIC3_SDA/SDHC_WP	General Purpose Input / Output	AM14	I/O	OV_{DD}	—
GPIO18/DMA1_DREQ0_B	General Purpose Input / Output	AP21	I/O	OV_{DD}	—
GPIO19/DMA1_DACK0_B	General Purpose Input / Output	AL19	I/O	OV_{DD}	—
GPIO20/DMA2_DREQ0_B/ALT_MDVAL	General Purpose Input / Output	AJ20	I/O	OV_{DD}	—
GPIO21/IRQ3	General Purpose Input / Output	AJ15	I/O	OV_{DD}	—
GPIO22/IRQ4	General Purpose Input / Output	AH17	I/O	OV_{DD}	—

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
GPIO23/IRQ5	General Purpose Input / Output	AJ13	I/O	OV_{DD}	—
GPIO24/IRQ6	General Purpose Input / Output	AG17	I/O	OV_{DD}	—
GPIO25/IRQ7	General Purpose Input / Output	AM13	I/O	OV_{DD}	—
GPIO26/IRQ8	General Purpose Input / Output	AG13	I/O	OV_{DD}	—
GPIO27/IRQ9	General Purpose Input / Output	AK11	I/O	OV_{DD}	—
GPIO28/IRQ10	General Purpose Input / Output	AH14	I/O	OV_{DD}	—
GPIO29/IRQ11	General Purpose Input / Output	AL12	I/O	OV_{DD}	—
GPIO30/TSEC_1588_ALARM_OUT2	General Purpose Input / Output	AK35	I/O	LV_{DD}	24
GPIO31/TSEC_1588_PULSE_OUT2	General Purpose Input / Output	AJ34	I/O	LV_{DD}	24
System Control					
PORESET_B	Power On Reset	AP17	I	OV_{DD}	—
HRESET_B	Hard Reset	AR17	I/O	OV_{DD}	1, 2
RESET_REQ_B	Reset Request	AT16	O	OV_{DD}	3, 30
CKSTP_OUT_B	Checkstop Out	AM19	O	OV_{DD}	1, 2
Debug					
EVT0_B	Event 0	AJ17	I/O	OV_{DD}	19
EVT1_B	Event 1	AK17	I/O	OV_{DD}	—
EVT2_B	Event 2	AN16	I/O	OV_{DD}	—
EVT3_B	Event 3	AK16	I/O	OV_{DD}	—
EVT4_B	Event 4	AM16	I/O	OV_{DD}	—
EVT5_B/IIC4_SCL	Event 5	AG14	I/O	OV_{DD}	—
EVT6_B/IIC4_SDA	Event 6	AL15	I/O	OV_{DD}	—
EVT7_B/DMA2_DACK0_B/ALT_MSRCID0	Event 7	AG19	I/O	OV_{DD}	—
EVT8_B/DMA2_DDONE0_B/ ALT_MSRCID1	Event 8	AP20	I/O	OV_{DD}	—
EVT9_B/IRQ_OUT_B	Event 9	AK14	I/O	OV_{DD}	—
MDVAL	Debug Data Valid	AR15	O	OV_{DD}	—
MSRCID0	Debug Source ID 0	AH20	O	OV_{DD}	4, 19, 30
MSRCID1	Debug Source ID 1	AJ19	O	OV_{DD}	3, 30
MSRCID2	Debug Source ID 2	AH18	O	OV_{DD}	3, 30
ALT_MDVAL/DMA2_DREQ0_B/GPIO20	Alternate Debug Data Valid	AJ20	O	OV_{DD}	25
ALT_MSRCID0/DMA2_DACK0_B/EVT7_B	Alternate Debug Source ID 0	AG19	O	OV_{DD}	25
ALT_MSRCID1/DMA2_DDONE0_B/ EVT8_B	Alternate Debug Source ID 1	AP20	O	OV_{DD}	25

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
CLK_OUT	Clock Out	AK20	O	OV_{DD}	6
Clock					
RTC	Real Time Clock	AN24	I	OV_{DD}	—
SYSCLK	System Clock	AT23	I	OV_{DD}	—
JTAG					
TCK	Test Clock	AR22	I	OV_{DD}	—
TDI	Test Data In	AN17	I	OV_{DD}	7
TDO	Test Data Out	AP15	O	OV_{DD}	6
TMS	Test Mode Select	AR20	I	OV_{DD}	7
TRST_B	Test Reset	AR19	I	OV_{DD}	7
DFT					
SCAN_MODE_B	Scan Mode	AL17	I	OV_{DD}	12
TEST_SEL_B	Test Mode Select	AT21	I	OV_{DD}	12, 27
Power Management					
ASLEEP	Asleep	AR21	O	OV_{DD}	3, 30
Input / Output Voltage Select					
IO_VSEL0	I/O Voltage Select	AL18	I	OV_{DD}	29
IO_VSEL1	I/O Voltage Select	AP18	I	OV_{DD}	29
IO_VSEL2	I/O Voltage Select	AK18	I	OV_{DD}	29
IO_VSEL3	I/O Voltage Select	AM18	I	OV_{DD}	29
IO_VSEL4	I/O Voltage Select	AH19	I	OV_{DD}	29
Power and Ground Signals					
GND	Ground	C3	—	—	—
GND	Ground	B5	—	—	—
GND	Ground	F3	—	—	—
GND	Ground	E5	—	—	—
GND	Ground	D7	—	—	—
GND	Ground	C9	—	—	—
GND	Ground	B11	—	—	—
GND	Ground	J3	—	—	—
GND	Ground	H5	—	—	—
GND	Ground	G7	—	—	—
GND	Ground	F9	—	—	—

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
GND	Ground	E11	—	—	—
GND	Ground	D13	—	—	—
GND	Ground	C15	—	—	—
GND	Ground	K19	—	—	—
GND	Ground	B20	—	—	—
GND	Ground	B22	—	—	—
GND	Ground	E19	—	—	—
GND	Ground	L22	—	—	—
GND	Ground	J23	—	—	—
GND	Ground	A22	—	—	—
GND	Ground	L20	—	—	—
GND	Ground	A26	—	—	—
GND	Ground	A18	—	—	—
GND	Ground	E17	—	—	—
GND	Ground	F23	—	—	—
GND	Ground	J27	—	—	—
GND	Ground	F27	—	—	—
GND	Ground	G21	—	—	—
GND	Ground	K25	—	—	—
GND	Ground	B18	—	—	—
GND	Ground	L18	—	—	—
GND	Ground	J21	—	—	—
GND	Ground	M27	—	—	—
GND	Ground	G13	—	—	—
GND	Ground	F15	—	—	—
GND	Ground	H11	—	—	—
GND	Ground	J9	—	—	—
GND	Ground	K7	—	—	—
GND	Ground	L5	—	—	—
GND	Ground	M3	—	—	—
GND	Ground	R3	—	—	—
GND	Ground	P5	—	—	—
GND	Ground	N7	—	—	—
GND	Ground	M9	—	—	—

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
GND	Ground	V25	—	—	—
GND	Ground	R9	—	—	—
GND	Ground	T7	—	—	—
GND	Ground	U5	—	—	—
GND	Ground	U3	—	—	—
GND	Ground	Y3	—	—	—
GND	Ground	Y5	—	—	—
GND	Ground	W7	—	—	—
GND	Ground	V10	—	—	—
GND	Ground	AA9	—	—	—
GND	Ground	AB7	—	—	—
GND	Ground	AC5	—	—	—
GND	Ground	AD3	—	—	—
GND	Ground	AD9	—	—	—
GND	Ground	AE7	—	—	—
GND	Ground	AF5	—	—	—
GND	Ground	AG3	—	—	—
GND	Ground	AG9	—	—	—
GND	Ground	AH7	—	—	—
GND	Ground	AJ5	—	—	—
GND	Ground	AK3	—	—	—
GND	Ground	AN3	—	—	—
GND	Ground	AM5	—	—	—
GND	Ground	AL7	—	—	—
GND	Ground	AK9	—	—	—
GND	Ground	AJ11	—	—	—
GND	Ground	AH13	—	—	—
GND	Ground	AR5	—	—	—
GND	Ground	AP7	—	—	—
GND	Ground	AN9	—	—	—
GND	Ground	AM11	—	—	—
GND	Ground	AL13	—	—	—
GND	Ground	AK15	—	—	—
GND	Ground	AG18	—	—	—

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
GND	Ground	AR11	—	—	—
GND	Ground	AP13	—	—	—
GND	Ground	AN15	—	—	—
GND	Ground	AM17	—	—	—
GND	Ground	AK19	—	—	—
GND	Ground	AF13	—	—	—
GND	Ground	AR18	—	—	—
GND	Ground	AB27	—	—	—
GND	Ground	AP19	—	—	—
GND	Ground	AH22	—	—	—
GND	Ground	AM21	—	—	—
GND	Ground	AL29	—	—	—
GND	Ground	AR16	—	—	—
GND	Ground	AT22	—	—	—
GND	Ground	AP23	—	—	—
GND	Ground	AR32	—	—	—
GND	Ground	AK28	—	—	—
GND	Ground	AE27	—	—	—
GND	Ground	L16	—	—	—
GND	Ground	AP34	—	—	—
GND	Ground	AJ32	—	—	—
GND	Ground	AN30	—	—	—
GND	Ground	AH34	—	—	—
GND	Ground	AT36	—	—	—
GND	Ground	AL34	—	—	—
GND	Ground	AM32	—	—	—
GND	Ground	AE26	—	—	—
GND	Ground	AC26	—	—	—
GND	Ground	AA26	—	—	—
GND	Ground	W26	—	—	—
GND	Ground	U26	—	—	—
GND	Ground	R26	—	—	—
GND	Ground	N26	—	—	—
GND	Ground	M11	—	—	—

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
GND	Ground	P11	—	—	—
GND	Ground	T11	—	—	—
GND	Ground	V11	—	—	—
GND	Ground	Y11	—	—	—
GND	Ground	AB11	—	—	—
GND	Ground	AD11	—	—	—
GND	Ground	AE12	—	—	—
GND	Ground	AC12	—	—	—
GND	Ground	AA12	—	—	—
GND	Ground	W12	—	—	—
GND	Ground	U12	—	—	—
GND	Ground	R12	—	—	—
GND	Ground	N12	—	—	—
GND	Ground	M13	—	—	—
GND	Ground	P13	—	—	—
GND	Ground	T13	—	—	—
GND	Ground	V13	—	—	—
GND	Ground	Y13	—	—	—
GND	Ground	AB13	—	—	—
GND	Ground	AD13	—	—	—
GND	Ground	AE14	—	—	—
GND	Ground	AC14	—	—	—
GND	Ground	AA14	—	—	—
GND	Ground	W14	—	—	—
GND	Ground	U14	—	—	—
GND	Ground	R14	—	—	—
GND	Ground	N14	—	—	—
GND	Ground	L14	—	—	—
GND	Ground	M15	—	—	—
GND	Ground	P15	—	—	—
GND	Ground	T15	—	—	—
GND	Ground	V15	—	—	—
GND	Ground	Y15	—	—	—
GND	Ground	AB15	—	—	—

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
GND	Ground	AD15	—	—	—
GND	Ground	AF15	—	—	—
GND	Ground	W16	—	—	—
GND	Ground	AC16	—	—	—
GND	Ground	AA16	—	—	—
GND	Ground	AE16	—	—	—
GND	Ground	U16	—	—	—
GND	Ground	R16	—	—	—
GND	Ground	N16	—	—	—
GND	Ground	M17	—	—	—
GND	Ground	P17	—	—	—
GND	Ground	T17	—	—	—
GND	Ground	N18	—	—	—
GND	Ground	R18	—	—	—
GND	Ground	U18	—	—	—
GND	Ground	Y17	—	—	—
GND	Ground	AB17	—	—	—
GND	Ground	AD17	—	—	—
GND	Ground	AF17	—	—	—
GND	Ground	W18	—	—	—
GND	Ground	AC18	—	—	—
GND	Ground	AA18	—	—	—
GND	Ground	AE18	—	—	—
GND	Ground	AF19	—	—	—
GND	Ground	AD19	—	—	—
GND	Ground	AB19	—	—	—
GND	Ground	Y19	—	—	—
GND	Ground	V19	—	—	—
GND	Ground	T19	—	—	—
GND	Ground	P19	—	—	—
GND	Ground	M19	—	—	—
GND	Ground	N20	—	—	—
GND	Ground	R20	—	—	—
GND	Ground	U20	—	—	—

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
GND	Ground	AE20	—	—	—
GND	Ground	AA20	—	—	—
GND	Ground	AC20	—	—	—
GND	Ground	W20	—	—	—
GND	Ground	AF21	—	—	—
GND	Ground	AD21	—	—	—
GND	Ground	AB21	—	—	—
GND	Ground	Y21	—	—	—
GND	Ground	V21	—	—	—
GND	Ground	T21	—	—	—
GND	Ground	P21	—	—	—
GND	Ground	M21	—	—	—
GND	Ground	AE22	—	—	—
GND	Ground	AC22	—	—	—
GND	Ground	AA22	—	—	—
GND	Ground	W22	—	—	—
GND	Ground	U22	—	—	—
GND	Ground	R22	—	—	—
GND	Ground	N22	—	—	—
GND	Ground	AF23	—	—	—
GND	Ground	AD23	—	—	—
GND	Ground	AB23	—	—	—
GND	Ground	Y23	—	—	—
GND	Ground	V23	—	—	—
GND	Ground	T23	—	—	—
GND	Ground	P23	—	—	—
GND	Ground	M23	—	—	—
GND	Ground	L24	—	—	—
GND	Ground	N24	—	—	—
GND	Ground	R24	—	—	—
GND	Ground	U24	—	—	—
GND	Ground	W24	—	—	—
GND	Ground	AA24	—	—	—
GND	Ground	AC24	—	—	—

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
GND	Ground	AE24	—	—	—
GND	Ground	AF25	—	—	—
GND	Ground	AD25	—	—	—
GND	Ground	AB25	—	—	—
GND	Ground	Y25	—	—	—
GND	Ground	P27	—	—	—
GND	Ground	V17	—	—	—
GND	Ground	T25	—	—	—
GND	Ground	P25	—	—	—
GND	Ground	M25	—	—	—
GND	Ground	T27	—	—	—
GND	Ground	V27	—	—	—
GND	Ground	Y27	—	—	—
GND	Ground	AD27	—	—	—
GND	Ground	L12	—	—	—
XGND	SerDes Transceiver GND	AA30	—	—	—
XGND	SerDes Transceiver GND	AB32	—	—	—
XGND	SerDes Transceiver GND	AC30	—	—	—
XGND	SerDes Transceiver GND	AC34	—	—	—
XGND	SerDes Transceiver GND	AD30	—	—	—
XGND	SerDes Transceiver GND	AD31	—	—	—
XGND	SerDes Transceiver GND	AF32	—	—	—
XGND	SerDes Transceiver GND	AG30	—	—	—
XGND	SerDes Transceiver GND	D33	—	—	—
XGND	SerDes Transceiver GND	E28	—	—	—
XGND	SerDes Transceiver GND	E30	—	—	—
XGND	SerDes Transceiver GND	F32	—	—	—
XGND	SerDes Transceiver GND	G29	—	—	—
XGND	SerDes Transceiver GND	G31	—	—	—
XGND	SerDes Transceiver GND	H29	—	—	—
XGND	SerDes Transceiver GND	H32	—	—	—
XGND	SerDes Transceiver GND	H34	—	—	—
XGND	SerDes Transceiver GND	J29	—	—	—
XGND	SerDes Transceiver GND	J31	—	—	—

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
XGND	SerDes Transceiver GND	K28	—	—	—
XGND	SerDes Transceiver GND	K29	—	—	—
XGND	SerDes Transceiver GND	L29	—	—	—
XGND	SerDes Transceiver GND	L32	—	—	—
XGND	SerDes Transceiver GND	M30	—	—	—
XGND	SerDes Transceiver GND	N29	—	—	—
XGND	SerDes Transceiver GND	N30	—	—	—
XGND	SerDes Transceiver GND	N32	—	—	—
XGND	SerDes Transceiver GND	P29	—	—	—
XGND	SerDes Transceiver GND	P34	—	—	—
XGND	SerDes Transceiver GND	R30	—	—	—
XGND	SerDes Transceiver GND	R32	—	—	—
XGND	SerDes Transceiver GND	U29	—	—	—
XGND	SerDes Transceiver GND	U31	—	—	—
XGND	SerDes Transceiver GND	V29	—	—	—
XGND	SerDes Transceiver GND	V31	—	—	—
XGND	SerDes Transceiver GND	W30	—	—	—
XGND	SerDes Transceiver GND	Y32	—	—	—
XGND	SerDes Transceiver GND	AH31	—	—	—
SGND	SerDes Core Logic GND	A28	—	—	—
SGND	SerDes Core Logic GND	A32	—	—	—
SGND	SerDes Core Logic GND	A36	—	—	—
SGND	SerDes Core Logic GND	AA34	—	—	—
SGND	SerDes Core Logic GND	AB36	—	—	—
SGND	SerDes Core Logic GND	AD35	—	—	—
SGND	SerDes Core Logic GND	AE34	—	—	—
SGND	SerDes Core Logic GND	AF36	—	—	—
SGND	SerDes Core Logic GND	AG33	—	—	—
SGND	SerDes Core Logic GND	B30	—	—	—
SGND	SerDes Core Logic GND	B34	—	—	—
SGND	SerDes Core Logic GND	C29	—	—	—
SGND	SerDes Core Logic GND	C33	—	—	—
SGND	SerDes Core Logic GND	D31	—	—	—
SGND	SerDes Core Logic GND	D35	—	—	—

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
SGND	SerDes Core Logic GND	E35	—	—	—
SGND	SerDes Core Logic GND	G34	—	—	—
SGND	SerDes Core Logic GND	G36	—	—	—
SGND	SerDes Core Logic GND	J35	—	—	—
SGND	SerDes Core Logic GND	K33	—	—	—
SGND	SerDes Core Logic GND	L36	—	—	—
SGND	SerDes Core Logic GND	M34	—	—	—
SGND	SerDes Core Logic GND	N35	—	—	—
SGND	SerDes Core Logic GND	R33	—	—	—
SGND	SerDes Core Logic GND	R36	—	—	—
SGND	SerDes Core Logic GND	T35	—	—	—
SGND	SerDes Core Logic GND	U34	—	—	—
SGND	SerDes Core Logic GND	V36	—	—	—
SGND	SerDes Core Logic GND	W33	—	—	—
SGND	SerDes Core Logic GND	Y35	—	—	—
SGND	SerDes Core Logic GND	AH35	—	—	—
SGND	SerDes Core Logic GND	AH33	—	—	—
AGND_SRDS1	SerDes PLL1 GND	B33	—	—	—
AGND_SRDS2	SerDes PLL2 GND	T36	—	—	—
AGND_SRDS3	SerDes PLL3 GND	AE36	—	—	—
SENSEGND_PL1	Platform GND Sense 1	AF12	—	—	8
SENSEGND_PL2	Platform GND Sense 2	K27	—	—	8
SENSEGND_CA	Core Group A GND Sense	K17	—	—	8
SENSEGND_CB	Core Group B GND Sense	AG16	—	—	8
OVDD	General I/O Supply	AN22	—	OV_{DD}	—
OVDD	General I/O Supply	AJ14	—	OV_{DD}	—
OVDD	General I/O Supply	AJ18	—	OV_{DD}	—
OVDD	General I/O Supply	AL16	—	OV_{DD}	—
OVDD	General I/O Supply	AJ12	—	OV_{DD}	—
OVDD	General I/O Supply	AN18	—	OV_{DD}	—
OVDD	General I/O Supply	AG21	—	OV_{DD}	—
OVDD	General I/O Supply	AL20	—	OV_{DD}	—
OVDD	General I/O Supply	AT15	—	OV_{DD}	—
OVDD	General I/O Supply	AJ23	—	OV_{DD}	—

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
OVDD	General I/O Supply	AP16	—	OV_{DD}	—
OVDD	General I/O Supply	AR24	—	OV_{DD}	—
CVDD	eSPI Supply	AJ29	—	CV_{DD}	—
CVDD	eSPI Supply	AP29	—	CV_{DD}	—
GVDD	DDR Supply	B2	—	GV_{DD}	—
GVDD	DDR Supply	B8	—	GV_{DD}	—
GVDD	DDR Supply	B14	—	GV_{DD}	—
GVDD	DDR Supply	C18	—	GV_{DD}	—
GVDD	DDR Supply	C12	—	GV_{DD}	—
GVDD	DDR Supply	C6	—	GV_{DD}	—
GVDD	DDR Supply	D4	—	GV_{DD}	—
GVDD	DDR Supply	D10	—	GV_{DD}	—
GVDD	DDR Supply	D16	—	GV_{DD}	—
GVDD	DDR Supply	E14	—	GV_{DD}	—
GVDD	DDR Supply	E8	—	GV_{DD}	—
GVDD	DDR Supply	E2	—	GV_{DD}	—
GVDD	DDR Supply	F6	—	GV_{DD}	—
GVDD	DDR Supply	F12	—	GV_{DD}	—
GVDD	DDR Supply	AR8	—	GV_{DD}	—
GVDD	DDR Supply	G4	—	GV_{DD}	—
GVDD	DDR Supply	G10	—	GV_{DD}	—
GVDD	DDR Supply	G16	—	GV_{DD}	—
GVDD	DDR Supply	H14	—	GV_{DD}	—
GVDD	DDR Supply	H8	—	GV_{DD}	—
GVDD	DDR Supply	H2	—	GV_{DD}	—
GVDD	DDR Supply	J6	—	GV_{DD}	—
GVDD	DDR Supply	K10	—	GV_{DD}	—
GVDD	DDR Supply	K4	—	GV_{DD}	—
GVDD	DDR Supply	L2	—	GV_{DD}	—
GVDD	DDR Supply	L8	—	GV_{DD}	—
GVDD	DDR Supply	M6	—	GV_{DD}	—
GVDD	DDR Supply	N4	—	GV_{DD}	—
GVDD	DDR Supply	N10	—	GV_{DD}	—
GVDD	DDR Supply	P8	—	GV_{DD}	—

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
GVDD	DDR Supply	P2	—	GV_{DD}	—
GVDD	DDR Supply	R6	—	GV_{DD}	—
GVDD	DDR Supply	T10	—	GV_{DD}	—
GVDD	DDR Supply	T4	—	GV_{DD}	—
GVDD	DDR Supply	J12	—	GV_{DD}	—
GVDD	DDR Supply	U2	—	GV_{DD}	—
GVDD	DDR Supply	U8	—	GV_{DD}	—
GVDD	DDR Supply	V7	—	GV_{DD}	—
GVDD	DDR Supply	AK10	—	GV_{DD}	—
GVDD	DDR Supply	W10	—	GV_{DD}	—
GVDD	DDR Supply	AA6	—	GV_{DD}	—
GVDD	DDR Supply	AR2	—	GV_{DD}	—
GVDD	DDR Supply	Y2	—	GV_{DD}	—
GVDD	DDR Supply	Y8	—	GV_{DD}	—
GVDD	DDR Supply	AC2	—	GV_{DD}	—
GVDD	DDR Supply	AD6	—	GV_{DD}	—
GVDD	DDR Supply	AE10	—	GV_{DD}	—
GVDD	DDR Supply	AE4	—	GV_{DD}	—
GVDD	DDR Supply	AF2	—	GV_{DD}	—
GVDD	DDR Supply	AF8	—	GV_{DD}	—
GVDD	DDR Supply	AB4	—	GV_{DD}	—
GVDD	DDR Supply	AB10	—	GV_{DD}	—
GVDD	DDR Supply	AC8	—	GV_{DD}	—
GVDD	DDR Supply	AG6	—	GV_{DD}	—
GVDD	DDR Supply	AH10	—	GV_{DD}	—
GVDD	DDR Supply	AH4	—	GV_{DD}	—
GVDD	DDR Supply	AJ2	—	GV_{DD}	—
GVDD	DDR Supply	AJ8	—	GV_{DD}	—
GVDD	DDR Supply	AR14	—	GV_{DD}	—
GVDD	DDR Supply	AK6	—	GV_{DD}	—
GVDD	DDR Supply	AL4	—	GV_{DD}	—
GVDD	DDR Supply	AL10	—	GV_{DD}	—
GVDD	DDR Supply	AM2	—	GV_{DD}	—
GVDD	DDR Supply	AM8	—	GV_{DD}	—

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
GVDD	DDR Supply	AP10	—	GV_{DD}	—
GVDD	DDR Supply	AN12	—	GV_{DD}	—
GVDD	DDR Supply	AN6	—	GV_{DD}	—
GVDD	DDR Supply	AP4	—	GV_{DD}	—
BVDD	Local Bus Supply	B24	—	BV_{DD}	—
BVDD	Local Bus Supply	K22	—	BV_{DD}	—
BVDD	Local Bus Supply	F20	—	BV_{DD}	—
BVDD	Local Bus Supply	F26	—	BV_{DD}	—
BVDD	Local Bus Supply	E24	—	BV_{DD}	—
BVDD	Local Bus Supply	E22	—	BV_{DD}	—
BVDD	Local Bus Supply	K24	—	BV_{DD}	—
BVDD	Local Bus Supply	H20	—	BV_{DD}	—
BVDD	Local Bus Supply	H18	—	BV_{DD}	—
SVDD	SerDes Core Logic Supply	A30	—	SV_{DD}	—
SVDD	SerDes Core Logic Supply	A34	—	SV_{DD}	—
SVDD	SerDes Core Logic Supply	AA33	—	SV_{DD}	—
SVDD	SerDes Core Logic Supply	AB35	—	SV_{DD}	—
SVDD	SerDes Core Logic Supply	AD36	—	SV_{DD}	—
SVDD	SerDes Core Logic Supply	AE33	—	SV_{DD}	—
SVDD	SerDes Core Logic Supply	AF35	—	SV_{DD}	—
SVDD	SerDes Core Logic Supply	AG34	—	SV_{DD}	—
SVDD	SerDes Core Logic Supply	B28	—	SV_{DD}	—
SVDD	SerDes Core Logic Supply	B32	—	SV_{DD}	—
SVDD	SerDes Core Logic Supply	B36	—	SV_{DD}	—
SVDD	SerDes Core Logic Supply	C31	—	SV_{DD}	—
SVDD	SerDes Core Logic Supply	C34	—	SV_{DD}	—
SVDD	SerDes Core Logic Supply	C35	—	SV_{DD}	—
SVDD	SerDes Core Logic Supply	D29	—	SV_{DD}	—
SVDD	SerDes Core Logic Supply	E36	—	SV_{DD}	—
SVDD	SerDes Core Logic Supply	F34	—	SV_{DD}	—
SVDD	SerDes Core Logic Supply	G35	—	SV_{DD}	—
SVDD	SerDes Core Logic Supply	J36	—	SV_{DD}	—
SVDD	SerDes Core Logic Supply	K34	—	SV_{DD}	—
SVDD	SerDes Core Logic Supply	L35	—	SV_{DD}	—

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
SVDD	SerDes Core Logic Supply	M33	—	SV_{DD}	—
SVDD	SerDes Core Logic Supply	N36	—	SV_{DD}	—
SVDD	SerDes Core Logic Supply	R34	—	SV_{DD}	—
SVDD	SerDes Core Logic Supply	R35	—	SV_{DD}	—
SVDD	SerDes Core Logic Supply	U33	—	SV_{DD}	—
SVDD	SerDes Core Logic Supply	V35	—	SV_{DD}	—
SVDD	SerDes Core Logic Supply	W34	—	SV_{DD}	—
SVDD	SerDes Core Logic Supply	Y36	—	SV_{DD}	—
SVDD	SerDes Core Logic Supply	AH36	—	SV_{DD}	—
XVDD	SerDes Transceiver Supply	AA29	—	XV_{DD}	—
XVDD	SerDes Transceiver Supply	AB30	—	XV_{DD}	—
XVDD	SerDes Transceiver Supply	AB31	—	XV_{DD}	—
XVDD	SerDes Transceiver Supply	AC33	—	XV_{DD}	—
XVDD	SerDes Transceiver Supply	AD32	—	XV_{DD}	—
XVDD	SerDes Transceiver Supply	AE30	—	XV_{DD}	—
XVDD	SerDes Transceiver Supply	AF31	—	XV_{DD}	—
XVDD	SerDes Transceiver Supply	E32	—	XV_{DD}	—
XVDD	SerDes Transceiver Supply	E33	—	XV_{DD}	—
XVDD	SerDes Transceiver Supply	F28	—	XV_{DD}	—
XVDD	SerDes Transceiver Supply	F30	—	XV_{DD}	—
XVDD	SerDes Transceiver Supply	G32	—	XV_{DD}	—
XVDD	SerDes Transceiver Supply	H31	—	XV_{DD}	—
XVDD	SerDes Transceiver Supply	H33	—	XV_{DD}	—
XVDD	SerDes Transceiver Supply	J28	—	XV_{DD}	—
XVDD	SerDes Transceiver Supply	J30	—	XV_{DD}	—
XVDD	SerDes Transceiver Supply	J32	—	XV_{DD}	—
XVDD	SerDes Transceiver Supply	K30	—	XV_{DD}	—
XVDD	SerDes Transceiver Supply	L30	—	XV_{DD}	—
XVDD	SerDes Transceiver Supply	L31	—	XV_{DD}	—
XVDD	SerDes Transceiver Supply	M29	—	XV_{DD}	—
XVDD	SerDes Transceiver Supply	N31	—	XV_{DD}	—
XVDD	SerDes Transceiver Supply	P30	—	XV_{DD}	—
XVDD	SerDes Transceiver Supply	P33	—	XV_{DD}	—
XVDD	SerDes Transceiver Supply	R29	—	XV_{DD}	—

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
XVDD	SerDes Transceiver Supply	R31	—	XV_{DD}	—
XVDD	SerDes Transceiver Supply	T29	—	XV_{DD}	—
XVDD	SerDes Transceiver Supply	T32	—	XV_{DD}	—
XVDD	SerDes Transceiver Supply	U30	—	XV_{DD}	—
XVDD	SerDes Transceiver Supply	V30	—	XV_{DD}	—
XVDD	SerDes Transceiver Supply	V32	—	XV_{DD}	—
XVDD	SerDes Transceiver Supply	W29	—	XV_{DD}	—
XVDD	SerDes Transceiver Supply	Y31	—	XV_{DD}	—
XVDD	SerDes Transceiver Supply	AH32	—	XV_{DD}	—
LVDD	Ethernet Controller 1 and 2 Supply	AK33	—	LV_{DD}	—
LVDD	Ethernet Controller 1 and 2 Supply	AP31	—	LV_{DD}	—
LVDD	Ethernet Controller 1 and 2 Supply	AL31	—	LV_{DD}	—
LVDD	Ethernet Controller 1 and 2 Supply	AN33	—	LV_{DD}	—
LVDD	Ethernet Controller 1 and 2 Supply	AJ35	—	LV_{DD}	—
LVDD	Ethernet Controller 1 and 2 Supply	AR35	—	LV_{DD}	—
LVDD	Ethernet Controller 1 and 2 Supply	AM35	—	LV_{DD}	—
POVDD	Fuse Programming Override Supply	AT17	—	POV_{DD}	34
VDD_PL	Platform Supply	M26	—	V_{DD}_PL	—
VDD_PL	Platform Supply	P26	—	V_{DD}_PL	—
VDD_PL	Platform Supply	T26	—	V_{DD}_PL	—
VDD_PL	Platform Supply	V26	—	V_{DD}_PL	—
VDD_PL	Platform Supply	Y26	—	V_{DD}_PL	—
VDD_PL	Platform Supply	AB26	—	V_{DD}_PL	—
VDD_PL	Platform Supply	AD26	—	V_{DD}_PL	—
VDD_PL	Platform Supply	N11	—	V_{DD}_PL	—
VDD_PL	Platform Supply	R11	—	V_{DD}_PL	—
VDD_PL	Platform Supply	W11	—	V_{DD}_PL	—
VDD_PL	Platform Supply	AA11	—	V_{DD}_PL	—
VDD_PL	Platform Supply	AE11	—	V_{DD}_PL	—
VDD_PL	Platform Supply	M12	—	V_{DD}_PL	—
VDD_PL	Platform Supply	P12	—	V_{DD}_PL	—
VDD_PL	Platform Supply	T12	—	V_{DD}_PL	—
VDD_PL	Platform Supply	V12	—	V_{DD}_PL	—
VDD_PL	Platform Supply	Y12	—	V_{DD}_PL	—

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
VDD_PL	Platform Supply	AB12	—	V_{DD}_PL	—
VDD_PL	Platform Supply	AD12	—	V_{DD}_PL	—
VDD_PL	Platform Supply	AE13	—	V_{DD}_PL	—
VDD_PL	Platform Supply	AE15	—	V_{DD}_PL	—
VDD_PL	Platform Supply	V16	—	V_{DD}_PL	—
VDD_PL	Platform Supply	AE17	—	V_{DD}_PL	—
VDD_PL	Platform Supply	L11	—	V_{DD}_PL	—
VDD_PL	Platform Supply	AE19	—	V_{DD}_PL	—
VDD_PL	Platform Supply	U11	—	V_{DD}_PL	—
VDD_PL	Platform Supply	AC11	—	V_{DD}_PL	—
VDD_PL	Platform Supply	V20	—	V_{DD}_PL	—
VDD_PL	Platform Supply	AE21	—	V_{DD}_PL	—
VDD_PL	Platform Supply	V22	—	V_{DD}_PL	—
VDD_PL	Platform Supply	U13	—	V_{DD}_PL	—
VDD_PL	Platform Supply	R27	—	V_{DD}_PL	—
VDD_PL	Platform Supply	U23	—	V_{DD}_PL	—
VDD_PL	Platform Supply	W23	—	V_{DD}_PL	—
VDD_PL	Platform Supply	AA27	—	V_{DD}_PL	—
VDD_PL	Platform Supply	AC27	—	V_{DD}_PL	—
VDD_PL	Platform Supply	AE23	—	V_{DD}_PL	—
VDD_PL	Platform Supply	M24	—	V_{DD}_PL	—
VDD_PL	Platform Supply	P24	—	V_{DD}_PL	—
VDD_PL	Platform Supply	T24	—	V_{DD}_PL	—
VDD_PL	Platform Supply	V24	—	V_{DD}_PL	—
VDD_PL	Platform Supply	Y24	—	V_{DD}_PL	—
VDD_PL	Platform Supply	AB24	—	V_{DD}_PL	—
VDD_PL	Platform Supply	AD24	—	V_{DD}_PL	—
VDD_PL	Platform Supply	N25	—	V_{DD}_PL	—
VDD_PL	Platform Supply	R25	—	V_{DD}_PL	—
VDD_PL	Platform Supply	U25	—	V_{DD}_PL	—
VDD_PL	Platform Supply	W25	—	V_{DD}_PL	—
VDD_PL	Platform Supply	AA25	—	V_{DD}_PL	—
VDD_PL	Platform Supply	AC25	—	V_{DD}_PL	—
VDD_PL	Platform Supply	N27	—	V_{DD}_PL	—

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
VDD_PL	Platform Supply	U27	—	V_{DD}_PL	—
VDD_PL	Platform Supply	W28	—	V_{DD}_PL	—
VDD_PL	Platform Supply	AE25	—	V_{DD}_PL	—
VDD_PL	Platform Supply	AF24	—	V_{DD}_PL	—
VDD_PL	Platform Supply	AF22	—	V_{DD}_PL	—
VDD_PL	Platform Supply	AF20	—	V_{DD}_PL	—
VDD_PL	Platform Supply	AF16	—	V_{DD}_PL	—
VDD_PL	Platform Supply	W13	—	V_{DD}_PL	—
VDD_PL	Platform Supply	AF18	—	V_{DD}_PL	—
VDD_PL	Platform Supply	V14	—	V_{DD}_PL	—
VDD_PL	Platform Supply	V18	—	V_{DD}_PL	—
VDD_PL	Platform Supply	L13	—	V_{DD}_PL	—
VDD_PL	Platform Supply	L15	—	V_{DD}_PL	—
VDD_PL	Platform Supply	L17	—	V_{DD}_PL	—
VDD_PL	Platform Supply	L19	—	V_{DD}_PL	—
VDD_PL	Platform Supply	L21	—	V_{DD}_PL	—
VDD_PL	Platform Supply	L23	—	V_{DD}_PL	—
VDD_PL	Platform Supply	L25	—	V_{DD}_PL	—
VDD_PL	Platform Supply	AF14	—	V_{DD}_PL	—
VDD_PL	Platform Supply	N23	—	V_{DD}_PL	—
VDD_PL	Platform Supply	R23	—	V_{DD}_PL	—
VDD_PL	Platform Supply	AA23	—	V_{DD}_PL	—
VDD_PL	Platform Supply	AC23	—	V_{DD}_PL	—
VDD_PL	Platform Supply	U21	—	V_{DD}_PL	—
VDD_PL	Platform Supply	W21	—	V_{DD}_PL	—
VDD_PL	Platform Supply	U15	—	V_{DD}_PL	—
VDD_PL	Platform Supply	AC21	—	V_{DD}_PL	—
VDD_PL	Platform Supply	AD22	—	V_{DD}_PL	—
VDD_PL	Platform Supply	M22	—	V_{DD}_PL	—
VDD_PL	Platform Supply	N13	—	V_{DD}_PL	—
VDD_PL	Platform Supply	AC13	—	V_{DD}_PL	—
VDD_PL	Platform Supply	P22	—	V_{DD}_PL	—
VDD_PL	Platform Supply	T22	—	V_{DD}_PL	—
VDD_PL	Platform Supply	Y22	—	V_{DD}_PL	—

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
VDD_PL	Platform Supply	AB22	—	V_{DD}_PL	—
VDD_PL	Platform Supply	AA13	—	V_{DD}_PL	—
VDD_PL	Platform Supply	R13	—	V_{DD}_PL	—
VDD_PL	Platform Supply	M14	—	V_{DD}_PL	—
VDD_PL	Platform Supply	U17	—	V_{DD}_PL	—
VDD_PL	Platform Supply	U19	—	V_{DD}_PL	—
VDD_PL	Platform Supply	T14	—	V_{DD}_PL	—
VDD_PL	Platform Supply	AD14	—	V_{DD}_PL	—
VDD_PL	Platform Supply	AD16	—	V_{DD}_PL	—
VDD_PL	Platform Supply	AD18	—	V_{DD}_PL	—
VDD_PL	Platform Supply	AD20	—	V_{DD}_PL	—
VDD_PL	Platform Supply	Y14	—	V_{DD}_PL	—
VDD_CA	Core/L2 Group A (0-3) Supply	T20	—	V_{DD}_CA	—
VDD_CA	Core/L2 Group A (0-3) Supply	P20	—	V_{DD}_CA	—
VDD_CA	Core/L2 Group A (0-3) Supply	R21	—	V_{DD}_CA	—
VDD_CA	Core/L2 Group A (0-3) Supply	R19	—	V_{DD}_CA	—
VDD_CA	Core/L2 Group A (0-3) Supply	P14	—	V_{DD}_CA	—
VDD_CA	Core/L2 Group A (0-3) Supply	N19	—	V_{DD}_CA	—
VDD_CA	Core/L2 Group A (0-3) Supply	M20	—	V_{DD}_CA	—
VDD_CA	Core/L2 Group A (0-3) Supply	N21	—	V_{DD}_CA	—
VDD_CA	Core/L2 Group A (0-3) Supply	M16	—	V_{DD}_CA	—
VDD_CA	Core/L2 Group A (0-3) Supply	N15	—	V_{DD}_CA	—
VDD_CA	Core/L2 Group A (0-3) Supply	P16	—	V_{DD}_CA	—
VDD_CA	Core/L2 Group A (0-3) Supply	T16	—	V_{DD}_CA	—
VDD_CA	Core/L2 Group A (0-3) Supply	R17	—	V_{DD}_CA	—
VDD_CA	Core/L2 Group A (0-3) Supply	T18	—	V_{DD}_CA	—
VDD_CA	Core/L2 Group A (0-3) Supply	R15	—	V_{DD}_CA	—
VDD_CA	Core/L2 Group A (0-3) Supply	N17	—	V_{DD}_CA	—
VDD_CA	Core/L2 Group A (0-3) Supply	M18	—	V_{DD}_CA	—
VDD_CA	Core/L2 Group A (0-3) Supply	P18	—	V_{DD}_CA	—
VDD_CB	Core/L2 Group B (4-7) Supply	W15	—	V_{DD}_CB	28
VDD_CB	Core/L2 Group B (4-7) Supply	W19	—	V_{DD}_CB	28
VDD_CB	Core/L2 Group B (4-7) Supply	AA19	—	V_{DD}_CB	28
VDD_CB	Core/L2 Group B (4-7) Supply	Y20	—	V_{DD}_CB	28

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
VDD_CB	Core/L2 Group B (4-7) Supply	AB14	—	V_{DD}_CB	29
VDD_CB	Core/L2 Group B (4-7) Supply	AA21	—	V_{DD}_CB	28
VDD_CB	Core/L2 Group B (4-7) Supply	Y16	—	V_{DD}_CB	28
VDD_CB	Core/L2 Group B (4-7) Supply	AA15	—	V_{DD}_CB	28
VDD_CB	Core/L2 Group B (4-7) Supply	AC15	—	V_{DD}_CB	28
VDD_CB	Core/L2 Group B (4-7) Supply	AA17	—	V_{DD}_CB	28
VDD_CB	Core/L2 Group B (4-7) Supply	AC17	—	V_{DD}_CB	28
VDD_CB	Core/L2 Group B (4-7) Supply	W17	—	V_{DD}_CB	28
VDD_CB	Core/L2 Group B (4-7) Supply	Y18	—	V_{DD}_CB	28
VDD_CB	Core/L2 Group B (4-7) Supply	AB18	—	V_{DD}_CB	28
VDD_CB	Core/L2 Group B (4-7) Supply	AB16	—	V_{DD}_CB	28
VDD_CB	Core/L2 Group B (4-7) Supply	AC19	—	V_{DD}_CB	28
VDD_CB	Core/L2 Group B (4-7) Supply	AB20	—	V_{DD}_CB	28
AVDD_CC1	Core Cluster PLL1 Supply	A20	—	—	13
AVDD_CC2	Core Cluster PLL2 Supply	A21	—	—	13
AVDD_CC3	Core Cluster PLL3 Supply	AT18	—	—	13
AVDD_CC4	Core Cluster PLL4 Supply	AT19	—	—	13
AVDD_PLAT	Platform PLL Supply	AT20	—	—	13
AVDD_DDR	DDR PLL Supply	A19	—	—	13
AVDD_SRDS1	SerDes PLL1 Supply	A33	—	—	13
AVDD_SRDS2	SerDes PLL2 Supply	U36	—	—	13
AVDD_SRDS3	SerDes PLL3 Supply	AE35	—	—	13
SENSEVDD_PL1	Platform Vdd Sense	AF11	—	—	8
SENSEVDD_PL2	Platform Vdd Sense	L27	—	—	8
SENSEVDD_CA	Core Group A Vdd Sense	K16	—	—	8
SENSEVDD_CB	Core Group B Vdd Sense	AG15	—	—	8
Analog Signals					
MVREF	SSTL_1.5/1.8 Reference Voltage	B19	I	$GV_{DD}/2$	—
SD_IMP_CAL_TX	SerDes Tx Impedance Calibration	AF30	I	200Ω (±1%) to XVDD	22
SD_IMP_CAL_RX	SerDes Rx Impedance Calibration	B27	I	200Ω (±1%) to SVDD	23
TEMP_ANODE	Temperature Diode Anode	C21	—	internal diode	9

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
TEMP_CATHODE	Temperature Diode Cathode	B21	—	internal diode	9
No Connection Pins					
NC01	No Connection	J13	—	—	11
NC02	No Connection	AB28	—	—	11
NC03	No Connection	E16	—	—	11
NC04	No Connection	AC29	—	—	11
NC05	No Connection	K14	—	—	11
NC06	No Connection	C26	—	—	11
NC07	No Connection	E27	—	—	11
NC08	No Connection	AE29	—	—	11
NC09	No Connection	AG26	—	—	11
NC10	No Connection	AF26	—	—	11
NC11	No Connection	AC28	—	—	11
NC12	No Connection	AA28	—	—	11
NC13	No Connection	J15	—	—	11
NC14	No Connection	J14	—	—	11
NC15	No Connection	AD29	—	—	11
NC16	No Connection	J16	—	—	11
NC17	No Connection	AG28	—	—	11
NC18	No Connection	AE28	—	—	11
NC19	No Connection	AF28	—	—	11
NC20	No Connection	H27	—	—	11
NC21	No Connection	H12	—	—	11
NC22	No Connection	H13	—	—	11
NC23	No Connection	H16	—	—	11
NC24	No Connection	AH30	—	—	11
NC25	No Connection	AH29	—	—	11
NC26	No Connection	Y28	—	—	11
NC27	No Connection	AN13	—	—	11
NC28	No Connection	J11	—	—	11
NC29	No Connection	AB29	—	—	11
NC30	No Connection	K11	—	—	11
NC31	No Connection	AD28	—	—	11

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
NC32	No Connection	A27	—	—	11
NC33	No Connection	K15	—	—	11
NC34	No Connection	H15	—	—	11
NC35	No Connection	K13	—	—	11
NC36	No Connection	K12	—	—	11
NC37	No Connection	G17	—	—	11
NC38	No Connection	H17	—	—	11
NC39	No Connection	C20	—	—	11
NC40	No Connection	F18	—	—	11
NC41	No Connection	AT14	—	—	11
NC42	No Connection	C27	—	—	11
NC43	No Connection	R28	—	—	11
NC44	No Connection	AM12	—	—	11
NC45	No Connection	AP11	—	—	11
NC46	No Connection	U28	—	—	11
NC47	No Connection	AG29	—	—	11
NC48	No Connection	G27	—	—	11
NC49	No Connection	V28	—	—	11
NC50	No Connection	AG27	—	—	11
NC51	No Connection	E18	—	—	11
NC52	No Connection	F17	—	—	11
NC53	No Connection	AF27	—	—	11
NC54	No Connection	AP14	—	—	11
NC55	No Connection	D26	—	—	11
NC56	No Connection	C19	—	—	11
NC57	No Connection	D18	—	—	11
NC58	No Connection	D27	—	—	11
NC59	No Connection	B26	—	—	11
NC60	No Connection	AF29	—	—	11
NC61	No Connection	T28	—	—	11
NC62	No Connection	W27	—	—	11
Reserved Pins					
Reserve01	—	AN28	—	—	11
Reserve02	—	AL25	—	—	11

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
Reserve03	—	AR28	—	—	11
Reserve04	—	AH25	—	—	11
Reserve05	—	AJ25	—	—	11
Reserve06	—	AH24	—	—	11
Reserve07	—	AK26	—	—	11
Reserve08	—	AM27	—	—	11
Reserve09	—	AR27	—	—	11
Reserve10	—	AK25	—	—	11
Reserve11	—	AH27	—	—	11
Reserve12	—	AR26	—	—	11
Reserve13	—	AT27	—	—	11
Reserve14	—	AH26	—	—	11
Reserve15	—	AJ27	—	—	11
Reserve16	—	AT26	—	—	11
Reserve17	—	AN26	—	—	11
Reserve18	—	AJ26	—	—	11
Reserve19	—	AG25	—	—	11
Reserve20	—	AP27	—	—	11
Reserve21	—	AM25	—	—	11
Reserve22	—	AP28	—	—	11
Reserve23	—	AL28	—	—	11
Reserve24	—	AG24	—	—	11
Reserve25	—	AP26	—	—	11
Reserve26	—	AJ24	—	—	11
Reserve27	—	AM28	—	—	11
Reserve28	—	AR25	—	—	11
Reserve29	—	AM24	—	—	11
Reserve30	—	AL27	—	—	11
Reserve31	—	AT28	—	—	11
Reserve32	—	AT25	—	—	11
Reserve33	—	AL24	—	—	11
Reserve34	—	AL26	—	—	11
Reserve35	—	AK24	—	—	11
Reserve36	—	AN25	—	—	11

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
Reserve37	—	AK27	—	—	11
Reserve38	—	AP25	—	—	11
Reserve39	—	AM26	—	—	11
Reserve40	—	AN27	—	—	11
Reserve41	—	AL33	—	—	11
Reserve42	—	C32	—	—	11
Reserve43	—	U35	—	—	11
Reserve44	—	AD34	—	—	11
Reserve45	—	D32	—	—	11
Reserve46	—	U32	—	—	11
Reserve47	—	AD33	—	—	11
Reserve48	—	N28	—	GND	20
Reserve49	—	AG11	—	GND	20
Reserve50	—	L28	—	GND	20
Reserve51	—	AG12	—	GND	20
Reserve52	—	M28	—	GND	20
Reserve53	—	AH12	—	GND	20
Reserve54	—	P28	—	GND	20
Reserve55	—	AH11	—	GND	20
Reserve56	—	A25	—	—	11

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note

Notes:

1. Recommend that a weak pull-up resistor (2–10 KΩ) be placed on this pin to OVDD.
2. This pin is an open drain signal.
3. This pin is a reset configuration pin. It has a weak (~20 KΩ) internal pull-up P-FET that is enabled only when the processor is in the reset state. This pull-up is designed such that it can be overpowered by an external 4.7-KΩ resistor. However, if the signal is intended to be high after reset, and if there is any device on the net that might pull down the value of the net at reset, a pull up or active driver is needed.
4. Functionally, this pin is an output, but structurally it is an I/O because it either samples configuration input during reset or because it has other manufacturing test functions. This pin is therefore described as an I/O for boundary scan.
5. Recommend that a weak pull-up resistor (2–10 KΩ) be placed on this pin to BVDD in order to ensure no random chip select assertion due to possible noise, and so forth.
6. This output is actively driven during reset rather than being three-stated during reset.
7. These JTAG pins have weak (~20 KΩ) internal pull-up P-FETs that are always enabled.
8. These pins are connected to the correspondent power and ground nets internally and may be connected as a differential pair to be used by the voltage regulators with remote sense function.
9. These pins may be connected to a temperature diode monitoring device such as the Analog Devices, ADT7461A™. If a temperature diode monitoring device is not connected, these pins may be connected to test point or left as a no connect.
10. If this pin is connected to a device that pulls down during reset, an external pull-up is required to drive this pin to a safe state during reset.
11. Do not connect.
12. These are test signals for factory use only and must be pulled up (100 Ω–1 KΩ) to OVDD for normal machine operation.
13. Independent supplies derived from board V_{DD_PL} (core clusters, platform, DDR) or SV_{DD} (SerDes).
14. Recommend that a pull-up resistor (1 KΩ) be placed on this pin to OVDD if I^2C interface is used.
15. This pin requires an external 1 KΩ pull-down resistor to prevent PHY from seeing a valid Transmit Enable before it is actively driven.
16. For DDR2, Dn_MDIC[0] is grounded through an 18.2-Ω (full-strength mode) or 36.4-Ω (half-strength mode) precision 1% resistor and Dn_MDIC[1] is connected to GVDD through an 18.2-Ω (full-strength mode) or 36.4-Ω (half-strength mode) precision 1% resistor. These pins are used for automatic calibration of the DDR2 IOs. For DDR3, Dn_MDIC[0] is grounded through an 20-Ω (full-strength mode) or 40.2-Ω (half-strength mode) precision 1% resistor and Dn_MDIC[1] is connected to GVDD through an 20-Ω (full-strength mode) or 40.2-Ω (half-strength mode) precision 1% resistor. These pins are used for automatic calibration of the DDR3 IOs.
17. These pins must be left floating.
18. These pins must be pulled up to 1.2 V through a 180 Ω ± 1% resistor for EM2_MDC and a 330 Ω ± 1% resistor for EM2_MDIO.
19. Pin has a weak (~20 KΩ) internal pull-up.
20. These pins must be pulled to ground (GND)
21. Ethernet MII Management Interface 2 pins function as open drain I/Os. The interface conforms to 1.2 V nominal voltage levels. LV_{DD} must be powered to use this interface.
22. This pin requires a 200-Ω pull-up to XV_{DD}.
23. This pin requires a 200-Ω pull-up to SV_{DD}.
24. GPIO is on LV_{DD} power plane, not OV_{DD}.
25. Functionally, this pin is an I/O, but may act as an output only or an input only depending on the pin mux configuration defined by the RCW.
26. See Section 3.6, “Connection Recommendations,” for additional details on this signal.

Table 1. Pins List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note

27. For reduced core (cores 4–7 disabled) P4080/P4081 mode, this signal must be pulled low to GND.
28. For reduced core (cores 4–7 disabled) P4080/P4081 mode, voltage rail may be connected to GND to reduce power consumption.
29. Warning, incorrect voltage select settings can lead to irreversible device damage. This pin requires an external pull-up or pulldown resistor to configure IO_VSEL[n] state. See Section 3.2, "Supply Power Setting."
30. Pin must NOT be pulled down during power-on reset. This pin may be pulled up, driven high, or if there are any externally connected devices, left in tristate.
31. SD_REF_CLK3 is required when either bank 2 or bank 3 are enabled. See Section 2.20.2, "SerDes Reference Clocks."
32. SDHC_DAT[4:7] require CV_{DD} = 3.3 V when muxed extended SDHC data signals are enabled via the RCW[SPI] field.
33. The *cfg_dram_type* (LA[24]) reset configuration pin must select the correct DRAM type such that the selected DDR GV_{DD} = XV_{DD}. Incorrect voltage select settings can lead to irreversible device damage.
34. See Section 2.2, "Power Sequencing," and Section 5, "Security Fuse Processor," for additional details on this signal.
35. For systems which boot from Local Bus (GPCM)-controlled NOR flash or (FCM)-controlled NAND flash, a pull up on LGPL4 is required.

2 Electrical Characteristics

This section provides the AC and DC electrical specifications for the chip. The chip is currently targeted to these specifications, some of which are independent of the I/O cell but are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 Overall DC Electrical Characteristics

This section describes the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

This table provides the absolute maximum ratings.

Table 2. Absolute Maximum Ratings[1]

Characteristic	Symbol	Max Value	Unit	Note
Core Group A (cores 0–3) supply voltage	SENSEVDD_CA	–0.3 to 1.1	V	10
Core Group B (cores 4–7) supply voltage	SENSEVDD_CB	–0.3 to 1.1	V	10
Platform supply voltage	SENSEVDD_PL*n*	–0.3 to 1.1	V	10, 11
PLL supply voltage (Core, Platform, DDR)	AV_{DD}	–0.3 to 1.1	V	—
PLL supply voltage (SerDes, filtered from SV_{DD})	AV_{DD_SRDS}	–0.3 to 1.1	V	—
Fuse programming override supply	POV_{DD}	–0.3 to 1.65	V	—
DUART, I^2C, eSHDC, DMA, MPIC, GPIO, system control and power management, clocking, debug, I/O voltage select, and JTAG I/O voltage	OV_{DD}	–0.3 to 3.63	V	—
eSPI	CV_{DD}	–0.3 to 3.63 –0.3 to 2.75 –0.3 to 1.98	V	—

Table 2. Absolute Maximum Ratings[1] (continued)

Characteristic	Symbol	Max Value	Unit	Note
DDR DRAM I/O voltage DDR2 DDR3	GV_{DD}	 –0.3 to 1.98 –0.3 to 1.65	V	—
Enhanced local bus I/O voltage	BV_{DD}	–0.3 to 3.63 –0.3 to 2.75 –0.3 to 1.98	V	—
Core power supply for SerDes transceivers	SV_{DD}	–0.3 to 1.1	V	—
Pad power supply for SerDes transceivers	XV_{DD}	–0.3 to 1.98 –0.3 to 1.65	V	9
Ethernet I/O, Ethernet Management Interface 1 (EMI1), USB, 1588, GPIO	LV_{DD}	–0.3 to 3.63 –0.3 to 2.75 –0.3 to 1.98	V	—
Ethernet Management Interface 2 (EMI2)	—	–0.3 to 1.32	V	8

Table 2. Absolute Maximum Ratings[1] (continued)

Characteristic		Symbol	Max Value	Unit	Note
Input voltage	DDR2/DDR3 DRAM signals	MV_{IN}	–0.3 to (GV_{DD} + 0.3)	V	2, 5
	DDR2/DDR3 DRAM reference	$MV_{REF}n$	–0.3 to (GV_{DD}/2 + 0.3)	V	2, 5
	Ethernet signals (except EMI2)	LV_{IN}	–0.3 to (LV_{DD} + 0.3)	V	4, 5
	eSPI	CV_{IN}	–0.3 to (CV_{DD} + 0.3)	V	5, 6
	Enhanced local bus signals	BV_{IN}	–0.3 to (BV_{DD} + 0.3)	V	5, 7
	DUART, I^2C, eSHDC, DMA, MPIC, GPIO, system control and power management, clocking, debug, I/O voltage select, and JTAG I/O voltage	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	3, 5
	SerDes signals	XV_{IN}	–0.4 to (XV_{DD} + 0.3)	V	5
	Ethernet Management Interface 2 signals	—	–0.3 to (1.2 + 0.3)	V	—
Storage temperature range		T_{STG}	–55 to 150	°C	—

Notes:

1. Functional operating conditions are given in Table 3. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution:** MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
3. **Caution:** OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. **Caution:** LV_{IN} must not exceed LV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
5. (C,X,B,G,L,O)V_{IN} and $MV_{REF}n$ may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 7.
6. **Caution:** CV_{IN} must not exceed CV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
7. **Caution:** BV_{IN} must not exceed BV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
8. Ethernet MII Management Interface 2 pins function as open drain I/Os. The interface conforms to 1.2 V nominal voltage levels. LV_{DD} must be powered to use this interface.
9. XV_{DD} must be at the same voltage level as GV_{DD}. The *cfg_dram_type* (LA[24]) reset configuration pin must select the correct DRAM type such that the selected DDR GV_{DD} = XV_{DD}. Incorrect voltage select settings can lead to irreversible device damage.
10. Supply voltage specified at the voltage sense pin. Voltage input pins must be regulated to provide specified voltage at the sense pin.
11. Implementation may choose either SENSEVDD_PL*n* pin for feedback loop. If the platform and core groups are supplied by a single regulator, it is recommended that SENSEVDD_CA be used.

2.1.2 Recommended Operating Conditions

This table provides the recommended operating conditions for this device. Note that the values shown are the recommended operating conditions and proper device operation outside these conditions is not guaranteed.

Table 3. Recommended Operating Conditions

Characteristic	Symbol	Recommended Value	Unit	Note
Core group A (cores 0–3) supply voltage	SENSEVDD_CA	1.0 V ± 50 mV	V	5

Table 3. Recommended Operating Conditions (continued)

Characteristic		Symbol	Recommended Value	Unit	Note
Core group B (cores 4–7) supply voltage		SENSEVDD_CB	1.0 V ± 50 mV	V	5
Platform supply voltage		SENSEVDD_PL*n*	1.0 V ± 50 mV	V	5
PLL supply voltage (core, platform, DDR)		AV_{DD}	1.0 V ± 50 mV	V	—
PLL supply voltage (SerDes)		AV_{DD_SRDS}	1.0 V ± 50 mV	V	—
Fuse Programming Override Supply		POV_{DD}	1.5 V ± 75 mV	V	2
DUART, I^2C, eSHDC, DMA, MPIC, GPIO, system control and power management, clocking, debug, I/O voltage select, and JTAG I/O voltage		OV_{DD}	3.3 V ± 165 mV	V	—
eSPI		CV_{DD}	3.3 V ± 165 mV 2.5 V ± 125 mV 1.8 V ± 90 mV		—
DDR DRAM I/O voltage	DDR2 DDR3	GV_{DD}	1.8 V ± 90 mV 1.5 V ± 75 mV	V	—
Enhanced local bus I/O voltage		BV_{DD}	3.3 V ± 165 mV 2.5 V ± 125 mV 1.8 V ± 90 mV	V	—
Core power supply for SerDes transceivers		SV_{DD}	1.0 V ± 50 mV	V	—
Pad power supply for SerDes transceivers		XV_{DD}	1.8 V ± 90 mV 1.5 V ± 75 mV	V	—
Ethernet I/O, Ethernet management interface 1 (EMI1), USB, 1588, GPIO		LV_{DD}	3.3 V ± 165 mV 2.5 V ± 125 mV 1.8 V ± 90 mV	V	1, 4
Input voltage	DDR2/DDR3 DRAM signals	MV_{IN}	GND to GV_{DD}	V	—
	DDR2 DRAM reference	$MV_{REF}n$	$GV_{DD}/2$ ± 2%	V	—
	DDR3 DRAM reference	$MV_{REF}n$	$GV_{DD}/2$ ± 1%	V	—
	Ethernet signals (except EMI2), USB, 1588, GPIO	LV_{IN}	GND to LV_{DD}	V	—
	eSPI	CV_{IN}	GND to CV_{DD}	V	—
	Local bus signals	BV_{IN}	GND to BV_{DD}	V	—
	DUART, I^2C, eSHDC, DMA, MPIC, GPIO, system control and power management, clocking, debug, I/O voltage select, and JTAG I/O voltage	OV_{IN}	GND to OV_{DD}	V	—
	Serdes signals	XV_{IN}	GND to XV_{DD}	V	—
	Ethernet management interface 2 (EMI2) signals	—	GND to 1.2V	V	3
Operating temperature range	Normal operation	T_A, T_J	T_A = 0 (min) to T_J = 105(max)	°C	—
	Secure Boot Fuse Programming	T_A, T_J	T_A = 0 (min) to T_J = 70 (max)	°C	2

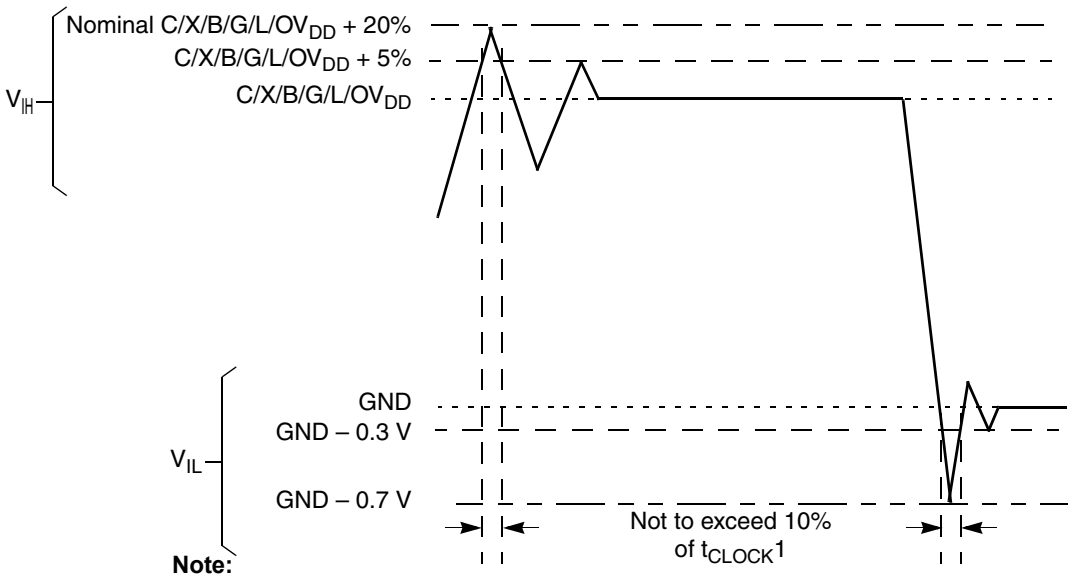
Table 3. Recommended Operating Conditions (continued)

Characteristic	Symbol	Recommended Value	Unit	Note

Note:

1. Selecting RGMII limits to LV_{DD} = 2.5 V
2. POV_{DD} must be supplied 1.5 V and the chip must operate in the specified fuse programming temperature range only during secure boot fuse programming. For all other operating conditions, POV_{DD} must be tied to GND, subject to the power sequencing constraints shown in Section 2.2, "Power Sequencing."
3. Ethernet MII Management Interface 2 pins function as open drain I/Os. The interface conforms to 1.2-V nominal voltage levels. LV_{DD} must be powered to use this interface.
4. If LV_{DD} = 3.3 V or 1.8 V is selected for USB, all other signals associated with LV_{DD} must meet all V_{IH} requirements associated with external device inputs.
5. Supply voltage specified at the voltage sense pin. Voltage input pins must be regulated to provide specified voltage at the sense pin.

This figure shows the undershoot and overshoot voltages at the interfaces of the chip.



Note:
t_{CLOCK} refers to the clock period associated with the respective interface:
For I2C OV_{DD}, t_{CLOCK} references SYSCLK.
For DDR GV_{DD}, t_{CLOCK} references SYSCLK.
For eSPI CV_{DD}, t_{CLOCK} references SPI_CLK.
For eLBC BV_{DD}, t_{CLOCK} references LCLK.
For SerDes XV_{DD}, t_{CLOCK} references SD_REF_CLK.
For dTSEC LV_{DD}, t_{CLOCK} references EC_GTX_CLK125.
For JTAG OV_{DD}, t_{CLOCK} references TCK.

Figure 7. Overshoot/Undershoot Voltage for $BV_{DD}/GV_{DD}/LV_{DD}/OV_{DD}/XV_{DD}/CV_{DD}$

The core and platform voltages must always be provided at nominal 1.0 V. See Table 3 for actual recommended core voltage. Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in Table 3. The input voltage threshold scales with respect to the associated I/O supply voltage. CV_{DD}, BV_{DD}, OV_{DD} and LV_{DD} based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR SDRAM interface uses differential receivers referenced by the externally supplied $MV_{REF}n$ signal (nominally set to $GV_{DD}/2$)

as is appropriate for the SSTL_1.5/SSTL_1.8 electrical signaling standard. The DDR DQS receivers cannot be operated in single-ended fashion. The complement signal must be properly driven and cannot be grounded.

2.1.3 Output Driver Characteristics

This table provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Table 4. Output Drive Capability

Driver Type	Output Impedance (Ω)	Supply Voltage	Note
Local bus interface utilities signals	45	BV_{DD} = 3.3 V BV_{DD} = 2.5 V BV_{DD} = 1.8 V	—
DDR2 signal	18 35 (half-strength mode)	GV_{DD} = 1.8 V	1
DDR3 signal	17 40 (half-strength mode)	GV_{DD} = 1.5 V	1
dTSEC/10/100 signals	45	LV_{DD} = 3.3 V LV_{DD} = 2.5 V LV_{DD} = 1.8 V	—
DUART, JTAG, System Control	45	OV_{DD} = 3.3 V	—
I^2C	45	OV_{DD} = 3.3 V	—
eSPI	45	CV_{DD} = 3.3 V CV_{DD} = 2.5 V CV_{DD} = 1.8 V	—

Note:
1. The drive strength of the DDR2 or DDR3 interface in half-strength mode is at T_j = 105 °C and at GV_{DD} (min).

2.2 Power Sequencing

The chip requires its power rails to be applied in a specific sequence in order to ensure proper device operation. The requirements are as follows for power up:

1. Bring up OV_{DD}, LV_{DD}, BV_{DD}, CV_{DD}. Drive POV_{DD} = GND.
   — PORESET_B input must be driven asserted and held during this step.
   — IO_VSEL inputs must be driven during this step and held stable during normal operation.
2. Bring up V_{DD_PL}, V_{DD_CA}, V_{DD_CB}, SV_{DD}, AV_{DD} (cores, platform, DDR, SerDes).
3. Bring up GV_{DD}, XV_{DD}.
4. Negate PORESET_B input as long as the required assertion/hold time has been met per Table 15.
5. For secure boot fuse programming: After negation of PORESET_B, drive POV_{DD} = 1.5 V after a required minimum delay per Table 5. After fuse programming is completed, it is required to return POV_{DD} = GND before the system is power cycled (PORESET_B assertion) or powered down (V_{DD_PL} ramp down) per the required timing specified in Table 5. See Section 5, "Security Fuse Processor," for additional details.

NOTE

Only two secure boot fuse programming events are permitted per lifetime of a device.

No activity other than that required for secure boot fuse programming is permitted while POV_{DD} is driven to any voltage above GND, including the reading of the fuse block. The reading of the fuse block may only occur while POV_{DD} = GND.

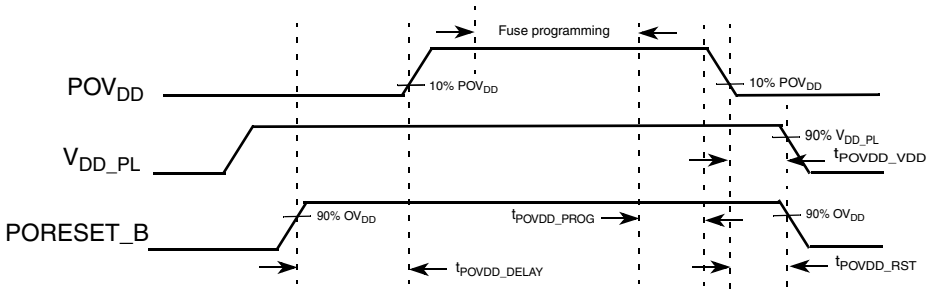
NOTE

While VDD is ramping, current may be supplied from VDD through the chip to GVDD. Nevertheless, GVDD from an external supply must follow the sequencing described in this section.

NOTE

Only 100,000 POR cycles are permitted per lifetime of a device.

This figure provides the POV_{DD} timing diagram.



NOTE: POV_{DD} must be stable at 1.5 V prior to initiating fuse programming.

Figure 8. POV_{DD} Timing Diagram

This table provides information on the power-down and power-up sequence parameters for POV_{DD}.

Table 5. POV_{DD} Timing[5]

Driver Type	Min	Max	Unit	Note
t_{POVDD_DELAY}	100	—	SYSCLKs	1
t_{POVDD_PROG}	0	—	µs	2
t_{POVDD_VDD}	0	—	µs	3
t_{POVDD_RST}	0	—	µs	4

Note:

1. Delay required from the negation of PORESET_B to driving POV_{DD} ramp up. Delay measured from PORESET_B negation at 90% OV_{DD} to 10% POV_{DD} ramp up.
2. Delay required from fuse programming finished to POV_{DD} ramp down start. Fuse programming must complete while POV_{DD} is stable at 1.5 V. No activity other than that required for secure boot fuse programming is permitted while POV_{DD} driven to any voltage above GND, including the reading of the fuse block. The reading of the fuse block may only occur while POV_{DD} = GND. After fuse programming is completed, it is required to return POV_{DD} = GND.
3. Delay required from POV_{DD} ramp down complete to V_{DD_PL} ramp down start. POV_{DD} must be grounded to minimum 10% POV_{DD} before V_{DD_PL} is at 90% V_{DD}.
4. Delay required from POV_{DD} ramp down complete to PORESET_B assertion. POV_{DD} must be grounded to minimum 10% POV_{DD} before PORESET_B assertion reaches 90% OV_{DD}.
5. Only two secure boot fuse programming events are permitted per lifetime of a device.

All supplies must be at their stable values within 75 ms.

Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90% of their value before the voltage rails on the current step reach 10% of theirs.

WARNING

Incorrect voltage select settings can lead to irreversible device damage. See Section 3.2, "Supply Power Setting."

NOTE

From a system standpoint, if any of the I/O power supplies ramp prior to the V_{DD_PL}, V_{DD_CA}, or V_{DD_CB} supplies, the I/Os associated with that I/O supply may drive a logic one or zero during power-up, and extra current may be drawn by the device.

2.3 Power Down Requirements

The power-down cycle must complete such that power supply values are below 0.4 V before a new power-up cycle can be started.

If performing secure boot fuse programming per Section 2.2, "Power Sequencing," it is required that POV_{DD} = GND before the system is power cycled (PORESET_B assertion) or powered down (V_{DD_PL} ramp down) per the required timing specified in Table 5.

2.4 Power Characteristics

This table shows the power dissipations of the V_{DD_CA}, V_{DD_CB}, SV_{DD}, and V_{DD_PL} supply for various operating platform clock frequencies versus the core and DDR clock frequencies.

Table 6. P4080/P4081 Power Dissipation

Power Mode	Core Freq (MHz)	Plat Freq (MHz)	DDR Data Rate (MHz)	PME/FM Freq (MHz)	V_{DD_CA}, V_{DD_CB}, V_{DD_PL}, SV_{DD} (V)	Junction Temperature (°C)	Core and Platform Power[1] (W)	V_{DD_PL} Power[6] (W)	V_{DD_CA} Power[6] (W)	V_{DD_CB} Power[6] (W)	SV_{DD} Power[6] (W)	Note
Typical	1000	600	1000	350	1.0	65	13	—	—	—	—	2, 3
Thermal						105	19	—	—	—	—	5
Maximum							20.5	11.6	5.3	5.3	1.7	4
Typical	1200	600	1200	450	1.0	65	14	—	—	—	—	2, 3
Thermal						105	20.4	—	—	—	—	5
Maximum							22	12.5	5.7	5.7	1.7	4
Typical	1333	667	1333	533	1.0	65	15	—	—	—	—	2, 3
Thermal						105	26.3	—	—	—	—	5
Maximum							28	15.4	7.4	7.4	1.7	4
Typical	1500	800	1300	600	1.0	65	16	—	—	—	—	2, 3
Thermal						105	28	—	—	—	—	5
Maximum							30	16.6	7.8	7.8	1.7	4

Table 6. P4080/P4081 Power Dissipation (continued)

Power Mode	Core Freq (MHz)	Plat Freq (MHz)	DDR Data Rate (MHz)	PME/FM Freq (MHz)	V_{DD_CA}, V_{DD_CB}, V_{DD_PL}, SV_{DD} (V)	Junction Temperature (°C)	Core and Platform Power[1] (W)	V_{DD_PL} Power[6] (W)	V_{DD_CA} Power[6] (W)	V_{DD_CB} Power[6] (W)	SV_{DD} Power[6] (W)	Note

Note:

1. Combined power of VDD_PL, VDD_CA, VDD_CB, SVDD at 1.0 V with both DDR controllers and all SerDes banks active. Does not include I/O power.
2. Multicore activity factor of 0.7 relative to Dhrystone and 0.4 platform activity factor.
3. Typical power based on nominal processed device.
4. Maximum power with Dhrystone executing at 100% on all eight cores and executing DMA on the platform.
5. Thermal power assumes multicore activity factor of 0.7 relative to Dhrystone and executing DMA on the platform.
6. Maximum power provided for power supply design sizing.

This table shows the estimated power dissipation on the AV_{DD} and AV_{DD_SRDS} supplies for the chip PLLs, at allowable voltage levels.

Table 7. AV_{DD} Power Dissipation

AV_{DD}s	Typical	Maximum	Unit	Note
AV_{DD_DDR1}	5	15	mW	1
AV_{DD_CC1}	5	15	mW	
AV_{DD_CC2}	5	15	mW	
AV_{DD_CC3}	5	15	mW	
AV_{DD_PLAT}	5	15	mW	
AV_{DD_SRDS1}	—	36	mW	2
AV_{DD_SRDS2}	—	36	mW	
AV_{DD_SRDS3}	—	36	mW	

Note:

1. V_{DD_PL}, V_{DD_CA}, V_{DD_CB} = 1.0 V, T_A = 80 °C, T_J = 105 °C
2. SV_{DD} = 1.0 V, T_A = 80 °C, T_J = 105 °C

This table shows the estimated I/O power supply values for the chip.

Table 8. I/O Power Supply Estimated Value

Interface	Parameter	Symbol	Typical	Maximum	Unit	Notes
DDR2 64 bits per controller	667 MHz data rate	GVdd (1.8 V)	1.173	2.933	W	1, 2, 5, 6
	800 MHz data rate		1.213	3.030		
	1066 MHz data rate		1.290	3.224		
	1200 MHz data rate		1.328	3.322		
	1333 MHz data rate		1.368	3.419		

Table 8. I/O Power Supply Estimated Value (continued)

Interface	Parameter	Symbol	Typical	Maximum	Unit	Notes
DDR3 64 bits per controller	667 MHz data rate	GVdd (1.5 V)	0.733	1.833	W	1, 2, 5, 6
	800 MHz data rate		0.758	1.894		
	1066 MHz data rate		0.806	2.015		
	1200 MHz data rate		0.830	2.076		
	1333 MHz data rate		0.855	2.137		
HSSI: PCI-e, SGMII, SATA, SRIO, Aurora, Debug, XAUI	x1, 1.25 G-baud	XVdd (1.5 V)	0.078	0.087	W	1
	x2, 1.25 G-baud		0.119	0.134		
	x4, 1.25 G-baud		0.202	0.226		
	x8, 1.25 G-baud		0.367	0.411		
	x1, 2.5/3.0/3.125/5.0 G-baud		0.088	0.099		
	x2, 2.5/3.0/3.125/5.0 G-baud		0.139	0.156		
	x4, 2.5/3.0/3.125/5.0 G-baud		0.241	0.270		
	x8, 2.5/3.0/3.125/5.0 G-baud		0.447	0.501		
dTSEC per controller	RGMII	LVdd (2.5 V)	0.075	0.100	W	1, 3, 6
IEEE 1588	—	LVdd (2.5 V)	0.004	0.005	W	1, 3, 6
eLBC	32-bit, 100 MHz	BVdd (1.8 V)	0.048	0.120	W	1, 3, 6
		BVdd (2.5 V)	0.072	0.193		
		BVdd (3.3 V)	0.120	0.277		
	16-bit, 100 MHz	BVdd (1.8 V)	0.021	0.030	W	1, 3, 6
		BVdd (2.5 V)	0.036	0.046		
		BVdd (3.3 V)	0.057	0.076		
eSDHC	—	Ovdd (3.3 V)	0.014	0.150	W	1, 3, 6
eSPI	—	CVdd (1.8 V)	0.004	0.005	W	1, 3, 6
		CVdd (2.5 V)	0.006	0.008		
		CVdd (3.3 V)	0.010	0.013		
USB	—	LVdd (1.8 V)	0.006	0.008	W	1, 3, 6
		LVdd (2.5 V)	0.008	0.010		
		LVdd (3.3 V)	0.012	0.015		
I2C	—	OVdd (3.3 V)	0.002	0.003	W	1, 3, 6
DUART	—	OV_{DD} (3.3 V)	0.006	0.008	W	1, 3, 6
GPIO	x8	1.8 V	0.005	0.006	W	1, 3, 4,6
		2.5 V	0.007	0.009		
		3.3 V	0.009	0.011		
Others (Reset, System Clock, JTAG & Misc)	—	3.3 V	0.030	0.015	W	1, 3, 6

Table 8. I/O Power Supply Estimated Value (continued)

Interface	Parameter	Symbol	Typical	Maximum	Unit	Notes

Note:
1. The typical values are estimates and based on simulations at 65 °C.
2. Typical DDR power numbers are based on one 2-rank DIMM with 40% utilization.
3. Assuming 15 pF total capacitance load
4. GPIOs are supported on 1.8 V, 2.5 V, and 3.3 V rails.
5. Maximum DDR power numbers are based on one 2-rank DIMM with 100% utilization.
6. The maximum values are estimated and they are based on simulations at 105 °C. The values are not intended to be used as the maximum guaranteed current.

This table shows the estimated power dissipation on the POV_{DD} supply for the chip, at allowable voltage levels.

Table 9. POV_{DD} Power Dissipation

Supply	Maximum	Unit	Note
POV_{DD}	450	mW	1

Note:
1. To ensure device reliability, fuse programming must be performed within the recommended fuse programming temperature range per Table 3.

2.5 Thermal

This table shows the thermal characteristics for the chip.

Table 10. Package Thermal Characteristics [6]

Rating	Board	Symbol	Value	Unit	Note
Junction to ambient, natural convection	Single-layer board (1s)	$R_{\Theta JA}$	13	°C/W	1, 2
Junction to ambient, natural convection	Four-layer board (2s2p)	$R_{\Theta JA}$	10	°C/W	1, 3
Junction to ambient (at 200 ft./min.)	Single-layer board (1s)	$R_{\Theta JMA}$	9	°C/W	1, 2
Junction to ambient (at 200 ft./min.)	Four-layer board (2s2p)	$R_{\Theta JMA}$	7	°C/W	1, 2
Junction to board	—	$R_{\Theta JB}$	3	°C/W	3
Junction to case top	—	$R_{\Theta JCtop}$	0.37	°C/W	4
Junction to lid top	—	$R_{\Theta JClid}$	0.15	°C/W	5

Note:
1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51–3 and JESD51-6 with the board (JESD51–9) horizontal.
3. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51–8. Board temperature is measured on the top surface of the board near the package.
4. Junction-to-case-top at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.
5. Junction-to-lid-top thermal resistance determined using the using MIL-STD 883 Method 1012.1. However, instead of the cold plate, the lid top temperature is used here for the reference case temperature. Reported value does not include the thermal resistance of the interface layer between the package and cold plate.
6. See Section 3.8, “Thermal Management Information,” for additional details.

2.6 Input Clocks

2.6.1 System Clock (SYSCLK) Timing Specifications

This section provides the system clock DC and AC timing specifications.

2.6.1.1 System Clock DC Timing Specifications

This table provides the system clock (SYSCLK) DC specifications.

Table 11. SYSCLK DC Electrical Characteristics

At recommended operating conditions with OV_{DD} = 3.3 V, see Table 3.

Parameter	Symbol	Min	Typical	Max	Unit	Note
Input high voltage	V_{IH}	2.0	—	—	V	1
Input low voltage	V_{IL}	—	—	0.8	V	1
Input capacitance	C_{IN}	—	—	15	pf	—
Input current (OV_{IN}= 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	—	± 50	μA	2

Note:
1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol OV_{IN}, in this case, represents the OV_{IN} symbol referenced in Section 2.1.2, "Recommended Operating Conditions."

2.6.1.2 System Clock AC Timing Specifications

This table provides the system clock (SYSCLK) AC timing specifications.

Table 12. SYSCLK AC Timing Specifications

At recommended operating conditions with OV_{DD} = 3.3 V, see Table 3.

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Note
SYSCLK frequency	f_{SYSCLK}	83.3	—	133.3	MHz	1, 2
SYSCLK cycle time	t_{SYSCLK}	7.5	—	12	ns	1, 2
SYSCLK duty cycle	t_{KHK}/t_{SYSCLK}	40	—	60	%	2
SYSCLK slew rate	—	1	—	4	V/ns	3
SYSCLK peak period jitter	—	—	—	+/–150	ps	—
SYSCLK jitter phase noise at –56 dBc	—	—	—	500	KHz	4
AC Input Swing Limits at 3.3 V OV_{DD}	ΔV_{AC}	1.9	—	—	V	—

Notes:
1. **Caution:** The relevant clock ratio settings must be chosen such that the resulting SYSCLK frequency, do not exceed their respective maximum or minimum operating frequencies.
2. Measured at the rising edge and/or the falling edge at $OV_{DD}/2$.
3. Slew rate as measured from ± 0.3 $\Delta \mathbf{V_{AC}}$ at center of peak to peak voltage at clock input.
4. Phase noise is calculated as FFT of TIE jitter.

2.6.2 Spread Spectrum Sources

Spread spectrum clock sources are an increasingly popular way to control electromagnetic interference emissions (EMI) by spreading the emitted noise to a wider spectrum and reducing the peak noise magnitude in order to meet industry and government requirements. These clock sources intentionally add long-term jitter to diffuse the EMI spectral content. The jitter specification given in Table 13 considers short-term (cycle-to-cycle) jitter only. The clock generator's cycle-to-cycle output jitter must meet the chip input cycle-to-cycle jitter requirement. Frequency modulation and spread are separate concerns; the chip is compatible with spread spectrum sources if the recommendations listed in the following table are observed.

Table 13. Spread Spectrum Clock Source Recommendations

At recommended operating conditions with OVDD = 3.3 V, see Table 3.

Parameter	Min	Max	Unit	Note
Frequency modulation	—	60	kHz	—
Frequency spread	—	1.0	%	1, 2

Notes:
1. SYSCLK frequencies that result from frequency spreading and the resulting core frequency must meet the minimum and maximum specifications given in Table 12.
2. Maximum spread spectrum frequency may not result in exceeding any maximum operating frequency of the device.

CAUTION

The processor's minimum and maximum SYSCLK and core/platform/DDR frequencies must not be exceeded regardless of the type of clock source. Therefore, systems in which the processor is operated at its maximum rated core/platform/DDR frequency must avoid violating the stated limits by using down-spreading only.

2.6.3 Real Time Clock Timing

The real time clock timing (RTC) input is sampled by the platform clock. The output of the sampling latch is then used as an input to the counters of the PIC and the time base unit of the e500-mc; there is no need for jitter specification. The minimum period of the RTC signal must be greater than or equal to 16× the period of the platform clock with a 50% duty cycle. There is no minimum RTC frequency; RTC may be grounded if not needed.

2.6.4 dTSEC Gigabit Reference Clock Timing

This table provides the dTSEC gigabit reference clocks AC timing specifications.

Table 14. EC_GTX_CLK125 AC Timing Specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Note
EC_GTX_CLK125 frequency	t_{G125}	—	125	—	MHz	—
EC_GTX_CLK125 cycle time	t_{G125}	—	8	—	ns	—
EC_GTX_CLK125 rise and fall time LV_{DD} = 2.5 V	t_{G125R}/t_{G125F}	—	—	0.75	ns	1
EC_GTX_CLK125 duty cycle 1000Base-T for RGMII	t_{G125H}/t_{G125}	47	—	53	%	2

Table 14. EC_GTX_CLK125 AC Timing Specifications (continued)

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Note
EC_GTX_CLK125 jitter	—	—	—	± 150	ps	2

Notes:
1. Rise and fall times for EC_GTX_CLK125 are measured from 0.5 and 2.0 V for LV_{DD} = 2.5 V.
2. EC_GTX_CLK125 is used to generate the GTX clock for the dTSEC transmitter with 2% degradation. EC_GTX_CLK125 duty cycle can be loosened from 47%/53% as long as the PHY device can tolerate the duty cycle generated by the dTSEC GTX_CLK. See Section 2.12.2.2, "RGMII AC Timing Specifications," for duty cycle for 10Base-T and 100Base-T reference clock.

2.6.5 Other Input Clocks

A description of the overall clocking of this device is available in the *P4080 QorIQ Integrated Multicore Communication Processor Family Reference Manual* in the form of a clock subsystem block diagram. For information about the input clock requirements of functional blocks sourced external of the device, such as SerDes, Ethernet Management, eSDHC, Local Bus, see the specific interface section.

2.7 RESET Initialization

This section describes the AC electrical specifications for the RESET initialization timing requirements. This table describes the AC electrical specifications for the RESET initialization timing.

Table 15. RESET Initialization Timing Specifications

Parameter/Condition	Min	Max	Unit	Note
Required assertion time of PORESET_B	1	—	ms	3
Required input assertion time of HRESET_B	32	—	SYSCLKs	1, 2
Input setup time for POR configs with respect to negation of PORESET_B	4	—	SYSCLKs	1
Input hold time for all POR configs with respect to negation of PORESET_B	2	—	SYSCLKs	1
Maximum valid-to-high impedance time for actively driven POR configs with respect to negation of PORESET_B	—	5	SYSCLKs	1

Notes:
1. SYSCLK is the primary clock input for the chip.
2. The device asserts HRESET_B as an output when PORESET_B is asserted to initiate the power-on reset process. The device releases HRESET_B sometime after PORESET_B is negated. The exact sequencing of HRESET_B negation is documented in Section 4.4.1 "Power-On Reset Sequence," of the *P4080 QorIQ Integrated Multicore Communication Processor Family Reference Manual*.
3. PORESET_B must be driven asserted before the core and platform power supplies are powered up.

This table provides the PLL lock times.

Table 16. PLL Lock Times

Parameter/Condition	Min	Max	Unit	Note
PLL lock times	—	100	µs	—

2.8 Power-on Ramp Rate

This section describes the AC electrical specifications for the power-on ramp rate requirements. Controlling the maximum power-on ramp rate is required to avoid falsely triggering the ESD circuitry. This table provides the power supply ramp rate specifications.

Table 17. Power Supply Ramp Rate

Parameter	Min	Max	Unit	Note
Required ramp rate for all voltage supplies (including OV_{DD}/CV_{DD}/ GV_{DD}/BV_{DD}/SV_{DD}/XV_{DD}/LV_{DD}, all core and platform V_{DD} supplies, MV_{REF} and all AV_{DD} supplies.)	—	36000	V/s	1, 2

Note:

1. Ramp rate is specified as a linear ramp from 10 to 90%. If non-linear (for example, exponential), the maximum rate of change from 200 to 500 mV is the most critical as this range might falsely trigger the ESD circuitry.
2. Over full recommended operating temperature range (see Table 3).

2.9 DDR2 and DDR3 SDRAM Controller

This section describes the DC and AC electrical specifications for the DDR2 and DDR3 SDRAM controller interface. Note that the required GV_{DD}(typ) voltage is 1.8 V or 1.5 V when interfacing to DDR2 or DDR3 SDRAM respectively.

2.9.1 DDR2 and DDR3 SDRAM Interface DC Electrical Characteristics

This table provides the recommended operating conditions for the DDR SDRAM controller when interfacing to DDR2 SDRAM.

Table 18. DDR2 SDRAM Interface DC Electrical Characteristics

At recommended operating condition with GV_{DD} = 1.8 V[1], see Table 3

Parameter/Condition	Symbol	Min	Max	Unit	Note
I/O reference voltage	MVREFn	0.49 × GVDD	0.51 × GVDD	V	2, 3, 4
Input high voltage	V_{IH}	MVREF*n* + 0.125	—	V	5
Input low voltage	V_{IL}	—	MVREF*n* – 0.125	V	5
I/O leakage current	I_{OZ}	–50	50	μA	6
Output high current (V_{OUT} = 1.420 V)	I_{OH}	—	–13.4	mA	7, 8
Output low current (V_{OUT} = 0.280 V)	I_{OL}	13.4	—	mA	7, 8

Notes:

1. GV_{DD} is expected to be within 50 mV of the DRAM's voltage supply at all times. The DRAM's and memory controller's voltage supply may or may not be from the same source.
2. MVREF*n* is expected to be equal to 0.5 × GV_{DD} and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MVREF*n* may not exceed the MVREF*n* DC level by more than ±1% of the DC value (that is, ±18 mV).
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made, and it is expected to be equal to MVREFn with a min value of MVREF*n* – 0.04 and a max value of MVREF*n* + 0.04. This rail must track variations in the DC level of MVREF*n*.
4. The voltage regulator for MVREF*n* must meet the specifications stated in Table 21.
5. Input capacitance load for DQ, DQS, and DQS_B are available in the IBIS models.
6. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.
7. See the IBIS model for the complete output IV curve characteristics.
8. IOH and IOL are measured at GVDD = 1.7 V.

This table provides the recommended operating conditions for the DDR SDRAM controller when interfacing to DDR3 SDRAM.

Table 19. DDR3 SDRAM Interface DC Electrical Characteristics

At recommended operating condition with GV_{DD} = 1.5 V[1], see Table 3

Parameter/Condition	Symbol	Min	Max	Unit	Note
I/O reference voltage	MVREFn	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2, 3, 4
Input high voltage	V_{IH}	MVREF*n* + 0.100	GV_{DD}	V	5
Input low voltage	V_{IL}	GND	MVREF*n* – 0.100	V	5
I/O leakage current	I_{OZ}	–50	50	μA	6

Notes:

1. GV_{DD} is expected to be within 50 mV of the DRAM's voltage supply at all times. The DRAM's and memory controller's voltage supply may or may not be from the same source.
2. MVREF*n* is expected to be equal to 0.5 × GV_{DD} and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MVREF*n* may not exceed the MVREFn DC level by more than ±1% of the DC value (that is, ±15mV).
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made, and it is expected to be equal to MVREF*n* with a min value of MVREF*n* – 0.04 and a max value of MVREF*n* + 0.04. This rail must track variations in the DC level of MVREF*n*.
4. The voltage regulator for MVREF*n* must meet the specifications stated in Table 21.
5. Input capacitance load for DQ, DQS, and DQS_B are available in the IBIS models.
6. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.

This table provides the DDR controller interface capacitance for DDR2 and DDR3.

Table 20. DDR2 and DDR3 SDRAM Capacitance

At recommended operating conditions with GV_{DD} of 1.8 V for DDR2 or 1.5 V for DDR3, see Table 3.

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input/output capacitance: DQ, DQS, DQS_B	C_{IO}	6	8	pF	1, 2
Delta input/output capacitance: DQ, DQS, DQS_B	C_{DIO}	—	0.5	pF	1, 2

Note:

1. This parameter is sampled. GVDD = 1.8 V ± 0.1 V (for DDR2), f = 1 MHz, T_A = 25°C, V_{OUT} = GVDD/2, V_{OUT} (peak-to-peak) = 0.2 V.
2. This parameter is sampled. GVDD = 1.5 V ± 0.075 V (for DDR3), f = 1 MHz, T_A = 25°C, V_{OUT} = GVDD/2, V_{OUT} (peak-to-peak) = 0.150 V.

This table provides the current-draw characteristics for MVREFn.

Table 21. Current-Draw Characteristics for MVREF*n*

For recommended operating conditions, see Table 3.

Parameter/Condition	Symbol	Min	Max	Unit	Note
Current draw for DDR2 SDRAM for MVREF*n*	MVREF*n*	—	1500	μA	—
Current draw for DDR3 SDRAM for MVREF*n*	MVREF*n*	—	500	μA	—

2.9.2 DDR2 and DDR3 SDRAM Interface AC Timing Specifications

This section provides the AC timing specifications for the DDR SDRAM controller interface. The DDR controller supports both DDR2 and DDR3 memories. Note that the required GV_{DD}(typ) voltage is 1.8 V or 1.5 V when interfacing to DDR2 or DDR3 SDRAM respectively.

2.9.2.1 DDR2 and DDR3 SDRAM Interface Input AC Timing Specifications

This table provides the input AC timing specifications for the DDR controller when interfacing to DDR2 SDRAM.

Table 22. DDR2 SDRAM Interface Input AC Timing Specifications

At recommended operating conditions with GVDD of 1.8 V, see Table 3

Parameter	Symbol	Min	Max	Unit	Note
AC input low voltage	V_{ILAC}	—	MVREF*n* – 0.20	V	—
AC input high voltage	V_{IHAC}	MVREF*n* + 0.20	—	V	—

This table provides the input AC timing specifications for the DDR controller when interfacing to DDR3 SDRAM.

Table 23. DDR3 SDRAM Interface Input AC Timing Specifications

At recommended operating conditions with GVDD of 1.5 V, see Table 3

Parameter		Symbol	Min	Max	Unit	Note
AC input low voltage	> 1200 MHz data rate	V_{ILAC}	—	MVREF*n* – 0.150	V	—
	≤ 1200 MHz data rate		—	MVREF*n* – 0.175		
AC input high voltage	> 1200 MHz data rate	V_{IHAC}	MVREF*n* + 0.150	—	V	—
	≤ 1200 MHz data rate		MVREF*n* + 0.175	—		

This table provides the input AC timing specifications for the DDR controller when interfacing to DDR2 and DDR3 SDRAM.

Table 24. DDR2 and DDR3 SDRAM Interface Input AC Timing Specifications

At recommended operating conditions with GVDD of 1.8 V for DDR2 or 1.5 V for DDR3, see Table 3.
Synchronous mode not supported for data rates above 800 MHz, data rate frequencies above 800 MHz must run in asynchronous mode.

Parameter	Symbol	Min	Max	Unit	Note
Controller Skew for MDQS—MDQ/MECC	t_{CISKEW}	—	—	ps	1, 2
1333 MHz data rate		–125	125		1, 2, 5
1200 MHz data rate		–142	142		1, 2, 5
1066 MHz data rate		–170	170		1, 2, 5
800 MHz data rate		–200	200		1, 5
667 MHz data rate		–240	240		1, 4, 5

Table 24. DDR2 and DDR3 SDRAM Interface Input AC Timing Specifications (continued)

At recommended operating conditions with GVDD of 1.8 V for DDR2 or 1.5 V for DDR3, see Table 3.
Synchronous mode not supported for data rates above 800 MHz, data rate frequencies above 800 MHz must run in asynchronous mode.

Parameter	Symbol	Min	Max	Unit	Note
Tolerated Skew for MDQS—MDQ/MECC	t_{DISKEW}	—	—	ps	3
1333 MHz data rate		–250	250		3, 2
1200 MHz data rate		–275	275		3, 2
1066 MHz data rate		–300	300		3, 2
800 MHz data rate		–425	425		3
667 MHz data rate		–510	510		3, 4

Note:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that are captured with MDQS[n]. This must be subtracted from the total timing budget.
2. DDR3 only.
3. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}.This can be determined by the following equation: $t_{DISKEW} = \pm(T \div 4 - abs(t_{CISKEW}))$ where T is the clock period and $abs(t_{CISKEW})$ is the absolute value of t_{CISKEW}.
4. DDR2 only.
5. t_{CISKEW} test coverage is derived from tested t_{DISKEW} parameter.

This figure shows the DDR2 and DDR3 SDRAM interface input timing diagram.

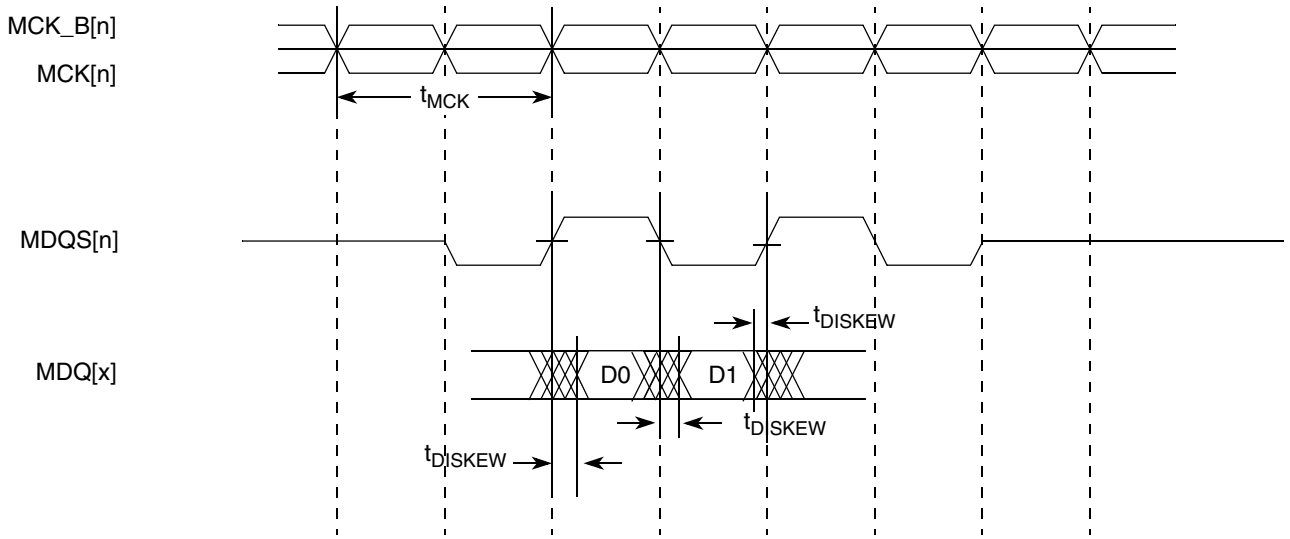


Figure 9. DDR2 and DDR3 SDRAM Interface Input Timing Diagram

2.9.2.2 DDR2 and DDR3 SDRAM Interface Output AC Timing Specifications

This table contains the output AC timing targets for the DDR2 and DDR3 SDRAM interface.

Table 25. DDR2 and DDR3 SDRAM Interface Output AC Timing Specifications

At recommended operating conditions with GVDD of 1.8 V for DDR2 or 1.5 V for DDR3, see Table 3.
Synchronous mode not supported above 800 MHz; frequencies above 800 MHz must run in asynchronous mode.

Parameter	Symbol[1]	Min	Max	Unit	Note
MCK[n] cycle time	t_{MCK}	1.5	5	ns	2
ADDR/CMD output setup with respect to MCK	t_{DDKHAS}			ns	3
1333 MHz data rate		0.606	—		6
1200 MHz data rate		0.675	—		6
1066 MHz data rate		0.744	—		6
800 MHz data rate		0.917	—		—
667 MHz data rate		1.10	—		7
ADDR/CMD output hold with respect to MCK	t_{DDKHAX}			ns	3
1333 MHz data rate		0.606	—		6
1200 MHz data rate		0.675	—		6
1066 MHz data rate		0.744	—		6
800 MHz data rate		0.917	—		—
667 MHz data rate		1.10	—		7
MCS_B[n] output setup with respect to MCK	t_{DDKHCS}			ns	3
1333 MHz data rate		0.606	—		6
1200 MHz data rate		0.675	—		6
1066 MHz data rate		0.744	—		6
800 MHz data rate		0.917	—		—
667 MHz data rate		1.10	—		7
MCS_B[n] output hold with respect to MCK	t_{DDKHCX}			ns	3
1333 MHz data rate		0.606	—		6
1200 MHz data rate		0.675	—		6
1066 MHz data rate		0.744	—		6
800 MHz data rate		0.917	—		—
667 MHz data rate		1.10	—		7
MCK to MDQS Skew	t_{DDKHMH}			ns	4
≥ 1066 MHz data rate		-0.245	0.245		6, 8
800 MHz data rate		–0.375	0.375		—
667 MHz data rate		–0.6	0.6		7

Table 25. DDR2 and DDR3 SDRAM Interface Output AC Timing Specifications (continued)

At recommended operating conditions with GVDD of 1.8 V for DDR2 or 1.5 V for DDR3, see Table 3.
Synchronous mode not supported above 800 MHz; frequencies above 800 MHz must run in asynchronous mode.

Parameter	Symbol[1]	Min	Max	Unit	Note
MDQ/MECC/MDM output setup with respect to MDQS	t_{DDKHDS}, t_{DDKLDS}			ps	5
1333 MHz data rate		250	—		5, 6
1200 MHz data rate		275	—		5, 6
1066 MHz data rate		300	—		5, 6
800 MHz data rate		375	—		5
667 MHz data rate		450	—		5
MDQ/MECC/MDM output hold with respect to MDQS	t_{DDKHDX}, t_{DDKLDX}			ps	5
1333 MHz data rate		250	—		5, 6
1200 MHz data rate		275	—		5, 6
1066 MHz data rate		300	—		5, 6
800 MHz data rate		375	—		5
667 MHz data rate		450	—		5
MDQS preamble	t_{DDKHMP}	$0.9 \times t_{MCK}$	—	ns	—
MDQS postamble	t_{DDKHME}	$0.4 \times t_{MCK}$	$0.6 \times t_{MCK}$	ns	—

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/MCK_B and MDQS/MDQS_B referenced measurements are made from the crossing of the two signals.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/MCK_B, MCS_B, and MDQ/MECC/MDM/MDQS.
4. t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the MDQS override bits (called WR_DATA_DELAY) in the TIMING_CFG_2 register. This is typically set to the same delay as in DDR_SDRAM_CLK_CNTL[CLK_ADJUST]. The timing parameters listed in the table assume that these two parameters have been set to the same adjustment value. See the *P4080 QorIQ Integrated Multicore Communication Processor Family Reference Manual* for a description and explanation of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe must be centered inside of the data eye at the pins of the microprocessor.
6. DDR3 only
7. DDR2 only
8. For 1200/1333 frequencies it is required to program the start value of the DQS adjust for write leveling.

NOTE

For the ADDR/CMD setup and hold specifications in Table 25, it is assumed that the clock control register is set to adjust the memory clocks by ½ applied cycle.

This figure shows the DDR2 and DDR3 SDRAM interface output timing for the MCK to MDQS skew measurement (tDDKHMH).

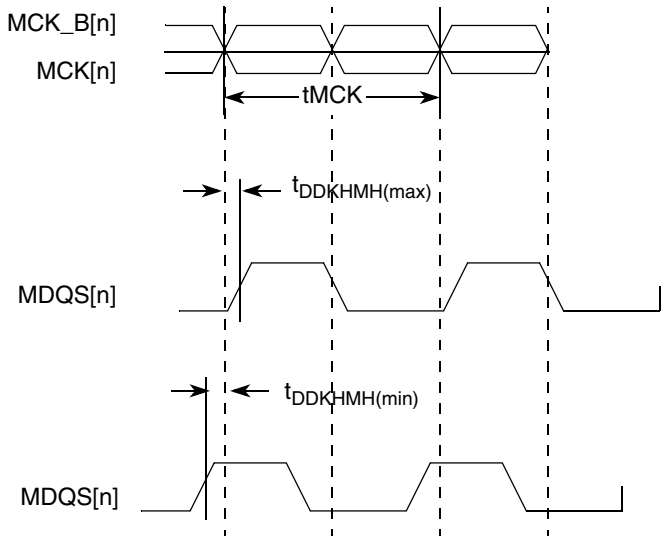


Figure 10. t_{DDKHMH} Timing Diagram

This figure shows the DDR2 and DDR3 SDRAM output timing diagram.

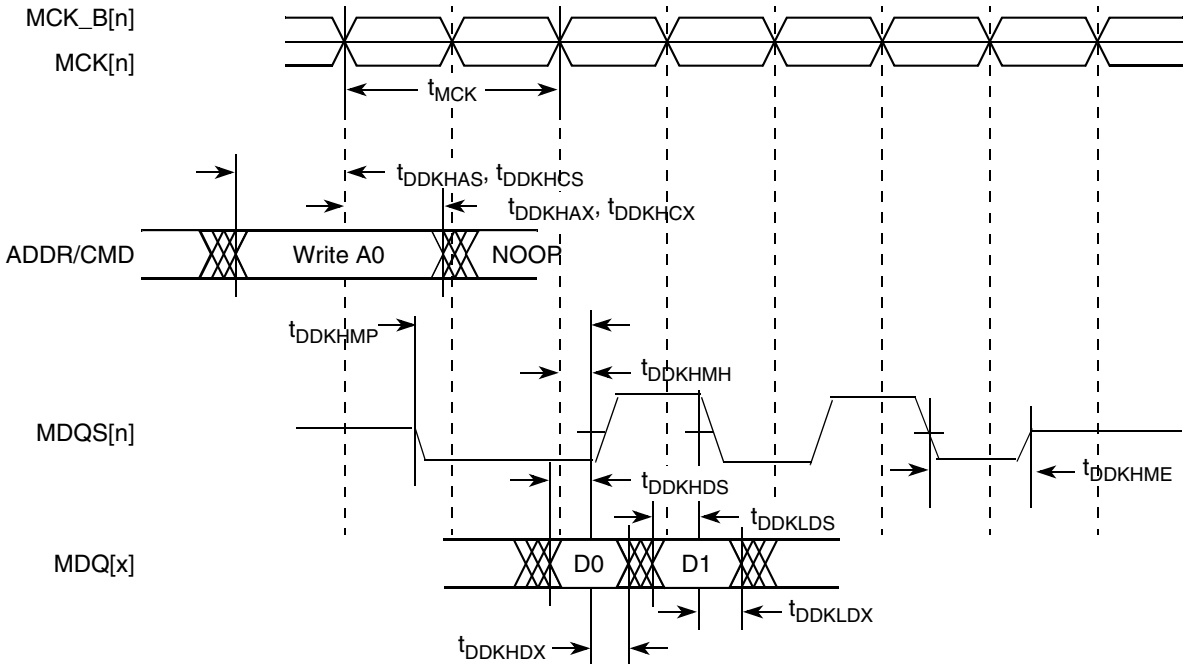


Figure 11. DDR2 and DDR3 Output Timing Diagram

This figure provides the AC test load for the DDR2 and DDR3 Controller bus.

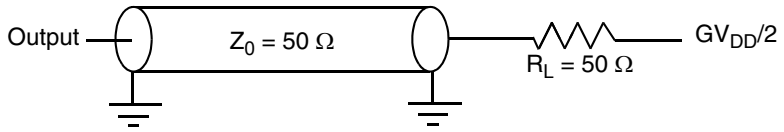


Figure 12. DDR2 and DDR3 Controller Bus AC Test Load

2.9.2.3 DDR2 and DDR3 SDRAM Differential Timing Specifications

This section describes the DC and AC differential timing specifications for the DDR2 and DDR3 SDRAM controller interface.

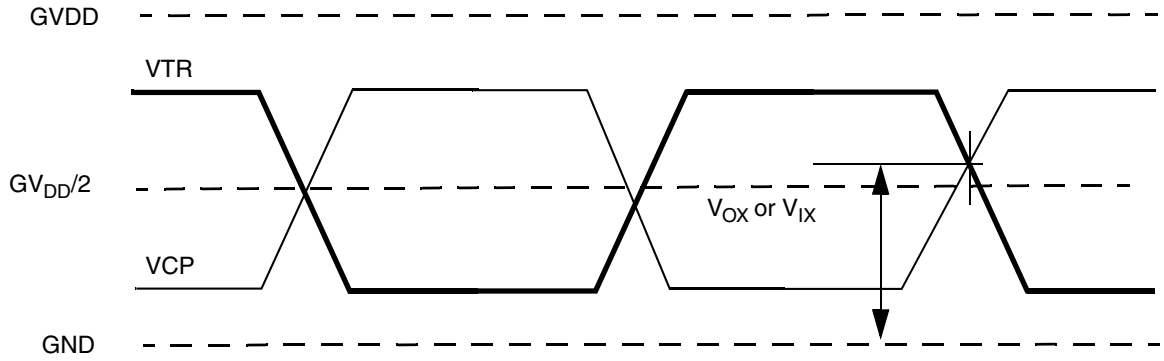


Figure 13. DDR2 and DDR3 SDRAM Differential Timing Specifications

NOTE

VTR specifies the true input signal (such as MCK or MDQS) and VCP is the complementary input signal (such as MCK_B or MDQS_B).

This table provides the DDR2 differential specifications for the differential signals MDQS/MDQS_B and MCK/MCK_B.

Table 26. DDR2 SDRAM Differential Electrical Characteristics

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input AC differential cross-point voltage	V_{IXAC}	0.5 × GVDD – 0.175	0.5 × GVDD + 0.175	V	—
Output AC differential cross-point voltage	V_{OXAC}	0.5 × GVDD – 0.125	0.5 × GVDD + 0.125	V	—

Note:
1. I/O drivers are calibrated before making measurements.

This table provides the DDR3 differential specifications for the differential signals MDQS/MDQS_B and MCK/MCK_B.

Table 27. DDR3 SDRAM Differential Electrical Characteristics

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input AC Differential Cross-point Voltage	V_{IXAC}	0.5 × GVDD – 0.150	0.5 × GVDD + 0.150	V	—
Output AC Differential Cross-point Voltage	V_{OXAC}	0.5 × GVDD – 0.115	0.5 × GVDD + 0.115	V	—

Note:
1. I/O drivers are calibrated before making measurements.

2.10 eSPI

This section describes the DC and AC electrical specifications for the eSPI interface.

2.10.1 eSPI DC Electrical Characteristics

This table provides the DC electrical characteristics for the eSPI interface operating at CV_{DD} = 3.3 V.

Table 28. eSPI DC Electrical Characteristics (3.3 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit
Input high voltage	V_{IH}	2	—	V
Input low voltage	V_{IL}	—	0.8	V
Input current (V_{IN} = 0 V or V_{IN} = CV_{DD})	I_{IN}	—	±40	μA
Output high voltage (CV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V
Output low voltage (CV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max CV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the CV_{IN} symbol referenced in Section 2.1.2, "Recommended Operating Conditions."

This table provides the DC electrical characteristics for the eSPI interface operating at CV_{DD} = 2.5 V.

Table 29. eSPI DC Electrical Characteristics (2.5 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit
Input high voltage	V_{IH}	1.7	—	V
Input low voltage	V_{IL}	—	0.7	V
Input current (V_{IN} = 0 V or V_{IN} = CV_{DD})	I_{IN}	—	±40	μA
Output high voltage (CV_{DD} = min, I_{OH} = –1 mA)	V_{OH}	2.0	—	V
Output low voltage (CV_{DD} = min, I_{OL} = 1 mA)	V_{OL}	—	0.4	V

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max CV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the CV_{IN} symbol referenced in Section 2.1.2, "Recommended Operating Conditions."

This table provides the DC electrical characteristics for the eSPI interface operating at CV_{DD} = 1.8 V.

Table 30. eSPI DC Electrical Characteristics (1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit
Input high voltage	V_{IH}	1.25	—	V
Input low voltage	V_{IL}	—	0.6	V
Input current (V_{IN} = 0 V or V_{IN} = CV_{DD})	I_{IN}	—	±40	μA
Output high voltage (CV_{DD} = min, I_{OH} = –0.5 mA)	V_{OH}	1.35	—	V
Output low voltage (CV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	—	0.4	V

Note:

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max CV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the CV_{IN} symbol referenced in Section 2.1.2, "Recommended Operating Conditions."

2.10.2 eSPI AC Timing Specifications

This table and provide the eSPI input and output AC timing specifications.

Table 31. eSPI AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Max	Unit	Note
SPI_MOSI output—Master data (internal clock) hold time	t_{NIKHOX}	2.2 + ($t_{PLATFORM_CLK}$ * SPMODE[HO_ADJ])	—	ns	2, 3
SPI_MOSI output—Master data (internal clock) delay	t_{NIKHOV}	—	2.5 + ($t_{PLATFORM_CLK}$ * SPMODE[HO_ADJ]	ns	2, 3
SPI_CS outputs—Master data (internal clock) hold time	$t_{NIKHOX2}$	0	—	ns	2
SPI_CS outputs—Master data (internal clock) delay	$t_{NIKHOV2}$	—	6.0	ns	2
SPI inputs—Master data (internal clock) input setup time	t_{NIIVKH}	5	—	ns	—
SPI inputs—Master data (internal clock) input hold time	t_{NIIXKH}	0	—	ns	—

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{NIKHOV} symbolizes the NMSI outputs internal timing (NI) for the time t_{SPI} memory clock reference (K) goes from the high state (H) until outputs (O) are valid (V).
2. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
3. See the *P4080 QorIQ Integrated Multicore Communication Processor Family Reference Manual* for details about the register SPMODE.

This figure provides the AC test load for the eSPI.

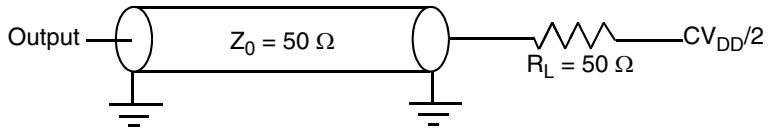


Figure 14. eSPI AC Test Load

This figure represent the AC timing from Table 31 in master mode (internal clock). Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge. Also, note that the clock edge is selectable on eSPI.

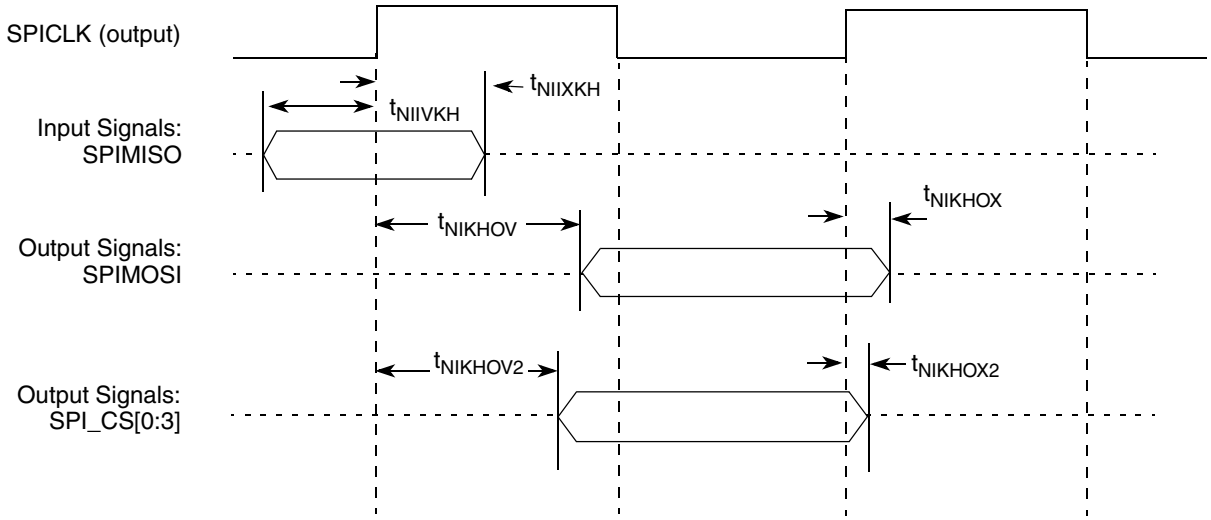


Figure 15. eSPI AC Timing in Master Mode (Internal Clock) Diagram

2.11 DUART

This section describes the DC and AC electrical specifications for the DUART interface.

2.11.1 DUART DC Electrical Characteristics

This table provides the DC electrical characteristics for the DUART interface.

Table 32. DUART DC Electrical Characteristics

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1

Table 32. DUART DC Electrical Characteristics (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	±40	μA	—
Output high voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Notes:

1. The symbol OV_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 3.

2.11.2 DUART AC Electrical Specifications

This table provides the AC timing parameters for the DUART interface.

Table 33. DUART AC Timing Specifications

Parameter	Value	Unit	Note
Minimum baud rate	$f_{PLAT}/(2 \times 1{,}048{,}576)$	baud	1, 3
Maximum baud rate	$f_{PLAT}/(2 \times 16)$	baud	1, 2

Notes:

1. f_{PLAT} refers to the internal platform clock.
2. The actual attainable baud rate is limited by the latency of interrupt processing.
3. This parameter is sampled.

2.12 Ethernet: Data Path Three-Speed Ethernet (dTSEC), Management Interface 1 and 2, IEEE Std 1588™

This section provides the AC and DC electrical characteristics for the data path three-speed Ethernet controller, and the Ethernet Management Interfaces.

2.12.1 SGMII Timing Specifications

See Section 2.20.8, “SGMII Interface.”

2.12.2 RGMII Timing Specifications

This section discusses the electrical characteristics for the RGMII interface.

2.12.2.1 RGMII DC Timing Specifications

This table provides the DC electrical characteristics for the RGMII interface.

Table 34. RGMII DC Electrical Characteristics (LV_{DD} = 2.5V)

For recommended operating conditions, see Table 3.

Parameters	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.70	—	V	1
Input low voltage	V_{IL}	—	0.70	V	1
Input current (LV_{IN} = 0 V or LV_{IN} = LV_{DD})	I_{IH}	—	±40	μA	2
Output high voltage (LV_{DD} = min, I_{OH} = –1.0 mA)	V_{OH}	2.00	—	V	—
Output low voltage (LV_{DD} = min, I_{OL} = 1.0 mA)	V_{OL}	—	0.40	V	—

Note:
1. The min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3.
2. The symbol LV_{IN}, in this case, represents the LV_{IN} symbol referenced in Section 2.1.2, "Recommended Operating Conditions."

2.12.2.2 RGMII AC Timing Specifications

This table presents the RGMII AC timing specifications.

Table 35. RGMII AC Timing Specifications (LV_{DD} = 2.5 V)

For recommended operating conditions, see Table 3.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Note
Data to clock output skew (at transmitter)	t_{SKRGT_TX}	–500	0	500	ps	7
Data to clock input skew (at receiver)	t_{SKRGT_RX}	1.0	—	2.6	ns	2
Clock period duration	t_{RGT}	7.2	8.0	8.8	ns	3
Duty cycle for 10BASE-T and 100BASE-TX	t_{RGTH}/t_{RGT}	40	50	60	%	3, 4
Duty cycle for Gigabit	t_{RGTH}/t_{RGT}	45	50	55	%	—
Rise time (20%–80%)	t_{RGTR}	—	—	0.75	ns	5, 6
Fall time (20%–80%)	t_{RGTF}	—	—	0.75	ns	5, 6

Notes:
1. In general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII timing. Note that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. This implies that PC board design requires clocks to be routed such that an additional trace delay of greater than 1.5 ns is added to the associated clock signal. Many PHY vendors already incorporate the necessary delay inside their chip. If so, additional PCB delay is probably not needed.
3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
5. Applies to inputs and outputs.
6. System/board must be designed to ensure this input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.
7. The frequency of RX_CLK (input) should not exceed the frequency of GTX_CLK (output) by more than 300 ppm.

This figure shows the RGMII AC timing and multiplexing diagrams.

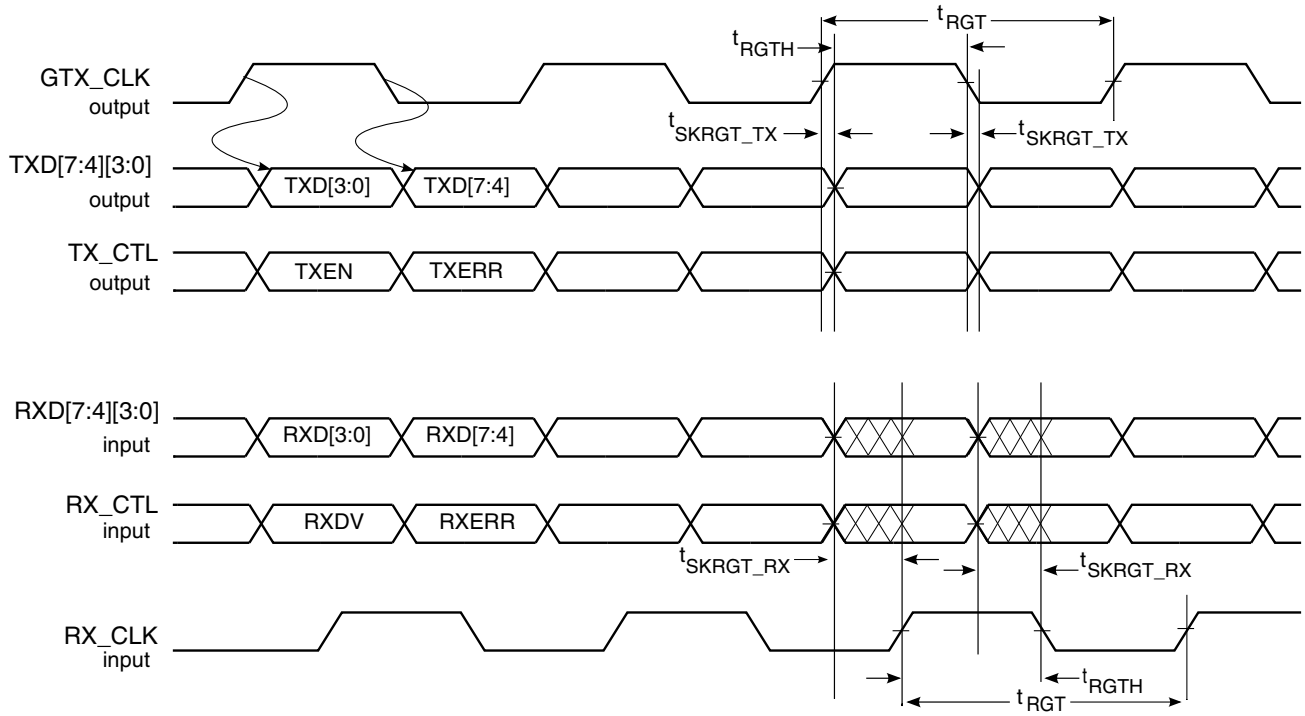


Figure 16. RGMII AC Timing and Multiplexing Diagrams

2.12.3 Ethernet Management Interface

This section discusses the electrical characteristics for the EMI1 and EMI2 interfaces. EMI1 is the PHY management interface controlled by the MDIO controller associated with Frame Manager 1 dTSEC1. EMI2 is the XAUI PHY management interface controlled by the MDIO controller associated with Frame Manager 1 10GEC.

2.12.3.1 Ethernet Management Interface 1 DC Electrical Characteristics

The DC electrical characteristics for EMI1_MDIO and EMI1_MDC are provided in this section.

Table 36. Ethernet Management Interface 1 DC Electrical Characteristics (LV_{DD} = 3.3 V)

Parameter	Symbol	Min	Max	Unit	Note
High-level input voltage	V_{IH}	2	—	V	1
Low-level input voltage	V_{IL}	—	0.8	V	1
Input high current (LV_{DD} = Max, LV_{IN} = 2.4 V)	I_{IH}	—	40	μA	2
Input low current (LV_{DD} = Max, LV_{IN} = 0.4 V)	I_{IL}	–600	—	μA	—
Output high voltage (LV_{DD} = min, I_{OH} = –4 mA)	V_{OH}	2.4	—	V	—

Table 36. Ethernet Management Interface 1 DC Electrical Characteristics (LV_{DD} = 3.3 V) (continued)

Parameter	Symbol	Min	Max	Unit	Note
Output low voltage (LV_{DD} = min, I_{OL} = 4 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min V_{IL} and max V_{IH} values are based on the min and max LV_{IN} respective values found in Table 3.
2. The symbol LV_{IN}, in this case, represents the LV_{IN} symbol referenced in Section 2.1.2, "Recommended Operating Conditions."

Table 37. Ethernet Management Interface 1 DC Electrical Characteristics (LV_{DD} = 2.5 V)

For recommended operating conditions, see Table 3.

Parameters	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.70	—	V	1
Input low voltage	V_{IL}	—	0.70	V	1
Input high current (V_{IN} = LV_{DD})	I_{IH}	—	40	μA	2
Input low current (V_{IN} = GND)	I_{IL}	–40	—	μA	
Output high voltage (LV_{DD} = min, I_{OH} = –1.0 mA)	V_{OH}	2.00	—	V	—
Output low voltage (LV_{DD} = min, I_{OL} = 1.0 mA)	V_{OL}	—	0.40	V	—

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Section 2.1.2, "Recommended Operating Conditions."

2.12.3.2 Ethernet Management Interface 2 DC Electrical Characteristics

Ethernet Management Interface 2 pins function as open drain I/Os. The interface conforms to 1.2 V nominal voltage levels. LV_{DD} must be powered to use this interface. The DC electrical characteristics for EMI2_MDIO and EMI2_MDC are provided in this section.

Table 38. Ethernet Management Interface 2 DC Electrical Characteristics (1.2 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	0.84	—	V	—
Input low voltage	V_{IL}	—	0.36	V	—
Output high voltage (I_{OH}= –100 μA)	V_{OH}	1.0	—	V	—
Output low voltage (I_{OL} = 100 μA)	V_{OL}	—	0.2	V	—
Output low current (V_{OL} = 0.2 V)	I_{OL}	4	—	mA	—
Input capacitance	C_{IN}	—	10	pF	—

2.12.3.3 Ethernet Management Interface 1 AC Electrical Specifications

Table 39. Ethernet Management Interface 1 AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Note
MDC frequency	f_{MDC}	—	—	2.5	MHz	2
MDC clock pulse width high	t_{MDCH}	160	—	—	ns	—
MDC to MDIO delay	t_{MDKHDX}	$(16 \times t_{plb_clk}) - 6$	—	$(16 \times t_{plb_clk}) + 6$	ns	3, 4
MDIO to MDC setup time	t_{MDDVKH}	8	—	—	ns	—
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	—

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time.
2. This parameter is dependent on the frame manager clock frequency (MIIMCFG [MgmtClk] field determines the clock frequency of the MgmtClk Clock EC_MDC).
3. This parameter is dependent on the frame manager clock frequency. The delay is equal to 16 frame manager clock periods ± 6 ns. For example, with a frame manager clock of 400 MHz, the min/max delay is 40 ns ± 6 ns.
4. t_{plb_clk} is the frame manager clock period.

2.12.3.4 Ethernet Management Interface 2 AC Electrical Characteristics

Table 40. Ethernet Management Interface 2 AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Note
MDC frequency	f_{MDC}	—	—	2.5	MHz	2
MDC clock pulse width high	t_{MDCH}	160	—	—	ns	—
MDC to MDIO delay	t_{MDKHDX}	$(0.5 \times (1/f_{MDC})) - 6$	—	$(0.5 \times (1/f_{MDC})) + 6$	ns	3
MDIO to MDC setup time	t_{MDDVKH}	8	—	—	ns	—
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	—

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time.
2. This parameter is dependent on the frame manager clock frequency (MIIMCFG [MgmtClk] field determines the clock frequency of the MgmtClk Clock EC_MDC).
3. This parameter is dependent on the management data clock frequency, f_{MDC}. The delay is equal to 0.5 management data clock period ±6 ns. For example, with a management data clock of 2.5 MHz, the min/max delay is 200 ns ± 6 ns.

This figure shows the Ethernet Management Interface timing diagram.

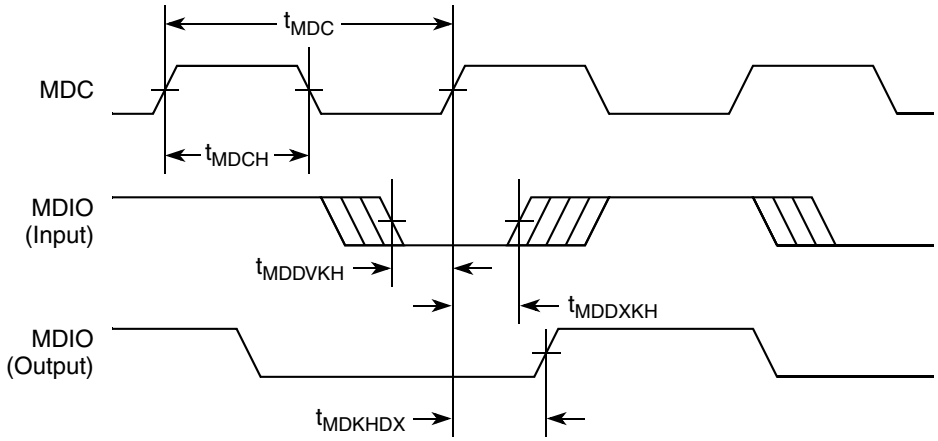


Figure 17. Ethernet Management Interface Timing Diagram

2.12.4 dTSEC IEEE 1588 Timing Specifications

2.12.4.1 dTSEC IEEE 1588 DC Timing Specifications

This table shows dTSEC IEEE 1588 DC electrical characteristics when operating at LV_{DD} = 3.3 V supply.

Table 41. dTSEC IEEE 1588 DC Electrical Characteristics (LV_{DD} = 3.3 V)

For recommended operating conditions with LV_{DD} = 3.3 V

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2.0	—	V	2
Input low voltage	V_{IL}	—	0.9	V	2
Input high current (LV_{DD} = Max, V_{IN} = 2.1 V)	I_{IH}	—	40	μA	1
Input low current (LV_{DD} = Max, V_{IN} = 0.5 V)	I_{IL}	–600	—	μA	1
Output high voltage (LV_{DD} = Min, I_{OH} = –1.0 mA)	V_{OH}	2.4	—	V	—
Output low voltage (LV_{DD} = Min, I_{OL} = 1.0 mA)	V_{OL}	—	0.4	V	—

Note:

1. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 2and Table 3.
2. The min V_{IL} and max V_{IH} values are based on the respective LV_{IN} values found in Table 3.

This table shows the dTSEC IEEE 1588 DC electrical characteristics when operating at LV_{DD} = 2.5 V supply.

Table 42. dTSEC IEEE 1588 DC Electrical Characteristics (LV_{DD} = 2.5 V)

For recommended operating conditions with LV_{DD} = 2.5 V

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.70	—	V	—
Input low voltage	V_{IL}	—	0.70	V	—

Table 42. dTSEC IEEE 1588 DC Electrical Characteristics (LV_{DD} = 2.5 V) (continued)

For recommended operating conditions with LV_{DD} = 2.5 V

Parameter	Symbol	Min	Max	Unit	Notes
Input current (LV_{IN} = 0 V or LV_{IN} = LV_{DD})	I_{IH}	—	±40	μA	2
Output high voltage (LV_{DD} = min, I_{OH} = –1.0 mA)	V_{OH}	2.00	—	V	—
Output low voltage (LV_{DD} = min, I_{OL} = 1.0 mA)	V_{OL}	—	0.40	V	—

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the LV_{IN} symbols referenced in Table 2and Table 3.

2.12.4.2 dTSEC IEEE 1588 AC Timing Specifications

This section discusses the electrical characteristics for the dTSEC IEEE 1588 interface.

Table 43. dTSEC IEEE 1588 AC Timing Specifications

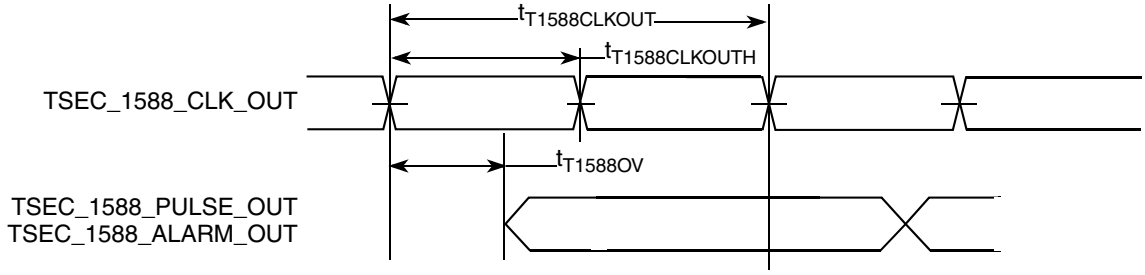
For recommended operating conditions, see Table 3.

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Note
TSEC_1588_CLK clock period	$t_{T1588CLK}$	3.3	—	$T_{RX_CLK} \times 7$	ns	1, 3
TSEC_1588_CLK duty cycle	$t_{T1588CLKH}$/ $t_{T1588CLK}$	40	50	60	%	2
TSEC_1588_CLK peak-to-peak jitter	$t_{T1588CLKINJ}$	—	—	250	ps	—
Rise time TSEC_1588_CLK (20%–80%)	$t_{T1588CLKINR}$	1.0	—	2.0	ns	—
Fall time TSEC_1588_CLK (80%–20%)	$t_{T1588CLKINF}$	1.0	—	2.0	ns	—
TSEC_1588_CLK_OUT clock period	$t_{T1588CLKOUT}$	$2 \times t_{T1588CLK}$	—	—	ns	4
TSEC_1588_CLK_OUT duty cycle	$t_{T1588CLKOTH}$/ $t_{T1588CLKOUT}$	30	50	70	%	—
TSEC_1588_PULSE_OUT, TSEC_1588_ALARM_OUT	$t_{T1588OV}$	0.5	—	3.0	ns	—
TSEC_1588_TRIG_IN pulse width	$t_{T1588TRIGH}$	$2 \times t_{T1588CLK_MAX}$	—	—	ns	3

Notes:

1. T_{RX_CLK} is the maximum clock period of dTSEC receiving clock selected by TMR_CTRL[CKSEL]. See the *P4080 QorIQ Integrated Multicore Communication Processor Family Reference Manual* for a description of TMR_CTRL registers.
2. It needs to be at least two times the clock period of the clock selected by TMR_CTRL[CKSEL]. See the *P4080 QorIQ Integrated Multicore Communication Processor Family Reference Manual* for a description of TMR_CTRL registers.
3. The maximum value of $t_{T1588CLK}$ is not only defined by the value of T_{RX_CLK}, but also defined by the recovered clock. For example, for 10/100/1000 Mbps modes, the maximum value of $t_{T1588CLK}$ are be 2800, 280, and 56 ns respectively.
4. For 1588, there are three input clock sources: TSEC_1588_CLK_IN, RTC and FMan/4. When using TSEC_1588_CLK_IN,the minimum clock period is $2 \times t_{T1588CLK}$.

This figure shows the data and command output AC timing diagram.



Note: The output delay is counted starting at the rising edge if $t_{T1588CLKOUT}$ is noninverting. Otherwise, it is counted starting at the falling edge.

Figure 18. dTSEC IEEE 1588 Output AC Timing

This figure shows the data and command input AC timing diagram.

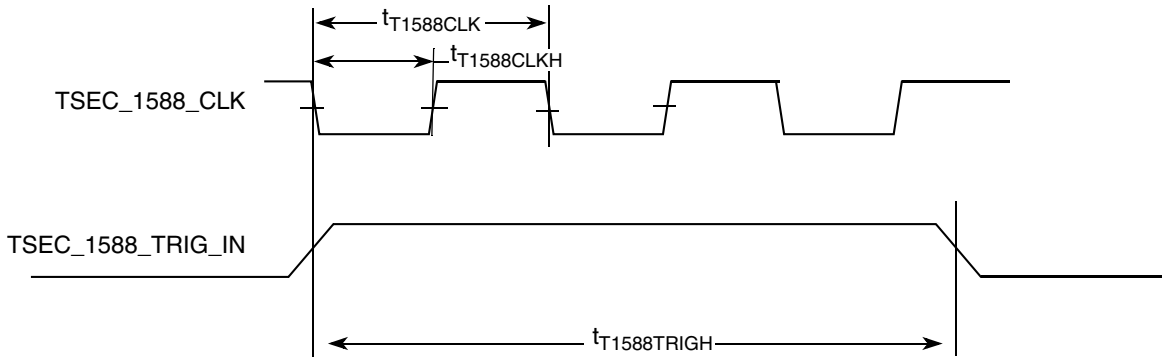


Figure 19. dTSEC IEEE 1588 Input AC Timing

2.13 USB

This section provides the AC and DC electrical specifications for the USB interface.

2.13.1 USB DC Electrical Characteristics

This section provides the DC electrical characteristics for the USB interface.

Table 44. USB DC Electrical Characteristics (LV_{DD} = 3.3 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage[1]	V_{IH}	2.0	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (LV_{IN} = 0 V or LV_{IN} = LV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (LV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.8	—	V	—

Table 44. USB DC Electrical Characteristics (LV_{DD} = 3.3 V) (continued)

For recommended operating conditions, see Table 3.

Output low voltage (LV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.3	V	—

Notes:
1. The min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3.
2. The symbol LV_{IN}, in this case, represents the LV_{IN} symbol referenced in Section 2.1.2, "Recommended Operating Conditions."

Table 45. USB DC Electrical Characteristics (LV_{DD} = 2.5 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage[1]	V_{IH}	1.7	—	V	1
Input low voltage	V_{IL}	—	0.7	V	1
Input current (LV_{IN} = 0 V or LV_{IN} = LV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (LV_{DD} = min, I_{OH} = –1 mA)	V_{OH}	2.0	—	V	—
Output low voltage (LV_{DD} = min, I_{OL} = 1 mA)	V_{OL}	—	0.4	V	—

Notes:
1. The min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3.
2. The symbol LV_{IN}, in this case, represents the LV_{IN} symbol referenced in Section 2.1.2, "Recommended Operating Conditions."

Table 46. USB DC Electrical Characteristics (LV_{DD} = 1.8 V)

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage[1]	V_{IH}	1.25	—	V	1
Input low voltage	V_{IL}	—	0.6	V	1
Input current (LV_{IN} = 0 V or LV_{IN} = LV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (LV_{DD} = min, I_{OH} = –0.5 mA)	V_{OH}	1.35	—	V	—
Output low voltage (LV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	—	0.4	V	—

Notes:
1. The min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3.
2. The symbol LV_{IN}, in this case, represents the LV_{IN} symbol referenced in Section 2.1.2, "Recommended Operating Conditions."

2.13.2 USB AC Electrical Specifications

This table describes the general timing parameters of the USB interface of the chip.

Table 47. USB General Timing Parameters (ULPI Mode Only)

Parameter	Symbol[1]	Min	Max	Unit	Note
USB clock cycle time	t_{USCK}	15	—	ns	2, 3, 4, 5
Input setup to USB clock—all inputs	t_{USIVKH}	4	—	ns	2, 3, 4, 5
Input hold to USB clock—all inputs	t_{USIXKH}	0	—	ns	2, 3, 4, 5
USB clock to output valid—all outputs	t_{USKHOV}	—	8	ns	2, 3, 4, 5
Output hold from USB clock—all outputs	t_{USKHOX}	2	—	ns	2, 3, 4, 5

Notes:

1. The symbols for timing specifications follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{USIXKH} symbolizes usb timing (US) for the input (I) to go invalid (X) with respect to the time the usb clock reference (K) goes high (H). Also, t_{USKHOX} symbolizes USB timing (US) for the USB clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to USB clock.
3. All signals are measured from $LV_{DD}/2$ of the rising edge of the USB clock to $0.4 \times LV_{DD}$ of the signal in question for 3.3 V signaling levels.
4. Input timings are measured at the pin.
5. For active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to that of the leakage current specification.

This figures provide the AC test load and signals for the USB, respectively.

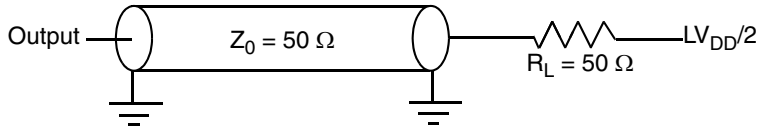


Figure 20. USB AC Test Load

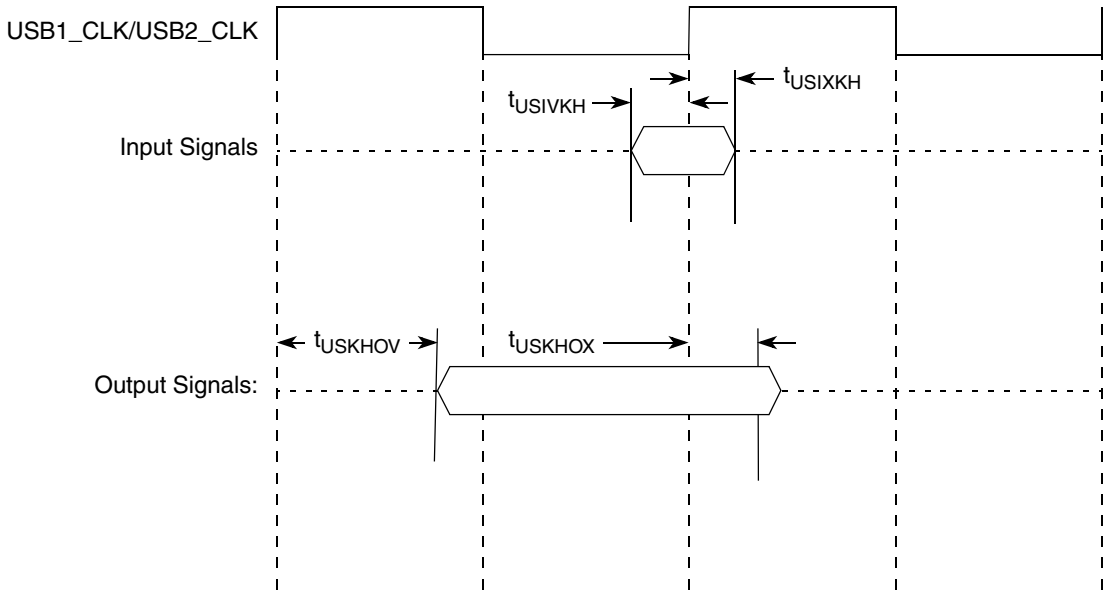


Figure 21. USB Signals

This table provides the USB clock input (USB*n*_CLK) AC timing specifications.

Table 48. USB*n*_CLK AC Timing Specifications

Parameter/Condition	Conditions	Symbol	Min	Typ	Max	Unit
Frequency range	—	$f_{USB_CLK_IN}$	59.97	60	60.03	MHz
Clock frequency tolerance	—	t_{CLK_TOL}	–0.05	0	0.05	%
Reference clock duty cycle	Measured at 1.6 V	t_{CLK_DUTY}	40	50	60	%
Total input jitter/time interval error	Peak-to-peak value measured with a second order high-pass filter of 500 kHz bandwidth	t_{CLK_PJ}	—	—	200	ps

2.14 Enhanced Local Bus Interface

This section describes the DC and AC electrical specifications for the enhanced local bus interface.

2.14.1 Enhanced Local Bus DC Electrical Characteristics

This table provides the DC electrical characteristics for the enhanced local bus interface operating at BV_{DD} = 3.3 V.

Table 49. Enhanced Local Bus DC Electrical Characteristics (3.3 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (V_{IN} = 0 V or V_{IN} = BV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (BV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (BV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max BV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the BV_{IN} symbol referenced in Section 2.1.2, "Recommended Operating Conditions."

This table provides the DC electrical characteristics for the enhanced local bus interface operating at BV_{DD} = 2.5 V.

Table 50. Enhanced Local Bus DC Electrical Characteristics (2.5 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.7	—	V	1
Input low voltage	V_{IL}	—	0.7	V	1
Input current (V_{IN} = 0 V or V_{IN} = BV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (BV_{DD} = min, I_{OH} = –1 mA)	V_{OH}	2.0	—	V	—
Output low voltage (BV_{DD} = min, I_{OL} = 1 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max BV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the BV_{IN} symbol referenced in Section 2.1.2, "Recommended Operating Conditions."

This table provides the DC electrical characteristics for the enhanced local bus interface operating at BV_{DD} = 1.8 V.

Table 51. Enhanced Local Bus DC Electrical Characteristics (1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.25	—	V	1
Input low voltage	V_{IL}	—	0.6	V	1
Input current (V_{IN} = 0 V or V_{IN} = BV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (BV_{DD} = min, I_{OH} = –0.5 mA)	V_{OH}	1.35	—	V	—
Output low voltage (BV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max BV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the BV_{IN} symbol referenced in Section 2.1.2, "Recommended Operating Conditions."

2.14.2 Enhanced Local Bus AC Timing Specifications

This section describes the AC timing specifications for the enhanced local bus interface.

2.14.2.1 Test Condition

This figure provides the AC test load for the enhanced local bus.

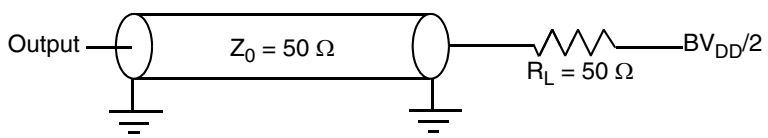


Figure 22. Enhanced Local Bus AC Test Load

2.14.2.2 Local Bus AC Timing Specification

All output signal timings are relative to the falling edge of any LCLKs. The external circuit must use the rising edge of the LCLKs to latch the data.

All input timings except LGTA/LUPWAIT/LFRB are relative to the rising edge of LCLKs. LGTA/LUPWAIT/LFRB are relative to the falling edge of LCLKs.

This table describes the timing specifications of the local bus interface.

Table 52. Enhanced Local Bus Timing Specifications (BV_{DD} = 3.3 V, 2.5 V, and 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol[1]	Min	Max	Unit	Note
Local bus cycle time	t_{LBK}	10	—	ns	—
Local bus duty cycle	t_{LBKH}/t_{LBK}	45	55	%	—
LCLK[n] skew to LCLK[m]	$t_{LBKSKEW}$	—	150	ps	2
Input setup (except LGTA/LUPWAIT/LFRB)	t_{LBIVKH}	6	—	ns	—
Input hold (except LGTA/LUPWAIT/LFRB)	t_{LBIXKH}	1	—	ns	—
Input setup (for LGTA/LUPWAIT/LFRB)	t_{LBIVKL}	6	—	ns	—
Input hold (for LGTA/LUPWAIT/LFRB)	t_{LBIXKL}	1	—	ns	—
Output delay (Except LALE)	t_{LBKLOV}	—	1.5	ns	—
Output hold (Except LALE)	t_{LBKLOX}	–3.5	—	ns	5
Local bus clock to output high impedance for LAD/LDP	t_{LBKLOZ}	—	2	ns	3
LALE output negation to LAD/LDP output transition (LATCH hold time)	t_{LBONOT}	0.8 (LBCR[AHD] = 1)	—	eLBC controller clock cycle (= 2 platform clock cycles)	4
		1.8 (LBCR[AHD] = 0)	—		

Note:

1. All signals are measured from $BV_{DD}/2$ of rising/falling edge of LCLK to $BV_{DD}/2$ of the signal in question.
2. Skew measured between different LCLKs at $BV_{DD}/2$.
3. For purposes of active/float timing measurements, the high impedance or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. t_{LBONOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBONOT} is determined by LBCR[AHD]. The unit is the eLBC controller clock cycle, which is the internal clock that runs the local bus controller, not the external LCLK. After power on reset, LBCR[AHD] defaults to 0.
5. Output hold is negative. This means that output transition happens earlier than the falling edge of LCLK.

This figure shows the AC timing diagram of the local bus interface.

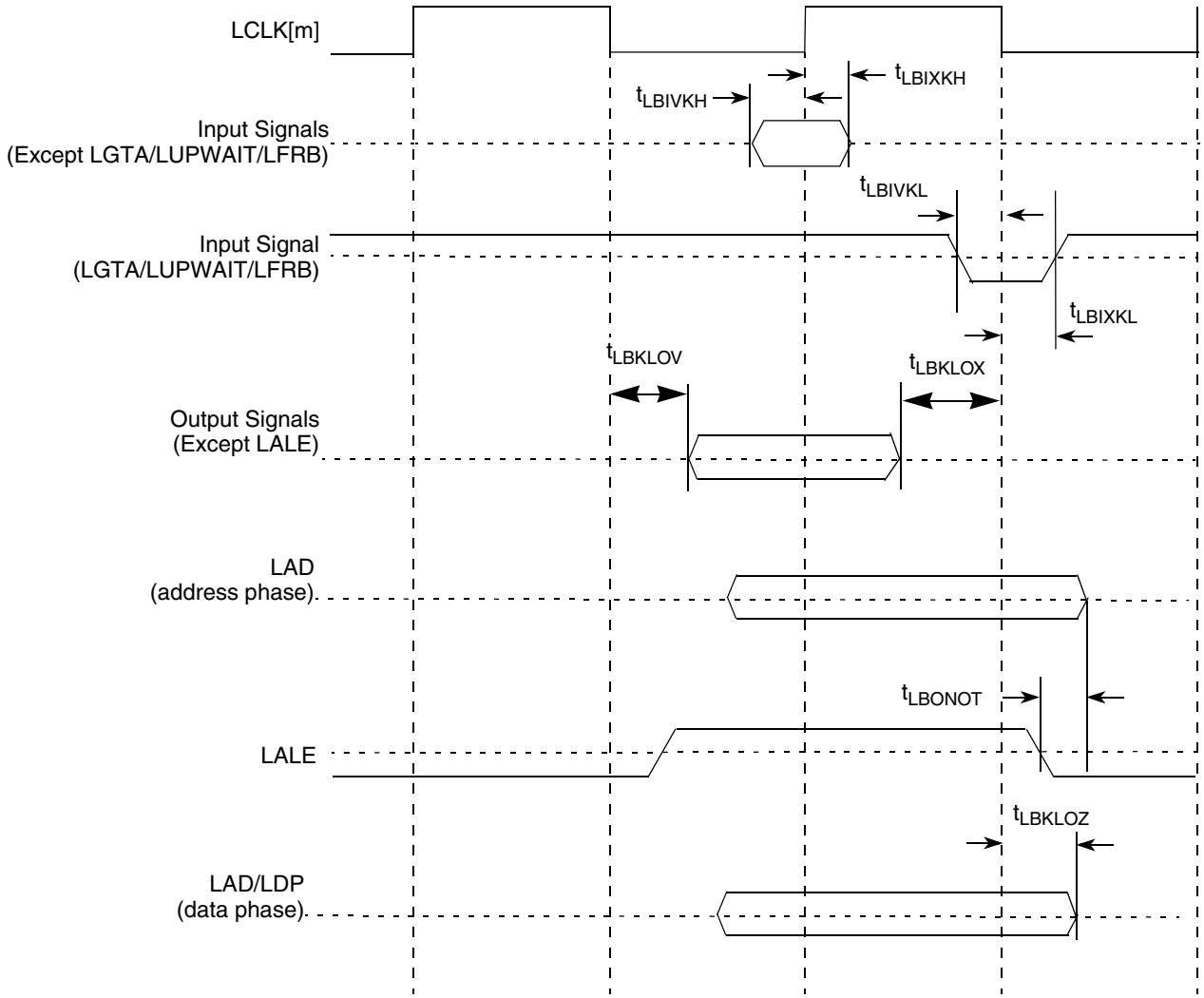
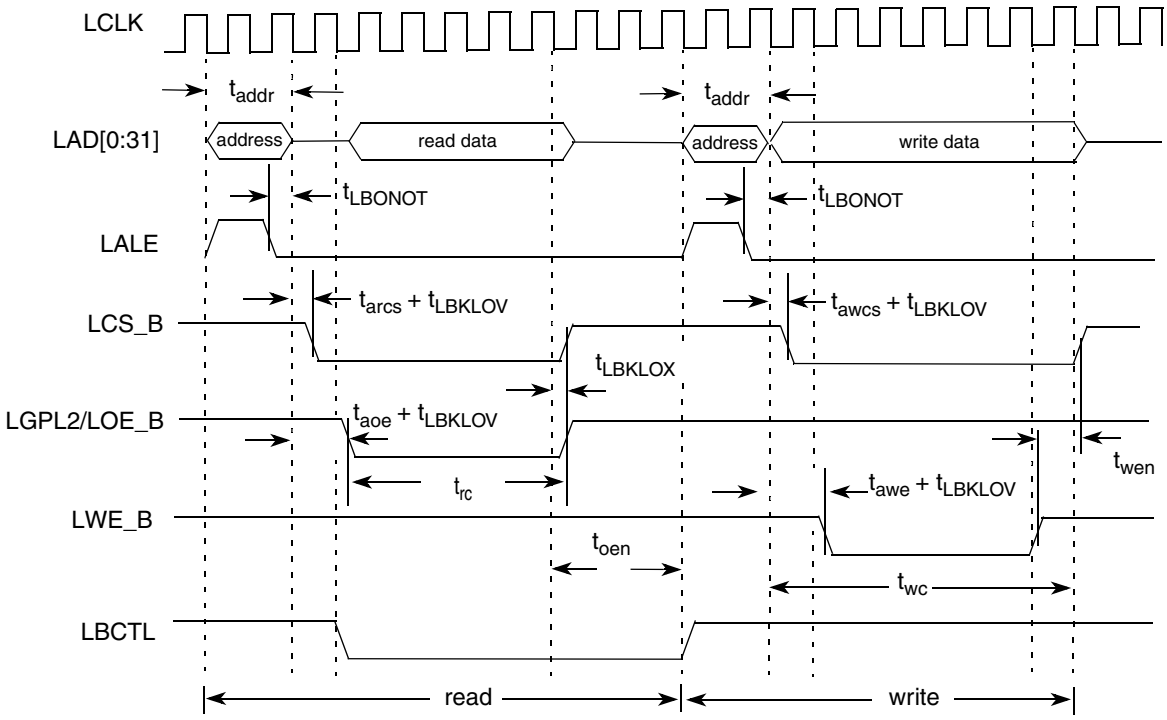


Figure 23. Enhanced Local Bus Signals

Figure 24 applies to all three controllers that eLBC supports: GPCM, UPM, and FCM. For input signals, the AC timing data is used directly for all three controllers.

For output signals, each type of controller provides its own unique method to control the signal timing. The final signal delay value for output signals is the programmed delay plus the AC timing delay. For example, for GPCM, LCS can be programmed to delay by t_{acs} (0, ¼, ½, 1, 1 + ¼, 1 + ½, 2, 3 cycles), so the final delay is $t_{acs} + t_{LBKHOV}$.

This figure shows how the AC timing diagram applies to GPCM. The same principle applies to UPM and FCM.



1 t_{addr} is programmable and determined by LCRR[EADC] and ORx[EAD].

2 t_{arcs}, t_{awcs}, t_{aoe}, t_{rc}, t_{oen}, t_{awe}, t_{wc}, t_{wen} are determined by ORx. See the *P4080 QorIQ Integrated Multicore Communication Processor Family Reference Manual*.

Figure 24. GPCM Output Timing Diagram

2.15 Enhanced Secure Digital Host Controller (eSDHC)

This section describes the DC and AC electrical specifications for the eSDHC interface.

2.15.1 eSDHC DC Electrical Characteristics

This table provides the DC electrical characteristics for the eSDHC interface. The eSDHC interface operates at OV_{DD} = 3.3 V, however, SDHC_DAT[4:7] require CV_{DD} = 3.3 V when muxed extended SDHC data signals are enabled via the RCW[SPI] field.

Table 53. eSDHC Interface DC Electrical Characteristics

For recommended operating conditions, see Table 3.

Characteristic	Symbol	Condition	Min	Max	Unit	Note
Input high voltage	V_{IH}	—	0.625 × OV_{DD}	—	V	1
Input low voltage	V_{IL}	—	—	0.25 × OV_{DD}	V	1
Input/output leakage current	I_{IN}/I_{OZ}	—	–50	50	μA	—
Output high voltage	V_{OH}	I_{OH} = –100 μA at OV_{DD} min	0.75 × OV_{DD}	—	V	—

Table 53. eSDHC Interface DC Electrical Characteristics (continued)

For recommended operating conditions, see Table 3.

Characteristic	Symbol	Condition	Min	Max	Unit	Note
Output low voltage	V_{OL}	I_{OL} = 100μA at OV_{DD} min	—	0.125 × OV_{DD}	V	—
Output high voltage	V_{OH}	I_{OH} = –100 μA at OV_{DD} min	OV_{DD} – 0.2	—	V	2
Output low voltage	V_{OL}	I_{OL} = 2 mA at OV_{DD} min	—	0.3	V	2

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. Open drain mode for MMC cards only.

2.15.2 eSDHC AC Timing Specifications

This table provides the eSDHC AC timing specifications as defined in Figure 25.

Table 54. eSDHC AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol[1]	Min	Max	Unit	Note
SD_CLK clock frequency: SD Full-speed/high-speed mode MMC Full-speed/high-speed mode	f_{SHSCK}	 0	 25/50 20/52	MHz	2, 4
SD_CLK clock low time—Full-speed/High-speed mode	t_{SHSCKL}	10/7	—	ns	4
SD_CLK clock high time—Full-speed/High-speed mode	t_{SHSCKH}	10/7	—	ns	4
SD_CLK clock rise and fall times	t_{SHSCKR}/ t_{SHSCKF}	—	3	ns	4
Input setup times: SD_CMD, SD_DATx, SD_CD to SD_CLK	$t_{SHSIVKH}$	2.5	—	ns	3, 4, 5
Input hold times: SD_CMD, SD_DATx, SD_CD to SD_CLK	$t_{SHSIXKH}$	2.5	—	ns	4, 5
Output delay time: SD_CLK to SD_CMD, SD_DATx valid	$t_{SHSKHOV}$	–3	3	ns	4, 5

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first three letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{FHSKHOV}$ symbolizes eSDHC high-speed mode device timing (SHS) clock reference (K) going to the high (H) state, with respect to the output (O) reaching the invalid state (X) or output hold time. Note that in general, the clock reference symbol is based on five letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. In full-speed mode, the clock frequency value can be 0–25 MHz for an SD card and 0–20 MHz for an MMC card. In high-speed mode, the clock frequency value can be 0–50 MHz for an SD card and 0–52 MHz for an MMC card.
3. To satisfy setup timing, one way board routing delay between Host and Card, on SD_CLK, SD_CMD and SD_DATx should not exceed 1 ns.
4. $C_{CARD} \leq 10$ pF, (1 card), and $C_L = C_{BUS} + C_{HOST} + C_{CARD} \leq 40$ pF
5. The parameter values apply to both full-speed and high-speed modes.

This figure provides the eSDHC clock input timing diagram.

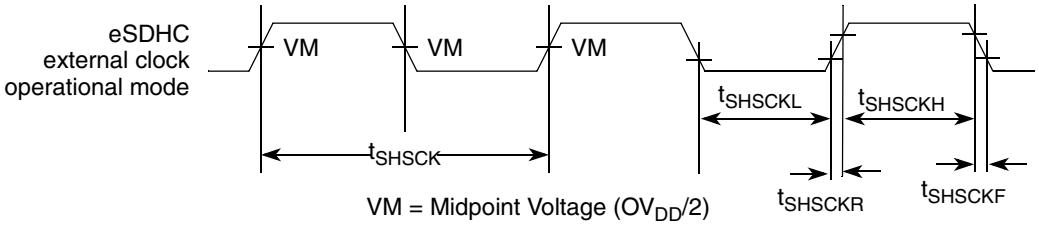


Figure 25. eSDHC Clock Input Timing Diagram

This figure provides the data and command input/output timing diagram.

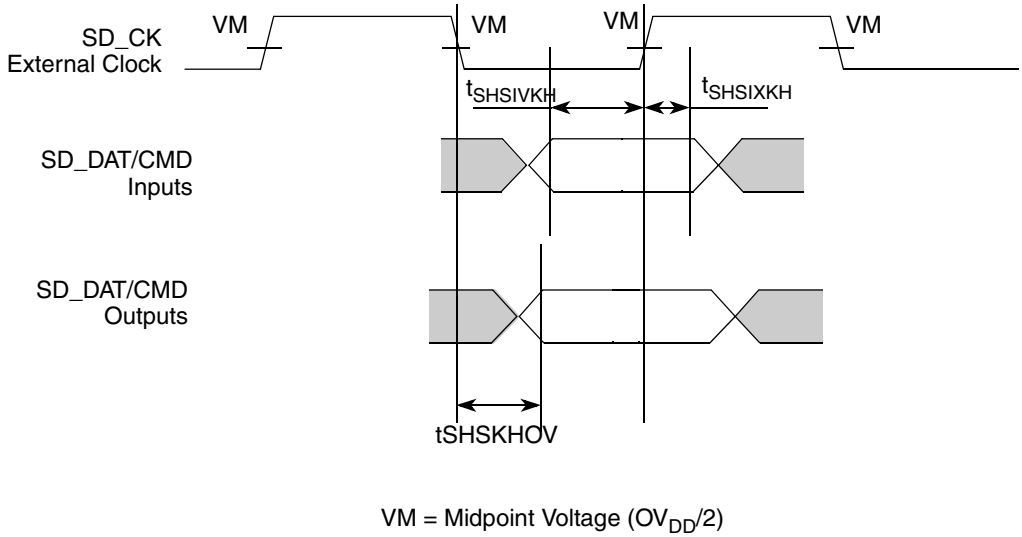


Figure 26. eSDHC Data and Command Input/Output Timing Diagram Referenced to Clock

2.16 Programmable Interrupt Controller (PIC) Specifications

This section describes the DC and AC electrical specifications for the programmable interrupt controller (PIC).

2.16.1 PIC DC specifications

This table provides the DC electrical characteristics for the PIC interface.

Table 55. PIC DC Electrical Characteristics

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—

Table 55. PIC DC Electrical Characteristics (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min V_{IL} and max V_{IH} values are based on the min and max OV_{IN} respective values found in Table 3.
2. The symbol OV_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 3.

2.16.2 PIC AC Timing Specifications

This table provides the PIC input and output AC timing specifications.

Table 56. PIC Input AC Timing Specifications

At recommended operating conditions at Table 3.

Characteristic	Symbol	Min	Max	Unit	Note
PIC inputs—minimum pulse width	t_{PIWID}	3	—	SYSCLKs	1

Note:

1. PIC inputs and outputs are asynchronous to any visible clock. PIC outputs must be synchronized before use by any external synchronous logic. PIC inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation when working in edge triggered mode

2.17 JTAG Controller

This section describes the DC and AC electrical specifications for the IEEE 1149.1 (JTAG) interface.

2.17.1 JTAG DC Electrical Characteristics

This table provides the JTAG DC electrical characteristics.

Table 57. JTAG DC Electrical Characteristics

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the OV_{IN} symbol found in Figure 3.

2.17.2 JTAG AC Timing Specifications

This table provides the JTAG AC timing specifications as defined in Figure 27 through Figure 30.

Table 58. JTAG AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter	Symbol[1]	Min	Max	Unit	Note
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t_{JTG}	30	—	ns	—
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	15	—	ns	—
JTAG external clock rise and fall times	t_{JTGR}/t_{JTGF}	0	2	ns	—
$\overline{TRST}$ assert time	t_{TRST}	25	—	ns	2
Input setup times	t_{JTDVKH}	4	—	ns	—
Input hold times	t_{JTDXKH}	10	—	ns	—
Output valid times Boundary-scan data TDO	t_{JTKLDV}	—	 15 10	ns	3
Output hold times	t_{JTKLDX}	0	—	ns	3

Notes:

1. The symbols used for timing specifications follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) reaching the invalid state (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. TRST_B is an asynchronous level sensitive signal. The setup time is for test purposes only.
3. All outputs are measured from the midpoint voltage of the falling edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load. Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.

This figure provides the AC test load for TDO and the boundary-scan outputs of the device.

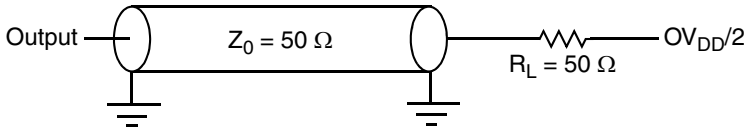


Figure 27. AC Test Load for the JTAG Interface

This figure provides the JTAG clock input timing diagram.

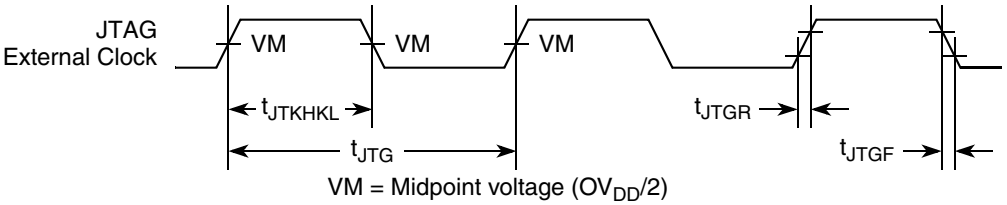


Figure 28. JTAG Clock Input Timing Diagram

This figure provides the $\overline{\text{TRST}}$ timing diagram.

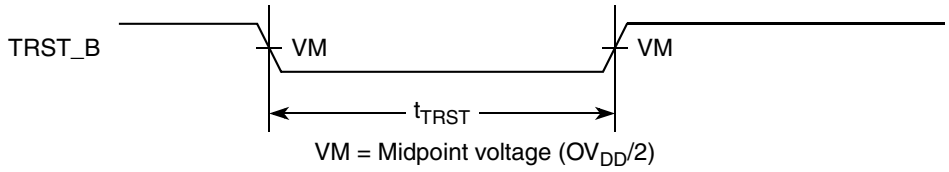


Figure 29. TRST_B Timing Diagram

This figure provides the boundary-scan timing diagram.

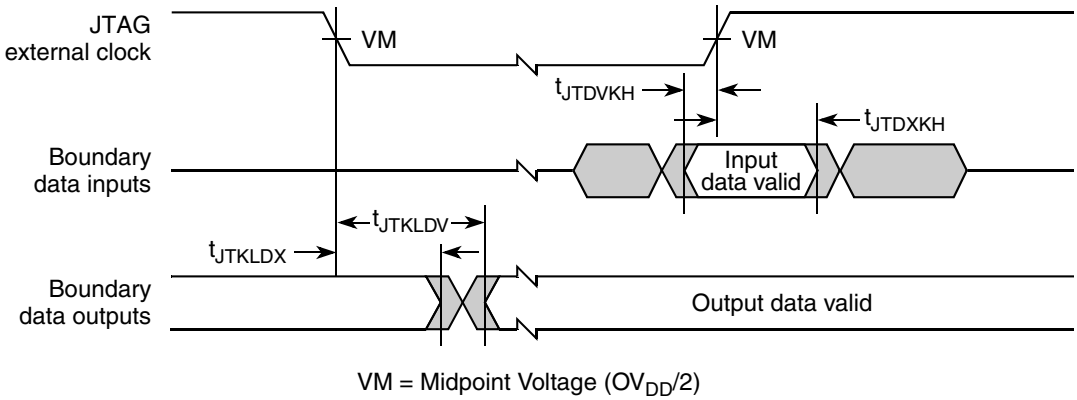


Figure 30. Boundary-Scan Timing Diagram

2.18 I²C

This section describes the DC and AC electrical characteristics for the I²C interface.

2.18.1 I²C DC Electrical Characteristics

This table provides the DC electrical characteristics for the I²C interfaces.

Table 59. I²C DC Electrical Characteristics

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	0	0.4	V	2
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	3
Input current each I/O pin (input voltage is between 0.1 × OV_{DD} and 0.9 × OV_{DD}(max)	I_I	–40	40	μA	4

Table 59. I²C DC Electrical Characteristics (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Capacitance for each I/O pin	C_I	—	10	pF	—

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. Output voltage (open drain or open collector) condition = 3 mA sink current.
3. For information about the digital filter used, see *P4080 QorIQ Integrated Multicore Communication Processor Family Reference Manual*.
4. I/O pins obstruct the SDA and SCL lines if OV_{DD} is switched off.

2.18.2 I²C AC Electrical Specifications

This table provides the AC timing parameters for the I²C interfaces.

Table 60. I²C AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol[1]	Min	Max	Unit	Note
SCL clock frequency	f_{I2C}	0	400	kHz	2
Low period of the SCL clock	t_{I2CL}	1.3	—	µs	—
High period of the SCL clock	t_{I2CH}	0.6	—	µs	—
Setup time for a repeated START condition	t_{I2SVKH}	0.6	—	µs	—
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL}	0.6	—	µs	—
Data setup time	t_{I2DVKH}	100	—	ns	—
Data input hold time: CBUS compatible masters I²C bus devices	t_{I2DXKL}	 — 0	 — —	µs	3
Data output delay time	t_{I2OVKL}	—	0.9	µs	4
Setup time for STOP condition	t_{I2PVKH}	0.6	—	µs	—
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	µs	—
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	$0.1 \times OV_{DD}$	—	V	—
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	$0.2 \times OV_{DD}$	—	V	—
Capacitive load for each bus line	Cb	—	400	pF	—

Table 60. I²C AC Timing Specifications (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol[1]	Min	Max	Unit	Note

Notes:

1. The symbols used for timing specifications herein follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the START condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the STOP condition (P) reaches the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time.
2. The requirements for I²C frequency calculation must be followed. See application note AN2919, "Determining the I²C Frequency Divider Ratio for SCL."
3. As a transmitter, the device provides a delay time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL to avoid unintended generation of a START or STOP condition. When the chip acts as the I²C bus master while transmitting, it drives both SCL and SDA. As long as the load on SCL and SDA are balanced, the chip does not generate an unintended START or STOP condition. Therefore, the 300 ns SDA output delay time is not a concern. If, under some rare condition, the 300 ns SDA output delay time is required for the chip as transmitter, see application note AN2919, "Determining the I²C Frequency Divider Ratio for SCL."
4. The maximum t_{I2OVKL} must be met only if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.

This figure provides the AC test load for the I²C.

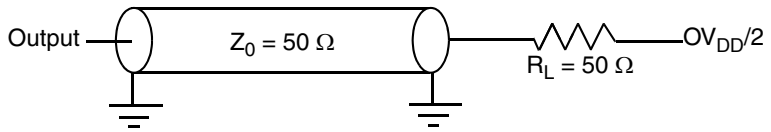


Figure 31. I²C AC Test Load

This figure shows the AC timing diagram for the I²C bus.

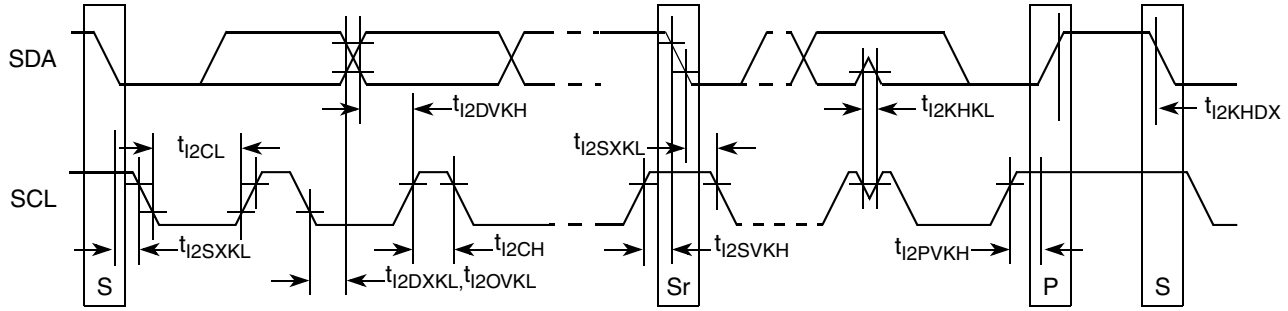


Figure 32. I²C Bus AC Timing Diagram

2.19 GPIO

This section describes the DC and AC electrical characteristics for the GPIO interface. GPIO[0:29] operate at OV_{DD} =3.3 V, while GPIO[30:31] operate at LV_{DD}. See Table 1.

2.19.1 GPIO DC Electrical Characteristics

This table provides the DC electrical characteristics for GPIO pins operating at LV_{DD} or OV_{DD} =3.3 V.

Table 61. GPIO DC Electrical Characteristics (3.3 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min V_{IL} and max V_{IH} values are based on the min and max OV_{IN} respective values found in Table 3.
2. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Section 2.1.2, "Recommended Operating Conditions."

This table provides the DC electrical characteristics for GPIO pins operating at LV_{DD} = 2.5 V.

Table 62. GPIO DC Electrical Characteristics (2.5 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.7	—	V	1
Input low voltage	V_{IL}	—	0.7	V	1
Input current (V_{IN} = 0 V or V_{IN} = LV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (LV_{DD} = min, I_{OH} = –1 mA)	V_{OH}	2.0	—	V	—
Output low voltage (LV_{DD} = min, I_{OL} = 1 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Section 2.1.2, "Recommended Operating Conditions."

This table provides the DC electrical characteristics for GPIO pins operating at LV_{DD} = 1.8 V.

Table 63. GPIO DC Electrical Characteristics (1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.25	—	V	1
Input low voltage	V_{IL}	—	0.6	V	1
Input current (V_{IN} = 0 V or V_{IN} = LV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (LV_{DD} = min, I_{OH} = –0.5 mA)	V_{OH}	1.35	—	V	—
Output low voltage (LV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Section 2.1.2, "Recommended Operating Conditions."

2.19.2 GPIO AC Timing Specifications

This table provides the GPIO input and output AC timing specifications.

Table 64. GPIO Input AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Unit	Note
GPIO inputs—minimum pulse width	t_{PIWID}	20	ns	1

Notes:

1. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs must be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} to ensure proper operation.

This figure provides the AC test load for the GPIO.

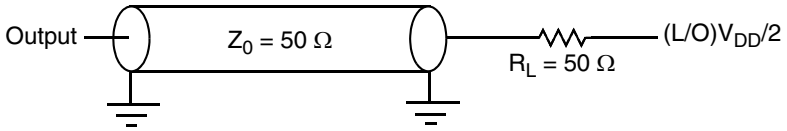


Figure 33. GPIO AC Test Load

2.20 High-Speed Serial Interfaces (HSSI)

The chip features a Serializer/Deserializer (SerDes) interface to be used for high-speed serial interconnect applications. The SerDes interface can be used for PCI Express, serial RapidIO, XAUI, Aurora and SGMII data transfers.

This section describes the common portion of SerDes DC electrical specifications: the DC requirement for SerDes reference clocks. The SerDes data lane's transmitter (Tx) and receiver (Rx) reference circuits are also shown.

2.20.1 Signal Terms Definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

The following figure shows how the signals are defined. For illustration purposes only, one SerDes lane is used in the description. The following figure shows the waveform for either a transmitter output (SD_TX*n* and SD_TX*n*_B) or a receiver input (SD_RX*n* and SD_RX*n*_B). Each signal swings between A volts and B volts where A > B.

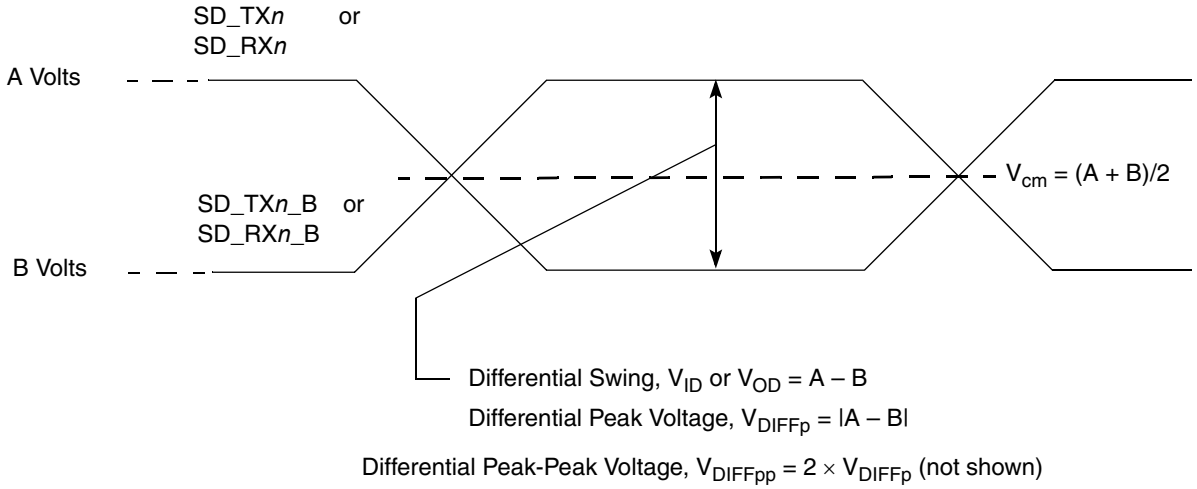


Figure 34. Differential Voltage Definitions for Transmitter or Receiver

Using this waveform, the definitions are as shown in the following list. To simplify the illustration, the definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment:

Single-Ended Swing The transmitter output signals and the receiver input signals SD_TX*n*, SD_TX*n*_B, SD_RX*n* and SD_RX*n*_B each have a peak-to-peak swing of A – B volts. This is also referred as each signal wire's single-ended swing.

Differential Output Voltage, V_{OD} (or **Differential Output Swing**):

The differential output voltage (or swing) of the transmitter, V_{OD}, is defined as the difference of the two complimentary output voltages: $V_{SD_TXn} - V_{SD_TXn_B}$. The V_{OD} value can be either positive or negative.

Differential Input Voltage, V_{ID} (or **Differential Input Swing**):

The differential input voltage (or swing) of the receiver, V_{ID}, is defined as the difference of the two complimentary input voltages: $V_{SD_RXn} - V_{SD_RXn_B}$. The V_{ID} value can be either positive or negative.

Differential Peak Voltage, V_{DIFFp}

The peak value of the differential transmitter output signal or the differential receiver input signal is defined as the differential peak voltage, $V_{DIFFp} = |A - B|$ volts.

Differential Peak-to-Peak, $V_{DIFFp-p}$

Since the differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to –(A – B) volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak-to-peak voltage, $V_{DIFFp-p} = 2 \times V_{DIFFp} = 2 \times |(A - B)|$ volts, which is twice the differential swing in amplitude, or twice of the differential peak. For example, the output differential peak-peak voltage can also be calculated as $V_{TX-DIFFp-p} = 2 \times |V_{OD}|$.

Differential Waveform

The differential waveform is constructed by subtracting the inverting signal (SD_TX*n*_B, for example) from the non-inverting signal (SD_TX*n*_B, for example) within a differential pair. There is only one signal trace curve in a differential waveform. The voltage represented in the differential waveform is not referenced to ground. See Figure 39 as an example for differential waveform.

Common Mode Voltage, V_{cm}

The common mode voltage is equal to half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, $V_{cm_out} = (V_{SD_TXn} + V_{SD_TXn_B}) \div 2 = (A + B) \div 2$, which is the arithmetic mean of the two complimentary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. It may be different between the receiver input and driver output circuits within the same component. It is also referred to as the DC offset on some occasions.

To illustrate these definitions using real values, consider the example of a current mode logic (CML) transmitter that has a common mode voltage of 2.25 V and outputs, TD and TD_B. If these outputs have a swing from 2.0 V to 2.5 V, the peak-to-peak voltage swing of each signal (TD or TD_B) is 500 mV p-p, which is referred to as the single-ended swing for each signal. Because the differential signaling environment is fully symmetrical in this example, the transmitter output's differential swing (V_{OD}) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 mV and –500 mV. In other words, V_{OD} is 500 mV in one phase and –500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage ($V_{DIFFp-p}$) is 1000 mV p-p.

2.20.2 SerDes Reference Clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks inputs are SD_REF_CLK1 and SD_REF_CLK1_B for SerDes bank1, SD_REF_CLK3 and SD_REF_CLK3_B for SerDes banks 2 and 3.

NOTE

SerDes bank 2 is driven internally by SD_REF_CLK3 and bank 3's PLL. SD_REF_CLK2 continues to clock internal logic for bank 2 and therefore, SD_REF_CLK2 and SD_REF_CLK2_B are still required when bank 2 is enabled. SD_REF_CLK3 is required when either bank 2 or bank 3 are enabled.

SerDes banks 1–3 may be used for various combinations of the following IP blocks based on the RCW Configuration field SRDS_PRTCL:

- SerDes bank 1: PEX1/2/3, sRIO1/2, SGMII, Aurora.
- SerDes bank 2: PEX3, SGMII, or XAUI.
- SerDes bank 3: SGMII, or XAUI.

The following sections describe the SerDes reference clock requirements and provide application information.

2.20.2.1 SerDes Reference Clock Receiver Characteristics

This figure shows a receiver reference diagram of the SerDes reference clocks.

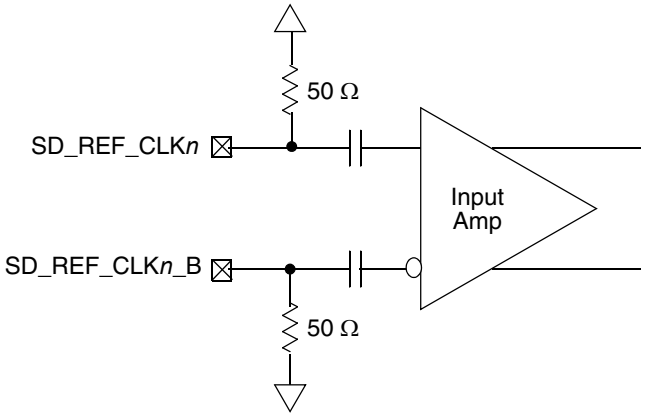


Figure 35. Receiver of SerDes Reference Clocks

The characteristics of the clock signals are as follows:

- The SerDes transceivers core power supply voltage requirements (SV_{DD}) are as specified in Section 2.1.2, "Recommended Operating Conditions."
- The SerDes reference clock receiver reference circuit structure is as follows:
  - The SD_REF_CLK*n* and SD_REF_CLK*n*_B are internally AC-coupled differential inputs as shown in Figure 35. Each differential clock input (SD_REF_CLK*n* or SD_REF_CLK*n*_B) has on-chip 50-Ω termination to SGND followed by on-chip AC-coupling.
  - The external reference clock driver must be able to drive this termination.
  - The SerDes reference clock input can be either differential or single-ended. See the differential mode and single-ended mode descriptions below for detailed requirements.
- The maximum average current requirement also determines the common mode voltage range.
  - When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8 mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA because the input is AC-coupled on-chip.
  - This current limitation sets the maximum common mode input voltage to be less than 0.4 V (0.4 V ÷ 50 = 8 mA) while the minimum common mode input level is 0.1 V above SGND. For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0 mA to 16 mA (0–0.8 V), such that each phase of the differential input has a single-ended swing from 0 V to 800 mV with the common mode voltage at 400 mV.
  - If the device driving the SD_REF_CLK*n* and SD_REF_CLK*n*_B inputs cannot drive 50 Ω to SGND DC or the drive strength of the clock driver chip exceeds the maximum input current limitations, it must be AC-coupled off-chip.
- The input amplitude requirement is described in detail in the following sections.

2.20.2.2 DC Level Requirement for SerDes Reference Clocks

The DC level requirement for the SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs, as described below:

- Differential Mode
  - The input amplitude of the differential clock must be between 400 mV and 1600 mV differential peak-peak (or between 200 mV and 800 mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing of less than 800 mV and greater than 200 mV. This requirement is the same for both external DC-coupled or AC-coupled connection.
  - For an external DC-coupled connection, as described in Section 2.20.2.1, "SerDes Reference Clock Receiver Characteristics," the maximum average current requirements sets the requirement for average voltage (common mode voltage) as between 100 mV and 400 mV. The following figure shows the SerDes reference clock input requirement for DC-coupled connection scheme.

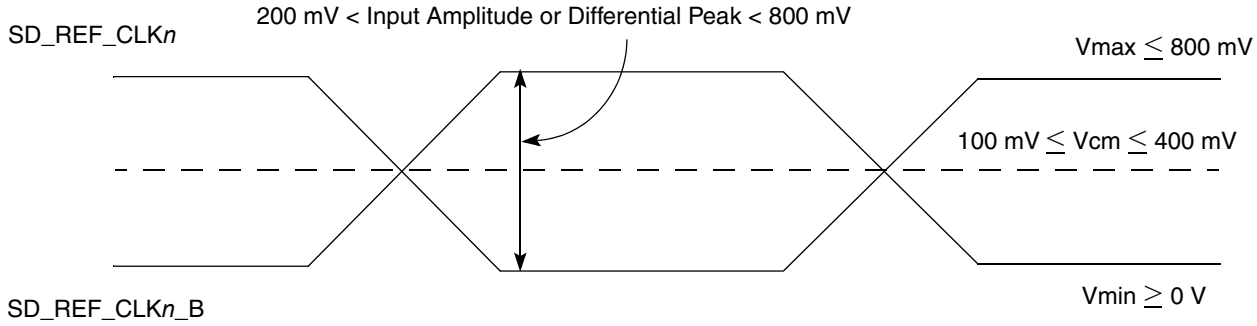


Figure 36. Differential Reference Clock Input DC Requirements (External DC-Coupled)

  - For an external AC-coupled connection, there is no common mode voltage requirement for the clock driver. Because the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different common mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to SGND. Each signal wire of the differential inputs is allowed to swing below and above the common mode voltage (SGND). The following figure shows the SerDes reference clock input requirement for AC-coupled connection scheme.

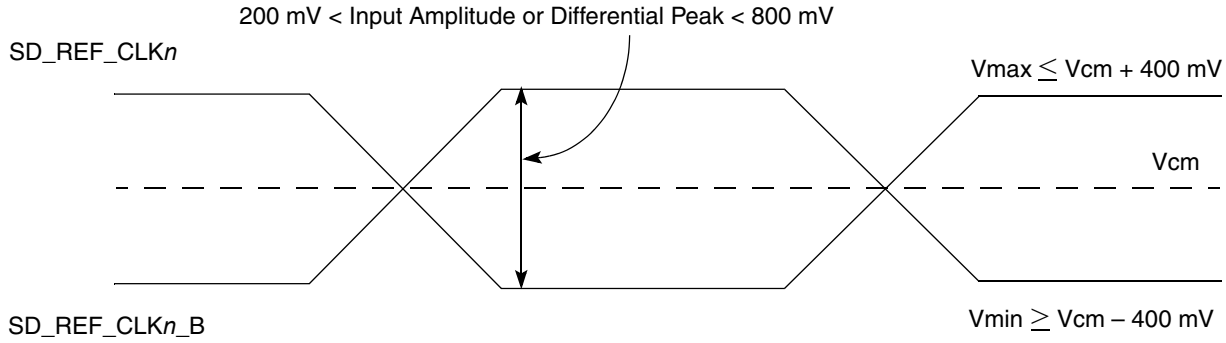


Figure 37. Differential Reference Clock Input DC Requirements (External AC-Coupled)

- Single-Ended Mode
  - The reference clock can also be single-ended. The SD_REF_CLK*n* input amplitude (single-ended swing) must be between 400 mV and 800 mV peak-peak (from V_{MIN} to V_{MAX}) with SD_REF_CLK*n*_B either left unconnected or tied to ground.
  - The SD_REF_CLK*n* input average voltage must be between 200 and 400 mV. The following figure shows the SerDes reference clock input requirement for single-ended signaling mode.

— To meet the input amplitude requirement, the reference clock inputs may need to be DC- or AC-coupled externally. For the best noise performance, the reference of the clock could be DC- or AC-coupled into the unused phase (SD_REF_CLK*n*_B) through the same source impedance as the clock input (SD_REF_CLK*n*) in use.

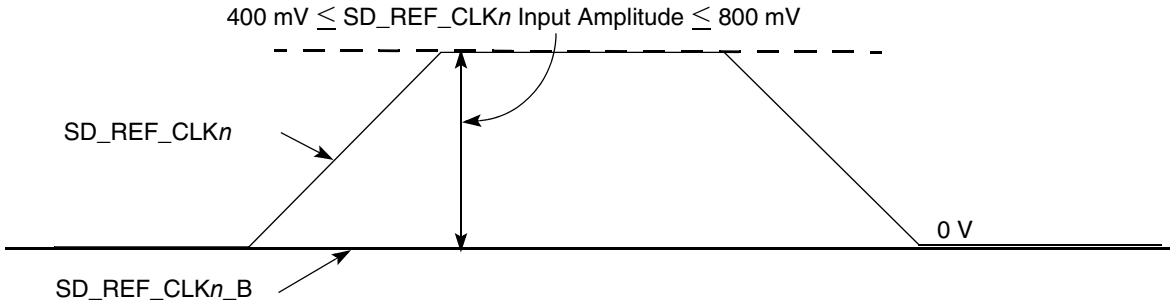


Figure 38. Single-Ended Reference Clock Input DC Requirements

2.20.2.3 AC Requirements for SerDes Reference Clocks

This table lists AC requirements for the PCI Express, SGMII, serial RapidIO and Aurora SerDes reference clocks to be guaranteed by the customer's application design.

Table 65. SD_REF_CLK*n* and SD_REF_CLK*n*_B Input Clock Requirements

At recommended operating conditions with SV_{DD} = 1.0 V.

Parameter	Symbol	Min	Typ	Max	Unit	Note
SD_REF_CLK/SD_REF_CLK_B frequency range	t_{CLK_REF}	—	100/125	—	MHz	1
SD_REF_CLK/SD_REF_CLK _B clock frequency tolerance	t_{CLK_TOL}	–350	—	350	ppm	—
SD_REF_CLK/SD_REF_CLK_B reference clock duty cycle (measured at 1.6 V)	t_{CLK_DUTY}	40	50	60	%	—
SD_REF_CLK/SD_REF_CLK_B max deterministic peak-peak jitter at 10^{-6} BER	t_{CLK_DJ}	—	—	42	ps	—
SD_REF_CLK/SD_REF_CLK_B total reference clock jitter at 10^{-6} BER (peak-to-peak jitter at refClk input)	t_{CLK_TJ}	—	—	86	ps	2
SD_REF_CLK/SD_REF_CLK_B rising/falling edge rate	t_{CLKRR}/t_{CLKFR}	1	—	4	V/ns	3

Table 65. SD_REF_CLK*n* and SD_REF_CLK*n*_B Input Clock Requirements (continued)

At recommended operating conditions with SV_{DD} = 1.0 V.

Parameter	Symbol	Min	Typ	Max	Unit	Note
Differential input high voltage	V_{IH}	200	—	—	mV	4
Differential input low voltage	V_{IL}	—	—	–200	mV	4
Rising edge rate (SD_REF_CLK*n*) to falling edge rate (SD_REF_CLK*n*) matching	Rise-fall matching	—	—	20	%	5, 6

Notes:
1. **Caution:** Only 100 and 125 have been tested. In-between values do not work correctly with the rest of the system.
2. Limits from PCI Express CEM Rev 2.0
3. Measured from –200 mV to +200 mV on the differential waveform (derived from SD_REF_CLK*n* minus SD_REF_CLK*n*_B). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See Figure 39.
4. Measurement taken from differential waveform
5. Measurement taken from single-ended waveform
6. Matching applies to rising edge for SD_REF_CLK*n* and falling edge rate for SD_REF_CLK*n*_B. It is measured using a 200 mV window centered on the median cross point where SD_REF_CLK*n* rising meets SD_REF_CLK*n*_B falling. The median cross point is used to calculate the voltage thresholds that the oscilloscope uses for the edge rate calculations. The rise edge rate of SD_REF_CLK*n* must be compared to the fall edge rate of SD_REF_CLK*n*_B, the maximum allowed difference must not exceed 20% of the slowest edge rate. See Figure 40.

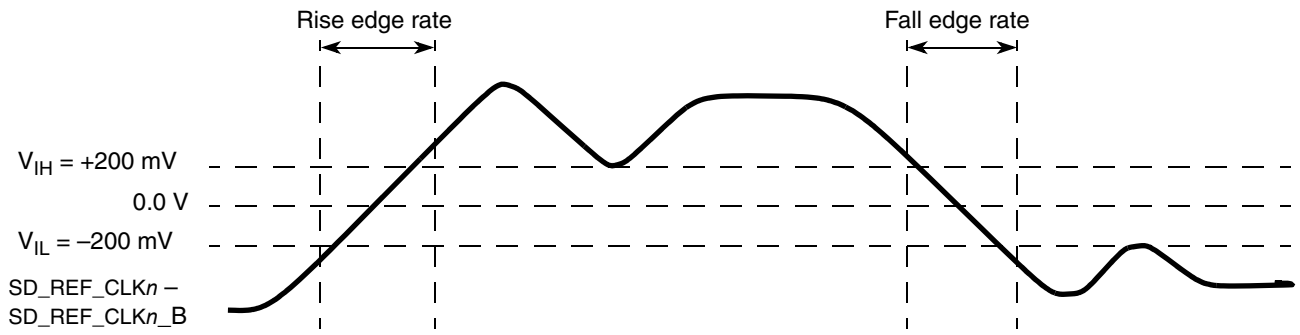


Figure 39. Differential Measurement Points for Rise and Fall Time

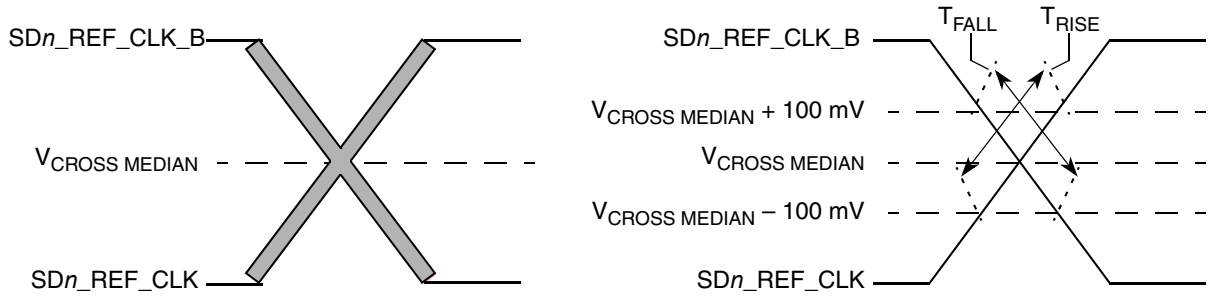


Figure 40. Single-Ended Measurement Points for Rise and Fall Time Matching

2.20.2.4 Spread-Spectrum Clock

- SD_REF_CLK1/SD_REF_CLK1_B were designed to work with a spread spectrum clock (+0 to 0.5% spreading at 30–33 kHz rate is allowed), assuming both ends have same reference clock. For better results, a source without significant unintended modulation must be used.
- SD_REF_CLK2/SD_REF_CLK2_B were designed to work with a spread spectrum clock (+0 to 0.5% spreading at 30–33 kHz rate is allowed), assuming both ends have same reference clock and the industry protocol specifications supports it. For better results, a source without significant unintended modulation must be used.
- SD_REF_CLK3/SD_REF_CLK3_B are not intended to be used with, and must not be clocked by, a spread spectrum clock source.

2.20.3 SerDes Transmitter and Receiver Reference Circuits

This figure shows the reference circuits for SerDes data lane's transmitter and receiver.

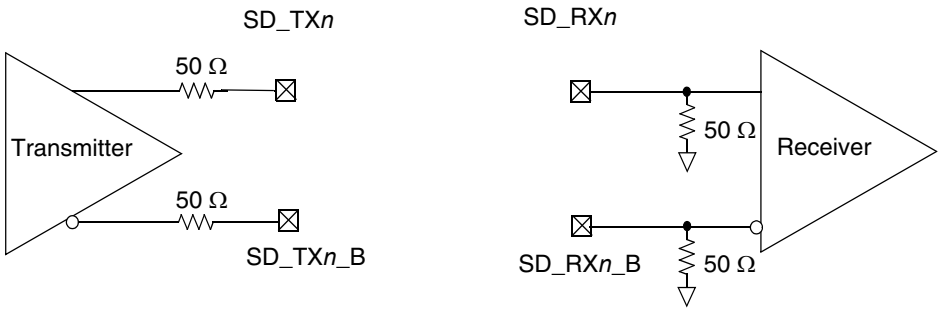


Figure 41. SerDes Transmitter and Receiver Reference Circuits

The DC and AC specification of SerDes data lanes are defined in each interface protocol section below based on the application usage:

- Section 2.20.4, "PCI Express"
- Section 2.20.5, "Serial RapidIO (sRIO)"
- Section 2.20.6, "XAUI"
- Section 2.20.7, "Aurora"
- Section 2.20.8, "SGMII Interface"

Note that external AC-coupling capacitor is required for the above serial transmission protocols per the protocol's standard requirements.

2.20.4 PCI Express

This section describes the clocking dependencies, DC and AC electrical specifications for the PCI Express bus.

2.20.4.1 Clocking Dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 parts per million (ppm) of each other at all times. This is specified to allow bit rate clock sources with a ±300 ppm tolerance.

2.20.4.2 PCI Express Clocking Requirements for SD_REF_CLK*n* and SD_REF_CLK*n*_B

This section specifies PCI Express requirements for SD_REF_CLK*n* and SD_REF_CLK*n*_B, where *n* = [1–3]. SerDes banks 1–2 may be used for various SerDes PCI Express configurations based on the RCW Configuration field SRDS_PRTCL. PCI Express is not supported on SerDes bank 3. SD_REF_CLK3 and SD_REF_CLK3_B must be supplied to use PCI Express on SerDes bank 2.

For more information on these specifications, see Section 2.20.2, "SerDes Reference Clocks."

2.20.4.3 PCI Express DC Physical Layer Specifications

This section contains the DC specifications for the physical layer of PCI Express on this device.

2.20.4.3.1 PCI Express DC Physical Layer Transmitter Specifications

This section discusses the PCI Express DC physical layer transmitter specifications for 2.5 GT/s and 5 GT/s.

This table defines the PCI Express 2.0 (2.5 GT/s) DC specifications for the differential output at all transmitters. The parameters are specified at the component pins.

Table 66. PCI Express 2.0 (2.5 GT/s) Differential Transmitter (Tx) Output DC Specifications

At recommended operating conditions with XV_{DD} = 1.5 V or 1.8 V.

Parameter	Symbol	Min	Typical	Max	Units	Note
Differential peak-to-peak output voltage	$V_{TX\text{-}DIFFp\text{-}p}$	800	1000	1200	mV	$V_{TX\text{-}DIFFp\text{-}p} = 2 \times \lvert V_{TX\text{-}D+} - V_{TX\text{-}D-} \rvert$ See Note 1.
De-emphasized differential output voltage (ratio)	$V_{TX\text{-}DE\text{-}RATIO}$	3.0	3.5	4.0	dB	Ratio of the $V_{TX\text{-}DIFFp\text{-}p}$ of the second and following bits after a transition divided by the $V_{TX\text{-}DIFFp\text{-}p}$ of the first bit after a transition. See Note 1.
DC differential Tx impedance	$Z_{TX\text{-}DIFF\text{-}DC}$	80	100	120	Ω	Tx DC differential mode low Impedance
Transmitter DC impedance	$Z_{TX\text{-}DC}$	40	50	60	Ω	Required Tx D+ as well as D– DC Impedance during all states

Note:
1. Measured at the package pins with a test load of 50 Ω to GND on each pin.

This table defines the PCI Express 2.0 (5 GT/s) DC specifications for the differential output at all transmitters. The parameters are specified at the component pins.

Table 67. PCI Express 2.0 (5 GT/s) Differential Transmitter (Tx) Output DC Specifications

At recommended operating conditions with XV_{DD} = 1.5 V or 1.8 V

Parameter	Symbol	Min	Typical	Max	Units	Note
Differential peak-to-peak output voltage	$V_{TX\text{-}DIFFp\text{-}p}$	800	1000	1200	mV	$V_{TX\text{-}DIFFp\text{-}p} = 2 \times \lvert V_{TX\text{-}D+} - V_{TX\text{-}D-} \rvert$ See Note 1.
Low Power differential peak-to-peak output voltage	$V_{TX\text{-}DIFFp\text{-}p_low}$	400	500	1200	mV	$V_{TX\text{-}DIFFp\text{-}p} = 2 \times \lvert V_{TX\text{-}D+} - V_{TX\text{-}D-} \rvert$ See Note 1.

Table 67. PCI Express 2.0 (5 GT/s) Differential Transmitter (Tx) Output DC Specifications (continued)

At recommended operating conditions with XV_{DD} = 1.5 V or 1.8 V

Parameter	Symbol	Min	Typical	Max	Units	Note
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-3.5dB}$	3.0	3.5	4.0	dB	Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition. See Note 1.
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-6.0dB}$	5.5	6.0	6.5	dB	Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition. See Note 1.
DC differential Tx impedance	$Z_{TX-DIFF-DC}$	80	100	120	Ω	Tx DC differential mode low impedance
Transmitter DC Impedance	Z_{TX-DC}	40	50	60	Ω	Required Tx D+ as well as D– DC impedance during all states

Note:
1. Measured at the package pins with a test load of 50Ω to GND on each pin.

2.20.4.4 PCI Express DC Physical Layer Receiver Specifications

This section discusses the PCI Express DC physical layer receiver specifications 2.5 GT/s, and 5 GT/s

This table defines the DC specifications for the PCI Express 2.0 (2.5 GT/s) differential input at all receivers. The parameters are specified at the component pins.

Table 68. PCI Express 2.0 (2.5 GT/s) Differential Receiver (Rx) Input DC Specifications

At recommended operating conditions with XV_{DD} = 1.5 V or 1.8 V

Parameter	Symbol	Min	Typ	Max	Units	Note
Differential input peak-to-peak voltage	$V_{RX-DIFFp-p}$	120	1000	1200	mV	$V_{RX-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$ See Note 1.
DC differential input impedance	$Z_{RX-DIFF-DC}$	80	100	120	Ω	Rx DC differential mode impedance. See Note 2
DC input impedance	Z_{RX-DC}	40	50	60	Ω	Required Rx D+ as well as D– DC Impedance (50 ±20% tolerance). See Notes 1 and 2.
Powered down DC input impedance	$Z_{RX-HIGH-IMP-DC}$	50	—	—	kΩ	Required Rx D+ as well as D– DC Impedance when the receiver terminations do not have power. See Note 3.

Table 68. PCI Express 2.0 (2.5 GT/s) Differential Receiver (Rx) Input DC Specifications (continued)

At recommended operating conditions with XV_{DD} = 1.5 V or 1.8 V

Parameter	Symbol	Min	Typ	Max	Units	Note
Electrical idle detect threshold	$V_{RX\text{-}IDLE\text{-}DET\text{-}DIFFp\text{-}p}$	65	—	175	mV	$V_{RX\text{-}IDLE\text{-}DET\text{-}DIFFp\text{-}p}$ = $2 \times \lvert V_{RX\text{-}D+} - V_{RX\text{-}D-} \rvert$ Measured at the package pins of the receiver

Notes:
1. Measured at the package pins with a test load of 50Ω to GND on each pin.
2. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.
3. The Rx DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the Rx ground.

This table defines the DC specifications for the PCI Express 2.0 (5 GT/s) differential input at all receivers (RXs). The parameters are specified at the component pins.

Table 69. PCI Express 2.0 (5 GT/s) Differential Receiver (Rx) Input DC Specifications

At recommended operating conditions with XV_{DD} = 1.5 V or 1.8 V

Parameter	Symbol	Min	Typ	Max	Units	Note
Differential input peak-to-peak voltage	$V_{RX\text{-}DIFFp\text{-}p}$	120	1000	1200	V	$V_{RX\text{-}DIFFp\text{-}p} = 2 \times \lvert V_{RX\text{-}D+} - V_{RX\text{-}D-} \rvert$ See Note 1.
DC differential input impedance	$Z_{RX\text{-}DIFF\text{-}DC}$	80	100	120	Ω	Rx DC Differential mode impedance. See Note 2
DC input impedance	$Z_{RX\text{-}DC}$	40	50	60	Ω	Required Rx D+ as well as D– DC Impedance (50 ±20% tolerance). See Notes 1 and 2.
Powered down DC input impedance	$Z_{RX\text{-}HIGH\text{-}IMP\text{-}DC}$	50	—	—	kΩ	Required Rx D+ as well as D– DC Impedance when the Receiver terminations do not have power. See Note 3.
Electrical idle detect threshold	$V_{RX\text{-}IDLE\text{-}DET\text{-}DIFFp\text{-}p}$	65	—	175	mV	$V_{RX\text{-}IDLE\text{-}DET\text{-}DIFFp\text{-}p}$ = $2 \times \lvert V_{RX\text{-}D+} - V_{RX\text{-}D-} \rvert$ Measured at the package pins of the receiver

Notes:
1. Measured at the package pins with a test load of 50Ω to GND on each pin.
2. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.
3. The Rx DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the Rx ground.

2.20.4.5 PCI Express AC Physical Layer Specifications

This section contains the DC specifications for the physical layer of PCI Express on this device.

2.20.4.5.1 PCI Express AC Physical Layer Transmitter Specifications

This section discusses the PCI Express AC physical layer transmitter specifications 2.5 GT/s, and 5 GT/s.

This table defines the PCI Express 2.0 (2.5 GT/s) AC specifications for the differential output at all transmitters (TXs). The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 70. PCI Express 2.0 (2.5 GT/s) Differential Transmitter (Tx) Output AC Specifications

At recommended operating conditions with XV_{DD} = 1.5 V or 1.8 V

Parameter	Symbol	Min	Typ	Max	Units	Note
Unit interval	UI	399.88	400	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for spread spectrum clock dictated variations. See Note 1.
Minimum Tx eye width	T_{TX-EYE}	0.75	—	—	UI	The maximum transmitter jitter can be derived as $T_{TX-MAX-JITTER} = 1 - T_{TX-EYE} = 0.25$ UI. Does not include spread spectrum or RefCLK jitter. Includes device random jitter at 10^{-12}. See Notes 2 and 3.
Maximum time between the jitter median and maximum deviation from the median.	$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	—	—	0.125	UI	Jitter is defined as the measurement variation of the crossing points ($V_{TX-DIFFp-p} = 0$ V) in relation to a recovered Tx UI. A recovered Tx UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the Tx UI. See Notes 2 and 3.
AC coupling capacitor	C_{TX}	75	—	200	nF	All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See Note 4.

Notes:
1. No test load is necessarily associated with this value.
2. Specified at the measurement point into a timing and voltage test load as shown in Figure 42 and measured over any 250 consecutive Tx UIs.
3. A T_{TX-EYE} = 0.75 UI provides for a total sum of deterministic and random jitter budget of $T_{TX-MAX-JITTER}$ = 0.25 UI for the transmitter collected over any 250 consecutive Tx UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total Tx jitter budget collected over any 250 consecutive Tx UIs. It must be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
4. The chip's SerDes transmitter does not have C_{TX} built-in. An external AC coupling capacitor is required.

This table defines the PCI Express 2.0 (5 GT/s) AC specifications for the differential output at all transmitters. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 71. PCI Express 2.0 (5 GT/s) Differential Transmitter (Tx) Output AC Specifications

At recommended operating conditions with XV_{DD} = 1.5 V or 1.8 V

Parameter	Symbol	Min	Typ	Max	Units	Note
Unit Interval	UI	199.94	200.00	200.06	ps	Each UI is 400 ps ± 300 ppm. UI does not account for spread spectrum clock dictated variations. See Note 1.
Minimum Tx eye width	T_{TX-EYE}	0.75	—	—	UI	The maximum Transmitter jitter can be derived as: $T_{TX-MAX-JITTER} = 1 - T_{TX-EYE} = 0.25$ UI. See Notes 2 and 3.
Tx RMS deterministic jitter > 1.5 MHz	$T_{TX-HF-DJ-DD}$	—	—	0.15	ps	—
Tx RMS deterministic jitter < 1.5 MHz	$T_{TX-LF-RMS}$	—	3.0	—	ps	Reference input clock RMS jitter (< 1.5 MHz) at pin < 1 ps
AC coupling capacitor	C_{TX}	75	—	200	nF	All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See Note 4.

Notes:

1. No test load is necessarily associated with this value.
2. Specified at the measurement point into a timing and voltage test load as shown in Figure 42 and measured over any 250 consecutive Tx UIs.
3. A T_{TX-EYE} = 0.75 UI provides for a total sum of deterministic and random jitter budget of $T_{TX-MAX-JITTER}$ = 0.25 UI for the Transmitter collected over any 250 consecutive Tx UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total Tx jitter budget collected over any 250 consecutive Tx UIs. It must be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
4. The chip's SerDes transmitter does not have C_{TX} built-in. An external AC coupling capacitor is required.

2.20.4.5.2 PCI Express AC Physical Layer Receiver Specifications

This section discusses the PCI Express AC physical layer receiver specifications 2.5 GT/s, and 5 GT/s.

This table defines the AC specifications for the PCI Express 2.0 (2.5 GT/s) differential input at all receivers. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 72. PCI Express 2.0 (2.5 GT/s) Differential Receiver (Rx) Input AC Specifications

At recommended operating conditions with XV_{DD} = 1.5 V or 1.8 V

Parameter	Symbol	Min	Typ	Max	Units	Note
Unit Interval	UI	399.88	400.00	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for spread spectrum clock dictated variations. See Note 1.
Minimum receiver eye width	T_{RX-EYE}	0.4	—	—	UI	The maximum interconnect media and Transmitter jitter that can be tolerated by the Receiver can be derived as $T_{RX-MAX-JITTER} = 1 - T_{RX-EYE} = 0.6$ UI. See Notes 2 and 3.
Maximum time between the jitter median and maximum deviation from the median.	$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	—	—	0.3	UI	Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p}$ = 0 V) in relation to a recovered Tx UI. A recovered Tx UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the Tx UI. See Notes 2, 3, and 4.

Notes:

1. No test load is necessarily associated with this value.
2. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 42 must be used as the Rx device when taking measurements. If the clocks to the Rx and Tx are not derived from the same reference clock, the Tx UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
3. A T_{RX-EYE} = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the Transmitter and interconnect collected any 250 consecutive UIs. The TRX-EYE-MEDIAN-to-MAX-JITTER specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive Tx UIs. It must be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the Rx and Tx are not derived from the same reference clock, the Tx UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
4. It is recommended that the recovered Tx UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

This table defines the AC specifications for the PCI Express 2.0 (5 GT/s) differential input at all receivers (RXs). The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 73. PCI Express 2.0 (5 GT/s) Differential Receiver (Rx) Input AC Specifications

At recommended operating conditions with XV_{DD} = 1.5 V or 1.8 V

Parameter	Symbol	Min	Typ	Max	Units	Note
Unit Interval	UI	199.40	200.00	200.06	ps	Each UI is 400 ps ±300 ppm. UI does not account for spread spectrum clock dictated variations. See Note 1.
Max Rx inherent timing error	$T_{RX-TJ-CC}$	—	—	0.4	UI	The maximum inherent total timing error for common RefClk Rx architecture
Maximum time between the jitter median and maximum deviation from the median	$T_{RX-TJ-DC}$	—	—	0.34	UI	Max Rx inherent total timing error
Max Rx inherent deterministic timing error	$T_{RX-DJ-DD-CC}$	—	—	0.30	UI	The maximum inherent deterministic timing error for common RefClk Rx architecture
Max Rx inherent deterministic timing error	$T_{RX-DJ-DD-DC}$	—	—	0.24	UI	The maximum inherent deterministic timing error for common RefClk Rx architecture

Note:
1. No test load is necessarily associated with this value.

2.20.4.6 Test and Measurement Load

The AC timing and voltage parameters must be verified at the measurement point. The package pins of the device must be connected to the test/measurement load within 0.2 inches of that load, as shown in the following figure.

NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D– not being exactly matched in length at the package pin boundary. If the vendor does not explicitly state where the measurement point is located, the measurement point is assumed to be the D+ and D– package pins.

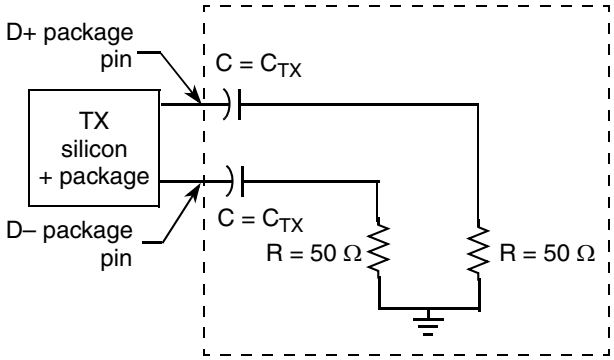


Figure 42. Test/Measurement Load

2.20.5 Serial RapidIO (sRIO)

This section describes the DC and AC electrical specifications for the serial RapidIO interface of the LP-Serial physical layer. The electrical specifications cover both single and multiple-lane links. Two transmitters (short run and long run) and a single receiver are specified for each of two baud rates: 2.50 and 3.125 GBaud.

Two transmitter specifications allow for solutions ranging from simple board-to-board interconnect to driving two connectors across a backplane. A single receiver specification is given that accepts signals from both the short run and long run transmitter specifications.

The short run transmitter must be used mainly for chip-to-chip connections on either the same printed circuit board or across a single connector. This covers the case where connections are made to a mezzanine (daughter) card. The minimum swings of the short run specification reduce the overall power used by the transceivers.

The long run transmitter specifications use larger voltage swings that are capable of driving signals across backplanes. This allows a user to drive signals across two connectors and a backplane. The specifications allow a distance of at least 50 cm at all baud rates.

All unit intervals are specified with a tolerance of ±100 ppm. The worst case frequency difference between any transmit and receive clock is 200 ppm.

To ensure interoperability between drivers and receivers of different vendors and technologies, AC coupling at the receiver input must be used.

2.20.5.1 Signal Definitions

This section defines the terms used in the description and specification of the differential signals used by the LP-Serial links. The following figure shows how the signals are defined. The figures show waveforms for either a transmitter output (TD and TD_B) or a receiver input (RD and RD_B). Each signal swings between A volts and B volts where A > B. Using these waveforms, the definitions are as follows:

- The transmitter output signals and the receiver input signals—TD, TD_B, RD, and RD_B—each have a peak-to-peak swing of A – B volts.
- The differential output signal of the transmitter, V_{OD}, is defined as $V_{TD} - V_{TD_B}$
- The differential input signal of the receiver, V_{ID}, is defined as $V_{RD} - V_{RD_B}$
- The differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to –(A – B) volts
- The peak value of the differential transmitter output signal and the differential receiver input signal is A – B volts.
- The peak-to-peak value of the differential transmitter output signal and the differential receiver input signal is 2 × (A – B) volts.

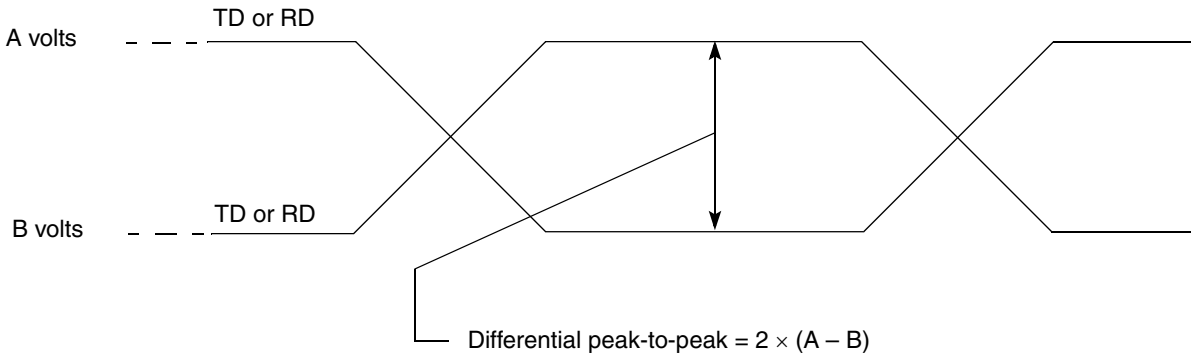


Figure 43. Differential Peak-Peak Voltage of Transmitter or Receiver

To illustrate these definitions using real values, consider the case of a CML (current mode logic) transmitter that has a common mode voltage of 2.25 V, and each of its outputs, TD and TD_B, has a swing that goes between 2.5 V and 2.0 V. Using these values, the peak-to-peak voltage swing of the signals TD and TD_B is 500 mV p-p. The differential output signal ranges between 500 mV and –500 mV. The peak differential voltage is 500 mV. The peak-to-peak differential voltage is 1000 mV p-p.

2.20.5.2 Equalization

With the use of high-speed serial links, the interconnect media causes degradation of the signal at the receiver and produces effects such as inter-symbol interference (ISI) or data-dependent jitter. This loss can be large enough to degrade the eye opening at the receiver beyond what is allowed in the specification. To negate a portion of these effects, equalization can be used. The most common equalization techniques that can be used are as follows:

- Pre-emphasis on the transmitter
- A passive high-pass filter network placed at the receiver, often referred to as passive equalization
- The use of active circuits in the receiver, often referred to as adaptive equalization

2.20.5.3 Serial RapidIO Clocking Requirements for SD_REF_CLK*n* and SD_REF_CLK*n*_B

This section specifies serial RapidIO DC requirements for SD_REF_CLK1 and SD_REF_CLK1_B. Only SerDes bank 1 may be used for various SerDes serial RapidIO configurations based on the RCW Configuration field SRDS_PRTCL. Serial RapidIO is not supported on SerDes banks 2–3.

For more information on these specifications, see Section 2.20.2, “SerDes Reference Clocks.”

2.20.5.4 DC Requirements for Serial RapidIO

This section explains the DC requirements for the serial RapidIO interface.

2.20.5.4.1 DC Serial RapidIO Timing Transmitter Specifications

LP-Serial transmitter electrical and timing specifications are stated in the text and tables of this section.

The differential return loss, S11, of the transmitter in each case is better than the following:

- –10 dB for (Baud Frequency) ÷ 10 < Freq(f) < 625 MHz
- –10 dB + 10log(f ÷ 625 MHz) dB for 625 MHz ≤ Freq(f) ≤ Baud Frequency

The reference impedance for the differential return loss measurements is 100-Ω resistive. Differential return loss includes contributions from on-chip circuitry, chip packaging, and any off-chip components related to the driver. The output impedance requirement applies to all valid output levels.

- It is recommended that the 20%–80% rise/fall time of the transmitter, as measured at the transmitter output, have a minimum value 60 ps in each case.
- It is recommended that the timing skew at the output of an LP-Serial transmitter between the two signals that comprise a differential pair not exceed 20 ps at 2.50 GBaud and 15 ps at 3.125 GBaud.

This table defines the transmitter DC specifications for serial RapidIO.

Table 74. sRIO Transmitter DC Timing Specifications—2.5 GBaud, 3.125 GBaud

At recommended operating conditions with XV_{DD} = 1.5 V or 1.8 V

Parameter	Symbol	Min	Typ	Max	Unit	Note
Output Voltage,	V_O	–0.40	—	2.30	V	1
Long-run differential output voltage	V_{DIFFPP}	800	—	1600	mV p-p	—
Short-run differential output voltage	V_{DIFFPP}	500	—	1000	mV p-p	—

Note:
1. Voltage relative to COMMON of either signal comprising a differential pair.

2.20.5.4.2 DC Serial RapidIO Receiver Specifications

LP-Serial receiver electrical and timing specifications are stated in the text and tables of this section.

Receiver input impedance results in a differential return loss better than 10 dB and a common mode return loss better than 6 dB from 100 MHz to (0.8) × (Baud Frequency). This includes contributions from on-chip circuitry, the chip package, and any off-chip components related to the receiver. AC coupling components are included in this requirement. The reference impedance for return loss measurements is 100-Ω resistive for differential return loss and 25-Ω resistive for common mode.

This table defines the receiver DC specifications for serial RapidIO.

Table 75. Serial RapidIO Receiver DC Timing Specifications—2.5 GBaud, 3.125 GBaud

At recommended operating conditions with XV_{DD} = 1.5 V or 1.8 V

Parameter	Symbol	Min	Typ	Max	Unit	Note
Differential input voltage	V_{IN}	200	—	1600	mV p-p	1

Note:
1. Measured at receiver

2.20.5.5 AC Requirements for Serial RapidIO

This section explains the AC requirements for the serial RapidIO interface.

2.20.5.5.1 AC Requirements for Serial RapidIO Transmitter

This table defines the transmitter AC specifications for the serial RapidIO. The AC timing specifications do not include RefClk jitter.

Table 76. Serial RapidIO Transmitter AC Timing Specifications

At recommended operating conditions with XV_{DD} = 1.5 V or 1.8 V

Parameter	Symbol	Min	Typical	Max	Unit	Note
Deterministic jitter	J_D	—	—	0.17	UI p-p	—
Total jitter	J_T	—	—	0.35	UI p-p	—
Unit Interval: 2.5 GBaud	UI	400 – 100ppm	400	400 + 100ppm	ps	—
Unit Interval: 3.125 GBaud	UI	320 – 100ppm	320	320 + 100ppm	ps	—

This table defines the receiver AC specifications for serial RapidIO. The AC timing specifications do not include RefClk jitter.

Table 77. Serial RapidIO Receiver AC Timing Specifications

At recommended operating conditions with XV_{DD} = 1.5 V or 1.8 V

Parameter	Symbol	Min	Typical	Max	Unit	Note
Deterministic jitter tolerance	J_D	0.37	—	—	UI p-p	1
Combined deterministic and random jitter tolerance	J_{DR}	0.55	—	—	UI p-p	1
Total jitter tolerance[2]	J_T	0.65	—	—	UI p-p	1
Bit error rate	BER	—	—	10^{-12}	—	—
Unit Interval: 2.5 GBaud	UI	400 – 100ppm	400	400 + 100ppm	ps	—
Unit Interval: 3.125 GBaud	UI	320 – 100ppm	320	320 + 100ppm	ps	—

Notes:
1. Measured at receiver
2. Total jitter is composed of three components: deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 44. The sinusoidal jitter component is included to ensure margin for low-frequency jitter, wander, noise, crosstalk, and other variable system effects.

This figure shows the single-frequency sinusoidal jitter limits.

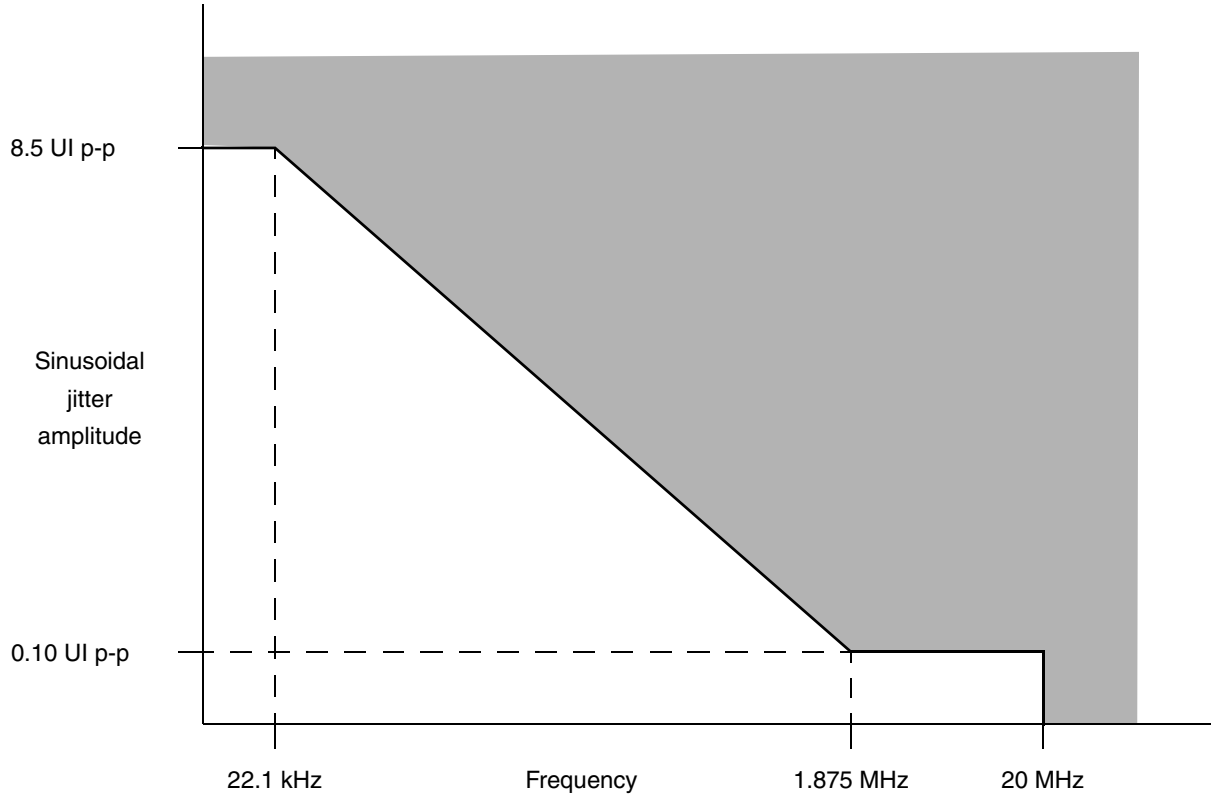


Figure 44. Single-Frequency Sinusoidal Jitter Limits

2.20.6 XAUI

This section describes the DC and AC electrical specifications for the XAUI bus.

2.20.6.1 XAUI DC Electrical Characteristics

This section discusses the XAUI DC electrical characteristics for the clocking signals, transmitter, and receiver.

2.20.6.1.1 DC Requirements for XAUI SD_REF_CLK*n* and SD_REF_CLKn_B

This section specifies XAUI DC level requirements for SD_REF_CLK*n* and SD_REF_CLK*n*_B, where *n* = [2–3]. Only SerDes banks 2–3 may be used for various SerDes XAUI configurations based on the RCW Configuration field SRDS_PRTCL. XAUI is not supported on SerDes bank 1.

For more information on these specifications, see Section 2.20.2, "SerDes Reference Clocks."

2.20.6.1.2 XAUI Transmitter DC Electrical Characteristics

This table defines the XAUI transmitter DC electrical characteristics.

Table 78. XAUI Transmitter DC Electrical Characteristics

At recommended operating conditions with XV_{DD} = 1.5 V or 1.8 V

Parameter	Symbol	Min	Typical	Max	Unit	Note
Output voltage	V_O	–0.40	—	2.30	V	1
Differential output voltage	V_{DIFFPP}	800	1000	1600	mV p-p	—

Note:
1. Absolute output voltage limit

2.20.6.1.3 XAUI Receiver DC Electrical Characteristics

This table defines the XAUI receiver DC electrical characteristics.

Table 79. XAUI Receiver DC Timing Specifications

At recommended operating conditions with XV_{DD} = 1.5 V or 1.8 V

Parameter	Symbol	Min	Typical	Max	Unit	Note
Differential input voltage	V_{IN}	200	900	1600	mV p-p	1

Note:
1. Measured at receiver

2.20.6.2 XAUI AC Timing Specifications

This section discusses the XAUI AC timing specifications for the clocking signals, transmitter, and receiver.

2.20.6.2.1 AC Requirements for XAUI SD_REF_CLK*n* and SD_REF_CLK*n*_B

The following table specifies AC requirements for SD_REF_CLK*n* and SD_REF_CLK*n*_B, where n = [2–3]. Only SerDes banks 2–3 may be used for various SerDes XAUI configurations based on the RCW Configuration field SRDS_PRTCL. XAUI is not supported on SerDes bank 1.

For more information on these specifications, see Section 2.20.2, "SerDes Reference Clocks."

Table 80. XAUI AC SD_REF_CLK3 and SD_REF_CLK3_B Input Clock Requirements

At recommended operating conditions with SV_{DD} = 1.0 V.

Parameter	Symbol	Min	Typ	Max	Unit	Note
SD_REF_CLK/SD_REF_CLK_B frequency range	t_{CLK_REF}	—	125 156.25	—	MHz	—
SD_REF_CLK/SD_REF_CLK_B clock frequency tolerance	t_{CLK_TOL}	–100	—	100	ppm	—
SD_REF_CLK/SD_REF_CLK_B reference clock duty cycle (measured at 1.6 V)	t_{CLK_DUTY}	40	50	60	%	—
SD_REF_CLK/SD_REF_CLK_B cycle to cycle jitter (period jitter at refClk input)	t_{CLK_CJ}	—	—	100	ps	—
SD_REF_CLK/SD_REF_CLK_B total reference clock jitter (peak-to-peak phase jitter at refClk input)	t_{CLK_PJ}	–50	—	50	ps	—
SD_REF_CLK/SD_REF_CLK_B rising/falling edge rate	t_{CLKRR}/t_{CLKFR}	1	—	4	V/ns	1
Differential input high voltage	V_{IH}	200	—	—	mV	2
Differential input low voltage	V_{IL}	—	—	–200	mV	2
Rising edge rate (SD_REF_CLK*n*) to falling edge rate (SD_REF_CLK*n*) matching	Rise-Fall Matching	—	—	20	%	3, 4

Notes:
1. Measured from –200 mV to +200 mV on the differential waveform (derived from SD_REF_CLK*n* minus SD_REF_CLK*n*_B). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See Figure 39.
2. Measurement taken from differential waveform
3. Measurement taken from single-ended waveform
4. Matching applies to rising edge for SD_REF_CLK*n* and falling edge rate for SD_REF_CLK*n*_B. It is measured using a 200 mV window centered on the median cross point where SD_REF_CLK*n* rising meets SD_REF_CLK*n*_B falling. The median cross point is used to calculate the voltage thresholds that the oscilloscope uses for the edge rate calculations. The rise edge rate of SD_REF_CLK*n* must be compared to the fall edge rate of SD_REF_CLK*n*_B, the maximum allowed difference must not exceed 20% of the slowest edge rate. See Figure 40.

2.20.6.2.2 XAUI Transmitter AC Timing Specifications

This table defines the XAUI transmitter AC timing specifications. RefClk jitter is not included.

Table 81. XAUI Transmitter AC Timing Specifications

At recommended operating conditions with XV_{DD} = 1.5 V or 1.8 V

Parameter	Symbol	Min	Typical	Max	Unit	Note
Deterministic jitter	J_D	—	—	0.17	UI p-p	—
Total jitter	J_T	—	—	0.35	UI p-p	—
Unit Interval: 3.125 GBaud	UI	320 – 100 ppm	320	320 + 100 ppm	ps	—

2.20.6.2.3 XAUI Receiver AC Timing Specifications

This table defines the receiver AC specifications for XAUI. RefClk jitter is not included.

Table 82. XAUI Receiver AC Timing Specifications

At recommended operating conditions with XV_{DD} = 1.5 V or 1.8 V

Parameter	Symbol	Min	Typical	Max	Unit	Note
Deterministic jitter tolerance	J_D	0.37	—	—	UI p-p	1
Combined deterministic and random jitter tolerance	J_{DR}	0.55	—	—	UI p-p	1
Total jitter tolerance[2]	J_T	0.65	—	—	UI p-p	1
Bit error rate	BER	—	—	10^{-12}	—	—
Unit Interval: 3.125 GBaud	UI	320 – 100 ppm	320	320 + 100 ppm	ps	—

Notes:
1. Measured at receiver
2. Total jitter is composed of three components: deterministic jitter, random jitter, and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 44. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk, and other variable system effects.

2.20.7 Aurora

This section describes the Aurora clocking requirements and AC and DC electrical characteristics.

2.20.7.1 Aurora Clocking Requirements for SD_REF_CLK*n* and SD_REF_CLK*n*_B

This section specifies Aurora DC requirements for SD_REF_CLK1 and SD_REF_CLK1_B. Only SerDes bank 1 may be used for SerDes Aurora configurations based on the RCW Configuration field SRDS_PRTCL. Aurora is not supported on SerDes banks 2–3.

For more information on these specifications, see Section 2.20.2, “SerDes Reference Clocks.”

2.20.7.2 Aurora DC Electrical Characteristics

This section describes the DC electrical characteristics for Aurora.

2.20.7.2.1 Aurora Transmitter DC Electrical Characteristics

This table defines the Aurora transmitter DC electrical characteristics.

:

Table 83. Aurora Transmitter DC Electrical Characteristics

At recommended operating conditions with XV_{DD} = 1.5 V or 1.8 V

Parameter	Symbol	Min	Typical	Max	Unit	Note
Differential output voltage	V_{DIFFPP}	800	1000	1600	mV p-p	—

2.20.7.2.2 Aurora Receiver DC Electrical Characteristics

This table defines the Aurora receiver DC electrical characteristics for Aurora.

Table 84. Aurora Receiver DC Electrical Characteristics

At recommended operating conditions with XV_{DD} = 1.5 V or 1.8 V

Parameter	Symbol	Min	Typical	Max	Unit	Note
Differential input voltage	V_{IN}	120	900	1200	mV p-p	1

Note:
1. Measured at receiver.

2.20.7.3 Aurora AC Timing Specifications

This section describes the AC timing specifications for Aurora.

2.20.7.3.1 Aurora Transmitter AC Timing Specifications

This table defines the Aurora transmitter AC timing specifications. RefClk jitter is not included.

Table 85. Aurora Transmitter AC Timing Specifications

At recommended operating conditions with XV_{DD} = 1.5 V or 1.8 V

Parameter	Symbol	Min	Typical	Max	Unit	Note
Deterministic jitter	J_D	—	—	0.17	UI p-p	—
Total jitter	J_T	—	—	0.35	UI p-p	—
Unit Interval: 2.5 GBaud	UI	400 – 100 ppm	400	400 + 100 ppm	ps	—
Unit Interval: 3.125 GBaud	UI	320 – 100 ppm	320	320 + 100 ppm	ps	—
Unit Interval: 5.0 GBaud	UI	200 – 100 ppm	200	200 + 100 ppm	ps	—

2.20.7.3.2 Aurora Receiver AC Timing Specifications

This table defines the Aurora receiver AC timing specifications. RefClk jitter is not included.

Table 86. Aurora Receiver AC Timing Specifications

At recommended operating conditions with XV_{DD} = 1.5 V or 1.8 V

Parameter	Symbol	Min	Typical	Max	Unit	Note
Deterministic jitter tolerance	J_D	0.37	—	—	UI p-p	1
Combined deterministic and random jitter tolerance	J_{DR}	0.55	—	—	UI p-p	1
Total jitter tolerance[2]	J_T	0.65	—	—	UI p-p	1
Bit error rate	BER	—	—	10^{-12}	—	—

Table 86. Aurora Receiver AC Timing Specifications (continued)

At recommended operating conditions with XV_{DD} = 1.5 V or 1.8 V

Parameter	Symbol	Min	Typical	Max	Unit	Note
Unit Interval: 2.5 GBaud	UI	400 – 100 ppm	400	400 + 100 ppm	ps	—
Unit Interval: 3.125 GBaud	UI	320 – 100 ppm	320	320 + 100 ppm	ps	—
Unit Interval: 5.0 GBaud	UI	200 – 100 ppm	200	200 + 100 ppm	ps	—

Note:

1. Measured at receiver
2. Total jitter is composed of three components: deterministic jitter, random jitter, and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 44. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

2.20.8 SGMII Interface

Each SGMII port features a 4-wire AC-coupled serial link from the SerDes interface of the chip, as shown in Figure 45, where C_{TX} is the external (on board) AC-coupled capacitor. Each output pin of the SerDes transmitter differential pair features 50-Ω output impedance. Each input of the SerDes receiver differential pair features 50-Ω on-die termination to XGND. The reference circuit of the SerDes transmitter and receiver is shown in Figure 41.

2.20.8.1 SGMII Clocking Requirements for SD_REF_CLK*n* and SD_REF_CLK*n*_B

When operating in SGMII mode, the EC_GTX_CLK125 clock is not required for this port. Instead, a SerDes reference clock is required on SD_REF_CLK*n* and SD_REF_CLK*n*_B pins. This section specifies SGMII requirements for SD_REF_CLK*n* and SD_REF_CLK*n*_B, where *n* = [1–3]. SerDes banks 1–3 may be used for SerDes SGMII configurations based on the RCW Configuration field SRDS_PRTCL.

For more information on these specifications, see Section 2.20.2, “SerDes Reference Clocks.”

2.20.8.2 SGMII DC Electrical Characteristics

This section discusses the electrical characteristics for the SGMII interface.

2.20.8.2.1 SGMII Transmit DC Timing Specifications

This table describe the SGMII SerDes transmitter and receiver AC-coupled DC electrical characteristics. Transmitter DC characteristics are measured at the transmitter outputs (SD_TX*n* and SD_TX*n*_B) as shown in Figure 46.

Table 87. SGMII DC Transmitter Electrical Characteristics

At recommended operating conditions with XV_{DD} = 1.5 V or 1.8 V

Parameter	Symbol	Min	Typ	Max	Unit	Note
Output high voltage	V_{OH}	—	—	1.5 x $\lvert V_{OD}\rvert_{-max}$	mV	1
Output low voltage	V_{OL}	$\lvert V_{OD}\rvert_{-min}/2$	—	—	mV	1

Table 87. SGMII DC Transmitter Electrical Characteristics (continued)

At recommended operating conditions with XV_{DD} = 1.5 V or 1.8 V

Parameter	Symbol	Min	Typ	Max	Unit	Note
Output differential voltage[2, 3, 4] $XV_{DD\text{-}Typ}$ at 1.5 V and 1.8 V)	$\lvert V_{OD}\rvert$	320	500.0	725.0	mV	B(1-3)TECR(lane)0[AMP_RED] =0b000000
		293.8	459.0	665.6		B(1-3)TECR(lane)0[AMP_RED] =0b000010
		266.9	417.0	604.7		B(1-3)TECR(lane)0[AMP_RED] =0b000101
		240.6	376.0	545.2		B(1-3)TECR(lane)0[AMP_RED] =0b001000
		213.1	333.0	482.9		B(1-3)TECR(lane)0[AMP_RED] =0b001100
		186.9	292.0	423.4		B(1-3)TECR(lane)0[AMP_RED] =0b001111
		160.0	250.0	362.5		B(1-3)TECR(lane)0[AMP_RED] =0b010011
Output impedance (single-ended)	R_O	40	50	60	Ω	—

Notes:
1. This does not align to DC-coupled SGMII.
2. $\lvert V_{OD}\rvert = \lvert V_{SD_TXn} - V_{SD_TXn_B}\rvert$. $\lvert V_{OD}\rvert$ is also referred to as output differential peak voltage. $V_{TX\text{-}DIFFp\text{-}p} = 2 \times \lvert V_{OD}\rvert$.
3. Example amplitude reduction setting for SGMII on SerDes bank 1 lane E: B1TECRE0[AMP_RED] = 0b000010 for an output differential voltage of 459 mV typical.
4. The $\lvert V_{OD}\rvert$ value shown in the Typ column is based on the condition of XVDD_SRDSn-Typ = 1.5 V or 1.8 V, no common mode offset variation. SerDes transmitter is terminated with 100-Ω differential load between SD_TX*n* and SD_TX*n*_B.

This figure shows an example of a 4-wire AC-coupled SGMII serial link connection.

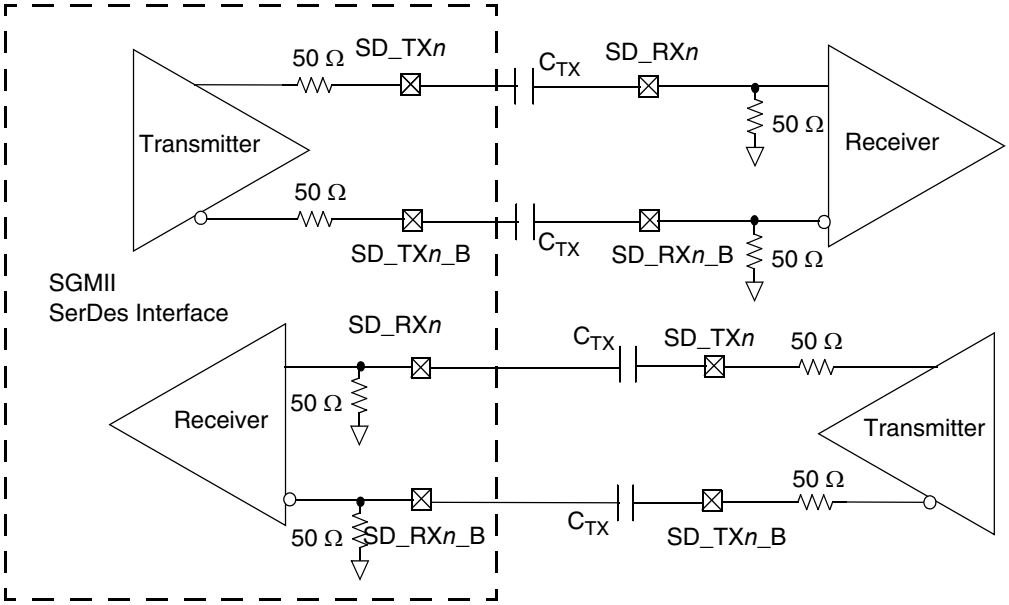


Figure 45. 4-Wire AC-Coupled SGMII Serial Link Connection Example

This figure shows the SGMII transmitter DC measurement circuit.

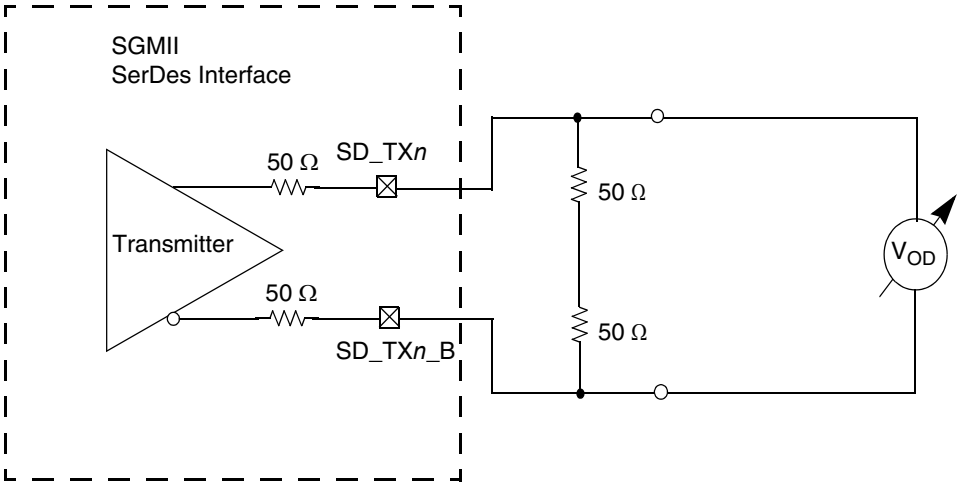


Figure 46. SGMII Transmitter DC Measurement Circuit

2.20.8.2.2 SGMII DC Receiver Electrical Characteristics

This table lists the SGMII DC receiver electrical characteristics. Source synchronous clocking is not supported. Clock is recovered from the data.

Table 88. SGMII DC Receiver Electrical Characteristics

At recommended operating conditions with XV_{DD} = 1.5 V or 1.8 V

Parameter		Symbol	Min	Typ	Max	Unit	Note
DC Input voltage range		—	N/A			—	1
Input differential voltage	REIDL_CTL = 001xx	$V_{RX_DIFFp-p}$	100	—	1200	mV	2, 4
	REIDL_CTL = 100xx		175	—			
Loss of signal threshold	REIDL_CTL = 001xx	V_{LOS}	30	—	100	mV	3, 4
	REIDL_CTL = 100xx		65	—	175		
Receiver differential input impedance		Z_{RX_DIFF}	80	—	120	Ω	—

Notes:
1. Input must be externally AC coupled.
2. $V_{RX_DIFFp-p}$ is also referred to as peak-to-peak input differential voltage.
3. The concept of this parameter is equivalent to the electrical idle detect threshold parameter in PCI Express. See to Section 2.20.4.4, "PCI Express DC Physical Layer Receiver Specifications," and Section 2.20.4.5.2, "PCI Express AC Physical Layer Receiver Specifications," for further explanation.
4. The REIDL_CTL shown in the table refers to the chip's SerDes control register B(1–3)GCR(lane)1[REIDL_CTL] bit field.

2.20.8.3 SGMII AC Timing Specifications

This section discusses the AC timing specifications for the SGMII interface.

2.20.8.3.1 SGMII Transmit AC Timing Specifications

This table provides the SGMII transmit AC timing specifications. A source synchronous clock is not supported. The AC timing specifications do not include RefClk jitter.

Table 89. SGMII Transmit AC Timing Specifications

At recommended operating conditions with XV_{DD} = 1.5 V or 1.8 V

Parameter	Symbol	Min	Typ	Max	Unit	Note
Deterministic jitter	JD	—	—	0.17	UI p-p	—
Total jitter	JT	—	—	0.35	UI p-p	2
Unit Interval	UI	799.92	800	800.08	ps	1
AC coupling capacitor	C_{TX}	10	—	200	nF	3

Notes:
1. Each UI is 800 ps ± 100 ppm.
2. See Figure 48 for single frequency sinusoidal jitter limits.
3. The external AC coupling capacitor is required. It is recommended that it be placed near the device transmitter outputs.

2.20.8.3.2 SGMII AC Measurement details

Transmitter and receiver AC characteristics are measured at the transmitter outputs (SD_TX*n* and SD_TX*n*_B) or at the receiver inputs (SD_RX*n* and SD_RX*n*_B) respectively, as depicted in the following figure.

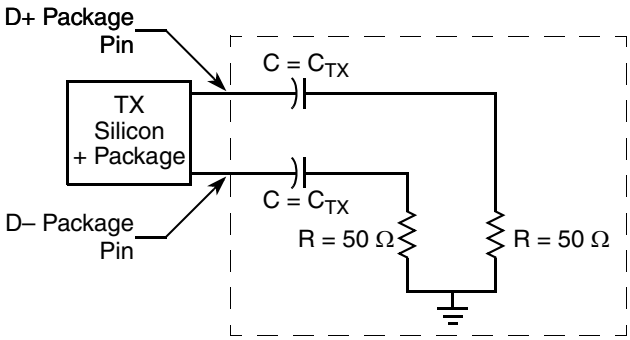


Figure 47. SGMII AC Test/Measurement Load

2.20.8.3.3 SGMII Receiver AC Timing Specifications

This table provides the SGMII receiver AC timing specifications. The AC timing specifications do not include RefClk jitter. Source synchronous clocking is not supported. Clock is recovered from the data.

Table 90. SGMII Receiver AC Timing Specifications

At recommended operating conditions with XV_{DD} = 1.5 V or 1.8 V

Parameter	Symbol	Min	Typ	Max	Unit	Note
Deterministic jitter tolerance	JD	0.37	—	—	UI p-p	1, 2
Combined deterministic and random jitter tolerance	JDR	0.55	—	—	UI p-p	1, 2
Total jitter tolerance	JT	0.65	—	—	UI p-p	1, 2
Bit error ratio	BER	—	—	10^{-12}	—	—
Unit Interval	UI	799.92	800.00	800.08	ps	3

Notes:

1. Measured at receiver
2. See the RapidIO 1×/4× LP Serial Physical Layer Specification for interpretation of jitter specifications.
3. Each UI is 800 ps ± 100 ppm.

The sinusoidal jitter in the total jitter tolerance may have any amplitude and frequency in the unshaded region of the following figure.

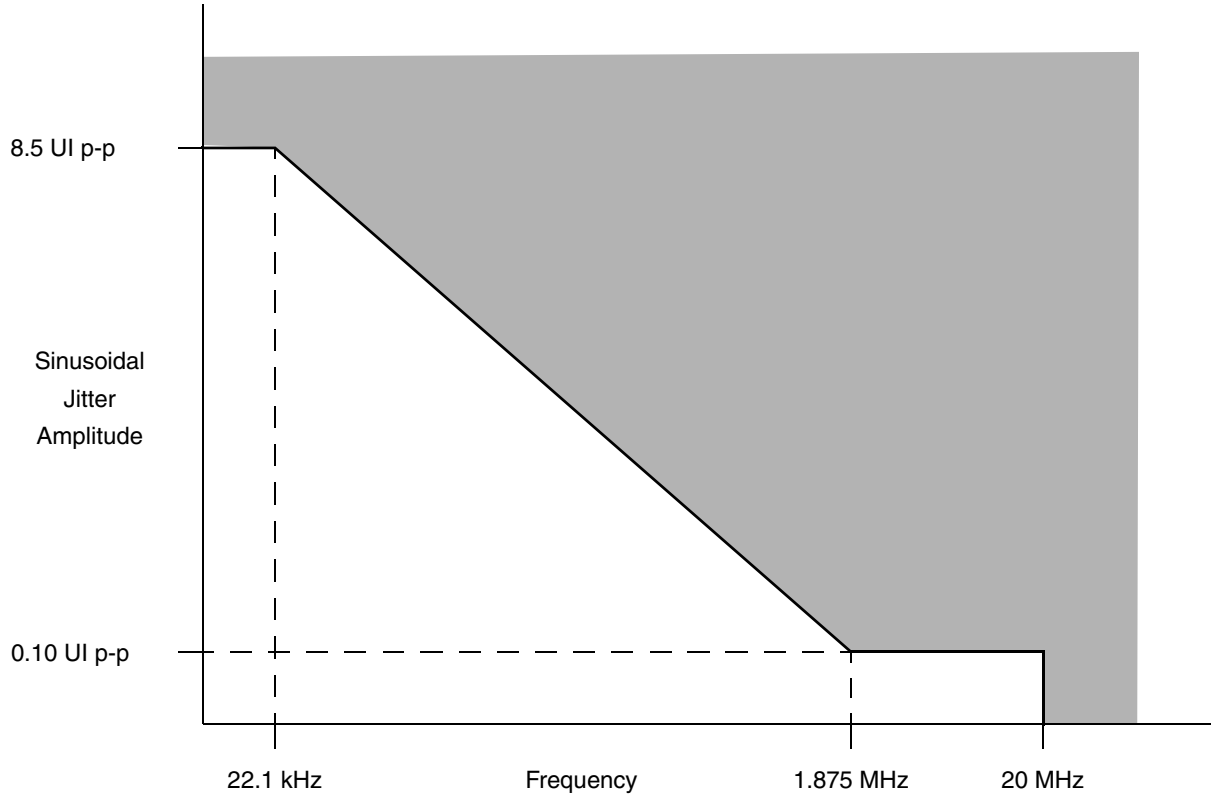


Figure 48. Single Frequency Sinusoidal Jitter Limits

3 Hardware Design Considerations

3.1 System Clocking

This section describes the PLL configuration of the chip.

This chip includes 9 PLLs, as follows:

- There are 4 selectable core cluster PLLs which generate a core clock from the externally supplied SYSCLK input. Core complex 0–3 can select from CC1 PLL, CC2 PLL or CC3 PLL. Core complex 4–7 can select from CC3 PLL, CC4 PLL or CC1 PLL. The frequency ratio between each of the 4 core cluster PLLs and SYSCLK is selected using the configuration bits as described in Section 3.1.3, "e500-mc Core Cluster to SYSCLK PLL Ratio." The frequency for each core complex 0–7 is selected using the configuration bits as described in Table 95 and Table 96.
- The platform PLL generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in Section 3.1.2, "Platform to SYSCLK PLL Ratio."
- The DDR block PLL generates the DDR clock from the externally supplied SYSCLK input (asynchronous mode) or from the platform clock (synchronous mode). The frequency ratio is selected using the Memory Controller Complex PLL multiplier/ratio configuration bits as described in Section 3.1.5, "DDR Controller PLL Ratios."
- Each of the three SerDes blocks has a PLL which generate a core clock from their respective externally supplied SD_REF_CLK*n*/SD_REF_CLK*n*_B inputs. The frequency ratio is selected using the SerDes PLL ratio configuration bits as described in Section 3.1.6, "SerDes PLL Ratio."

3.1.1 Clock Ranges

This table provides the clocking specifications for the processor core, platform, memory, and local bus.

Table 91. P4080 Processor Clocking Specifications

Characteristic	Maximum Processor Core Frequency						Unit	Note
	1200 MHz		1333 MHz		1500 MHz			
	Min	Max	Min	Max	Min	Max		
e500-mc core PLL frequency	800	1200	800	1333	800	1500	MHz	1, 4
e500-mc core frequency (core PLL/2)	400	600	400	667	400	750	MHz	4
Platform clock frequency	600	600	600	667	600	800	MHz	1
Memory bus clock frequency	333	600	333	667	333	667	MHz	1, 2, 5, 6, 7, 8
Local bus clock frequency	—	75	—	83.3	—	100	MHz	3
PME and FM*n*	300	450	300	542	300	600	MHz	9

Notes:

1. **Caution:** The platform clock to SYSCLK ratio and e500-mc core to SYSCLK ratio settings must be chosen such that the resulting SYSCLK frequency, e500-mc (core) frequency, and platform clock frequency do not exceed their respective maximum or minimum operating frequencies.
2. The memory bus clock speed is half the DDR2/DDR3 data rate. DDR2 memory bus clock frequency is limited to max = 400 MHz. DDR3 memory bus clock frequency is limited to min = 400 MHz.
3. The local bus clock speed on LCLK[0:1] is determined by the platform clock divided by the local bus ratio programmed in LCRR[CLKDIV]. For more information, see *P4080 QorIQ Integrated Multicore Communication Processor Family Reference Manual*.
4. The e500-mc core can run at e500-mc core complex PLL/1 or PLL/2. With a minimum core complex PLL frequency of 800 MHz, this results in a minimum allowable e500-mc core frequency of 400 MHz for PLL/2.
5. In synchronous mode, the memory bus clock speed is half the platform clock frequency. In other words, the DDR data rate is the same as the platform frequency. If the desired DDR data rate is higher than the platform frequency, asynchronous mode must be used.
6. In asynchronous mode, the memory bus clock speed is dictated by its own PLL.
7. DDR data rate frequency must be ≤ 2× platform frequency.
8. For Maximum Processor Core Frequency = 1500 MHz, due to clock ratio combinations, Memory bus clock frequency maximum = 650 MHz.
9. For the FMan: 300 MHz is the minimum to support 1 G. 450 MHz is the minimum to support 10 G. 500 MHz is the minimum to support 10 G with PCD. 600 MHz is the minimum to support 12 G (10 G + 2*1 G) with PCD.

This table provides the clocking specifications for the P4081 processor core, platform, memory, and local bus.

Table 92. P4081 Processor Clocking Specifications

Characteristic	Maximum Processor Core Frequency				Unit	Note
	1000 MHz		1200 MHz			
	Min	Max	Min	Max		
e500-mc core PLL frequency	800	1000	800	1200	MHz	1, 4
e500-mc core frequency (core PLL/2)	400	500	400	600	MHz	4
Platform clock frequency	533	600	600	600	MHz	1

Table 92. P4081 Processor Clocking Specifications (continued)

Characteristic	Maximum Processor Core Frequency				Unit	Note
	1000 MHz		1200 MHz			
	Min	Max	Min	Max		
Memory bus clock frequency	333	600	333	600	MHz	1, 2, 5, 6, 7, 8
Local bus clock frequency	—	75	—	75	MHz	3
PME and FM*n*	300	467	300	450	MHz	9

Notes:

1. **Caution:** The platform clock to SYSCLK ratio and e500-mc core to SYSCLK ratio settings must be chosen such that the resulting SYSCLK frequency, e500-mc (core) frequency, and platform clock frequency do not exceed their respective maximum or minimum operating frequencies.
2. The memory bus clock speed is half the DDR2/DDR3 data rate. DDR2 memory bus clock frequency is limited to max = 400 MHz. DDR3 memory bus clock frequency is limited to min = 400 MHz.
3. The local bus clock speed on LCLK[0:1] is determined by the platform clock divided by the local bus ratio programmed in LCRR[CLKDIV]. For more information, see *P4080 QorIQ Integrated Multicore Communication Processor Family Reference Manual*.
4. The e500-mc core can run at e500-mc core complex PLL/1 or PLL/2. With a minimum core complex PLL frequency of 800 MHz, this results in a minimum allowable e500-mc core frequency of 400 MHz for PLL/2.
5. In synchronous mode, the memory bus clock speed is half the platform clock frequency. In other words, the DDR data rate is the same as the platform frequency. If the desired DDR data rate is higher than the platform frequency, asynchronous mode must be used.
6. In asynchronous mode, the memory bus clock speed is dictated by its own PLL.
7. DDR data rate frequency must be ≤ 2× platform frequency.
8. For Maximum Processor Core Frequency = 1500 MHz, due to clock ratio combinations, Memory bus clock frequency maximum = 650 MHz.
9. For the FMan: 300 MHz is the minimum to support 1 G. 450 MHz is the minimum to support 10 G. 500 MHz is the minimum to support 10 G with PCD. 600 MHz is the minimum to support 12 G (10 G + 2*1 G) with PCD.

3.1.2 Platform to SYSCLK PLL Ratio

The allowed platform clock to SYSCLK ratios are shown in Table 93.

Note that in synchronous DDR mode, the DDR data rate is the determining factor for selecting the platform bus frequency because the platform frequency must equal the DDR data rate.

In asynchronous DDR mode, the memory bus clock frequency is decoupled from the platform bus frequency. The platform frequency must be greater than or equal to ½ the DDR data rate.

For platform clock frequency targeting 667 MHz and above, set the RCW Configuration field SYS_PLL_CFG = 0b00. For 533–666-MHz frequencies, set SYS_PLL_CFG = 0b01.

Table 93. Platform to SYSCLK PLL Ratios

Binary Value of SYS_PLL_RAT	Platform:SYSCLK Ratio
0_0101	5:1
0_0110	6:1
0_0111	7:1
0_1000	8:1
0_1001	9:1
0_1010	10:1
0_1011	11:1
0_1100	12:1
All Others	Reserved

3.1.3 e500-mc Core Cluster to SYSCLK PLL Ratio

The clock ratio between SYSCLK and each of the 4 core cluster PLLs is determined by the binary value of the RCW Configuration field CCn_PLL_RAT. Table 94 describes the supported ratios. Note that for core cluster PLL frequency targeting 1 GHz and above must set RCW Configuration field CCn_PLL_CFG = b’00, for frequency targeting below 1 GHz set CCn_PLL_CFG = b’01.

This table lists the supported Core Cluster to SYSCLK ratios.

Table 94. e500-mc Core Cluster PLL to SYSCLK Ratios

Binary Value of CCn_PLL_RAT	Core Cluster:SYSCLK Ratio
0_1000	8:1
0_1001	9:1
0_1010	10:1
0_1011	11:1
0_1100	12:1
0_1110	14:1
0_1111	15:1
1_0000	16:1
All Others	Reserved

3.1.4 e500-mc Core Complex PLL Select

The clock frequency of each e500-mc core complex is determined by the binary value of the RCW Configuration field CCn_PLL_SEL. Table 95 and Table 96 describe the supported ratios for each core complex, where each individual core complex can select a frequency from their respective tables.

Note, for Table 95, if CC3 PLL is ever used by any core 0–3, its maximum allowed frequency is 80% of the maximum rated frequency of the core at nominal voltage.

Note, for Table 96, if CC1 PLL is ever used by any core 4–7, its maximum allowed frequency is 80% of the maximum rated frequency of the core at nominal voltage.

Table 95. e500-mc Core Complex [0–3] PLL Select

Binary Value of Cn_PLL_SEL for *n* = 0–3	e500-mc:Core Cluster Ratio
0000	CC1 PLL /1
0001	CC1 PLL /2
0100	CC2 PLL /1
0101	CC2 PLL /2
1000	CC3 PLL /1
All Others	Reserved

Table 96. e500-mc Core Complex [4–7] PLL Select

Binary Value of Cn_PLL_SEL for *n* = 4–7	e500-mc:Core Cluster Ratio
0000	CC1 PLL /1
1000	CC3 PLL /1
1001	CC3 PLL /2
1100	CC4 PLL /1
1101	CC4 PLL /2
All Others	Reserved

3.1.5 DDR Controller PLL Ratios

The dual DDR memory controller complexes can be synchronous with or asynchronous to the platform, depending on configuration. Both of the chip's DDR controllers operate at the same frequency configuration.

Table 97 describes the clock ratio between the DDR memory controller PLLs and the externally supplied SYSCLK input (asynchronous mode) or from the platform clock (synchronous mode).

In asynchronous DDR mode, the DDR data rate to SYSCLK ratios supported are listed in Table 97. In synchronous mode, the DDR data rate to platform clock ratios supported are listed in Table 98. This ratio is determined by the binary value of the RCW Configuration field MEM_PLL_RAT (bits 10–14).

The RCW Configuration field MEM_PLL_CFG (bits 8–9) must be set to MEM_PLL_CFG = 0b01 if the applied DDR PLL reference clock frequency is greater than the cutoff frequency listed in Table 97 and Table 98 for asynchronous and synchronous DDR clock ratios respectively, else set MEM_PLL_CFG = 0b00.

NOTE

The RCW Configuration field DDR_SYNC (bit 184) must be set to 0b0 for asynchronous mode and 0b1 for synchronous mode.

The RCW Configuration field DDR_RATE (bit 232) must be set to 0b0 for asynchronous mode and 0b1 for synchronous mode.

The RCW Configuration field DDR_RSV0 (bit 234) must be set to 0b0 for all ratios.

In asynchronous DDR mode, the DDR data rate to SYSCLK ratios supported are listed in this table.

Table 97. Asynchronous DDR Clock Ratio

Binary Value of MEM_PLL_RAT[2]	DDR Data Rate:SYSCLK Ratio	Set MEM_PLL_CFG = 01 for SYSCLK Freq[1] (Rev 2.0 Silicon)
0_0101	5:1	> 96.7 MHz
0_0110	6:1	≥ 83.3 MHz
0_1000	8:1	> 120.9 MHz
0_1001	9:1	> 107.4 MHz
0_1010	10:1	> 96.7 MHz
0_1100	12:1	≥ 83.3 MHz
0_1101	13:1	≥ 83.3 MHz
1_0000	16:1	≥ 83.3 MHz
All Others	Reserved	—

Notes:
1. Set RCW field MEM_PLL_CFG = 0b01 if the applied DDR PLL reference clock (SYSCLK) frequency is greater than given cutoff, else set to 0b00 for frequency that is less than or equal to cutoff.
2. DDR data rate frequency must be ≤ 2× platform frequency. Platform frequency must be ≥ ½ DDR data rate.

In synchronous mode, the DDR data rate to platform clock ratios supported are listed in this table.

Table 98. Synchronous DDR Clock Ratio

Binary Value of MEM_PLL_RAT	DDR Data Rate:Platform CLK Ratio	Set MEM_PLL_CFG = 01 for Platform CLK Freq[1]
0_0001	1:1	>600 MHz
All Others	Reserved	—

Notes:
1. Set MEM_PLL_CFG=0b01 if the applied DDR PLL reference clock (Platform clock) frequency is greater than given cutoff, else set to 0b00 for frequency that is less than or equal to cutoff.

3.1.6 SerDes PLL Ratio

The clock ratio between each of the three SerDes PLLs and their respective externally supplied SD_REF_CLK*n*/SD_REF_CLK*n*_B inputs is determined by the binary value of the RCW Configuration field SRDS_RATIO*n*_B as shown in Table 99. Furthermore, each SerDes lane grouping can be run at a SerDes PLL frequency divider determined by the binary value of the RCW Configuration field SRDS_DIV*n*_B as shown in Table 100 and Table 101.

This table lists the supported SerDes PLL Bank *n* to SD_REF_CLK*n* ratios.

Table 99. SerDes PLL Bank *n* to SD_REF_CLK*n* Ratios

Binary Value of SRDS_RATIO*n*_B	SRDS_PLL_*n*:SD_REF_CLK*n* Ratio	NOTE
000	10:1	—
001	20:1	—
010	25:1	—
011	40:1	1
100	50:1	1
All Others	Reserved	Reserved

Notes:
1. SerDes bank 1only.

This table lists the supported SerDes PLL dividers. Table 100 shows the PLL divider support for each pair of lanes on SerDes Bank 1. This table shows the PLL dividers supported for each 4 lane group for SerDes Banks 2 and 3.

Table 100. SerDes Bank 1 PLL Dividers

Binary Value of SRDS_DIV1_B[0:4]	SerDes Bank 1 PLL Divider
0b0	Divide by 1 off Bank 1 PLL
0b1	Divide by 2 off Bank 1 PLL

Notes:
1. One bit (of 5 total SRDS_DIV1_B bits) controls each pair of lanes. Where first bit controls config of lanes A/B (or 0/1) and last bit controls config of lanes I/J (or 8/9).

Table 101. SerDes Banks 2 and 3 PLL Dividers

Binary Value of SRDS_DIV*n*_B	SerDes Bank *n* PLL Divider
0b0	Divide by 1 off Bank *n* PLL
0b1	Divide by 2 off Bank *n* PLL

Notes:
1. One bit controls all 4 lanes of each bank.
2. n = 2 or 3 (SerDes bank 2 or bank 3)

3.1.7 Frame Manager (FM*n*) Clock Select

The frame managers, FM1 and FM2, can each be synchronous with or asynchronous to the platform, depending on configuration.

This table describes the clocking options that may be applied to each FM. The clock selection is determined by the binary value of the RCW Clocking Configuration fields FM1_CLK_SEL and FM2_CLK_SEL.

Table 102. Frame Manager (FM*n*) Clock Select

Binary Value of FM*n*_CLK_SEL	FM*n* Frequency
0b0	Platform Clock Frequency /2
0b1	Core Cluster 3 Frequency /2 [1]

Notes:

1. For asynchronous mode, max frequency see Table 91.

3.1.8 Pattern Matching Engine (PME) Clock Select

The PME can be synchronous with or asynchronous to the platform, depending on configuration.

This table describes the clocking options that may be applied to the PME. The clock selection is determined by the binary value of the RCW Clocking Configuration field PME_CLK_SEL.

Table 103. Pattern Matching Engine Clock Select

Binary Value of PME_CLK_SEL	PME Frequency
0b0	Platform Clock Frequency /2
0b1	Core Cluster 3 Frequency /2 [1]

Notes:

1. For asynchronous mode, max frequency see Table 91.

3.1.9 Frequency Options

This section discusses interface frequency options.

3.1.9.1 SYSCLK and Platform Frequency Options

This table shows the expected frequency options for SYCLK and platform frequencies.

Table 104. SYSCLK and Platform Frequency Options

Platform: SYSCLK Ratio	SYSCLK (MHz)			
	83.33	100.00	111.11	133.33
	Platform Frequency (MHz)[1]			
5:1				666
6:1		600	666	799
7:1		700	777	
8:1	666	800		
9:1	749			

Table 104. SYSCLK and Platform Frequency Options (continued)

10:1				
11:1				
12:1				

Notes:

1. Platform frequency values are shown rounded down to the nearest whole number (decimal place accuracy removed)

3.1.9.2 Minimum Platform Frequency Requirements for High-Speed Interfaces

The platform clock frequency must be considered for proper operation of high-speed interfaces as described below.

Note per Table 91, the minimum platform frequency supported on the chip always meets the minimum platform frequency requirements for high-speed interfaces given in the formulas below.

For proper PCI Express operation, the platform clock frequency must be greater than or equal to:

$$\frac{527\text{ MHz x (PCI Express link width)}}{8}$$

Figure 49. Gen 1 PEX Minimum Platform Frequency

$$\frac{527\text{ MHz x (PCI Express link width)}}{4}$$

Figure 50. Gen 2 PEX Minimum Platform Frequency

See the “Link Width” section of the *P4080 QorIQ Integrated Multicore Communication Processor Family Reference Manual* for PCI Express interface width details. Note that “PCI Express link width” in the above equation refers to the negotiated link width as the result of PCI Express link training, which may or may not be the same as the link width POR selection.

For proper serial RapidIO operation, the platform clock frequency must be greater than or equal to:

$$\frac{2 \times (0.8512) \times \text{(serial RapidIO interface frequency)} \times \text{(serial RapidIO link width)}}{64}$$

Figure 51. Serial RapidIO Minimum Platform Frequency

See the “1x/4x LP-Serial Signal Descriptions” section of the *P4080 QorIQ Integrated Multicore Communication Processor Family Reference Manual* for serial RapidIO interface width and frequency details.

3.2 Supply Power Setting

This chip is capable of supporting multiple power supply levels on its I/O supplies. The I/O voltage select inputs, shown in the following table, properly configure the receivers and drivers of the I/Os associated with the BVDD, CVDD, and LVDD power planes, respectively.

WARNING

Incorrect voltage select settings can lead to irreversible device damage.

Table 105. I/O Voltage Selection

Signals	Value (Binary)	VDD Voltage Selection		
		BVDD	CVDD	LVDD
IO_VSEL[0:4]	0_0000	3.3 V	3.3 V	3.3 V
	0_0001	3.3 V	3.3 V	2.5 V
	0_0010	3.3 V	3.3 V	1.8 V
	0_0011	3.3 V	2.5 V	3.3 V
	0_0100	3.3 V	2.5 V	2.5 V
	0_0101	3.3 V	2.5 V	1.8 V
	0_0110	3.3 V	1.8 V	3.3 V
	0_0111	3.3 V	1.8 V	2.5 V
	0_1000	3.3 V	1.8 V	1.8 V
	0_1001	2.5 V	3.3 V	3.3 V
	0_1010	2.5 V	3.3 V	2.5 V
	0_1011	2.5 V	3.3 V	1.8 V
	0_1100	2.5 V	2.5 V	3.3 V
	0_1101	2.5 V	2.5 V	2.5 V
	0_1110	2.5 V	2.5 V	1.8 V
	0_1111	2.5 V	1.8 V	3.3 V
	1_0000	2.5 V	1.8 V	2.5 V
	1_0001	2.5 V	1.8 V	1.8 V
	1_0010	1.8 V	3.3 V	3.3 V
	1_0011	1.8 V	3.3 V	2.5 V
	1_0100	1.8 V	3.3 V	1.8 V
	1_0101	1.8 V	2.5 V	3.3 V
	1_0110	1.8 V	2.5 V	2.5 V
	1_0111	1.8 V	2.5 V	1.8 V
	1_1000	1.8 V	1.8 V	3.3 V
	1_1001	1.8 V	1.8 V	2.5 V
	1_1010	1.8 V	1.8 V	1.8 V
	1_1011	3.3 V	3.3 V	3.3 V
	1_1100	3.3 V	3.3 V	3.3 V
	1_1101	3.3 V	3.3 V	3.3 V
	1_1110	3.3 V	3.3 V	3.3 V
	1_1111	3.3 V	3.3 V	3.3 V

3.3 Power Supply Design

3.3.1 PLL Power Supply Filtering

Each of the PLLs described in Section 3.1, "System Clocking," is provided with power through independent power supply pins (AV_{DD_PLAT}, AV_{DD_CCn}, AV_{DD_DDR}, and AV_{DD_SRDSn}). AV_{DD_PLAT}, A_{VDD_CCn}, and AV_{DD_DDR} voltages must be derived directly from the V_{DD_PL} source through a low frequency filter scheme. AV_{DD_SRDSn} voltages must be derived directly from the SV_{DD} source through a low frequency filter scheme.

The recommended solution for PLL filtering is to provide independent filter circuits per PLL power supply, as illustrated in Figure 52, one for each of the AV_{DD} pins. By providing independent filters to each PLL, the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLL's resonant frequency range from a 500-kHz to 10-MHz range.

Each circuit must be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It must be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of the footprint, without the inductance of vias.

The following figure shows the PLL power supply filter circuit.

Where:

R = 5 Ω ± 5%

C1 = 10 µF ± 10%, 0603, X5R, with ESL ≤ 0.5 nH

C2 = 1.0 µF ± 10%, 0402, X5R, with ESL ≤ 0.5 nH

NOTE

A higher capacitance value for C2 may be used to improve the filter as long as the other C2 parameters do not change (0402 body, X5R, ESL ≤ 0.5 nH).

Voltage for AV_{DD} is defined at the input of the PLL supply filter and not the pin of AV_{DD}.

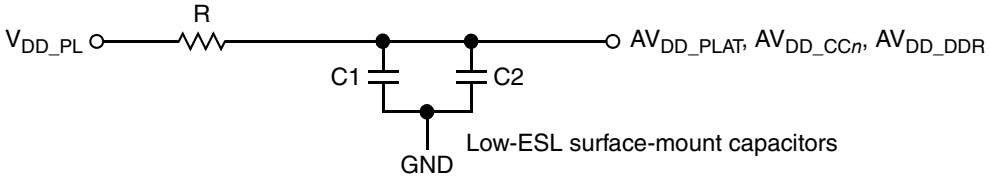


Figure 52. PLL Power Supply Filter Circuit

The AV_{DD_SRDS} signals provides power for the analog portions of the SerDes PLL. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit similar to the one shown in following the following figure. For maximum effectiveness, the filter circuit is placed as closely as possible to the AV_{DD_SRDSn} balls to ensure it filters out as much noise as possible. The ground connection must be near the AV_{DD_SRDSn} balls. The 0.003-µF capacitor is closest to the balls, followed by two 2.2-µF capacitors, and finally the 1-Ω resistor to the board supply plane. The capacitors are connected from AV_{DD_SRDSn} to the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces must be kept short, wide, and direct.

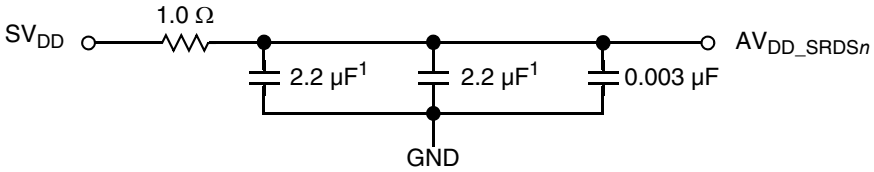


Figure 53. SerDes PLL Power Supply Filter Circuit

Note the following:

- AV_{DD_SRDSn} must be a filtered version of SV_{DD}.
- Signals on the SerDes interface are fed from the XV_{DD} and SV_{DD} power plane.
- Voltage for AV_{DD_SRDSn} is defined at the PLL supply filter and not the pin of AV_{DD_SRDSn}.
- An 0805 sized capacitor is recommended for system initial bring-up.

3.3.2 XV_{DD} Power Supply Filtering

XV_{DD} may be supplied by a linear regulator or sourced by a filtered GV_{DD}. Systems may design in both options to allow flexibility to address system noise dependencies.

An example solution for XV_{DD} filtering, where XV_{DD} is sourced from GV_{DD}, is illustrated in the following figure. The component values in this example filter are system dependent and are still under characterization, component values may need adjustment based on the system or environment noise.

Where:

C1 = 2.2 µF ± 10%, X5R, with ESL ≤ 0.5 nH
C2 = 2.2 µF ± 10%, X5R, with ESL ≤ 0.5 nH
F1 = 120 Ω at 100-MHz 2A 25% 0603 Ferrite
F2 = 120 Ω at 100-MHz 2A 25% 0603 Ferrite

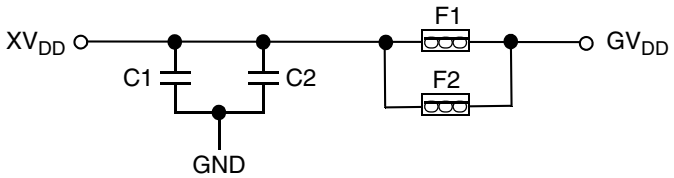


Figure 54. XV_{DD} Power Supply Filter Circuit

3.4 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the chip's system, and the device itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD}, BV_{DD}, OV_{DD}, CV_{DD}, GV_{DD}, and LV_{DD} pin of the device. These decoupling capacitors must receive their power from separate V_{DD}, BV_{DD}, OV_{DD}, CV_{DD}, GV_{DD}, LV_{DD}, and GND power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors must have a value of 0.01 or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors must be used to minimize lead inductance, preferably 0402 or 0603 sizes.

Additionally, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD}, BV_{DD}, OV_{DD}, CV_{DD}, GV_{DD}, and LV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors must have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They must also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 µF (AVX TPS tantalum or Sanyo OSCON).

3.5 SerDes Block Power Supply Decoupling Recommendations

The SerDes block requires a clean, tightly regulated source of power (SV_{DD} and XV_{DD}) to ensure low jitter on transmit and reliable recovery of data in the receiver. An appropriate decoupling scheme is outlined below.

Only SMT capacitors must be used to minimize inductance. Connections from all capacitors to power and ground must be done with multiple vias to further reduce inductance.

- First, the board must have at least 10 × 10-nF SMT ceramic chip capacitors as close as possible to the supply balls of the device. Where the board has blind vias, these capacitors must be placed directly below the chip supply and ground connections. Where the board does not have blind vias, these capacitors must be placed in a ring around the device as close to the supply and ground connections as possible.
- Second, there must be a 1-µF ceramic chip capacitor on each side of the device. This must be done for all SerDes supplies.
- Third, between the device and any SerDes voltage regulator there must be a 10-µF, low ESR SMT tantalum chip capacitor and a 100-µF, low ESR SMT tantalum chip capacitor. This must be done for all SerDes supplies.

3.6 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. All unused active low inputs must be tied to $V_{DD,}$ BV_{DD}, CV_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} as required. All unused active high inputs must be connected to GND. All NC (no-connect) signals must remain unconnected. Power and ground connections must be made to all external V_{DD}, BV_{DD}, CV_{DD}, OV_{DD}, GV_{DD}, $LV_{DD,}$ and GND pins of the device.

The Ethernet controllers 1 and/or 2 input pins may be disabled by setting their respective RCW Configuration field EC1 (bits 360-361) to 0b11, and EC2 (bits 363–365) to 0b111 = No parallel mode Ethernet, no USB. When disabled, these inputs do not need to be externally pulled to an appropriate signal level.

EC_GTX_CLK125 is a 125-MHz input clock shared among all dTSEC ports. If the dTSEC ports are not used for RGMII, the EC_GTX_CLK125 input can be tied off to GND.

- If RCW field DMA1 = 0b1 (RCW bit 384), the DMA1 external interface is not enabled and the DMA1_DDONE0_B pin must be left as a no connect.
- If RCW field I2C3 = 0b11 (RCW bits 369–370) is selected, the SDHC_WP and SDHC_CD_B input signals are enabled for external use. If SDHC_WP and SDHC_CD_B are selected an not used, they must be externally pulled low such that SDHC_WP = 0 = write enabled and SDHC_CD_B = 0 = card detected. If RCW field I2C3 != 0b11, thereby selecting either I2C3 or GPIO functionality, SDHC_WP and SDHC_CD_B are internally driven such that SDHC_WP = write enabled and SDHC_CD_B = card detected and the selected I2C3 or GPIO external pin functionality maybe used.

This chip may be run with cores 4–7 disabled by connecting $\overline{\text{TEST_SEL}}$ to GND. In this mode, it is recommended that the associated power plane, V_{DD_CB}, be tied to the GND plane as well to save static power. Note that with $\overline{\text{TEST_SEL}}$ = 0, SVR = 8201_0010h for 4 core P4080/P4081 without security and SVR = 8209_0010h for 4 core P4080/P4081E with security.

The TMP_DETECT_B pin is an active low input to the Security Monitor (reference the *Secure Boot and Trust Architecture* chapter of the *P4080 QorIQ Integrated Multicore Communication Processor Family Reference Manual*). When using Trust Architecture functionality, external logic must ramp TMP_DETECT_B with OV_{DD}. If not using Trust Architecture functionality, TMP_DETECT_B must be tied to OV_{DD} to prevent the input from going low.

3.6.1 Legacy JTAG Configuration Signals

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 56. Care must be taken to ensure that these pins are maintained at a valid negated state under normal operating conditions as most have asynchronous behavior and spurious assertion gives unpredictable results.

Boundary-scan testing is enabled through the JTAG interface signals. The TRST_B signal is optional in the IEEE Std 1149.1 specification, but it is provided on all processors built on Power Architecture technology. The device requires TRST_B to be asserted during power-on reset flow to ensure that the JTAG boundary logic does not interfere with normal chip operation. While the TAP controller can be forced to the reset state using only the TCK and TMS signals, generally systems assert TRST_B during the power-on reset flow. Simply tying TRST_B to PORESET_B is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP), which implements the debug interface to the chip.

The COP function of these processors allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert PORESET_B or TRST_B in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 56 allows the COP port to independently assert PORESET_B or TRST_B, while ensuring that the target can drive PORESET_B as well.

The COP interface has a standard header, shown in Figure 55, for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header; so emulator vendors have issued many different pin numbering schemes. Some COP headers are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom. Still others number the pins counter-clockwise from pin 1 (as with an IC). Regardless of the numbering scheme, the signal placement recommended in Figure 55 is common to all known emulators.

3.6.1.1 Termination of Unused Signals

If the JTAG interface and COP header are not used, Freescale recommends the following connections:

- TRST_B must be tied to PORESET_B through a 0 KΩ isolation resistor so that it is asserted when the system reset signal (PORESET_B) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system as shown in Figure 56. If this is not possible, the isolation resistor allows future access to TRST_B in case a JTAG interface may need to be wired onto the system in future debug situations.
- No pull-up/pull-down is required for TDI, TMS or TDO.

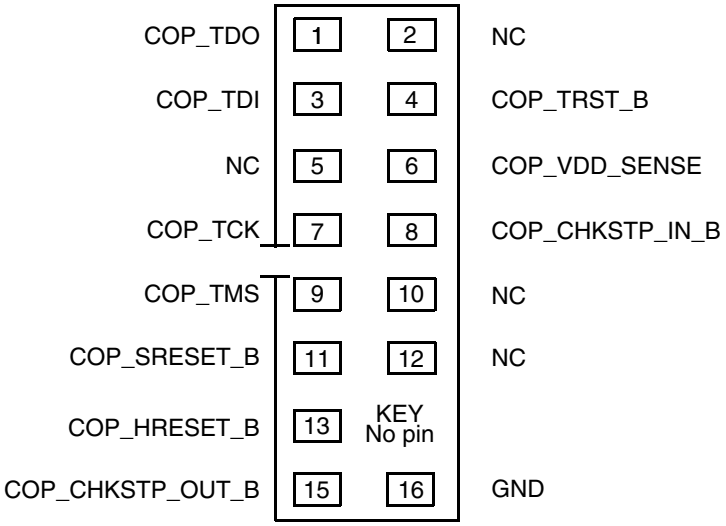
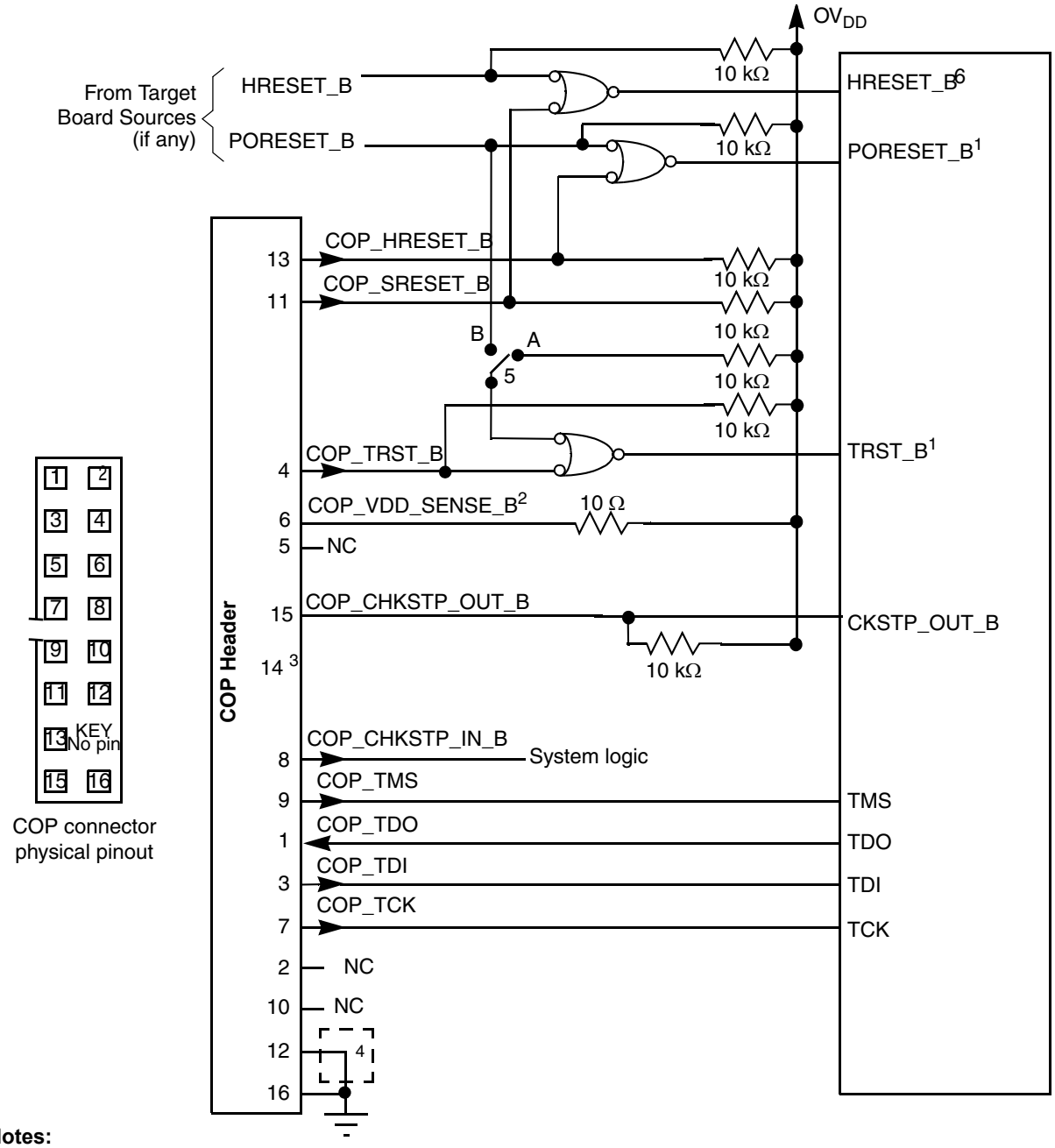


Figure 55. Legacy COP Connector Physical Pinout



Notes:

1. The COP port and target board must be able to independently assert PORESET_B and TRST_B to the processor in order to fully control the processor as shown here.
2. Populate this with a 10 Ω resistor for short-circuit/current-limiting protection.
3. The KEY location (pin 14) is not physically present on the COP header.
4. Although pin 12 is defined as a No-Connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.
5. This switch is included as a precaution for BSDL testing. The switch must be closed to position A during BSDL testing to avoid accidentally asserting the TRST_B line. If BSDL testing is not being performed, this switch must be closed to position B.
6. Asserting HRESET_B causes a hard reset on the device.

Figure 56. Legacy JTAG Interface Connection

3.6.2 Aurora Configuration Signals

Correct operation of the Aurora interface requires configuration of a group of system control pins as demonstrated in Figure 57 and Figure 58. Care must be taken to ensure that these pins are maintained at a valid negated state under normal operating conditions as most have asynchronous behavior and spurious assertion gives unpredictable results.

Freescale recommends that the Aurora 22 pin duplex connector be designed into the system as shown in Figure 59 or the 70 pin duplex connector be designed into the system as shown in Figure 60.

If the Aurora interface is not used, Freescale recommends the legacy COP header be designed into the system as described in Section 3.6.1.1, "Termination of Unused Signals."

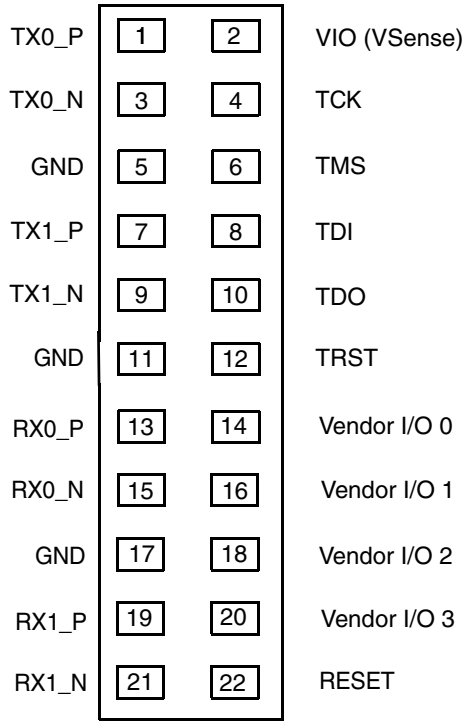


Figure 57. Aurora 22 Pin Connector Duplex Pinout

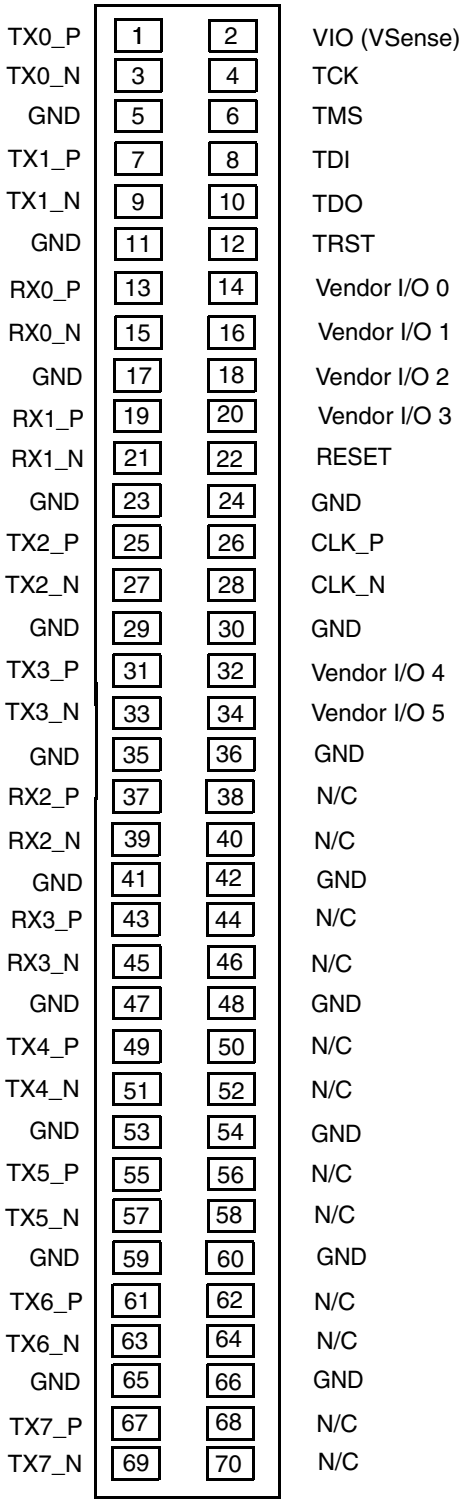
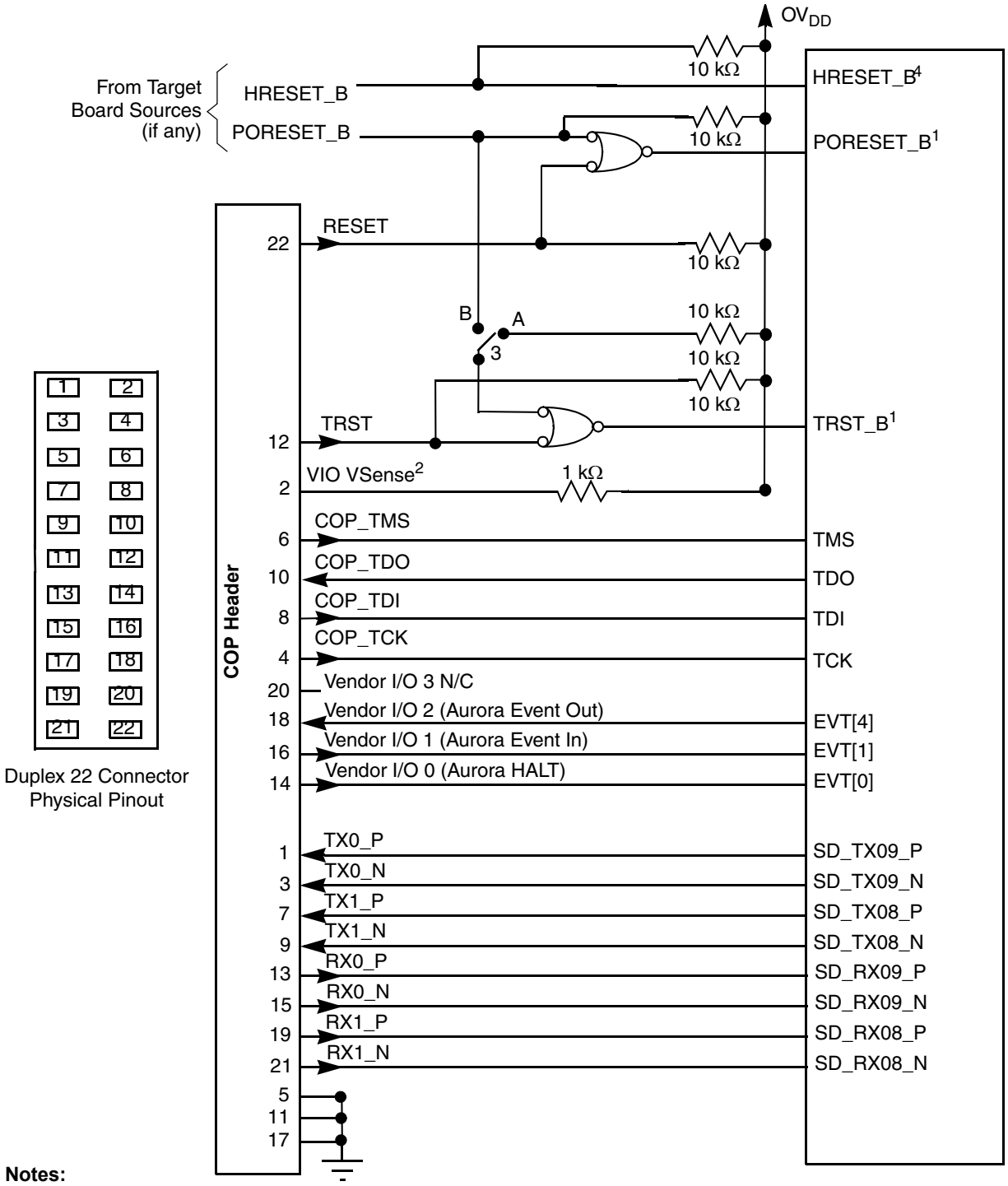


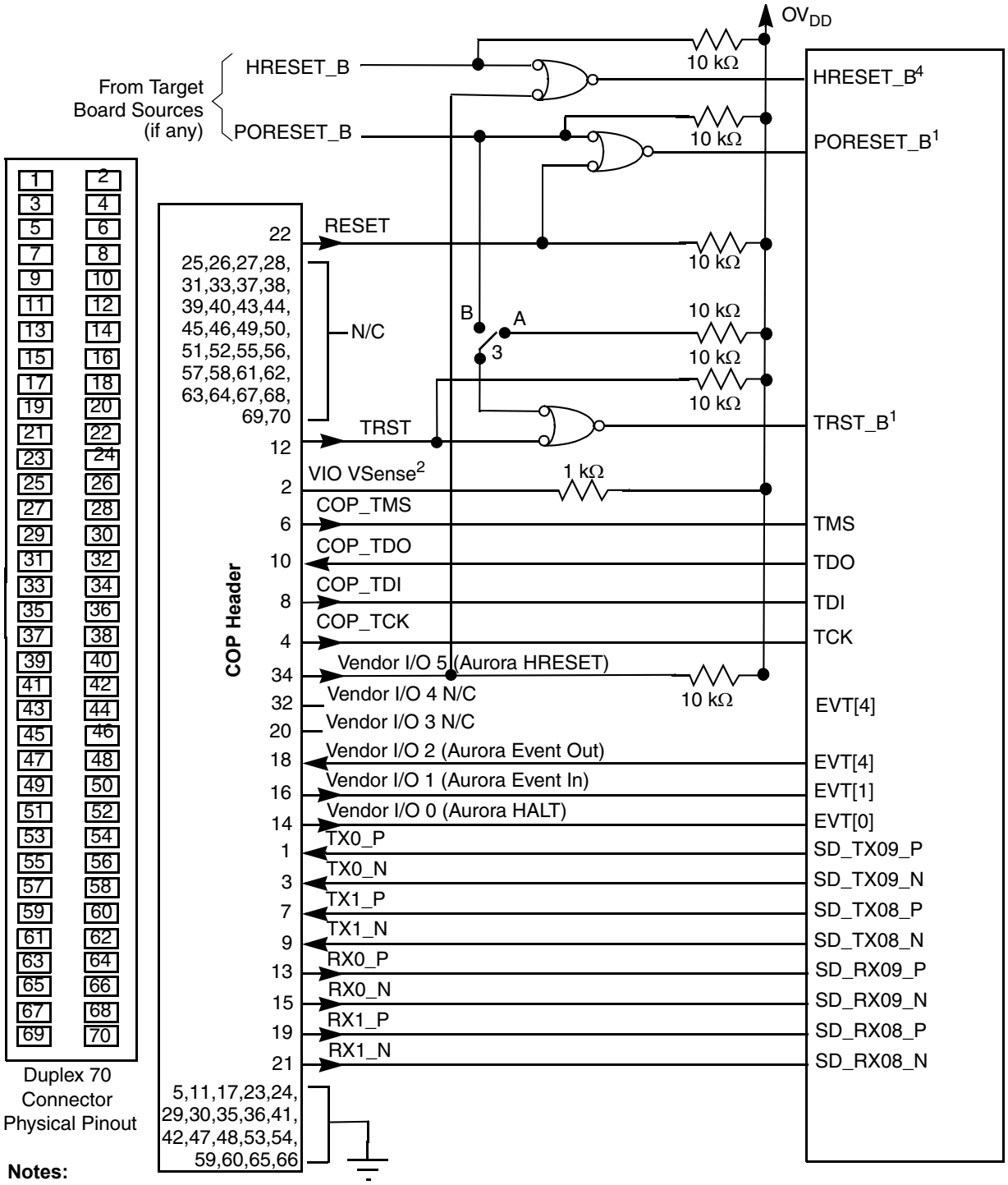
Figure 58. Aurora 70 Pin Connector Duplex Pinout



Notes:

1. The Aurora port and target board must be able to independently assert PORESET_B and TRST_B to the processor in order to fully control the processor as shown here.
2. Populate this with a 1 kΩ resistor for short-circuit/current-limiting protection.
3. This switch is included as a precaution for BSDL testing. The switch must be closed to position A during BSDL testing to avoid accidentally asserting the TRST_B line. If BSDL testing is not being performed, this switch must be closed to position B.
4. Asserting HRESET_B causes a hard reset on the device. HRESET_B is not used by the Aurora 22 pin connector.

Figure 59. Aurora 22 Pin Connector Duplex Interface Connection



Notes:

1. The Aurora port and target board must be able to independently assert PORESET_B and TRST_B to the processor in order to fully control the processor as shown here.
2. Populate this with a 1 kΩ resistor for short-circuit/current-limiting protection.
3. This switch is included as a precaution for BSDL testing. The switch must be closed to position A during BSDL testing to avoid accidentally asserting the TRST_B line. If BSDL testing is not being performed, this switch must be closed to position B.
4. Asserting HRESET_B causes a hard reset on the device.

Figure 60. Aurora 70 Pin Connector Duplex Interface Connection

3.6.3 Guidelines for High-Speed Interface Termination

3.6.3.1 SerDes Interface Entirely Unused

If the high-speed SerDes interface is not used at all, the unused pin must be terminated as described in this section.

The following pins must be left unconnected:

- SD_TX[17:0]
- SD_TX_B[17:0]

The following pins must be connected to SGND:

- SD_RX[17:0]
- SD_RX_B[17:0]
- SD_REF_CLK1, SD_REF_CLK2, SD_REF_CLK3
- SD_REF_CLK1_B, SD_REF_CLK2_B, SD_REF_CLK3_B

The following pins must be left unconnected:

- SD_IMP_CAL_RX
- SD_IMP_CAL_TX

In the RCW configuration fields SRDS_LPD1_B, SRDS_LPD2_B, and SRDS_LPD3_B, all bits must be set to power down all the lanes in each bank.

The RCW configuration field SRDS_EN may be cleared to power down the SerDes block for power saving. RCW[SRDS_EN] = 0 power downs the PLLs of all three banks.

Additionally, software may configure SRDSB*n*RSTCTL[SDPD] = 1 for the unused banks to power down the SerDes bank PLLs for power savings.

Note that both SVDD and XVDD must remain powered.

3.6.3.2 SerDes Interface Partly Unused

If only part of the high speed SerDes interface pins are used, the remaining high-speed serial I/O pins must be terminated as described in this section.

The following unused pins must be left unconnected:

- SD_TX[*n*]
- SD_TX_B[*n*]

The following unused pins must be connected to SGND:

- SD_RX[*n*]
- SD_RX_B[*n*]
- SD_REF_CLK1, SD_REF_CLK1_B (If entire SerDes bank 1 unused)
- SD_REF_CLK2, SD_REF_CLK2_B (If entire SerDes bank 2 unused)
- SD_REF_CLK3, SD_REF_CLK3_B (If entire SerDes bank 2 and 3 are unused)

In the RCW configuration field SRDS_LPD*n*_B for each bank, the respective bit for each unused lane must be set to power down the lane.

If an entire SerDes bank is unused, software may configure SRDSB*n*RSTCTL[SDPD] = 1 for the unused bank to power down the SerDes bank PLL for power savings, however, SerDes bank 3 PLL may only be powered down if the entire SerDes bank 2 and 3 are unused.

3.7 Recommended Thermal Model

Information about Flotherm models of the package or thermal data not available in this document can be obtained from your local Freescale sales office.

3.8 Thermal Management Information

This section provides thermal management information for the flip chip plastic ball grid array (FC-PBGA) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design—the heat sink, airflow, and thermal interface material. The chip implements several features designed to assist with thermal management, including the temperature diode. The temperature diode allows an external device to monitor the die temperature in order to detect excessive temperature conditions and alert the system; see Section 3.8.3, "Temperature Diode," for more information.

The recommended attachment method to the heat sink is illustrated in the following figure. The heat sink must be attached to the printed-circuit board with the spring force centered over the die. This spring force must not exceed 10 pounds force (45 Newton).

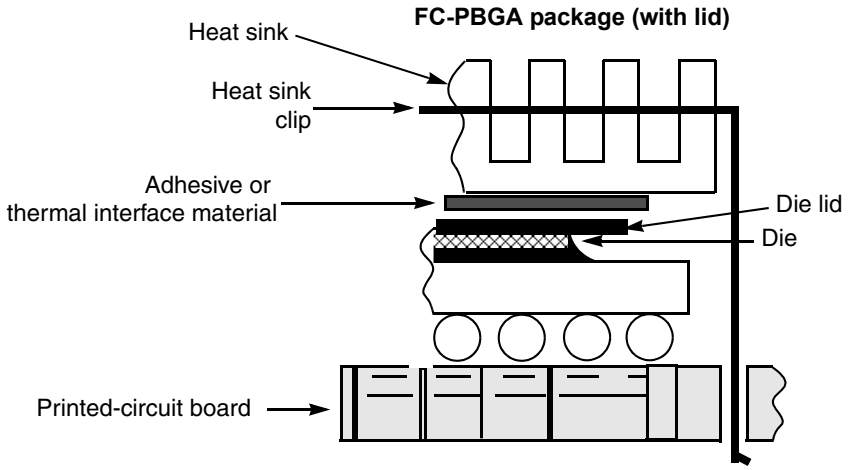


Figure 61. Package Exploded Cross-Sectional View—FC-PBGA (with Lid) Package

The system board designer can choose between several types of heat sinks to place on the device. There are several commercially-available thermal interfaces to choose from in the industry. Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

3.8.1 Internal Package Conduction Resistance

For the package, the intrinsic internal conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance
- The die junction-to-lid-top thermal resistance
- The die junction-to-board thermal resistance

This figure depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

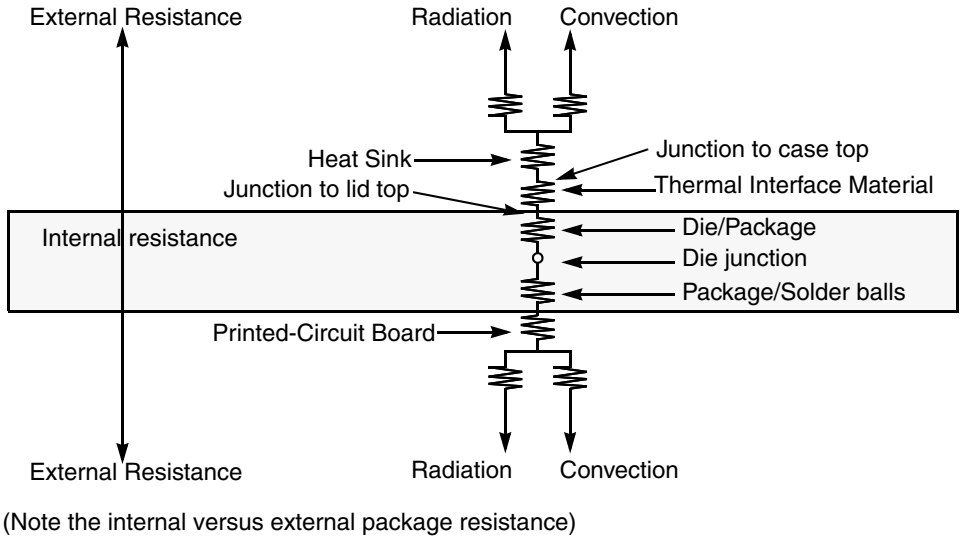


Figure 62. Package with Heat Sink Mounted to a Printed-Circuit Board

The heat sink removes most of the heat from the device. Heat generated on the active side of the chip is conducted through the silicon and through the heat sink attach material (or thermal interface material), and finally to the heat sink. The junction-to-case thermal resistance is low enough that the heat sink attach material and heat sink thermal resistance are the dominant terms.

3.8.2 Thermal Interface Materials

A thermal interface material is required at the package-to-heat sink interface to minimize the thermal contact resistance. The performance of thermal interface materials improves with increasing contact pressure; this performance characteristic chart is generally provided by the thermal interface vendor. The recommended method of mounting heat sinks on the package is by means of a spring clip attachment to the printed-circuit board (see Figure 61).

The system board designer can choose among several types of commercially-available thermal interface materials.

3.8.3 Temperature Diode

The chip has a temperature diode on the microprocessor that can be used in conjunction with other system temperature monitoring devices (such as Analog Devices, ADT7461A™). These devices use the negative temperature coefficient of a diode operated at a constant current to determine the temperature of the microprocessor and its environment.

The following are the specifications of the chip's on-board temperature diode:

Operating range: 10 – 230μA

Ideality factor over 13.5 – 220 μA: n = 1.007 ± 0.008

4 Package Information

The following section describes the detailed content and mechanical description of the package.

4.1 Package Parameters for the P4080/P4081 FC-PBGA

The package parameters are as provided in the following list. The package type is 37.5 mm × 37.5 mm, 1295 flip-chip, plastic-ball grid array (FC-PBGA).

Package outline	37.5 mm × 37.5 mm
Interconnects	1295
Ball Pitch	1.0 mm
Ball Diameter (typical)	0.60 mm
Solder Balls	96.5% Sn, 3% Ag, 0.5% Cu
Module height (typical)	2.88 mm to 3.53 mm (maximum)

4.2 Mechanical Dimensions of the P4080/P4081 FC-PBGA

This figure shows the mechanical dimensions and bottom surface nomenclature of the chip

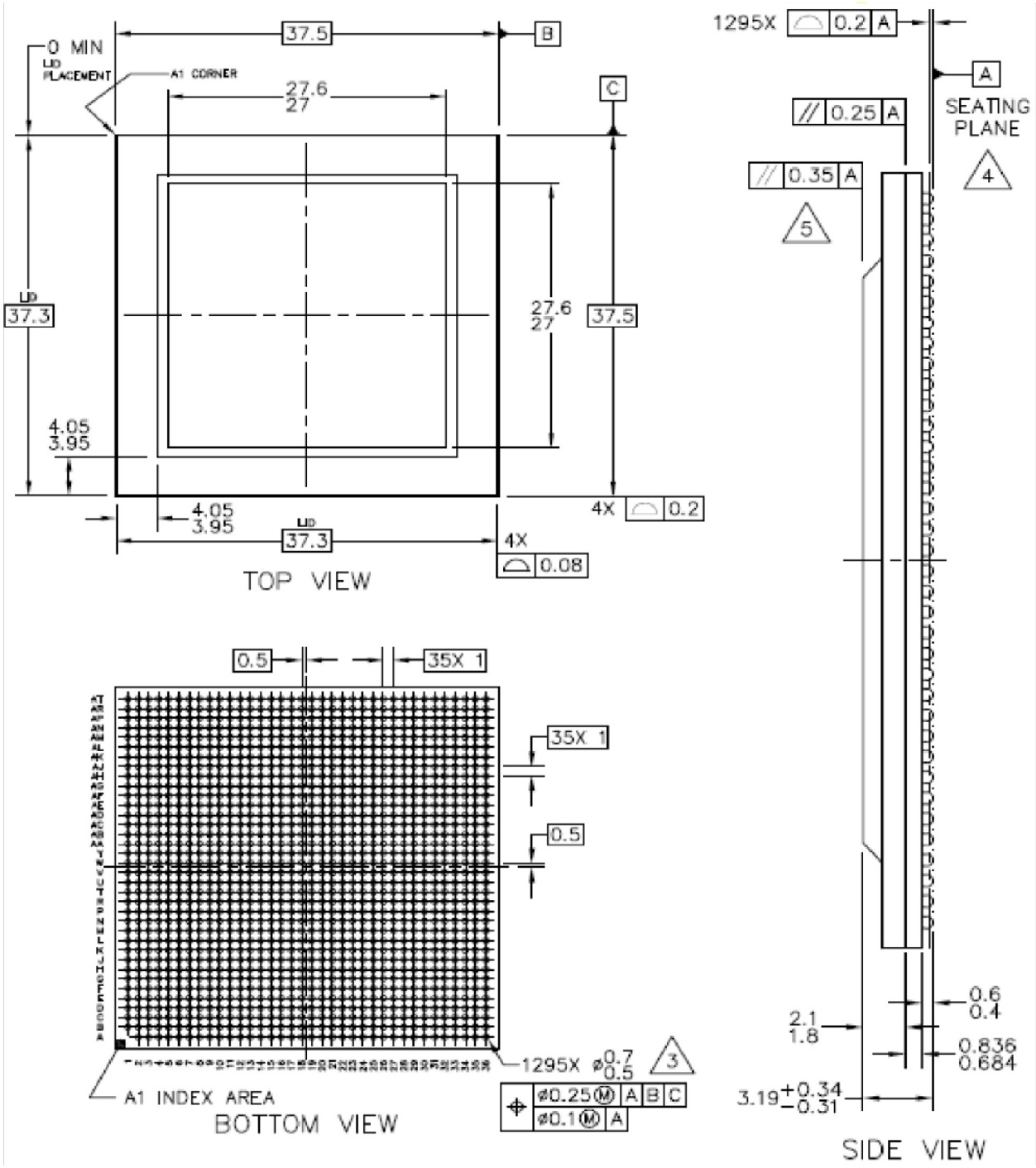


Figure 63. Mechanical Dimensions of the P4080/P4081 FC-PBGA with Full Lid

NOTES:

1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.

3. All dimensions are symmetric across the package center lines unless dimensioned otherwise.
4. Maximum solder ball diameter measured parallel to datum A.
5. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
6. Parallelism measurement excludes any effect of mark on top surface of package.

5 Security Fuse Processor

The P4040 implements the QorIQ platform's Trust Architecture, supporting capabilities such as secure boot. Use of the Trust Architecture features is dependent on programming fuses in the Security Fuse Processor (SFP). The details of the Trust Architecture and SFP can be found in the *P4080 QorIQ Integrated Multicore Communication Processor Family Reference Manual*.

In order to program SFP fuses, the user is required to supply 1.5 V to the POV_{DD} pin per Section 2.2, "Power Sequencing." POV_{DD} must only be powered for the duration of the fuse programming cycle, with a per device limit of two fuse programming cycles. All other times POV_{DD} must be connected to GND. The sequencing requirements for raising and lowering POV_{DD} are shown in Figure 8. To ensure device reliability, fuse programming must be performed within the recommended fuse programming temperature range per Table 3.

Users not implementing the QorIQ platform's Trust Architecture features are not required to program fuses and must connect POV_{DD} to GND.

6 Ordering Information

Contact your local Freescale sales office or regional marketing team for order information.

6.1 Part Numbering Nomenclature

This table provides the Freescale QorIQ platform part numbering nomenclature.

Table 106. Part Numbering Nomenclature

p	*n*	*nn*	*n*	*x*	*t*	*e*	*n*	*c*	*d*	*a*	*r*
Generation	**Platform**	**Number of Cores**	**Derivative**	**Qual Status**	**Temperature Range**	**Encryption**	**Package Type**	**CPU Speed**	**DDR Speed**	**V_{DD}**	**Die Revision**
P = 45 nm	1–5	01 = 1 core 02 = 2 core 04 = 4 core 08 = 8 core	0–9	P = Prototype N = Qualified	S = Std temp (0 to 105 C) X = Ext temp (–40 to 105 C)	E = SEC present N = SEC not present	1 = FC-PBGA Lead free 7=FC-PBGA C4/C5 Lead free	K= 1000 MHz M = 1200 MHz N = 1333 MHz P = 1500 MHz	K= 1000 MHz M = 1200 MHz N = 1300 or 1333 MHz Z =Not specified	blank=1.0 V± 50 mV A=1.0V –30/+50 mV	A = Rev 1.0 B = Rev 2.0 C = Rev 3.0

6.2 Orderable Part Numbers Addressed by This Document

This table provides the Freescale orderable part numbers addressed by this document for the chip.

Table 107. Orderable Part Numbers Addressed by This Document for P4080 Rev 2.0

Part Number	*p*	*n*	*nn*	*n*	*x*	*t*	*e*	*n*	*c*	*d*	*r*
P4080NSE1MMB	P	4	08 = 8 core	0	N = Qualified	S = Std temp	E = SEC present	1	M = 1200 MHz	M	B
P4080NSE1NNB							E = SEC present		N = 1333 MHz	N	
P4080NSE1PNB							E = SEC present		P = 1500 MHz	N	
P4080NSN1MMB							N = SEC not present		M = 1200 MHz	M	
P4080NSN1NNB							N = SEC not present		N = 1333 MHz	N	
P4080NSN1PNB							N = SEC not present		P = 1500 MHz	N	
P4080NXE1MMB						X = Ext temp	E = SEC present		M = 1200 MHz	M	
P4080NXN1MMB							N = SEC not present				

Table 108. Orderable Part Numbers Addressed by This Document for P4080 Rev 3.0

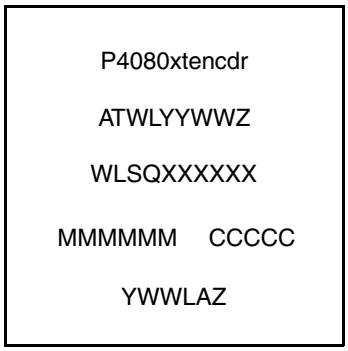
Part Number	*p*	*n*	*nn*	*n*	*x*	*t*	*e*	*n*	*c*	*d*	*a*	*r*
P4080NSE7MMC	P	4	08 = 8 core	0	N	S	E = SEC present	7	M = 1200 MHz	M		C
P4080NSN7MMC						S	N = SEC not present		M = 1200 MHz	M		
P4080NXE7MMC						X	E = SEC present		M = 1200 MHz	M		
P4080NXN7MMC						X	N = SEC not present		M = 1200 MHz	M		
P4080NSE7PNC						S	E = SEC present		P = 1500 MHz	N		
P4080NSN7PNC						S	N = SEC not present		P = 1500 MHz	N		
P4080NSE7PNAC						S	E = SEC present		P = 1500 MHz	N	A	
P4080NSN7PNAC						S	N = SEC not present		P = 1500 MHz	N	A	
P4080NXE7PNAC						X	E = SEC present		P = 1500 MHz	N	A	

Table 109. Orderable Part Numbers Addressed by This Document for P4081

Part Number	*p*	*n*	*nn*	*n*	*x*	*t*	*e*	*n*	*c*	*d*	*r*
P4081NSE7MMC	P	4	08 = 8 core	1	N = Qualified	S = Std temp	E = SEC present	7	M = 1200 MHz	M	C
P4081NSN7MMC							N = SEC not present		M = 1200 MHz	M	
P4081NSE7KKC							E = SEC present		K = 1000 MHz	K	
P4081NSN7KKC							N = SEC not present		K = 1000 MHz	K	

6.2.1 Part Marking

Parts are marked as in the example shown in this figure.



FC-PBGA

Notes:

P4080xtencdr is the orderable part number. See Table 107 for details.

ATWLYYWWZ is the test traceability code.

WLSQXXXXXX is the lot label.

MMMMMM is the mask number.

CCCCC is the country code.

YWWLAZ is the assembly traceability code.

Figure 64. Part Marking for FC-PBGA Device

7 Revision History

This table provides a revision history for this document.

Table 110. Document Revision History

Rev. Number	Date	Substantive Change(s)
4	04/2013	• Added P4081 • Added power dissipation values for P4081 to Table 6, “P4080/P4081 Power Dissipation” • Removed information pertaining to Rev 1.0 silicon from Table 91 “P4080 Processor Clocking Specifications”. • Added Table 92 “P4081 Processor Clocking Specifications” In Table 106 Added new column and values for Vdd. Added values to columns Package Type, CPU Speed, DDR Speed and Die Revision. • Included new tables in Section 6.2, “Orderable Part Numbers Addressed by This Document”

Table 110. Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
3	06/2012	• In Table 31, eSPI AC Timing Specifications1," updated note 3 from "The greater of the two output timings for t_{NIKHOX} and t_{NIKHOV} are used when SPCOM[RxDelay] of the eSPI command register is set. For example, the t_{NIKHOX} is 4.0 and t_{NIKHOV} is 7.0 if SPCOM[RxDelay] is set to be 1" to "See the P4080RM for details about the register SPMODE." • Throughout document, updated kOhm to KΩ. • In Table 35, "RGMII AC Timing Specifications (LVDD = 2.5 V)," added note 7 as follows: "The frequency of RX_CLK (input) should not exceed the frequency of GTX_CLK (output) by more than 300 ppm." • In Table 35, "RGMII AC Timing Specifications (LVDD = 2.5 V)," added note 7 to the notes column for the "Data to clock output skew (at transmitter)" row. • In Table 43, "dTSEC IEEE 1588 AC Timing Specifications," added note 4 as follows: "For 1588, there are three input clock sources: TSEC_1588_CLK_IN, RTC and FMan/4. When using TSEC_1588_CLK_IN, the minimum clock period is $2 \times t_{T1588CLK}$." • In Table 43, "dTSEC IEEE 1588 AC Timing Specifications," added note 4 to the notes column for the "TSEC_1588_CLK_OUT clock period" row and updated the "TSEC_1588_PULSE_OUT" row to "TSEC_1588_PULSE_OUT, TSEC_1588_ALARM_OUT." • In Figure 18, "dTSEC IEEE 1588 Output AC Timing," updated TSEC_1588_TRIG_OUT to TSEC_1588_ALARM_OUT. • In Figure 24, "GPCM Output Timing Diagram," updated t_{LBKHOX} to t_{LBKLOX} and t_{LBKHOV} to t_{LBKLOV}. • In Table 54, "eSDHC AC Timing Specifications," updated note 3 from "To satisfy setup timing, the delay difference between clock input and cmd/data input must not exceed 2 ns" to "To satisfy setup timing, one way board routing delay between Host and Card, on SD_CLK, SD_CMD and SD_DATx should not exceed 1 ns." • In Table 54, "eSDHC AC Timing Specifications," updated note 4 from"$C_{CARD} \leq 10$ pF, (1 card), and $C_L = C_{BUS} + C_{HOST} + C_{CARD} \leq 40$ pF" to "$C_{CARD} \leq 10$ pF, (1 card), and $C_L = C_{BUS} + C_{HOST} + C_{CARD} \leq 40$ pF" and added note 5 as follows: "The parameter values apply to both full-speed and high-speed modes." • Updated signal naming convention to _N and _P in Figure 57 and Figure 58. • Updated Figure 33. • In Table 54, "eSDHC AC Timing Specifications," updated the min value for the Input setup times from 5 to 2.5 and added notes 3 and 5 in the notes column for this row. • In Table 107, "Orderable Part Numbers Addressed by This Document for P4080 Rev 2.0," updated P4080NSE1MM to P4080NSE1MMB. • In Table 54, "eSDHC AC Timing Specifications," in the notes column for the "Input hold times" row, added note 5 and removed note 3. In the notes column for the "Output delay time" row, included notes 4 and 5.

Table 110. Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
2	02/2012	• In Table 1, “Pins List by Bus,” changed the power supply to SVDD for all SerDes receiver pins. • In Table 1, “Pins List by Bus,” added note 3 for the following pins: LA[16:22], LA[25], USB1_D[7:4], USB2_D[7:4], EC1_TXD[3:0], EC2_TXD[3:0], RESET_REQ, MSRCID[1:2], and ASLEEP. • In Table 1, “Pins List by Bus,” added note 30 for MSRCID[0]. • In Table 1, “Pins List by Bus,” modified note 30, as follows: “Pin must NOT be pulled down during power-on reset. This pin may be pulled up, driven high, or if there are any externally connected devices, left in tristate.” • In Table 3, “Recommended Operating Conditions,” added note 5, as follows: “Supply voltage specified at the voltage sense pin. Voltage input pins must be regulated to provide specified voltage at the sense pin.” • Added a new note in Section 2.2, “Power Sequencing”: “Only 100,000 POR cycles are permitted per lifetime of a device.” • Added Table 8, “I/O Power Supply Estimated Value.” • In Table 12, “SYSCLK AC Timing Specifications,” changed the max to +/– 150 for SYSCLK peak period jitter. • In Table 18, “DDR2 SDRAM Interface DC Electrical Characteristics, modified note 2 as follows: “MVREF*n* is expected to be equal to 0.5 × GV_{DD} and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MVREF*n* may not exceed the MVREF*n* DC level by more than ±1% of the DC value (that is, ±18 mV).” • In Table 21, “Current-Draw Characteristics for MVREFn”, changed the max to 500 μA for current draw for DDR3 SDRAM for MVREF*n*. • In Figure 9, “DDR2 and DDR3 SDRAM Interface Input Timing Diagram,” modified the rightmost t_{DISKEW} range marker. • In Table 31, “eSPI AC Timing Specifications1,” updated the values for SPI_MOSI output rows. • In Table 35, “RGMII AC Timing Specifications (LVDD = 2.5 V),” updated the minimum value to 2.6 for data to clock input skew (at receiver). • Completely updated Figure 16, “RGMII AC Timing and Multiplexing Diagrams.” • Added Section 2.12.4.1, “dTSEC IEEE 1588 DC Timing Specifications.” • In Table 58, “JTAG AC Timing Specifications,” updated the Boundary-scan data value to 15. • In Table 80, “XAUI AC SD_REF_CLK3 and SD_REF_CLK3_B Input Clock Requirements,” updated the minimum and maximum values to –100 and 100, respectively, for SD_REF_CLK/SD_REF_CLK_B clock frequency tolerance. • In Table 89, “SGMII Transmit AC Timing Specifications,” remove the typical value for AC coupling capacitor.Also changed the minimum value to 10. • In Table 91, “P4040 Processor Clocking Specifications,” removed the first row from Local bus clock frequency, added value of 300 to empty cells, and added note 9 to PME and FM*n*, as follows: “For the FMan: 300 MHz is the minimum to support 1 G. 450 MHz is the minimum to support 10 G. 500 MHz is the minimum to support 10 G with PCD. 600 MHz is the minimum to support 12 G (10 G + 2*1 G) with PCD.” • In Section 3.3.1, “PLL Power Supply Filtering,” updated the second bullet in the list at the end of the section to read as follows: “Signals on the SerDes interface are fed from the XV_{DD} and SV_{DD} power plane.” • In Section 6.2, “Orderable Part Numbers Addressed by This Document,” added new part numbers and changed prototype parts to qualified.

Table 110. Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
1	07/2011	• In Table 1, “Pins List by Bus,” added note “For systems which boot from Local Bus (GPCM)-controlled NOR flash or (FCM)-controlled NAND flash, a pull up on LGPL4 is required.” • Added note reference 3 to LA[16:22] pins. • Updated note 16 to “For DDR2, Dn_MDIC[0] is grounded through an 18.2-Ω (full-strength mode) or 36.4-Ω (half-strength mode) precision 1% resistor and Dn_MDIC[1] is connected to GVDD through an 18.2-Ω (full-strength mode) or 36.4-Ω (half-strength mode) precision 1% resistor. These pins are used for automatic calibration of the DDR2 IOs. For DDR3, Dn_MDIC[0] is grounded through an 20-Ω (full-strength mode) or 40.2–Ω precision 1% resistor and Dn_MDIC[1] is connected to GVDD through an 20-Ω (full-strength mode) or 40.2-Ω precision 1% resistor. These pins are used for automatic calibration of the DDR3 IOs.” • In Table 91, P4080 Processor Clocking Specifications,” added note “For Maximum Processor Core Frequency = 1500 MHz, due to clock ratio combinations, Memory bus clock frequency maximum = 650 MHz.”
0	02/2011	Initial release

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