

Inverting 1.2MHz/2.7MHz DC/DC Converters with Integrated Schottky

FEATURES

- Integrated Schottky Rectifier
- Fixed Frequency 1.2MHz/2.7MHz Operation
- Very Low Noise: 1mV_{P-P} Output Ripple
- Low V_{CESAT} Switch: 270mV at 250mA
- -5V at 100mA from 5V Input
- -12V at 30mA from 3.3V Input
- Low Input Bias Current GND Based FB Input
- Low Impedance (40Ω) 1.265V Reference Output
- High Output Voltage: Up to -38V
- Wide Input Range: 2.5V to 16V
- Uses Tiny Surface Mount Components
- Low Shutdown Current: <10μA
- Low Profile (1mm) SOT-23 (ThinSOT™) Package
- 8-Lead DFN (2mm × 2mm × 0.75mm) Package, LT3462A Only

APPLICATIONS

- CCD Bias
- LCD Bias
- GaAs FET Bias
- General Purpose Negative Voltage Supply

DESCRIPTION

The LT[®]3462/LT3462A are general purpose fixed frequency current mode inverting DC/DC converters. Both devices feature an integrated Schottky and a low V_{CESAT} switch allowing a small converter footprint and lower parts cost. The LT3462 switches at 1.2MHz while the LT3462A switches at 2.7MHz. These high speeds enable the use of tiny, low cost and low height capacitors and inductors.

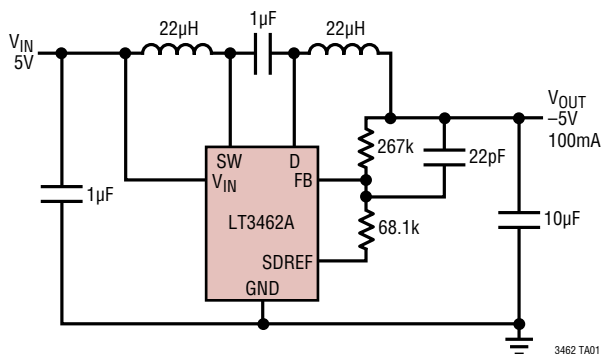
The LT3462/LT3462A operate in a dual inductor inverting topology that filters both the input and output currents. Very low output voltage ripple approaching 1mV_{P-P} can be achieved when ceramic capacitors are used. Fixed frequency switching ensures a clean output free from low frequency noise typically present with charge pump solutions. The 40V switch allows a V_{IN} to V_{OUT} differential of up to 38V for dual inductor topologies.

Both devices provide a low impedance 1.265V reference output to supply the feedback resistor network. A ground referenced, high impedance FB input allows high feedback resistor values without compromising output accuracy.

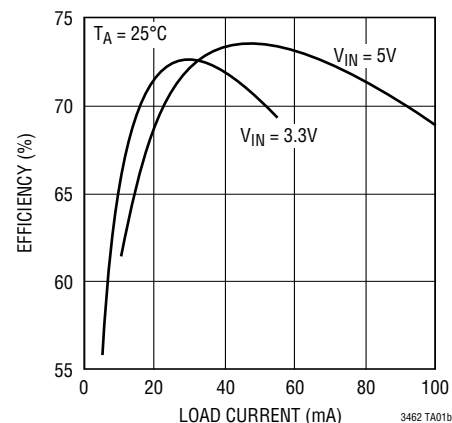
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TYPICAL APPLICATION

5V to -5V, 100mA Inverting DC/DC Converter



Efficiency



LT3462/LT3462A

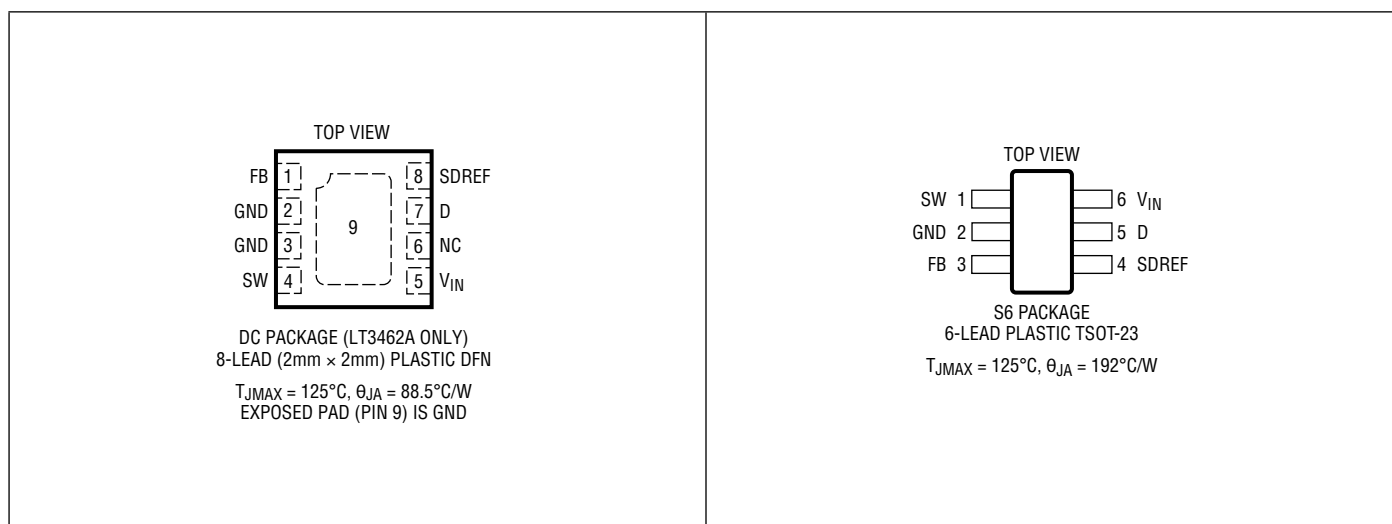
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Input Voltage (V_{IN}) 16V
SW Voltage 40V
D Voltage -40V
SDREF, FB Voltage 2.5V
Operating Ambient
Temperature Range (Note 3) -40°C to 85°C

Maximum Junction Temperature 125°C
Storage Temperature Range -65°C to 150°C
Lead Temperature (Soldering, 10sec)
(TSOT-23 Package Only) 300°C

PIN CONFIGURATION



ORDER INFORMATION

<http://www.linear.com/product/LT3462#orderinfo>

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3462ES6#PBF	LT3462ES6#TRPBF	LTBBV	6-Lead Plastic TSOT-23	-40°C to 85°C
LT3462AES6#PBF	LT3462AES6#TRPBF	LTBGB	6-Lead Plastic TSOT-23	-40°C to 85°C
LT3462AEDC#PBF	LT3462AEDC#TRPBF	LHGH	8-Lead (2mm × 2mm) Plastic DFN	-40°C to 85°C

Consult ADI Marketing for parts specified with wider operating temperature ranges.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreel/>. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$, $V_{IN} = 3\text{V}$, unless otherwise noted.

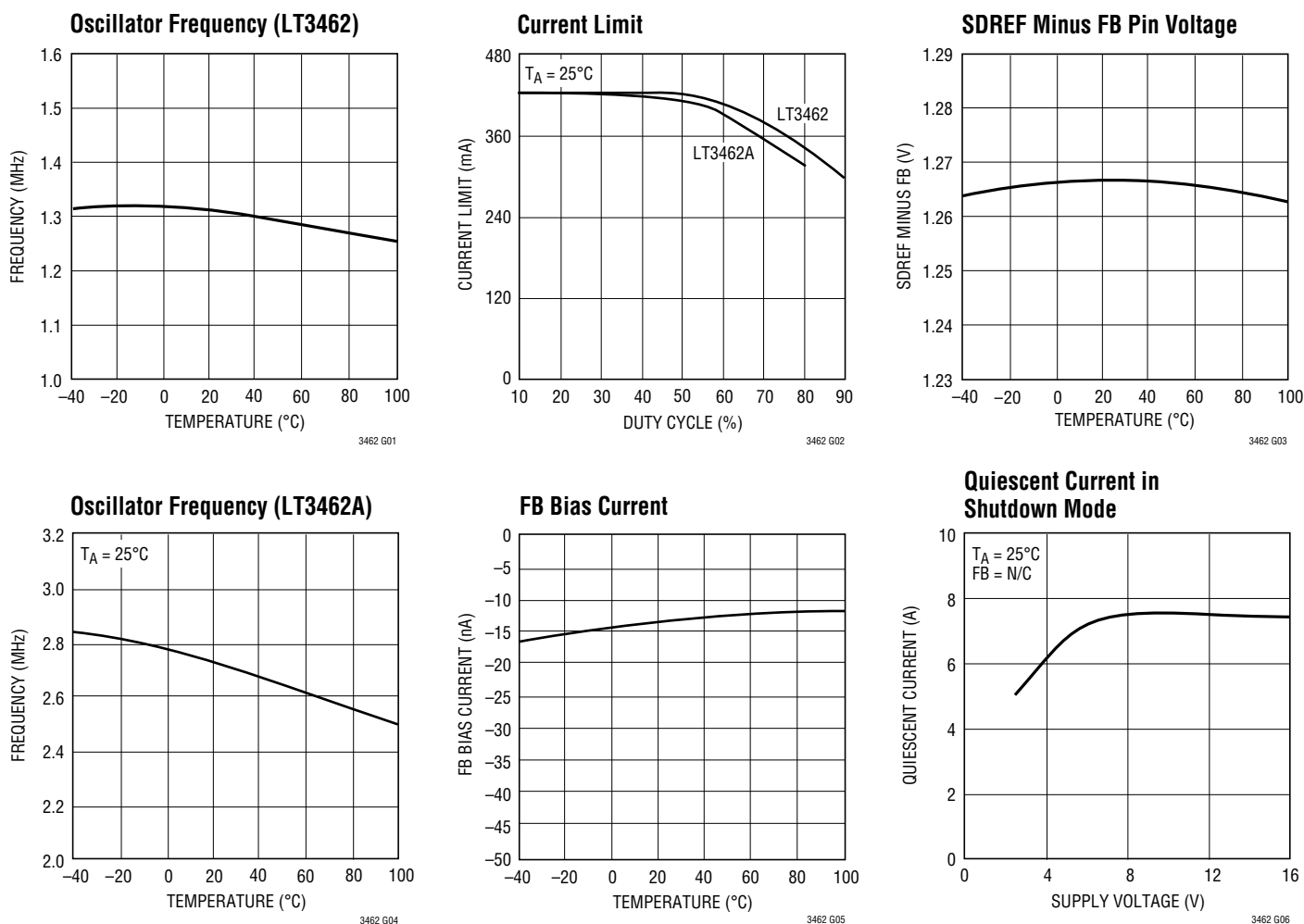
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Operating Voltage			2.5			V
Maximum Operating Voltage					16	V
SDREF Voltage	$10\mu\text{A} > I_{SDREF} \geq -80\mu\text{A}$	●	1.245	1.265	1.285	V
FB Pin Bias Current (Note 2)				15	50	nA
SDREF Minus FB Voltage	$10\mu\text{A} > I_{SDREF} \geq -80\mu\text{A}$	●	1.235	1.263	1.285	V
Error Amp Offset Voltage			-12		12	mV
SDREF Reference Source Current	$SDREF > 1.2\text{V}$	●	120	180		μA
Supply Current	$FB = -0.05\text{V}$, Not Switching $SDREF = 0\text{V}$, $FB = \text{Open}$, $V_{IN} = 5\text{V}$			2.9 6.5	3.6 10	mA μA
SDREF Line Regulation				0.007		%/V
Switching Frequency (LT3462)		●	0.8	1.2	1.6	MHz
Switching Frequency (LT3462A)		●	2.0	2.7	3.5	MHz
Maximum Duty Cycle (LT3462)		●	90			%
Maximum Duty Cycle (LT3462A)		●	77			%
Switch Current Limit			300	420		mA
Switch V_{CESAT}	$I_{SW} = 250\text{mA}$			270	350	mV
Switch Leakage Current	$V_{SW} = 5\text{V}$			0.01	1	μA
Rectifier Leakage Current	$V_D = -40\text{V}$			0.03	4	μA
Rectifier Forward Drop	$I_{SCHOTTKY} = 250\text{mA}$			800	1100	mV
SDREF Voltage Low		●			0.20	V
SDREF Off-State Pull-Up Current			1	2	3	μA
SDREF Turn-Off Current			-300	-200		μA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Current flows out of the pin.

Note 3: The LT3462E is guaranteed to meet specifications from 0°C to 70°C . Specifications over the -40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

TYPICAL PERFORMANCE CHARACTERISTICS



PIN FUNCTIONS (TSOT-23/DFN)

SW (Pin 1/Pin 4): Switch Pin. Connect to external inductor L1 and positive terminal of transfer cap.

GND (Pin 2/Pins 2, 3): Ground. Tie directly to local ground plane.

FB (Pin 3/Pin 1): Feedback Pin. Connect resistive divider tap here. Set R1 according to $R1 = R2 \cdot (V_{OUT}/1.265V)$. In shutdown, a proprietary shutdown bias current cancellation circuit allows the internal 3 μ A source to pull up the SDREF pin, even with residual negative voltage on V_{OUT} .

SDREF (Pin 4/Pin 8): Dual Function Shutdown and 1.265V Reference Output Pin. Pull to GND with external N-FET to turn regulator off. Turn-off pull-down and a 2 μ A internal source will pull SDREF up to turn-on the

regulator. At turn-on, a 180 μ A internal source pulls the pin to the regulation voltage. The SDREF pin can supply up to 80 μ A at 1.265V to bias the feedback resistor divider. An optional soft-start circuit capacitor connects from this pin to $-V_{OUT}$.

D (Pin 5/Pin 7): Anode Terminal of Integrated Schottky Diode. Connect to negative terminal of transfer cap and external inductor L2.

V_{IN} (Pin 6/Pin 5): Input Supply Pin. Must be locally bypassed.

Exposed Pad (NA/Pin 9): GND. The exposed pad should be soldered to the PCB ground to achieve the rated thermal performance.

BLOCK DIAGRAM

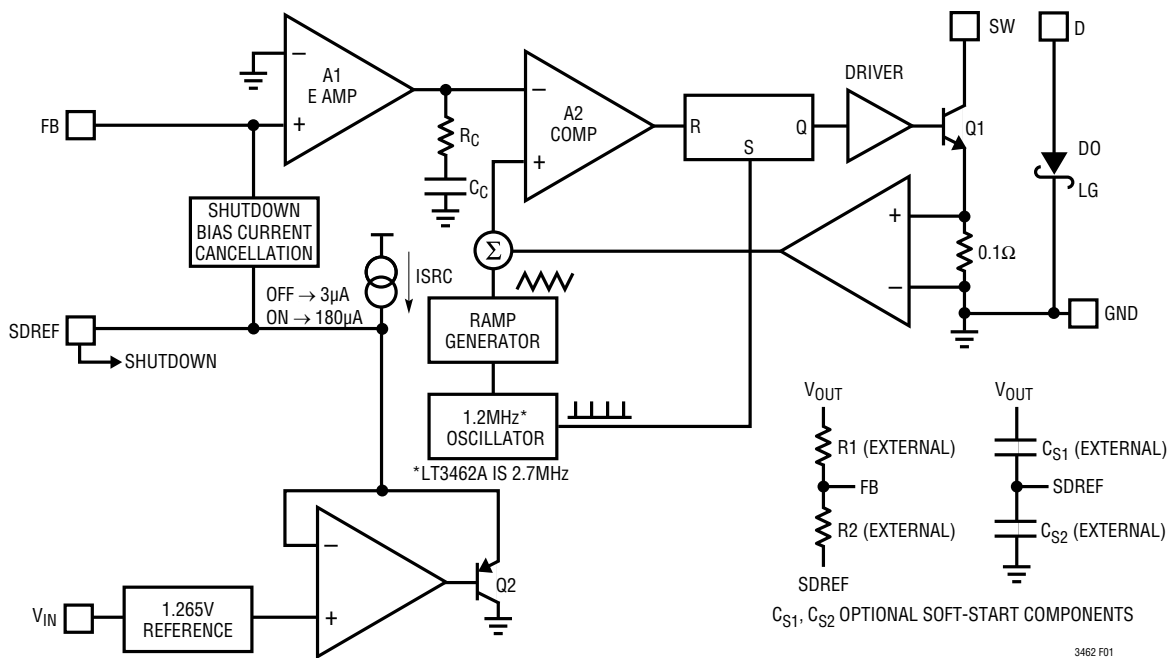


Figure 1. Block Diagram

OPERATION

The LT3462 uses a constant frequency, current mode control scheme to provide excellent line and load regulation. Operation can be best understood by referring to the Block Diagram in Figure 1. At the start of each oscillator cycle, the SR latch is set, turning on the power switch Q1. A voltage proportional to the switch current is added to a stabilizing ramp and the resulting sum is fed into the positive terminal of the PWM comparator. When this voltage exceeds the voltage at the output of the EAMP, the SR latch is reset, turning off the power switch. The level at the output of the EAMP is simply an amplified version of the difference between the feedback voltage and GND. In this manner, the error amplifier sets the correct peak current level to keep the output in regulation. If the error amplifier's output increases, more current is taken from the output; if it decreases, less current is taken. One function not shown in Figure 1 is the current limit. The switch current is constantly monitored and not allowed to exceed the nominal value of 400mA. If the switch current reaches 400mA, the SR latch is reset regardless of the output state

of the PWM comparator. This current limit cell protects the power switch as well as various external components connected to the LT3462.

SDREF is a dual function input pin. When driven low it shuts the part down, reducing quiescent supply current to less than 10 μ A. When not driven low, the SDREF pin has an internal pull-up current that turns the regulator on. Once the part is enabled, the SDREF pin sources up to 180 μ A nominally at a fixed voltage of 1.265V through external resistor R2 to FB. If there is no fault condition present, FB will regulate to 0V, and V_{OUT} will regulate to $1.265V \cdot (-R1/R2)$. An optional soft-start circuit uses the fixed SDREF pull-up current and a capacitor from SDREF to V_{OUT} to set the dV/dt on V_{OUT} . In shutdown, an FB bias current cancellation circuit supplies up to 150 μ A biasing current to external resistor R1 while V_{OUT} is lower than FB. This function eliminates R2 loading of SDREF during shutdown. As a result, supply current in shutdown may exceed 10 μ A by the amount of current flowing in R1.

APPLICATIONS INFORMATION

Inrush Current

The LT3462 has a built-in Schottky diode. When supply voltage is applied to the V_{IN} pin, the voltage difference between V_{IN} and V_D generates inrush current flowing from input through the inductor and the Schottky diode to charge the flying capacitor to V_{IN} . The maximum non-repetitive surge current the Schottky diode in the LT3462 can sustain is 1.5A. The selection of inductor and capacitor value should ensure the peak of the inrush current to be below 1.5A. The peak inrush current can be calculated as follows:

$$I_P = \frac{V_{IN} - 0.6}{\sqrt{\frac{L}{C}} - 1} \exp\left(-\frac{\pi}{2\sqrt{\frac{L}{C}} - 1}\right)$$

where L is the inductance between supply and SW, and C is the capacitance between SW and D.

Table 3 gives inrush peak currents for some component selections.

Table 3. Inrush Peak Current

V_{IN} (V)	L (μ H)	C (μ F)	I_P (A)
5	22	1	0.70
5	33	1	0.60
12	47	1	1.40

Inductor Selection

Each of the two inductors used with LT3462 should have a saturation current rating (where inductance is approximately 70% of zero current inductance) of approximately 0.25A or greater. If the device is used in the charge pump mode, where there is only one inductor, then its rating should be 0.35A or greater. DCR of the inductors should be less than 1 Ω . For LT3462, a value of 22 μ H is suitable if using a coupled inductor such as Sumida CLS62-220. If using two separate inductors, increasing the value to 47 μ H will result in the same ripple current. For LT3462A, a value of 10 μ H for the coupled inductor and 22 μ H for two inductors will be acceptable for most applications.

Capacitor Selection

Ceramic capacitors are recommended. An X7R or X5R dielectric should be used to avoid capacitance decreasing severely with applied voltage and at temperature limits. The “flying” capacitor between the SW and D pins should be a ceramic type of value 1 μ F or more. When used in the dual inductor or coupled inductor topologies the flying capacitor should have a voltage rating that is more than the difference between the input and output voltages. For the charge pump inverter topology, the voltage rating should be more than the output voltage. The output capacitor should be a ceramic type. Acceptable output capacitance varies from 1 μ F for high V_{OUT} (–36V), to 10 μ F for low V_{OUT} (–5V). The input capacitor should be a 1 μ F ceramic type and be placed as close as possible to the LT3462/LT3462A.

Layout Hints

The high speed operation of the LT3462 demands careful attention to board layout. You will not get advertised performance with careless layout. Figure 2 shows the recommended component placement. A ceramic capacitor of 1 μ F or more must be placed close to the IC for input supply bypassing.

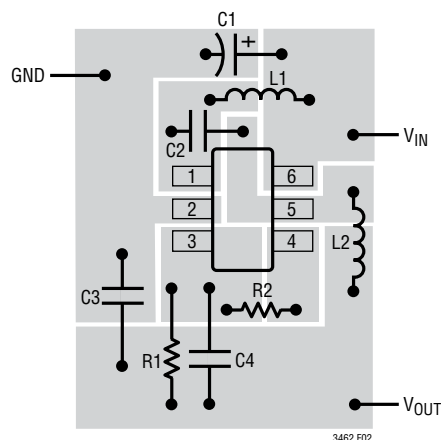
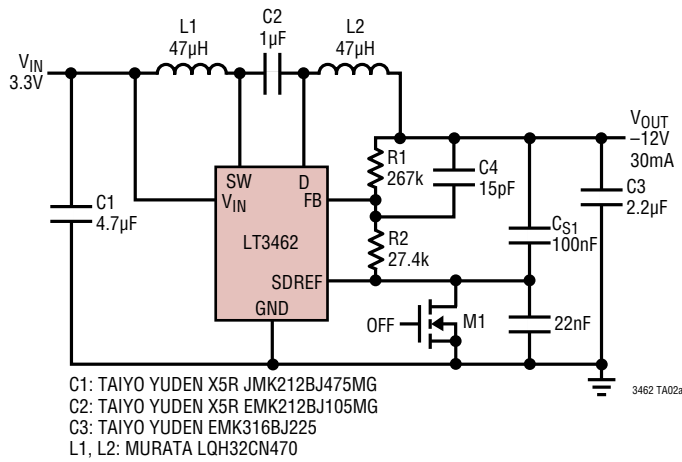


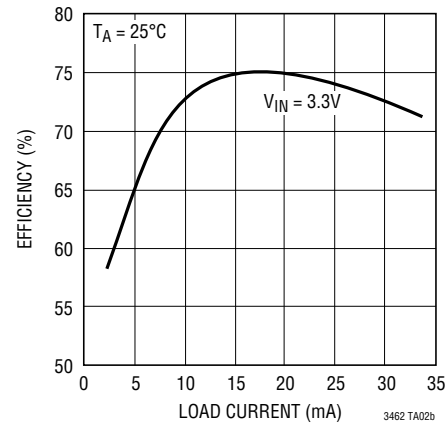
Figure 2. Suggested Layout

TYPICAL APPLICATIONS

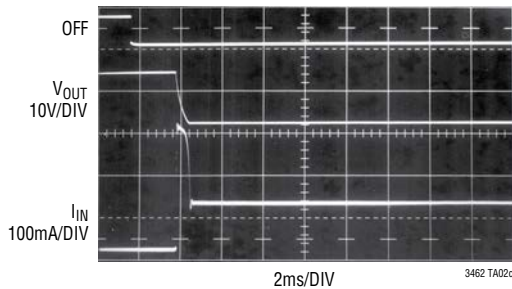
3.3V to -12V with Soft-Start Circuit



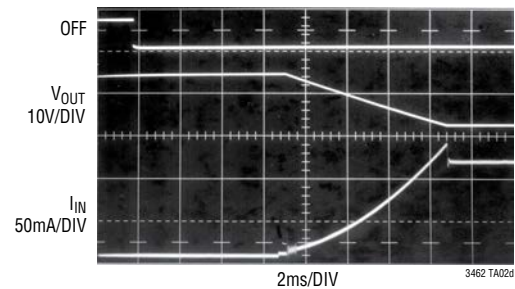
-12V Efficiency



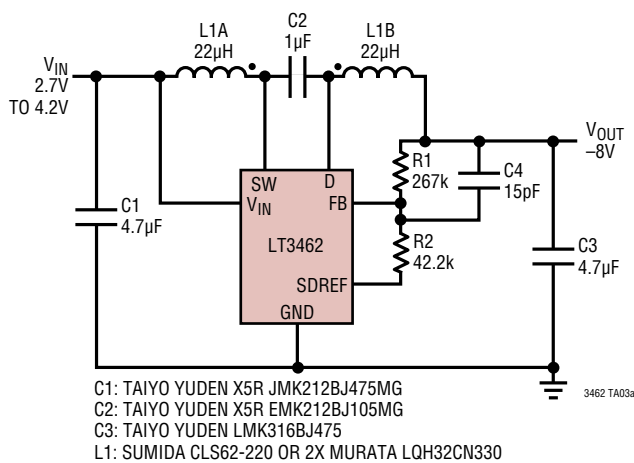
V_{OUT} Reaches -12V in 750µs; Input Current Peaks at 300mA without C_{S1}



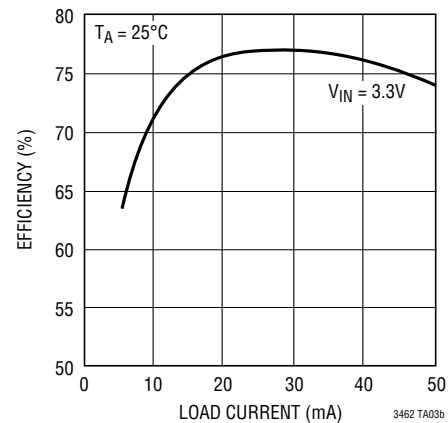
V_{OUT} Reaches -12V in 7.5ms; Input Current Peaks at 125mA with C_{S1} = 100nF



Li⁺ to -8V Supply



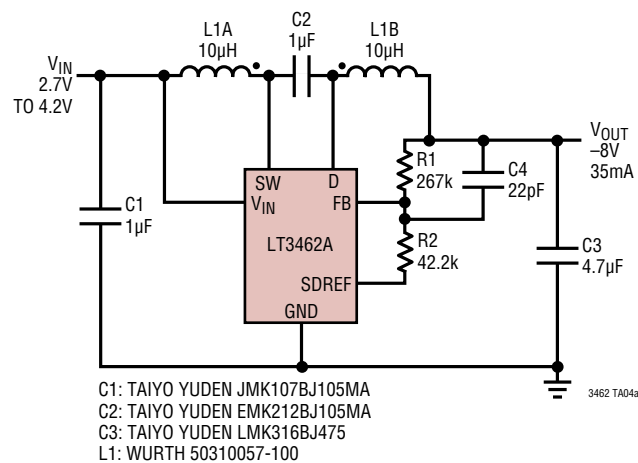
-8V Efficiency



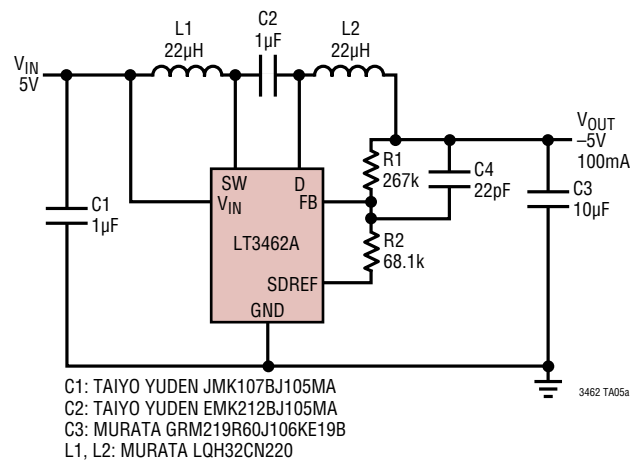
LT3462/LT3462A

TYPICAL APPLICATIONS

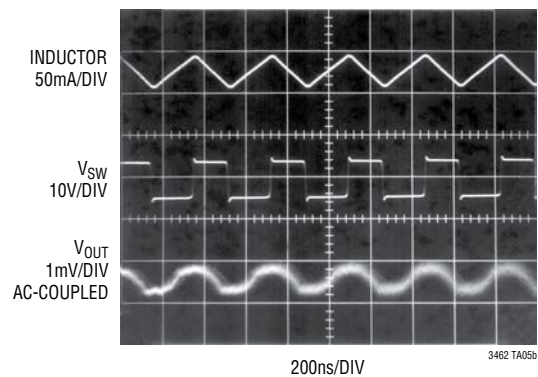
3.3V to -8V (LT3462A)



5V to -5V Supply (LT3462A)



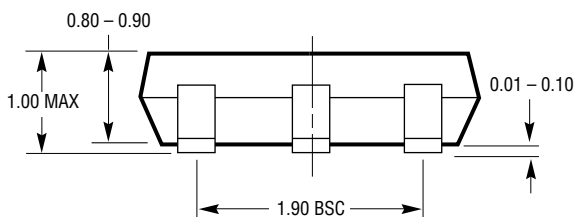
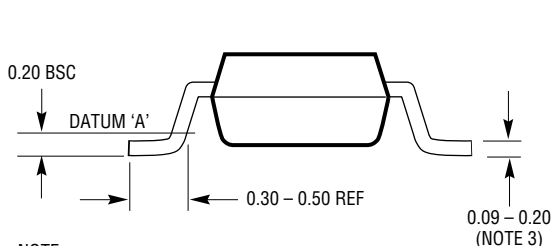
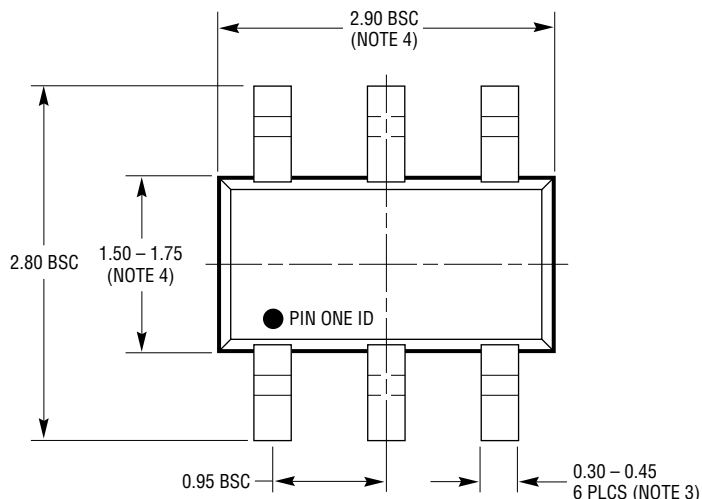
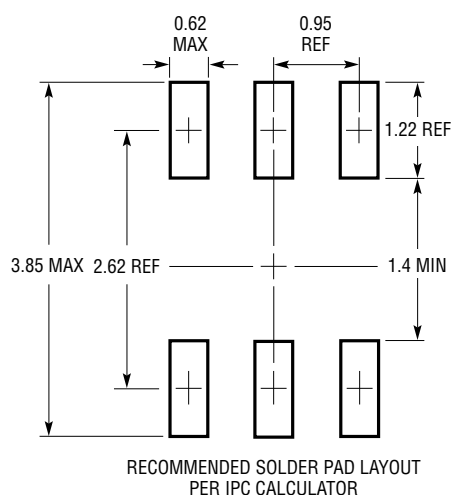
Switching Waveform



PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/product/LT3462#packaging> for the most recent package drawings.

S6 Package 6-Lead Plastic TSOT-23 (Reference LTC DWG # 05-08-1636)



- NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
 2. DRAWING NOT TO SCALE
 3. DIMENSIONS ARE INCLUSIVE OF PLATING
 4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
 5. MOLD FLASH SHALL NOT EXCEED 0.254mm
 6. JEDEC PACKAGE REFERENCE IS MO-193

S6 TSOT-23 0302

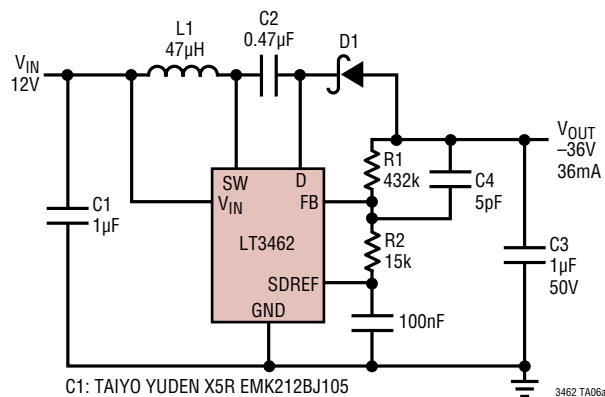
REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	05/18	Add 2mm × 2mm 8-lead DFN package information (A-grade version only) to data sheet	1, 2, 4, 9

LT3462/LT3462A

TYPICAL APPLICATION

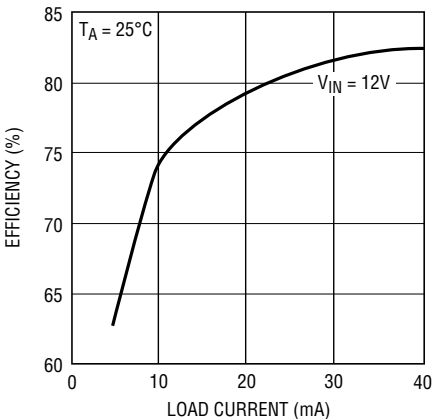
12V to -36V DC/DC Converter



C1: TAIYO YUDEN X5R EMK212BJ105
C2: MURATA GRM42-6X7R474K50
C3: MURATA GRM42-6X7R474K50 x2
D1: CENTRAL CMSH5-4-LTN
L1: MURATA LQH32CN470

3462 TA06a

-36V Efficiency



3462 TA06b

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1617/LT1617-1	350mA/100mA (I_{SW}) High Efficiency Micropower Inverting DC/DC Converter	V_{IN} : 1.2V to 15V, $V_{OUT(MAX)}$ = -34V, I_Q = 20µA, I_{SD} <1µA ThinSOT Package
LT1931/LT1931A	1A (I_{SW}), 1.2MHz/2.2MHz, High Efficiency Micropower Inverting DC/DC Converter	V_{IN} : 2.6V to 16V, $V_{OUT(MAX)}$ = -34V, I_Q = 5.8mA, I_{SD} <1µA ThinSOT Package
LT1945	Dual Output, Boost/Inverter, 350mA (I_{SW}), Constant Off-Time, High Efficiency Step-Up DC/DC Converter	V_{IN} : 1.2V to 15V, $V_{OUT(MAX)}$ = ±34V, I_Q = 40µA, I_{SD} <1µA, MS10 Package
LT1946/LT1946A	1.5A (I_{SW}), 1.2MHz/2.7MHz, High Efficiency Step-Up DC/DC Converter	V_{IN} : 2.45V to 16V, $V_{OUT(MAX)}$ = 34V, I_Q = 3.2mA, I_{SD} <1µA MS8 Package
LT3463	Dual Output, Boost/Inverter, 250mA (I_{SW}), Constant Off-Time, High Efficiency Step-Up DC/DC Converter with Integrated Schottky Diodes	V_{IN} : 2.3V to 15V, $V_{OUT(MAX)}$ = ±40V, I_Q = 40µA, I_{SD} <1µA DFN Package
LT3464	85mA (I_{SW}), High Efficiency Step-Up DC/DC Converter with Integrated Schottky and PNP Disconnect	V_{IN} : 2.3V to 10V, $V_{OUT(MAX)}$ = 34V, I_Q = 25µA, I_{SD} <1µA ThinSOT Package

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[DC670A](#) [LT3462AEDC#TRMPBF](#) [LT3462AEDC#TRPBF](#)