5.5V 6A Low-I_Q Monolithic Buck-Boost DC/DC Converter

FEATURES

- **Single Inductor Buck-Boost Architecture**
- **Low Noise Buck-Boost Architecture**
- **Wide V_{IN} Range 1.8V to 5.5V**
- **Adjustable V_{OUT} Range 1.8V to 5.5V**
- **5A of Continuous Output Current with $V_{IN} > V_{OUT}$**
- **Up to 97% Efficiency**
- Selectable Internal 2.2MHz Fixed Frequency Adjustable and Synchronizable: Up to 4MHz
- Burst Mode® I_Q 17µA for High Efficiency at Light Loads
- Programmable Soft-Start and V_{IN} UVLO
- Simple Solution with Minimal External Components
- Small 3mm × 3mm × 0.74mm LQFN package

APPLICATIONS

- Portable Inventory Terminals
- Handheld Computers
- Medical and Industrial Instruments
- Wireless RF Transmitter
- Backup Power Applications
- Battery Powered Systems

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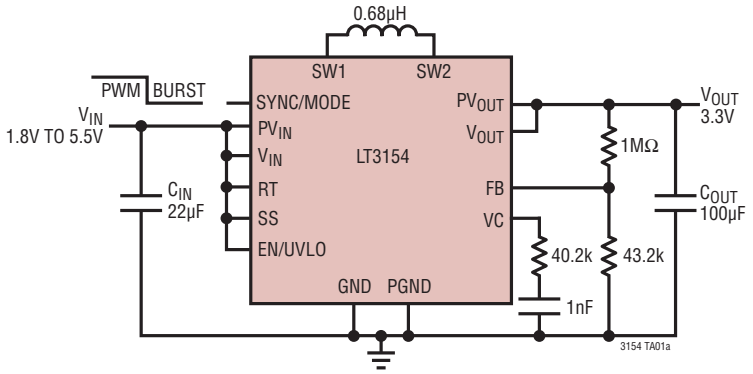
DESCRIPTION

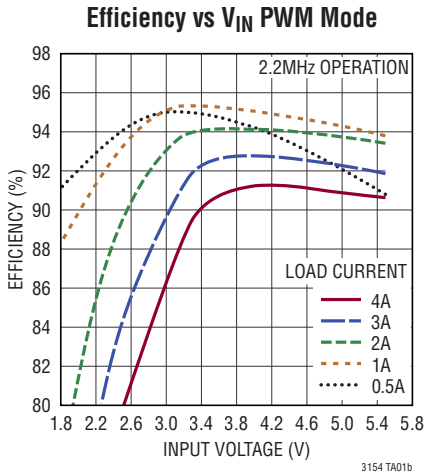
The LT®3154 is a highly efficient, high current, buck-boost DC/DC converter that operates from input voltages above, below or equal to the regulated output voltage. The LT3154's advanced topology provides a continuous transfer through all operating modes. V_{IN} operation from 1.8V to 5.5V provides flexibility for a wide variety of power sources. The output voltage is adjustable between 1.8V to 5.5V.

To minimize external components the LT3154 can be configured to operate from a 2.2MHz internal oscillator. To optimize applications for highest efficiency or smallest footprint the oscillator can be programmed between 500kHz to 4MHz, or synchronized to an external clock for noise sensitive circuits.

Selectable Burst Mode operation reduces quiescent current to 17µA, ensuring high efficiency across the entire load range. The V_{IN} start-up threshold (UVLO) can be adjusted for various input sources. An internal or externally programmable soft-start limits inrush current during start-up. Other features include <1µA shutdown current, short circuit, and thermal overload protection. The LT3154 is housed in the thermally enhanced 16-lead (3mm × 3mm × 0.74mm) LQFN package.

TYPICAL APPLICATION





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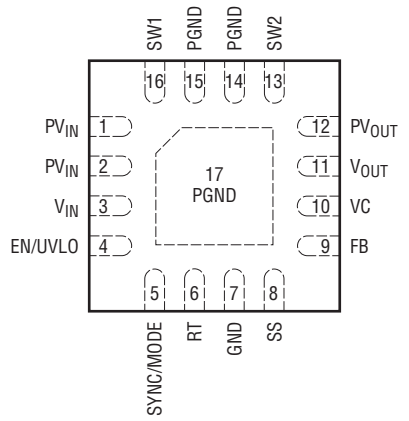
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltages
PV_{IN}, V_{IN}, PV_{OUT}, V_{OUT} ..... –0.3V to 6V
SW1, SW2 Voltage (Notes 4, 6)
DC..... –0.3V to 6V
PULSED (<100ns) .....–1.0V to 7V
All Other Pins..... –0.3V to 6V
Operating Junction Temperature Range (Notes 2, 3, 5)
LT3154A ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

PIN CONFIGURATION



LQFN PACKAGE
16-LEAD (3mm × 3mm × 0.75mm)
T_{JMAX} = 150°C, DEMOBOARD θ_{JA} = 22°C/W
θ_{JC} = 6°C/W, JEDEC θ_{JA} = 30°C/W (NOTE 5)
EXPOSED PAD (PIN 17) IS PGND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

PART NUMBER	TAPE AND REEL	PAD OR BALL FINISH	PART MARKING*		PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE (SEE NOTE 2)
			DEVICE	FINISH CODE			
LT3154AV#PBF	LT3154AV#TRPBF	Au (RoHS)	LHGJ	e4	LQFN (Laminate Package with QFN Footprint)	3	–40°C to 125°C

- Contact the factory for parts specified with wider operating temperature ranges. *Pad or ball finish code is per IPC/JEDEC J-STD-609.
- Parts ending with PBF are RoHS and WEEE compliant.
- The LT3154 package has the same footprint as a standard 3mm × 3mm QFN Package.
- For more information on tape and reel specifications, go to: Tape and reel specifications.
- Recommended LGA and BGA PCB Assembly and Manufacturing Procedures
- LGA and BGA Package and Tray Drawings

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2), PV_{IN} = V_{IN} = 3.6V, PV_{OUT} = V_{OUT} = 3.3V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN} Operating Voltage	EN/UVLO > 1.245V	●	1.8		5.5	V
V_{OUT} Operating Voltage	Adjustable Version with External Divider	●	1.8		5.5	V
Feedback Voltage		●	0.97	0.99	1.01	V
V_{IN}/V_{OUT} Currents						
PWM Mode No-Load Current – V_{IN}				20		mA
Sleep Quiescent Current – V_{IN}	SYNC/MODE = 0V, V_{OUT} in Regulation, Non-Switching			17	30	µA
Sleep Quiescent Current – V_{OUT}	SYNC/MODE = 0V			1	2	µA
Shutdown Current – V_{IN}	EN/UVLO = 0V			0.5	2	µA
Current in UVLO – V_{IN}	EN/UVLO = 1.05V			8	25	µA
EN/UVLO Operation						
EN/UVLO Pin Rising Threshold		●	1.155	1.2	1.245	V
EN/UVLO Pin Falling Threshold		●	1.055	1.1	1.145	V
EN/UVLO Pin Input Leakage Current	EN/UVLO = 5.5V			1	50	nA
EN/UVLO Pin Shutdown Threshold	EN/UVLO Pin Voltage	●	0.2	0.75	1.05	V
Switch Operation						
Average Inductor Current Limit		●	5.4	6.8	8.7	A
Peak Inductor Current Limit			8	9.7	12	A
I_{ZERO} Current	SYNC/MODE = 0V		–0.3	0	0.3	A
Reverse Inductor Current Limit	SYNC/MODE = 3.6V		–1.8	–1.2	–0.9	A
Lowside (B & C) MOSFET $R_{DS(ON)}$	V_{IN} = 3.6V, V_{OUT} = 3.0V			18		mΩ
Highside (A & D) MOSFET $R_{DS(ON)}$	V_{IN} = V_{OUT} = 3.6V			25		mΩ
Lowside MOSFETs Leakage Currents	V_{SW} = 5.5V, EN/UVLO = 0			0.05	2	µA
Highside MOSFETs Leakage Current	V_{IN} = V_{OUT} = 5.5V, V_{SW1} = V_{SW2} = 0V, EN/UVLO = 0			0.1	10	µA
Oscillator Operation						
Switching Frequency	RT to V_{IN} or R_T = 49.9kΩ	●	1.8	2.2	2.6	MHz
Switching Frequency Range	R_T Programmable	●	0.5		4	MHz
Max Boost Duty Cycle (SW2 Low)	R_T = V_{IN}, FB = 0.94V	●	83	88	95	%
Min Duty Cycle (SW1 High)	R_T = V_{IN}, FB = 1.04V	●			0	%
SYNC/MODE Applied Clock Frequency	R_T Chosen to Program a 25% Lower Frequency	●	0.5		4	MHz
SYNC/MODE High or Low Pulse Width			75			ns
SYNC/MODE Input High Logic Level		●	1.5			V
SYNC/MODE Input Low Logic Level		●			0.5	V
SYNC/MODE Input Leakage Current	SYNC/MODE = 5.5V			1	50	nA
Soft-Start						
Soft-Start Period (C_{SS} Charge Time to 0.8V)	SS = V_{IN} or C_{SS} = 2.7nF			2.2		ms
External SS Regulation Voltage	Capacitor to GND Sets SS Time			1.0		V
Voltage GM Amp						
Feedback Pin Input Current	FB = 1V			0	50	nA
V_C Source/Sink Current	FB = 0.9V Source, FB = 1.1V Sink			±12		µA
Error Amplifier Transconductance	VC Current = ±4µA			110		µS

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT3154 is tested under pulsed load conditions such that $T_J \approx T_A$. The LT3154A is specified over the –40°C to 125°C operating junction temperature. High junction temperatures degrade operating lifetimes; operating lifetime is derated for temperatures greater than 125°C.The maximum ambient temperature is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors. The junction temperature (T_J in °C) is calculated from the ambient temperature (T_A in °C) and power dissipation (P_D in Watts) according to the following formula:

$$T_J = T_A + (P_D) \bullet (\theta_{JA}\ °C/W)$$

Where θ_{JA} is the package thermal impedance. Note the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

Note 3: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. The maximum rated junction temperature will be exceeded when this protection is active. Continuous operation above the maximum operating junction temperature may impair device reliability or permanently damage the device.

Note 4: Specification is guaranteed by design and not 100% tested in production.

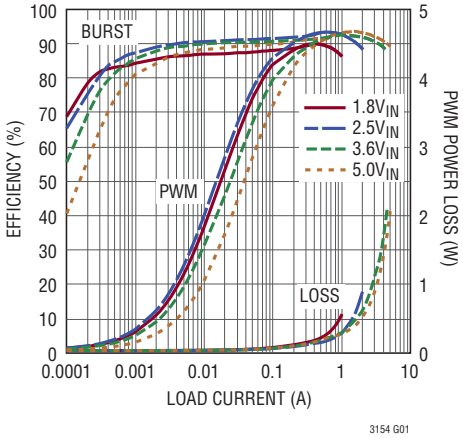
Note 5: Failure to solder exposed backside of the package to the PC Board will result in a higher thermal resistance

Note 6: Voltage transients on the switch pins beyond the DC limits specified in Absolute Maximum Ratings are non-disruptive to normal operation when using good layout practices as described elsewhere in the data sheet and as seen on the demo board.

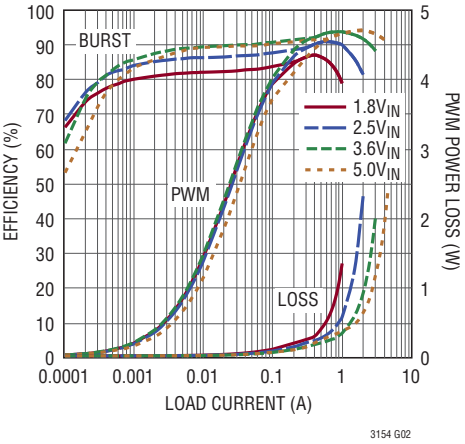
TYPICAL PERFORMANCE CHARACTERISTICS

(T_A = 25°C, V_{IN} = 3.6, V_{OUT} = 3.3V unless otherwise specified)

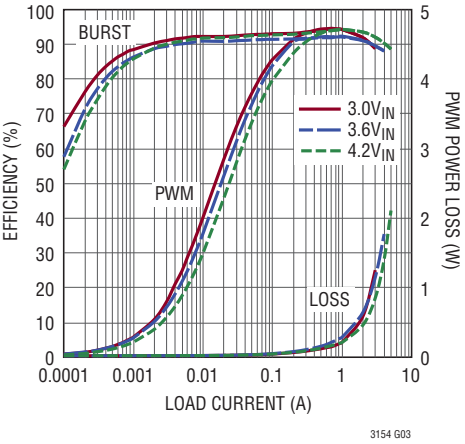
Efficiency/Power Loss at 2.2MHz 1.8V, 2.5V, 3.6V, 5.0V to 3.3V_{OUT}, L = 0.68µH



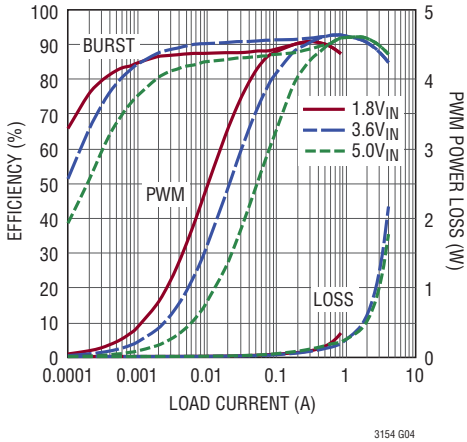
Efficiency/Power Loss at 2.2MHz 1.8V, 2.5V, 3.6V, 5.0V to 5.0V_{OUT}, L = 0.68µH



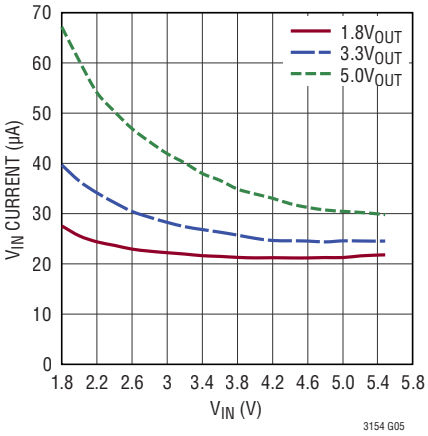
Efficiency/Power Loss at 1.2MHz Li-Ion (3.0V, 3.6V, 4.2V) to 3.3V_{OUT}, L = 1µH



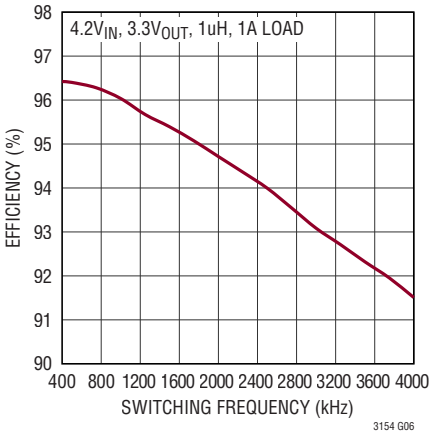
Efficiency/Power Loss at 2.2MHz 1.8V, 3.6V, 5.0V to 2.5V_{OUT}, L = 0.68µH



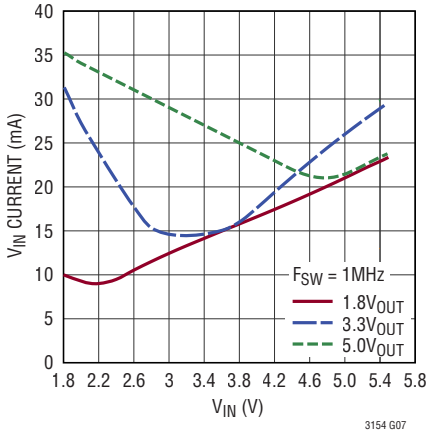
Burst Mode Operation No-Load Input Current vs V_{IN}



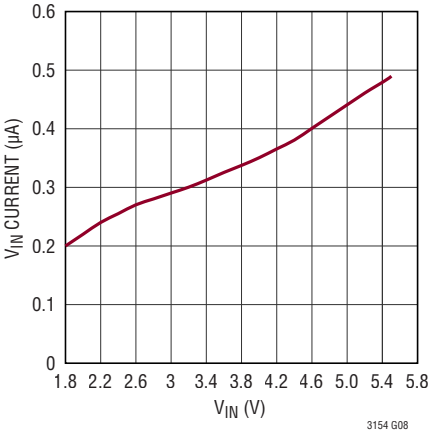
PWM Mode Efficiency vs f_{SW}



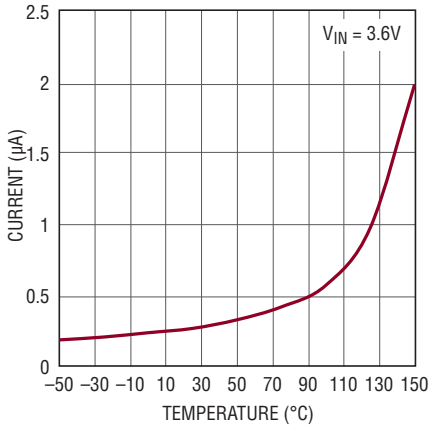
PWM Mode No-Load Input Current vs V_{IN}



Shutdown vs V_{IN}



V_{IN} Current in Shutdown Current vs Temperature



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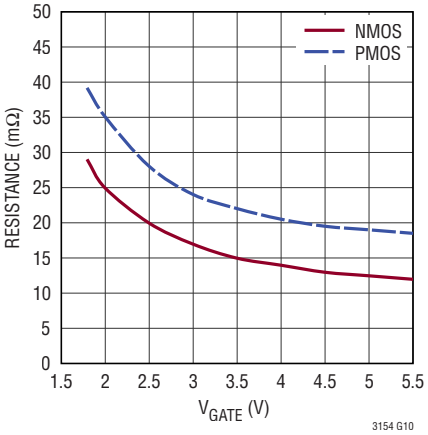
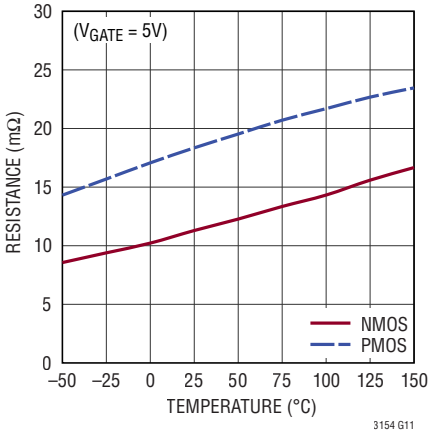
TYPICAL PERFORMANCE CHARACTERISTICS

(T_A = 25°C, V_{IN} = 3.6, V_{OUT} = 3.3V unless otherwise specified)

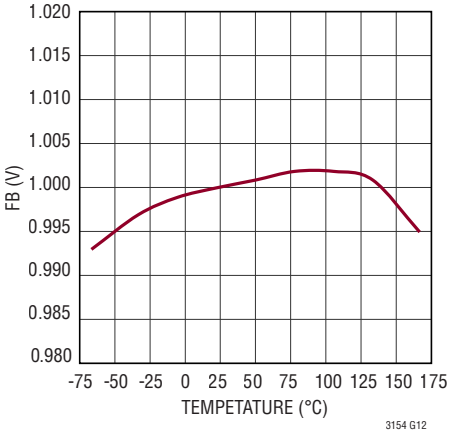
Normalized N-/P-Channel Switch Resistance vs Temperature



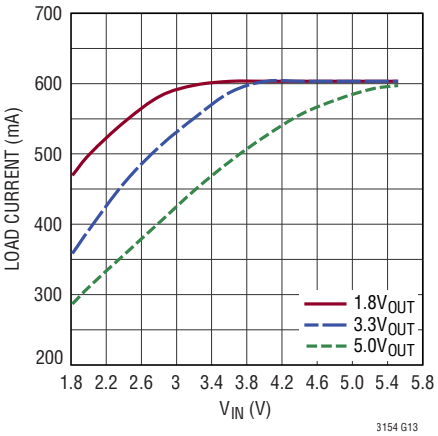
Normalized N-/P-Channel Switch Resistance vs V_{GATE}



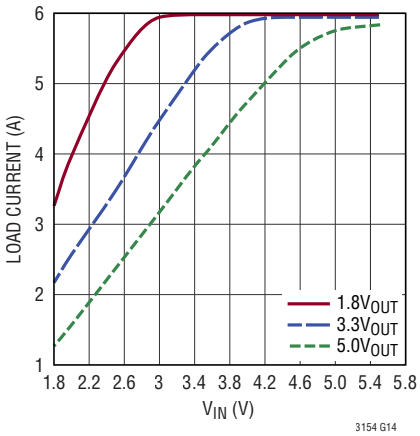
Feedback Voltage vs Temperature



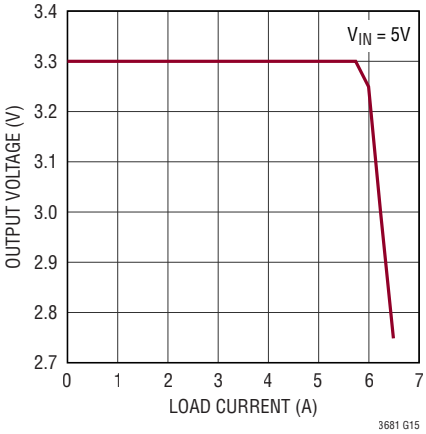
Burst to PWM Mode Thresholds vs V_{IN} and V_{OUT}



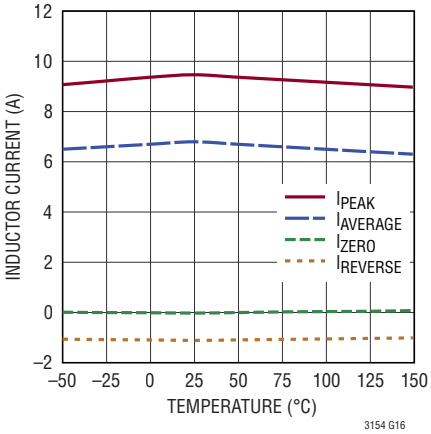
Maximum Load Current in PWM Mode vs V_{IN}



Output Voltage vs I_{LOAD}



Peak, Average, Zero and Reverse Limits vs Temperature

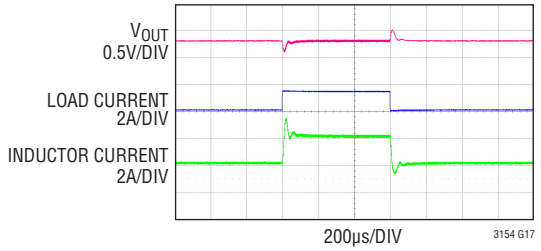


Rev. A

TYPICAL PERFORMANCE CHARACTERISTICS

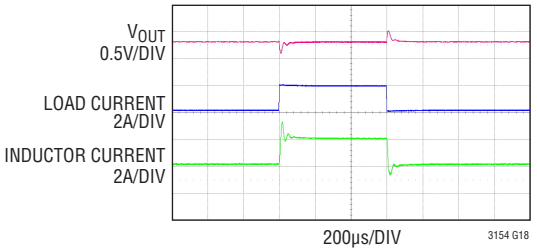
(T_A = 25°C, V_{IN} = 3.6, V_{OUT} = 3.3V unless otherwise specified)

3.3V_{OUT} Load Step, 0.15A to 1.5A, V_{IN} = 2.5V, SYNC/MODE = V_{IN}



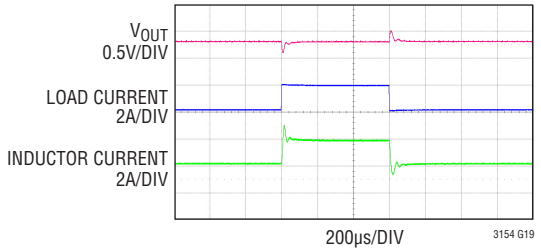
FRONT PAGE APPLICATION

3.3V_{OUT} Load Step, 0.2A to 2A, V_{IN} = 3.3V, SYNC/MODE = V_{IN}



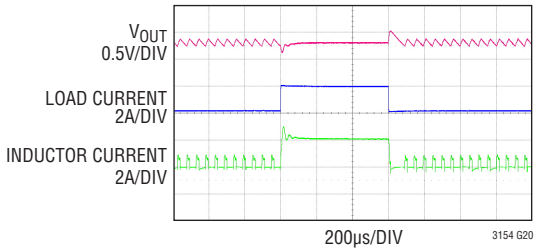
FRONT PAGE APPLICATION

3.3V_{OUT} Load Step, 0.2A to 2A, V_{IN} = 5.0V, SYNC/MODE = V_{IN}



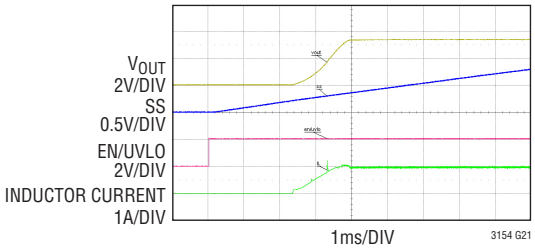
FRONT PAGE APPLICATION

3.3V_{OUT} Load Step, 0.2A to 2A, V_{IN} = 3.3V, SYNC/MODE = 0V



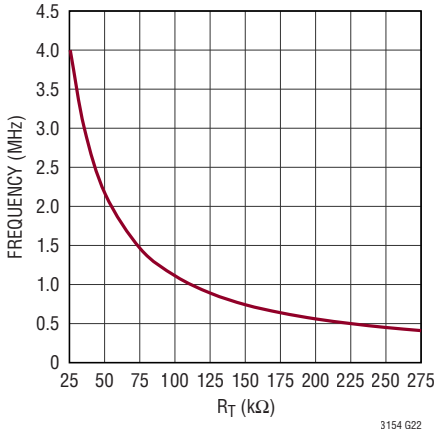
FRONT PAGE APPLICATION

Soft-Start Waveforms 3.3Ω Load



C_{SS} = 10nF

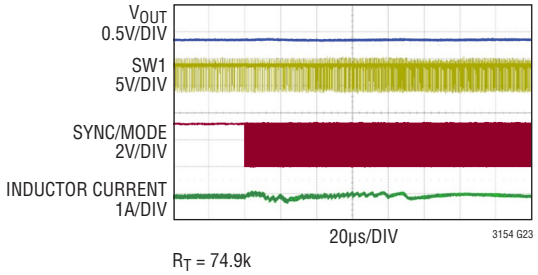
Frequency vs R_T



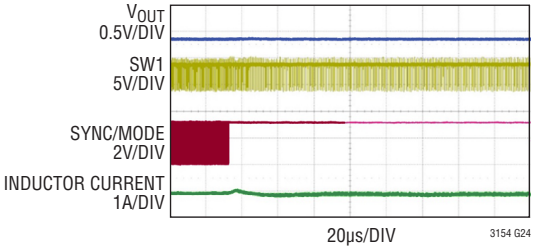
TYPICAL PERFORMANCE CHARACTERISTICS

(T_A = 25°C, V_{IN} = 3.6, V_{OUT} = 3.3V unless otherwise specified)

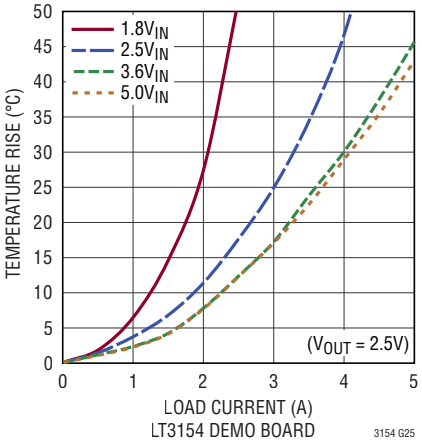
SYNC/MODE Pin Clock Acquisition 1.5MHz to 2.5MHz



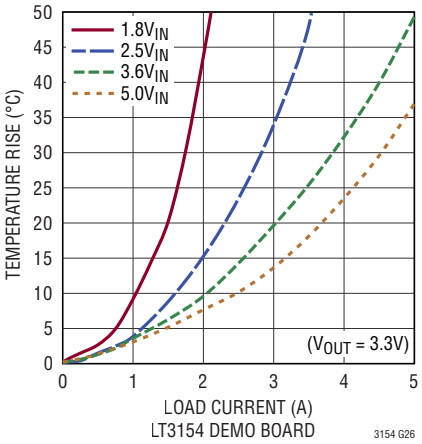
SYNC/MODE Pin Clock Release, 2.5MHz to 1.5MHz



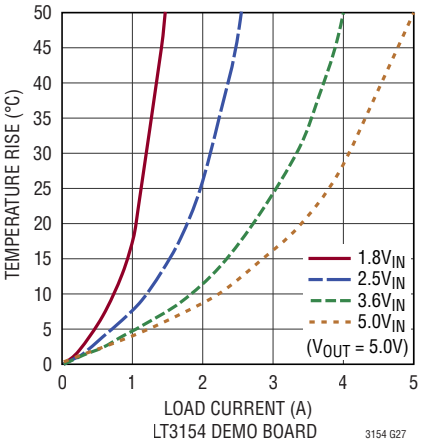
Die Temperature vs Load and V_{IN} at 2.5V_{OUT}, 2.2MHz, L = 0.68µH



Die Temperature vs Load and V_{IN} at 3.3V_{OUT}, 2.2MHz, L = 0.68µH



Die Temperature vs Load and V_{IN} at 5V_{OUT}, 2.2MHz, L = 0.68µH



PIN FUNCTIONS

PV_{IN} (Pins 1, 2): Power Input for Buck-Boost Converter. Connect a minimum 22µF low ESR capacitor to PGND as close to the device as possible. This pin must be connected to V_{IN} in application.

V_{IN} (Pin 3): Signal Input Voltage. Decouple with minimum 1µF capacitor. Low noise input for control circuitry.

EN/UVLO (Pin 4): Input to Enable the IC. Connect EN/UVLO to V_{IN} to enable the LT3154 at the 1.8V minimum operating voltage. Connect to an external divider from V_{IN} to provide a programmable accurate V_{IN} undervoltage threshold:

$$V_{(TURNON)} = 1.2V\left(1+\frac{R1}{R2}\right)$$

The accurate EN/UVLO pin threshold has 100mV of hysteresis provided internally:

$$V_{(TURNOFF)} = 1.1V\left(1+\frac{R1}{R2}\right)$$

SYNC/MODE (Pin 5): Burst Mode operation Select and Oscillator Synchronization. Do not leave this pin floating.

SYNC/MODE = High (V_{IN}). Disable Burst Mode Operation and maintain low noise, constant frequency PWM operation.

SYNC/MODE = Low (GND). The converter operates in Automatic Burst Mode operation.

SYNC/MODE = External CLK. The internal oscillator is synchronized to the external CLK signal, Burst Mode operation is disabled. A clock pulse width between 75ns and *T period* –75ns is required to synchronize the oscillator. An external resistor must be connected between RT and GND to program the oscillator 25% to 50% below the desired synchronization frequency.

RT (Pin 6): Oscillator Frequency Programming Input. Connect to V_{IN} for 2.2MHz fixed frequency operation. Connect an external resistor from RT to GND to program the switching frequency according to the formula:

$$R_T\ (k\Omega) = \frac{110}{f_{SW}\ (MHz)}$$

GND (Pin 7): Signal Ground. Low noise ground for control circuits.

SS (Pin 8): External Soft Start. Connect to V_{IN} for 2.2ms default soft-start period. Connect an external capacitor to set soft start period according to the formula:

$$t_{SS}\ (ms) = 0.8 \times C_{SS}\ (nF)$$

FB (Pin 9): Feedback Input to Error Amplifier. The resistor divider connected to this pin sets the converter output voltage.

$$V_{OUT} = 1.0V\left(1+\frac{R3}{R4}\right)$$

VC (Pin 10): Voltage error amplifier output VC is used to program average inductor current. An R-C from this pin to ground sets the voltage loop compensation.

V_{OUT} (Pin 11): Signal Output Voltage. Decouple with minimum 1µF capacitor. Low noise input for V_{OUT} control circuitry. V_{OUT} must be connected to PV_{OUT} at the IC.

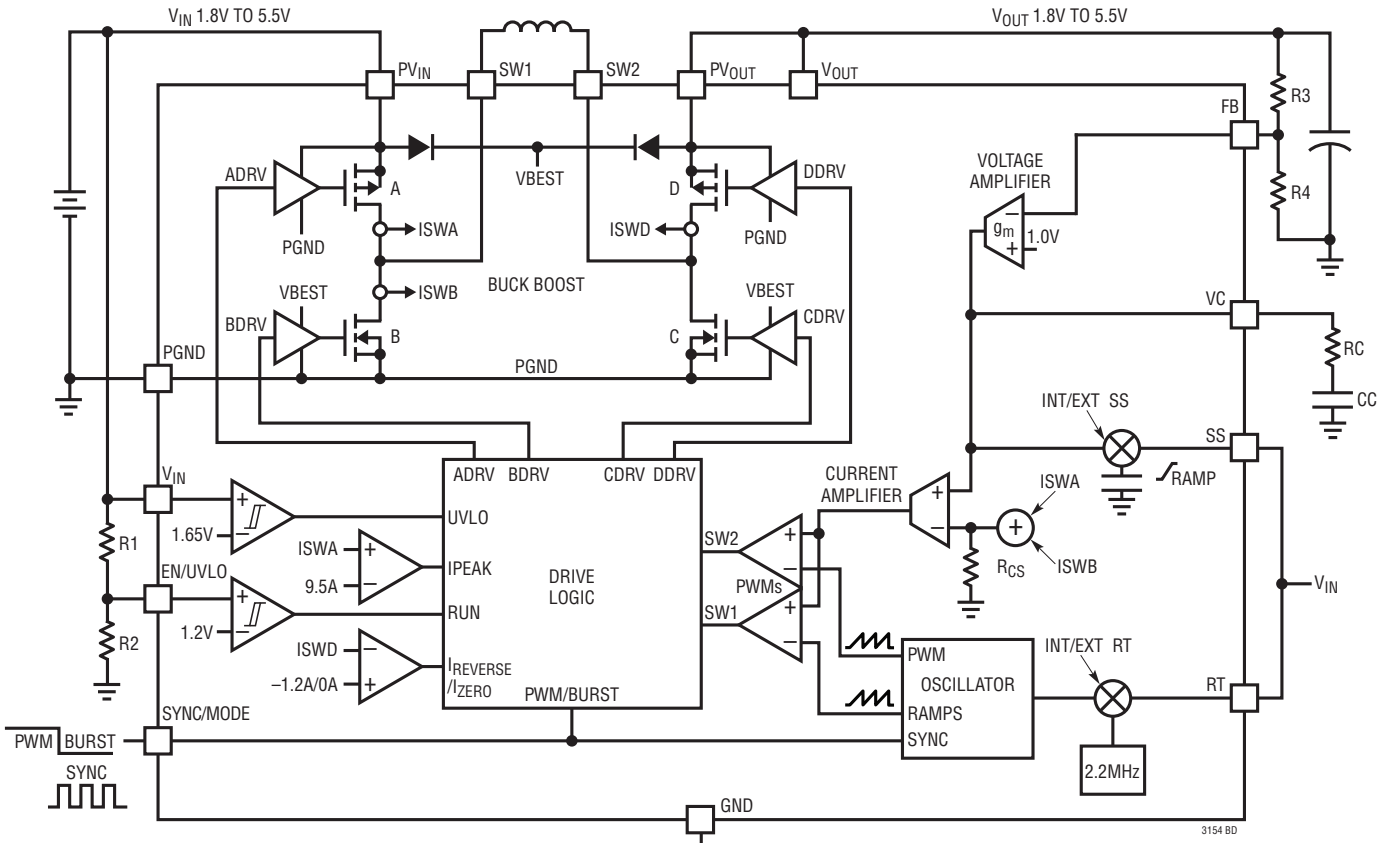
PV_{OUT} (Pin 12): Power Output for Buck-Boost Converter. Connect a minimum 68µF (see Table 3 low ESR capacitor to PGND as close to the device as possible. Capacitor value may change depending on V_{OUT} voltage and load current requirements. This pin must be connected to V_{OUT} in application.

SW2 (Pin 13): Buck-Boost Converter Switch Pin. Connect inductor between SW1 and SW2 pins.

PGND (Pins 14, 15, 17-Exposed Pad): Power Ground Connection. These pins and exposed thermal pad must make full connection to PCB ground plane to meet specified thermal requirements. PGND must be connected to the GND pin in the application.

SW1 (Pin 16): Buck-Boost Converter Switch Pin. Connect inductor between SW1 and SW2 pins.

BLOCK DIAGRAM



NOTE: PV_{IN} AND V_{IN} MUST BE CONNECTED TOGETHER IN THE APPLICATION
PV_{OUT} AND V_{OUT} MUST BE CONNECTED TOGETHER IN THE APPLICATION
PGND AND GND MUST BE CONNECTED TOGETHER IN THE APPLICATION

QUICK REFERENCE

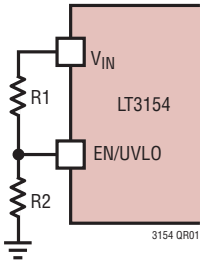
This section of the data sheet contains equations for external component selection for the LT3154 where applicable.

V_{IN} UVLO Threshold

The V_{IN} threshold is internally set to a typical value of 1.7V for turn-on and 1.6V for turn-off when EN/UVLO is connected to V_{IN}. The V_{IN} UVLO can be adjusted to a higher threshold voltage with a resistor network on EN/UVLO according to the following equations:

$$V_{(TURNON)} = 1.2V\left(1+\frac{R1}{R2}\right)$$

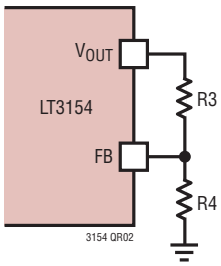
$$V_{(TURNOFF)} = 1.2V\left(1+\frac{R1}{R2}\right)$$



Output Voltage Programming

The output voltage for the LT3154 is set via a resistor divider connected at the FB pin:

$$V_{OUT} = 1.0V\left(1+\frac{R3}{R4}\right)$$



In most applications, choosing R4 equal to 1Meg represents a good trade-off between quiescent current and robustness against PCB leakage. The minimum recommended V_{OUT} setting is 1.8V, the maximum is 5.5V.

Switching Frequency

The buck-boost converter switching frequency, f_{SW}, is set by the value of the R_T resistor connected between the RT pin and ground according to the following equation. Connecting the RT pin to V_{IN} will set a default frequency of 2.2MHz.

$$f_{SW}(MHz) = \frac{110}{R_T}(k\Omega)$$

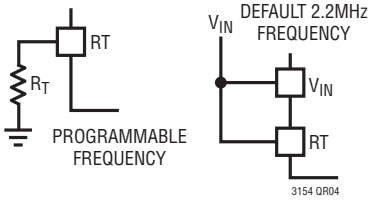


Table 1. R_T Value for Common Switching Frequencies

f_{SW}	R_T
500kHz	221kΩ
750kHz	147kΩ
1.0MHz	110kΩ
2.0MHz	54.9kΩ
2.2MHz	Connect to V_{IN}
3.0MHz	36.5kΩ
4.0MHz	27.4kΩ

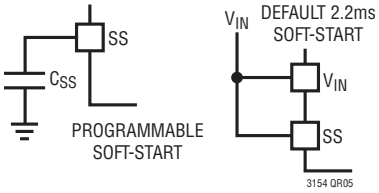
QUICK REFERENCE

The buck-boost converter can be synchronized to an external clock applied to the SYNC/MODE pin. The frequency of the external clock must be higher than the internal oscillator frequency as set by the RT pin. In order to accommodate the ±18% possible variation in the oscillator frequency, the R_T resistor should be chosen to set the internal oscillator frequency between 25% to 50% below the lowest synchronization frequency. For example, to synchronize to an external 2.5MHz clock, R_T should be selected to set the internal oscillator at 1.9MHz or lower.

Soft-Start Period

The soft-start circuit linearly ramps the average inductor current during the soft-start period (t_{SS}) from 0A up to 6A. An internal soft-start interval of approximately 2.2ms can be selected by connecting SS to V_{IN}. For applications requiring a longer soft-start period, an external capacitor C_{SS} on SS sets soft-start period according to the formula:

$$t_{SS}(ms) = 0.8 \bullet C_{SS}(nF)$$



In most applications, the initial load current at V_{OUT} requires only a fraction of the 6A maximum current limit, resulting in V_{OUT} achieving regulation in a fraction of the soft-start period. Table 2 gives approximate times for V_{OUT} to regulate for various C_{SS} values and initial load currents in buck mode.

Table 2. Approximate Time for V_{OUT} to Achieve Regulation vs Load Current and C_{SS}

Load Current	0.1A	1A	2A	4A
C_{SS} Value	V_{OUT} in Regulation Time (ms)			
SS to V_{IN}	0.5	0.75	1	1.5
10nF	2	3	4	6
47nF	10	15	20	30

Inductor Value

While the ideal inductor value is influenced by many factors, in most cases, the maximum value is dictated by the right-half plane zero (RHPZ) frequency at high load current in boost mode based on the following equation:

$$L < \frac{V_{IN}^2 \bullet R_L}{V_{OUT}^2 \bullet 2\pi \bullet f_{RHPZ}}$$

The internal control loop crossover frequency varies between 5kHz to 15kHz in boost mode. To get adequate frequency separation, the inductor value should be chosen to give a RHPZ frequency > 100kHz. A 0.47µH to 1µH inductor works well for most applications and load currents with switching frequencies above 1MHz. Applications with switching frequencies below 1MHz may require larger inductor values and control loop adjustments, at the V_C pin, to lower the crossover frequency to avoid the RHPZ.

Output Capacitor Value

The recommended minimum output capacitor, C_{MIN}, is given below as a function of output voltage:

$$C_{MIN} = \frac{1V}{V_{OUT}} 330\mu F$$

Table 3. Minimum Output Capacitor vs V_{OUT}

V_{OUT}	Minimum C_{OUT}
5	68µF
3.3	100µF
1.8	200µF

Control Pin Voltage Limitations

1. SYNC/MODE and EN/UVLO are low voltage input pins and cannot be forced above 6V.
2. The RT and SS pins should be connected to V_{IN} to select default values or to GND though the appropriate external resistor or capacitor when programmed.

OPERATION

Introduction

The LT3154 is a 6A synchronous buck-boost DC/DC converter optimized for demanding high current applications. The low $R_{DS(ON)}$, low gate charge synchronous switches provide, highly efficient, high frequency pulse width modulation control. The LT3154 utilizes a proprietary low noise switching algorithm, which allows its output voltage to be regulated above, below or equal to the input voltage.

Burst Mode capability is included in the LT3154 and is user-selected via the SYNC/MODE input pin. In Burst Mode operation, the LT3154 provides exceptional efficiency at light output loads by operating the converter only when necessary to maintain voltage regulation. At higher loads, the LT3154 automatically transitions to fixed frequency PWM operation. Continuous PWM mode can also be selected via the SYNC/MODE pin for low noise operation.

The LT3154 features an accurate, resistor programmable EN/UVLO comparator which allows the buck-boost DC/DC converter to turn on and off at user-selected voltage thresholds depending on the power source. Other programmable features include the soft-start period, oscillator frequency and output voltage. Default values for each feature can selected by connecting pins to V_{IN} or GND, reducing external component count.

Power Stage Topology

The switch topology for the buck-boost converter is shown in Figure 1. When the input voltage is significantly greater than the output voltage, the buck-boost converter operates in buck mode. Switch D turns on continuously and switch C remains off. Switches A and B are pulse width modulated to produce the required duty cycle to support the output regulation voltage. As the input voltage decreases, switch A remains on for a larger portion of the switching cycle. As the input voltage approaches the output voltage, the period of switch B will shorten and switch C will begin to turn on to maintain regulation. The voltages where this transition region occur will vary depending on load current and switching frequency. Additional inductor current ripple may occur as SW1 and SW2 begin to transition on/off near the edges of their respective PWM ramps (see block diagram). As the input voltage drops below the output voltage, switch A remains on continuously while switch pair CD is pulse width modulated to obtain the desired output voltage. At this point, the converter is operating solely in boost mode.

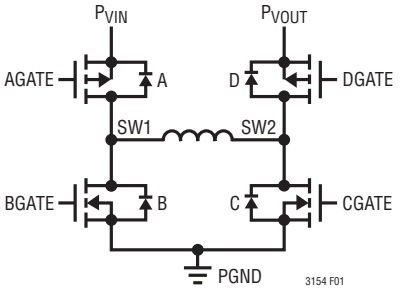


Figure 1. Buck-Boost Switch Topology

This switching algorithm provides a smooth transition between operating modes and reduces discontinuities in average inductor current, inductor current ripple, and loop transfer function throughout all three operational modes. These advantages result in increased efficiency and stability in comparison to the traditional four-switch buck-boost converter.

PWM Mode Operation

If the SYNC/MODE pin is high or if the load current on the converter is high enough to force PWM mode operation, the LT3154 operates at a fixed frequency programmed by the RT pin. PWM mode minimizes output voltage ripple and yields a low noise switching frequency spectrum. A proprietary switching algorithm provides seamless transitions between operating modes and eliminates discontinuities in the average inductor current, inductor ripple current and loop transfer function throughout all modes of operation. These advantages result in increased efficiency, improved loop stability, and lower output voltage ripple. In response to the internal control loop command, an internal pulse width modulator generates the appropriate switch duty cycle to maintain regulation of the output voltage.

OPERATION

Automatic Burst Mode Operation

When the SYNC/MODE pin is held low, the LT3154 is configured for automatic Burst mode operation. As a result, the buck-boost DC/DC converter will operate with normal continuous PWM switching above a predetermined average inductor current and will automatically transition to power saving Burst mode operation below this level. Refer to the Typical Performance Characteristics section of this data sheet to determine the Burst mode transition threshold for various combinations of V_{IN} and V_{OUT}. With SYNC/MODE low, at light output loads, the LT3154 will go into a standby or sleep state when the output voltage achieves its nominal regulation level. The sleep state halts PWM switching and powers down all non-essential functions of the IC, significantly reducing the quiescent current of the LT3154. This greatly improves overall power conversion efficiency when the output load is light. Since the converter is not operating in sleep, the output voltage will slowly decay at a rate determined by the output load resistance and the output capacitor value. When the output voltage has decayed by a small amount, typically 1% to 2%, the LT3154 will wake up and resume normal PWM switching operation until the voltage on V_{OUT} is restored to the previous level. If the load is very light, the LT3154 may only need to switch for a few cycles to restore V_{OUT} and may sleep for extended periods of time, significantly improving efficiency.

Average Current Mode Control

The LT3154 utilizes Average Current mode control for the pulse width modulator as shown in Figure 2. Current mode control, both average and the better known peak method, enjoy some benefits compared to other control methods including: simplified loop compensation, rapid response to load transients and inherent line voltage rejection.

Referring to Figure 2, an internal high gain transconductance error amplifier labeled V_AMP monitors V_{OUT} through a voltage divider connected to the FB node and

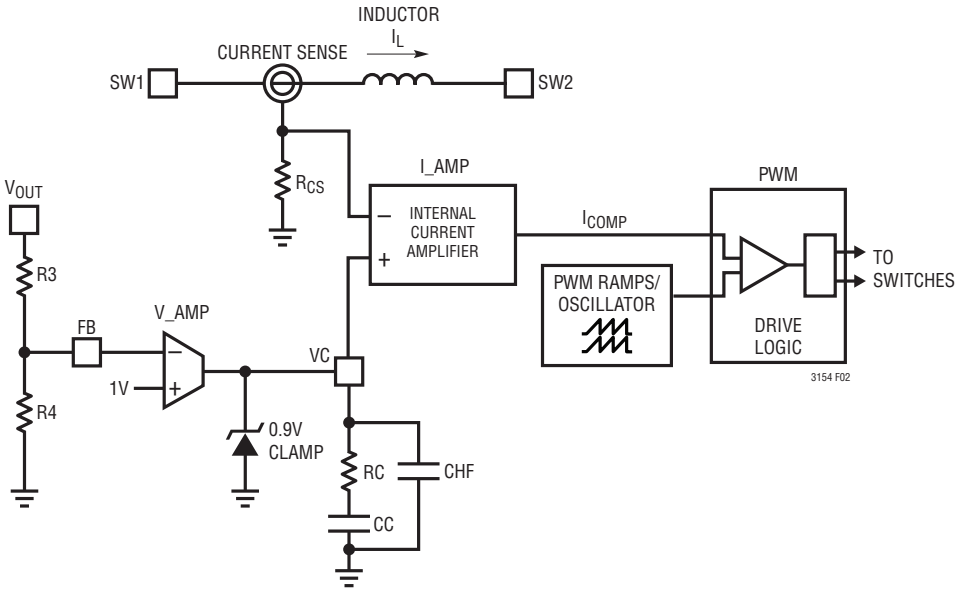


Figure 2. Average Current Mode Control Loop

OPERATION

generates an output, VC, used by the current mode control loop to command the appropriate inductor current level. To ensure stability, external frequency compensation components (RC, CC and CHF) must be installed between VC and GND. The procedure for determining these components is provided in the Applications Section of this data sheet.

VC is internally connected to the non-inverting input of a second amplifier, referred to in Figure 2 as I_AMP. The inverting input of the average current amplifier is connected to the inductor current sense resistor R_{CS} with a 200mV offset. I_AMP contains an internal averaging filter and frequency compensation network to stabilize operation of the internal current loop. The average current amplifier's output (I_{COMP}) provides the cycle-by-cycle duty cycle command into the buck-boost PWM circuitry.

The non-inverting reference level input to the average current amplifier is VC and the feedback or inverting input is driven from the inductor current sensing circuitry. The inductor current sensing circuitry alternately measures the current through switches A and B. The output of the sensing circuitry produces a voltage across resistor R_{CS} that resembles the inductor current waveform transformed to a voltage. If there is an increase in the power converter load on V_{OUT}, the instantaneous level of V_{OUT} will drop slightly, which will increase the voltage level on VC by the inverting action of the voltage error amplifier. When the increase on VC first occurs, the output of the current averaging amplifier, I_{COMP}, will increase momentarily to command a larger duty cycle. This duty cycle increase will result in a higher inductor current level, ultimately raising the average voltage across R_{CS}. Once the average value of the voltage on R_{CS} is equivalent to the VC level, the voltage on I_{COMP} will revert very closely to its previous level into the PWM and force the correct duty cycle to maintain voltage regulation at this new higher inductor current level. The average current amplifier is configured, so in steady state, the average value of the voltage applied to its inverting input (voltage across R_{CS}) will be equivalent to the voltage on its non-inverting input VC. As a result, the average value of the inductor current is controlled in order to maintain voltage regulation. The entire current amplifier and PWM can be simplified as a voltage controlled current source, with the driving voltage coming from VC.

The voltage error amplifier monitors V_{OUT} through a voltage divider and makes adjustments to the current command as necessary to maintain regulation. The voltage error amplifier therefore controls the outer voltage regulation loop. The average current amplifier makes adjustments to the inductor current as directed by the voltage Error Amplifier output via VC and is commonly referred to as the inner current loop amplifier. The average current mode control technique is similar to peak current mode control except that the average current amplifier controls average current instead of the peak current. This difference eliminates the peak to average current error inherent to peak current mode control, while maintaining most of the advantages inherent to peak current mode control. Control loop compensation techniques are detailed in the Applications section of this data sheet.

Inductor Current Sense and Maximum Output Current

As part of the current control loop, the LT3154 has current sense circuitry that measures the inductor current of the buck-boost converter as shown in Figure 2. This circuitry measures the current through switches A and B separately and produces proportional output currents that are summed at the current sense resistor R_{CS}. Sensed A and B switch currents form a voltage replica of the inductor current at R_{CS}, which is used by the average current amplifier as described in the Quick Reference section.

The voltage amplifier output, VC, is internally clamped to a nominal value of 0.9V. Since the average inductor current is proportional to VC, the 0.9V clamp sets the maximum average inductor current that can be programmed by the inner current loop. Taking into account the current sense amplifier's gain and the value of R_{CS}, the maximum average inductor current is 6.8A typical.

OPERATION

In buck mode, the output current is approximately equal to the inductor current I_L:

$$I_{OUT(BUCK)} \approx I_L$$

In boost mode, the output current is related to average inductor current and duty cycle by:

$$I_{OUT(BOOST)} \approx I_L \bullet (1\text{-}D)$$

where D is the converter duty cycle

Since the output current in boost mode is reduced by the duty cycle (D), the output current rating in buck mode is always greater than in boost mode. Also, because boost mode operation requires a higher inductor current for a given output current compared to buck mode, the efficiency in boost mode will be lower due to higher conduction ($I_L^2 \times R_{DS(ON)}$) losses in the power switches. This will further reduce the output current capability in boost mode. In either operating mode, however, the inductor peak-to-peak ripple current does not play a major role in determining the output current capability, unlike peak current mode control.

The maximum output current capability in PWM mode curves in the Typical Performance Characteristics section show the relationship of input voltage and the ability to deliver load current at V_{OUT} = 3.3V. If V_{OUT} drops below approximately 1V, the inductor current will be reduced by approximately 50% to limit power dissipation during a short circuit.

Peak, Reverse and Zero Current Comparators

The internal current sense waveforms are used by the Peak (I_{PEAK}), Reverse ($I_{REVERSE}$) and Zero current (I_{ZERO}) comparators. The I_{PEAK} current comparator monitors I_{SENSE} and interrupts normal PWM operation if the inductor current level exceeds its maximum internal threshold. This threshold is approximately 33% above the maximum average current level of the current control loop or 9.5 Amps. If the internal current sense waveform rises above this level, the LT3154 will disconnect the inductor from V_{IN} by shutting off switch A to prevent higher current in the inductor. The I_{PEAK} circuitry is reset by the oscillator clock at the end of each switching cycle. In the event that the I_{PEAK} comparator is tripped as the result of an output short circuit condition, where V_{OUT} is discharged below approximately 1V, the LT3154 will initiate a soft-start event keeping the on-chip power dissipation to low levels. Once the short circuit is removed, the LT3154 will restart in the normal fashion. If the average current loop is able to prevent inductor current from reaching I_{PEAK} during a short circuit event, soft-start will not be initiated, but the maximum current capability of the current loop will be reduced by 50% to reduce power dissipation.

In addition to controlling the maximum inductor current, the LT3154 contains sense circuitry on the D switch to limit the reverse current as well. The amount of reverse current allowed depends on the mode of operation. In PWM mode (SYNC/MODE = 1), the typical reverse current limit is –1.2A, providing clean, fixed frequency switch operation at light loads and during load step transients. In BURST mode (SYNC/MODE = 0), the LT3154 operates with a traditional zero current comparator, maintaining high efficiency at light loads and during burst packet intervals. Once $I_{REVERSE}$ or I_{ZERO} is detected, the D switch is shut off for the remainder of the switching cycle and reset by the oscillator clock at the end of the cycle.

Oscillator

The frequency of operation is programmed by an external resistor from the RT pin to ground, according to the following equation:

$$R_T(k\Omega) = \frac{110}{f_{SW}(MHz)}$$

The recommended frequency range is between 500kHz and 4MHz, allowing efficiency and external component sizes to be optimized for each application. An internal 2.2MHz oscillator frequency can be selected by connecting RT to V_{IN}, eliminating the need for an external R_T resistor. The LT3154 can also be synchronized to an external clock source using the SYNC/MODE pin and an internal phase lock loop (PLL). If synchronization to an external source is desired, the value of the R_T resistor should be chosen at a frequency 25% to 50% below the applied clock signal for proper operation.

OPERATION

EN/UVLO Pin Comparator and V_{IN} UVLO

In addition to serving as a logic level input to enable certain functions of the device, the EN/UVLO pin includes an accurate internal comparator that allows custom rising and falling ON/OFF thresholds for V_{IN} to be set with the addition of external resistor dividers. When the EN/UVLO pin is driven above a logic threshold (0.7V typical) certain control circuitry of the IC is enabled, drawing additional quiescent current. If the EN/UVLO voltage is increased further, so that it exceeds the accurate comparator rising threshold (1.2V nominal), all functions of the buck-boost converter will be enabled and a startup sequence will commence, assuming the V_{IN} is above the UVLO level (see Figure 3). If EN/UVLO is brought below the accurate comparator falling threshold (1.1V nominal), the buck-boost converter will inhibit switching, but certain control circuitry will remain powered until EN/UVLO is brought below the logic threshold. In order to completely shut down the IC and reduce the V_{IN} currents to < 1µA (typical), it is necessary to ensure that EN/UVLO is brought below the worst case low logic threshold of 0.3V.

In addition to the EN/UVLO pin comparators, the LT3154 incorporates additional under voltage lockout (UVLO) circuits to control operation. The V_{IN} UVLO comparator prevents operation below 1.8V over temperature (typical values are 1.7V rising/1.6V falling).

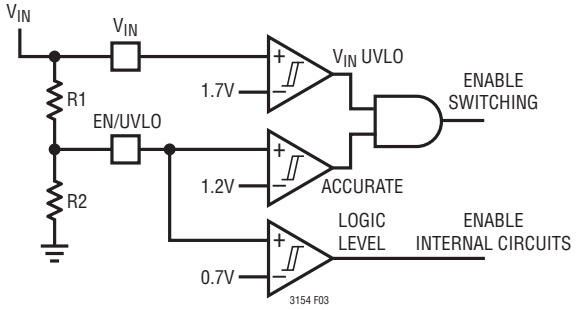


Figure 3. Accurate and Logic Level EN/UVLO Pin Comparators and V_{IN} UVLO

Soft-Start

The LT3154 soft-start circuit minimizes input current transients and output voltage overshoot on initial power-up. An internal soft-start interval of approximately 2.2ms can be selected by connecting SS to V_{IN}, eliminating the need for an external SS capacitor. For applications requiring a longer or custom soft-start period, an external capacitor on SS sets soft-start period according to the formula:

$$C_{SS}(nF) = 1.25 \bullet t_{SS}(ms)$$

The soft-start circuit slowly ramps the Error Amplifier output at VC. In doing so, the current command of the IC is slowly increased, starting from zero. The soft-start period is defined as the time it takes the internal or external SS capacitor to ramp to 0.8V, allowing VC to command full rated current. In most situations, V_{OUT} comes into regulation without needing full inductor current, resulting in power-up times at a fraction of the soft-start period. After initial power-up, soft-start can be reset by V_{IN} UVLO asserting, Thermal Shutdown, or a V_{OUT} short circuit.

Note: An internal resistor is used to discharge the external SS capacitor in shutdown. If SS is connected to V_{IN}, EN/UVLO should be initially enabled during V_{IN} power-up to allow the LT3154 to determine the internal SS pin configuration and ensure low current shutdown. This can be done by connecting EN/UVLO to V_{IN} directly or through a resistive divider network shown in most data sheet circuits. For applications where EN/UVLO is controlled through a microprocessor or controller, an external SS capacitor is recommended to prevent initial higher shutdown current.

OPERATION

Thermal Considerations

The power switches of the LT3154 are designed to operate continuously with currents up to the internal current limit thresholds. However, when operating at high current levels, there may be significant heat generated within the IC. Careful consideration must be given to the thermal environment of the IC in order to provide a means to remove heat from the IC and ensure that the LT3154 is able to provide its full rated output current. Specifically, the exposed die attach pad of both the LQFN package must be soldered to a copper layer on the PCB to maximize the conduction of heat out of the IC package. This can be accomplished by utilizing multiple vias from the die attach pad connection underneath the IC package to other PCB layer(s) containing large copper planes. A recommended board layout incorporating these concepts is show in Figure 4. Typical temperature rise versus load current curves using Figure 4 PCB are given in the Typical Performance Characteristics section.

If the IC die temperature exceeds approximately 170°C, thermal shutdown will be invoked and all switching will be inhibited. The part will remain disabled until the die temperature cools by approximately 10°C. The soft-start circuit is re-initialized in thermal shutdown to provide a smooth recovery when the die temperature cools enough to resume operation.

APPLICATIONS INFORMATION

Application circuits for the LT3154 are shown throughout the data sheet with varied use of pin-strapped/default or programmable operation as described in the Quick Reference section. The selection of external components is dependent upon the required performance of each particular application given considerations and trade-offs such as PCB area, input and output voltage range, output voltage ripple, required efficiency, thermal considerations and cost. This section of the data sheet provides some basic guidelines and considerations to aid in the selection of external components and the design of the applications circuit.

Inductor Selection

The choice of inductor used in LT3154 applications influences the maximum deliverable output current, the converter bandwidth, the magnitude of the inductor current ripple and the overall converter efficiency. The inductor must have a low DC series resistance or output current capability and efficiency will be compromised. Larger inductor values reduce inductor current ripple but will not increase output current capability as is the case with peak current mode control as described in the “Inductor Current Sense and Maximum Output Current” section of this data sheet. Larger value inductors also tend to have a higher DC series resistance for a given case size, which will have a negative impact on efficiency. Larger values of inductance will also lower the Right Half Plane (RHP) zero frequency when operating in boost mode, which requires the converter bandwidth to be set lower in frequency, slowing the converter’s response to load transients.

$$f_{RHPZ(Hz)} = \frac{V_{IN}^2 \bullet R_L}{V_{OUT}^2 \bullet 2\pi \bullet L}$$

Regardless of inductor value, the saturation current rating should be selected such that it is greater than the worst case average inductor current plus half of the ripple current. The peak-to-peak inductor current ripple for each operational mode can be calculated from the following formula, where f_{SW} is the switching frequency in MHz and L is the inductance in µH.

$$\Delta I_{L(P-P)(BUCK)} = \frac{V_{OUT}}{f_{SW} \bullet L}\left(\frac{V_{IN} - V_{OUT}}{V_{IN}}\right) \text{Amps}$$

$$\Delta I_{L(P-P)(BOOST)} = \frac{V_{IN}}{f_{SW} \bullet L}\left(\frac{V_{OUT} - V_{IN}}{V_{OUT}}\right) \text{Amps}$$

It should be noted that the worst case inductor peak-to-peak inductor ripple current occurs when the duty cycle in

APPLICATIONS INFORMATION

buck mode is maximum (highest V_{IN}) and in boost mode when the duty cycle is 50% ($V_{OUT} = 2V_{IN}$).

Recommended values based on switching frequency are given in Table 4.

Table 4. Recommended Values

Frequency	Value
500kHz < f_{SW} < 900kHz	1.5µH
900kHz < f_{SW} < 1.5MHz	1µH
1.5MHz < f_{SW} < 2.5MHz	0.68µH
2.5MHz < f_{SW} < 4.0MHz	0.47µH

In addition to its influence on power conversion efficiency, the inductor DC resistance can also impact the maximum output current capability of the buck-boost converter particularly at low input voltages. In buck mode, the output current of the buck-boost converter is primarily limited by the inductor current reaching the average current limit threshold defined by V_C. However, in boost mode, especially at large step-up ratios, the output current capability can also be limited by the total resistive losses in the power stage. These losses include, switch resistances, inductor DC resistance and PCB trace resistance. Avoid inductors with a high DC resistance (DCR) as they can degrade the maximum output current capability from what is shown in the Typical Performance Characteristics section. As a guideline, the inductor DCR should be similar to the typical power switch resistance of 20mΩ. The only exceptions are applications that have a maximum output current much less than what the LT3154 is capable of delivering.

Different inductor core materials and styles have an impact on the size and price of an inductor at any given current rating. Shielded construction is generally preferred as it minimizes the chances of interference with other circuitry. The choice of inductor style depends upon the price, sizing, and EMI requirements of a particular application. Table 5 provides a small sampling of inductors that are well suited to many LT3154 applications with L × W dimensions around 3mm to 5mm.

Table 5. Representative Surface Mount Inductors

SERIES	VALUE (µH)	DCR (mΩ)	MAX DC CURRENT (A)
Bourns			www.bourns.com
SRP	0.47–1.5	5–15	>6
Coilcraft			www.coilcraft.com
XAL, XEL	0.5–1.5	10–20	>6
Cooper Bussmann/Eaton www.eaton.com			
HCM0703	0.68–1.5	6–15	>6
Sumida			www.sumida.com
0420CDM	0.5–1.5	8–22	>6
Taiyo Yuden			www.t-yuden.com
MDW, NRS	0.5–1.5	10–30	>6
TDK			www.tdk.com
SPM	0.6–1.5	15–40	>6
Toko – Murata			www.murata.com
FDSD, DEM	0.68–1.5	10–22	>6
Wurth			www.we-online.com
WE-MAPI, WE-LHMI	0.68–1.5	6–15	>6

Output Capacitor Selection

A low effective series resistance (ESR) output capacitor should be connected at the output of the buck-boost converter in order to minimize output voltage ripple. Multilayer ceramic capacitors are an excellent option as they have low ESR and are available in small foot prints. The capacitor value should be chosen large enough to reduce the output voltage ripple to acceptable levels. Neglecting the capacitor's ESR and ESL (effect series inductance), the peak-to-peak output voltage ripple can be calculated by the following formula, where f_{SW} is the frequency in MHz and C_{OUT} is the capacitance in µF. A formula for calculating ΔI_L, in buck mode is given in the Operation section.

$$\Delta V_{P-P(BUCK)} = \frac{\Delta I_L}{8 f_{SW}\, C_{OUT}} \text{Volts}$$

$$\Delta V_{P-P(BOOST)} = \frac{I_{LOAD}}{f C_{OUT}} \left(\frac{V_{OUT} - V_{IN}}{V_{OUT}} \right) \text{Volts}$$

APPLICATIONS INFORMATION

Examining the previous equations reveals that the output voltage ripple increases with load current and is generally higher in boost mode than in buck mode. Note that these equations only take into account the voltage ripple that occurs from the inductor current to the output being discontinuous. They provide a good approximation to the ripple at any significant load current but underestimate the output voltage ripple at very light loads where the output voltage ripple is dominated by the inductor current ripple.

In addition to the output voltage ripple generated across the output capacitance, there is also output voltage ripple produced across the internal resistance of the output capacitor. The ESR-generated output voltage ripple is proportional to the series resistance of the output capacitor and is given by the following expressions where RESR is the series resistance of the output capacitor and all other terms as previously defined.

$$\Delta V_{P-P(BUCK)} = \Delta I_L \, R_{ESR} \text{Volts}$$

$$\Delta V_{P-P(BOOST)} = I_{LOAD} \, R_{ESR} \left(\frac{V_{OUT}}{V_{IN}} \right) \text{Volts}$$

In most LT3154 applications, an output capacitor between 68µF and 220µF from PV_{OUT} to PGND will work well. An additional low value ceramic capacitor such as 4.7µF can be placed between V_{OUT} and GND to reduce switching noise to the control circuitry.

Input Capacitor Selection

The PV_{IN} pin carries the full inductor current and provides power to internal switches and drivers where V_{IN} powers control circuits in the IC. To minimize input voltage ripple and ensure proper operation of the IC, a low ESR bypass capacitor with a value of at least 22µF should be located as close to PV_{IN} as possible. The traces connecting this capacitor to PV_{IN} and the ground plane (PGND) should be made as short as possible. An additional low value ceramic capacitor such as 2.2µF can be placed between V_{IN} and GND to reduce switching noise to the control circuitry.

Recommended Input and Output Capacitors

The capacitors used to filter the input and output of the LT3154 must have low ESR and must be rated to handle the large AC currents generated by the switching converters. While there are many capacitor types for these applications (including low ESR tantalum, OS-CON and POSCAP), ceramic capacitors are often utilized in switching converter applications due to their small size, low ESR and low leakage currents. Table 6 provides a partial listing of multilayer ceramic capacitors. Many ceramic capacitors intended for power applications experience a significant loss in capacitance from their rated value as the DC bias voltage on the capacitor increases. It is not uncommon for a small surface mount capacitor to lose more than 50% of its rated capacitance when operated nears it maximum rated voltage. This effect is generally reduced as the case size is increased for the same nominal value capacitor. As a result, it is often necessary to use a larger value capacitance or a higher voltage rated capacitor than would ordinarily be required to actually realize the intended capacitance at the operating voltage of the application. X5R, X6S, X7R or X8R dielectric types are recommended as they exhibit the best performance over the wide operating range and temperature. To verify that the intended capacitance is achieved in the application circuit, be sure to consult the capacitor vendor's curve of capacitance vs DC bias voltage.

Table 6. Representative Multilayer Ceramic Capacitors

Part Series	Values (µF)	Voltage (V)	Capacitor Types
AVX		www.avx.com	
0805, 1206, 1210	Up to 100	6.3, 10	X5R, X6S, X7R
Kemet		www.kemet.com	
C0805–C1210	Up to 100	6.3, 10	X5R, X7R
Murata		www.murata.com	
GRM	Up to 100	6.3, 10	X5R, X7R
Taiyo Yuden		www.t-yuden.com	
EMK, JMK, LMK	Up to 47	6.3, 10	X5R, X6S, X7R
TDK		www.tdk.com	
CGA4 – CGA9	Up to 47	6.3	X5R, X7R

APPLICATIONS INFORMATION

PCB LAYOUT CONSIDERATIONS

The LT3154 switches large currents at high frequencies. Special attention should be paid to the PCB layout to ensure a stable, noise-free and efficient application circuit. Figure 4 presents a representative PCB layout for the LT3154 to outline some of the primary considerations. A few key guidelines are outlined below:

1. All circulating high current paths should be kept as short as possible. This can be accomplished by keeping the routes to all bold boxed components in Figure 4 as short and as wide as possible. Capacitor ground connections should via down to the ground plane in the shortest route possible. The bypass capacitors on PV_{IN} and PV_{OUT} to PGND should be placed as close to the IC as possible and should have the shortest possible paths to ground. These connections should be made as wide as possible to reduce the series resistance. This will improve efficiency and maximize the output current capability of the buck-boost converter.
2. The exposed pad is the power ground connection for the LT3154. Multiple vias should connect the back-pad directly to the ground plane. In addition maximization of the metallization connected to the back-pad will improve the thermal environment and improve the power handling capabilities of the IC.
3. The components shown in bold boxes and their connections should all be placed over a complete ground plane to minimize loop cross-sectional areas. This minimizes EMI and reduces inductive drops.
4. Keep the connection from the resistor dividers (R3, R4) to the FB pin as short as possible and away from the switch pin connections, return to the ground plane close to the IC.

Compensation of the Buck-Boost Converter

The LT3154 utilizes an average current architecture to regulate the output voltage. Average current mode control has two loops that require frequency compensation, the inner average current loop and the outer voltage loop. The compensation for the inner average current loop is fixed to simplify the loop design and provide the highest possible bandwidth over a wide operating range.

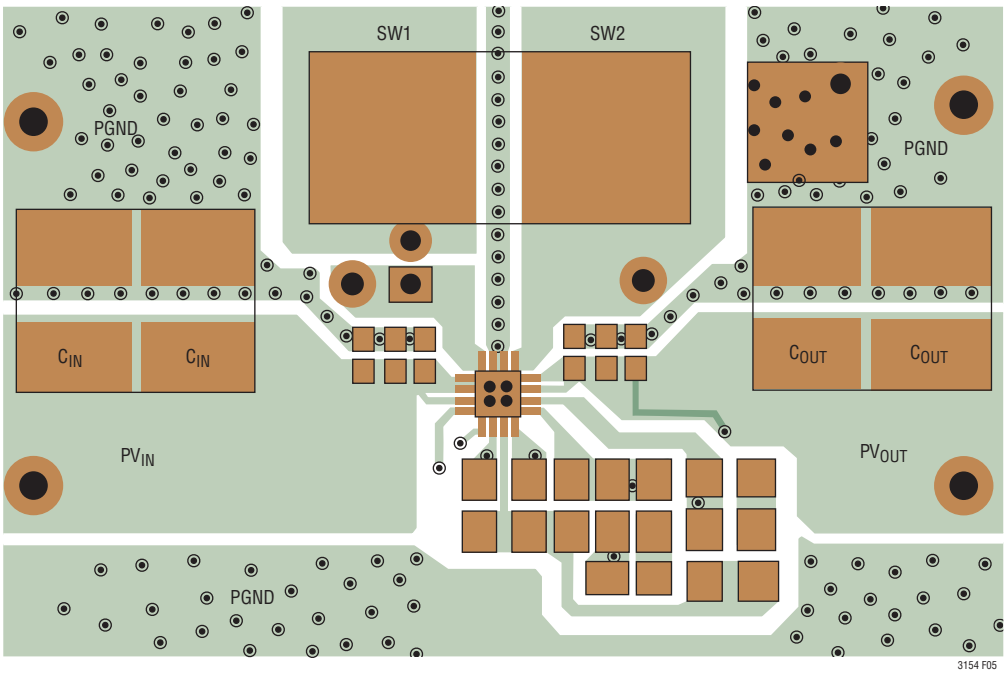


Figure 4. Example PCB Layout, Top Layer is Shown, Bottom Layer is Mostly PGND Plane

APPLICATIONS INFORMATION

The outer voltage loop requires external compensation components, which allows the overall loop characteristics to be customized depending on the programmed output voltage, oscillator frequency, inductor value and/or output capacitance. The average current mode control can be conceptualized as a voltage-controlled current source (VCCS), driving the output load formed primarily by R_{LOAD} and C_{OUT}, as shown in Figure 5.

The Voltage Error Amplifier output (V_C), provides a command input to the VCCS. The full scale range of V_C is 0.7V (200mV to 900mV). With a full scale command on V_C, the LT3154 buck-boost converter will generate an average 7A of inductor current (typical) from the converter making the transconductance gain 10A/V. As with peak current mode control, the inner average current control loop effectively turns the inductor into a current source over the frequency range of interest, resulting in a frequency response from the power stage that exhibits a single pole (–20dB/decade) roll-off. The output capacitor (C_{OUT}) and load resistance (R_{LOAD}) form a dominant low frequency pole, where the effective series resistance of the output capacitor and its capacitance form a zero, usually at a high enough frequency to be ignored.

A potentially troublesome Right Half Plane Zero (RHPZ) is also encountered if the converter is operated in boost mode. The RHPZ causes an increase in gain, like a zero, but a decrease in phase, like a pole. This can ultimately limit the maximum converter bandwidth that can be achieved with the LT3154. The RHPZ is not present when operating in buck mode.

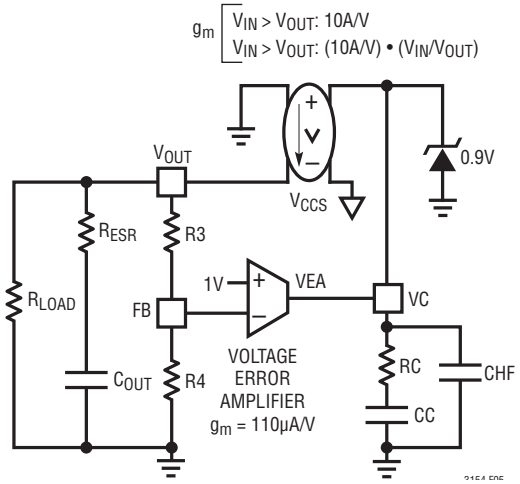


Figure 5. Simplified Representation of Average Current Mode Control Loop

The overall open loop gain at DC is the product of the following terms:

$$\text{Voltage Error Amp Gain}: g_{mVEA} \bullet R_{VEA} = 110\mu s \bullet 5M\Omega = 550V/V(\text{Fixed})$$

$$\text{Voltage Divider Gain}: \frac{V_{FB}}{V_{OUT}} = \frac{1V}{V_{OUT}}$$

$$\text{Current Loop Trans-Conductance}: g_m = 10A/V(\text{Fixed})$$

$$\text{Load Resistance } (R_{LOAD}) = \frac{V_{OUT}}{I_{LOAD}}$$

The application dependent terms that affect the loop gain include:

$$\text{Output Load Pole (P1)} := \frac{1}{(2\pi R_{LOAD} \bullet C_{OUT})}$$

$$\text{Right Half Plane Zero (RHPZ)}: \frac{V_{IN}^2 \bullet R_{LOAD}}{V_{OUT}^2 \bullet 2\pi \bullet L}$$

Voltage Error Amplifier Compensation

(2 Poles and 1 Zero)

The voltage amplifier's frequency response is designed to optimize the response for the overall loop. Measurement of the power stage gain over line, load, component variation, and frequency is strongly recommended prior to loop design. The design parameters for compensation design will focus on the series resistor and capacitors connected from VC to GND (RC, CC and CHF). Being a buck-boost converter, the target loop crossover frequency for the compensation design will be dictated by the highest boost ratio and load current that is expected as this will result in the lowest RHPZ frequency. The general goal is to set the crossover frequency and provide sufficient phase boost using the external compensation network.

APPLICATIONS INFORMATION

Compensation Example

This section will demonstrate how to derive and select the compensation components for a typical LT3154 application. Designing compensation for other applications is a matter of substituting different values in the equations provided based on the power stage Bode plots. Since the compensation design procedure uses the simplified model of Figure 5, the results from the following compensation design should always be verified with time domain step load response tests to validate the effectiveness of the compensation design. It is assumed that the value and type of output capacitor will be selected based on the guidelines provided elsewhere in this data sheet. Particular attention needs to be paid to the voltage bias effect on ceramic capacitors typically used for output bypassing. Similarly, it is assumed that the inductor value and current rating have been selected as well based on the application requirements.

Example Application Details:

V_{IN} = 1.8V to 5.5V

V_{OUT} = 3.3V

Maximum I_{OUT} = 1.65A, R_{LOAD} = 2Ω

C_{OUT} = 100µF (Use 3x47µF due to DC Bias)

L = 1µH

Since this application includes boost mode operation, the first step is to calculate the worst case RHPZ frequency as this will dictate the maximum loop bandwidth for the converter.

$$f_{RHPZ} = \frac{V_{IN}^2 \bullet R_{LOAD}}{V_{OUT}^2 \bullet 2\pi \bullet L} = \frac{(1.8V)^2 \bullet 2\Omega}{(3.3V)^2 \bullet 2\pi \bullet 1\mu H} = 95kHz$$

In order to account for internal IC component variations, it is good practice to set the converter bandwidth or cross-over frequency, F_{CC}, at least 5 times lower than the RHPZ frequency to avoid excessive phase loss from the RHPZ when operating in boost mode. In this example design, we'll plan to achieve a loop bandwidth (F_{CC}) of 20kHz, well below the RHPZ frequency. The 3.3V, 1.65A design example Bode plots are shown in Figure 6 and Figure 7. The DC power stage gain in buck mode is simply the current loop transconductance (10A/V) multiplied by the load resistance (2Ω). The V_{OUT} resistor divider will be accounted for in voltage error amplifier (VEA gain) network:

$$\text{Buck DC Gain } 20\text{Log}\left(\frac{10A \bullet 2\Omega}{V}\right) = 26dB$$

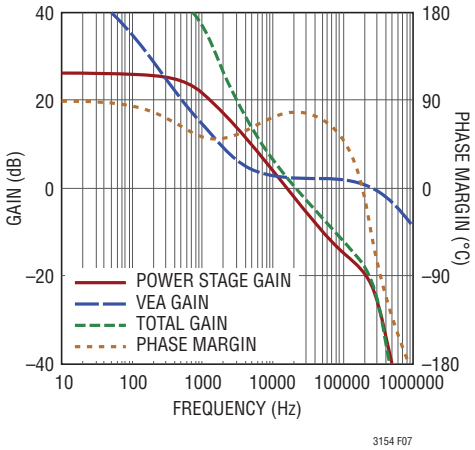


Figure 6. Buck Bode Plots (V_{IN} > V_{OUT}, V_{OUT} = 3.3V): Power Stage Gain, VEA Loop Gain, Total Loop Gain and Phase Margin vs Frequency

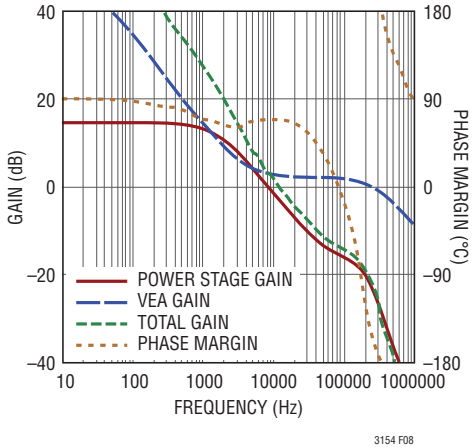


Figure 7. Boost Bode Plots (V_{IN} = 1.8V, V_{OUT} = 3.3V): Power Stage Gain, VEA Loop Gain, Total Loop Gain and Phase Margin vs Frequency

APPLICATIONS INFORMATION

In boost mode the power stage gain is reduced by $V_{IN}/2 \bullet V_{OUT}$:

Boost DC Gain at $1.8V_{IN}$

$$20\,\text{Log}\left(\frac{\frac{10A}{V}\bullet 2\Omega\bullet 1.8V}{2\bullet 3.3V}\right)=15dB$$

The output load pole will move depending on the output load resistance. The power stage gains and pole locations at full load are shown in Figure 6 and Figure 7.

Output Load Pole (Buck)

$$\frac{1}{2\pi\bullet R_{LOAD}\bullet C_{OUT}}=\frac{1}{2\pi\bullet 2\Omega\bullet 100\mu F}=800Hz$$

Output Load Pole (Boost)

$$\frac{2}{2\pi\bullet R_{LOAD}\bullet C_{OUT}}=\frac{2}{2\pi\bullet 2\Omega\bullet 100\mu F}=1600Hz$$

The resulting power stage crossover frequencies are around 16kHz in buck mode ($V_{IN} > 3.3V$), 8.5kHz in boost mode at $1.8V_{IN}$.

The uncompensated power stage crossover frequency is lower than the goal of 20kHz. More importantly, the uncompensated power stage DC gain is low especially in boost mode. A pole-zero-pole network is now added to the voltage amplifier to increase the DC gain, increase the crossover frequency, and reduce the overall gain at high frequencies.

$$\text{VEA Pole 1} = \frac{1}{2\pi R_{VEA}\bullet CC}$$

This pole is close to DC, R_{VEA} = Voltage Error Amp output resistance, which is approximately 5M. This pole is mentioned for completeness, but has no effect on the overall loop design.

$$\text{VEA Zero 1} = \frac{1}{2\pi\, RC\bullet CC}$$

This zero is placed below the crossover frequency to flatten the VA gain at the crossover to improve phase margin

$$\text{VEA Pole 2} = \frac{1}{2\pi\, RC\bullet CHF};$$

This pole is placed above the crossover frequency to reduce the gain to suppress noise and mitigate any RHPZ effects.

Referring to the buck power stage gain curves in Figure 6, the loop gain needs to be increased by 3dB to achieve a total loop crossover frequency of 20kHz. Assuming Zero 1 is placed well below the crossover frequency and Pole 2 is placed well above the crossover frequency, the voltage amplifiers gain at crossover is given by:

VEA gain at crossover:

$$20\,\text{Log}\left(\frac{V_{FB}\bullet g_m\bullet RC}{V_{OUT}}\right)=20\,\text{Log}\left(\frac{1V\bullet 110\mu A/V\bullet RC}{3.3V}\right)=3dB$$

Where g_m is the VEA transconductance, V_{FB}/V_{OUT} is the feedback divider gain, and RC is the external zero resistor:

$$RC=\frac{3.3V}{1V\bullet 110\mu A/V}\bullet 10^{3dB/20dB}=40.2k\Omega$$

A 60k value for RC will provide 3dB of gain at crossover. With RC selected, CC's value is determined by setting the Zero 1 frequency at 1/5 the crossover frequency or 4kHz:

$$CC=\frac{1}{2\pi\bullet RC\bullet f_{ZERO1}}=\frac{1}{2\pi\bullet 40.2k\Omega\bullet 4kHz}=1nF$$

Optionally, a high frequency Pole 2 is set at 20 times the crossover frequency to provide a high frequency pole at 400kHz:

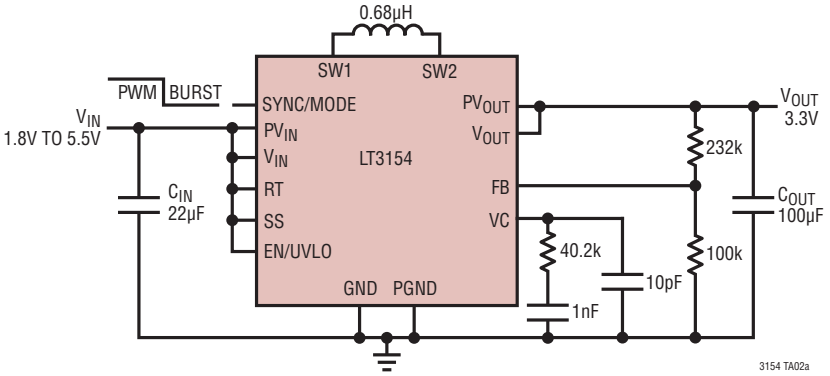
$$CHF=\frac{1}{2\pi\bullet RC\bullet f_{POLE2}}=\frac{1}{2\pi\bullet 40.2k\Omega\bullet 400kHz}=10pF$$

VEA Gain in Figure 6 or Figure 7 shows the resulting voltage error amplifier (VEA) response to the selected values.

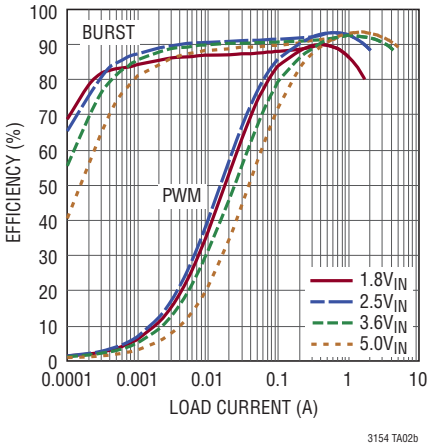
Combining the power stage and VEA frequency responses, the measured total loop gains are illustrated in Figure 6 and Figure 7. As shown, the crossover frequency was increased to 20kHz in buck mode, 10kHz in boost mode. The phase margin at crossover is around 70°C in both cases. The VEA loop design provided the additional benefits of high gain (>60dB) at DC and gain attenuation above the crossover frequency to prevent RHPZ issues.

TYPICAL APPLICATIONS

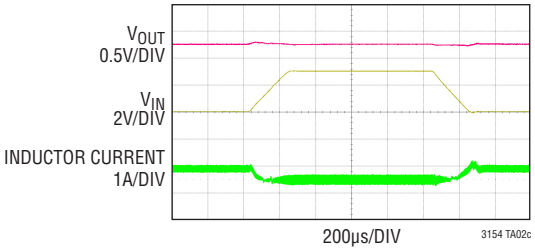
Wide V_{IN} to 3.3V with Minimal External Components



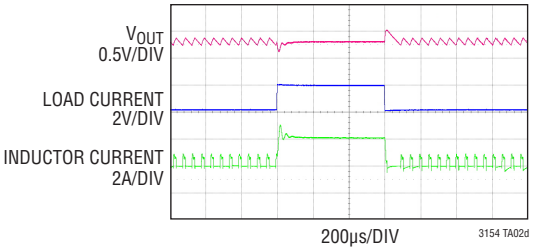
Efficiency vs V_{IN} and Load at 2.2MHz



V_{IN} Step 2V to 5V at 0.5A PWM Mode

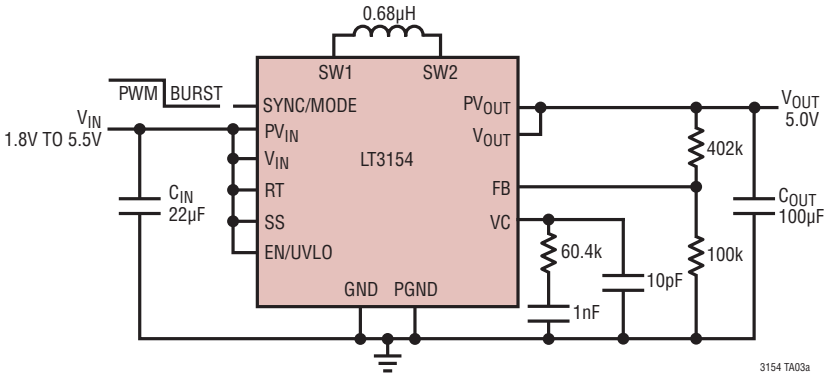


Load Transient Burst Mode $3.6V_{IN}$, 200mA to 2A

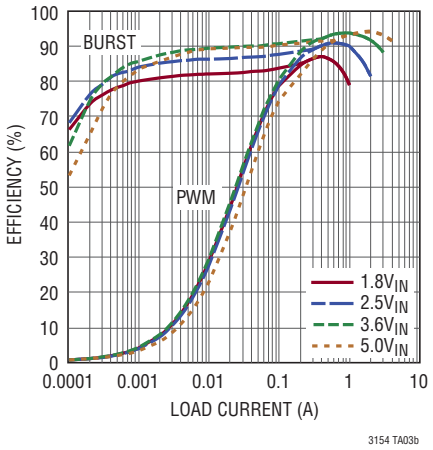


TYPICAL APPLICATIONS

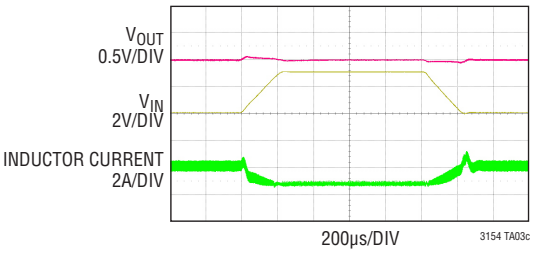
Wide V_{IN} to 5.0V with Minimal External Components



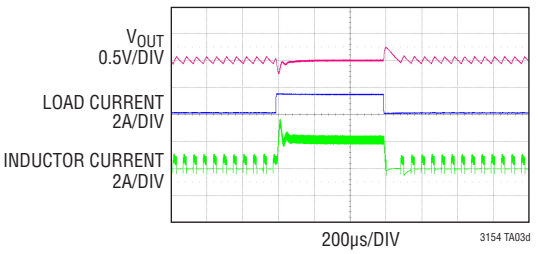
Efficiency vs V_{IN} and Load at 2.2MHz



V_{IN} Step 2V to 5V at 0.5A PWM Mode

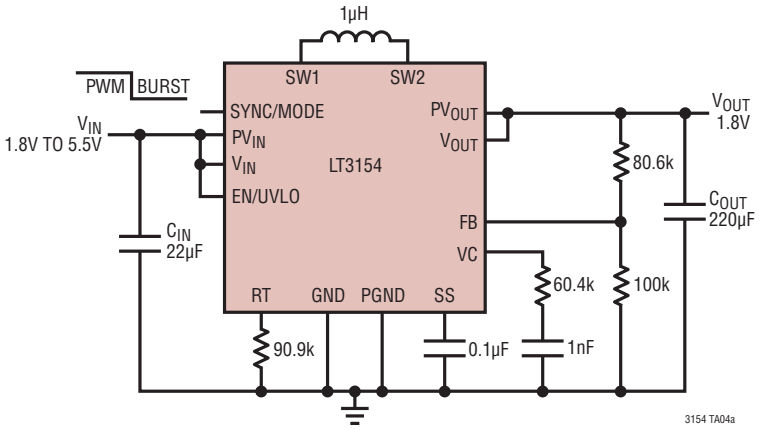


Load Transient Burst Mode 3.6V_{IN}, 150mA to 1.5A

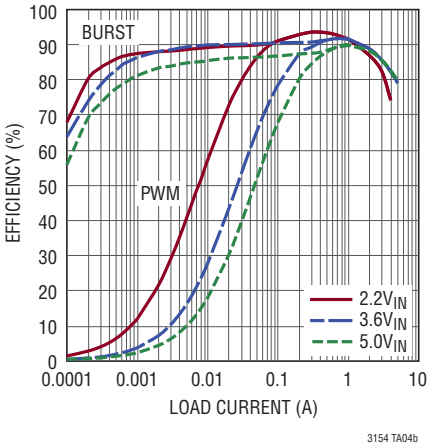


TYPICAL APPLICATIONS

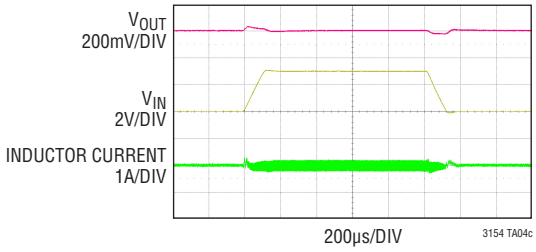
Wide V_{IN} to 1.8V-4A Buck Converter



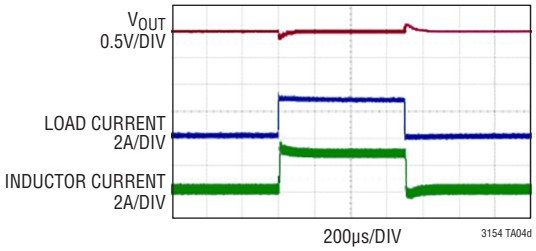
Efficiency vs V_{IN} and Load at 1.2MHz



V_{IN} Step 2V to 5V at 1A

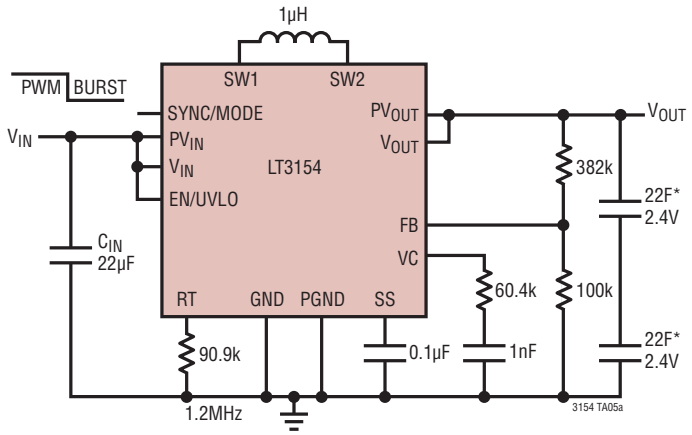


Load Transient PWM Mode $3.3V_{IN}$, 300mA to 3A



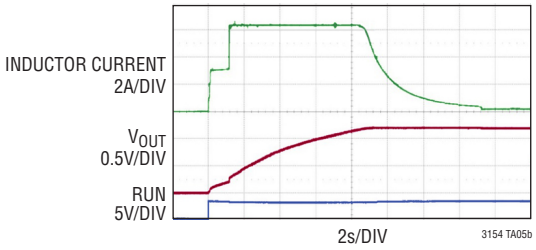
TYPICAL APPLICATIONS

Stacked Supercapacitor Charging Application



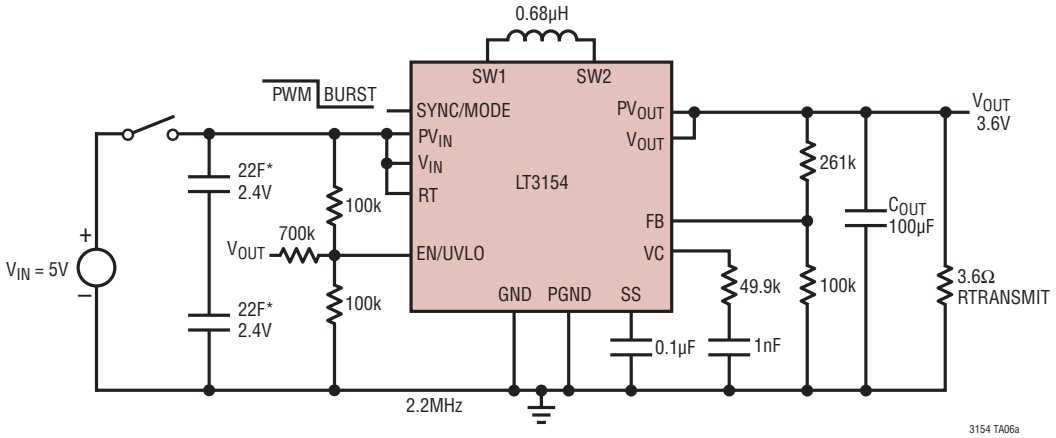
*COOPER BUSSMAN POWERSTOR AEROGEL B SERIES

I_L current and V_{OUT} Voltage from 0V to 4.8V Charging



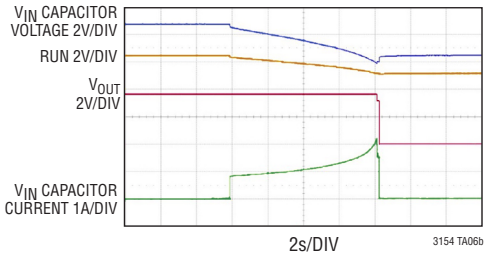
TYPICAL APPLICATIONS

Stacked Supercapacitor Powering PA Application



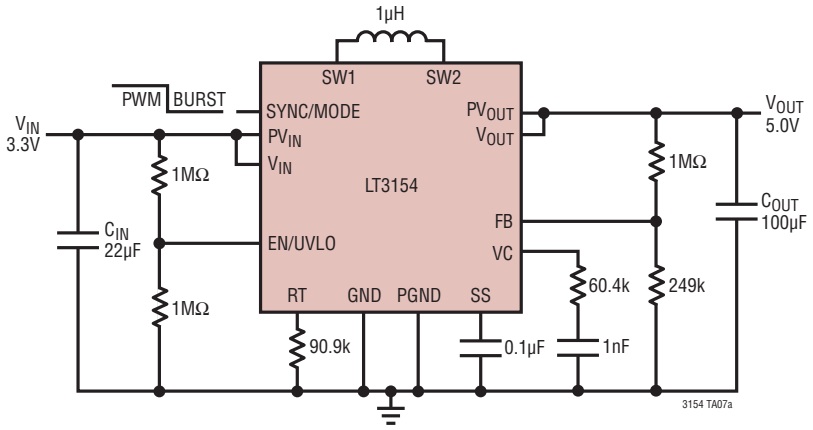
*COOPER BUSSMAN POWERSTOR AEROGEL B SERIES

Waveforms of V_{IN}, V_{OUT}, I_L During Discharge

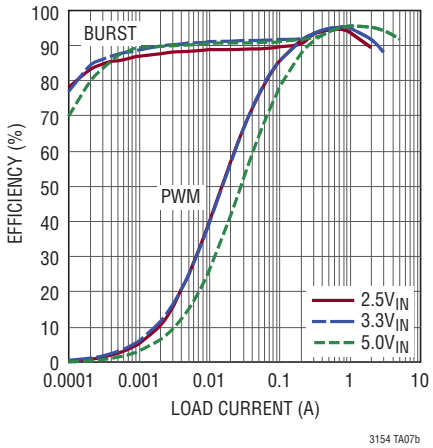


TYPICAL APPLICATIONS

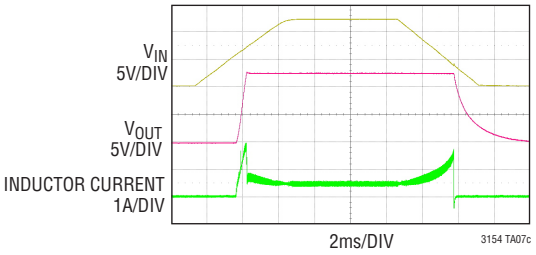
3.3V to 5.0V – 3A Boost Converter, 2.4V UVLO with Output Disconnect



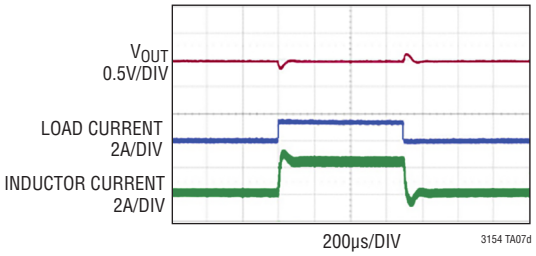
Efficiency vs Load at 1.2MHz



Power-Up/Down Waveforms 0.5A Load

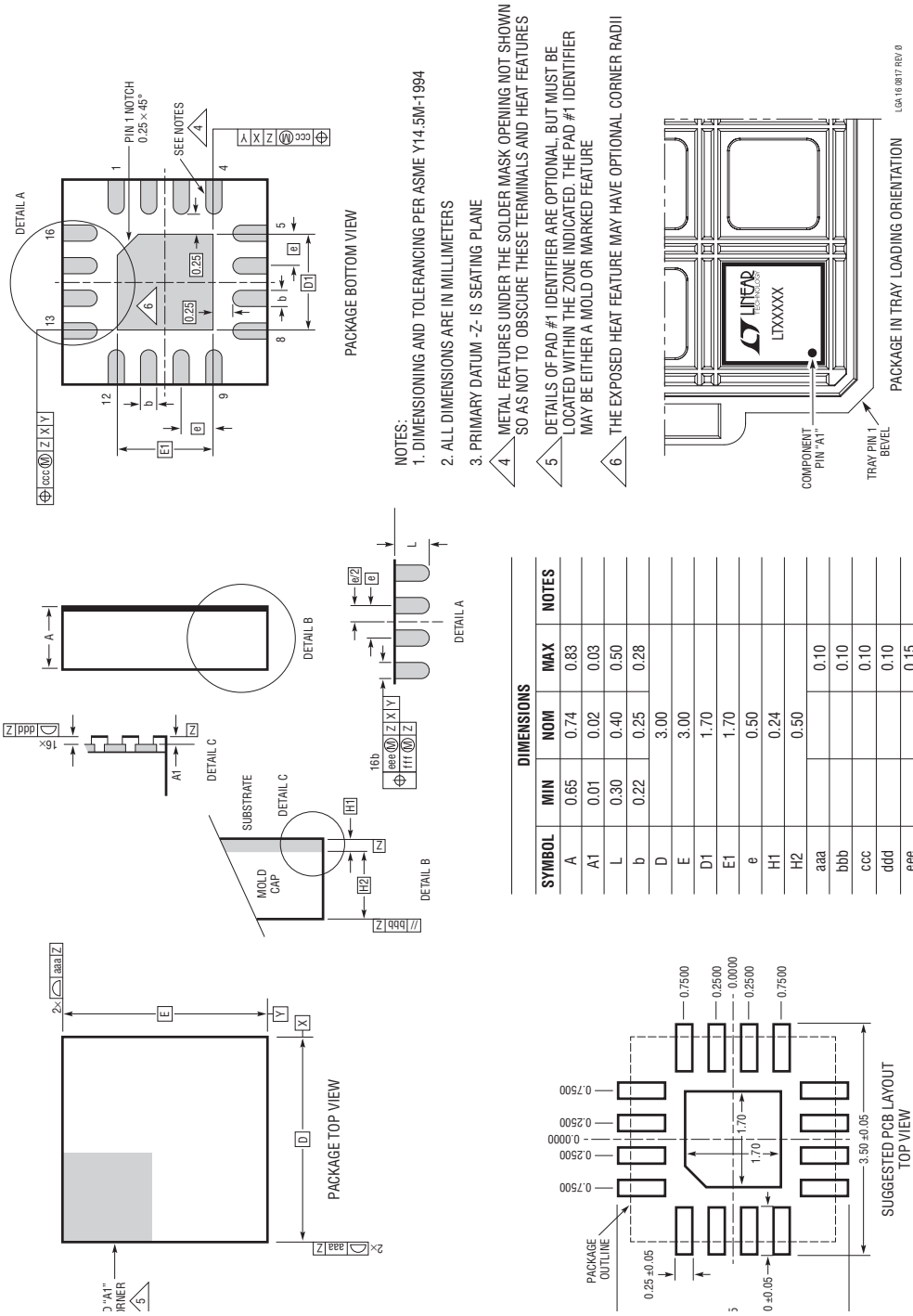


Load Transient PWM Mode $3.6V_{IN}$, 150mA to 1.5A



PACKAGE DESCRIPTION

LQFN Package
16-Lead (3mm × 3mm × 0.74mm)
(Reference LTC DWG # 05-08-1595 Rev Ø)



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. PRIMARY DATUM -Z- IS SEATING PLANE
4. METAL FEATURES UNDER THE SOLDER MASK OPENING NOT SHOWN SO AS NOT TO OBSCURE THESE TERMINALS AND HEAT FEATURES
5. DETAILS OF PAD #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PAD #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
6. THE EXPOSED HEAT FEATURE MAY HAVE OPTIONAL CORNER RADII

DIMENSIONS

SYMBOL	MIN	NOM	MAX	NOTES
A	0.65	0.74	0.83	
A1	0.01	0.02	0.03	
L	0.30	0.40	0.50	
b	0.22	0.25	0.28	
D		3.00		
E		3.00		
D1		1.70		
E1		1.70		
e		0.50		
H1		0.24		
H2		0.50		
aaa			0.10	
bbb			0.10	
ccc			0.10	
ddd			0.10	
eee			0.15	
fff			0.08	

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	08/23	Added tape and reel version to the Order Information.	2

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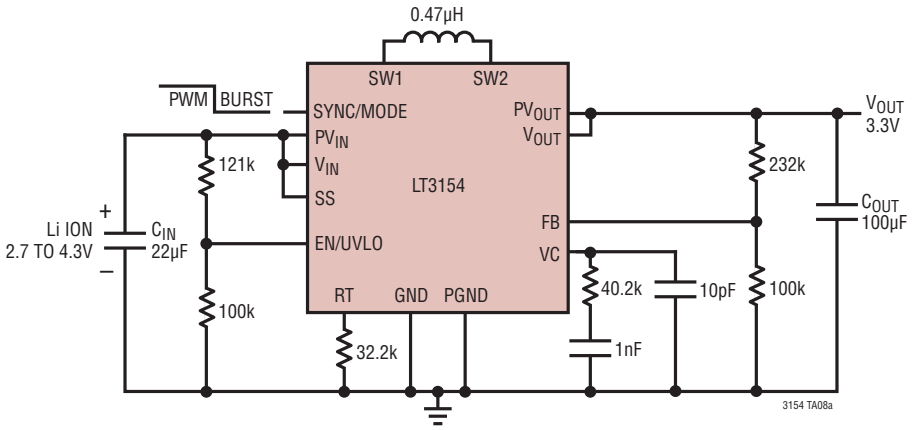
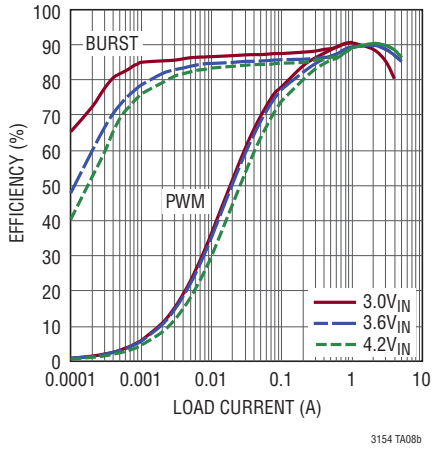
TYPICAL APPLICATION

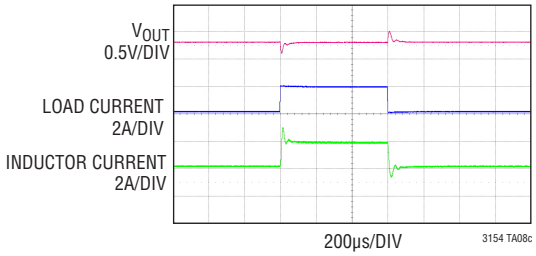
Li-Chemistry to 3.3V at 3.4MHz



Efficiency vs Load at 3.4MHz



Load Transient PWM Mode
V_{IN} = 3.6V, 200mA to 2A



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3533	5V, 2A Wide V_{IN}, Buck-Boost DC/DC Converter	V_{IN}: 1.8V to 5.5V, V_{OUT}: 1.8V to 5.25V, I_Q = 40µA, I_{SD} <1µA, DFN Package
LTC3113	5V, 3A Wide V_{IN}, Low Noise, Buck-Boost DC/DC Converter	V_{IN}: 1.8V to 5.5V, V_{OUT}: 1.8V to 5.5V, I_Q = 40µA, I_{SD} <1µA, DFN and TSSOP Packages
LTC3112	15V, 2.5A Synchronous Buck-Boost DC/DC Converter	V_{IN}: 2.7V to 15V, V_{OUT}: 2.5V to 14V, I_Q = 50µA, I_{SD} <1µA, DFN Package
LT3120	26V, 9A Low I_Q CC/CV Monolithic Buck-Boost Converter	V_{IN}: 2.5V to 26V, V_{OUT}: 0.8V to 24V, I_Q = 30µA, I_{SD} <1µA, LQFN Package
ADP2503/ ADP2504	600mA/100mA, 2.5MHz Buck-Boost DC/DC Converters	V_{IN}: 2.3V to 5.5V, V_{OUT}: 2.8V to 5.25V, I_Q = 38µA, I_{SD} <1µA, QFN Package

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