40V, 1.2A Micropower Synchronous Boost Converter with PassThru

FEATURES

- **Wide Input Voltage Range: 3.0V to 40V**
- **Low Quiescent Current in Burst Mode® Operation**
  - **<6μA I_Q**
  - **<20mV$_{P-P}$ Output Ripple**
- **Synchronous Operation for High Efficiency**
- **Monolithic 40V, 240mΩ Power Switches**
- **100% Duty Cycle PassThru™ Mode for Boost Preregulation Applications**
- **Adjustable and Synchronizable: 300kHz to 3MHz**
- **Spread Spectrum for Reduced EMI/EMC Emissions**
- Accurate EN/UVLO
- Internal Compensation
- 20MΩ Internal Feedback Divider
- Output Voltage Up to 40V
- Available in 10-Lead MSOP Package
- AEC-Q100 Automotive Qualification in Progress

APPLICATIONS

- Industrial and Automotive Power Supplies
- Battery-Powered Systems
- General Purpose Step-Up

DESCRIPTION

The LT®8338 is a synchronous monolithic step-up regulator that provides high efficiency for input and output up to 40V. It consumes only 6μA quiescent current at Burst Mode operation to maintain high efficiency at very low output current, while keeping the output ripple below 20mV$_{P-P}$. The LT8338 switching frequency can be set with an external resistor over the range of 300kHz to 3MHz. A SYNC/MODE pin allows synchronization to an external clock. It can also be used to select between Burst Mode operation and pulse-skipping mode, or to enable spread spectrum modulation to reduce EMI. The EN/UVLO pin has an accurate 1V threshold and can be used to program V_{IN} UVLO or to shut down the part. The LT8338 enters 100% duty cycle PassThru mode when V_{IN} is higher than the regulated V_{OUT}. The LT8338 also features frequency foldback and internal soft-start for inductor current control during start-up.

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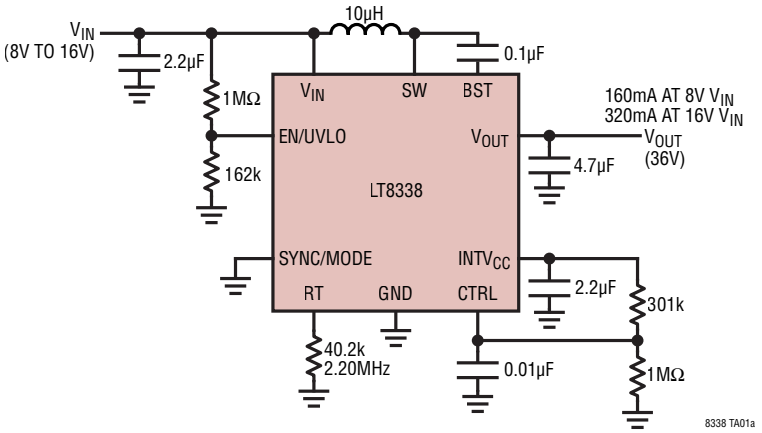
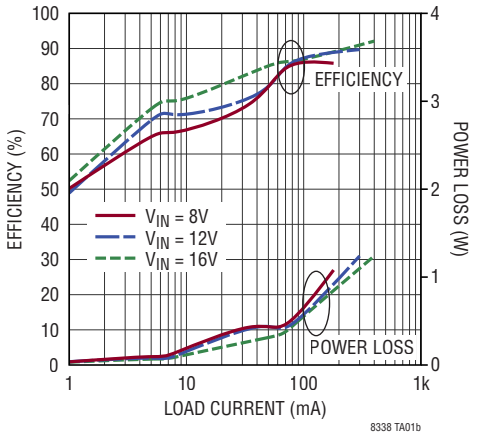
TYPICAL APPLICATION

8V to 16V Input, 36V Output Micropower Synchronous Boost Converter



Efficiency



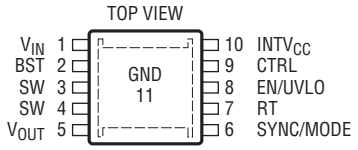
Rev. A

ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN}, V_{OUT}, EN/UVLO, SW 40V
SYNC/MODE 6V
CTRL Above $INTV_{CC}$ 0.3V
RT .....(Note 2)
$INTV_{CC}$ .....(Note 2)
BST Above SW .....(Note 2)
Operating Junction Temperature Range (Notes 2, 3)
LT8338E .....–40°C to 125°C
LT8338J.....–40°C to 150°C
Storage Temperature Range .....–65°C to 150°C

PIN CONFIGURATION



MSE PACKAGE
10-LEAD PLASTIC MSOP

θ_{JA} = 40°C/W
EXPOSED PAD (PIN 11) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT8338EMSE#PBF	LT8338EMSE#TRPBF	LTHGQ	10-Lead Plastic MSOP	–40°C to 125°C
LT8338JMSE#PBF	LT8338JMSE#TRPBF	LTHGQ	10-Lead Plastic MSOP	–40°C to 150°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, V_{OUT} = 36V, CTRL = 2.0V, EN/UVLO = 12V, $INTV_{CC}$ = 2.2µF to GND, R_T = 40.2kΩ to GND, BST = 0.1µF to SW and SYNC/MODE is tied to GND.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN} Operating Voltage		●	3.0		40	V
V_{IN} Quiescent Current (Note 5)	EN/UVLO = 0V (Shutdown Mode)			0.1	1	µA
	EN/UVLO = 2V, SYNC/MODE = 0V, Not Switching, V_{OUT}–V_{IN} = +100mV (Burst Mode Operation)			6	18	µA
	EN/UVLO = 2V, SYNC/MODE = 0V, Not Switching, V_{OUT}–V_{IN} < –100mV (PassThru Mode)			12	35	µA
	EN/UVLO = 2V, SYNC/MODE = 2.6V (Pulse-Skipping Mode + SSFM)			1200	1500	µA
V_{OUT} Regulation (Note 6)	V_{IN} = 3.3V, CTRL = 0.5V (D = 33.33%)	●	8.8	9.00	9.2	V
	V_{IN} = 9V, CTRL = 1.0V (D = 50%)	●	17.8	18.00	18.2	V
	V_{IN} = 24V, CTRL = 2.0V (D = 66.67%)	●	35.6	36.00	36.4	V
V_{OUT} Limit Threshold Voltage (Note 6)		●	40.2	41.4		V
V_{OUT} I_Q in Shutdown	EN/UVLO = 0V				5	µA
EN/UVLO Threshold Voltage	EN/UVLO Falling	●	0.975	1.000	1.025	V
	EN/UVLO Rising Hysteresis			50		mV
EN/UVLO Input Bias Current	EN/UVLO = 2V		–40		40	nA
$INTV_{CC}$ Regulation Voltage		●	2.56	2.6	2.64	V
$INTV_{CC}$ Line Regulation	3V ≤ V_{IN} ≤ 40V				0.02	%/V
$INTV_{CC}$ Load Regulation	1µA ≤ I_{INTVCC} ≤ 10mA				0.04	%/mA
V_{OUT}-to-CTRL Divider Ratio (Note 6)	9V ≤ V_{OUT} ≤ 36V	●	17.85	18.00	18.15	V/V
V_{OUT} Internal Divider Resistance				20		MΩ
CTRL Pin Input Current			–20		20	nA
Switching Frequency	R_T = 301k	●	270	300	335	kHz
	R_T = 80.6k	●	1.05	1.15	1.25	MHz
	R_T = 40.2k	●	2.00	2.20	2.40	MHz
SYNC Function Input Frequency Range	SYNC/MODE = External Clock		0.3		3.0	MHz
Spread Spectrum Frequency Range Range = $(f_{SW(SPREAD-ON)}/f_{SW(SPREAD-OFF)-1})$ • 100%	SYNC/MODE = $INTV_{CC}$			+14		%
Spread Spectrum Modulation Frequency				10		kHz
SYNC Function Input Low Threshold Voltage	SYNC/MODE Pulse Falling				0.8	V
SYNC Function Input High Threshold Voltage	SYNC/MODE Pulse Rising		2.0			V
SYNC/MODE Pin Voltage	SYNC/MODE = Floating			1.3		V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, V_{OUT} = 36V, CTRL = 2.0V, EN/UVLO = 12V, $INTV_{CC}$ = 2.2µF to GND, R_T = 40.2kΩ to GND, BST = 0.1µF to SW and SYNC/MODE is tied to GND.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SYNC/MODE Pulse Width High	Synchronization Mode		100			ns
SYNC/MODE Pulse Width Low	Synchronization Mode		100			ns
Bottom Switch Current Limit		●	1.2	1.4	1.6	A
Bottom Switch Minimum Off-Time					50	ns
Bottom Switch Minimum On-Time					80	ns
Bottom Switch On-Resistance				240		mΩ
Top Switch Current Limit (Note 7)	PassThru Mode		1.3	1.6	1.9	A
Top Switch On-Resistance				240		mΩ

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Do not drive these pins.

Note 3: The LT8338E is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT8338J is guaranteed over the full –40° to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures of greater than 125°C.

Note 4: These ICs include overtemperature protection that is intended to protect the device during momentary overload conditions. The maximum rated junction temperature will be exceeded when this protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

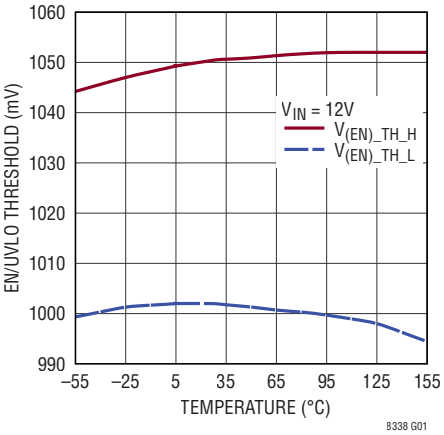
Note 5: The V_{IN} Quiescent Current specifications include the 2.6µA current implied by the specified R_{INTVCC} = 1M resistor.

Note 6: V_{OUT} regulation is tested in a servo loop.

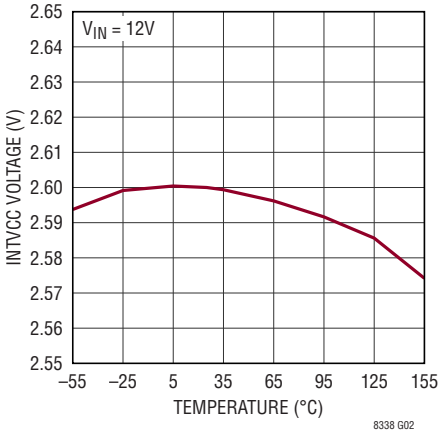
Note 7: Top Switch Current Limit prevents the bottom switch from turning on until the switch current has dropped below the limit.

TYPICAL PERFORMANCE CHARACTERISTICS

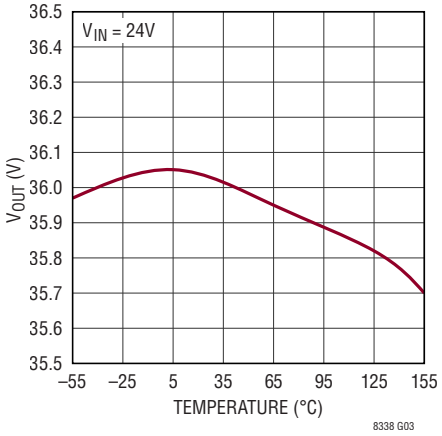
EN/UVLO Thresholds vs Temperature



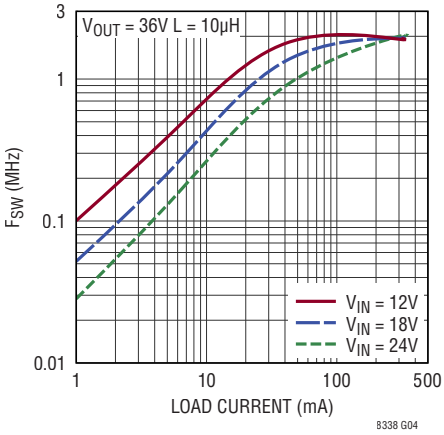
$INTV_{CC}$ Voltage vs Temperature



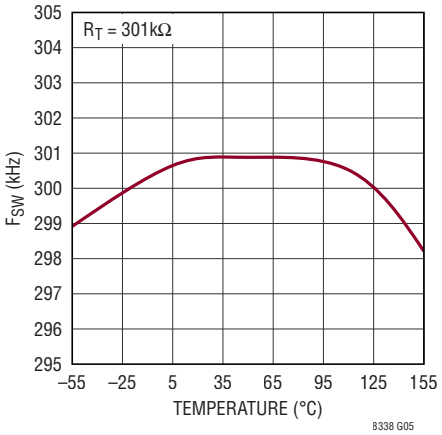
Output Voltage vs Temperature



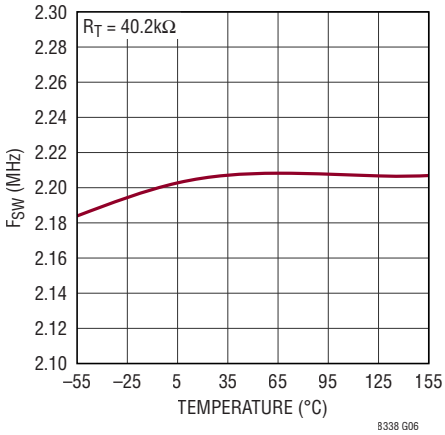
Burst Mode Switching Frequency vs Load Current



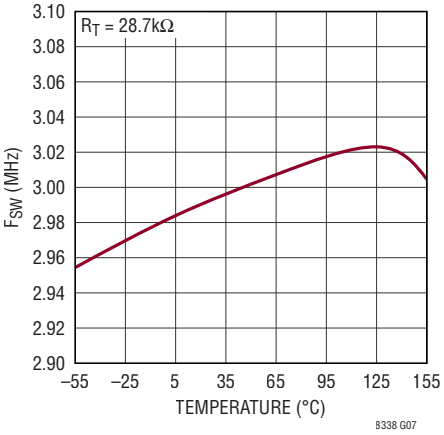
Switching Frequency vs Temperature



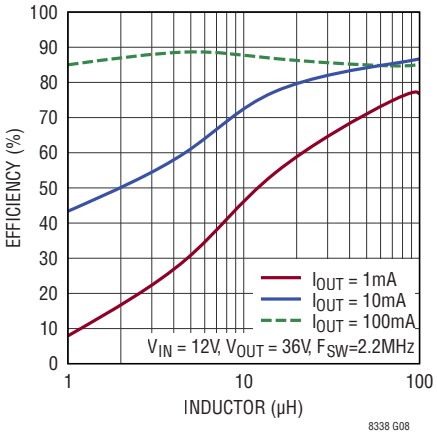
Switching Frequency vs Temperature



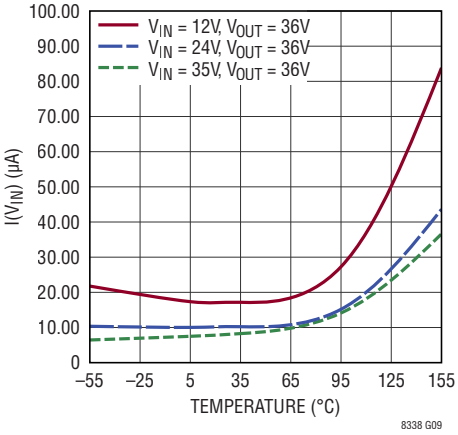
Switching Frequency vs Temperature



Burst Mode Efficiency vs Inductor Value

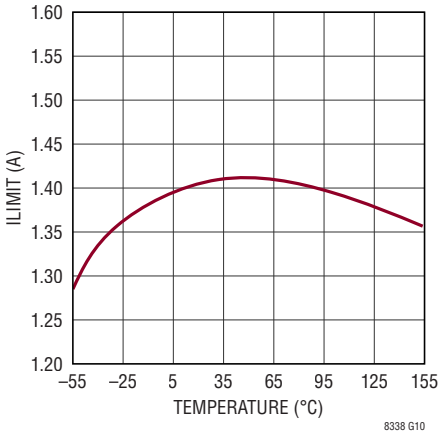


No-Load V_{IN} Current vs Temperature, V_{IN}

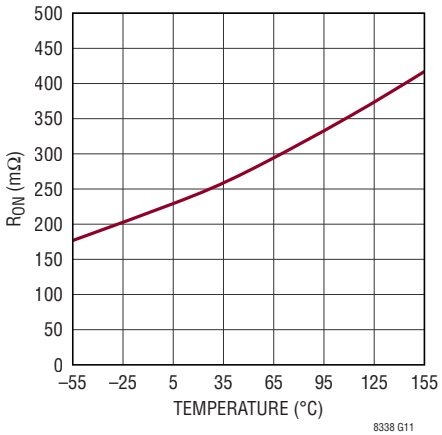


TYPICAL PERFORMANCE CHARACTERISTICS

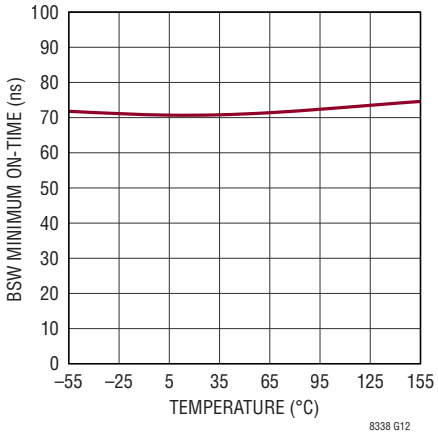
Power Switch Current Limit vs Temperature



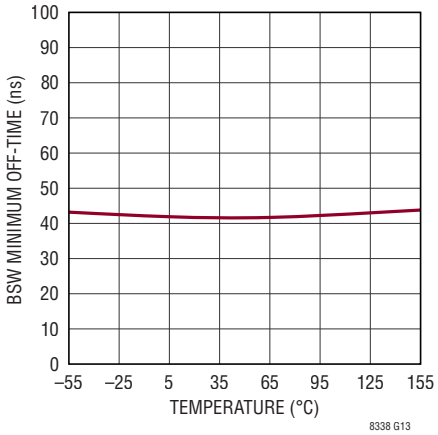
Bottom Switch On-Resistance vs Temperature



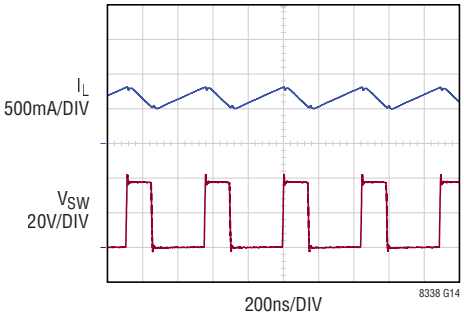
Bottom Switch Minimum On-Time vs Temperature



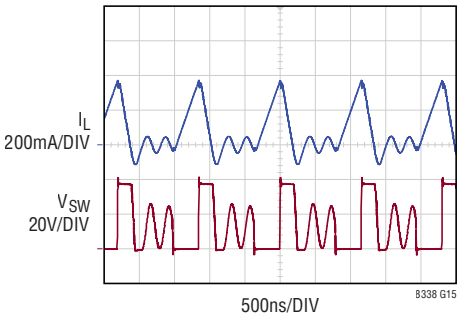
Bottom Switch Minimum Off-Time vs Temperature



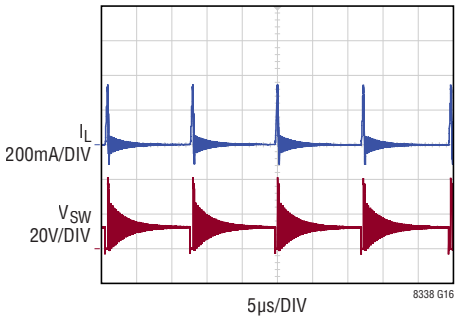
Switch Waveforms (In CCM)



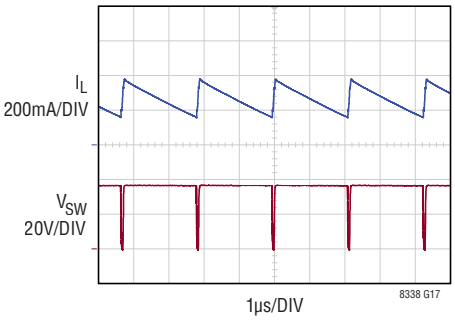
Switching Waveforms (In Light Burst Mode Operation)



Switching Waveforms (In Sleep Mode)

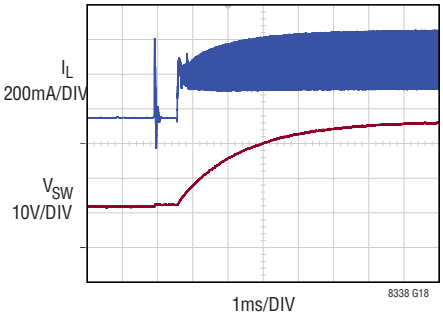


Switching Waveforms (V_{IN} Approaching V_{OUT})



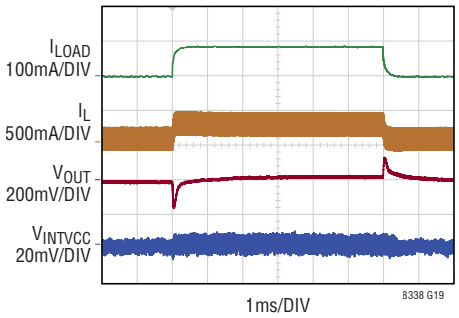
V_{IN} = 35V, V_{OUT} = 36V, I_{LOAD} = 300mA

Start-Up Waveforms

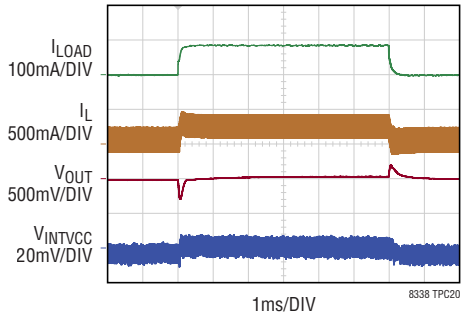


TYPICAL PERFORMANCE CHARACTERISTICS

Load Step Response (Pulse-Skipping Mode)



Load Step Response (Burst Mode Operation)



PIN FUNCTIONS

V_{IN} (Pin 1): Input Supply Pin. Bypass this pin to GND with a low ESR ceramic capacitor of 0.1µF or greater. Place the capacitor as close to the pin as possible.

BST (Pin 2): Top Switch Gate Driver Supply Pin. Tie a 0.1µF capacitor between BST and SW as close as possible to the pins to keep the trace length short.

SW (Pins 3, 4): Switch Node. Connect this pin to inductor, and to the boost capacitor. SW is a high dV/dt node that should be kept as compact as possible and away from high impedance nodes.

V_{OUT} (Pin 5): Output Voltage Pin. Bypass this pin to GND with a low ESR ceramic capacitor of 4.7µF or greater. Place the capacitor as close to the pin as possible. Additional capacitance as required by specific applications must be similarly closely placed. See the Applications and Physical Layout sections for details. An 18:1 internal resistive voltage divider provides feedback sensing of the output voltage to the error amplifier.

SYNC/MODE (Pin 6): External Synchronization Input and Light Load Operation Mode Selection Pin. This pin allows five selectable modes for optimization of performance.

SYNC/MODE PIN INPUT	CAPABLE MODE(S) OF OPERATION
(1) GND or <0.14V	Burst
(2) 100k Resistor to GND	Burst/SSFM
(3) Float (Pin Open)	Pulse-Skipping
(4) $INTV_{CC}$ or >2.0V	Pulse-Skipping/SSFM
(5) External Clock	Pulse-Skipping/SYNC

where the selectable modes of operation are:

Burst = Low I_Q, low output ripple operation at light loads

Pulse-Skipping = Skipped pulse(s) at light load (aligned to clock)

SYNC = Switching frequency synchronized to external clock

SSFM = Spread Spectrum Frequency Modulation for low EMI

RT (Pin 7): Switching Frequency Set Pin. Set the switching frequency with a resistor between this pin and GND. Do not leave this pin open. In frequency synchronization mode, use a resistor R_T to program the frequency the same as the synchronization signal.

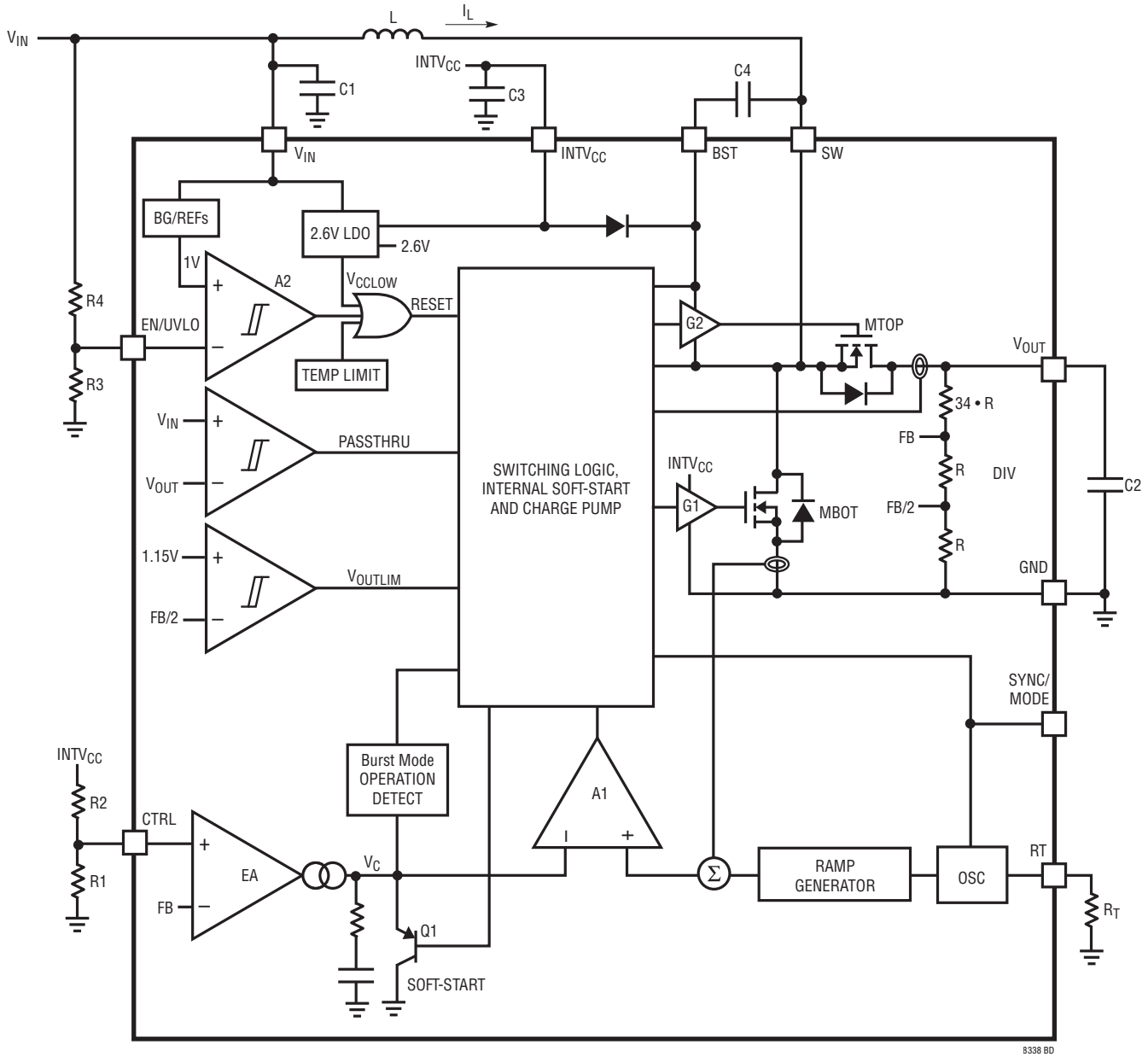
EN/UVLO (Pin 8): Enable and Input Undervoltage Lockout Pin. The LT8338 is shut down when this pin is below 1V (typ), and is enabled when this pin is above 1.05V (typ). A resistor divider from V_{IN} to GND programs a V_{IN} threshold below which the LT8338 is shut down. Tying this pin to GND shuts down operation and reduces quiescent supply current to 0.2µA (max). Tie to V_{IN} if the shutdown feature is not used.

CTRL (Pin 9): Reference Input Pin. Tie the tap point of a resistive voltage divider between $INTV_{CC}$ and GND to this pin to set the error amplifier reference input to 1/18 of the desired system output voltage.

$INTV_{CC}$ (Pin 10): Internal 2.6V Regulator Pin. Bypass this pin to GND with a low ESR ceramic capacitor of 2.2µF or greater. Place the capacitor as close to the pin as possible. Set the output voltage (V_{OUT}) by programming the CTRL pin voltage via a resistive voltage divider between $INTV_{CC}$ and GND. Use a minimum total resistance of 1M to keep the divider's contribution to the V_{IN} quiescent current to 2.6µA in shut down.

GND (Pin 11): Ground Pin. Connect this pin to system ground and to the ground plane to achieve the best thermal performance.

BLOCK DIAGRAM



OPERATION

The LT8338 is a synchronous boost converter that uses a fixed frequency, current mode control scheme to provide excellent line and load regulation. Referring to the Block Diagram, the Switching Logic and Charge Pump block turns on the power switch MBOT through driver G1 at the start of each oscillator cycle. The inductor current I_L flows through MBOT, whose current sensing signal is added to a stabilizing slope compensation ramp and the resulting sum is fed into the positive terminal of the PWM comparator A1. The level at the negative input of A1, labeled "V_C", is set by the error amplifier EA and is an amplified version of the difference between the feedback voltage (from the internal voltage divider) and the reference voltage (from CTRL pin). During the MBOT-on phase, I_L increases. When the signal at the positive input of A1 exceeds V_C, A1 sends a signal to turn off MBOT. When MBOT turns off, the synchronous power switch MTOP turns on until the next clock cycle begins or inductor current I_L falls to zero. If overload conditions result in excess current flowing through the top switch, the next clock cycle will be delayed until switch current returns to a safe level. Through this repetitive action, the EA sets the correct I_L peak current level to keep the output voltage in regulation.

If the EN/UVLO pin is lower than 0.3V, the LT8338 is shut down and draws < 0.2µA from the input. When the EN/UVLO pin is above 1.05V, the switching regulator becomes active.

The LT8338 can be configured to work in different modes by setting SYNC/MODE pin. If the SYNC/MODE pin is tied to ground directly, the LT8338 provides low output ripple Burst Mode operation with ultralow quiescent current at light loads. Connecting SYNC/MODE pin to ground through a 100k resistor enables Burst Mode operation with frequency spread spectrum modulation (see Frequency Spread Spectrum Modulation section). When Burst Mode operation is selected, all circuitries associated with controlling the output switches are shut down to reduce the quiescent current between bursts. When SYNC/MODE pin is floated, the LT8338 operates in pulse-skipping mode, which reduces output ripple compared to Burst Mode operation and increases the quiescent current to hundreds of microamps. Connecting the SYNC/MODE pin to $INTV_{CC}$ selects pulse-skipping operation with spread spectrum modulation enabled. Spread spectrum modulation varies the switching frequency to reduce EMI. When the SYNC/MODE pin is driven by an external clock, the converter switching frequency is synchronized to that clock and pulse-skipping mode is enabled.

APPLICATIONS INFORMATION

Programming V_{IN} Turn-On and Turn-Off Thresholds with the EN/UVLO Pin

The LT8338 is in shutdown when the EN/UVLO pin is low. The falling threshold of the EN comparator is 1V, with 50mV of hysteresis. The EN pin can be tied to V_{IN} if the shutdown feature is not used, or tied to a logic level if shutdown control is required. The LT8338 draws very low shutdown quiescent current (0.2µA typ) When EN/UVLO is below 0.3V.

Adding a resistor divider from V_{IN} to EN/UVLO programs the LT8338 to regulate the output only when V_{IN} is above a desired voltage. Typically, this threshold, $V_{IN(EN)}$, is used in situations where the input supply is current limited, or has a relatively high source resistance. A switching regulator draws constant power from the source, so source current increases as source voltage drops. This looks like a negative resistance load to the source and can cause the source to current limit or latch low under low source voltage conditions. The $V_{IN(EN)}$ threshold prevents the regulator from operating at source voltages where the problems might occur. This threshold can be adjusted by setting the values R3 and R4 (refer to the Block Diagram) such that they satisfy Equation 1.

$$V_{IN,FALLING} = 1V \bullet \frac{(R3+R4)}{R3}$$
$$V_{IN,RISING} = 40mV \bullet \frac{(R3+R4)}{R3} + V_{IN,FALLING} \quad (1)$$

When operating in Burst Mode operation for light load applications, the current through the R3 and R4 resistor network can easily be greater than the supply current consumed by the LT8338. Therefore, R3 and R4 should be large to minimize their effect on efficiency at low loads.

$INTV_{CC}$ Regulator

An internal low dropout (LDO) regulator produces the 2.6V supply from V_{IN} that powers the drivers and the internal bias circuitry. $INTV_{CC}$ can supply enough current for the LT8338's circuitry and must be bypassed to ground with a minimum of 2.2µF low ESR ceramic capacitor. Good bypassing is necessary to supply the high transient currents required by the power MOSFET gate drivers. Applications with high V_{IN} voltage and high switching frequency will increase die temperature due to the higher power dissipation across the LDO. The $INTV_{CC}$ falling threshold (to stop switching and reset soft-start) is typically 2.2V, and the rising threshold is 2.3V. Do not connect an external load to the $INTV_{CC}$ pin.

Achieving Ultralow Quiescent Current

When LT8338 is set for Burst Mode operation to enhance efficiency at light loads, the minimum peak inductor current is set to approximately 300mA even though V_C node indicates a lower value (refer to the Block Diagram). In Burst Mode operation, the LT8338 delivers single pulses of current to the output capacitor followed by sleep periods where the output power is supplied by the output capacitor. That is, at light load condition, the LT8338 maintains the output regulation voltage by reducing the switching frequency instead of reducing the inductor peak current.

As the output load decreases, the frequency of single current pulses decreases (see Figure 1) and the percentage of time the LT8338 is in sleep mode increases, resulting in much higher light load efficiency than typical converters. By maximizing the time between pulses, the converter quiescent current approaches 6µA for a typical application when there is no output load. In addition, if high light load efficiency is desired, a larger inductor value should be chosen. See the Burst Mode Efficiency vs Inductor Value curve in the Typical Performance Characteristics.

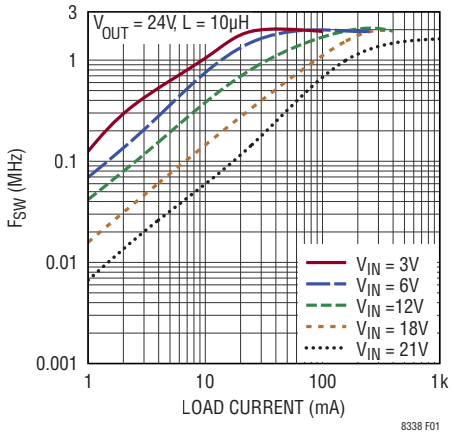


Figure 1. Burst Mode Frequency vs Load

APPLICATIONS INFORMATION

While in Burst Mode operation (Figure 2), the current limit of the bottom switch is approximately 300mA (as shown in Switching Waveforms in Burst Mode Operation in Typical Performance Characteristics), resulting in larger output voltage ripple comparing to that in pulse-skipping mode operation. Increasing the output capacitance will decrease output ripple proportionally. As the load ramps upward from zero, the switching frequency increases until reaching the switching frequency programmed by the R_T resistor. The output load at which the LT8338 reaches the programmed frequency varies based on input voltage, output voltage, and inductor choice.

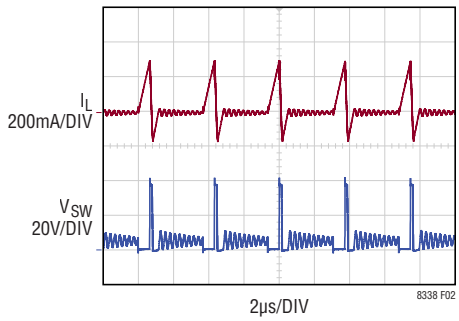


Figure 2. Burst Mode Operation Waveforms

For some applications it is desirable for the LT8338 to operate in pulse-skipping mode. Pulse-skipping mode operation offers two major differences from Burst Mode operation. First the clock stays awake at all times and all switching cycles are aligned to the clock. In this mode much of the internal circuitry is awake at all times, increasing quiescent current to thousand µA (compared to 6µA quiescent current in Burst Mode operation). Secondly pulse-skipping mode operation exhibits lower output ripple as well as lower audio noise and RF interference.

Operating Frequency and Synchronization

The choice of operating frequency is a trade-off between efficiency and component size. Low frequency operation improves efficiency by reducing the power switches' switching losses and gate drive current. However, lower frequency operation requires a physically larger inductor.

The LT8338 uses a constant-frequency architecture that can be programmed over a 300kHz to 3MHz range with a single external resistor from the RT pin to ground, as shown in the Block Diagram.

Table 1 gives some specific examples of R_T values for specific switching frequencies.

Table 1. SW Frequency (f_{SW}) vs R_T Value

f_{SW} (MHz)	R_T (kΩ)	f_{SW} (MHz)	R_T (kΩ)
0.3	301	1.7	52.3
0.4	226	1.8	49.9
0.5	182	1.9	46.4
0.6	154	2.0	44.2
0.7	133	2.1	42.2
0.8	118	2.2	40.2
0.9	102	2.3	38.3
1.0	93.1	2.4	36.5
1.1	84.5	2.5	34.8
1.2	76.8	2.6	33.2
1.3	71.5	2.7	32.4
1.4	64.9	2.8	30.9
1.5	60.4	2.9	29.4
1.6	56.2	3.0	28.7

The operating frequency of the LT8338 can be synchronized to an external clock source. By providing a clock signal into the SYNC/MODE pin, the LT8338 operates at the SYNC pulse frequency and automatically enters pulse-skipping mode operation at light load. If this feature is used, an R_T resistor should be chosen to program a switching frequency equal to, or slightly less than the SYNC pulse frequency. For example, if the synchronization signal is 500kHz or higher, the R_T should be selected for 500kHz. The slope compensation is set by the R_T value, while the minimum slope compensation required to avoid subharmonic oscillations is established by the inductor size, input voltage, and output voltage. Since the synchronization frequency will not change the slope of the inductor current waveform, if the inductor is large enough to avoid subharmonic oscillation at the frequency set by R_T, then the slope compensation will be sufficient for all synchronization frequencies.

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The input synchronization clock signal can be square wave, triangle wave, or sinusoidal wave. The input signal should have valleys that are below 1V and peaks above 2V. The minimum duration time that the input signal amplitude stays higher than the 2V threshold and lower than the 0.8V threshold, should be no less than 30ns.

Frequency Spread Spectrum Modulation

The LT8338 features spread spectrum operation to further reduce EMI/EMC emissions. The user can select frequency spectrum modulation with Burst Mode operation by connecting the SYNC/MODE pin to ground through a 100k resistor, or frequency spread modulation with pulse-skipping operation by connecting the SYNC/MODE pin to $INTV_{CC}$. When frequency spectrum modulation is selected and the converter operates at heavy load, the triangular frequency modulation varies the switching frequency between the value programmed by R_T to approximately 14% higher than that value. The modulation frequency is approximately 0.42% of the switching frequency. For example, when the LT8338 is programmed to 2MHz, the frequency will vary from 2MHz to 2.3MHz at a 9kHz rate. When operating at light load, frequency spread spectrum modulation is more effective in pulse-skipping mode than in Burst Mode operation, due to the fact that pulse-skipping operation maintains the switching frequency with spread spectrum down to a much lower load current compared to Burst Mode operation.

CTRL Resistor Network

The output voltage is internally set as shown in Equation 2.

$$V_{OUT} = V_{CTRL} \bullet 18 \qquad (2)$$

Typically, the CTRL pin voltage is programmed with a resistor divider between the $INTV_{CC}$ and ground (refer to the Block Diagram).

1% resistors are recommended to maintain output voltage accuracy. The current flowing in the divider acts as a load current of the internal LDO and will increase the no-load input current to the converter. If low input quiescent current and good light-load efficiency are desired, use large resistor values for the CTRL resistor divider.

V_{IN} to V_{OUT} PassThru Mode Operation

When V_{IN} rises above the regulated V_{OUT} voltage programmed by the CTRL pin voltage, the LT8338 boost converter enters PassThru operation, where the synchronous power switch MTOP (refer to the Block Diagram) is kept on continuously and power switch MBOT is kept off continuously. An internal charge pump circuit is activated to deliver sufficient current to the boost capacitor (CBST) to maintain the MTOP's gate drive voltage. In PassThru mode V_{OUT} is essentially shorted to V_{IN} by the inductor and power switch. When V_{IN} falls below V_{OUT} voltage, or the inductor conducts more than 300mA current from V_{OUT} to V_{IN}, LT8338 exits PassThru mode operation. If V_{OUT} is lower than the desired voltage, the normal boost switching operation resumes.

Switching Frequency Foldback when V_{IN} Approaches V_{OUT}

In some boost applications, V_{IN} may rise to a voltage very close to V_{OUT}. When this occurs, the switching regulator must operate at very low duty cycle to keep V_{OUT} in regulation. However, the minimum on-time limitation may prevent the switcher from attaining a sufficiently low duty cycle at the programmed switching frequency; as a result a typical boost converter may experience a large output ripple. LT8338 addresses this issue by adopting a switching frequency foldback function to smoothly decrease the switching frequency when its minimum on-time starts to limit the switcher from attaining a sufficiently low duty cycle. The typical switching waveforms when V_{IN} approaches V_{OUT} are shown in the Typical Performance Characteristics section.

Soft-Start

High peak switch currents during start-up may occur in switching regulators. Since V_{OUT} is far from its final value, the feedback loop is saturated and the regulator tries to charge the output capacitor as quickly as possible, resulting in large peak currents. A large surge current may cause inductor saturation or power switch failure.

The LT8338 utilizes a soft-start function to limit peak switch currents and output voltage (V_{OUT}) overshoot during start-up or recovery from a fault condition to

APPLICATIONS INFORMATION

prevent damage to external components or the load. As shown in the Block Diagram, the soft-start function controls the ramp of the power switch current by controlling the ramp of V_C through Q1. This allows the output capacitor to be charged gradually toward its final value while limiting the start-up peak currents. The typical start-up waveforms are shown in the Typical Performance Characteristics section.

Hot Plug

If the LT8338 boost converter is plugged into a live supply, V_{OUT} can ring to twice the V_{IN} voltage due to the resonant circuit composed by L, C2, and the body diode of MTOP (refer to the Block Diagram). If such overshoot exceeds the V_{OUT} rating, it needs to be limited to protect the load and the converter. In these conditions, a small diode (Schottky diode or silicon diode) can be connected between V_{IN} and V_{OUT} to deactivate the resonant circuit and limit V_{OUT} overshoot as shown in Figure 3. With the diode connected, the LT8338 boost is also more robust against output fault conditions such as output short circuit or overload, due to the diode's ability to divert a great amount of output current from the LT8338. The diode can be rated for about one-half to one-fifth the full load current since it only conducts current during start-up or output fault conditions.

Fault Protection

$INTV_{CC}$ undervoltage ($INTV_{CC} < 2.2V$), or thermal lockout ($T_J > 170°C$) will immediately stop the converter from switching, pull down V_C and reset soft-start. Faults are removed when $INTV_{CC} > 2.3V$, and the die temperature has dropped down to 165°C or lower. Once all faults are removed, the LT8338 will resume switching with a soft-started V_C inductor peak current limiting.

In addition, converter will stop switching immediately when V_{OUT} overvoltage ($V_{OUT} > 41.4V$) happens, and will resume switching once V_{OUT} is lower than 40.6V.

Duty Cycle Consideration

The LT8338 minimum on-time, minimum off-time and switching frequency define the allowable minimum and

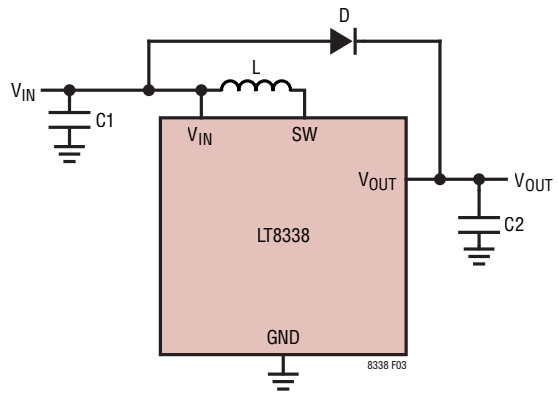

Figure 3. A Simplified LT8338 Power Stage with a Diode Added Between V_{IN} and V_{OUT}

maximum duty cycles of the converter (see Minimum On-Time, Minimum Off-Time, and Switching Frequency in the Electrical Characteristics table) as:

$$\text{Minimum Allowable Duty Cycle} = \text{Minimum On-Time}_{(MAX)} \bullet f_{OSC(MAX)}$$

$$\text{Maximum Allowable Duty Cycle} = 1 - \text{Minimum Off-Time}_{(MAX)} \bullet f_{OSC(MAX)}$$

The required switch duty cycle range for a boost converter operating in continuous conduction mode (CCM) can be calculated using Equation 3.

$$D_{MIN} = \frac{V_{OUT} - V_{IN(MAX)}}{V_{OUT}} \qquad (3)$$

$$D_{MAX} = \frac{V_{OUT} - V_{IN(MIN)}}{V_{OUT}}$$

If the above duty cycle calculations for a given application violate the minimum and/or maximum allowed duty cycles, operation in discontinuous conduction mode (DCM) may provide a solution. For the same V_{IN} and V_{OUT} levels, operation in DCM does not demand as low a duty cycle as in CCM. DCM also allows higher duty cycle operation than CCM. The additional advantage of DCM is the removal of the limitations to inductor value and duty cycle required to avoid sub-harmonic oscillations and the right half plane zero (RHPZ). While DCM provides these

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benefits, the trade-off is higher inductor peak current, lower available output power and reduced efficiency.

Inductor Selection

The inductor peak-to-peak current ripple ΔI_{SW} has a direct effect on the choice of the inductor value, the converter's maximum output current capability, and the light load efficiency in Burst Mode operation. Smaller values of ΔI_{SW} increase output current capability and light load efficiency in Burst Mode operation, but require large inductances and reduces the current loop gain (the converter will approach voltage mode). Larger values of ΔI_{SW} provide fast transient response and allow the use of low inductances, but result in higher input current ripple and greater core losses, reduce the light load efficiency in Burst Mode operation, and reduce output current capability.

Given an operating input voltage range, and having chosen the operating frequency and ripple current in the inductor, the inductor value of the boost converter can be determined using the following equation:

$$L = \frac{V_{IN(MIN)}}{\Delta I_{SW} \bullet f} \bullet D_{MAX} \quad (4)$$

here the ripple current ΔI_{SW} can be set to 0.2A as a good starting point. The peak inductor current is the switch current limit (1.2A typical). The user should choose an inductor having a sufficient saturation and RMS current rating, and a low DCR to minimize I^2R power losses.

Input Capacitor Selection

Bypass the input of the LT8338 circuit with a ceramic capacitor of type X7R or X5R. The value of the input bypass capacitor is a function of the source impedance, and in general, the higher the source impedance, the higher the required input capacitance. The capacitor value depends on the input current ripple as well. The input ripple current in a boost converter is relatively low (compared with the output ripple current) because this current is continuous. A 2.2µF to 10µF ceramic capacitor is adequate to bypass the LT8338 and will easily handle the ripple current. If the input power source has high impedance or there is significant inductance due to long wires or cables, additional bulk capacitance may be necessary. This can be provided with a low performance electrolytic capacitor.

The voltage rating of the input capacitor, C1, should comfortably exceed the maximum input voltage. Although ceramic capacitors can be relatively tolerant of overvoltage conditions, aluminum electrolytic capacitors are not. Be sure to characterize the input voltage for any possible overvoltage transients that could apply excess stress to the input capacitors.

Output Capacitor Selection

The output capacitor has two essential functions. First, it filters LT8338's discontinuous top switch current to produce the DC output. In this role it determines the output ripple, and thus low impedance at the switching frequency is important. The second function is to store energy in order to satisfy transient loads and stabilize the LT8338's control loop. The X5R or X7R type ceramic capacitors have very low equivalent series resistance (ESR), which provides low output ripple and good transient response. Transient performance can be improved with higher value output capacitance. Increasing the output capacitance will also decrease the output voltage ripple. Lower values of output capacitance can be used to save space and cost but transient performance will suffer and may cause loop instability.

A 4.7µF ceramic capacitor is adequate for the LT8338 output capacitor. This ceramic should be placed near to V_{OUT}/GND. See the Board Layout section for more details. Note that larger output capacitance is required when a lower switching frequency is used. When choosing a capacitor, special attention should be given to capacitor's data sheet to calculate the effective capacitance under the relevant operating conditions of voltage bias and temperature. A physically larger capacitor or one with a higher voltage rating may be required. For good starting values, refer to the Typical Application section.

Board Layout

Figure 4 shows a recommended PCB layout. For more details and PCB design files refer to the Demo Board guide for the LT8338.

APPLICATIONS INFORMATION

The output capacitor, along with the inductor and input capacitor, should be placed on the same side of the circuit board, and their connections should be made on that layer. Place a local, unbroken power ground plane under the application circuit on the layer closest to the surface layer. The SW and BST nodes should be as small as possible.

Keep the CTRL and R_T nodes small so that the ground traces will shield them from the noise generated by the SW and BST nodes. The exposed pad on the bottom of the package should be soldered to GND to reduce thermal resistance to ambient temperature. To keep thermal resistance low, extend the power ground plane from GND as much as possible and add thermal vias to additional power ground planes within the circuit board and on the bottom side.

Thermal Considerations

Care should be taken in the layout of the PCB to ensure good heat sinking of the LT8338. The power ground plane should consist of large copper layers with thermal vias; these layers spread heat dissipated by the LT8338. Placing additional vias can reduce thermal resistance further. The maximum load current should be derated as the ambient temperature approaches the maximum junction temperature rating. Power dissipation within the LT8338 can be estimated by calculating the total power loss from an efficiency measurement and subtracting the inductor loss. The junction temperature can be calculated by multiplying the total LT8338 power dissipation by the thermal resistance from junction to ambient and adding the ambient temperature. The LT8338 includes internal overtemperature protection that is intended to protect the device during momentary overload conditions. The overtemperature protection triggers the internal soft-start when junction temperature exceeds 170°C. The maximum rated junction temperature is exceeded when this protection is active. Continuous operation above the specified absolute maximum operating junction temperature (see Absolute Junction Ratings section) may impair device reliability or permanently damage the device.

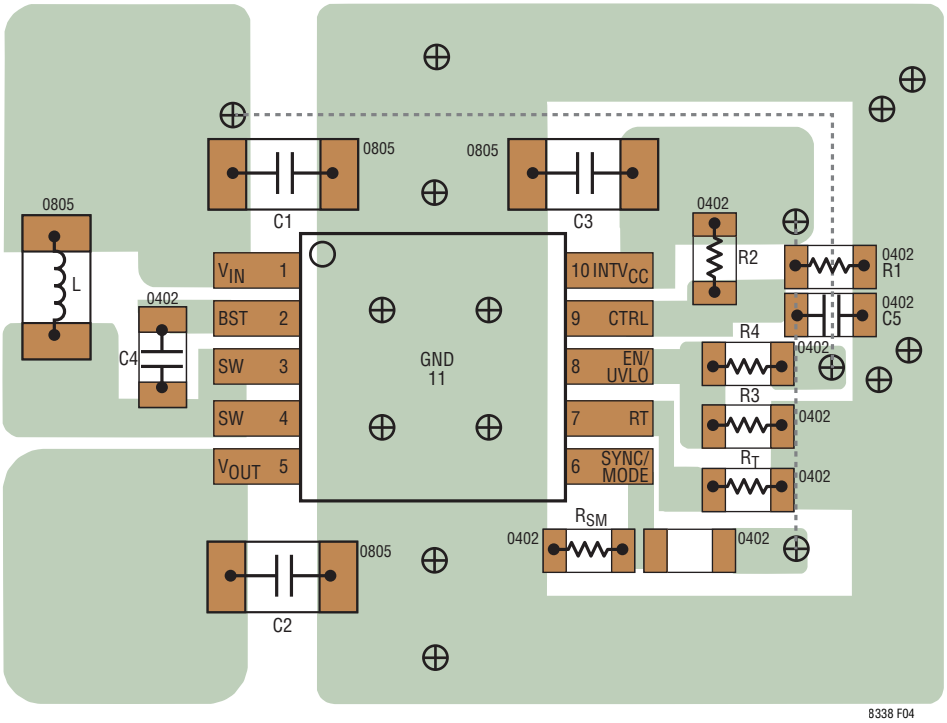
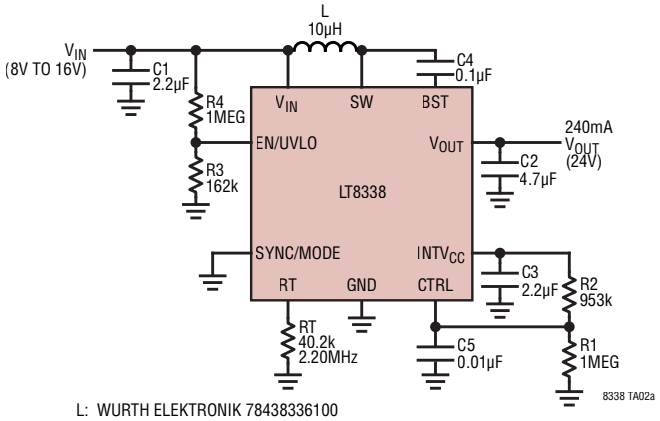


Figure 4. A Recommended PCB Layout for the LT8338

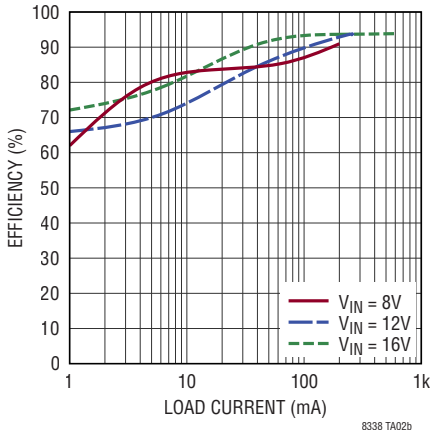
TYPICAL APPLICATION

8V to 16V Input, 24V Output Boost Converter

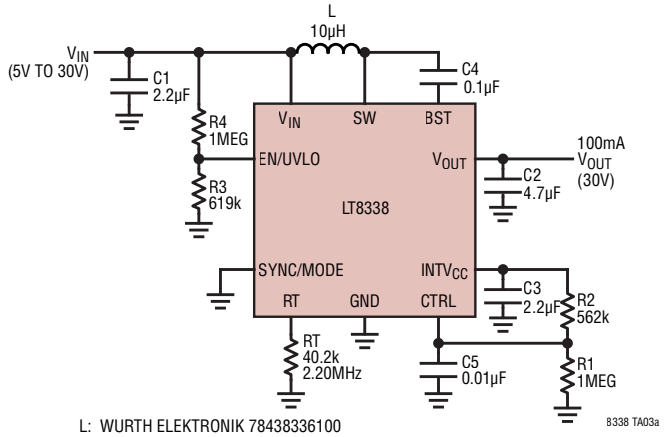


L: WURTH ELEKTRONIK 78438336100
C1: TDK CGA4J3X7R1H225K125AB
C2: TDK CGA4J1X7R1H475K125AC

Efficiency

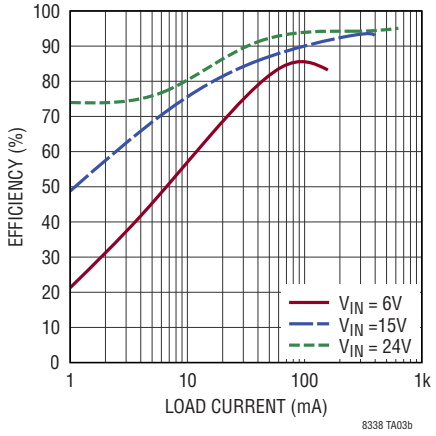


5V to 30V Input, 30V Output Boost Converter



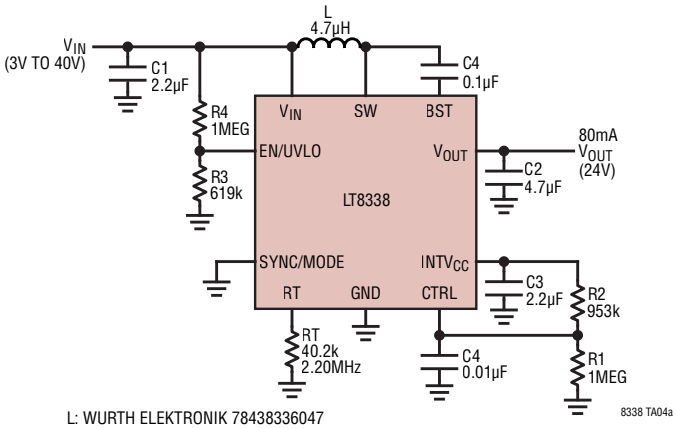
L: WURTH ELEKTRONIK 78438336100
C1: TDK CGA4J3X7R1H225K125AB
C2: TDK CGA4J1X7R1H475K125AC

Efficiency



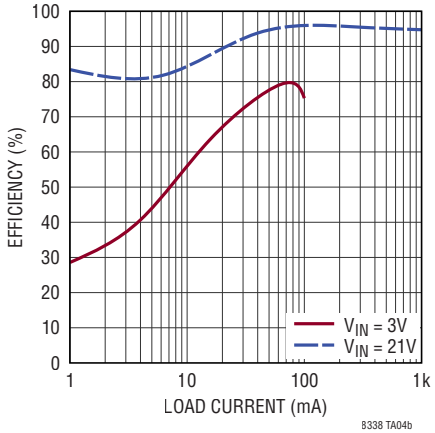
TYPICAL APPLICATION

3V to 40V Input, 24V Output Pre-Boost Converter

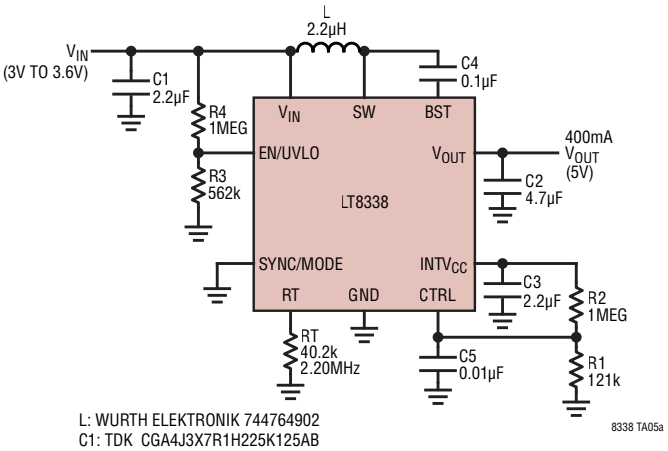


L: WURTH ELEKTRONIK 78438336047
C1: TDK CGA4J3X7R1H225K125AB
C2: TDK CGA4J1X7R1H475K125AC

Efficiency

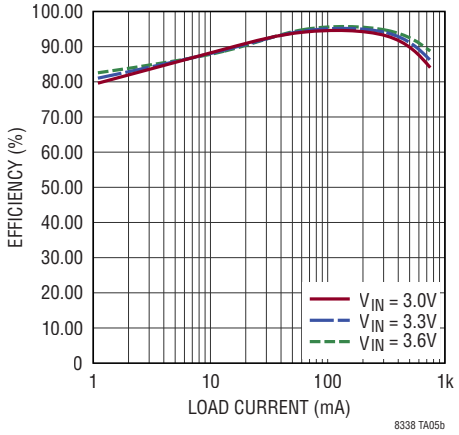


3V to 3.6V Input, 5V Output Boost Converter



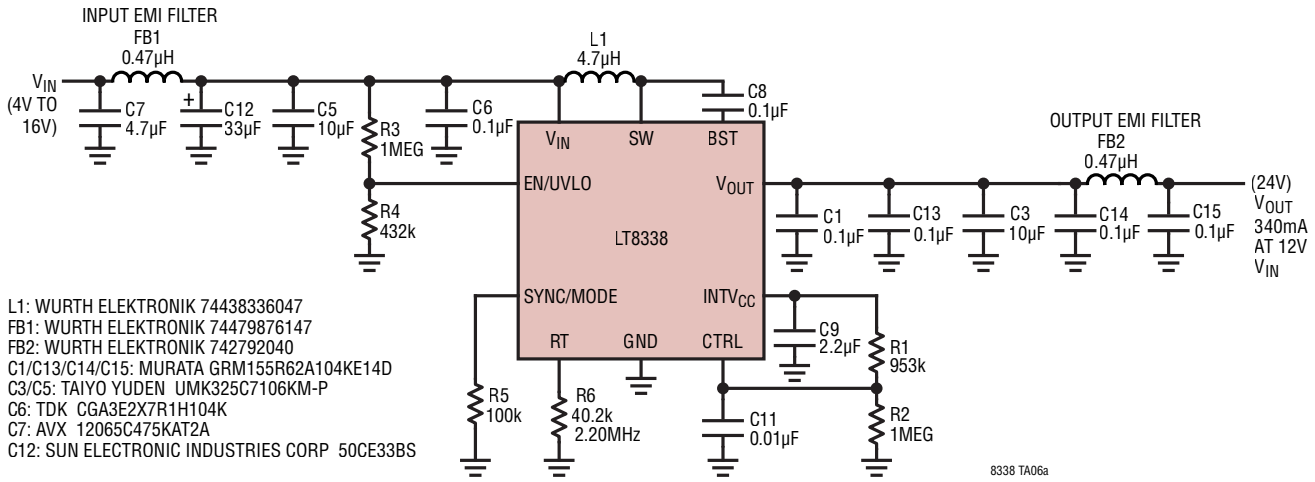
L: WURTH ELEKTRONIK 744764902
C1: TDK CGA4J3X7R1H225K125AB
C2: TDK CGA4J1X7R1H475K125AC

Efficiency



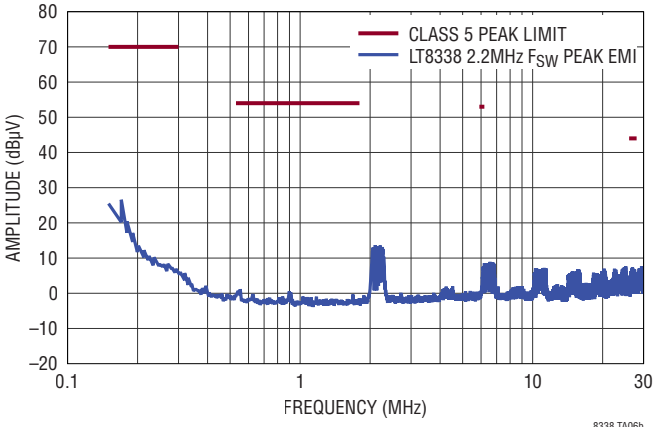
TYPICAL APPLICATION

4V to 16V Input, 24V Output Micropower Synchronous Boost Converter with SSFM



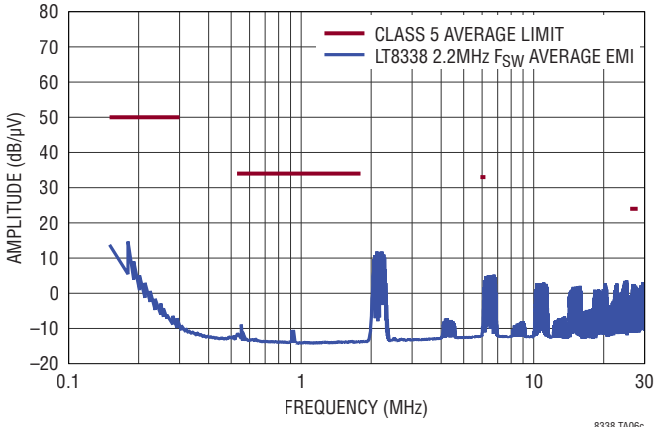
L1: WURTH ELEKTRONIK 74438336047
FB1: WURTH ELEKTRONIK 74479876147
FB2: WURTH ELEKTRONIK 742792040
C1/C13/C14/C15: MURATA GRM155R62A104KE14D
C3/C5: TAIYO YUDEN UMK325C7106KM-P
C6: TDK CGA3E2X7R1H104K
C7: AVX 12065C475KAT2A
C12: SUN ELECTRONIC INDUSTRIES CORP 50CE33BS

Conducted EMI Performance (CISPR25 Class 5 Peak)



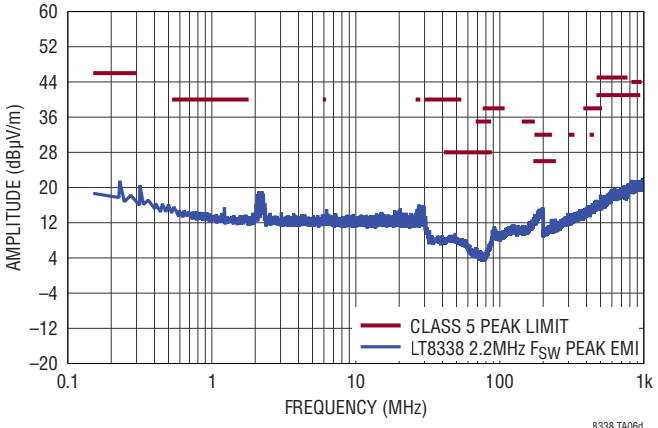
12V INPUT TO 24V OUTPUT AT 340mA, F_{SW} = 2.2MHz

Conducted EMI Performance (CISPR25 Class 5 Average)



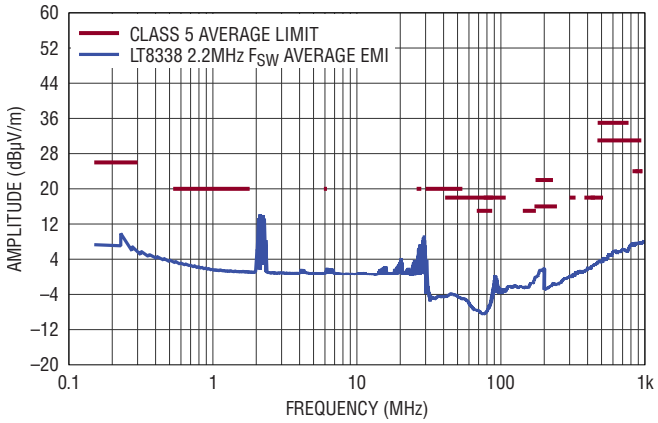
12V INPUT TO 24V OUTPUT AT 340mA, F_{SW} = 2.2MHz

Radiated EMI Performance (CISPR25 Class 5 Peak)



12V INPUT TO 24V OUTPUT AT 340mA, F_{SW} = 2.2MHz

Radiated EMI Performance (CISPR25 Class 5 Average)

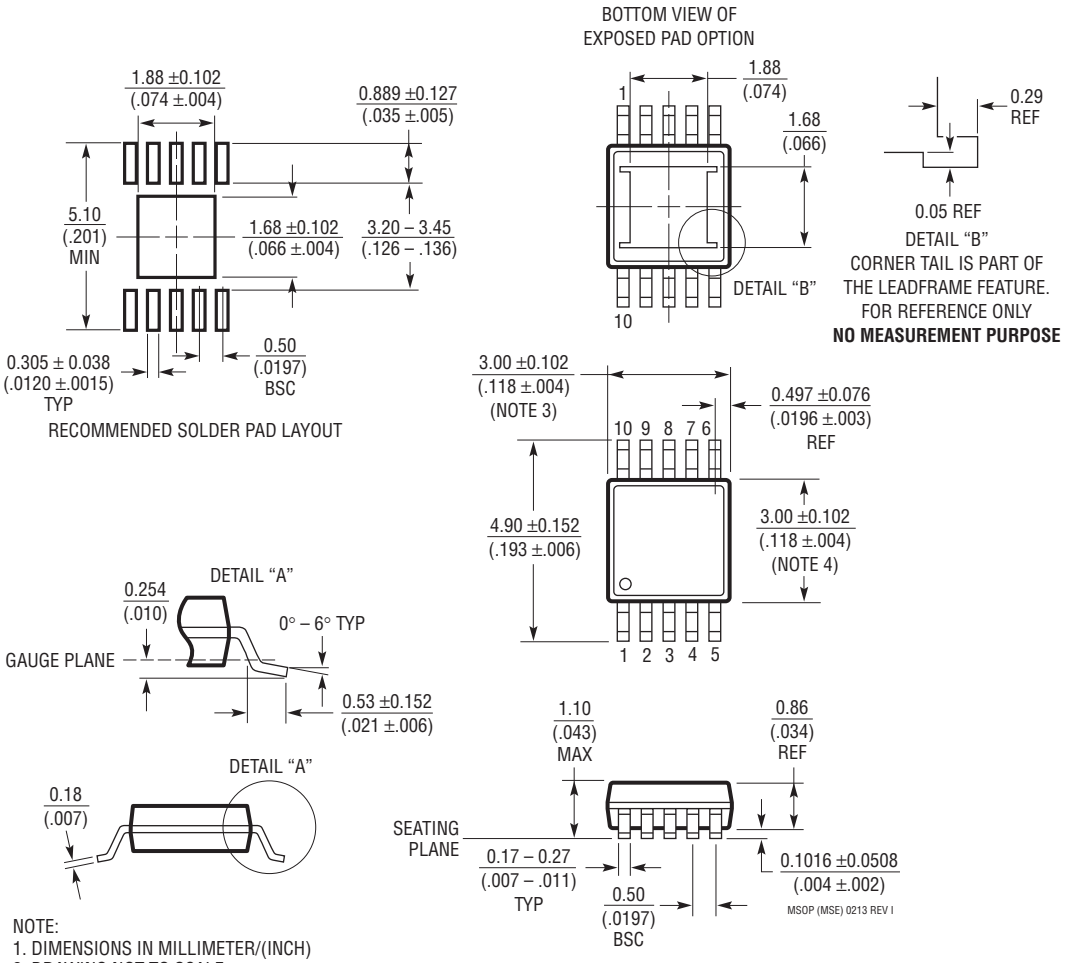


12V INPUT TO 24V OUTPUT AT 340mA, F_{SW} = 2.2MHz

Rev. A

PACKAGE DESCRIPTION

MSE Package
10-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1664 Rev I)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD
   SHALL NOT EXCEED 0.254mm (.010") PER SIDE.

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
0	3/21	Initial release	—
A	3/24	Updated Electrical Characteristics	4

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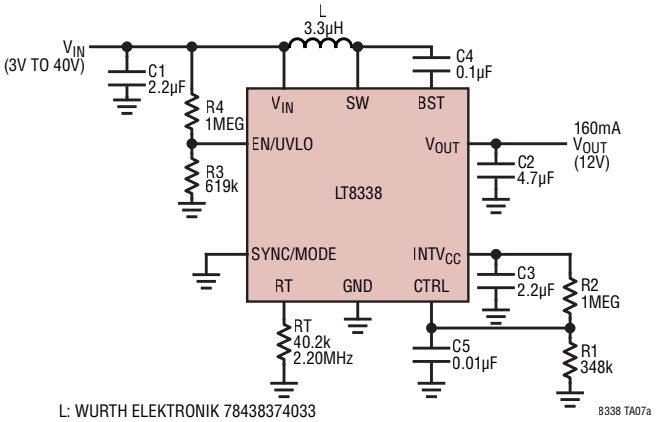
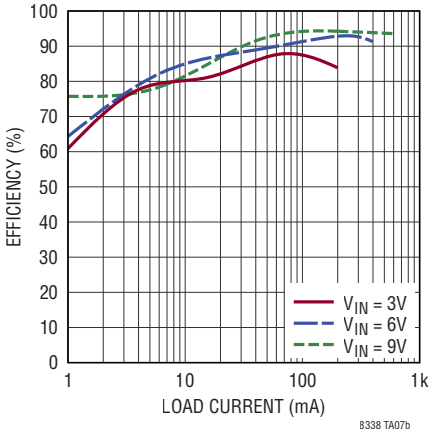
TYPICAL APPLICATION

3V to 40V Input, 12V Output Pre-Boost Converter



L: WURTH ELEKTRONIK 78438374033
C1: TDK CGA4J3X7R1H225K125AB
C2: TDK CGA4J1X7R1H475K125AC

Efficiency



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT8336	Boost, Monolithic Converter with 2.5A/40 Switch	2.7V ≤ V_{IN} ≤ 40V, Current Mode Control, 300kHz to 3MHz Programmable Operation Frequency, QFN-16 Package
LT8335	28V, 2A, Low IQ Boost/SEPIC/Inverting 2MHz Converter	V_{IN} = 3V to 25V, $V_{OUT(MAX)}$ = 25V, I_Q = 6µA (Burst Mode Operation), 3mm × 2mm DFN package
LT8362	60V, 2A, Low I_Q Boost/SEPIC/Inverting Converter	V_{IN} = 2.8V to 60V, $V_{OUT(MAX)}$ = 60V, I_Q = 9µA (Burst Mode Operation), MSOP-16(12)E, 3mm × 3mm DFN-8 packages
LT8330	60V, 1A, Low I_Q Boost/SEPIC/Inverting 2MHz Converter	V_{IN} = 3V to 40V, $V_{OUT(MAX)}$ = 60V, I_Q = 6µA (Burst Mode Operation), 6-Lead TSOT-23, 3mm × 2mm DFN packages
LT3958	High Input Voltage, Boost, Flyback, SEPIC and Inverting Converter with 3.5A/80V Switch	5V ≤ V_{IN} < 80V, Current Mode Control, 100kHz to 1MHz Programmable Operation Frequency, 5mm × 6mm QFN-36 Package
LT3757A	Boost, Flyback, SEPIC and Inverting Controller	2.9V ≤ V_{IN} ≤ 40V, Current Mode Control, 100kHz to 1MHz Programmable Operation Frequency, 3mm × 3mm DFN-10 and MSOP-10E Package
LT3758	Boost, Flyback, SEPIC and Inverting Controller	5.5V ≤ V_{IN} ≤ 100V, Current Mode Control, 100kHz to 1MHz Programmable Operation Frequency, 3mm × 3mm DFN-10 and MSOP-10E Package

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