Dual Channel 8.5A, 18V, Synchronous Step-Down Silent Switcher with 16µA Quiescent Current

FEATURES

- **Silent Switcher®2 Architecture:**
  - **Ultralow EMI on Any PCB**
  - **Eliminates PCB Layout Sensitivity**
  - **Internal Bypass Capacitors Reduce Radiated EMI**
  - **Spread Spectrum Frequency Modulation**
- **8.5A DC from Each Channel Simultaneously**
- **Up to 12A on Either Channel**
- **Ultralow Quiescent Current Burst Mode® Operation:**
  - **16µA I_Q Regulating $12V_{IN}$ to $3.3V_{OUT}$ (Both Channels)**
  - **Output Ripple <10mV_{P-P}**
- **±1.2% 600mV Feedback Voltage with Remote Sense**
- **Output Current Monitor Pins with Current Limiting**
- Forced Continuous Mode
- CLKOUT for Up to 4-Phase Operation
- 93.6% Efficiency at 6A, $3.3V_{OUT}$ from $12V_{IN}$ at 1MHz
- 85.6% Efficiency at 6A, $1.0V_{OUT}$ from $12V_{IN}$ at 1MHz
- Fast Minimum Switch-On Time: 20ns
- Adjustable and Synchronizable: 300kHz to 3MHz
- Small 4mm × 7mm 36-Pin LQFN Package
- AEC-Q100 Qualified for Automotive Applications

APPLICATIONS

- Server Power Applications
- General Purpose Step-Down

DESCRIPTION

The LT®8652S is a dual step-down regulator that delivers up to 8.5A of continuous current from both channels and supports loads up to 12A from each channel. The LT8652S uses second generation Silent Switcher technology including integrated bypass capacitors to deliver a high frequency, high efficiency, small solution with excellent EMI performance. The LT8652S is ideal for noise sensitive applications such as PLLs and high bandwidth data and communications systems.

The fast, clean, low overshoot switching edges enable high efficiency operation even at high switching frequencies, enabling a wide control loop bandwidth for fast transient response. Output current monitoring and limiting allows inductors to be selected for the maximum output current in a given application. Differential output voltage sensing provides accurate voltage regulation at the point of load for high current applications. The two channels can be combined to deliver 17A, and two LT8652S ICs can be combined for a 4-phase, 34A supply.

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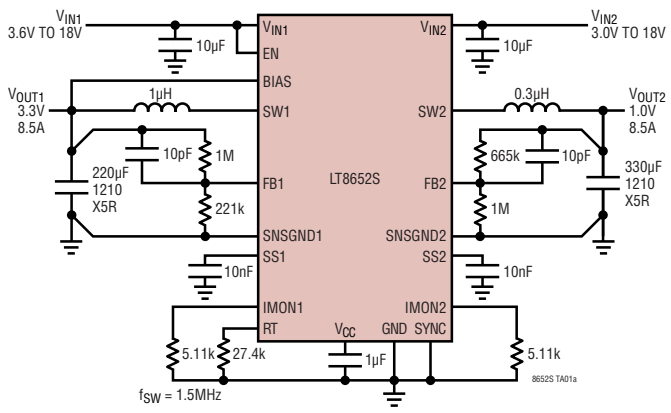
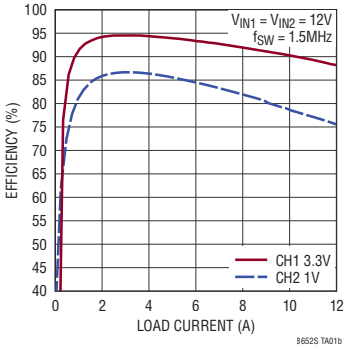
TYPICAL APPLICATION

3.3V/8.5A, 1.0V/8.5A 1.5MHz Step-Down Converter



Efficiency

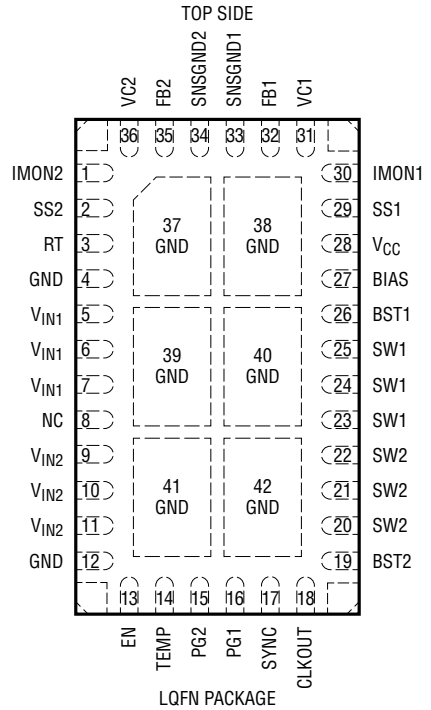


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN1}, V_{IN2}, EN, PG1, PG2 ..... 18V
BIAS 12V
FB1, FB2, VC1, VC2, SS1, SS2, IMON1, IMON2 ..... 4V
SYNC. 6V
Operating Junction Temperature Range (Note 2)
LT8652SE ..... –40°C to 125°C
LT8652SI ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Maximum Reflow (Package Body) Temperature ... 260°C

PIN CONFIGURATION



LQFN PACKAGE
36-LEAD (4mm × 7mm × 0.94mm)

θ_{JA} = 18°C/W, θ_{JCTOP} = 24.6°C/W, θ_{JCbot} = 4.2°C/W
EXPOSED PAD (PINS 37, 38, 39, 40, 41, 42) ARE GND, MUST BE SOLDERED TO PCB

NOTES:
1. θ VALUES ARE DETERMINED BY SIMULATION PER JESD51 CONDITIONS
2. θ_{JA} VALUE IS OBTAINED WITH DEMO BOARD

ORDER INFORMATION

PART NUMBER	TAPE AND REEL	PAD OR BALL FINISH	PART MARKING* DEVICE	PART MARKING* FINISH CODE	PACKAGE** TYPE	MSL RATING	TEMPERATURE RANGE (SEE NOTE 2)
LT8652SEV#PBF	LT8652SEV#TRPBF	Au (RoHS)	8652SV	e4	LQFN	3	–40°C to 125°C
LT8652SIV#PBF	LT8652SIV#TRPBF	Au (RoHS)	8652SV	e4	LQFN	3	–40°C to 125°C

AUTOMOTIVE PRODUCTS*

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION				TEMPERATURE RANGE
LT8652SEV#WPBF	LT8652SEV#WTRPBF	Au (RoHS)	8652SV	e4	LQFN	3	–40°C to 125°C
LT8652SIV#WPBF	LT8652SIV#WTRPBF	Au (RoHS)	8652SV	e4	LQFN	3	–40°C to 125°C

- Device temperature grade is indicated by a label on the shipping container.
- Pad or ball finish code is per IPC/JEDEC J-STD-609.

**The LT8652S package has the same dimensions as a standard 4mm × 7mm QFN package.

*LQFN is Laminate Package with QFN footprint

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

**Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Input Voltage		●		2.6	3.0	V
V_{IN1} Quiescent Current in Shutdown	V_{EN} = 0V, V_{SYNC} = 0V			6	15	µA
V_{IN1} Quiescent Current in Sleep with Internal Compensation	V_{EN} = 2V, V_{FB1} = V_{FB2} > 0.6V, V_{VC1} = V_{VC2} = V_{CC}, V_{SYNC} = 0V	 ●		16	30 100	µA µA
V_{IN1} Quiescent Current in Sleep with External Compensation	V_{EN} = 2V, V_{FB1} = V_{FB2} > 0.6V, V_{VC1} = V_{VC2} = FLOAT, V_{SYNC} = 0V	 ●		210	260 300	µA µA
V_{IN} Current in Regulation	V_{IN} = 6, V_{OUT} = 0.6, Output Load = 50mA, V_{SYNC} = 0V			7	10	mA
Feedback Reference Voltage		 ●	596 592.8	600 600	604 607.2	mV mV
Feedback Voltage Line Regulation	V_{IN} = 3.0V to 18V	●		0.004	0.02	%/V
Feedback Pin Input Current	V_{FB} = 0.6V		–20		20	nA
Minimum On-Time	I_{LOAD} = 4A, SYNC = FLOAT	●		20	45	ns
Oscillator Frequency	R_T = 143k R_T = 60.4k R_T = 20k	● ● ●	255 660 1.85	300 700 2.00	345 740 2.15	kHz kHz MHz
Top Power NMOS Current Limit		●	22	26.5	32	A
Bottom Power NMOS Current Limit			12.5	16.5	20.5	A
Top Power NMOS $R_{DS(ON)}$				24		mΩ
Bottom Power NMOS $R_{DS(ON)}$				8		mΩ
SW Leakage Current	V_{IN} = 18V, V_{SW} = 0V,18V		–15		15	µA
EN/UV Pin Threshold	EN/UV Falling	●	0.76	0.8	0.84	V
EN/UV Pin Hysteresis				20		mV
EN/UV Pin Current	$V_{EN/UV}$ = 2V		–20		20	nA
PG Upper Threshold Offset from V_{FB}	V_{FB} Rising	●	3	6.5	11	%
PG Lower Threshold Offset from V_{FB}	V_{FB} Falling	●	–3	–7	–11	%
PG Hysteresis				0.5		%
PG Leakage	V_{PG} = 3.3V		–40		40	nA
PG Pull-Down Resistance	V_{PG} = 0.1V	●		630	1300	Ω
SYNC Threshold	SYNC DC and Clock Low Level Voltage SYNC DC High Level Voltage SYNC Clock High Level Voltage		0.4		 2.8 1.5	V V V
SYNC Pin Current	V_{SYNC} = 6V			60		µA
TR/SS Source Current		●	1.0	2.0	3.0	µA
TR/SS Pull-Down Resistance	Fault Condition, TR/SS = 0.1V			200		Ω
Error Amplifier Transconductance	VC = 1.2V			1.4		mS
VC Source Current	V_{FB} = 0.4V, V_{VC} = 1.2V			200		µA
VC Sink Current	V_{FB} = 0.8V, V_{VC} = 1.2V			225		µA
VC Pin to Switch Current Gain				15		A/V
TEMP Output Voltage	I_{TEMP} = 0µA, Temperature = 25°C I_{TEMP} = 0µA, Temperature = 125°C			250 1250		mV mV
IMON Current	I_{SW} = 2A, 12% Duty Cycle I_{SW} = 6A, 12% Duty Cycle	 ●	27 77	30 82	33 87	µA µA
MON Pin Limit Regulation Voltage		●	0.95	1.00	1.05	V

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

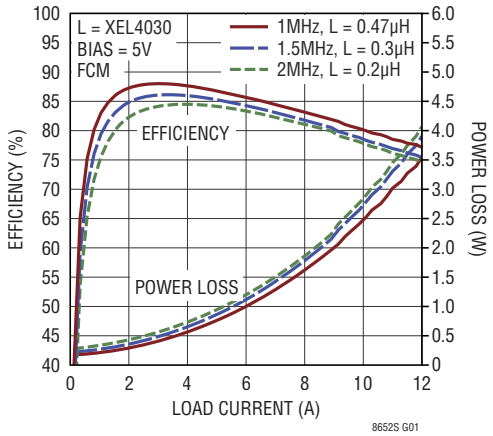
Note 2: The LT8652SE is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT8652SI is guaranteed over the full –40°C to 125°C operating junction temperature range. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperatures greater than 125°C. The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (P_D, in watts) according to the formula:

$T_J = T_A + (P_D \bullet \theta_{JA})$, where θ_{JA} (in °C/W) is the package thermal impedance.

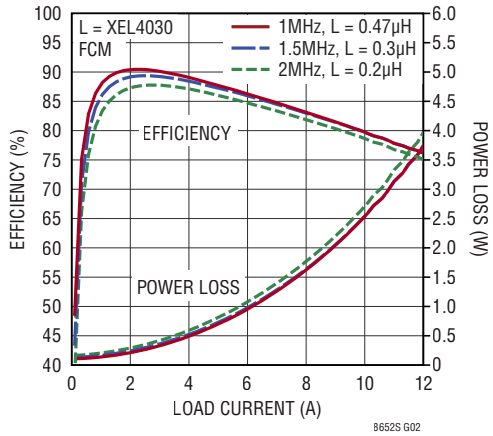
Note 3: This IC includes overtemperature protection that is intended to protect the device during overload conditions. Junction temperature will exceed 150°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

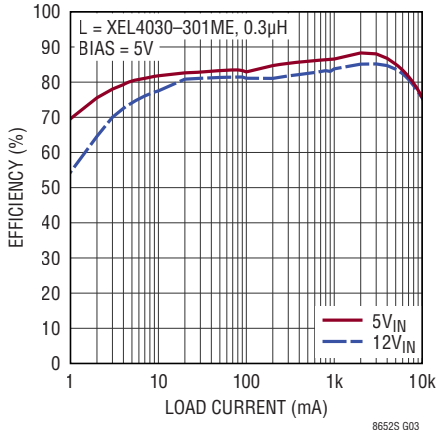
12V_{IN} to 1.0V_{OUT} Efficiency



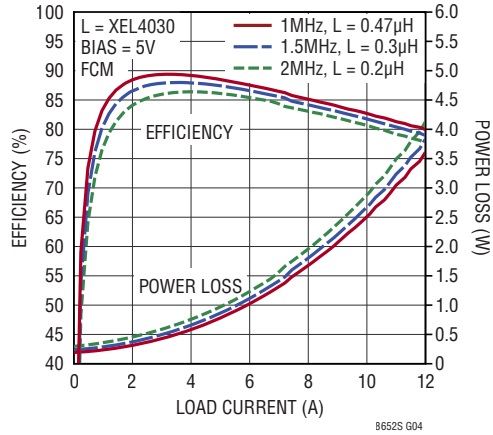
5.0V_{IN} to 1.0V_{OUT} Efficiency



1.0V_{OUT} Efficiency—Burst Mode Operation

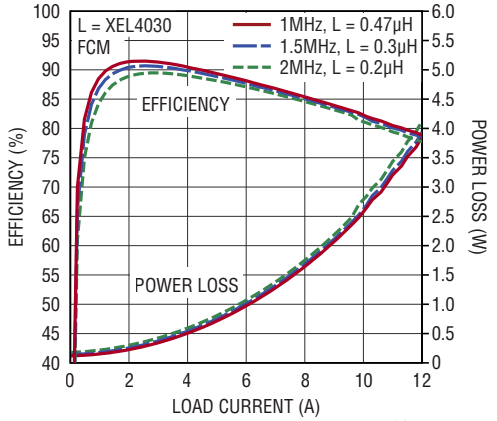


12.0V_{IN} to 1.2V_{OUT} Efficiency

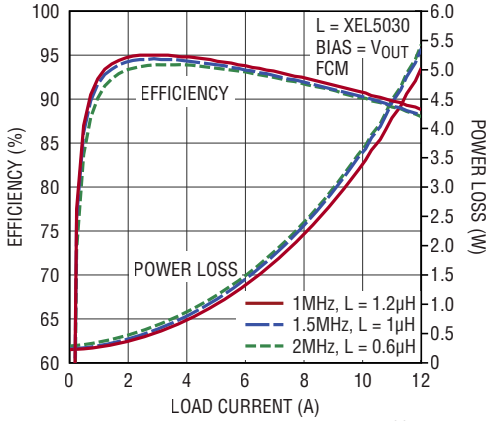


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

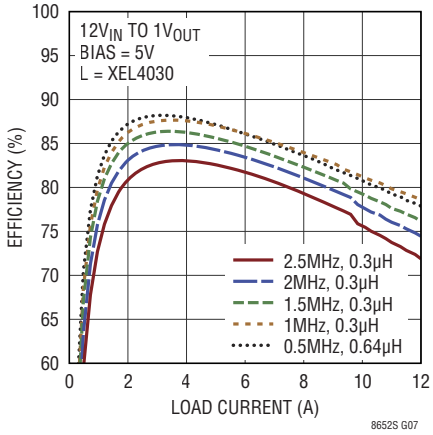
5.0V_{IN} to 1.2V_{OUT} Efficiency



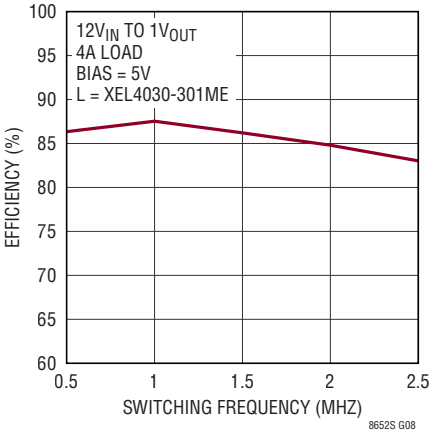
12.0V_{IN} to 3.3V_{OUT} Efficiency



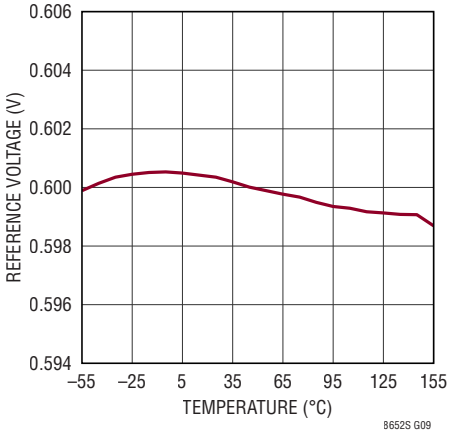
Efficiency at Different f_{SW}



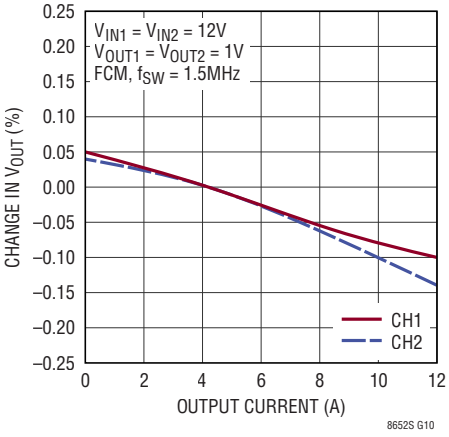
Efficiency vs f_{SW}



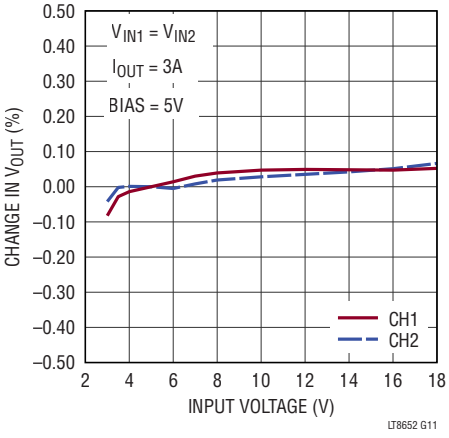
Reference Voltage



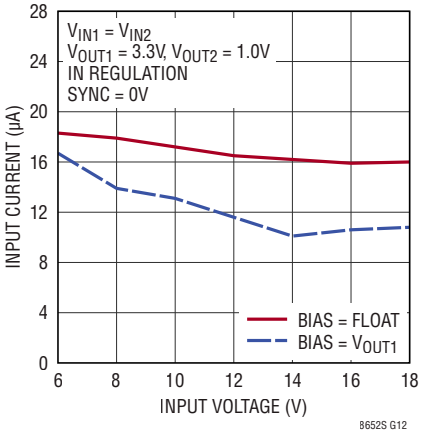
Load Regulation



Line Regulation



No Load Supply Current with Internal Compensation



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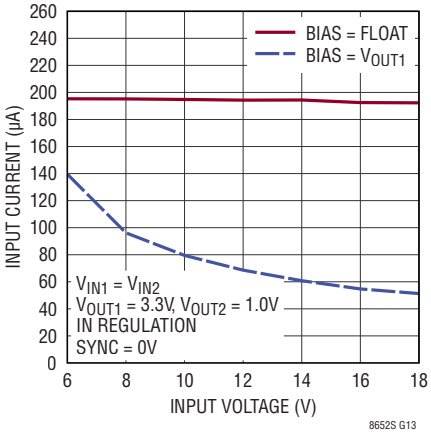
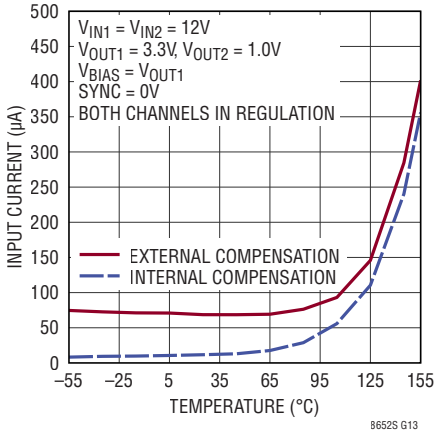
No Load Supply Current with External Compensation

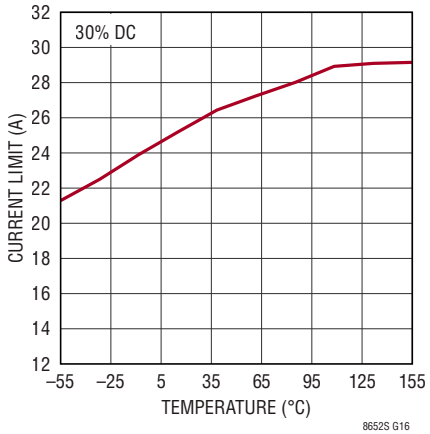


No Load Supply Current

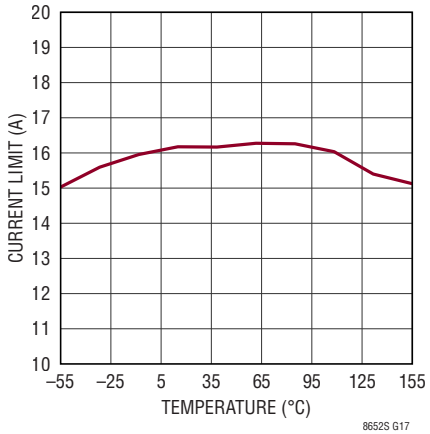


Top FET Current Limit

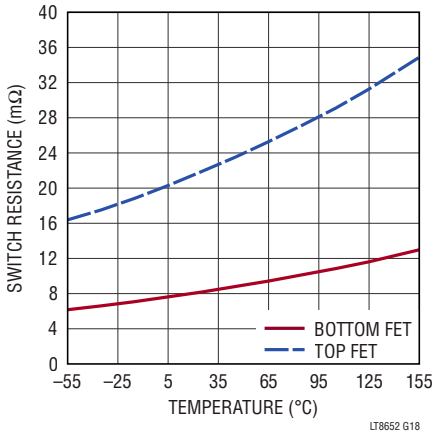
Top FET Current Limit



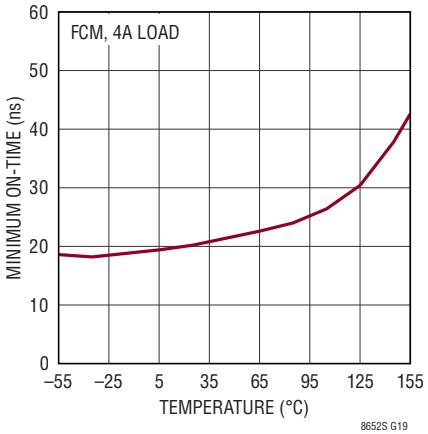
Bottom FET Current Limit



Switch Resistance



Minimum On-Time



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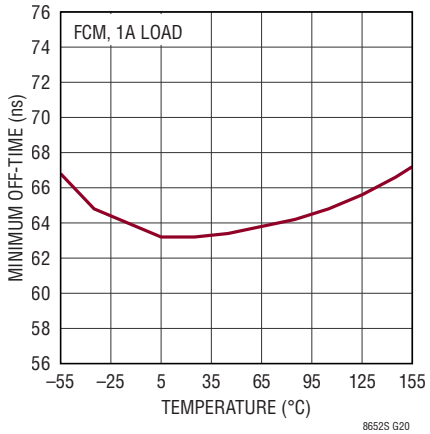
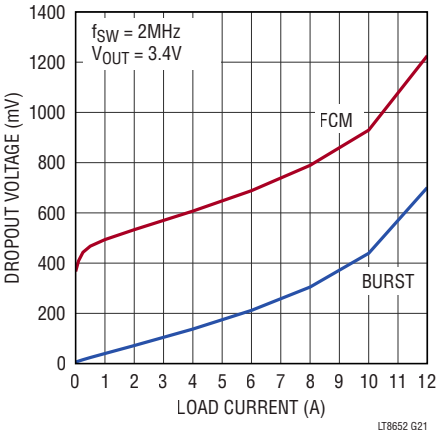
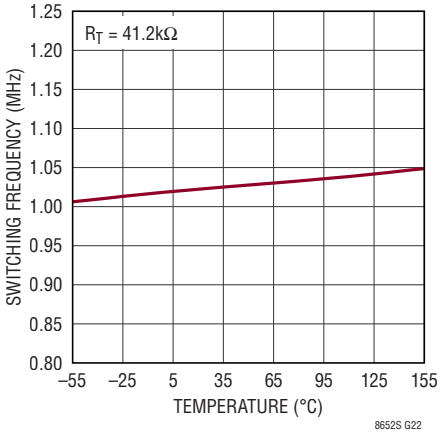


Dropout Voltage

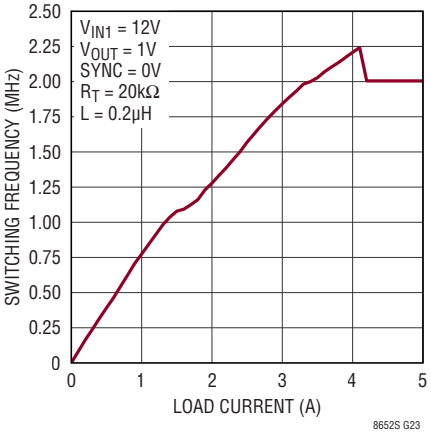


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

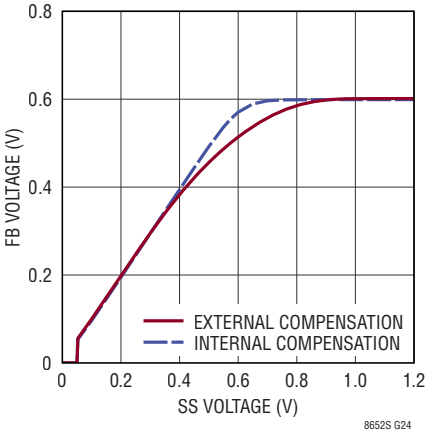
Switching Frequency



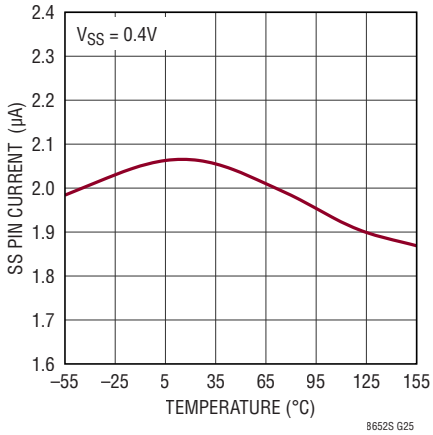
Burst Frequency



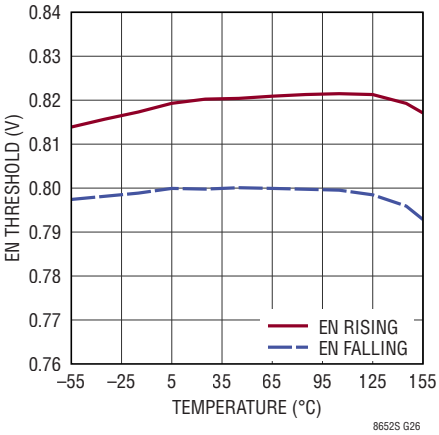
Soft-Start Tracking



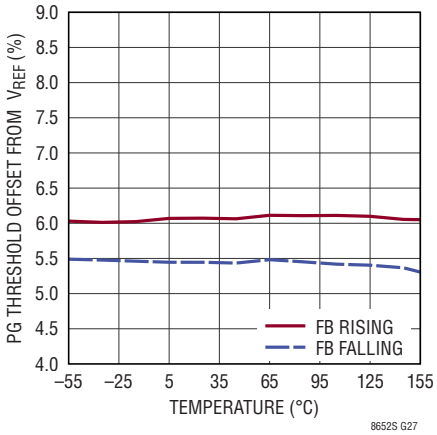
Soft-Start Current



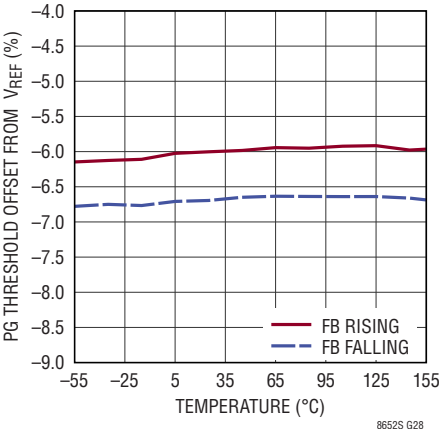
EN Pin Thresholds



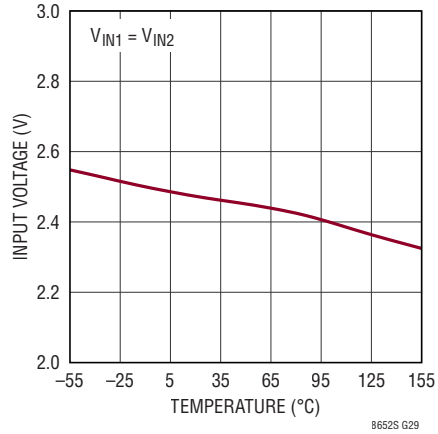
PG High Thresholds



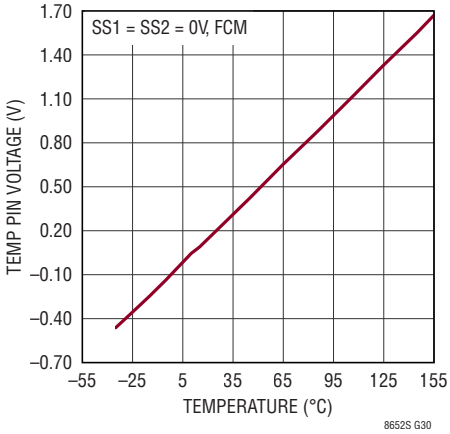
PG Low Thresholds



Minimum Input Voltage



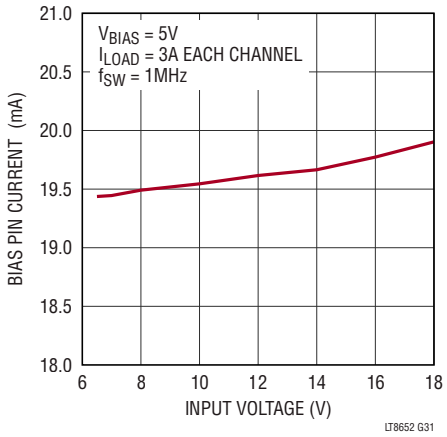
Temperature Monitor Pin



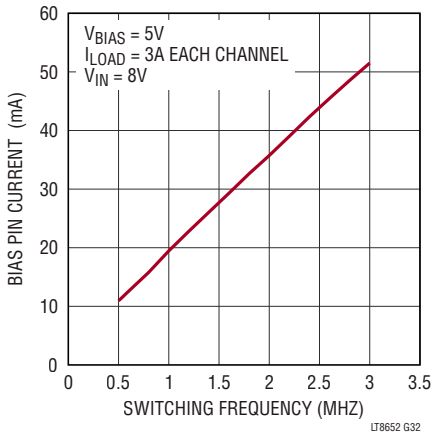
BELOW 5°C: 100kΩ RESISTOR FROM TEMP TO –4V
ABOVE 5°C: FLOAT TEMP

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

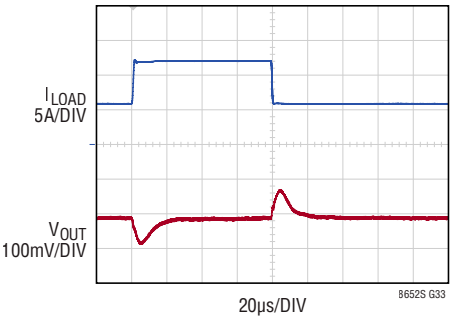
Bias Pin Current



Bias Pin Current

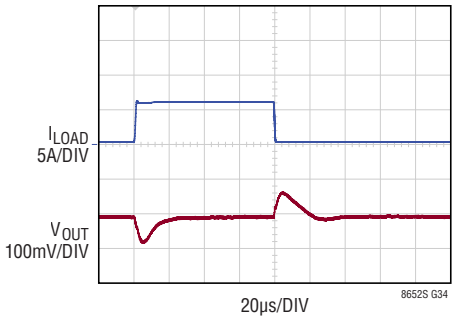


LT8652S Transient Response Internal Compensation



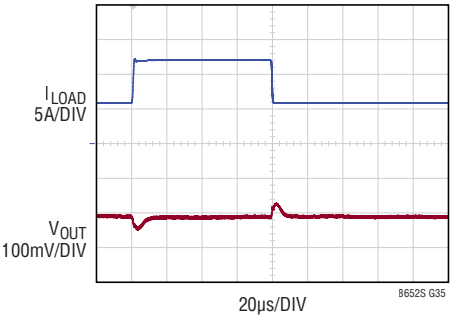
6A TO 12A TRANSIENT
$12V_{IN}$ TO $1V_{OUT}$
C_{OUT} = 340µF
FCM, f_{SW} = 2MHz

LT8652S Transient Response Internal Compensation



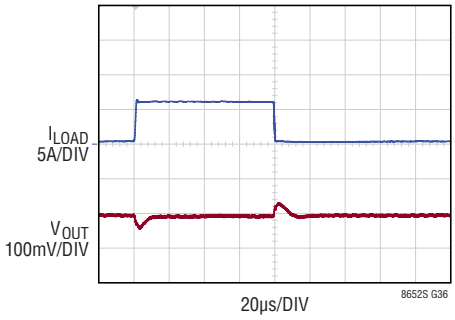
500mA TO 6A TRANSIENT
$12V_{IN}$ TO $1V_{OUT}$
C_{OUT} = 340µF
FCM, f_{SW} = 2MHz

LT8652S Transient Response External Compensation



6A TO 12A TRANSIENT
$12V_{IN}$ TO $1V_{OUT}$
C_{OUT} = 340µF
FCM, f_{SW} = 2MHz
C_C = 220pF, R_C = 17.1kΩ

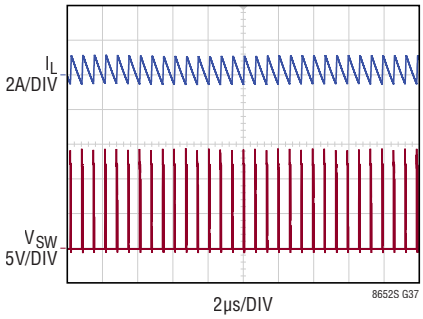
LT8652S Transient Response External Compensation



500mA TO 6A TRANSIENT
$12V_{IN}$ TO $1V_{OUT}$
C_{OUT} = 340µF
FCM, f_{SW} = 2MHz
C_C = 220pF, R_C = 17.1kΩ

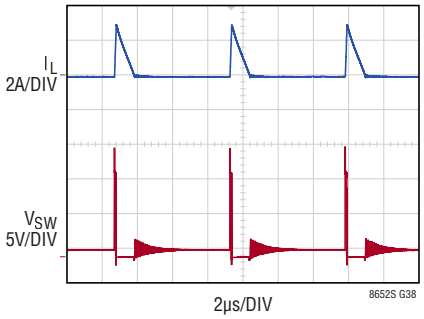
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

Forced Continuous Mode (FCM)



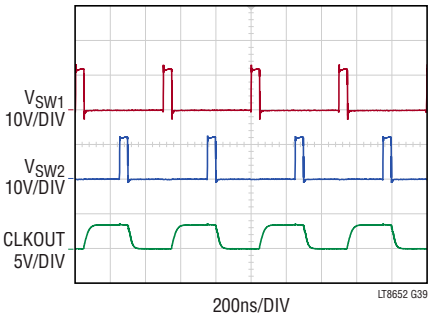
$12V_{IN}$ TO $1V_{OUT}$ AT 250mA
SYNC = FLOAT
f_{SW} = 1.5MHz

Burst Mode Operation



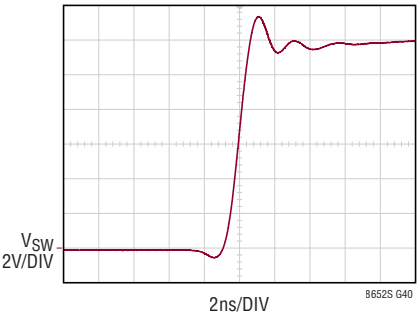
$12V_{IN}$ TO $1V_{OUT}$ AT 250mA
SYNC = 0V

CH1, CH2 and CLKOUT Two-Phase Operation



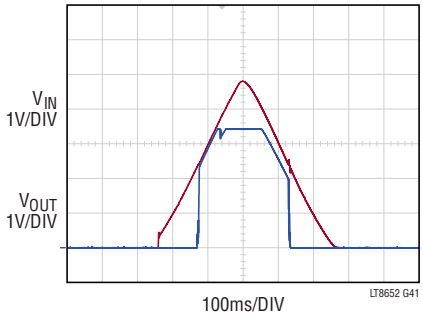
$12V_{IN}$ TO $1V_{OUT}$ AT 12A
SYNC = FLOAT
f_{SW} = 2MHz

Switch Rising Edge



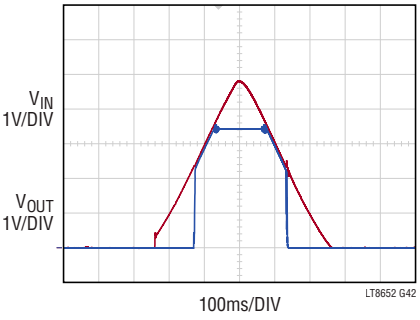
V_{IN} = 12V
I_{OUT} = 6A

Start-Up Dropout Performance Forced Continuous Mode



1Ω LOAD
(3.2A IN REGULATION)

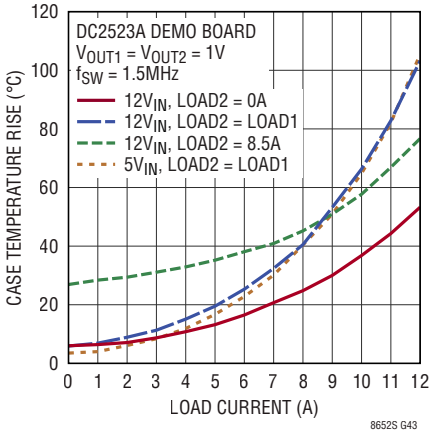
Start-Up Dropout Performance Burst Mode Operation



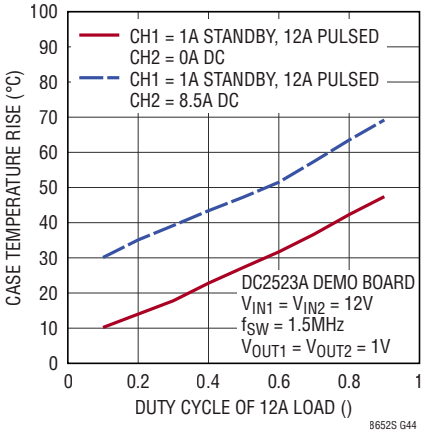
1Ω LOAD
(3.2A IN REGULATION)

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

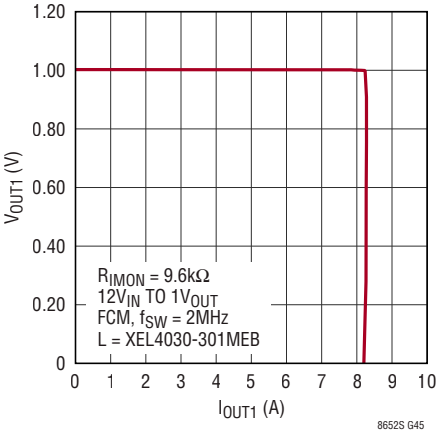
Case Temperature Rise Single Channel



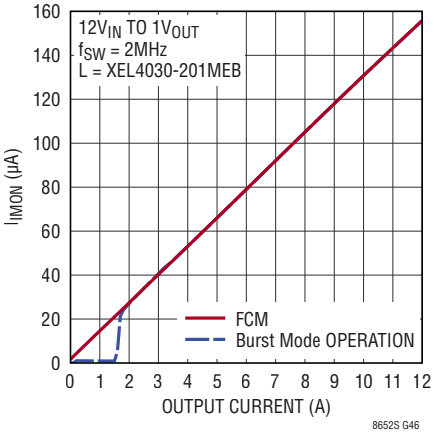
Case Temperature Rise Single Channel



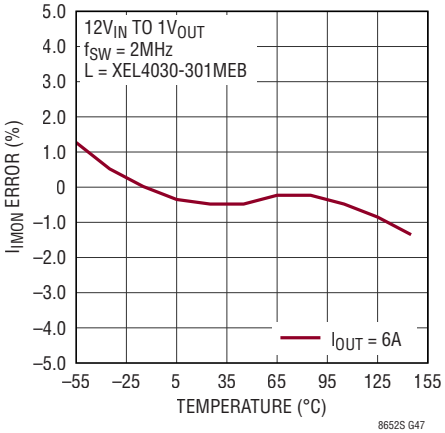
I_{IMON} Current Limit



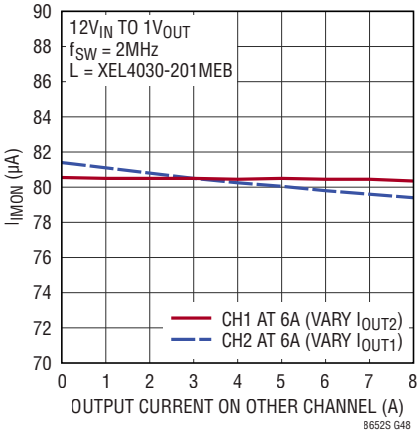
I_{IMON} vs I_O, FCM and Burst Mode Operation



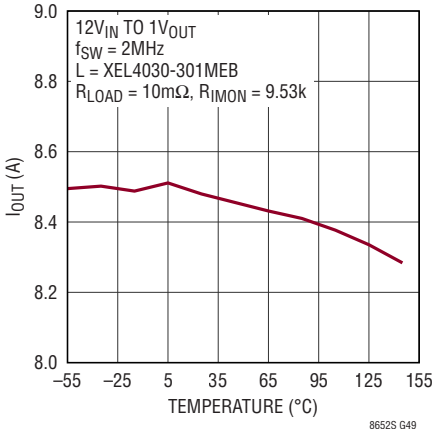
I_{IMON} Error



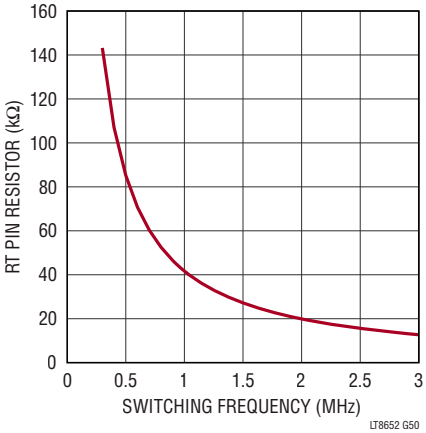
I_{IMON} vs Other Channel Load



I_{IMON} Current Limit

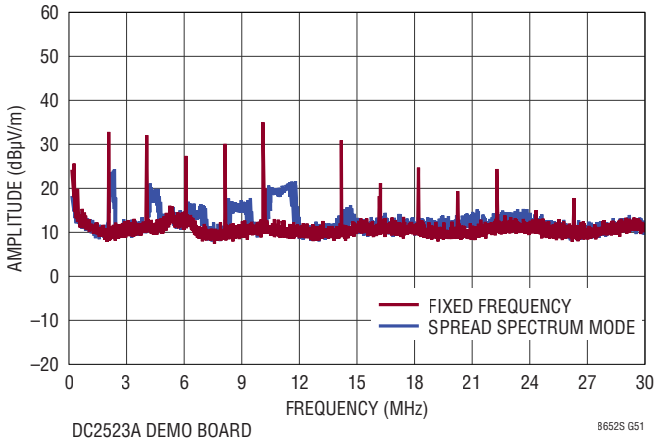


RT Programmed Switching Frequency



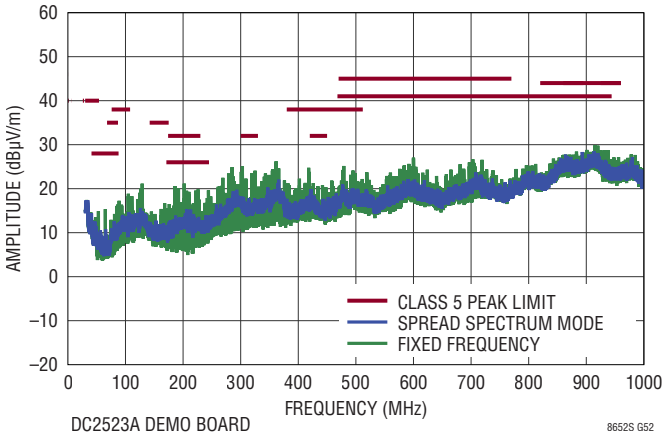
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

Conducted EMI Performance



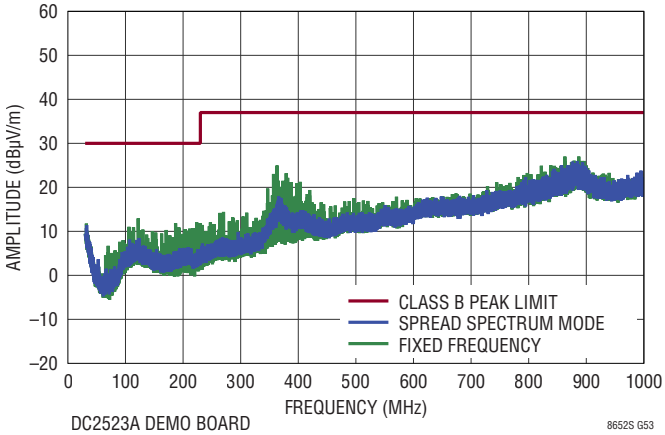
DC2523A DEMO BOARD
(WITH EMI FILTER INSTALLED)
14V INPUT TO 3.3V OUTPUT1 AT 8.5A AND 1.2V OUTPUT2 AT 8.5A, f_{SW} = 2MHz

Radiated EMI Performance (CISPR25 Radiated Emission Test with Class 5 Peak Limits)



DC2523A DEMO BOARD
(WITH EMI FILTER INSTALLED)
14V INPUT TO 3.3V OUTPUT1 AT 8.5A AND 1.2V OUTPUT2 AT 8.5A, f_{SW} = 2MHz

Radiated EMI Performance (CISPR22 Radiated Emission Test with Class B Peak Limits)



DC2523A DEMO BOARD
(WITH EMI FILTER INSTALLED)
14V INPUT TO 3.3V OUTPUT1 AT 8.5A AND 1.2V OUTPUT2 AT 8.5A, f_{SW} = 2MHz

PIN FUNCTIONS

IMON2 (Pin 1): Channel 2 Average Output Current Monitor Pin. A current proportional to the average output current flows out of this pin. An error amplifier compares the voltage on this pin to 1.0V (typical) and regulates the average current as required based on the external resistor value from this pin to GND. Selecting the external resistor value allows the user to control the maximum average output current such that:

$R_{IMON} = 78{,}000/I_{LIM}$

If IMON2 pin functionality is not desired, tie this pin to GND. See the Applications Information section for more details.

SS2 (Pin 2): Channel 2 Output Tracking and Soft-Start Pin. This pin allows user control of output voltage ramp rate during start-up. A SS2 voltage below 0.6V forces the LT8652S to regulate the FB2 pin to equal the SS2 pin voltage. When SS2 is above 0.6V, the internal reference resumes control of the error amplifier. An internal 2µA pull-up current from V_{CC} on this pin allows a capacitor to program output voltage slew rate. This pin is pulled to ground with a 200Ω MOSFET during shutdown and fault conditions; use a series resistor if driving from a low impedance output. This pin may be left floating if the soft-start feature is not being used.

RT (Pin 3): A resistor is tied between RT and ground to set the switching frequency.

V_{IN1} (Pins 5, 6, 7): The V_{IN1} pins supply current to the LT8652S internal circuitry and to the internal top side power switch of Channel 1. These pins must be locally bypassed. Be sure to place the positive terminal of the input capacitor as close as possible to the V_{IN1} pins and the negative capacitor terminal as close as possible to the GND pins. V_{IN1} must be greater than 3V for the LT8652S to operate.

NC (Pin 8): No Connect. This pin is not connected to internal circuitry. It is recommended that this be left floating or tied to GND.

V_{IN2} (Pin 9, 10, 11): The V_{IN2} pins supply current to the internal top side power switch of Channel 2. These pins must be locally bypassed. Be sure to place the positive terminal of the input capacitor as close as possible to the V_{IN2} pins and the negative capacitor terminal as close as possible to the GND pins. This input is capable of operating from a different supply than V_{IN1}. V_{IN1} must be present to run channel 2.

EN/UV (Pin 13): The LT8652S is shutdown when this pin is low and active when this pin is high. The hysteretic threshold voltage is 0.82V going up and 0.80V going down. Tie to V_{IN1} if shutdown feature is not used. An external resistor divider from V_{IN1} can be used to program a V_{IN} threshold below which Channel 1 and Channel 2 of the LT8652S will shut down. Do not float this pin. For individual channel shutdown, pull that channel's soft start pin to GND.

TEMP (Pin 14): Temperature Output Pin. This pin outputs a voltage proportional to junction temperature. The pin is 250mV for 25°C and has a slope of 11mV/°C. The output of this pin is not valid during light output loads on both channels while in Burst Mode operation. Put the LT8652S in forced continuous mode for the TEMP output to be valid across the entire output load range. See the Applications Information section for more information.

PG2 (Pin 15): The PG2 pin is the open-drain output of an internal comparator. PG2 remains low until the FB2 pin is within ±7% of the final regulation voltage and there are no fault conditions. PG2 is pulled low during V_{IN1} UVLO, V_{CC} UVLO, Thermal Shutdown or when the EN/UV pin is low.

PG1 (Pin 16): The PG1 pin is the open-drain output of an internal comparator. PG1 remains low until the FB1 pin is within ±7% of the final regulation voltage and there are no fault conditions. PG1 is pulled low during V_{IN1} UVLO, V_{CC} UVLO, Thermal Shutdown or when the EN/UV pin is low.

PIN FUNCTIONS

SYNC (Pin 17): External Clock Synchronization Input. Ground this pin for low ripple Burst Mode operation at low output loads. Apply a DC voltage of 2.8V or higher or tie to V_{CC} for forced continuous mode with spread spectrum modulation. Float the SYNC pin for forced continuous mode without spread spectrum modulation. When in forced continuous mode, the I_Q will increase to several mA. Apply a clock source to the SYNC pin for synchronization to an external frequency. The LT8652S will be in forced continuous mode when an external frequency is applied.

CLKOUT (Pin 18): In forced continuous mode, the CLKOUT pin provides a 50% duty cycle square wave 90 degrees out of phase with Channel 1. This allows synchronization with other regulators with up to four phases. When an external clock is applied to the SYNC pin, the CLKOUT pin will output a waveform with the same phase, duty cycle and frequency as the SYNC waveform. In Burst Mode operation, the CLKOUT pin will be grounded. Float this pin if the CLKOUT function is not used.

BST2 (Pin 19): This pin is used to provide a drive voltage, higher than the input voltage, to the top side power switch of Channel 2.

SW2 (Pins 20, 21, 22): The SW2 pins are the output of the Channel 2 internal power switches. Tie these pins together and connect them to the inductor. This node should be kept small on the PCB for good performance.

SW1 (Pins 23, 24, 25): The SW1 pins are the output of the Channel 1 internal power switches. Tie these pins together and connect them to the inductor. This node should be kept small on the PCB for good performance.

BST1 (Pin 26): This pin is used to provide a drive voltage, higher than the input voltage, to the top side power switch of Channel 1.

BIAS (Pin 27): The internal regulator will draw current from BIAS instead of V_{IN1} when BIAS is tied to a voltage higher than 3.1V. For output voltages of 3.3V and above, this pin should be tied to V_{OUT}. If this pin is tied to a supply other than V_{OUT}, use a 1µF local bypass capacitor on this pin. This pin should be grounded if the BIAS feature is not being used.

V_{CC} (Pin 28): Internal Regulator Bypass Pin. The internal power drivers and control circuits are powered from this voltage. V_{CC} current will be supplied from BIAS if $V_{BIAS} > 3.1V$, otherwise current will be drawn from V_{IN1}. Voltage on V_{CC} will vary between 2.8V and 3.3V when V_{BIAS} is between 3.0V and 3.5V. Decouple this pin to ground with at least a 1µF low ESR ceramic capacitor. Do not load the V_{CC} pin with external circuitry.

SS1 (Pin 29): Channel 1 Output Tracking and Soft-Start Pin. This pin allows user control of output voltage ramp rate during start-up. A SS1 voltage below 0.6V forces the LT8652S to regulate the FB1 pin to equal the SS1 pin voltage. When SS1 is above 0.6V, the tracking function is disabled and the internal reference resumes control of the error amplifier. An internal 2µA pull-up current from V_{CC} on this pin allows a capacitor to program output voltage slew rate. This pin is pulled to ground with a 200Ω MOSFET during shutdown and fault conditions; use a series resistor if driving from a low impedance output. This pin may be left floating if the soft-start feature is not being used.

IMON1 (Pin 30): Channel 1 Average Output Current Monitor Pin. A current proportional to the average output current flows out of this pin. An error amplifier compares the voltage on this pin to 1.0V (typical) and regulates the average current as required based on the external resistor value from this pin to GND. Selecting the external resistor value allows the user to control the maximum average output current such that:

$$R_{IMON} = 78{,}000/I_{LIM}$$

If IMON1 pin functionality is not desired, tie this pin to GND. See the Applications Information section for more details.

PIN FUNCTIONS

VC1 (Pin 31): Channel 1 Error Amplifier Output and Switching Regulator Compensation Pin. Connect this pin to appropriate external components to compensate the regulator loop frequency response. Connect this pin to V_{CC} to use the default internal compensation. If internal compensation is used, the Burst Mode quiescent current is only 12.8µA for Channel 1. If external compensation is used, the Burst Mode quiescent current is increased to about 100µA for Channel 1.

FB1 (Pin 32): The LT8652S regulates the FB1 pin to 600mV referenced to SNSGND1. Connect the feedback resistor divider tap to this pin.

SNSGND1 (Pin 33): The LT8652S regulates the FB1 pin to 600mV referenced to SNSGND1. Connect the ground pin of the output capacitor to this pin with a Kelvin line. If SNSGND1 pin functionality is not desired, tie this pin to GND.

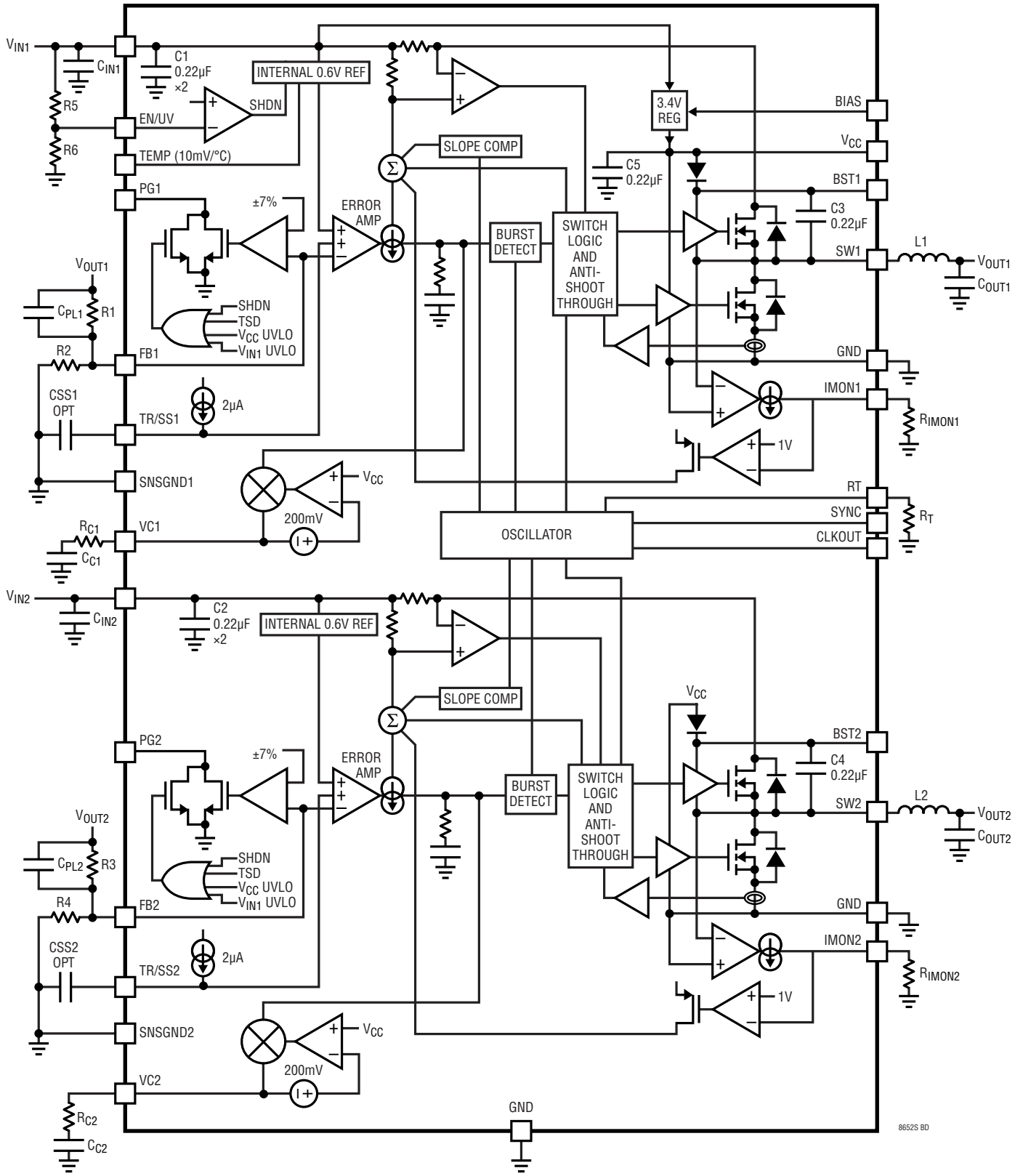
SNSGND2 (Pin 34): The LT8652S regulates the FB2 pin to 600mV referenced to SNSGND2. Connect the ground pin of the output capacitor to this pin with a Kelvin line. If SNSGND2 pin functionality is not desired, tie this pin to GND.

FB2 (Pin 35): The LT8652S regulates the FB2 pin to 600mV referenced to SNSGND2. Connect the feedback resistor divider tap to this pin.

VC2 (Pin 36): Channel 2 Error Amplifier Output and Switching Regulator Compensation Pin. Connect this pin to appropriate external components to compensate the regulator loop frequency response. Connect this pin to V_{CC} to use the default internal compensation. If internal compensation is used, the Burst Mode quiescent current is only 12.8µA for Channel 2. If external compensation is used, the Burst Mode quiescent current is increased to about 100µA for Channel 2.

GND (Pins 4, 12, Exposed Pad Pins 37 to 42): LT8652S System Ground. Connect these pins to the system ground and the board ground plane. Place the negative terminal of the input capacitors as close to the GND pins as possible. The exposed pad must be soldered to the PCB in order to lower the thermal resistance.

BLOCK DIAGRAM



OPERATION

Foreword

The LT8652S is a dual monolithic step-down regulator. The two channels are the same in terms of current capability and power switch size. The following sections describe the operation of Channel 1 and common circuits. They will highlight Channel 2 differences and interactions only when relevant. To simplify the application, both V_{IN1} and V_{IN2} are assumed to be connected to the same input supply. However, note that V_{IN1} must be greater than 3.0V for either channel to operate.

Operation

The LT8652S is a dual monolithic, constant frequency, peak current mode step-down DC/DC converter. An oscillator, with frequency set using a resistor on the RT pin, turns on the internal top power switch at the beginning of each clock cycle. Current in the inductor then increases until the top switch current comparator trips and turns off the top power switch. The peak inductor current at which the top switch turns off is controlled by the voltage on the VC node. The error amplifier servos the VC node by comparing the voltage on the V_{FB} pin with an internal 0.6V reference. When the load current increases it causes a reduction in the feedback voltage relative to the reference leading the error amplifier to raise the VC voltage until the average inductor current matches the new load current. When the top power switch turns off, the synchronous power switch turns on until the next clock cycle begins or inductor current falls to zero when not in forced continuous mode (FCM). If overload conditions result in more than the bottom NMOS current limit flowing through the bottom switch, the next clock cycle will be delayed until switch current returns to a safe level.

The “S” in LT8652S refers to the second generation Silent Switcher technology. This technology allows fast switching edges for high efficiency at high switching frequencies, while simultaneously achieving good EMI/EMC performance. This includes the integration of ceramic capacitors into the package for V_{IN1}, V_{IN2}, V_{CC}, BST1, and BST2 (C1–C5 in the Block Diagram). These capacitors keep all the fast AC current loops small which improves EMI performance.

The output voltage is resistively divided externally to create a feedback voltage for the regulator. In high current operation, a ground offset may be present between the LT8652S local ground and ground at the load. To overcome this offset, SNSGND should have a Kelvin connection to the load ground, and the lowest potential node of the resistor divider should be connected to SNSGND. The internal error amplifier senses the difference between this feedback voltage and a 0.6V SNSGND referenced voltage. This scheme overcomes any ground offsets between local ground and remote output ground, resulting in a more accurate output voltage. The LT8652S allows for remote output ground deviations as much as ±300mV with respect to local ground.

If the EN/UV pin is low, both channels are fully shut down and the LT8652S draws 6µA from the input supply. When the EN/UV pin is above 0.82V, both channels’ switching regulators will become active. 16µA is supplied by V_{IN1} to common bias circuits for both channels.

Each channel can independently enter Burst Mode operation to optimize efficiency at light load. Between bursts, all circuitry associated with controlling the output switch is shut down, reducing the channel’s contribution to input supply current. In a typical application, 17µA will be consumed from the input supply when regulating both channels with no load. Ground the SYNC pin for Burst Mode operation, float it for forced continuous mode (FCM) or apply a DC voltage higher than 2.8V to use FCM with spread spectrum modulation (SSM). If a clock is applied to the SYNC pin, both channels will synchronize to the external clock frequency and operate in FCM. While in FCM, the oscillator operates continuously and rising SW transitions are aligned to the clock. During light loads, the inductor current is allowed to go negative to maintain the programmed switching frequency. Minimum current limits for both power switches are enforced to prevent large negative inductor current from flowing back to the input. SSM dithers the switching frequency from the programmed value set by the RT pin up to 20% higher than the programmed value to spread out the switching energy in the frequency domain. The CLKOUT pin has no output

OPERATION

in Burst Mode operation, but outputs a square wave 90 degrees phase shifted from Channel 1 when in FCM. If a clock is applied to the SYNC pin, the CLKOUT pin has the same phase and duty cycle as the external clock.

To improve efficiency across all loads, supply current to internal circuitry can be sourced from the BIAS pin when biased at 3.3V or above. Otherwise, the internal circuitry will draw current exclusively from V_{IN1}. The BIAS pin should be connected to the lowest V_{OUT} programmed at 3.3V or above.

The VC pin allows the loop compensation of the switching regulator to be optimized based on the programmed switching frequency. Internal compensation can be selected by connecting the VC pin to V_{CC}, which simplifies the application circuit. External compensation improves the transient response at the expense of about 100µA more quiescent current per channel.

The LT8652S provides a scaled replica of the average Channel 1 and Channel 2 output current at the IMON1 and IMON2 pins respectively. The average current at each of these pins will be 1/78,000th of the measured average current plus a sampling offset. Further, the voltage at each pin is continuously fed to independent current limit amplifiers that have a voltage reference at 1V. Thus, a programmable average current limit for the output current may be obtained by placing a resistor of suitable value from IMON to GND so as to produce 1V at the desired current limit. When the current limit feature is used, a compensation capacitor should not be placed in parallel with the chosen resistor. The output monitor and limit circuits may be individually disabled by shorting IMON to GND.

Comparators monitoring the FB pin voltage will pull the corresponding PG pin low if the output voltage varies more than ±7% (typical) from the regulation voltage or if a fault condition is present.

The voltage present at the TEMP pin is proportional to the average die temperature of the LT8652S. The TEMP pin will be 250mV for a die temperature of 25°C and will have a slope of 11mV/°C.

Tracking soft-start is implemented by providing constant current via the SS/TR pin to an external soft-start capacitor to generate a voltage ramp. FB voltage is regulated to the voltage at the SS pin until it exceeds 0.6V; FB is then regulated to the reference 0.6V. When the SS pin is below 40mV, the corresponding switching regulator will stop switching. The SS capacitor is reset during shutdown, V_{IN1} undervoltage, or thermal shutdown.

Both channels are designed for output currents up to 12A, but thermal considerations practically limit the output currents to 8.5A of continuous current from each channel simultaneously. Channel 1 has a minimum V_{IN1} requirement of 3.0V, Channel 2 can operate with no minimum V_{IN2} provided the minimum V_{IN1} has been satisfied.

APPLICATIONS INFORMATION

Achieving Ultralow Quiescent Current

To enhance efficiency at light loads, the LT8652S operates in low ripple Burst Mode operation, which keeps the output capacitor charged to the desired output voltage while minimizing the input quiescent current and minimizing output voltage ripple. 16µA is supplied by V_{IN1} to common bias circuits. In Burst Mode operation, the LT8652S delivers single small pulses of current to the output capacitor followed by sleep periods where the output power is supplied by the output capacitor. While in sleep mode, both channels consume a combined 16µA.

As the output load decreases, the frequency of single current pulses decreases (see Figure 1) and the percentage of time the LT8652S is in sleep mode increases, resulting in much higher light load efficiency than for typical converters. By maximizing the time between pulses, the converter quiescent current approaches 16µA for a typical application when there is no output load. Therefore, to optimize the quiescent current performance at light loads, the current in the feedback resistor divider must be minimized as it appears to the output as load current.

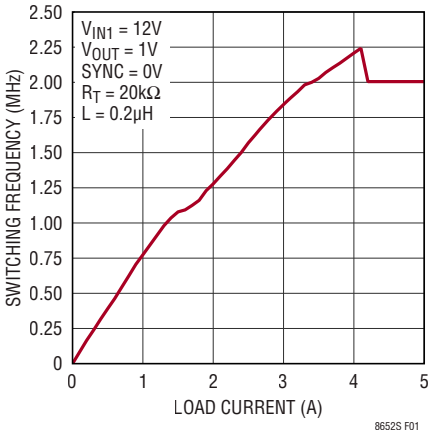


Figure 1. Burst Frequency

While in Burst Mode operation, the current limit of the top switch is approximately 3A resulting in output voltage ripple shown in Figure 2. Increasing the output capacitance will decrease the output ripple proportionally. As load ramps upward from zero, the switching frequency will increase, but only up to the switching frequency programmed by the resistor at the RT pin as shown in Figure 1. The output load at which the LT8652S reaches the programmed frequency varies based on input voltage, output voltage and inductor choice.

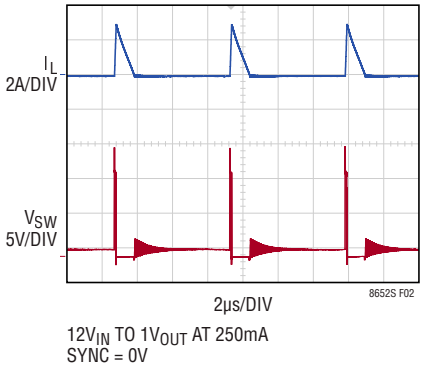


Figure 2. Burst Mode Operation

For some applications, it is desirable to select forced continuous mode (FCM) to maintain full switching frequency down to zero output load. See Forced Continuous Mode section.

FB Resistor Network and Differential Output Sensing

The output voltage is programmed with an external resistor divider from the output to its SNSGND (R1–2 for Channel 1, R3–4 for Channel 2). The resistive divider is tapped by the FB pin. Choose the resistor values according to:

$$R1 = R2\left(\frac{V_{OUT1}}{0.6V} - 1\right)$$

Reference designators refer to the Block Diagram. 1% resistors or better are recommended to maintain output voltage accuracy. More precisely, the V_{OUT} value programmed in the previous equation is with respect to SNSGND and thus is a differential quantity. For example, if V_{OUT} is programmed to 3V and V_{SNSGND} is –0.1V, then the output will be 2.9V with respect to ground at the LT8652S.

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Differential output sensing allows for more accurate output regulation in high power distributed systems having large line losses. Figure 3 illustrates the potential variations in the power and ground lines due to parasitic elements. These variations are exacerbated in multi-application systems with shared ground planes. Without differential output sensing, these variations directly reflect as an error in the regulated output voltage. The LT8652S's differential output sensing can correct for up to ±300mV of variation in the output's power and ground lines.

The LT8652S allows for seamless differential output sensing by sensing the resistively divided feedback voltage differentially. This allows for differential sensing in the full output range from 0.6V to 18V.

To avoid noise coupling into FB, the resistor divider should be placed near the FB and SNSGND pins and physically close to the LT8652S. The remote output and ground traces should be routed together as a differential pair to the remote output. These traces should be terminated as close as physically possible to the remote output point that is to be accurately regulated through remote differential sensing.

If low input quiescent current and good light-load efficiency are desired, use large resistor values for the FB resistor divider. The current flowing in the divider acts as a load current and will increase the no-load input current to the converter which is approximately:

$$I_Q = 16\mu A + \left(\frac{V_{OUT1}}{R1+R2}\right)\left(\frac{V_{OUT1}}{V_{IN1}}\right)\left(\frac{1}{\eta}\right)$$

where 16µA is the quiescent current of both channels and common circuitries, the second term is the current in the feedback divider reflected to the input of Channel 1 operating at its light load efficiency η. For a 1.2V application with R1 = 1M and R2 = 1M, the feedback divider draws 0.6µA. With V_{IN} = 12V and h = 80%, this adds 75nA to the 16µA quiescent current resulting in 16.075µA no-load current from the 12V supply. Note that this equation implies that the no-load current is a function of V_{IN}; this is plotted in the Typical Performance Characteristics section.

A similar calculation can be done to determine the input current contribution from the Channel 2 feedback resistors. For a 3.3V application with R3 = 1M, R4 = 221k, V_{IN} = 12V, and η = 80%, this adds 0.9µA to the input current resulting in a total of 17µA with both channels on.

For a typical FB resistor of 1MΩ, a 4.7pF to 10pF phase-lead capacitor should be connected from V_{OUT} to FB.

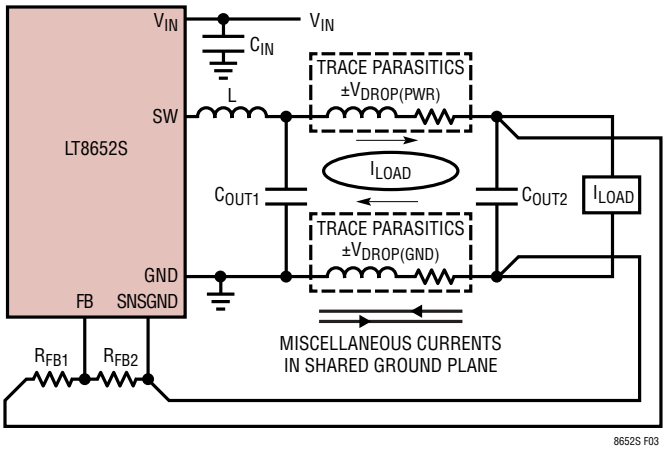

Figure 3. Differential Output Sensing Used to Correct Line Loss Variations in a High Power Distributed System with a Shared Ground Plane

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Setting the Switching Frequency

The LT8652S uses a constant frequency PWM architecture that can be programmed to switch from 300kHz to 3MHz by using a resistor tied from the RT pin to ground. Table 1 shows the necessary R_T value for a desired switching frequency.

The R_T resistor required for a desired switching frequency can be calculated using:

$$R_T = \frac{43.5}{f_{SW}} - 1.8$$

where R_T is in kΩ and f_{SW} is the desired switching frequency in MHz.

The two channels of the LT8652S operate 180° out of phase to avoid aligned switching edge noise and reduce input current ripple.

Table 1. SW Frequency vs. R_T Value

f_{SW} (MHz)	R_T (kΩ)
0.3	143
0.4	107
0.5	84.5
0.6	69.8
0.8	52.3
1.0	41.2
1.2	34.8
1.4	29.4
1.6	25.5
1.8	22.6
2.0	20.0
2.2	18.2
2.5	15.8
3.0	12.7

Operating Frequency Selection and Trade-Offs

Selection of the operating frequency is a trade-off between efficiency, component size, and input voltage range. The advantage of high frequency operation is that smaller inductor and capacitor values may be used. The disadvantages are lower efficiency and a smaller input voltage range.

The highest switching frequency ($f_{SW(MAX)}$) for a given application can be calculated as follows:

$$f_{SW(MAX)} = \frac{V_{OUT} + V_{SW(BOT)}}{t_{ON(MIN)}\left(V_{IN} - V_{SW(TOP)} + V_{SW(BOT)}\right)}$$

where V_{IN} is the typical input voltage, V_{OUT} is the output voltage, $V_{SW(TOP)}$ and $V_{SW(BOT)}$ are the internal switch drops (~0.3V, ~0.1V, respectively at maximum load) and $t_{ON(MIN)}$ is the minimum top switch on-time of 45nS (see the Electrical Characteristics). This equation shows that a slower switching frequency is necessary to accommodate a high V_{IN}/V_{OUT} ratio. Choose the switching frequency based on which channel has the lower frequency constraint.

For transient operation, V_{IN} may go as high as the absolute maximum rating of 18V regardless of the R_T value, however the LT8652S will reduce switching frequency on each channel independently as necessary to maintain control of inductor current to assure safe operation.

In Burst Mode operation, the LT8652S is capable of a maximum duty cycle of greater than 99%, and the V_{IN} to V_{OUT} dropout is limited by the $R_{DS(ON)}$ of the top switch. In this mode the channel that enters dropout skips switch cycles, resulting in a lower switching frequency. The LT8652S in forced continuous mode will not skip cycles to achieve a higher duty cycle. The part will maintain the programmed switching frequency and the dropout voltage will be larger due to the smaller maximum duty cycle.

For applications that cannot allow deviation from the programmed switching frequency at low V_{IN}/V_{OUT} ratios, use the following formula to set switching frequency:

$$V_{IN(MIN)} = \frac{V_{OUT} + V_{SW(BOT)}}{1 - f_{SW} \bullet t_{OFF(MIN)}} - V_{SW(BOT)} + V_{SW(TOP)}$$

where $V_{IN(MIN)}$ is the minimum input voltage without skipped cycles, V_{OUT} is the output voltage, $V_{SW(TOP)}$ and $V_{SW(BOT)}$ are the internal switch drops (~0.3V, ~0.1V, respectively at maximum load), f_{SW} is the switching frequency (set by RT), and $t_{OFF(MIN)}$ is the minimum switch off-time. Note that higher switching frequency will increase the minimum input voltage below which cycles will be dropped to achieve higher duty cycle.

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Note there is no minimum V_{IN2} voltage requirement as it does not supply the internal common bias circuits, making the Channel 2 uniquely capable of operating from very low input voltages as long as V_{IN1} has a supply of 3V or greater.

Inductor Selection and Maximum Output Current

The LT8652S is designed to minimize solution size by allowing the inductor to be chosen based on the output load requirements of the application. During overload or short-circuit conditions, the LT8652S safely tolerates operation with a saturated inductor through the use of a high speed peak-current mode architecture.

A good first choice for the inductor value is:

$$L_{1,2} = \frac{V_{OUT1,2} + V_{SW(BOT)}}{3 \bullet f_{SW}}$$

where f_{SW} is the switching frequency in MHz, V_{OUT} is the output voltage, $V_{SW(BOT)}$ is the bottom switch drop (~0.1V) and L is the inductor value in µH. To avoid overheating and poor efficiency, an inductor must be chosen with an RMS current rating that is greater than the maximum expected output load of the application. In addition, the saturation current (typically labeled I_{SAT}) rating of the inductor must be higher than the load current plus 1/2 of in inductor ripple current:

$$I_{L(PEAK)} = I_{LOAD(MAX)} + \frac{1}{2}\Delta I_L$$

where ΔI_L is the inductor ripple current as calculated in Equation 1 and $I_{LOAD(MAX)}$ is the maximum output load for a given application.

As a quick example, an application requiring 7A output should use an inductor with an RMS rating of greater than 7A and an I_{SAT} of greater than 9.1A. During long duration overload or short-circuit conditions, the inductor RMS rating requirement must be greater to avoid overheating of the inductor. To keep the efficiency high, the series resistance (DCR) should be less than 3mΩ and the core material should be intended for high frequency applications.

The LT8652S limits the peak switch current in order to protect the switches and the system from overload faults. The top switch current limit (I_{LIM}) is at least 29A at low duty cycles and decreases linearly to 19A at DC = 0.8. The inductor value must then be sufficient to supply the desired maximum output current ($I_{OUT(MAX)}$), which is a function of the switch current limit (I_{LIM}) and the ripple current.

$$I_{OUT(MAX)} = I_{LIM} - \frac{\Delta I_L}{2}$$

The peak-to-peak ripple current in the inductor can be calculated as follows:

$$\Delta I_L = \frac{V_{OUT}}{L \bullet f_{SW}} \bullet \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right) \quad (1)$$

where f_{SW} is the switching frequency of the LT8652S and L is the value of the inductor. Therefore, the maximum output current that the LT8652S will deliver depends on the switch current limit, the inductor value, and the input and output voltages.

Each channel has a secondary bottom switch current limit. After the top switch has turned off, the bottom switch carries the inductor current. If for any reason the inductor current is too high, the bottom switch will remain on, delaying the top switch turning on until the inductor current returns to a safe level. This level is specified as the bottom NMOS current limit and is independent of duty cycle. Maximum output current in the application circuit is limited to this valley current plus one half of the inductor ripple current.

In most cases, current limit is enforced by the top switch. The bottom switch limit controls the inductor current when the minimum on-time condition is violated (high input voltage, high frequency or saturated inductor).

The bottom switch current limit is designed to be equal to the peak current limit to avoid any contribution to maximum rated current of the LT8652S.

For more information about maximum output current and discontinuous operation, see Analog Devices Application Note 44.

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Finally, for duty cycles greater than 50% ($V_{OUT}/V_{IN} > 0.5$), a minimum inductance is required to avoid sub-harmonic oscillation. See Analog Devices Application Note 19.

Table 2. Inductor Manufacturers

VENDOR	URL
Coilcraft	www.coilcraft.com
Sumida	www.sumida.com
Würth Elektronik	www.we-online.com
Vishay	www.vishay.com

Output Current Monitor and Limit

The LT8652 senses the average current through the bottom switch during the off state and outputs a scaled replica of this current (which corresponds to the regulator's load current) to the IMON pin. The average current at the monitor pin is 1/78000th the measured average output current plus a sampling offset inversely proportional to the switch off-time:

$$I_{IMON} = \frac{I_{OUT}}{0.078} + \frac{1}{t_{OFF}}$$

$$t_{OFF} = \frac{\left(1 - \frac{V_{OUT}}{V_{IN}}\right)}{f_{SW}}$$

where f_{SW} is the programmed switching frequency measured in MHz, t_{OFF} is the switch off-time measured in microseconds, I_{OUT} is the output current in amps, and I_{IMON} is in microamps.

The output current may be measured directly or converted to a voltage with an external resistor. The voltages at the IMON pins are continuously fed to independent current limit amplifiers that have a voltage reference of 1V (typical). A programmable average current limit for either channels' average output current may be obtained by placing a resistor, R_{IMON}, from the monitor pin to GND according to the following equation:

$$R_{IMON} = \frac{78{,}000}{I_{LIM}}$$

where I_{LIM} is the programmed current limit in amps and R_{IMON} is in ohms. It is recommended to set the programmed average current limit to allow for at least 10% margin.

When active, the current limit amplifiers form a feedback loop that controls the maximum average current produced by the LT8652S. In current limit the output voltage drops, resulting in frequency stretching to maintain a decreased duty-cycle. This results in the sampling offset term becoming negligible in current limit. When using the current limit feature, a capacitor should not be placed between GND and the monitor pin, otherwise loop stability could be adversely effected. However, if high frequency noise reduction is desired a capacitor may be placed in parallel with R_{IMON} if:

$$R_{IMON} \bullet C_{FILTER} < 3.2\mu s$$

This will ensure the pole created by the filter capacitor and R_{IMON} will not affect the current limit feedback loop. Do not use a R_{IMON} greater than 80kΩ.

When operating in BURST mode (SYNC low), if the load is low enough that the switching frequency starts to decrease, then IMON will cease to monitor output current and will instead pull the IMON voltage to ground.

As previously described, the LT8652S senses the average output current through the bottom FET during the off time. As a result, it is recommended the LT8652S be operated with an off time of greater than 150ns for best current monitor accuracy. For many applications, this is of little concern unless operating at or near regulator dropout conditions (extremely high duty cycle operation).

Input Capacitor

Bypass the input of the LT8652S circuit with a ceramic capacitor of X7R or X5R type placed as close as possible to the V_{IN} and GND pins. Y5V types have poor performance over temperature and applied voltage, and should not be used. A 10µF or higher value ceramic capacitor is adequate to bypass the LT8652S and will easily handle the ripple current. Note that larger input capacitance is required when a lower switching frequency is used. If the input power source has high impedance, or there is

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significant inductance due to long wires or cables, additional bulk capacitance may be necessary. This can be provided with a low performance electrolytic capacitor.

Output Capacitor and Output Ripple

The output capacitor has two essential functions. Along with the inductor, it filters the square wave generated by the LT8652S to produce the DC output. In this role, it determines the output ripple, thus low impedance at the switching frequency is important. The second function is to store energy in order to satisfy transient loads and stabilize the LT8652S's control loop. Ceramic capacitors have very low equivalent series resistance (ESR) and provide the best ripple performance. For good starting values, see the Typical Applications section.

Use X5R or X7R types. This choice will provide low output ripple and good transient response. Transient performance can be improved with a higher value output capacitor and the addition of a feed forward capacitor placed between V_{OUT} and FB. Increasing the output capacitance will also decrease the output voltage ripple. A lower value of output capacitor can be used to save space and cost but transient performance will suffer and may cause loop instability. See the Typical Applications in this data sheet for suggested capacitor values.

When choosing a capacitor, special attention should be given to the data sheet to calculate the effective capacitance under the relevant operating conditions of voltage bias and temperature. A physically larger capacitor or one with a higher voltage rating may be required.

Ceramic Capacitors

Ceramic capacitors are small, robust and have very low ESR. However, ceramic capacitors can cause problems when used with the LT8652S due to their piezoelectric nature. When in Burst Mode operation, the LT8652S's switching frequency depends on the load current, and at very light loads the LT8652S can excite the ceramic capacitor at audio frequencies, generating audible noise. Since the LT8652S operates at a lower current limit during Burst Mode operation, the noise is typically very quiet to a casual ear. If this is unacceptable, use a high performance tantalum or electrolytic capacitor at the output. Low noise ceramic capacitors are also available.

Table 3. Ceramic Capacitor Manufacturers

MANUFACTURER	WEB
Taiyo Yuden	www.t-yuden.com
AVX	www.avxcorp.com
Murata	www.murata.com
TDK	www.tdk.com

Enable Pin

The LT8652S is in shutdown when the EN/UV pin is low and active when the pin is high. The rising threshold of the EN/UV comparator is 0.83V, with 30mV of hysteresis. The EN/UV pins can be tied to V_{IN} if the shutdown feature is not used, or tied to a logic level if shutdown control is required.

Adding a resistor divider from V_{IN} to EN/UV programs the LT8652S to operate only when V_{IN} is above a desired voltage (see the Block Diagram). Typically, this threshold, $V_{IN(EN)}$, is used in situations where the input supply is current limited or has a relatively high source resistance. A switching regulator draws constant power from the source, so source current increases as source voltage drops. This looks like a negative resistance load to the source and can cause the source to current limit or latch low under low source voltage conditions. The $V_{IN(EN)}$ threshold prevents the regulator from operating at source voltages where the problems might occur. This threshold can be adjusted by setting the values R5 and R6 such that they satisfy the following equation:

$$V_{IN(EN)} = \left(\frac{R5}{R6} + 1\right) \bullet 0.8V$$

where the corresponding channel will remain off until V_{IN} is above $V_{IN(EN)}$. Due to the comparator's hysteresis, switching will not stop until the input falls slightly below $V_{IN(EN)}$.

When operating in Burst Mode operation for light load currents, the current through the $V_{IN(EN)}$ resistor network can easily be greater than the supply current consumed by the LT8652S. Therefore, the $V_{IN(EN)}$ resistors should be large to minimize their effect on efficiency at low loads.

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V_{CC} Regulator

An internal low dropout (LDO) regulator produces the 3.4V supply from V_{IN1} that powers the drivers and the internal bias circuitry. For this reason, V_{IN1} must be present and valid to use either channel. The V_{CC} can supply enough current for the LT8652S's circuitry and must be bypassed to ground with a 1µF ceramic capacitor. Good bypassing is necessary to supply the high transient currents required by the power MOSFET gate drivers. To improve efficiency the internal LDO can also draw current from the BIAS pin when the BIAS pin is at 3.1V or higher. Typically the BIAS pin can be tied to the lowest output or external supply above 3.1V. If BIAS is connected to a supply other than V_{OUT}, be sure to bypass with a local ceramic capacitor. If the BIAS pin is below 3.0V, the internal LDO will consume current from V_{IN1}.

Applications with high input voltage and high switching frequency where the internal LDO pulls current from V_{IN1} will increase die temperature because of the higher power dissipation across the LDO. Do not connect an external load to the V_{CC} pin.

Frequency Compensation

The LT8652S has VC pins which can be used to optimize the loop compensation of each channel. If the VC pins are shorted to V_{CC}, then internal compensation is used. This simplifies the circuit design and minimizes the quiescent current, but since the internal compensation has to be stable across the 300kHz to 3MHz range of switching frequencies, the internal compensation will not be optimal, especially at high switching frequencies. If the best transient response is desired, an external compensation network can be connected to the VC pin, which usually consists of a series resistor and capacitor (see R_C and C_C in the Block Diagram).

Designing the compensation network is a bit complicated and the best values depend on the application and in particular the type of output capacitor. A practical approach is to start with one of the circuits in the data sheet that is similar to your application and tune the compensation network to optimize the performance. LTspice® simulations can help in this process. Stability should then be checked across all operating conditions, including load current, input voltage and temperature.

The LT1375 data sheet contains a more thorough discussion of loop compensation and describes how to test the stability using a transient load.

Figure 4 shows an equivalent circuit for the LT8652S control loop. The error amplifier is a transconductance amplifier with finite output impedance. The power section, consisting of the modulator, power switches, and inductor, is modeled as a transconductance amplifier generating an output current proportional to the voltage at the VC pin. Note that the output capacitor integrates this current and that the capacitor on the VC pin (C_C) integrates the error amplifier output current, resulting in two poles in the loop. A zero is required and comes from a resistor R_C in series with C_C. This simple model works well as long as the value of the inductor is not too high and the loop crossover frequency is much lower than the switching frequency. A phase lead capacitor (C_{PL}) across the feedback divider can be used to improve the transient response and is required to cancel the parasitic pole caused by the feedback node to ground capacitance.

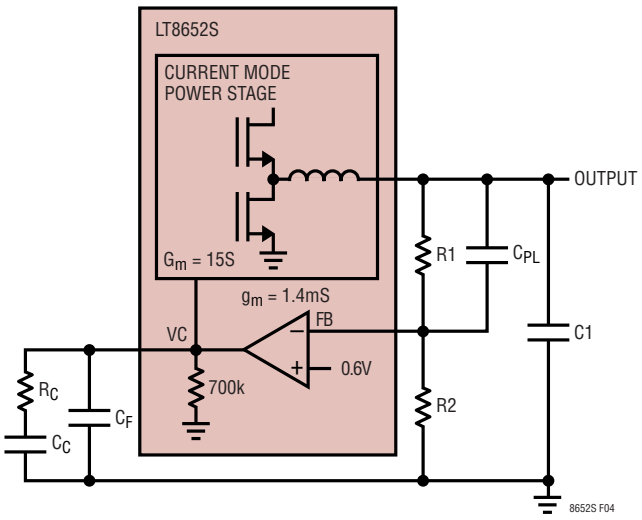

Figure 4. Model for Loop Response

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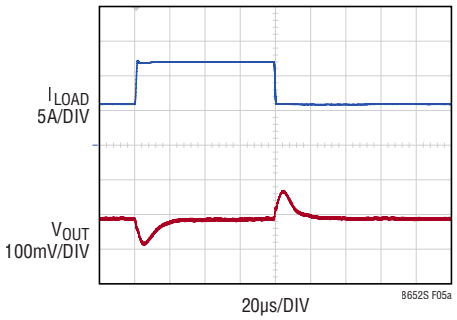
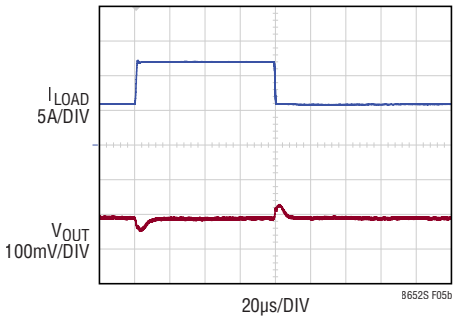
Figure 5a shows the transient response for the front page application which uses internal compensation. Figure 5b shows the improved transient response of the same application when a 17.1k R_C and 220pF C_C compensation network is used. Use of an external compensation network increases the quiescent current by about 50µA per channel.



6A TO 12A TRANSIENT
$12V_{IN}$ TO $1V_{OUT}$
C_{OUT} = 340µF
FCM, f_{SW} = 2MHz

a)



6A TO 12A TRANSIENT
$12V_{IN}$ TO $1V_{OUT}$
C_{OUT} = 340µF
FCM, f_{SW} = 2MHz
C_C = 220pF, R_C = 17.1kΩ

b)

Figure 5. Transient Response

Output Voltage Tracking and Soft-Start

The LT8652S allows the user to program its output voltage ramp rate with the SS pin. An internal 2µA current pulls up the SS pin to V_{CC}. Putting an external capacitor on SS, enables soft-starting the output to prevent current surge on the input supply. During the soft-start ramp, the output voltage will proportionally track the SS pin voltage. For output tracking applications, SS can be externally driven by another voltage source. From 0V to 0.04V, the SS pin will stop the corresponding channel from switching, thus allowing the SS pin to be used as a shutdown pin. From 0.04V to 0.6V, the SS voltage will override the internal 0.6V reference input to the error amplifier, thus regulating the FB pin voltage to that of SS pin (Figure 6). When SS is sufficiently above 0.6V, tracking is disabled and the feedback voltage will regulate to the internal reference voltage. The SS pin may be left floating if the function is not needed. Note that in both Burst Mode operation and forced continuous mode (FCM), the LT8652S will not discharge the output to regulate to a lower SS voltage.

An active pull-down circuit is connected to the SS pin which will discharge the external soft-start capacitor in the case of fault conditions and restart the ramp when the faults are cleared. Fault conditions that clear the soft-start capacitor are the EN/UV pin below 0.8V, V_{IN1} voltage falling too low, or thermal shutdown.

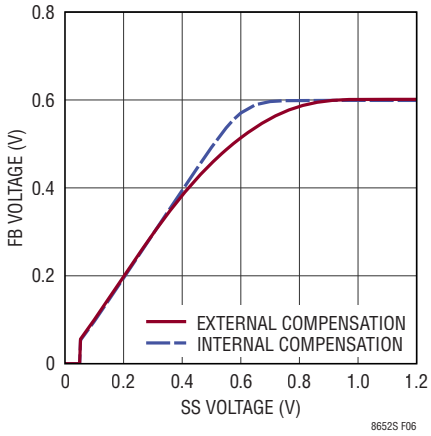


Figure 6. Soft Start Pin Tracking

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Output Power Good

When the LT8652S's output voltage is within the ±7% window of the regulation point, which is a FB voltage in the range of 0.56V to 0.64V (typical), the output voltage is considered good and the open-drain PG pin goes high impedance and is typically pulled high with an external resistor. Otherwise, the internal pull-down device will pull the PG pin low. To prevent glitching both the upper and lower thresholds, include 0.25% of hysteresis.

The PG pin is also actively pulled low during several fault conditions: corresponding EN/UV pin below 0.8V, V_{CC} voltage falling too low, V_{IN1} under voltage or thermal shutdown.

Sequencing

Start-up sequencing and tracking can be configured in several ways with the LT8652S. One channel can be required to be valid before enabling the other channel to sequence their start-up order. This can be done by connecting the PG pin of the first channel to the SS pin of the second channel.

The channels can also be started at the same time where the output voltages can track in a ratiometric fashion (see Figure 7).

Paralleling

To increase the possible output current, the two channels can be connected in parallel to the same output. To do this, the VC, SS, and FB pins of each channel are connected together, while each channel's SW node is connected to the common output through its own inductor. Figure 8 shows an application where the two channels of one LT8652S regulator are combined to get one output capable of 17A DC with 24A peak transients.

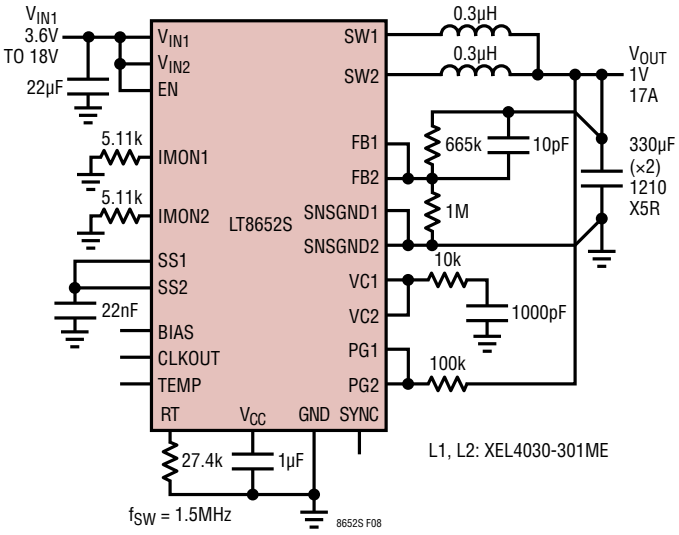

Figure 8. Two-Phase Application

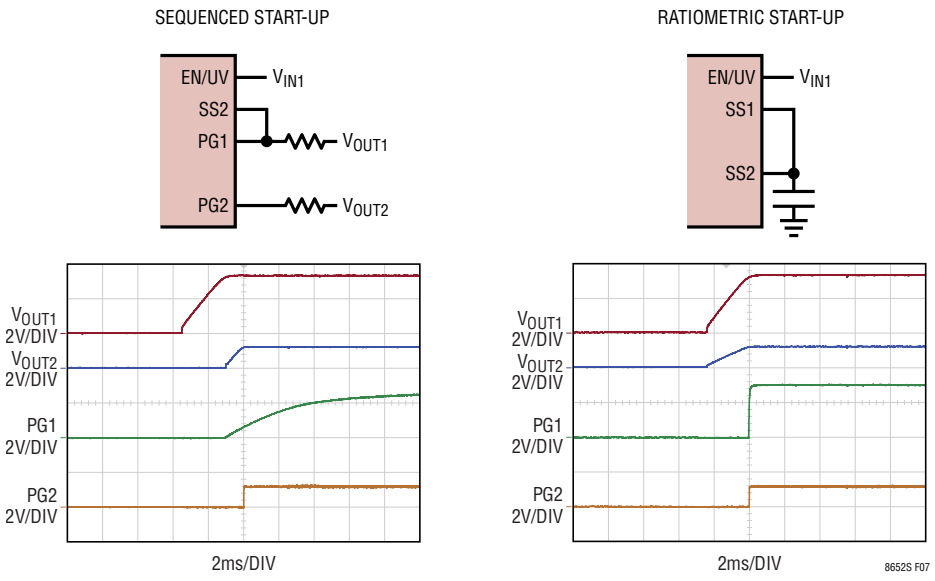

Figure 7. Sequencing and Start-up Configurations

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Synchronization

To select low ripple Burst Mode operation, tie the SYNC pin below 0.4V (this can be ground or a logic low output). To select forced continuous mode (FCM), float the SYNC pin. To select FCM with Spread Spectrum Modulation (SSM), tie the SYNC pin above 2.8V (SYNC can be tied to V_{CC}). To synchronize the LT8652S oscillator to an external frequency connect a square wave (with 20% to 80% duty cycle) to the SYNC pin. The square wave amplitude should have valleys that are below 0.4V and peaks above 1.5V (up to 6V). When synchronized to an external clock the LT8652S will use FCM.

Channel 1 will synchronize its positive switch edge transitions to the positive edge of the SYNC signal and Channel 2 will synchronize to the negative edge of the SYNC signal.

The LT8652S may be synchronized over a 300kHz to 3MHz range. The R_T resistor should be chosen to set the LT8652S switching frequency equal to or below the lowest synchronization input. For example, if the synchronization signal will be 500kHz and higher, the R_T should be selected for nominal 500kHz.

The slope compensation is set by the R_T value, while the minimum slope compensation required to avoid subharmonic oscillations is established by the inductor size, input voltage, and output voltage. Since the synchronization frequency will not change the slopes of the inductor current waveform, if the inductor is large enough to avoid subharmonic oscillations at the frequency set by R_T, then the slope compensation will be sufficient for all synchronization frequencies.

A synchronizing signal that incorporates spread spectrum may reduce EMI. The duty cycle of the SYNC signal can be used to set the relative phasing of the two channels for minimizing input ripple.

Forced Continuous Mode

Forced continuous mode (FCM) is activated by either floating the SYNC pin, applying a DC voltage above 2.8V to the SYNC pin, or applying an external clock to the SYNC pin.

While in FCM, discontinuous mode operation is disabled and the inductor current is allowed to go negative so that the regulator can switch at the programmed frequency all the way down to zero output current. This has the advantage of maintaining the programmed switching frequency across the entire load range so that the switch harmonics and EMI are consistent and predictable. The disadvantage of FCM is that the light load efficiency will be low compared to Burst Mode operation.

At low input voltages when the part enters dropout, the programmed switching frequency will be maintained and off time skipping will not be allowed. This keeps the switching frequency controlled, but the dropout voltage will be higher than in Burst Mode operation due to maximum duty cycle constraints.

The negative inductor current is limited to a maximum of about –4A, so the LT8652S can only sink a maximum of about –2A. This prevents boosting an excessive amount of current back from the output to the input. Additional safety features include disabling FCM when the SS pin voltage is below 1.8V during start-up to prevent discharging the output when starting up into a pre-biased output, and a bottom FET current limit to prevent over charging the output if the minimum on time is violated.

Spread Spectrum Modulation

Spread spectrum modulation (SSM) is activated by applying a DC voltage above 2.8V to the SYNC pin. SSM reduces the EMI/EMC emissions by modulating the switching frequency between the value programmed by R_T to approximately 20% higher than that value. The switching frequency is modulated linearly up and then linearly down at a 7kHz rate. This is an analog function, so each switching period will be different than the previous one. For example, when the LT8652S is programmed to 2MHz and the SSM feature is enabled, the switching frequency will vary from 2MHz to 2.4MHz at a 7kHz rate. When in SSM, the part will also operate in forced continuous mode.

APPLICATIONS INFORMATION

Clock Output

The CLKOUT pin outputs a clock which can be used to synchronous other regulators to the LT8652S. In Burst Mode operation (SYNC pin low), the CLKOUT pin is grounded. In forced continuous mode (SYNC pin float or DC high), the CLKOUT pin outputs a 50% duty cycle clock where the CLKOUT rising edge is 90 degrees phase shifted relative to Channel 1. If this CLKOUT waveform is applied to the SYNC pin of another LT8652S regulator, then four-phase operation can be achieved. If an external clock is applied to the SYNC pin of the LT8652S, then the CLKOUT pin will output a waveform with the same phasing and duty cycle as the SYNC pin clock. The low and high levels of the CLKOUT pin are ground and V_{CC}, respectively. The edge rates will be slower if the CLKOUT trace has extra capacitance.

Temperature Monitor Function

The TEMP pin will output a voltage proportional to die temperature. The TEMP pin typically outputs 250mV for 25°C and has a slope of 11mV/°C. Without the aid of an external circuitry, the TEMP pin output is valid from 20°C to 150°C (200mV to 1.6V). Do not load the TEMP pin with more than 100µA. To extend the TEMP pin output below 20°C, connect a resistor from the TEMP pin to a negative voltage. The TEMP pin output is valid down to –35°C.

As a safeguard, the LT8652S has an additional thermal shutdown set at a typical value of 165°C. If the thermal shutdown is exceeded, both channels of the LT8652S will be shutdown until the thermal overload event expires.

It should be noted that the TEMP pin voltage represents the steady-state, average die temperature and should not be used to guarantee that maximum junction temperatures are not exceeded. Instantaneous power along with thermal gradients and time constants may cause portions of the die to exceed maximum ratings. Be sure to calculate die temperature rise for steady state (>1 Min) as well as impulse conditions.

Shorted and Reversed Input Protection

The LT8652S will tolerate a shorted output. The bottom switch current is monitored such that if inductor current is beyond safe levels, switching of the top switch will be delayed until such time as the inductor current falls to safe levels. Fault condition of one channel will not affect the operation of the other channel.

There is another situation to consider in systems where the output will be held high when the input to the LT8652S is absent. This may occur in battery charging applications or in battery-backup systems where a battery or some other supply is ORed with Channel 1's output. If the V_{IN1} pin is allowed to float and the EN/UV pin is held high (either by a logic signal or because it is tied to V_{IN1}), then the LT8652S's internal circuitry will pull its quiescent current through its SW1 pin. This is acceptable if the system can tolerate current draw in this state. If the EN/UV pin is grounded, the SW1 pin current will drop to near 6µA. However, if the V_{IN1} pin is grounded while Channel 1 output is held high, regardless of EN/UV1, parasitic body diodes inside the LT8652S can pull current from the output through the SW1 pin and the V_{IN1} pin, damaging the IC.

V_{IN2} is not connected to the shared internal supply and will not draw any current if left floating. If both V_{IN1} and V_{IN2} are floating, regardless of EN/UV pin states, no load will be present at the output of Channel 2. However, if the V_{IN2} pin is grounded while Channel 2 output is held high, parasitic body diodes inside the LT8652S can pull current from the output through the SW2 pin and the V_{IN2} pin, damaging the IC.

Figure 9 shows a connection of the V_{IN} pins and EN/UV pin that will allow the LT8652S to run only when the input voltage is present and that protects against a shorted or reversed input.

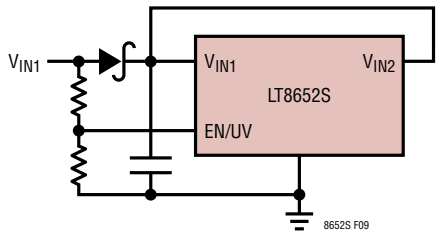


Figure 9. Reverse V_{IN} Protection

APPLICATIONS INFORMATION

PCB Layout

For proper operation and minimum EMI, care must be taken during printed circuit board layout. Figure 10 shows the recommended component placement with trace, ground plane and via locations. Note that large, switched currents flow in the LT8652S's V_{IN} pins, GND pins, and the input capacitors. The loop formed by the input capacitor should be as small as possible by placing the capacitor adjacent to the V_{IN} and GND pins. When using a physically large input capacitor, the resulting loop may become too large in which case using a small case/value capacitor placed close to the V_{IN} and GND pins plus a larger capacitor further away is preferred. These components, along with the inductor and output capacitor, should be placed on the same side of the circuit board and their connections should be made on that layer. Place a local, unbroken ground plane under the application circuit on the layer closest to the surface layer. The SW and BOOST nodes should be as small as possible. Finally, keep the FB and RT nodes small so that the ground traces will shield them from the SW and BOOST nodes. The exposed pad acts as a heat sink and is connected electrically to ground. To keep thermal resistance low, extend the ground plane as much as possible and add thermal vias under and near the LT8652S to additional ground planes within the circuit board and on the bottom side. See Figure 10 for example PCB layout.

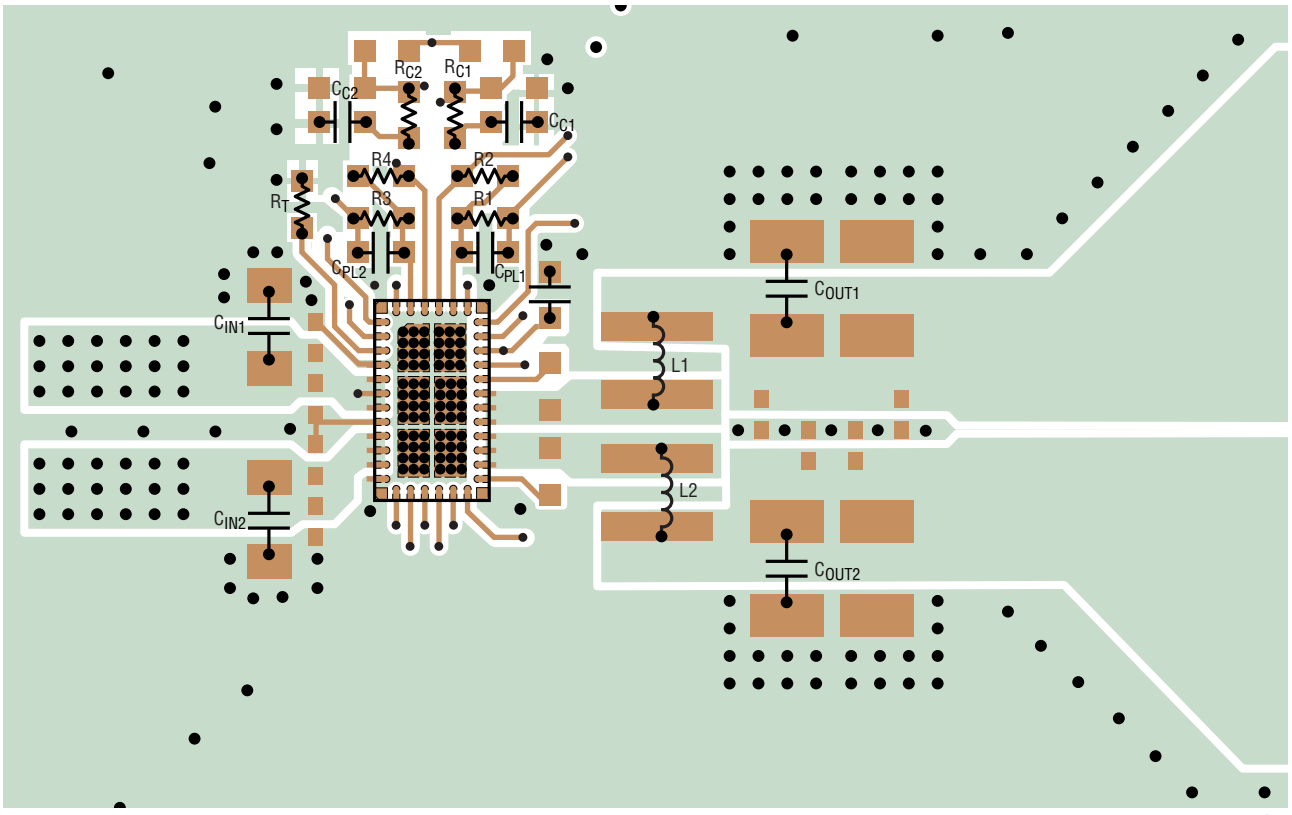


Figure 10. Recommended Layout

APPLICATIONS INFORMATION

High Temperature Considerations

Care should be taken in the layout of the PCB to ensure good heat sinking of the LT8652S. The exposed pad on the bottom of the package must be soldered to a ground plane. This ground should be tied to large copper layers below with thermal vias; these layers will spread heat dissipated by the LT8652S. Placing additional vias can reduce thermal resistance further. The maximum load current should be derated as the ambient temperature approaches the maximum junction rating. Power dissipation within the LT8652S can be estimated by calculating the total power loss from an efficiency measurement and subtracting the inductor loss. The die temperature is calculated by multiplying the LT8652S power dissipation by the thermal resistance from junction to ambient.

The internal thermal shutdown protection of LT8652S will stop switching and indicate a fault condition if junction temperature exceeds 165°C. The fault condition will clear and switching resume when the temperature drops back below 160°C.

Temperature rise of the LT8652S is worst when operating at high load, high V_{IN} and high switching frequency. If the case temperature is too high for a given application, then either V_{IN}, switching frequency or load current can be decreased to reduce the temperature to an acceptable level. Figure 11 shows examples case temperature vs V_{IN}, switching frequency and load.

The LT8652S's internal power switches are capable of safely delivering up to 12A of maximum output current. However, due to thermal limits, the package can only handle 12A loads for short periods of time. Figure 12 shows an example of how case temperature rise changes with the duty cycle of a 1kHz pulsed 12A load.

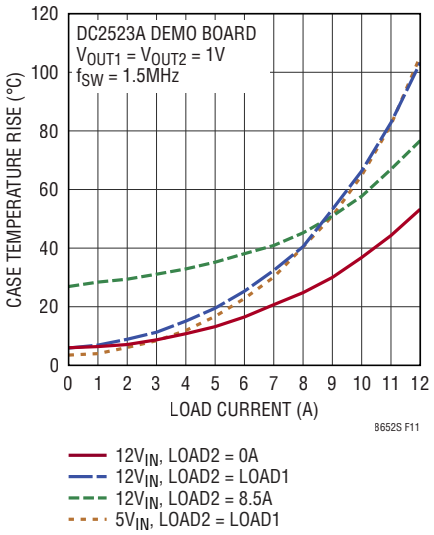


Figure 11. Case Temperature Rise

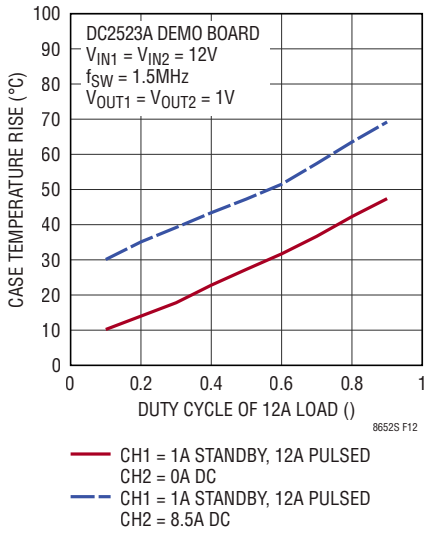
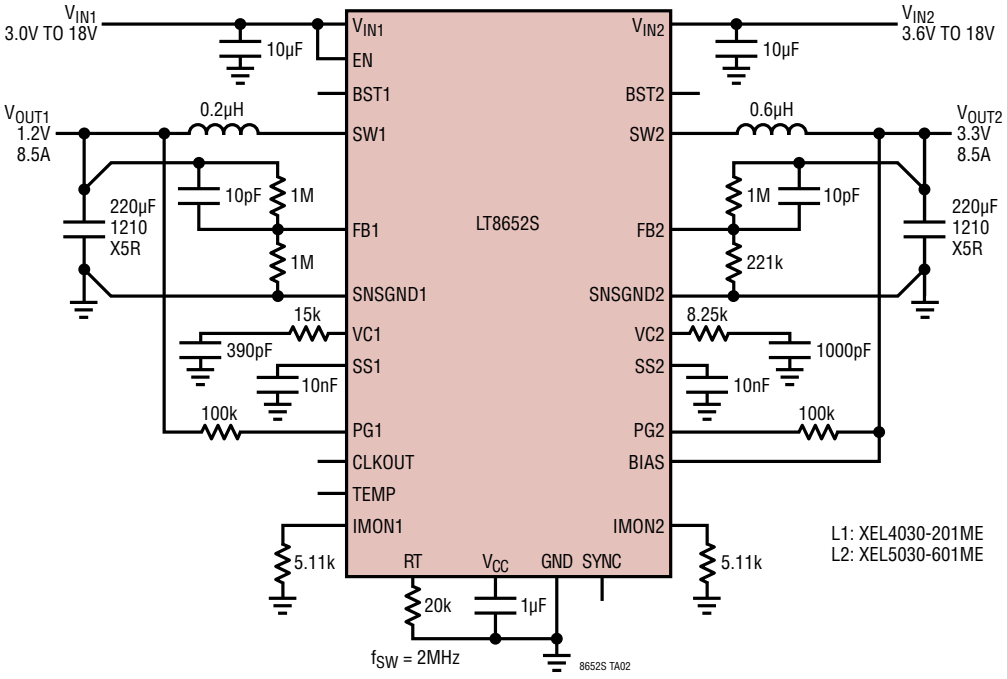


Figure 12. Case Temperature Rise vs 12A Pulsed Load

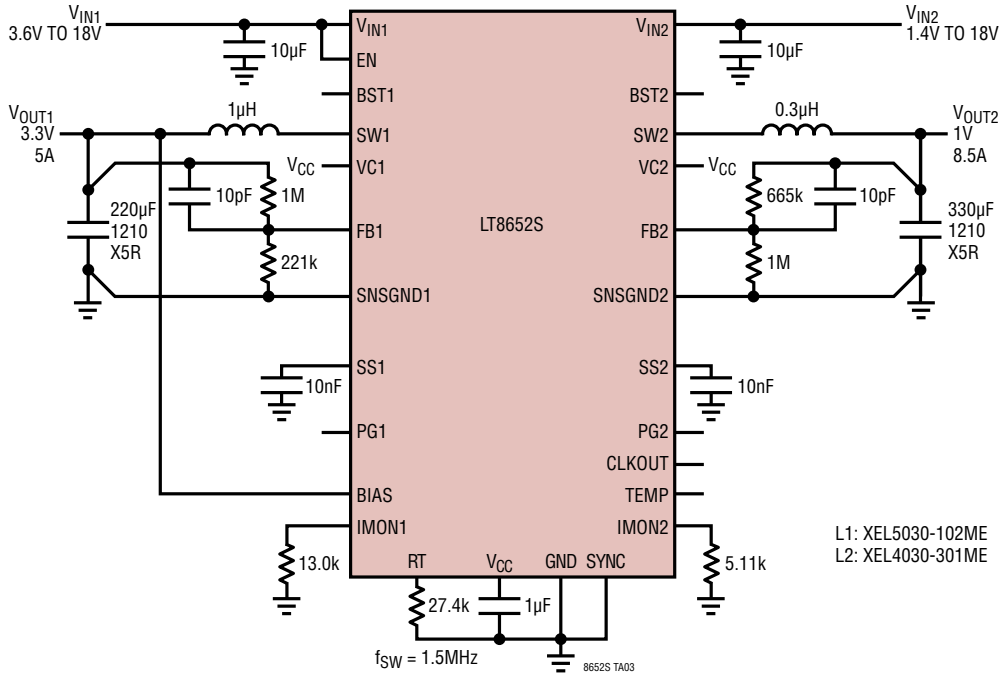
TYPICAL APPLICATIONS

1.2V, 3.3V, 2MHz Step-Down Converter with FCM and External Compensation



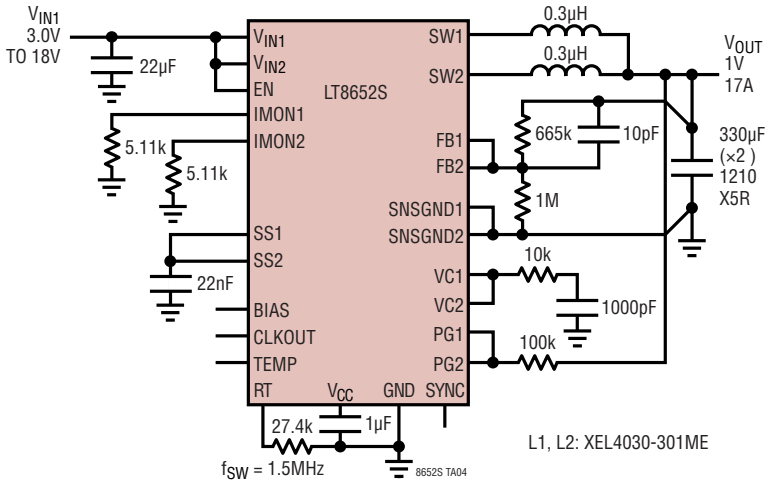
TYPICAL APPLICATIONS

3.3V, 1V, 1.5MHz Step-Down Converter with Burst Mode Operation, CH1 6A Current Limit and Internal Compensation

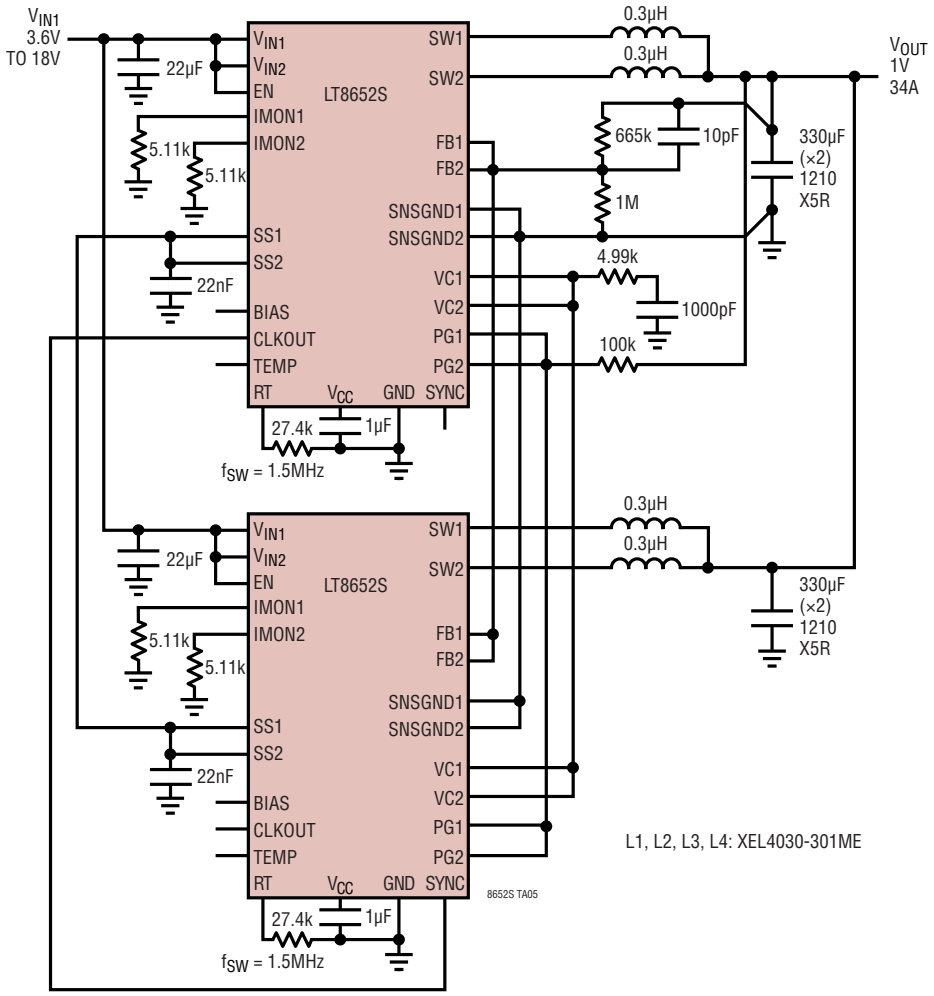


TYPICAL APPLICATIONS

Two-Phase, 1V, 17A, 1.5MHz Step-Down Converter

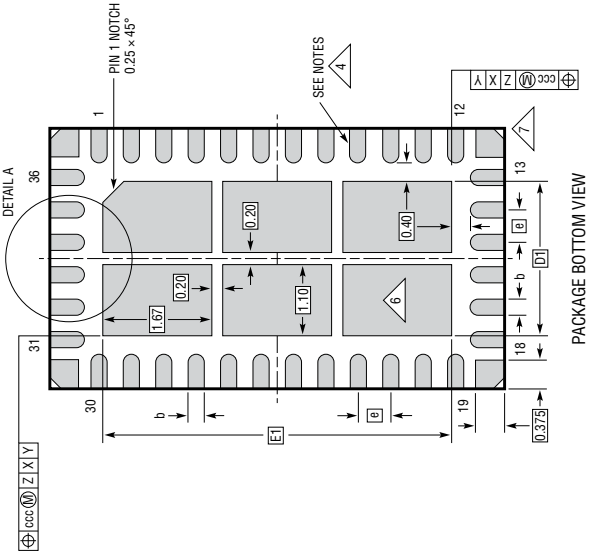


Four-Phase, 1V, 34A, 1.5MHz Step-Down Converter

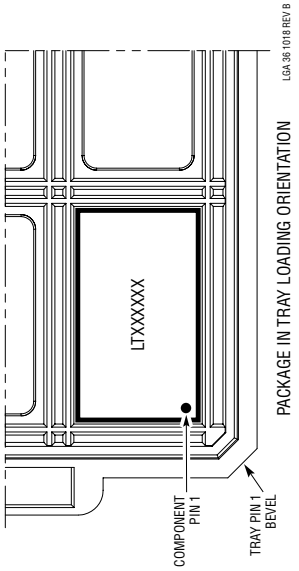


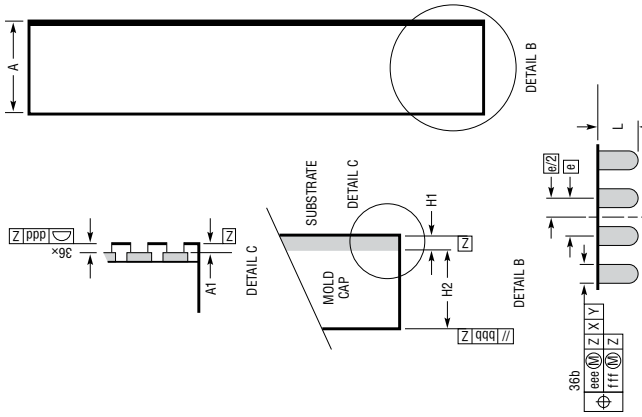
PACKAGE DESCRIPTION

LQFN Package
36-Lead (4mm × 7mm × 0.94mm)
(Reference LTC DWG # 05-08-1525 Rev B)

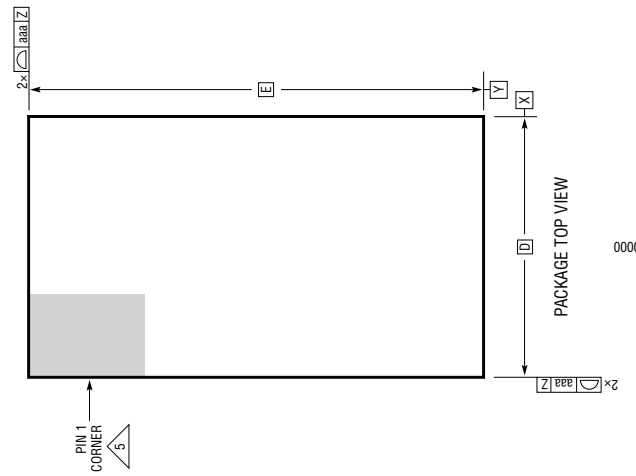


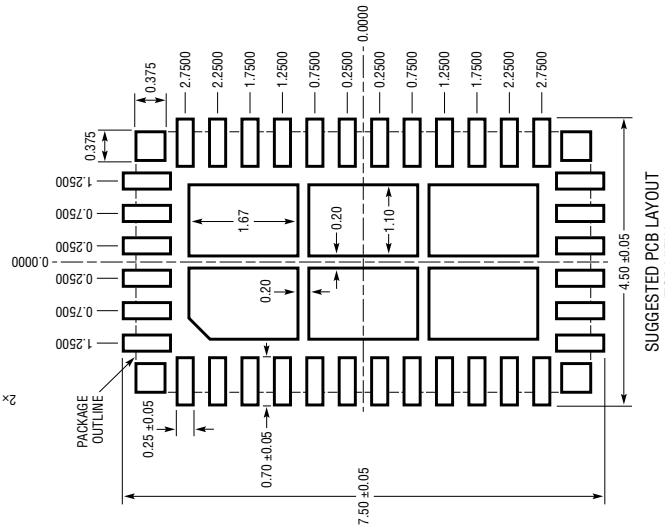
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. PRIMARY DATUM -Z- IS SEATING PLANE
4. METAL FEATURES UNDER THE SOLDER MASK OPENING NOT SHOWN SO AS NOT TO OBSCURE THESE TERMINALS AND HEAT FEATURES
5. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN 1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
6. THE EXPOSED HEAT FEATURE IS SEGMENTED AND ARRANGED IN A MATRIX FORMAT. IT MAY HAVE OPTIONAL CORNER RADII ON EACH SEGMENT
7. CORNER SUPPORT PAD CHAMFER IS OPTIONAL





DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	0.85	0.94	1.03	
A1	0.01	0.02	0.03	
L	0.30	0.40	0.50	
b	0.22	0.25	0.28	
D		4.00		
E		7.00		
D1		2.40		
E1		5.40		
e		0.50		
H1		0.24 REF		SUBSTRATE THK
H2		0.70 REF		MOLD CAP HT
aaa			0.10	
bbb			0.10	
ccc			0.10	
ddd			0.10	
eee			0.15	
fff			0.08	





Rev. B

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	10/20	AEC-Q100 Qualified for Automotive Applications.	1
		Added Pin Configuration notes.	2
		Updated #W Order Information.	2
B	06/21	Updated Tape and Reel Order Information.	2
		Clarified V_{IN1} current to 16µA in 5th paragraph.	16
		Clarified typical application input supply current to 17µA in 6th paragraph.	16

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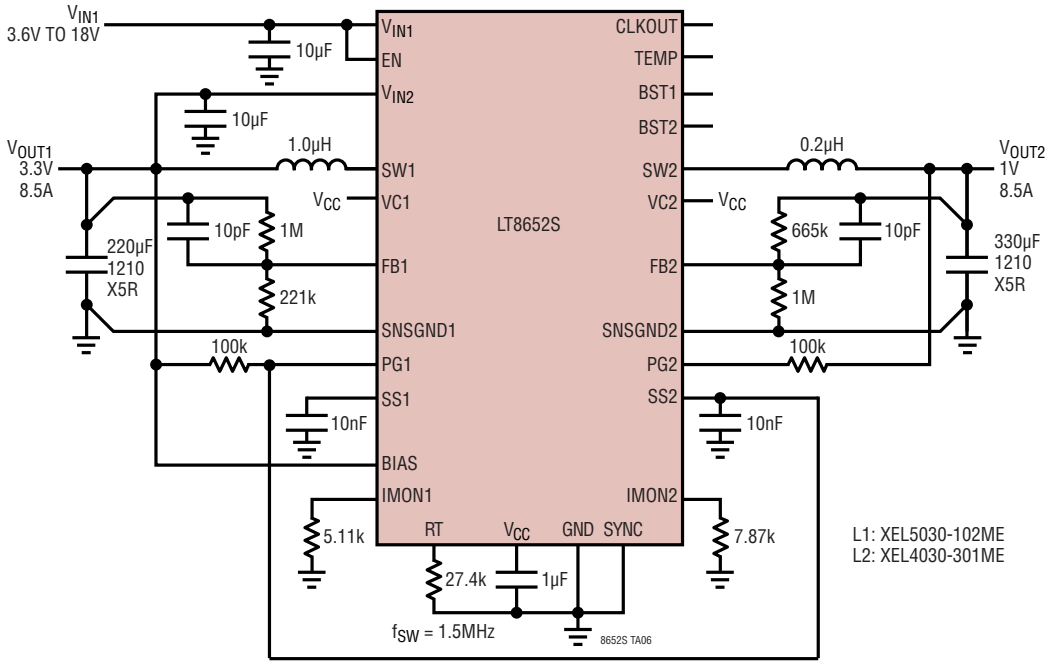
TYPICAL APPLICATION

3.3V, 1V, 1.5MHz Two-Stage Step-Down Converter with Output Sequencing and CH2 10A Current Limit



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT8642S	18V, 10A, 96% Efficiency, 3MHz Synchronous Silent Switcher 2 Step-Down DC/DC Converter	V_{IN} Min = 3V, V_{IN} Max = 18V, V_{OUT} Min = 0.6V, I_Q = 2160µA, I_{SD} <1µA, 4x4 LQFN-24 Package
LT8650S	42V, Dual 4A, 95% Efficiency, 2.2MHz Synchronous Silent Switcher 2 Step-Down DC/DC Converter with I_Q = 6.2µA	V_{IN} Min = 3V, V_{IN} Max = 42V, V_{OUT} Min = 0.8V, I_Q = 6.2µA, I_{SD} <1µA, 4x6 LQFN-32 Package
LT8640S	42V, 5A, 95% Efficiency, 2.2MHz Synchronous Silent Switcher 2 Step-Down DC/DC Converter with I_Q = 2.5µA	V_{IN} Min = 3.4V, V_{IN} Max = 42V, V_{OUT} Min = 0.97V, I_Q = 2.5µA, I_{SD} <1µA, 4x4 LQFN-24 Package
LT8609S	42V, 2A, 95% Efficiency, 2.2MHz Synchronous Silent Switcher 2 Step-Down DC/DC Converter with I_Q = 2.5µA	V_{IN} Min = 3V, V_{IN} Max = 42V, V_{OUT} Min = 0.8V, I_Q = 2.5µA, I_{SD} <1µA, 3x3 LQFN-16 Package
LT8645S	65V, 7A, 95% Efficiency, 2.2MHz Synchronous Silent Switcher 2 Step-Down DC/DC Converter with I_Q = 2.5µA	V_{IN} Min = 3.4V, V_{IN} Max = 65V, V_{OUT} Min = 0.8V, I_Q = 2.5µA, I_{SD} <1µA, 4x6 LQFN-32 Package
LT8609/ LT8609A	42V, 2A, 94% Efficiency, 2.2MHz Synchronous MicroPower Step-Down DC/DC Converter with I_Q = 2.5µA	V_{IN} Min = 3V, V_{IN} Max = 42V, V_{OUT} Min = 0.8V, I_Q = 2.5µA, I_{SD} <1µA, MSOP-10E Package
LT8610A/ LT8610AB	42V, 3.5A, 96% Efficiency, 2.2MHz Synchronous MicroPower Step-Down DC/DC Converter with I_Q = 2.5µA	V_{IN} Min = 3.4V, V_{IN} Max = 42V, V_{OUT} Min = 0.97V, I_Q = 2.5µA, I_{SD} <1µA, MSOP-16E Package
LT8610AC	42V, 3.5A, 96% Efficiency, 2.2MHz Synchronous MicroPower Step-Down DC/DC Converter with I_Q = 2.5µA	V_{IN} Min = 3V, V_{IN} Max = 42V, V_{OUT} Min = 0.8V, I_Q = 2.5µA, I_{SD} <1µA, MSOP-16E Package
LT8610	42V, 2.5A, 96% Efficiency, 2.2MHz Synchronous MicroPower Step-Down DC/DC Converter with I_Q = 2.5µA	V_{IN} Min = 3.4V, V_{IN} Max = 42V, V_{OUT} Min = 0.97V, I_Q = 2.5µA, I_{SD} <1µA,MSOP-16E Package
LT8612	42V, 6A, 96% Efficiency, 2.2MHz Synchronous MicroPower Step-Down DC/DC Converter with I_Q = 2.5µA	V_{IN} Min = 3.4V, V_{IN} Max = 42V, V_{OUT} Min = 0.97V, I_Q = 3.0µA, I_{SD} <1µA, 3x6 QFN-28 Package
LT8602	42V, Quad Output (2.5A+1.5A+1.5A+1.5A) 95% Efficiency, 2.2MHz Synchronous MicroPower Step-Down DC/DC Converter with I_Q = 25µA	V_{IN} Min = 3V, V_{IN} Max = 42V, V_{OUT} Min = 0.8V, I_Q = 25µA, I_{SD} <1µA, 6x6 QFN-40 Package

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