5V, 3A Synchronous Step-Down Silent Switcher in 2mm x 2mm LQFN and 1.6mm x 1.6mm WLCSP

FEATURES

- **Pin Compatible with LTC3308(4A) and LTC3309(6A)**
- **High Efficiency: 8mΩ NMOS, 31mΩ PMOS**
- **Programmable Frequency 1MHz to 3MHz**
  - **Tiny Inductor and Capacitors**
- **Peak Current Mode Control**
  - **22ns Minimum On-Time**
  - **Wide Bandwidth, Fast Transient Response**
- **Silent Switcher® Architecture**
  - **Ultralow EMI Emissions**
- **Low Ripple Burst Mode® Operation with I_Q of 40µA**
- Safely Tolerates Inductor Saturation in Overload
- V_{IN} Range: 2.25V to 5.5V
- V_{OUT} Range: 0.5V to V_{IN}
- V_{OUT} Accuracy: ±1% Over Temperature Range
- Precision 400mV Enable Threshold, 1µA in Shutdown
- Power Good, Internal Compensation and Soft-Start
- Thermally Enhanced 12-Lead 2mm × 2mm LQFN and 16-Pin 1.64mm × 1.64mm WLCSP Packages
- AEC-Q100 Qualified for Automotive Applications

APPLICATIONS

- Optical Networking, Servers, Telecom
- Automotive, Industrial, Communications
- Distributed DC Power Systems (POL)
- FPGA, ASIC, µP Core Supplies
- Battery Operated Systems

DESCRIPTION

The LTC®3307A is a very small, high efficiency, low noise, monolithic synchronous 3A step-down DC/DC converter operating from a 2.25V to 5.5V input supply. Using constant frequency, peak current mode control at switching frequencies 1MHz to 3MHz and minimum on-time as low as 22ns, this regulator achieves fast transient response with small external components. Silent Switcher architecture minimizes EMI emissions.

The LTC3307A operates in forced continuous or pulse-skipping mode for low noise, or low-ripple Burst Mode operation for high efficiency at light loads, ideal for battery-powered systems. The IC regulates output voltages as low as 500mV. Other features include output overvoltage protection, short-circuit protection, thermal shutdown, clock synchronization, and up to 100% duty cycle operation for low dropout. The device is available in a low profile 12-lead 2mm × 2mm × 0.74mm LQFN package with exposed pad for low thermal resistance, and a 16-pin 1.64mm × 1.64mm × 0.5mm WLCSP package.

For applications that require a faster power-on and transient response, the LTC3307A-1 has reduced power-on time, soft-start time, and higher bandwidth.

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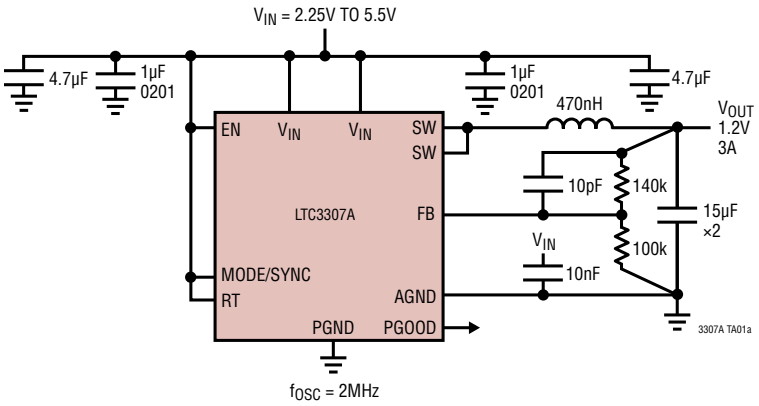
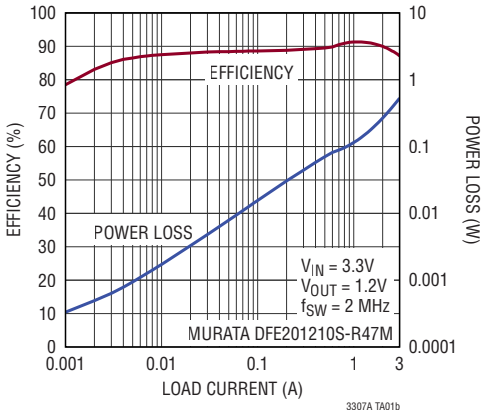
TYPICAL APPLICATION

High Efficiency, 2MHz, 1.2V, 3A Step-Down Converter



Efficiency and Power Loss in Burst Mode Operation



Rev. E

ABSOLUTE MAXIMUM RATINGS

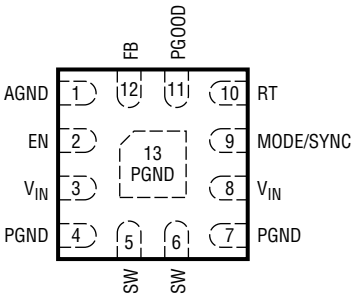
(Note 1)

V_{IN} ..... –0.3V to 6V
EN ..... –0.3V to Lesser of (V_{IN} + 0.3V) or 6V
FB ..... –0.3V to Lesser of (V_{IN} + 0.3V) or 6V
MODE/SYNC ..... –0.3V to Lesser of (V_{IN} + 0.3V) or 6V
RT ..... –0.3V to Lesser of (V_{IN} + 0.3V) or 6V
AGND to PGND ..... –0.3V to +0.3V
PGOOD..... –0.3V to 6V
I_{PGOOD}.....5mA

Operating Junction Temperature Range (Note 2):
LTC3307AE ..... –40˚C to +125°C
LTC3307AI ..... –40˚C to +125°C
LTC3307AA..... –40˚C to +125°C
LTC3307AA-1 ..... –40˚C to +125°C
LTC3307AJ ..... –40˚C to +150°C
LTC3307AH..... –40˚C to +150°C
LTC3307AMP ..... –55˚C to +150°C
Storage Temperature Range ..... –65˚C to +150°C
Maximum Reflow (Package Body) Temperature ... 260°C

PIN CONFIGURATION

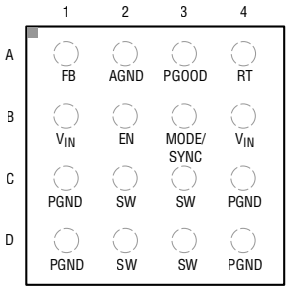
TOP VIEW



LQFN PACKAGE
12-LEAD (2mm × 2mm × 0.74mm)

T_{JMAX} = 150°C, θ_{JA} = 51°C/W, θ_{JB} = 12°C/W,
$\theta_{JCBOTTOM}$ = 8.6°C/W, θ_{JCTOP} = 73°C/W, Ψ_{JT} = 0.6°C/W
θ AND Ψ VALUES DETERMINED PER JESD51-7 ON A JEDEC 2S2P PCB
EXPOSED PAD (PIN 13) IS PGND, MUST BE SOLDERED TO PCB

TOP VIEW



WLCSP PACKAGE
CB-16-11
16-PIN (1.64mm × 1.64mm × 0.5mm)

T_{JMAX} = 125°C, θ_{JA} = 58°C/W, θ_{JCTOP} = 2.7°C/W,
θ_{JB} = 14.8°C/W, Ψ_{JT} = 2.1°C/W, Ψ_{JB} = 15°C/W
θ AND Ψ VALUES DETERMINED PER JESD51-7 ON A JEDEC 2S2P PCB

ORDER INFORMATION

TAPE AND REEL	TAPE AND REEL MINI	PART MARKING*	PACKAGE TYPE	TEMPERATURE RANGE
LTC3307AEV#TRPBF	LTC3307AEV#TRMPBF	LHFR	LQFN (Laminate Package with QFN Footprint)	–40°C to 125°C
LTC3307AIV#TRPBF	LTC3307AIV#TRMPBF	LHFR	LQFN (Laminate Package with QFN Footprint)	–40°C to 125°C
LTC3307AJV#TRPBF	LTC3307AJV#TRMPBF	LHFR	LQFN (Laminate Package with QFN Footprint)	–40°C to 150°C
LTC3307AHV#TRPBF	LTC3307AHV#TRMPBF	LHFR	LQFN (Laminate Package with QFN Footprint)	–40°C to 150°C
LTC3307AMPV#TRPBF	LTC3307AMPV#TRMPBF	LHFR	LQFN (Laminate Package with QFN Footprint)	–55°C to 150°C
LTC3307AACBZ-R7	N/A	3307A	WLCSP (16-Pin Wafer Level Chip Scale Package)	–40°C to 125°C
LTC3307AACBZ-1-R7	N/A	33071	WLCSP (16-Pin Wafer Level Chip Scale Package)	–40°C to 125°C
AUTOMOTIVE PRODUCTS**				
LTC3307AEV#WTRPBF	LTC3307AEV#WTRMPBF	LHFR	LQFN (Laminate Package with QFN Footprint)	–40°C to 125°C
LTC3307AIV#WTRPBF	LTC3307AIV#WTRMPBF	LHFR	LQFN (Laminate Package with QFN Footprint)	–40°C to 125°C
LTC3307AJV#WTRPBF	LTC3307AJV#WTRMPBF	LHFR	LQFN (Laminate Package with QFN Footprint)	–40°C to 150°C
LTC3307AHV#WTRPBF	LTC3307AHV#WTRMPBF	LHFR	LQFN (Laminate Package with QFN Footprint)	–40°C to 150°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500-unit reels through designated sales channels with #TRMPBF suffix.

**Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #W suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range (Note 2), otherwise specifications are at T_A = 25°C; V_{IN} = 3.3V, V_{EN} = V_{IN}, unless otherwise noted.

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Input Supply							
Operating Supply Voltage (V_{IN})			●	2.25		5.5	V
V_{IN} Undervoltage Lockout V_{IN} Undervoltage Lockout Hysteresis	V_{IN} Rising		●	2.0	2.1 150	2.2	V mV
V_{IN} Quiescent Current in Shutdown	V_{EN} = 0.1V				1	2	µA
V_{IN} Quiescent Current	Burst Mode Operation, Sleeping All Modes, Not Sleeping (Note 3)				40 1.2	60 2	µA mA
Enable Threshold Enable Threshold Hysteresis	V_{EN} Rising		●	0.375	0.4 50	0.425	V mV
EN Pin Leakage	V_{EN} =0.5V					±20	nA
Voltage Regulation							
Regulated Feedback Voltage (V_{FB})			●	0.495	0.5	0.505	V
Feedback Voltage Line Regulation	V_{IN} = 2.25V to 5.5V				0.015	0.05	%/V
FB Pin Input Current	V_{FB} = 0.5V					±20	nA
Minimum On Time ($t_{ON,MIN}$)	V_{IN} = 5.5V		●		22	42	ns
Maximum Duty Cycle			●	100			%
Top Switch ON-Resistance					31		mΩ
Bottom Switch ON-Resistance					8		mΩ
Top Switch Current Limit ($I_{PEAKMAX}$)	$V_{OUT}/V_{IN} \leq 0.2$	LTC3307A/LTC3307A-1		4.5	4.8	5.1	A
		LTC3307A-1	●	4.0	4.8	5.7	A

Rev. E

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range (Note 2), otherwise specifications are at T_A = 25°C; V_{IN} = 3.3V, V_{EN} = V_{IN}, unless otherwise noted.

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Bottom Switch Current Limit ($I_{VALLEYMAX}$)	LTC3307A/LTC3307A-1				3.9		A
	LTC3307A-1		●	3.2	3.9	4.5	A
Bottom Switch Reverse Current Limit (I_{REVMAX})	Forced Continuous Mode, LQFN Forced Continuous Mode, WLCSP			–0.75 –0.75	–1.5 –1.5	–2.25 –2.55	A A
SW Leakage Current	V_{EN} = 0.1V				±100		nA
Power Good and Soft-Start							
PGOOD Rising Threshold PGOOD Hysteresis	As a Percentage of the Regulated V_{OUT}		● ●	97 0.7	98 1.2	99 1.7	% %
Overvoltage Rising Threshold Overvoltage Hysteresis	As a Percentage of the Regulated V_{OUT}		● ●	107 1	110 2.2	114 3.5	% %
PGOOD Delay					120		µs
PGOOD Pull Down Resistance	V_{PGOOD} = 0.1V				10	20	Ω
PGOOD Leakage Current	V_{PGOOD} = 5.5V					20	nA
Soft-Start Duration	V_{OUT} rising from 0V to PGOOD Threshold	LTC3307A	●	0.25	1	3	ms
		LTC3307A-1	●	0.3	0.5	0.7	ms
Oscillator and MODE/SYNC							
Default Oscillator Frequency			●	1.9	2	2.1	MHz
Oscillator Frequency with R_T = 34.8kΩ			●	1.9	2	2.1	MHz
Frequency Range	R_T Programming and Synchronization		●	1		3	MHz
Minimum SYNC High or Low Pulse Width			●	40			ns
SYNC Pulse Voltage Levels	Level High Level Low		● ●	1.2		 0.4	V V
MODE/SYNC No Clock Detect Time					10		µs
MODE/SYNC Pin Threshold	For Programming Pulse-Skipping Mode For Programming Forced Continuous Mode For Programming Burst Mode Operation		● ● ●	 1.0 V_{IN} – 0.1	 Float	0.1 V_{IN} – 1.0	V V V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3307A is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3307AEV is guaranteed to meet specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization, and correlation with statistical process controls. The LTC3307AIV is guaranteed over the –40°C to 125°C operating junction temperature range. The LTC3307AJV and LTC3307AHV are guaranteed over the –40°C to 150°C operating junction temperature range. The LTC3307AMPV is guaranteed over the –55°C to 150°C operating junction temperature range. The LTC3307AACBZ/LTC3307AACBZ-1 specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization, and correlation with statistical process controls. High junction temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures above 125°C. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance, and other environmental factors. The junction temperature (T_J in °C) is calculated from ambient temperature (T_A in °C) and power dissipation (P_D in Watts) according to the formula:

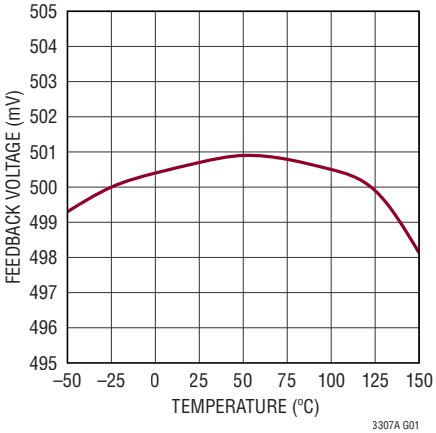
$T_J = T_A + (P_D \bullet \theta_{JA})$, where θ_{JA} (in °C/W) is the package thermal impedance. See High Temperature Considerations section for more details.

The LTC3307A includes overtemperature protection that protects the device during momentary overload conditions. Junction temperatures will exceed 150°C when overtemperature protection is engaged. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

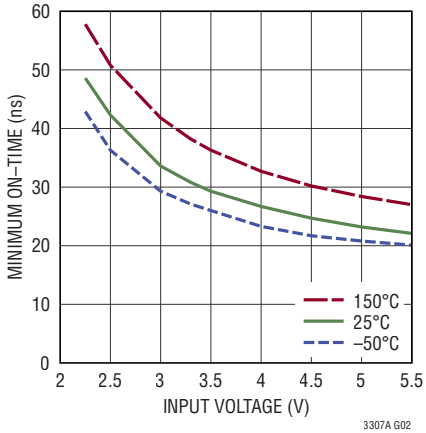
Note 3: Supply current specification does not include switching currents. Actual supply currents will be higher.

TYPICAL PERFORMANCE CHARACTERISTICS V_{IN} = 3.3V, T_A = 25°C, unless otherwise noted.

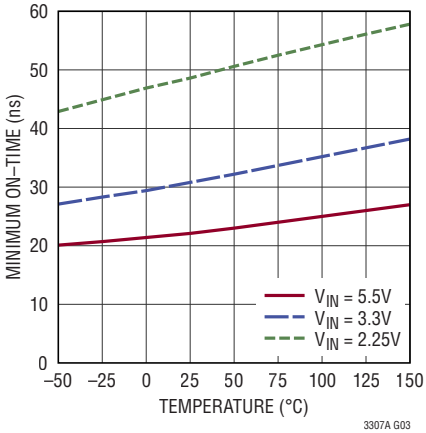
Feedback Voltage



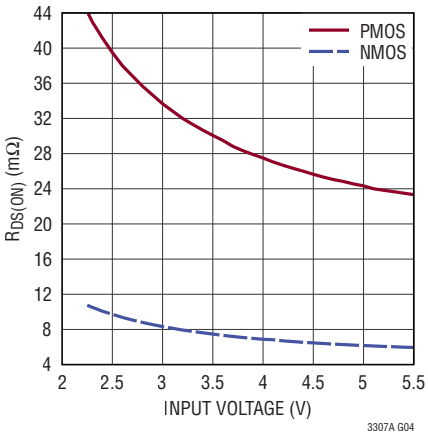
Minimum On-Time



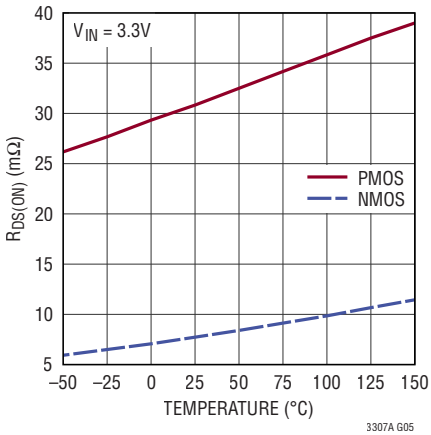
Minimum On-Time



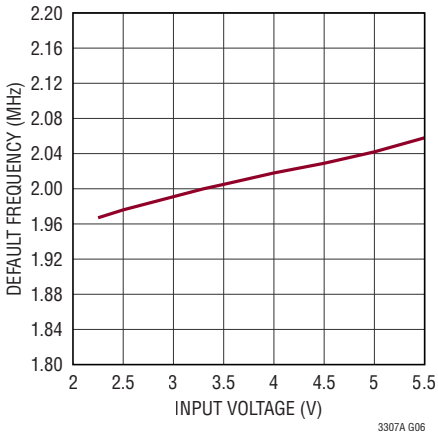
Switch On Resistance



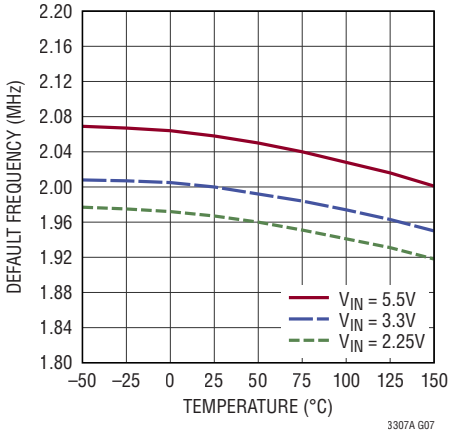
Switch On Resistance



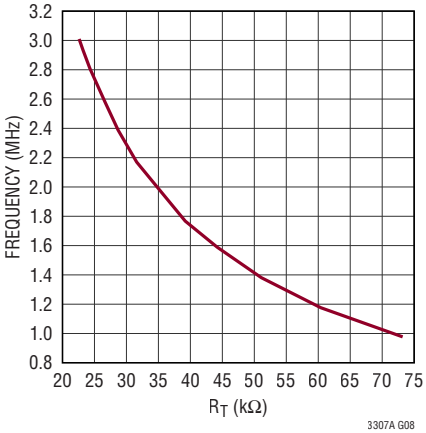
Default Switching Frequency



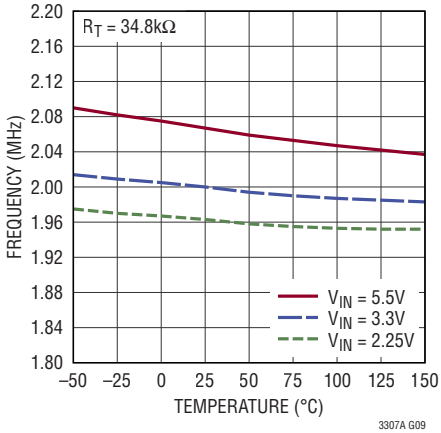
Default Switching Frequency



Switching Frequency

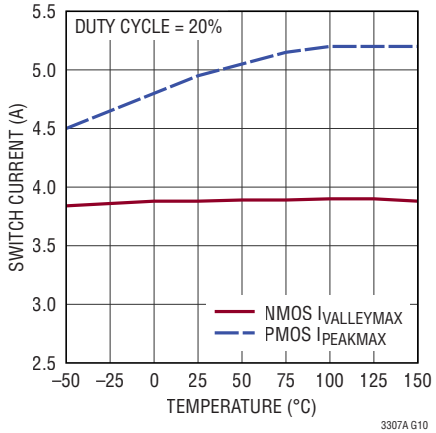


R_T Switching Frequency

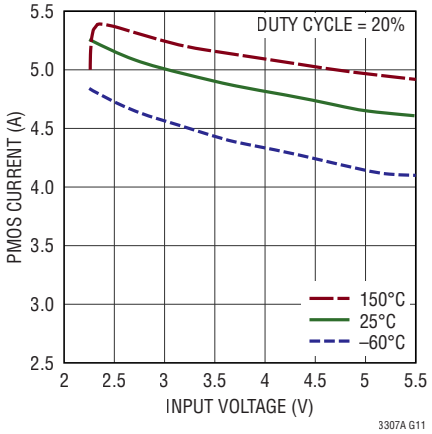


TYPICAL PERFORMANCE CHARACTERISTICS V_{IN} = 3.3V, T_A = 25°C, unless otherwise noted.

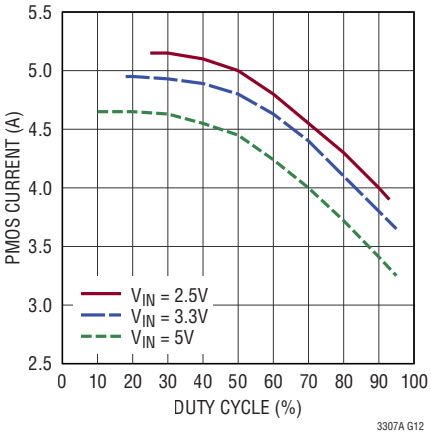
Switch Current Limits



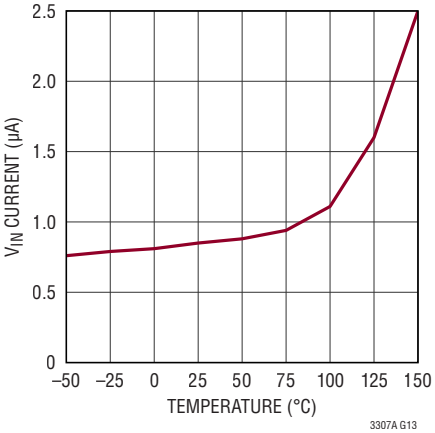
PMOS Current Limit



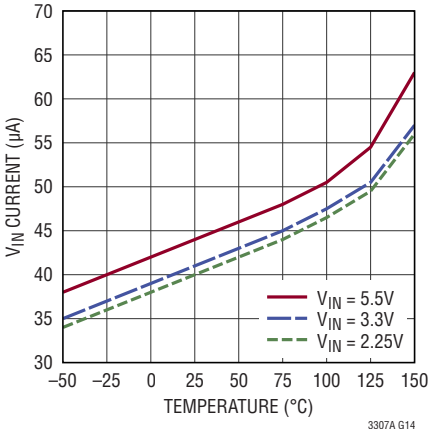
PMOS Current Limit



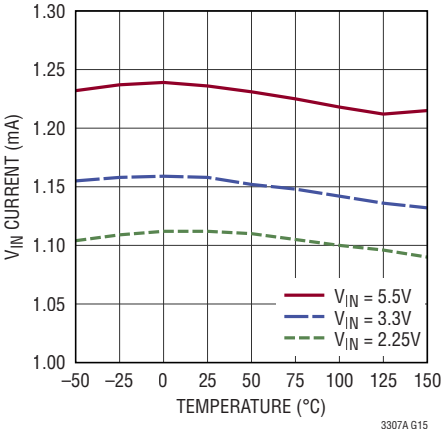
V_{IN} Shutdown Current



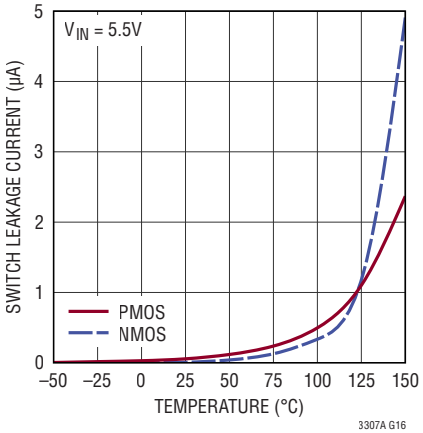
V_{IN} Quiescent Current, Burst Mode Operation, Sleeping



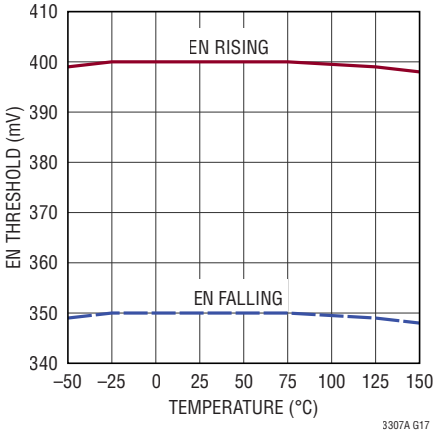
V_{IN} Quiescent Current All Modes, Not Sleeping



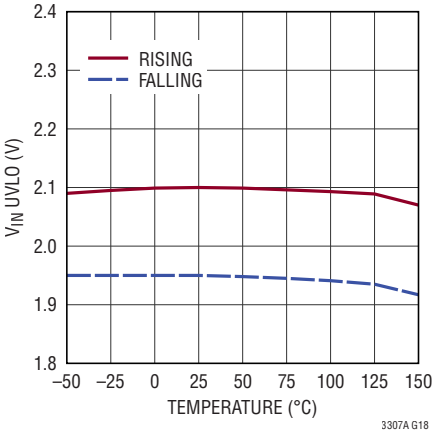
Switch Leakage



EN Threshold

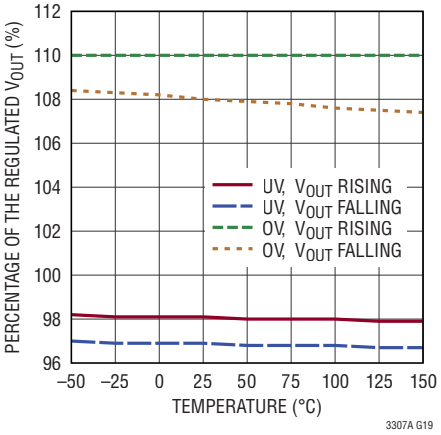


V_{IN} UVLO Threshold

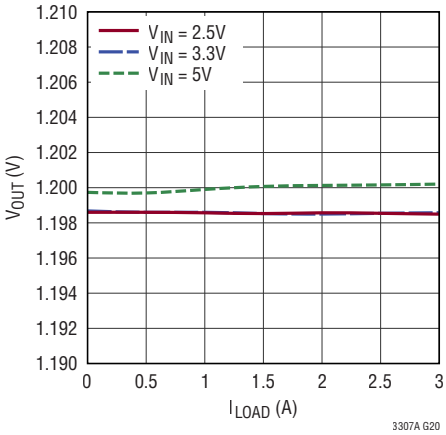


TYPICAL PERFORMANCE CHARACTERISTICS V_{IN} = 3.3V, T_A = 25°C, unless otherwise noted.

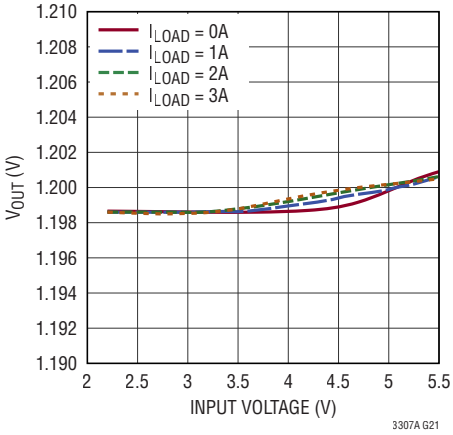
UV, OV PGOOD Thresholds



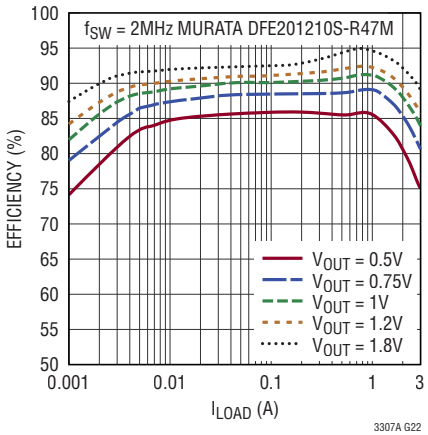
V_{OUT} Load Regulation in V_{OUT} = 1.2V Application



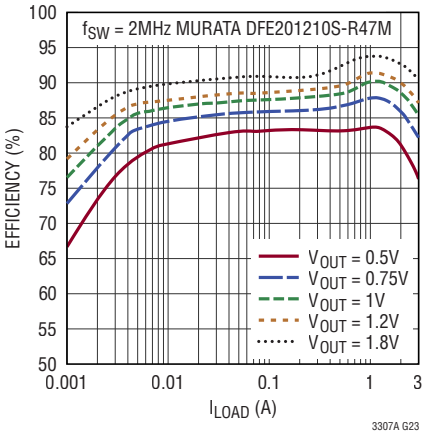
V_{OUT} Line Regulation in V_{OUT} = 1.2V Application



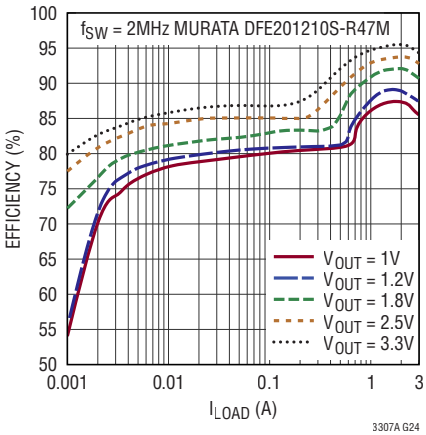
Efficiency, V_{IN} = 2.5V Burst Mode Operation



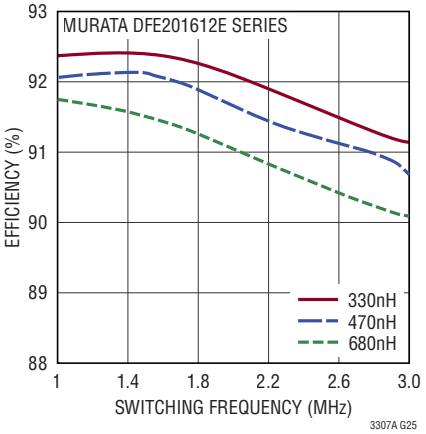
Efficiency, V_{IN} = 3.3V Burst Mode Operation



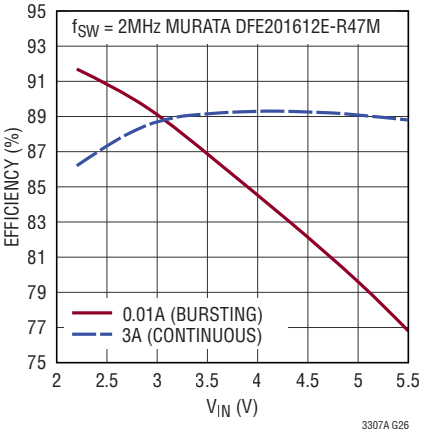
Efficiency, V_{IN} = 5.0V Burst Mode Operation



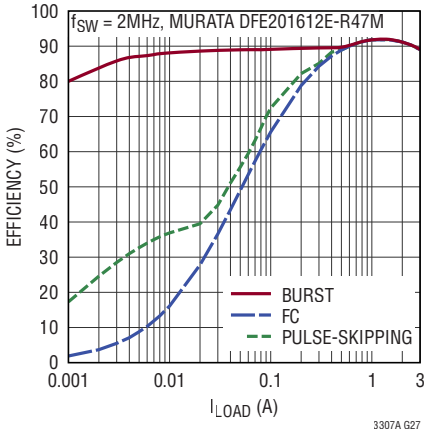
Efficiency vs f_{SW}, $3.3V_{IN}$ to $1.2V_{OUT}$, I_{LOAD} = 1.5A



Efficiency vs V_{IN}, V_{OUT} = 1.2V, f_{SW} = 2MHz, Burst Mode Operation

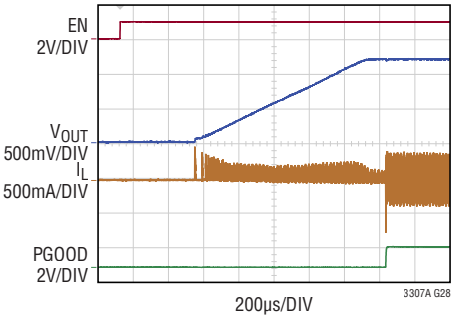


Efficiency vs Load, 3.3V to 1.2V, f_{SW} = 2MHz



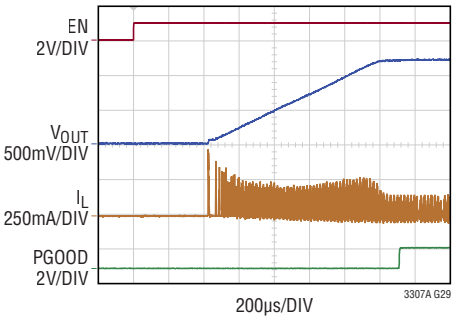
TYPICAL PERFORMANCE CHARACTERISTICS V_{IN} = 3.3V, T_A = 25°C, unless otherwise noted.

Start-Up Waveforms Forced Continuous Mode



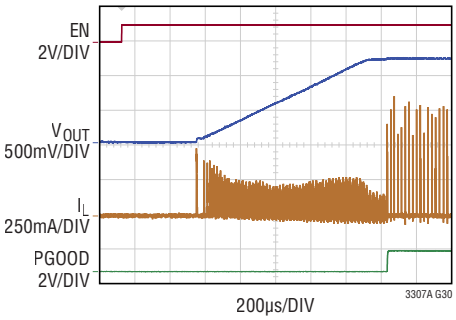
$3.3V_{IN}$ TO $1.2V_{OUT}$, 2MHz TYPICAL APPLICATION
R_{LOAD} = 120Ω The LTC3307A is shown.
The time scale for the LTC3307A-1 is different.

Start-Up Waveforms Pulse-Skipping Mode



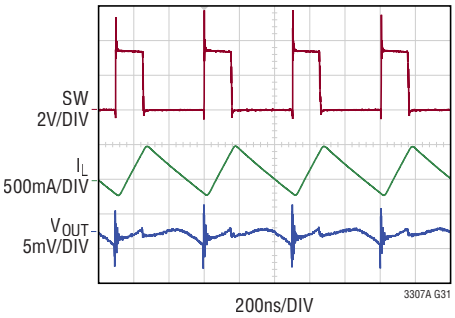
$3.3V_{IN}$ TO $1.2V_{OUT}$, 2MHz TYPICAL APPLICATION
R_{LOAD} = 120Ω The LTC3307A is shown.
The time scale for the LTC3307A-1 is different.

Start-Up Waveforms Burst Mode



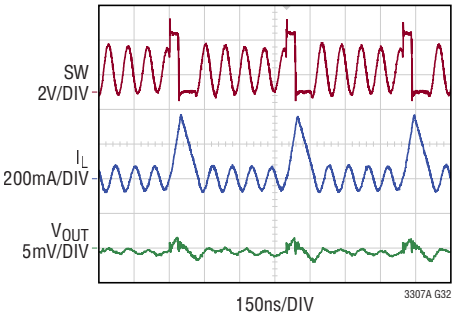
$3.3V_{IN}$ TO $1.2V_{OUT}$, 2MHz TYPICAL APPLICATION
R_{LOAD} = 120Ω The LTC3307A is shown.
The time scale for the LTC3307A-1 is different.

Switching Waveforms, Forced Continuous Mode



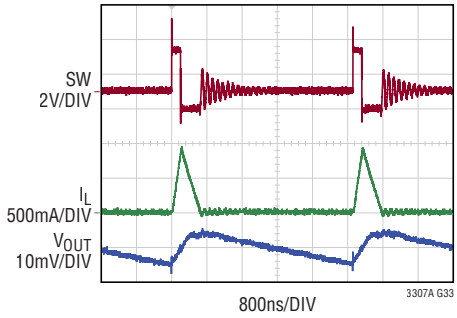
$3.3V_{IN}$ TO $1.2V_{OUT}$, 2MHz TYPICAL APPLICATION
I_{LOAD} = 500mA

Switching Waveforms, Pulse-Skipping Mode



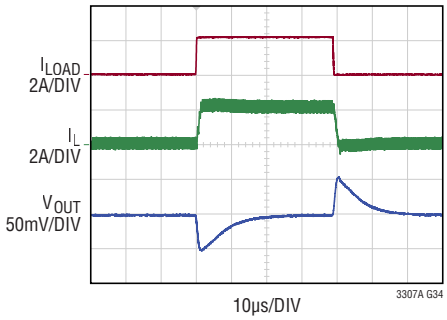
$3.3V_{IN}$ TO $1.2V_{OUT}$, 2MHz TYPICAL APPLICATION
I_{LOAD} = 40mA

Switching Waveforms, Burst Mode Operation



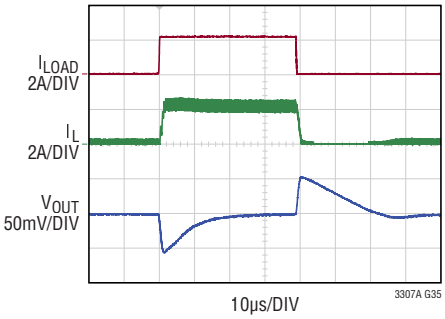
$3.3V_{IN}$ TO $1.2V_{OUT}$, 2MHz TYPICAL APPLICATION
I_{LOAD} = 50mA

Load Transient Response, Forced Continuous Mode



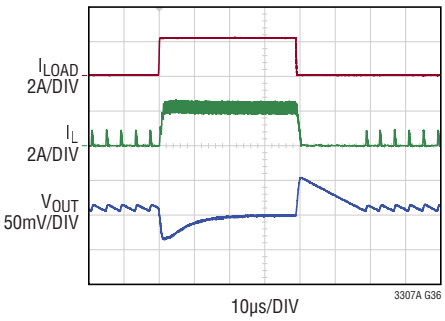
$3.3V_{IN}$ TO $1.2V_{OUT}$, 2MHz TYPICAL APPLICATION
C_{OUT} = 30µF, L = 470nH
LOAD STEP: 50mA TO 2.25A (10A/µs)

Load Transient Response, Pulse-Skipping Mode



$3.3V_{IN}$ TO $1.2V_{OUT}$, 2MHz TYPICAL APPLICATION
C_{OUT} = 30µF, L = 470nH
LOAD STEP: 50mA TO 2.25A (10A/µs)

Load Transient Response, Burst Mode Operation



$3.3V_{IN}$ TO $1.2V_{OUT}$, 2MHz TYPICAL APPLICATION
C_{OUT} = 30µF, L = 470nH
LOAD STEP: 50mA TO 2.25A (10A/µs)

PIN FUNCTIONS (LQFN/WLCSP)

AGND (Pin 1/Pin A2): The AGND pin is the output voltage remote ground sense. Connect the AGND pin directly to the negative terminal of the output capacitor at the load. The AGND pin is also the ground reference for the internal analog circuitry. Place a small analog bypass 0201 or 0402 ceramic capacitor as close as possible to the V_{IN} (Pin 3/Pin B1) and AGND pins. Connect RT and FB returns to AGND as well.

EN (Pin 2/Pin B2): The EN pin has a precision IC enable threshold with hysteresis. An external resistor divider, from V_{IN} or from another supply, can be used to program the threshold below which the LTC3307A will shut down. If the precision threshold is not required, tie EN directly to V_{IN}. When the EN pin is low the LTC3307A enters a low current shutdown mode where all internal circuitry is disabled. Do not float this pin.

V_{IN} (Pins 3, 8/Pins B1, B4): The V_{IN} pins supply current to internal circuitry and topside power switch. Connect both V_{IN} pins together with short wide traces and bypass to PGND and AGND with low ESR capacitors located as close as possible to the pins.

PGND (Pins 4, 7, Exposed Pad Pin 13/Pins C1, C4, D1, D4): The PGND pins are the return path of the internal bottom side power switch. Connect the negative terminal of the input capacitors as close to the PGND pins as possible. For low parasitic inductance and good thermal performance, connect Pin 4 and Pin 7 (Pins C1, C4, D1, D4) to a large continuous ground plane on the printed circuit board directly under the LTC3307A. On the LQFN package, the PGND exposed pad is the main electrical and thermal highway and should be connected to large PCB ground plane(s) with many vias.

SW (Pins 5, 6/Pins C2, C3, D2, D3): The SW pins are the switching outputs of the internal power switches. Connect these pins together and to the inductor with a short, wide trace.

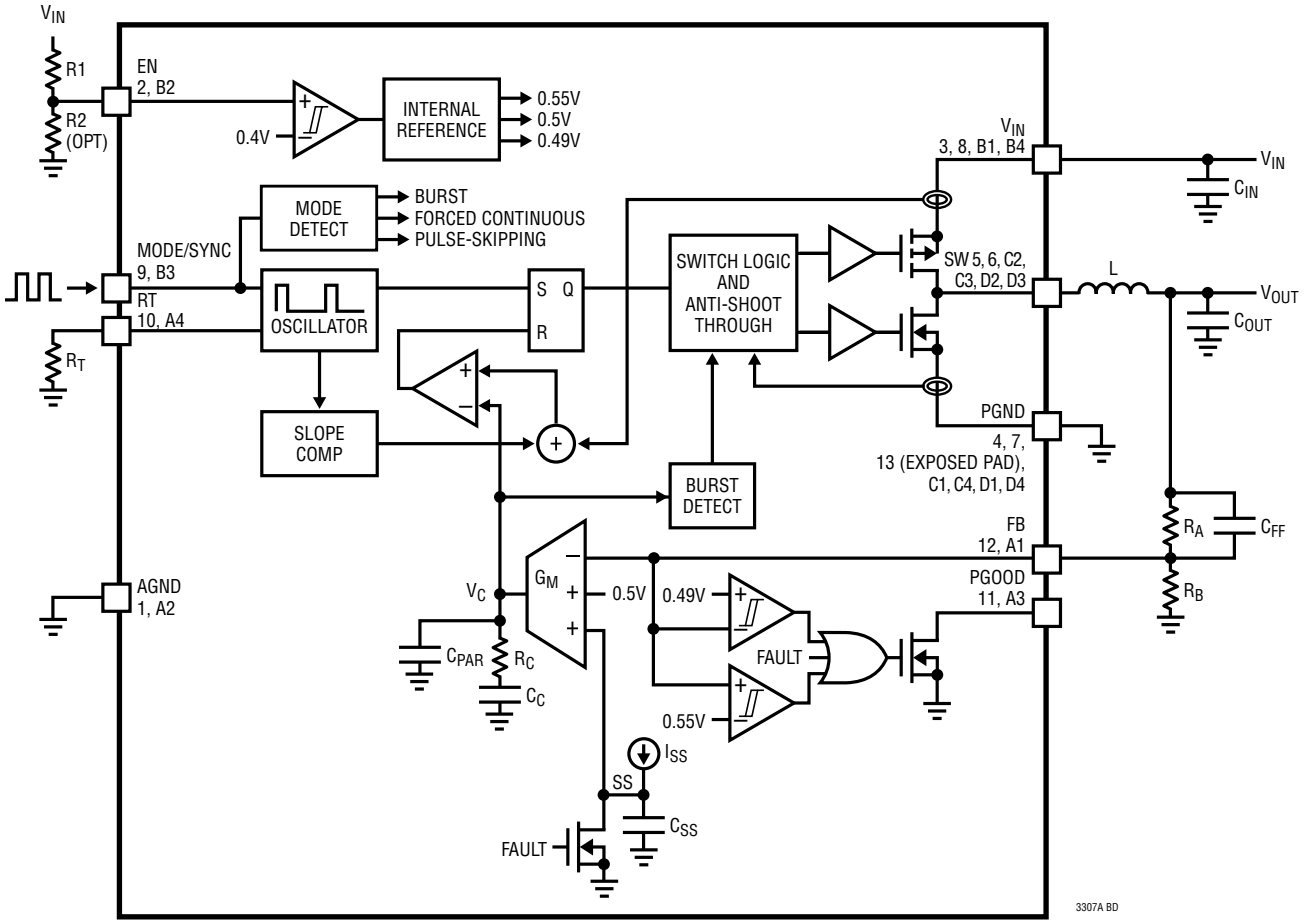
MODE/SYNC (Pin 9/Pin B3): The MODE/SYNC pin is a mode selection and external clock synchronization input. Ground this pin to enable pulse-skipping mode at light loads. For higher efficiency at light loads, tie this pin to V_{IN} to enable the low-ripple Burst Mode operation. For faster transient response, lower noise and full frequency operation over a wide load range, float this pin to enable forced continuous mode. Drive MODE/SYNC with an external clock to synchronize the switcher to the applied frequency. While synchronizing, the part operates in the forced continuous mode. The slope compensation is automatically adapted to the external clock frequency. In the absence of an external clock the switching frequency is determined by the RT pin.

RT (Pin 10/Pin A4): The RT pin sets the switching frequency with an external resistor to AGND. If this pin is tied to V_{IN}, the buck will switch at the default oscillator frequency. If the external clock is driving the MODE/SYNC pin, the RT pin is ignored.

PGOOD (Pin 11/Pin A3): The PGOOD pin is the open drain output of an internal power good comparator. When the regulated output voltage falls below the PGOOD threshold or rises above the overvoltage threshold, this pin is pulled low. When V_{IN} is above V_{IN} UVLO and the part is in shutdown, this pin is also pulled low.

FB (Pin 12/Pin A1): Program the output voltage and close the control loop by connecting this pin to the middle node of a resistor divider between the V_{OUT} and AGND. The LTC3307A regulates FB to 500mV (typical). A phase lead capacitor connected between FB and V_{OUT} may be used to optimize transient response.

BLOCK DIAGRAM



OPERATION

Voltage Regulation

The LTC3307A is a 5V, 3A monolithic, constant frequency, peak current mode control, step-down DC/DC converter. The synchronous buck switching regulators are internally compensated and require only external feedback resistors to set the output voltage. An internal oscillator, with the frequency set using a resistor on the RT pin or synchronized to an external clock, turns on the internal top power switch at the beginning of each clock cycle. Current in the inductor ramps up until the top switch current comparator trips and turns off the top power switch. The peak inductor current at which the top switch turns off is controlled by an internal V_C voltage. The error amplifier regulates V_C by comparing the voltage on the FB pin with an internal 500mV reference. An increase in the load current causes a reduction in the feedback voltage relative to the reference, causing the error amplifier to raise the V_C voltage until the average inductor current matches the new load current. When the top power switch turns off, the synchronous power switch turns on and ramps down the inductor current for the remainder of the clock cycle or, if in pulse-skipping or Burst mode, until the inductor current falls to zero. If an overload condition results in excessive current flowing through the bottom switch, the next clock cycle will be skipped until switch current returns to a safe level.

The enable pin has a precision 400mV threshold to provide event-based power-up sequencing by connecting the EN pin to the output of another buck through a resistor divider. If the EN pin is low, the device is shut down and in a low quiescent current state. When the EN pin is above its threshold, the switching regulator will be enabled.

The LTC3307A has forward and reverse inductor current limiting, short-circuit protection, output over-voltage protection, and soft-start to limit inrush current during start-up or recovery from a short-circuit.

Mode Selection

The LTC3307A operates in three different modes set by the MODE/SYNC pin: pulse-skipping mode (when the MODE/SYNC pin is set low), forced continuous mode (when the MODE/SYNC pin is floating) and Burst Mode operation (when the MODE/SYNC pin is set high).

In pulse-skipping mode, the oscillator operates continuously and positive SW transitions are aligned to the clock. Negative inductor current is disallowed and, during light loads, switch pulses are skipped to regulate the output voltage.

In forced continuous mode, the oscillator operates continuously. The top switch turns on every cycle and regulation is maintained by allowing the inductor current to reverse at light load. This mode allows the buck to run at a fixed frequency with minimal output ripple. In forced continuous mode, if the inductor current reaches I_{REVMAX} (into the SW pin), the bottom switch will turn off for the remainder of the cycle to limit the current.

In Burst Mode operation at light loads, the output capacitor is charged to a voltage slightly higher than its regulation point. The regulator then goes into a sleep state, during which time the output capacitor provides the load current. In sleep, most of the regulator's circuitry is powered down, helping conserve input power. When the output voltage drops below its programmed value, the circuitry is powered on and another burst cycle begins. The sleep time decreases as load current increases. In Burst Mode operation, the regulator will burst at light loads whereas at higher loads it will operate in constant frequency PWM mode.

OPERATION

Synchronizing the Oscillator to an External Clock

The LTC3307A's internal oscillator can be synchronized through an internal PLL circuit to an external frequency by applying a square wave clock signal to the MODE/SYNC pin.

During synchronization, the top power switch turn-on is locked to the rising edge of the external frequency source. While synchronizing, the switcher operates in forced continuous mode. The slope compensation is automatically adapted to the external clock frequency. The synchronization frequency range is 1MHz to 3MHz.

After detecting an external clock on the first rising edge of the MODE/SYNC pin, the internal PLL gradually adjusts its operating frequency to match the frequency and phase of the signal on the MODE/SYNC pin. When the external clock is removed, the LTC3307A will detect the absence of the external clock within approximately 10µs. During this time, the PLL will continue to provide clock cycles. Once the external clock removal has been detected, the oscillator will gradually adjust its operating frequency to the one programmed by the RT pin.

Output Power Good

When the LTC3307A's output voltage is within the –2%/+10% window of the nominal regulation voltage the output is considered good and the open-drain PGOOD pin goes high impedance and is typically pulled high with an external resistor. Otherwise, the internal pull-down device will pull the PGOOD pin low. The PGOOD pin is also pulled low during the following fault conditions: EN pin is low, V_{IN} is too low or thermal shutdown. To filter noise and short duration output voltage transients, the lower threshold has a hysteresis of 1.2%, the upper threshold has a hysteresis of 2.2%, and both have a built-in time delay to report PGOOD, typically 120µs.

Output Overvoltage Protection

During an output overvoltage event, when the FB pin voltage is greater than 110% of nominal, the LTC3307A top power switch will be turned off. If the output remains out of regulation for more than 120µs, the PGOOD pin will be pulled low.

An output overvoltage event should not happen under normal operating conditions.

Overtemperature Protection

To prevent thermal damage to the LTC3307A and its surrounding components, the device incorporates an overtemperature (OT) function. When the die temperature reaches 165°C (typical, not tested) the switcher is shut down and remains in shutdown until the die temperature falls to 160°C (typical, not tested).

Output Voltage Soft-Start

Soft starting the output prevents current surge on the input supply and/or output voltage overshoot. During the soft-start, the output voltage will proportionally track the internal node voltage ramp. An active pull-down circuit discharges that internal node in the case of fault conditions. The ramp will restart when the fault is cleared. Fault conditions that initiate the soft-start ramp are the EN pin transitioning low, V_{IN} voltage falling too low, or thermal shutdown.

Dropout Operation

As the input supply voltage approaches the output voltage, the duty cycle increases toward 100%. Further reduction of the supply voltage forces the main switch to remain on for more than one cycle, eventually reaching 100% duty cycle. The output voltage will then be determined by the input voltage minus the DC voltage drop across the internal P-channel MOSFET and the inductor.

Low Supply Operation

The LTC3307A is designed to operate down to an input supply voltage of 2.25V. One important consideration at low input supply voltages is that the $R_{DS(ON)}$ of the internal power switches increases. Calculate the worst case LTC3307A power dissipation and die junction temperature at the lowest input voltages.

Output Short-Circuit Protection and Recovery

The peak inductor current level, at which the current comparator shuts off the top power switch, is controlled by the internal V_C voltage. When the output current increases, the error amplifier raises V_C until the average inductor current matches the load current. The LTC3307A clamps the maximum V_C voltage, thereby limiting the peak inductor current.

When the output is shorted to ground, the inductor current decays very slowly when the bottom power switch is on because the voltage across the inductor is low. To keep the inductor current in control, a secondary limit is imposed on the valley of the inductor current. If the inductor current measured through the bottom power switch remains greater than $I_{VALLEYMAX}$ at the end of the cycle, the top power switch will be held off. Subsequent switching cycles will be skipped until the inductor current falls below $I_{VALLEYMAX}$.

Recovery from an output short circuit may involve a soft-start cycle if V_{FB} falls more than approximately 100mV below regulation. During such a recovery, V_{FB} will quickly charge up by that ~100mV and then follow the soft-start ramp until regulation is reached.

APPLICATIONS INFORMATION

Refer to the Block Diagram for reference.

Output Voltage and Feedback Network

The output voltage is programmed by a resistor divider between the output and the FB pin. Choose the resistor values according Equation 1.

$$R_A = R_B\left(\frac{V_{OUT}}{500mV} - 1\right) \quad (1)$$

as shown in Figure 1:

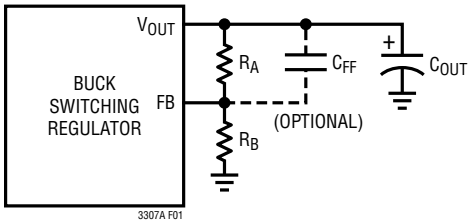


Figure 1. Feedback Resistor Network

Reference designators refer to the Block Diagram. Typical values for R_B range from 40kΩ to 400kΩ. 0.1% resistors are recommended to maintain output voltage accuracy. The buck regulator transient response may improve with an optional phase lead capacitor C_{FF} that helps cancel the pole created by the feedback resistors and the input capacitance of the FB pin. Experimentation with capacitor values between 2pF and 22pF may improve transient response. The values used in the typical application circuits are a good starting point.

Operating Frequency Selection and Trade-Offs

Selection of the operating frequency is a trade-off between efficiency, component size, transient response and input voltage range.

The advantage of high frequency operation is that smaller inductor and capacitor values may be used. Higher switching frequencies allow for higher control loop bandwidth and, therefore, faster transient response. The disadvantages of higher switching frequencies are lower efficiency, because of increased switching losses, and a smaller input voltage range, because of minimum switch on-time limitations.

APPLICATIONS INFORMATION

The minimum on-time of the buck regulator imposes a minimum operating duty cycle. The highest switching frequency ($f_{SW(MAX)}$) for a given application can be calculated with Equation 2.

$$f_{SW(MAX)} = \frac{V_{OUT}}{t_{ON(MIN)} \bullet V_{IN(MAX)}} \quad (2)$$

where $V_{IN(MAX)}$ is the maximum input voltage, V_{OUT} is the output voltage and $t_{ON(MIN)}$ is the minimum top switch on-time. This equation shows that a slower switching frequency is necessary to accommodate a high $V_{IN(MAX)}/V_{OUT}$ ratio.

The LTC3307A is capable of a maximum duty cycle of 100%, therefore, the V_{IN}-to-V_{OUT} dropout is limited by the $R_{DS(ON)}$ of the top switch, the inductor DCR and the load current.

Setting the Switching Frequency

The LTC3307A uses a constant frequency peak current mode control architecture. There are three methods to set the switching frequency.

The first method, connecting the RT pin to V_{IN}, sets the switching frequency to the internal default with a nominal value of 2MHz.

The second method is with a resistor (R_T) tied from the RT pin to ground. The frequency can be programmed from 1MHz to 3MHz. Table 1 and the Equation 3 show the necessary R_T value for a desired switching frequency.

$$R_T = \frac{73.4}{f_{sw}} - 1.9 \quad (3)$$

where R_T is in kΩ and f_{SW} is the desired switching frequency in MHz, ranging from 1MHz to 3MHz.

The third method to set the switching frequency is by synchronizing the internal PLL circuit to an external square wave clock applied to the MODE/SYNC pin. The synchronization frequency range is 1MHz to 3MHz. The square wave amplitude should have valleys that are below 0.4V and peaks above 1.2V. High and low pulse widths should both be at least 40ns.

Table 1. R_T Value vs Switching Frequency

f_{SW} (MHz)	R_T (kΩ)
1.0	71.5
1.2	59.0
1.4	49.9
1.6	43.2
1.8	38.3
2.0	34.8
2.2	30.9
2.4	28.7
2.6	26.1
2.8	24.3
3.0	22.6

Inductor Selection and Maximum Output Current

Considerations in choosing an inductor are inductance, RMS current rating, saturation current rating, DCR and core loss.

Select the inductor value based on Equation 4 and Equation 5.

$$L \approx \frac{V_{OUT}}{0.9A \bullet f_{SW}} \bullet \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right) \text{ for } \frac{V_{OUT}}{V_{IN(MAX)}} \le 0.5 \quad (4)$$

$$L \approx \frac{0.25 \bullet V_{IN(MAX)}}{0.9A \bullet f_{SW}} \text{ for } \frac{V_{OUT}}{V_{IN(MAX)}} > 0.5 \quad (5)$$

where f_{SW} is the switching frequency, $V_{IN(MAX)}$ is the maximum input voltage.

To avoid overheating of the inductor choose an inductor with an RMS current rating that is greater than the maximum expected output load of the application. Overload and short-circuit conditions need to be taken into consideration.

In addition, ensure that the saturation current rating (typically labeled I_{SAT}) of the inductor is higher than the maximum expected load current plus half the inductor ripple current use Equation 6.

$$I_{SAT} > I_{LOAD(MAX)} + \frac{1}{2}\Delta I_L \quad (6)$$

APPLICATIONS INFORMATION

where $I_{LOAD(MAX)}$ is the maximum output load current for a given application and ΔI_L is the inductor ripple current calculated with Equation 7.

$$\Delta I_L = \frac{V_{OUT}}{L \bullet f_{SW}} \bullet \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (7)$$

A more conservative choice would be to use an inductor with an I_{SAT} rating higher than the maximum current limit of the LTC3307A.

To keep the efficiency high, choose an inductor with the lowest series resistance (DCR). The core material should be intended for high frequency applications. Table 2 shows recommended inductors from several manufacturers.

Input Capacitors

Bypass the input of the LTC3307A with at least two ceramic capacitors close to the part, one on each side from V_{IN} to PGND, for best performance. These capacitors should be 0603 or 0805 in size. Smaller, optional 0201 capacitors can also be placed as close as possible to the LTC3307A directly on the traces leading from V_{IN} (Pin 3, Pin B1) and PGND (Pin 4, Pins C1, D1) and on the traces leading from V_{IN} (Pin 8, Pin B4) and PGND (Pin 7, Pins C4, D4) for better performance with minimal (if at all)

Table 2. Recommended Inductors with Typical Specifications

MANUFACTURER	INDUCTOR FAMILY	INDUCTANCE (nH)	I_{TEMP} (A)*	I_{SAT} (A)	DCR (mΩ)	W × L × H (mm)
Murata	DFE18SAN-E0	240	3.2	4.2	36	1.6 × 0.8 × 0.8
Murata	DFE18SAN-G0	240	3.5	4.9	30	1.6 × 0.8 × 1.0
Murata	DFE201210S	110, 470	6.3, 4.0	11, 5.3	8, 27	2.0 × 1.2 × 1.0
Murata	DFE201210U	240 to 470	3.8 to 3.0	6.5 to 4.4	20 to 34	2.0 × 1.2 × 1.0
Murata	DFE201610E	240 to 680	5.5 to 3.7	7.0 to 4.8	16 to 36	2.0 × 1.6 × 1.0
Murata	DFE201612E	240 to 680	6.0 to 4.1	7.8 to 4.8	13 to 27	2.0 × 1.6 × 1.2
Murata	DFE201612PD	150	5.2	6.2	12	2.0 × 1.6 × 1.2
Murata	DFE252010F	330 to 680	5.6 to 4.1	7.6 to 5.5	16 to 31	2.5 × 2.0 × 1.0
Murata	DFE252012F	330 to 680	6.0 to 4.6	8.5 to 6.0	14 to 25	2.5 × 2.0 × 1.2
Vishay	IHHP-0806AB-01	220 to 470	5.3 to 4.2	5.8 to 4.4	13 to 29	2.0 × 1.6 × 1.2
Vishay	IHHP-1008AB-01	220 to 680	7.4 to 3.8	7.1 to 4.1	8.4 to 28	2.5 × 2.0 × 1.2
XFRMS	XFHCL43LT	220 to 470	8.0 to 4.5	7.0 to 3.8	13 to 25 (Max)	2.5 × 2.0 × 1.2
NIC	NPMH0805B	240, 470	4.2, 3.0	4.8, 3.2	25, 48 (Max)	2.0 × 1.2 × 0.8
NIC	NPMH0805C	240 to 470	3.7 to 3.0	4.5 to 3.3	28 to 42 (Max)	2.0 × 1.2 × 1.0
NIC	NPMH0806C	240 to 470	4.7 to 3.5	5.6 to 3.9	23 to 42 (Max)	2.0 × 1.6 × 1.0
NIC	NPIM26LP	240 to 680	6.5 to 4.2	7.5 to 5.1	15 to 36	2.0 × 1.6 × 1.0
NIC	NPIM20LP	240 to 680	6.0 to 4.4	9.5 to 5.5	18 to 32	2.5 × 2.0 × 1.0
Sumida	201610CDMCC/DS	240, 470	5.2, 3.8	6.5, 4.2	19, 34	2.2 × 1.8 × 1.0
Sumida	252010CDMCC/DS	330 to 1000	5.2 to 3.2	6.8 to 3.8	16 to 46	2.7 × 2.2 × 1.0
Wurth Electronik	WE-PMMI-0805LP	110	3	6	24	2.0 × 1.2 × 0.6
Wurth Electronik	WE-PMMI-0806	240 to 470	3.5 to 3.0	4.0 to 3.4	15 to 20	2.0 × 1.6 × 0.6
Wurth Electronik	WE-PMCI-0806	240, 470	3.6, 2.9	5.4, 4.2	19, 34	2.0 × 1.6 × 1.0
Wurth Electronik	WE-PMCI-1008	470	3.3	5	25	2.5 × 2.0 × 1.0
Wurth Electronik	WE-LQS-2512	160	3.7	6.4	16	2.5 × 2.0 × 1.2
TDK	TFM201208BLD	110	6.8	8.8	10	2.0 × 1.2 × 0.8

*Strongly depends on the PCB thermal properties

APPLICATIONS INFORMATION

increase in application footprint. See the layout section for more detail. X7R or X5R capacitors are recommended for best performance across temperature and input voltage variations (see Table 3). Note that larger input capacitance is required when a lower switching frequency is used. If the input power source has high impedance, or there is significant inductance due to long wires or cables, additional bulk capacitance may be necessary. This can be provided with an electrolytic capacitor.

A ceramic input capacitor combined with trace or cable inductance forms a high quality (under damped) tank circuit. If the LTC3307A circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the LTC3307A's voltage rating. This situation is easily avoided (see Application Note AN88).

Table 3. Ceramic Capacitor Manufacturers

VENDOR	URL
AVX	www.avxcorp.com
Murata	www.murata.com
TDK	www.tdk.com
Taiyo Yuden	www.t-yuden.com
Samsung	www.samsungsem.com
Wurth Elektronik	www.we-online.com

Output Capacitor, Output Ripple and Transient Response

The output capacitor has two essential functions. Along with the inductor, it filters the square wave generated by the LTC3307A at the SW pin to produce the DC output. In this role, it determines the output ripple; thus, low impedance at the switching frequency is important. The second function is to store energy in order to satisfy transient loads and stabilize the LTC3307A's control loop. The LTC3307A is internally compensated and has been designed to operate at a high bandwidth for fast transient response capability. The selection of C_{OUT} affects the bandwidth of the system, but the transient response is also affected by V_{OUT}, V_{IN}, f_{SW} and other factors. A good place to start is with the output capacitance approximately value given by Equation 8.

$$C_{OUT} = 20 \bullet \frac{I_{MAX}}{f_{SW}} \sqrt{\frac{0.5}{V_{OUT}}} \qquad (8)$$

Note: Multiply by 2x for the LTC3307A-1.

where C_{OUT} is the recommended output capacitor value in µF, f_{SW} is the switching frequency in MHz, I_{MAX} = 3A is the rated output current in Amps, and V_{OUT} is in Volts.

A lower value output capacitor saves space and cost but transient performance will suffer and loop stability must be verified. The LTC3307A-1 requires 2x the minimum capacitance indicated by Equation 8.

Ceramic capacitors have very low equivalent series resistance (ESR) and provide the best output ripple and transient performance. Use X5R or X7R ceramic capacitors (see Table 3). Even better output ripple and transient performance can be achieved by using low-ESL reverse geometry or three-terminal ceramic capacitors.

During a load step, the output capacitor must instantaneously supply the current to support the load until the feedback loop increases the switch current enough to support the load. The time required for the feedback loop to respond is dependent on the compensation components and the output capacitor size. Typically, 3 to 4 cycles are required to respond to a load step, but only in the first cycle does the output drop linearly. Although affected by V_{OUT}, V_{IN}, f_{SW}, $t_{ON(MIN)}$, the equivalent series inductance (ESL) of the output capacitor, and other factors, the output droop, V_{DROOP}, is usually about 3 times the linear drop of the first cycle given by Equation 9.

$$V_{DROOP} = \frac{3 \bullet \Delta I_{OUT}}{C_{OUT} \bullet f_{SW}} \qquad (9)$$

where ΔI_{OUT} is the load step.

Transient performance and control loop stability can be improved with a higher C_{OUT} and/or the addition of a feedforward capacitor C_{FF} placed between V_{OUT} and FB. Capacitor C_{FF} provides phase lead compensation by creating a high frequency zero which improves the phase margin and the high-frequency response. The values used in the typical application circuits are a good starting point. LTpowerCAD® is a useful tool to help optimize C_{FF} and C_{OUT} for a desired transient performance.

Applying a load transient and monitoring the response of the system or using a network analyzer to measure the actual loop response are two ways to experimentally verify

APPLICATIONS INFORMATION

transient performance and control loop stability, and to optimize C_{FF} and C_{OUT}.

When using the load transient response method to stabilize the control loop apply an output current pulse of 20% to 100% of full load current having a very fast rise time. This will produce a transient on the output voltage. Monitor V_{OUT} for overshoot or ringing that might indicate a stability problem (see Application Note AN149).

Output Voltage Sensing

The LTC3307A's AGND pin is the ground reference for the internal analog circuitry, including the bandgap voltage reference. To achieve good load regulation connect the AGND pin to the negative terminal of the output capacitor (C_{OUT}) at the load. Any drop in the high current power ground return path will be compensated. The AGND node carries very little current and, therefore, can be a minimal size trace. Place a small analog bypass 0201 or 0402 ceramic capacitor as close as possible to the LTC3307A directly on the traces leading from V_{IN} (Pin 3, B1) and AGND pin. All of the signal components, such as the FB resistor dividers and the R_T resistor, should be referenced to the AGND node. See the example PCB Layout for more information.

Enable Threshold Programming

The LTC3307A has a precision threshold enable pin to enable or disable the switching. When forced low, the device enters a low current shutdown mode.

The rising threshold of the EN comparator is 400mV, with 50mV of hysteresis. The EN pin can be tied to V_{IN} if the shutdown feature is not used. Adding a resistor divider from V_{IN} to EN programs the LTC3307A to regulate the output only when V_{IN} is above a desired voltage (see Figure 2). Typically, this threshold, $V_{IN(EN)}$, is used in situations where the input supply is current limited, or has a relatively high source resistance. A switching regulator draws near constant power from its input source, so source current increases as source voltage drops. This looks like a negative resistance load to the source and can cause the source to current limit or latch low under low source voltage conditions. The $V_{IN(EN)}$ threshold prevents the regulator from operating at source voltages where problems may occur. This threshold can be adjusted by setting the values R1 and R2 such that they satisfy Equation 10.

$$V_{IN(EN)} = \left(\frac{R1}{R2} + 1\right) \bullet 400mV \qquad (10)$$

as shown in Figure 2:

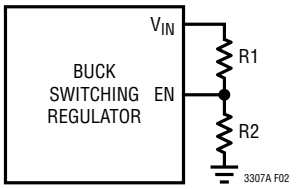


Figure 2. EN Divider

The LTC3307A will remain off until V_{IN} is above $V_{IN(EN)}$. The buck regulator will remain enabled until V_{IN} falls to $0.875 \bullet V_{IN(EN)}$ and EN is 350mV typical.

Alternatively, a resistor divider from an output of an upstream regulator to the EN pin of the LTC3307A provides event-based power-up sequencing, enabling the LTC3307A when the output of the upstream regulator reaches a predetermined level (e.g. 90% of the regulated output). Replace $V_{IN(EN)}$ in Equation 10 with that predetermined level.

Low EMI PCB Layout

The LTC3307A is specifically designed to minimize EMI/EMC emissions and also to maximize efficiency and improve transient response when switching at high frequencies.

Reference the layout design files for the demo board for both the LQFN and WLCSP packages on the LTC3307A product page on the ADI website to see the optimal PCB layout. See Figure 3 for a recommended PCB layout.

For optimal performance the LTC3307A requires that both input supply V_{IN} pins (Pins 3, 8/Pins B1, B4) each have a local decoupling capacitor with their ground terminals soldered directly to the ground plane on the top layer near PGND pins (Pins 4, 7/Pins C1, C4, D1, D4). These

APPLICATIONS INFORMATION

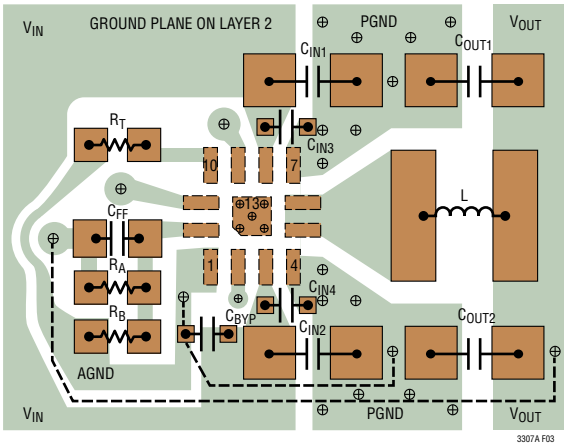
capacitors provide the AC current to the internal power MOSFETs and their drivers. Large, switched currents flow in the V_{IN} and PGND pins and the input capacitors. The loops formed by the input capacitors should be as small as possible by placing the capacitors adjacent to the V_{IN} and PGND pins. Capacitors with small case size such as 0603 are optimal due to lowest parasitic inductance. Even smaller 0201 capacitors can additionally be placed right next to the respective V_{IN} and PGND pins for better performance with minimal (if at all) increase in application footprint. In addition, place a local, unbroken ground plane under the application circuit on the layer closest to the surface layer.

Decoupling AGND is also very important. Place a small analog bypass 0201 or 0402 capacitor as close as possible to the LTC3307A directly on the traces leading from V_{IN} (Pin 3/Pin B1) and AGND (Pin 1/Pin A2).

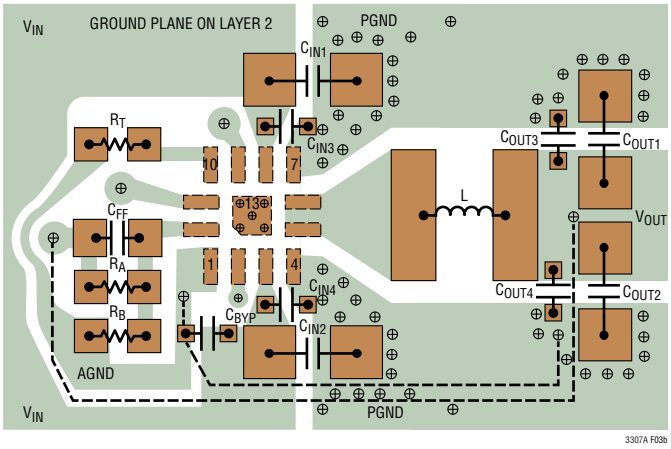
Place the inductor on the same side of the circuit board. The trace connecting SW pins (Pins 5, 6/Pins C2, C3, D2, D3) to the inductor should be as short as possible to reduce radiated EMI and parasitic coupling.

Keep the FB and RT nodes small and far away or shielded from the noisy SW node.

On the LQFN package, five 5mil vias are used to provide the best conductivity to the GND plane within the EPAD. For layouts where 5mil vias are not allowed, it is recommended to use either four 8mil vias or a single (filled or tented) 12mil diameter via. Refer to the Thermal Via Design section of the Analog Devices Application Note, Application Notes for Thermally Enhanced Leaded Plastic Packages for more information on thermal via recommendations.



(a) Small Solution Size. On the LQFN Package, Five 5mil Vias Are Used within the EPAD. For Layouts Where 5mil Vias Are Not Allowed, It Is Recommended to Use Either Four 8mil Vias or a Single (Filled or Tented) 12mil Diameter Via.



(b) With Capacitors C_{OUT1} and C_{OUT2} Rotated by 90°, Which Reduces High Frequency Output Ripple. Optional 0201 Capacitors C_{OUT3} and C_{OUT4} Further Improve the High Frequency Output Ripple. On the LQFN Package, Five 5mil Vias Are Used within the EPAD. For Layouts Where 5mil Vias Are Not Allowed, It Is Recommended to Use Either Four 8mil Vias or a Single (Filled or Tented) 12mil Diameter Via.

Figure 3. Recommended PCB Layout for the LTC3307A LQFN Package

APPLICATIONS INFORMATION

High Temperature Considerations

Care should be taken in the layout of the PCB to ensure good heat sinking of the LTC3307A. On the LQFN package, connect the exposed pad on the bottom of the package (Pin 13) to a large, unbroken ground plane under the application circuit on the layer closest to the surface layer. Place many vias to minimize thermal and electrical impedance. Solder the PGND pins (Pins 4, 7/Pins C1, C4, D1, D4) directly to a ground plane on the top layer. Connect the top layer ground plane to ground plane(s) on lower levels with many thermal vias. These layers will spread heat dissipated by the LTC3307A. Figure 4 is a simplified thermal representation of a thermally enhanced LQFN package with exposed pad, with the silicon die and thermal metrics identified. A simplified thermal representation of a WLCSP package is very similar, with $\theta_{JCBOTTOM}$ representing the thermal conductivity of the Pins and redistribution layer instead of the LQFN substrate. The current source represents power loss P_D on the die; node voltages represent temperatures; electrical impedances represent conductive thermal impedances $\theta_{JCBOTTOM}$, θ_{JCTOP}, θ_{VIA}, θ_{CB}, and convective thermal impedances θ_{BA} and θ_{CA}. The junction temperature, T_J, is calculated from the ambient temperature, T_A, as:

$$T_J = T_A + P_D \bullet \theta_{JA} \quad (11)$$

where, neglecting the $\theta_{JCTOP} + \theta_{CA}$ path:

$$\theta_{JA} \approx \theta_{JCBOTTOM} + \left(\frac{\theta_{CB}+\theta_{BA}}{2}\right) \| \left(\frac{\theta_{CB}+\theta_{BA}}{2} + \theta_{VIA}\right) \quad (12)$$

where $\theta_{JCBOTTOM}$ = 8.6°C/W. The value of θ_{JA} = 51°C/W reported in the Pin Configuration section corresponds to JEDEC standard 2S2P test PCB, which does not have good thermal vias, i.e., θ_{VIA} is relatively high. Assuming, somewhat arbitrarily but not unreasonably, that $\theta_{VIA} \sim (\theta_{CB} + \theta_{BA})/2$, we back calculate $(\theta_{CB} + \theta_{BA})/2 = \theta_{VIA} \approx 60$°C/W for such a board. The importance of thermal vias becomes clear once we observe that if the test PCB had low-thermal-resistance vias, the θ_{JA} would have been reduced by up to 10°C/W, which is an improvement of up to 20%. Similarly, having more ground planes that are larger, uninterrupted and higher-copper-weight improves $\theta_{CB} + \theta_{BA}$, which has a dominant effect on θ_{JA}, given the low value of $\theta_{JCBOTTOM}$ of the package. See the Application Note, Application Notes for Thermally Enhanced Leaded Plastic Packages, for the proper size and layout of the thermal vias and solder stencils. The maximum load current should be derated as the ambient temperature approaches the maximum junction rating. Power dissipation within the LTC3307A is estimated by calculating the total power loss from an efficiency measurement and subtracting the inductor loss.

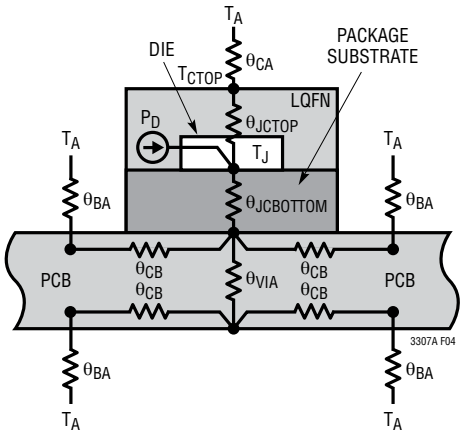
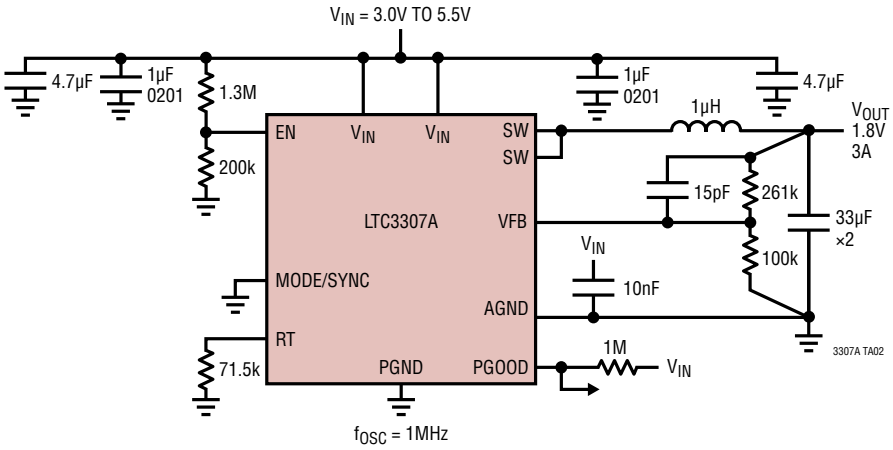


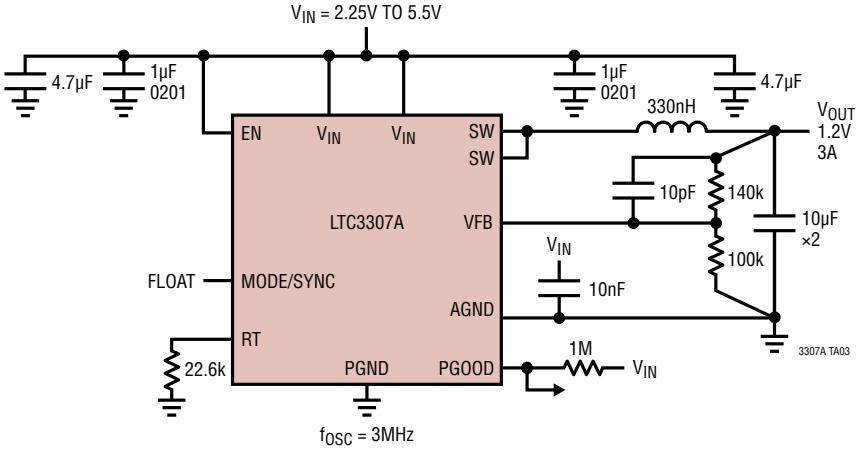
Figure 4. Multi-Layer PCB with Thermal Vias Acts as a Heat Sink

TYPICAL APPLICATIONS

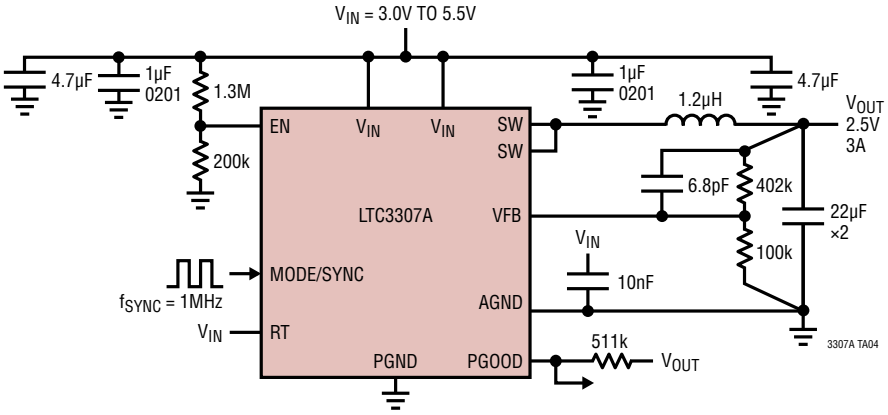
V_{IN} UVLO 3.0V, 1MHz, 1.8V, 3A, Pulse-Skipping Mode



Small Solution Size, 3MHz, 1.2V, 3A, Forced Continuous Mode

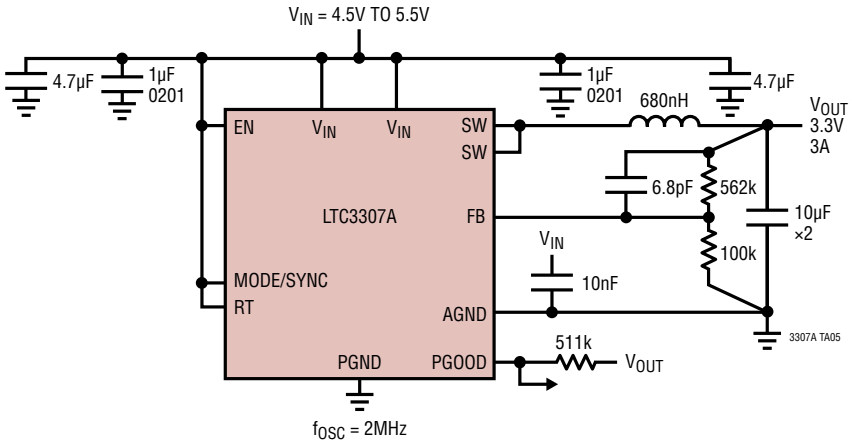


V_{IN} UVLO 3.0V, 2.5V, 3A, Syncing to 1MHz, Forced Continuous Mode

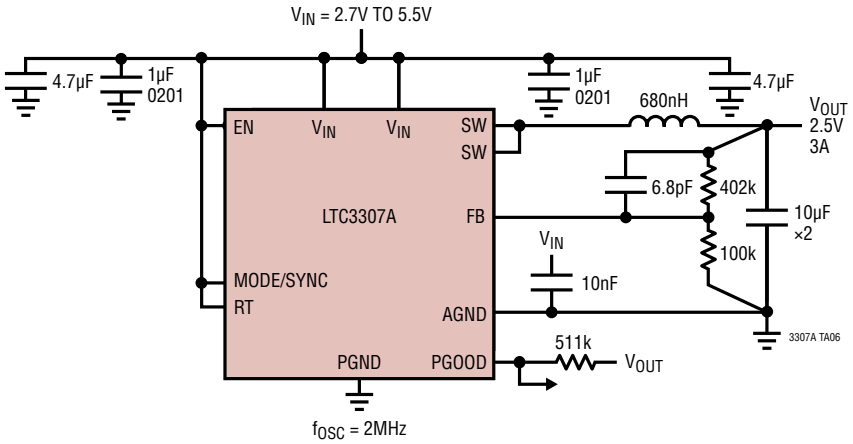


TYPICAL APPLICATIONS

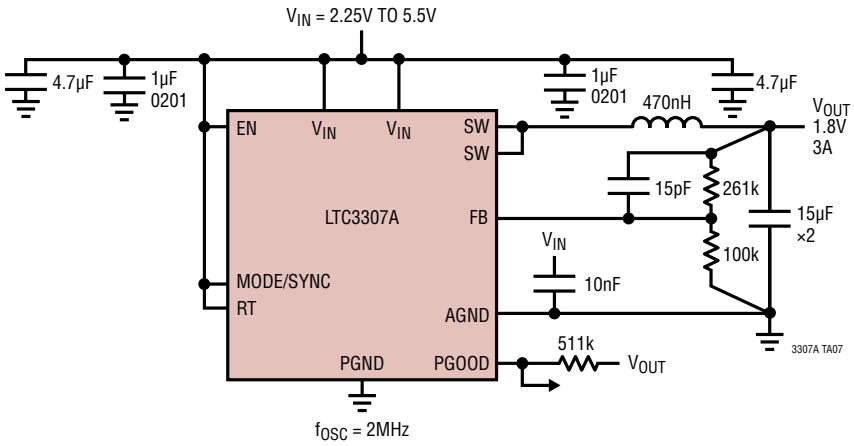
High Efficiency, 2MHz, 3A, 5V to 3.3V, Burst Mode Operation



High Efficiency, 2MHz, 3A, 2.5V, Burst Mode Operation

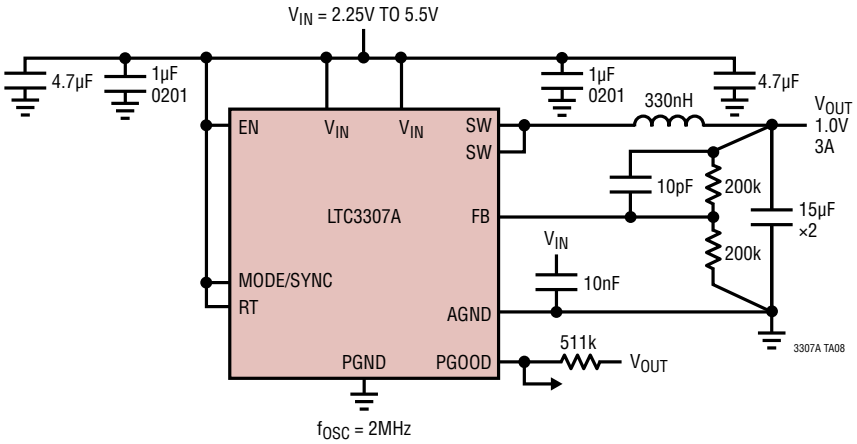


High Efficiency, 2MHz, 3A, 1.8V, Burst Mode Operation

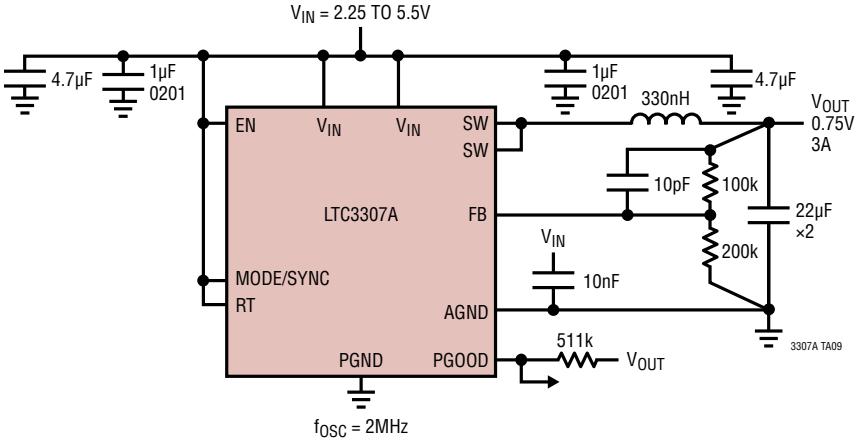


TYPICAL APPLICATIONS

High Efficiency, 2MHz, 3A, 1.0V, Burst Mode Operation

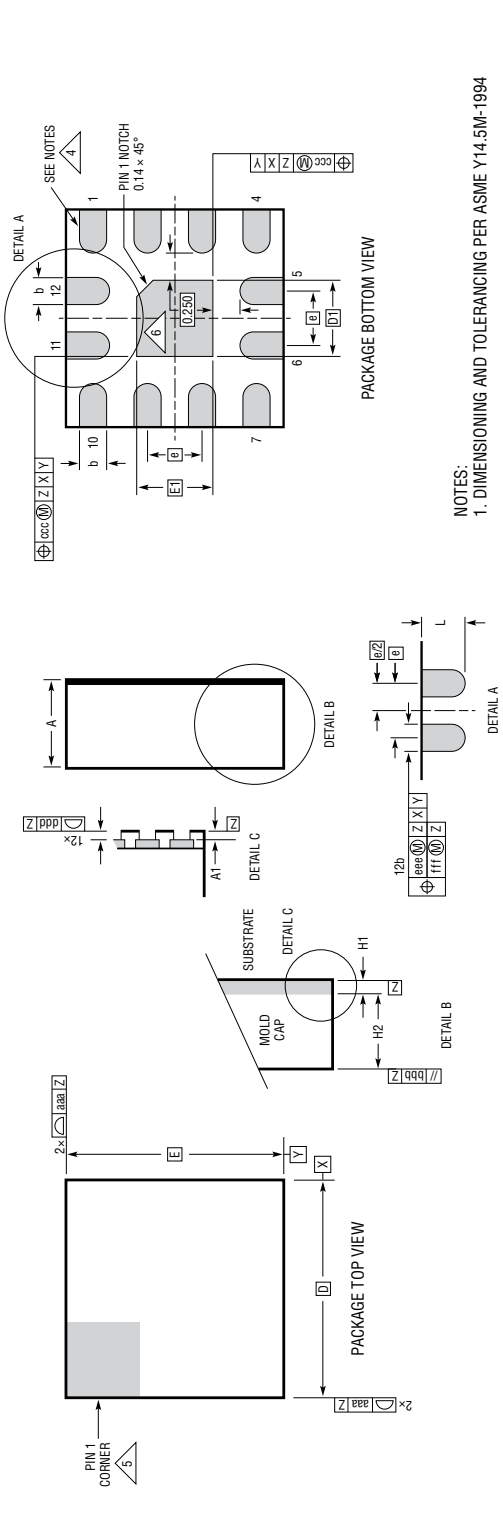


High Efficiency, 2MHz, 3A, 0.75V, Burst Mode Operation



PACKAGE DESCRIPTION

LQFN Package
12-Lead (2mm × 2mm × 0.74mm)
(Reference LTC DWG # 05-08-1530 Rev C)

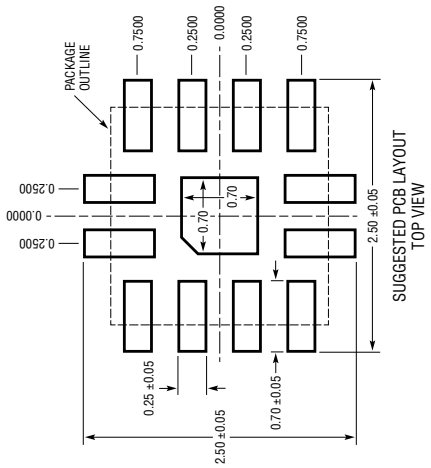


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. PRIMARY DATUM -Z- IS SEATING PLANE
4. METAL FEATURES UNDER THE SOLDER MASK OPENING NOT SHOWN SO AS NOT TO OBSCURE THESE TERMINALS AND HEAT FEATURES
5. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN 1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
6. THE EXPOSED HEAT FEATURE MAY HAVE OPTIONAL CORNER RADII

LQFN 12 0721 REV C

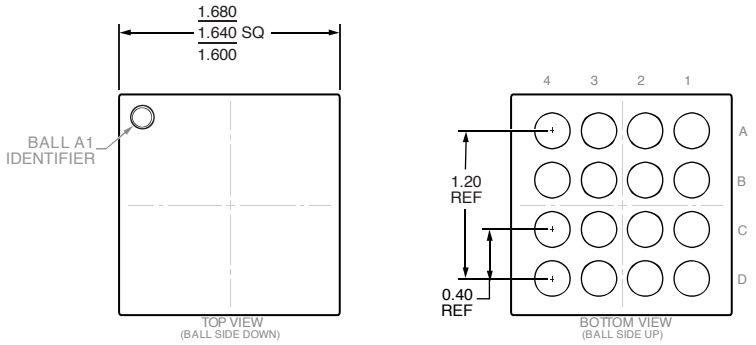
DIMENSIONS

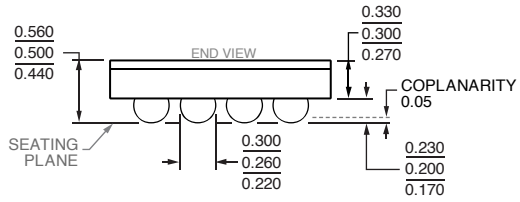
SYMBOL	MIN	NOM	MAX	NOTES
A	0.65	0.74	0.83	
A1			0.03	
L	0.30	0.40	0.50	
b	0.22	0.25	0.28	
D		2.00		
E		2.00		
D1		0.70		
E1		0.70		
e		0.50		
H1		0.24 REF		SUBSTRATE THK
H2		0.50 REF		MOLD CAP HT
aaa			0.10	
bbb			0.10	
ccc			0.10	
ddd			0.10	
eee			0.15	
fff			0.08	



PACKAGE DESCRIPTION

WLCSP PACKAGE
CB-16-11
16-Pin (1.64mm × 1.64mm × 0.5mm)





PKG-006569

09-12-2019-B

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	11/19	Added AEC-Q100 Qualified. Added J-Grade and #W Parts. Note 2: Added J-Grade. Table 2: Added Thermal Properties Note. Modified Figure 3 into 3a and 3b. Capacitor App Circuit Changes.	1 2 4 15 18 20-26
B	01/21	Updated Features List. Added “Battery Powered Systems” to Applications List. Corrected Default Conditions for Electrical Characteristics Table. Updated Load and Line Regulation Typical Curves. Corrected PGOOD Upper Threshold Hysteresis Typical Value. Changed Inductor Value Equation to Approximate Value. Updated Recommended Inductor Table. Added Description of Allowable Modifications to Epad Vias. Added Mode of Operation Descriptors to All Typical Applications. Expanded Allowed Input Voltages in Typical Applications. Updated Related Parts Table.	1 1 3 7 12 14 15 18 21, 22, 23, 26 22, 23 26
C	11/22	Added WLCSP Package Option. Updated Typical Switching Waveform In Pulse-Skipping Mode.	1-24 8
D	2/24	Added new part numbers and references for LTC3307A-1. Added new spec for Soft-Start Duration for LTC3307A-1. Added LTC3307A-1 info to descriptors of soft-start waveforms. Added note and comment on Equation 8 for LTC3307A-1.	1, 2, 4 4 8 16
E	6/24	Added Top Switch Current Limit for LTC3307A-1 at room and over temp. Added Bottom Switch Current Limit for LTC3307A-1 at room and over temp.	3 4

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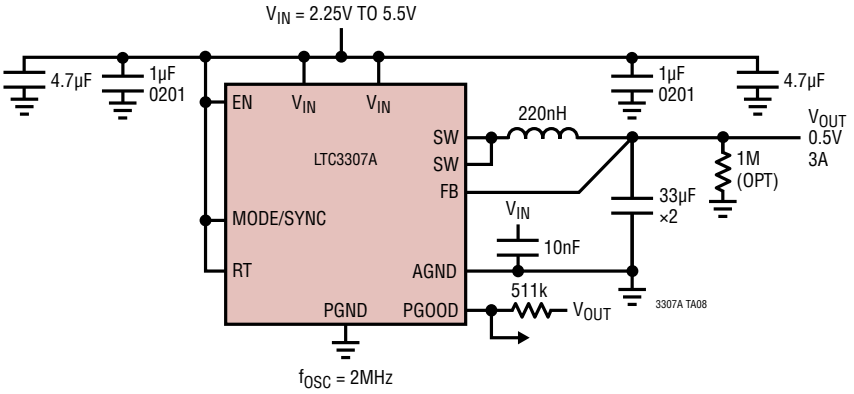
TYPICAL APPLICATION

High Efficiency, 2MHz, 0.5V, 3A, Burst Mode Operation



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3307B	5V, 3A Synchronous Step-Down Silent Switcher in 2mm × 2mm LQFN	Monolithic Synchronous Step-Down DC/DC Capable of Supplying 3A at Switching Frequencies Up to 10MHz; Silent Switcher Architecture for Ultralow EMI Emissions; 2.25V to 5.5V Input Operating Range; 0.5V to V_{IN} Output Voltage Range with ±1% Accuracy; PGOOD Indication, RT Programming, SYNC Input; 2mm × 2mm LQFN
LTC3308A/ LTC3308B	5V, 4A Synchronous Step-Down Silent Switcher in 2mm × 2mm LQFN	Monolithic Synchronous Step-Down DC/DC Capable of Supplying 4A at Switching Frequencies Up to 3MHz/10MHz; Silent Switcher Architecture for Ultralow EMI Emissions; 2.25V to 5.5V Input Operating Range; 0.5V to V_{IN} Output Voltage Range with ±1% Accuracy; PGOOD Indication, RT Programming, SYNC Input; 2mm × 2mm LQFN
LTC3309A/ LTC3309B	5V, 6A Synchronous Step-Down Silent Switcher in 2mm × 2mm LQFN	Monolithic Synchronous Step-Down DC/DC Capable of Supplying 6A at Switching Frequencies Up to 3MHz/10MHz; Silent Switcher Architecture for Ultralow EMI Emissions; 2.25V to 5.5V Input Operating Range; 0.5V to V_{IN} Output Voltage Range with ±1% Accuracy; PGOOD Indication, RT Programming, SYNC Input; 2mm × 2mm LQFN
LTC3315A/ LTC3315B	Dual 5V, 2A Synchronous Step-Down DC/DCs in 2mm × 2mm LQFN	Dual Monolithic Synchronous Step-Down Voltage Regulators each Capable of Supplying 2A at Switching Frequencies Up to 3MHz/10MHz; 2.25V to 5.5V Input Operating Range; 0.5V to V_{IN} Output Voltage Range with ±1% Accuracy; PGOOD Indication, SYNC Input; 2mm × 2mm LQFN
LTC3310/ LTC3310S LTC3311/ LTC3311S	5V, 10A/12.5A Synchronous Step-Down Silent Switcher/Silent Switcher 2 in 3mm × 3mm LQFN	Monolithic Synchronous Step-Down DC/DC Capable of Supplying 10A/12.5A at Switching Frequencies Up to 5MHz; Silent Switcher Architecture for Ultralow EMI Emissions; 2.25V to 5.5V Input Operating Range; 0.5V to V_{IN} Output Voltage Range with ±1% Accuracy; PGOOD Indication, RT Programming, SYNC Input; Configurable for Paralleling Power Stages; 3mm × 3mm LQFN
LTC3370/ LTC3371	4-Channel 8A Configurable 1A Buck DC/DCs	Four Synchronous Buck Regulators with 8 × 1A Power Stages; Can Connect Up to Four Power Stages in Parallel to Make a High Current Output (4A Maximum) with a Single Inductor, 8 Output Configurations Possible, Precision PGOOD Indication; LTC3371 Has a Watchdog Timer; LTC3370: 32-Lead 5mm × 5mm QFN; LTC3371: 38-Lead 5mm × 7mm QFN and TSSOP
LTC3374A	8-Channel Parallelable 1A Buck DC/DCs	Eight 1A Synchronous Buck Regulators; Can Connect Up to Four Power Stages in Parallel to Make a High Current Output (4A Maximum) with a Single Inductor, 15 Output Configurations Possible; Precision Enable inputs and PGOOD_ALL reporting; 38-Lead 5mm × 7mm QFN and TSSOP
LTC3375	8-Channel Parallelable 1A Buck DC/DCs	Eight 1A Synchronous Buck Regulators; Can Connect Up to Four Power Stages in Parallel to Make a High Current Output (4A Maximum) with a Single Inductor, 15 Output Configurations Possible; Precision Enable Inputs and PGOOD_ALL Reporting; I^2C Programming with a Watchdog Timer and Pushbutton; 48-Lead 7mm × 7mm QFN
LTC3616	5.5V, 6A, 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.25 to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 75µA, I_{SD} < 1µA, 3mm × 5mm QFN-24 Package
LTC3412A	3A, 4MHz, Monolithic Synchronous Step-Down Regulator	95% Efficiency, V_{IN}: 2.25 to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 64µA, I_{SD} < 1µA, 4mm × 4mm QFN-16 Package

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