Low V_{IN}, High Efficiency, Dual 2A Step-Down DC/DC µModule Regulator

FEATURES

- **Tiny Surface Mount, Low Profile 3mm × 4mm × 1.18mm LGA Package and 3mm × 4mm × 1.48mm BGA Package**
- Input Voltage Range: 2.25V to 3.6V
- Dual 2A DC Output Current
- ±1.5% Total Output Voltage Regulation
- Current Mode Control, Fast Transient Response
- External Frequency Synchronization
- 180° Out-of-Phase Operation
- Selectable Pulse-Skipping Mode/Burst Mode® Operation/Forced Continuous Mode
- Power Good Indicator
- Internal Soft-Start
- Internal Compensation
- Overvoltage, Overcurrent and Overtemperature Protection

APPLICATIONS

- Telecom, Networking and Industrial Equipment
- Point-of-Load Regulation
- FPGA, ASIC Core Supplies

DESCRIPTION

The LTM®4691 is a complete dual 2A output switching mode DC/DC power supply in a tiny 3mm × 4mm × 1.18mm LGA package and a 3mm × 4mm × 1.48mm BGA package. Included in the package are the switching controller, power FETs, inductors and all supporting components. Operating over an input voltage range of 2.25V to 3.6V, the LTM4691 supports two outputs with programmable output voltage range from 0.5V to 2.5V set by external resistors. Its high efficiency design delivers up to 2A continuous current on each output. Only bulk input and output capacitors are needed.

The LTM4691 operates in forced continuous mode for low noise pulse-skipping mode or Burst Mode operation for high efficiency at lights loads. The typical buck switching frequency is 2MHz and can be synchronized from 1MHz to 3MHz. Its high switching frequency and a current mode architecture enables a very fast transient response to line and load changes without sacrificing stability.

Other features include precision run thresholds, a PGOOD signal, output overvoltage protection, thermal shutdown and output short-circuit protection. The LTM4691 is Pb-free and RoHS compliant.

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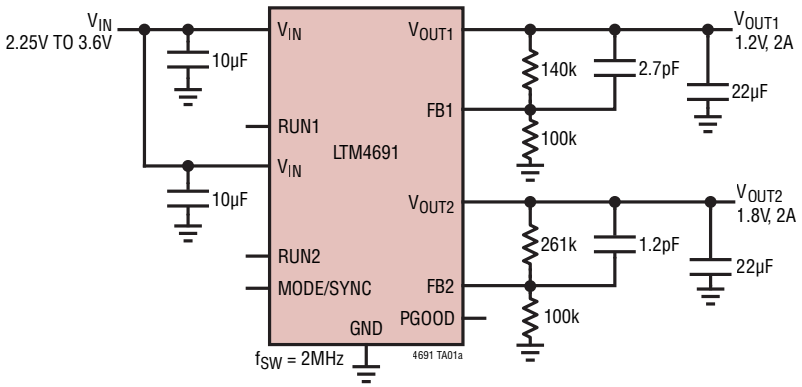
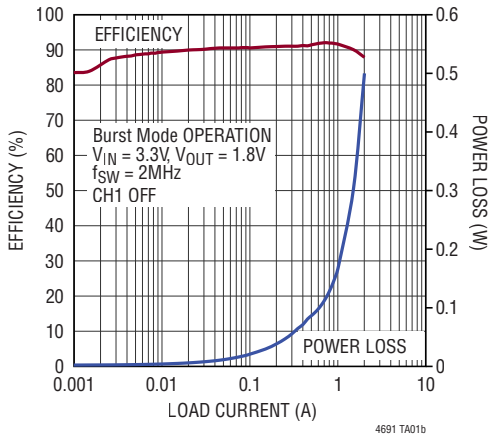
TYPICAL APPLICATION

Dual 2A DC/DC µModule Regulator



Efficiency vs Load Current



Rev. A

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ABSOLUTE MAXIMUM RATINGS

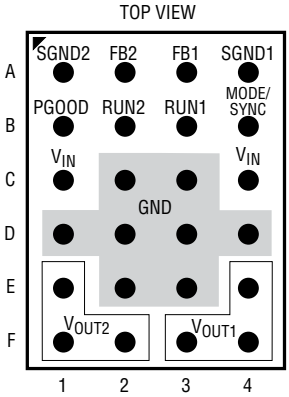
(Note 1)

V_{IN} ..... –0.3V to 4V
V_{OUT1}, V_{OUT2} ..... –0.3V to 2.5V
PGOOD, RUN1, RUN2, MODE/SYNC,
FB1, FB2 ..... –0.3V to 4V

PIN CONFIGURATION

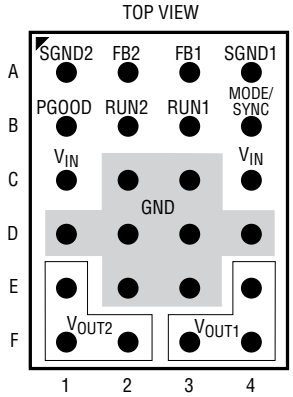
(See Pin Functions, Pin Configuration Table)

Operating Junction Temperature
(Note 2) ..... –40°C to 125°C
Storage Temperature Range ..... –55°C to 125°C
Peak Solder Reflow Body Temperature ..... 260°C



LGA PACKAGE
24-LEAD (3mm × 4mm × 1.18mm) LGA PACKAGE
T_{JMAX} = 125°C, θ_{JA} = 40.4°C/W,
θ_{JCtop} = 47.9°C/W, θ_{JCbot} = 8.5°C/W
WEIGHT = 0.042gram

NOTES:
1. θ VALUES ARE DETERMINED BY SIMULATION PER JESD-51 CONDITIONS.
2. θ_{JA} VALUE IS OBTAINED WITH DEMO BOARD.
3. REFER TO PAGE 17 FOR LAB MEASUREMENT AND DE-RATING INFORMATION.



BGA PACKAGE
24-LEAD (3mm × 4mm × 1.48mm) BGA PACKAGE
T_{JMAX} = 125°C, θ_{JA} = 40°C/W,
θ_{JCtop} = 50°C/W, θ_{JCbot} = 8.5°C/W
WEIGHT = 0.048gram

NOTES:
1. θ VALUES ARE DETERMINED BY SIMULATION PER JESD-51 CONDITIONS.
2. θ_{JA} VALUE IS OBTAINED WITH DEMO BOARD.
3. REFER TO PAGE 17 FOR LAB MEASUREMENT AND DE-RATING INFORMATION.

ORDER INFORMATION

PART NUMBER	PAD OR BALL FINISH	PART MARKING		JDEC FINISH CODE	PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE
		DEVICE	FINISH CODE				
LTM4691EV#PBF	Au (RoHS)	4691V	v	e4	LGA	3	–40°C to 125°C
LTM4691IV#PBF							
LTM4691EY#PBF	SAC305 (RoHS)	4691Y		e1	BGA		
LTM4691IY#PBF							

- Contact the factory for parts specified with wider operating temperature ranges. *Pad or ball finish code is per IPC/JEDEC J-STD-609.
- Recommended LGA and BGA PCB Assembly and Manufacturing Procedures
- LGA and BGA Package and Tray Drawings

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C (Note 2), V_{IN} = 3.3V, per the typical application.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Input DC Voltage		●	2.25		3.6	V
$V_{OUT1,2(RANGE)}$	Output Voltage Range	V_{IN} = 2.25V to 3.6V	●	0.5		2.5	V
$V_{OUT1,2(DC)}$	Output Voltage, Total Variation with Line and Load	MODE/SYNC = Float V_{IN} = 2.5V to 3.6V I_{OUT} = 0A to 2A, V_{IN} = 2.5V	●	1.477	1.50	1.523	V
V_{IN_UVLO}	V_{IN} Undervoltage Lockout	V_{IN} Rising		2.05	2.15	2.25	V
$V_{IN_UVLO_HYS}$	V_{IN} Undervoltage Lockout Hysteresis				150		mV
$V_{RUN1,2}$	RUN Pin On-Threshold	V_{RUN} Rising		0.375	0.4	0.425	V
$V_{RUN1HYS}/V_{RUN2HYS}$	RUN Pin Hysteresis				50		mV
$I_{RUN1,2}$	RUN Pin Leakage Current	RUN = 3.6V				±100	nA
V_{IN} Quiescent Current in Shutdown		V_{IN} = 3.6V, RUN = 0V			1.5		µA
$I_{Q(VIN)}$ with Both Bucks Enabled	Input Supply Bias Current	V_{OUT} = 1.5V, MODE/SYNC = V_{IN} MODE/SYNC = GND MODE/SYNC = FLOAT			85 2.6 32		µA mA mA
$I_{OUT1,2(DC)}$	Output Continuous Current Range	V_{OUT} = 1.5V (Note 3)		0		2	A
$\Delta V_{OUT1(LINE)}/V_{OUT1}$ $\Delta V_{OUT2(LINE)}/V_{OUT2}$	Line Regulation Accuracy	V_{OUT} = 1.5V, V_{IN} = 2.25V to 3.6V, I_{OUT} = 0A	●		0.001	0.5	%/V
$\Delta V_{OUT1(LOAD)}/V_{OUT1}$ $\Delta V_{OUT2(LOAD)}/V_{OUT2}$	Load Regulation Accuracy	V_{OUT} = 1.5V, I_{OUT} = 0A to 2A V_{IN} = 2.5V	●		0.2	1.5	%
$V_{OUT1,2(AC)}$	Output Ripple Voltage	I_{OUT} = 0A, C_{OUT} = 22µF Ceramic V_{IN} = 3.3V, V_{OUT} = 1.5V			5.5		mV
$\Delta V_{OUT(START)}$ (Each Channel)	Turn-On Overshoot	I_{OUT} = 0A, C_{OUT} = 22µF Ceramic V_{IN} = 3.3V, V_{OUT} = 1.5V			12		mV
t_{START} (Each Channel)	Turn-On Time	C_{OUT} = 22µF Ceramic, No Load, V_{IN} = 3.3V, V_{OUT} = 1.5V (Note 4)			1		ms
ΔV_{OUTLS} (Each Channel)	Peak Deviation for Dynamic Load	Load: 0% to 50% to 0% of Full Load C_{OUT} = 100µF Ceramic, V_{IN} = 3.3V, V_{OUT} = 1.5V			55		mV
t_{SETTLE} (Each Channel)	Settling Time for Dynamic Load Step	Load: 0% to 50% to 0% of Full Load C_{OUT} = 100µF Ceramic, V_{IN} = 3.3V, V_{OUT} = 1.5V			25		µs
I_{OUT1PK}, I_{OUT2PK}	Output Current Limit	V_{IN} = 3.3V, V_{OUT} = 1.5V			2.8		A
$V_{FB1,2}$	Voltage at FB Pin	I_{OUT} = 0A, V_{OUT} = 1.5V	●	0.495	0.50	0.505	V
$I_{FB1,2}$	Current at FB Pin					±20	nA
PGOOD Threshold/HYS	PGOOD Rising Threshold PGOOD Hysteresis Overvoltage Rising Threshold Overvoltage Hysteresis	As a Percentage of the Regulated V_{FB}			–2.5 1.1 10 2	–3.5 14 	% % % %
I_{PGOOD}	Internal PGOOD Leakage	V_{PGOOD} = 3.6V				±100	nA
f_{OSC}	Oscillator Frequency				2		MHz
MODE/SYNC Threshold	Programming Pulse-Skipping Mode		●			0.1	V
	Programming Burst Mode Operation		●	V_{IN} – 0.1			V
SYNC_RANGE	SYNC Frequency Range			1		3	MHz
SYNC_LEVEL	Clock Level High on SYNC Clock Level Low on SYNC			1.2		 0.4	V V

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

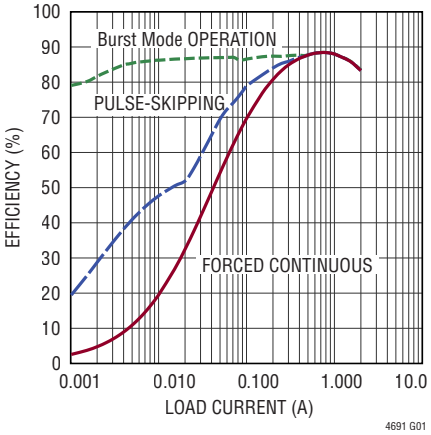
Note 2:. The LTM4691 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTM4691E is guaranteed to meet performance specifications over the 0°C to 125°C internal operating temperature range. Specifications over the full –40°C to 125°C internal operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTM4691I is guaranteed to meet specifications over the full –40°C to 125°C internal operating temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

Note 3: See output current derating curves for different V_{IN}, V_{OUT} and T_A.

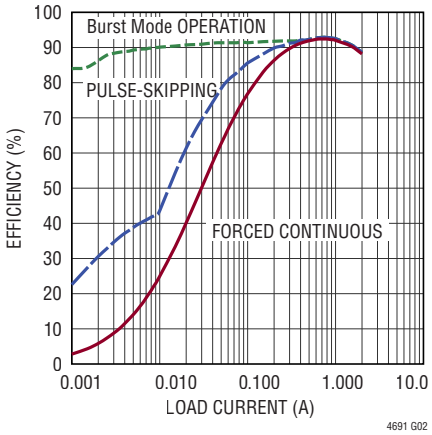
Note 4: Guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

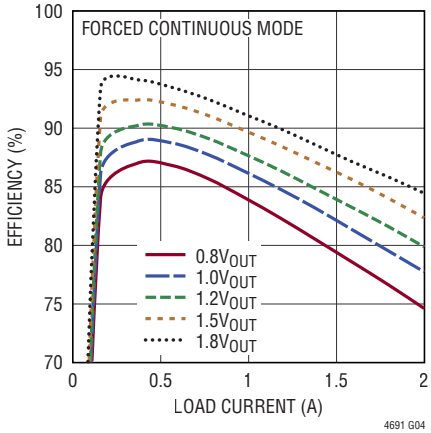
Efficiency vs Load Current at Different Modes of Operation V_{IN} = 3.3V, V_{OUT} = 1.2V



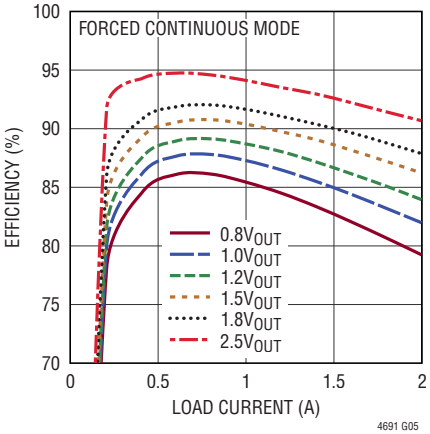
Efficiency vs Load at Different Modes of Operation V_{IN} = 3.3V, V_{OUT} = 1.8V



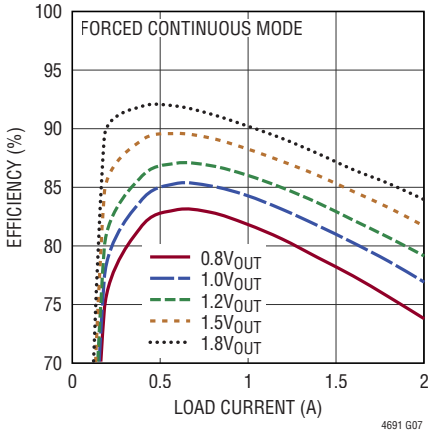
Efficiency vs Load Current at 2.25V_{IN}, Channel 2 off



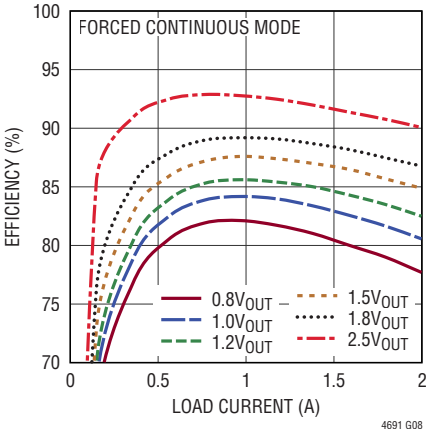
Efficiency vs Load Current at 3.3V_{IN}, Channel 2 off



Efficiency vs Load Current at 2.25V_{IN}, Both Channels On

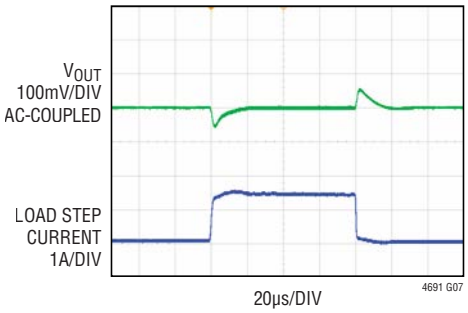


Efficiency vs Load Current at 3.3V_{IN}, Both Channels On



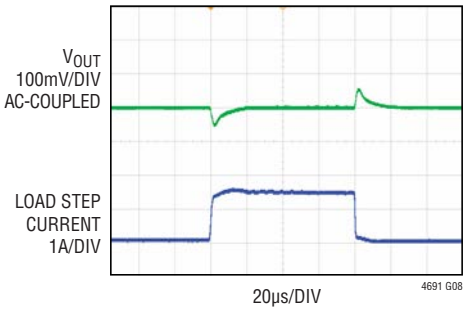
TYPICAL PERFORMANCE CHARACTERISTICS

Transient Response, Pulse-Skipping Mode



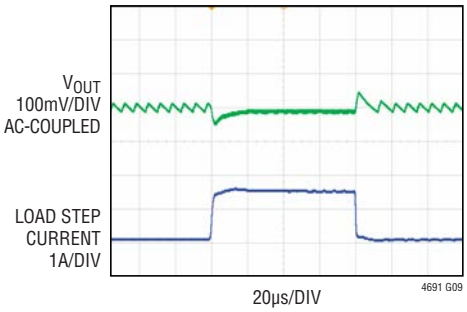
LOAD STEP: 0.1A TO 1.5A
V_{IN} = 3.3V
V_{OUT} = 1.2V

Transient Response, Forced Continuous Mode



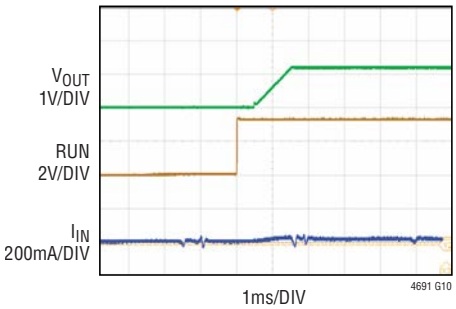
LOAD STEP: 0.1A TO 1.5A
V_{IN} = 3.3V
V_{OUT} = 1.2V

Transient Response, Burst Mode Operation



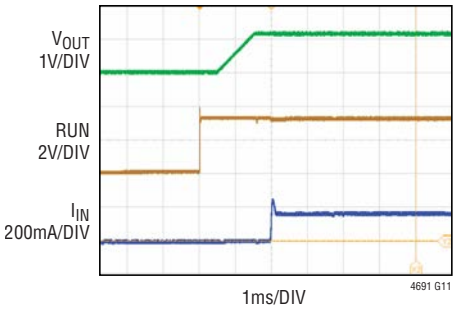
LOAD STEP: 0.1A TO 1.5A
V_{IN} = 3.3V
V_{OUT} = 1.2V

Start-Up Transient, No Load



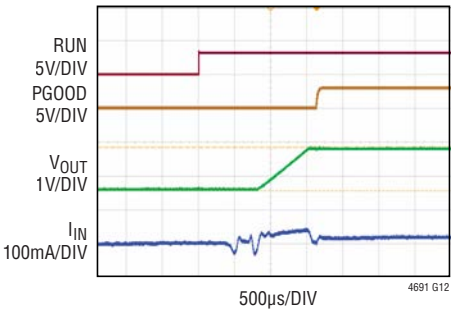
V_{IN} = 3.3V
V_{OUT} = 1.2V

Start-Up Transient, Full Load



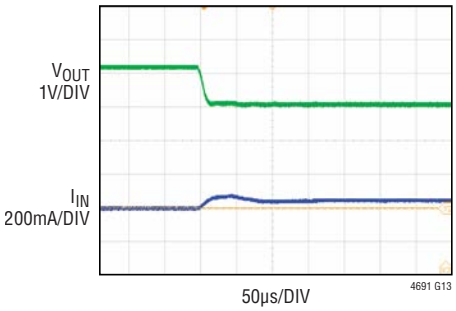
V_{IN} = 3.3V
V_{OUT} = 1.2V
R_{LOAD} = 0.6Ω

Start-Up with Prebiased Output



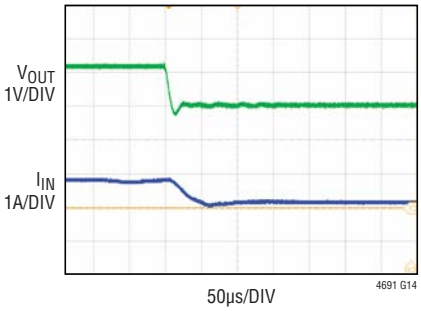
V_{IN} = 3.3V
V_{OUT} = 1.2V

Short-Circuit, No Load



V_{IN} = 3.3V
V_{OUT} = 1.2V

Short-Circuit, Full Load



V_{IN} = 3.3V
V_{OUT} = 1.2V

PIN FUNCTIONS

PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.

V_{IN} (C4, C1): Power Input Pins. Both V_{IN} pins are internally connected and must be connected with a short. Each V_{IN} should have its own input bypass capacitors. Recommend placing input decoupling capacitors as close as possible to the pins.

V_{OUT1} (E4, F3, F4), V_{OUT2} (E1, F1, F2): Power Output Pins of Each Switching Mode Regulator. Apply output load between these pins and GND pins. Recommend placing output decoupling capacitance directly between these pins and GND pins.

GND (C2, C3, D1, D2, D3, D4, E2, E3): Power Ground Pins for Both Input and Output Returns.

SGND1 (A4), SGND2 (A1): Signal Ground Connection

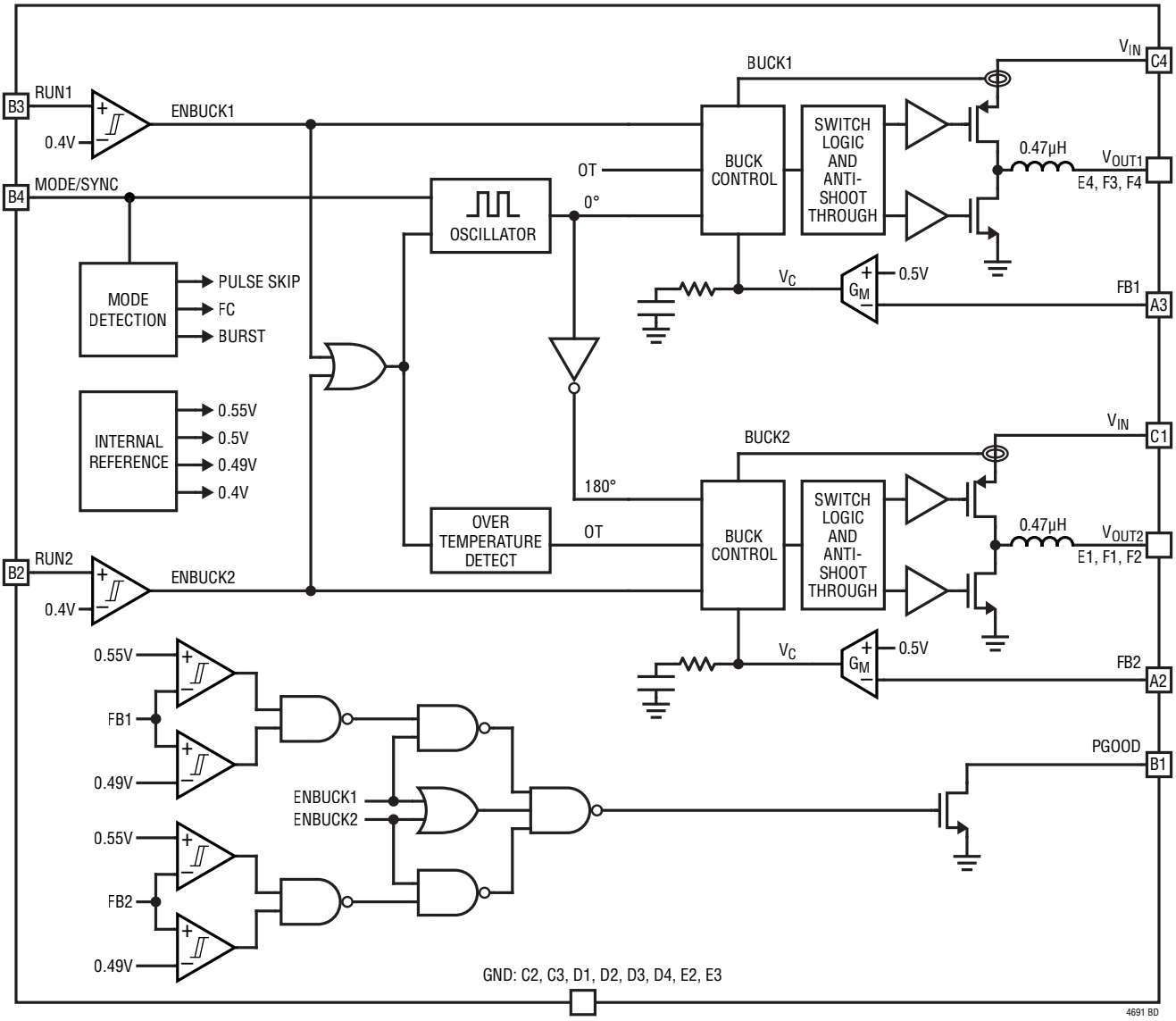
PGOOD (B1): Power Good Output. Open-drain output. When the regulated output voltage of either switching regulator falls below its PGOOD threshold or rises above its overvoltage threshold, this pin is driven low.

RUN1 (B3), RUN2 (B2): Run Control Input of Each Switching Mode Regulator Channel. It has a precision threshold and an optional external resistor divider from V_{IN} or another supply programs when each channel is enabled. If the precision threshold is not required, drive RUN1, RUN2 to V_{IN} to enable. Do Not Float.

FB1 (A3), FB2 (A2): The Negative Input of the Error Amplifier for the switching Mode Regulator Channel. The LTM4691 regulates the voltage between FB and SGND to 500mV. A resistor divider connecting to V_{OUT} sets the output voltage.

MODE/SYNC (B4): Mode Selection and External Clock Synchronization Input. Ground this pin to enable pulse-skipping mode. For higher efficiency at light loads, tie this pin to V_{IN} to enable Burst Mode. For fast transient response and constant frequency operation over a wide load range, float this pin to enable forced continuous mode. Drive MODE/SYNC with an external clock to synchronize both buck converters to the applied frequency. When syncing, the operating mode is forced continuous. The slope compensation is automatically adapted to the external clock frequency. In the absence of an external clock both buck converters will switch at the default switching frequency.

BLOCK DIAGRAM



DECOUPLING REQUIREMENTS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
C_{IN}	External Input Capacitor Requirement (V_{IN} = 2.25V to 3.6V, V_{OUT} = 1.5V)	I_{OUT} = 2A (Each Channel)	10 (For Each Channel)			µF
$C_{OUT1,2}$	External Output Capacitor Requirement (V_{IN} = 2.25V to 3.6V, V_{OUT} = 1.5V)	I_{OUT} = 2A	22			µF

OPERATION

The LTM4691 is a dual standalone non-isolated switching mode DC/DC power supply. Each channel can deliver up to 2A of DC output current with few external input and output capacitors. This module provides precisely regulated output voltage programmable via external resistor divider from 0.5V to 3.6V over 2.5V to 3.6V input voltage range. The typical application schematic is shown on page 1.

The LTM4691 integrates two constant frequency peak current mode regulators, power MOSFETs, inductors, and other supporting discrete components. The typical switching frequency of the LTM4691 is 2MHz, it can be externally synchronized to a clock from 1MHz to 3MHz. See the Applications Information section.

With current mode control and internal feedback loop compensation, the LTM4691 module has sufficient stability margins and good transient performance with minimum output capacitors. Current mode control provides cycle-by-cycle fast current limiting. Peak current limiting is provided in an over-current condition. Each buck switching regulator has its own internal PGOOD signal. If either enabled buck's internal PGOOD signal stays low for greater than 120µs, then the PGOOD pin is pulled low indicating to a microprocessor that a power fault has occurred.

The RUN pins have precision 400mV threshold with 50mV hysteresis. It can be used to provide event-based power up sequencing by connecting the RUN pin to the output of another buck through a resistor divider. If the RUN pin of a buck is low, that buck is shut down and in a low quiescent current state. If both RUN pins are low, both bucks are in shutdown, the SW pins are high impedance, and the quiescent current of the LTM4691 is less than 1µA. If either pin is above the enable threshold of 400mV, its respective buck is enabled.

All buck regulators have forward and reverse-current limiting, soft-start to limit inrush current during start-up, and short-circuit protection. When both bucks are disabled and either back is enabled, there is a 400µs (typical) delay while internal circuitry powers up followed by a 100µs (typical) no start-time before switching commences and the soft-start ramp begins. If a second buck is enabled, it will also have a 100µs (typical) no start-time. If the second buck is enabled within 400µs of the first buck, it will wait until the expiry of the 400µs to begin its no start-time.

The buck switching regulators are 180° out of phase with respect to each other. The phase determines the fixed edge of the switching sequence, which is when the internal top PMOS turns on. The PMOS off (NMOS on) phase is subject to the duty cycle demanded by the regulator.

APPLICATIONS INFORMATION

The typical LTM4691 application circuit is shown on page 1. External component selection is primarily determined by the input voltage, the output voltage and the maximum load current. Refer to Table 4 for specific external capacitor requirements for a particular application.

V_{IN} to V_{OUT} Step-Down Ratios

There are restrictions in the minimum V_{OUT} step-down ratio that can be achieved for a given input voltage due to the minimum on-time limits of the regulator.

The minimum on-time limit imposes a minimum duty cycle of the converter which can be calculated using Equation 1.

$$D_{MIN} = t_{ON(MIN)} \bullet f_{SW} \quad (1)$$

where $t_{ON(MIN)}$ is the minimum on-time, 35ns typical for LTM4691. In rare cases where the minimum duty cycle is surpassed, the output voltage will remain in regulation, but the switching frequency will decrease from its programmed value.

There is no maximum V_{OUT} step-down ratio limitation for the LTM4691. Operating at 100% duty-cycle low dropout, the output voltage of the LTM4691 could be as high as 2.5V.

Output Voltage Programming

The PWM controller has an internal 0.5V reference voltage. Adding a resistor divider from V_{OUT} remote sensing point to FB pin and from FB pin to SGND pin programs the output voltage as shown in Equation 2.

$$V_{OUT} = 0.5V \bullet \frac{R_{TOP} + R_{BOT}}{R_{BOT}} \quad (2)$$

1% resistors are recommended to maintain output voltage accuracy. The buck regulator transient response may improve with an optional phase lead capacitor CFF that helps cancel the pole created by the feedback resistors and the input capacitance of the FB pin (Figure 1).

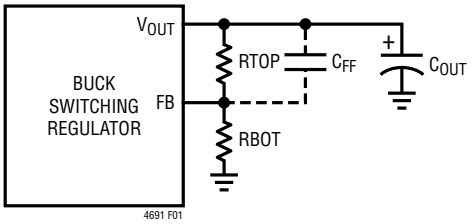


Figure 1. Feedback Components

Input Decoupling Capacitors

The LTM4691 module should be connected to a low AC-impedance DC source. For the regulator, one-piece 10µF input ceramic capacitor near each V_{IN} pin is recommended for RMS ripple current decoupling. Bulk input capacitor is only needed when the input source impedance is compromised by long inductive leads, traces or not enough source capacitance. The bulk capacitor can be an electrolytic aluminum capacitor and polymer capacitor.

Without considering the inductor current ripple, the RMS current of the input capacitor can be estimated as shown in Equation 3.

$$I_{CIN(RMS)} = \frac{I_{OUT(MAX)}}{\eta\%} \bullet \sqrt{D \bullet (1-D)} \quad (3)$$

where $\eta\%$ is the estimated efficiency of the power module.

Output Decoupling Capacitors

With an optimized high frequency, high bandwidth design, only one 22µF low ESR output ceramic capacitor is required for LTM4691 to achieve low output voltage ripple and very good transient response. Additional output filtering may be required by the system designer, if further reduction of output ripples or dynamic transient spikes is required. Table 4 shows a matrix of different output voltages and output capacitors to minimize the voltage droop and overshoot during a 500mA (25%) load step transient.

Mode Selection

The buck switching regulators can operate in three different modes by setting the MODE/SYNC pin: pulse-skipping mode (when the MODE/SYNC pin is set low), forced continuous PWM mode (when the MODE/SYNC pin is floating), and Burst Mode operation (when the MODE/SYNC

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pin is set high). The MODE/SYNC pin sets the operating mode for both buck switching regulators.

In pulse-skipping mode, the oscillator operates continuously and positive SW transitions are aligned to the clock. Negative inductor current is not allowed and during light loads switch pulses are skipped to regulate the output.

In forced continuous mode, the oscillator runs continuously. To maintain regulation, the inductor current is allowed to reverse under light load conditions. This mode allows the buck to run at a fixed frequency with minimal output ripple.

In Burst Mode operation, at light loads, the output capacitor is charged to a voltage slightly higher than its regulation point. The regulator then goes into a sleep state, during which time the output capacitor provides the load current. In sleep, most of the regulator's circuitry is powered down, helping to conserve input power. When the output voltage drops below its programmed value, the circuitry is powered on and another burst cycle begins. The sleep time decreases as load current increases. In Burst Mode operation, the regulator will burst at light loads whereas at higher loads it will operate in constant frequency PWM mode.

Operating Frequency and External Synchronization

The operating frequency of the LTM4691 is optimized to achieve the compact package size and the minimum output ripple voltage while still keeping high efficiency. The default frequency is internally set to 2MHz. If any operating frequency other than 2MHz is required, it can be synchronized to an external clock from 1MHz to 3MHz.

The LTM4691's internal oscillator is synchronized through an internal PLL circuit to an external frequency by applying a square wave clock signal to the MODE/SYNC pin. After detecting an external clock on the SYNC pin, the internal PLL starts up at default frequency, then gradually adjusts its operating frequency to match the frequency of the SYNC signal. During synchronization, the buck 1 PMOS turns on is locked to the rising edge of the external frequency source. Buck 2 will be 180° out of the phase with respect to buck 1. While syncing, the buck switching regulators operate in forced continuous mode.

When the external clock is removed, the LTM4691 will detect the absence of the external clock within approximately 10µs. During this time, it will continue to provide clock cycles. Once the external clock removal has been detected, the oscillator will gradually adjust to its operating frequency back to the default.

Power GOOD

Power failure conditions are reported back via the PGOOD pin. Both buck switching regulators have an internal power good (PGOOD) signal and if a buck is enabled, its internal PGOOD signal must be high for PGOOD pin to be high. When the regulated output voltage of an enabled buck rises above 98% of its programmed value the PGOOD signal transitions high. If the regulated output voltage subsequently falls below 97% of the programmed value the PGOOD signal is pulled low. If either enabled buck's internal PGOOD signal stays low for greater than 120µs, then the PGOOD pin is pulled low, indicating to a microprocessor that a power failure fault has occurred. The 120µs filter time prevents the pin from being pulled low during a load transient. In addition, whenever PGOOD transitions high there will be a 120µs assertion delay.

The LTM4691 also reports overvoltage conditions at the PGOOD pin. If either enabled buck regulators output voltages rises above 110% of the programmed value, the PGOOD pin is pulled low after 120µs. Similarly, if both enabled outputs that are overvoltage subsequently fall below 107.8% of the programmed value, the PGOOD pin transitions high again after 120µs.

PGOOD is also low in the following scenarios: if neither buck switching regulator is enabled, if V_{IN} is below the UVLO threshold, or if the LTM4691 is in overtemperature condition.

Output Overvoltage Protection

During an output overvoltage event, when the FB pin voltage is greater than 110% of its regulated value, the LTM4691 PMOS will be turned off immediately.

An output overvoltage event should not happen under normal operating conditions.

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Output Voltage Soft-Start

Soft-starting the output is needed to prevent current surge on the input supply and output voltage overshoot.

The LTM4691 has internal soft-start, during soft-start, the output voltage will proportionally track an internal voltage ramp. An active pull-down circuit discharges that internal voltage in the case of fault conditions. The ramp will restart when the fault is cleared. Fault conditions that clear the soft-start ramp are the RUN pin goes low, V_{IN} voltage falling too low or thermal shutdown.

Dropout Operation

As the input supply voltage approaches the output voltage, the duty cycle increase toward 100%. Further reduction of the supply voltage forces the PMOS to remain on for more than one cycle, eventually reaching 100% duty cycle. The output voltage will then be determined by the input voltage minus the DC voltage drop across the internal PMOS and the inductor.

Output Short-Circuit Protection and Recovery

The peak inductor current level at which the current comparator shuts off the PMOS is controlled by the error amplifier. When the output current increase, the error amplifier raised the internal V_C voltage until the average inductor current matches the load current. The LTM4691 clamps the maximum internal V_C voltage, thereby limiting the peak inductor current. The LTM4691 can not be paralleled due to the V_C node being internal and not accessible.

When the output is shorted to ground, the inductor current decays very slowly because the voltage across the inductor current is low during the downslope. To keep the inductor current in control a secondary limit is imposed on the valley of the inductor current. If the inductor current measured through the NMOS remains greater than I_{VALLEY} at the end of the cycle, the PMOS will be held off. Subsequent switching cycles will be skipped until the inductor current falls below I_{VALLEY}.

Load Sharing

The LTM4691 is not designed to load share.

Using the Precision RUN Threshold

The LTM4691 has precision threshold RUN pins for each buck regulator to enable or disable each buck. When both are forced low, the device enters into a low current shutdown mode.

The rising threshold of both RUN comparators is 400mV, with 50mV of hysteresis. The RUN pins can be tied to V_{IN} if the shutdown feature is not used. Adding a resistor divider from V_{IN} to a RUN pin to ground programs the LTM4691 to regulate that output only when V_{IN} is above a desired voltage.

Typically, this threshold ($V_{IN(RUN)}$) is used in situations where the input supply is current limited or has a relatively high source resistance. A switching regulator draws near constant power from its input source, so source current increases as source voltage drops. This looks like a negative resistance load to the source and can cause the source to current limit or latch low under low source voltage conditions. The $V_{IN(RUN)}$ threshold prevents the regulator from operating at source voltages where problems may occur. As illustrated in Figure 2, this threshold can be adjusted by setting the values of R1 and R2 such that they satisfy Equation 4.

$$V_{IN(RUN)} = 400mV \bullet \left(1 + \frac{R2}{R1}\right) \quad (4)$$

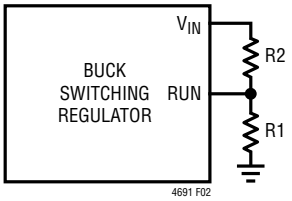

Figure 2. RUN Divider

The buck regulator will remain off until V_{IN} is above $V_{IN(RUN)}$. The buck regulator will remain enabled until V_{IN} falls to 0.875 • $V_{IN(RUN)}$ and RUN is 350mV.

Alternatively, a resistor divider from the output of one buck to the RUN pin of the second buck to ground provides event-based power-up sequencing as the first buck reaching regulation enables the second buck. Replace $V_{IN(RUN)}$ in Equation 4 with the desired output voltage of the first buck (e.g., 90% of the regulated value) at which the second buck is enabled.

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Thermal Considerations and Output Current Derating

To prevent thermal damage, the LTM4691 incorporates an overtemperature (OT) function. If the junction temperature reaches approximately 165°C, both power switches will be turned off resulting in thermal shutdown until the temperature falls to 160°C.

The thermal resistances reported in the Pin Configuration section of the data sheet are consistent with those parameters defined by JESD51-12 and are intended for use with finite element analysis (FEA) software modeling tools that leverage the outcome of thermal modeling, simulation, and correlation to hardware evaluation performed on a µModule® package mounted to a hardware test board. The motivation for providing these thermal coefficients is found in JESD51-12 (“Guidelines for Reporting and Using Electronic Package Thermal Information”).

Many designers may opt to use laboratory equipment and a test vehicle such as the demo board to anticipate the µModule regulator’s thermal performance in their application at various electrical and environmental operating conditions to compliment any FEA activities. Without FEA software, the thermal resistances reported in the Pin Configuration section are in-and-of themselves not relevant to providing guidance of thermal performance; instead, the derating curves provided in the data sheet can be used in a manner that yields insight and guidance pertaining to one’s application-usage, and can be adapted to correlate thermal performance to one’s own application.

The Pin Configuration section typically gives four thermal coefficients explicitly defined in JESD51-12; these coefficients are quoted or paraphrased below:

1. θ_{JA}, the thermal resistance from junction to ambient, is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as “still air” although natural convection causes the air to move. This value is determined with the part mounted.
2. θ_{JCbot}, the thermal resistance from junction to the bottom of the product case, is determined with all of the components power dissipation flowing through the bottom of the package. In the typical µModule regulator, the bulk of the heat flows out the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance value maybe useful for comparing packages, but the test conditions don’t generally match the user’s application.
3. θ_{JCtop}, the thermal resistance from junction to top of the product case, is determined with nearly all of the component power dissipation flowing through the top of the package. As the electrical connections of the typical µModule are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of θ_{JCbot}, this value may be useful for comparing packages but the test conditions don’t generally match the user’s application.

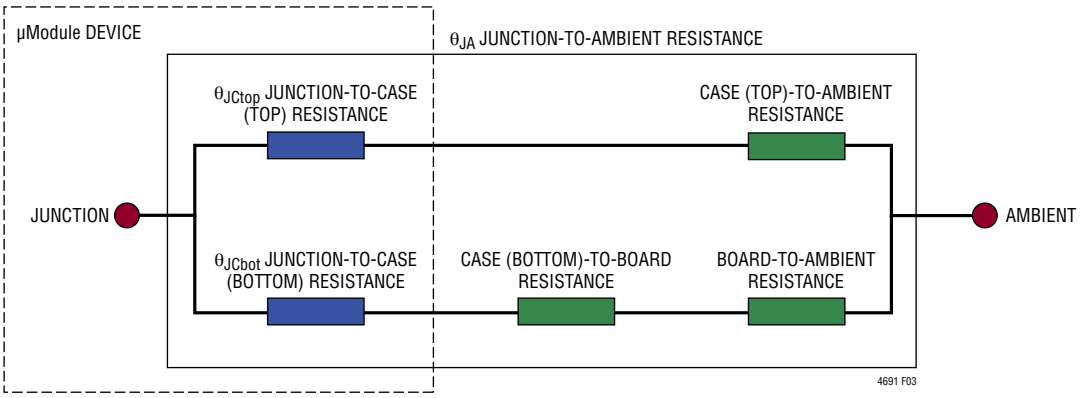

Figure 3. Graphical Representation of JESD51-12 Thermal Coefficients

APPLICATIONS INFORMATION

A graphical representation of the aforementioned thermal resistances is given in Figure 3; blue resistances are contained within the µModule regulator, whereas green resistances are external to the µModule.

As a practical matter, it should be clear to the reader that no individual or sub-group of the four thermal resistance parameters defined by JESD51-12 or provided in the Pin Configuration section replicates or conveys normal operating conditions of a µModule. For example, in normal board-mounted applications, never does 100% of the device's total power loss (heat) thermally conduct exclusively through the top or exclusively through bottom of the µModule—as the standard defines for θ_{JCtop} and $\theta_{JCbottom}$, respectively. In practice, power loss is thermally dissipated in both directions away from the package—granted, in the absence of a heat sink and airflow, a majority of the heat flow is into the board.

Within the LTM4691 module, be aware there are multiple power devices and components dissipating power, with a consequence that the thermal resistances relative to different junctions of components or die are not exactly linear with respect to total package power loss. To reconcile this complication without sacrificing modeling simplicity—but also, not ignoring practical realities—an approach has been taken using FEA software modeling along with laboratory testing in a controlled-environment chamber to reasonably define and correlate the thermal resistance values supplied in this data sheet: (1) Initially, FEA software is used to accurately build the mechanical geometry of the µModule and the specified PCB with all of the correct material coefficients along with accurate power loss source definitions; (2) this model simulates a software-defined JEDEC environment consistent with JSED51-12 to predict power loss heat flow and temperature readings at different interfaces that enable the calculation of the JEDEC-defined thermal resistance values; (3) the model and FEA software is used to evaluate the µModule with heat sink and airflow; (4) having solved for and analyzed these thermal resistance values and simulated various operating conditions in the software model, a thorough laboratory evaluation replicates the simulated conditions with thermocouples within a controlled-environment chamber while operating the device at the same power loss as that which was simulated. An outcome of this process and due-diligence yields a set of derating curves provided in other sections of this data sheet. After these laboratory test have been performed and correlated to the µModule model, then θ_{JA} is shown to correlate quite well with the µModule model with no airflow or heat sinking in a properly defined chamber. This θ_{JA} value is shown in the Pin Configuration section and should accurately equal the θJ_A value because approximately 100% of power loss flows from the junction through the board into ambient with no airflow or top mounted heat sink.

The power loss curves in Figure 4 and Figure 5 can be used in coordination with the load current derating curves in Figure 6 and Figure 7 for calculating an approximate θ_{JA} thermal resistance for the LTM4691 with various heat sinking and airflow conditions. The power loss curves are taken at room temperature, and are increased with multiplicative factors according to the junction temperature. This approximate factor is: 1.15 for 125°C at junction temperature. Maximum load current is achievable while increasing ambient temperature as long as the junction temperature is less than 125°C. When the ambient temperature reaches a point where the junction temperature is 125°C, then the load current is lowered to maintain the junction at 125°C. The derating curves are plotted with the output current starting at 2A per channel and the ambient temperature at 30°C. The output voltages are 1.0V, 1.5V and 2.5V. These are chosen to include the lower and higher output voltage ranges for correlating the thermal resistance. Thermal models are derived from several temperature measurements in a controlled temperature chamber along with thermal modeling analysis. The junction temperatures are monitored while ambient temperature is increased with and without airflow. The power loss increase with ambient temperature change is factored into the derating curves. The junctions are maintained at 125°C maximum while lowering output current or power with increasing ambient temperature. The decreased output current will decrease the internal module loss as ambient temperature is increased. The monitored junction temperature of 125°C minus the ambient operating temperature specifies how much module temperature rise can be allowed.

APPLICATIONS INFORMATION

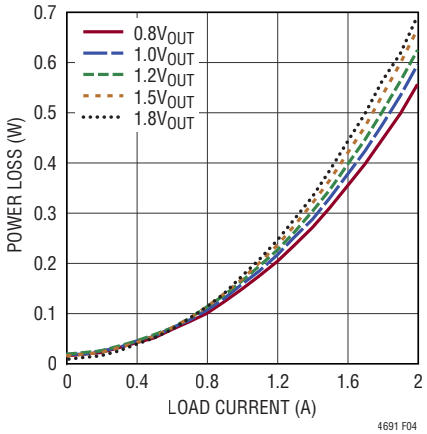

Figure 4. Power Loss at 2.25V_{IN}, Per Channel

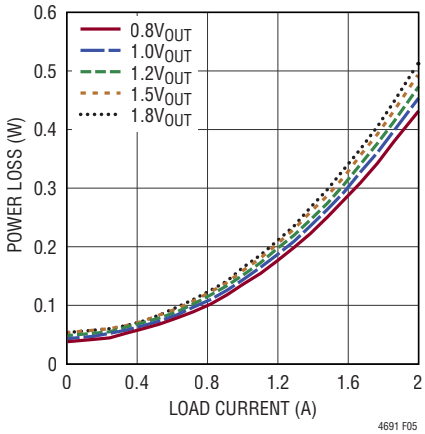

Figure 5. Power Loss at 3.3V_{IN}, Per Channel

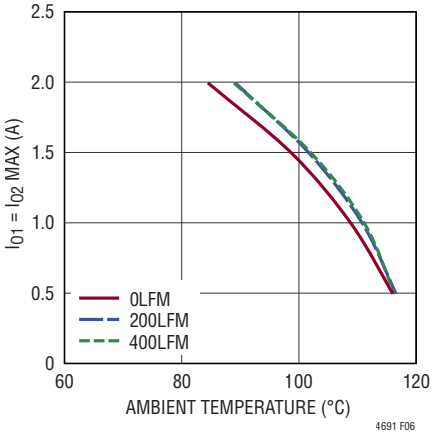

Figure 6. 3.3V_{IN} to 1V_{OUT} Derating Curve, No Heat Sink

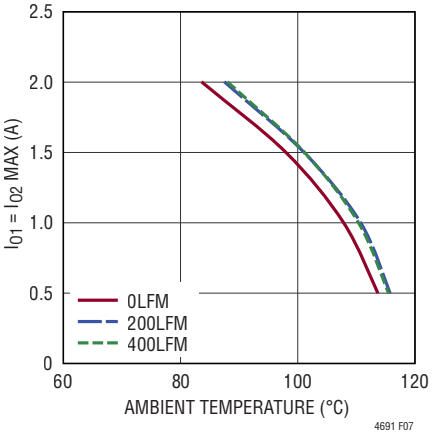

Figure 7. 3.3V_{IN} to 1.5V_{OUT} Derating Curve, No Heat Sink

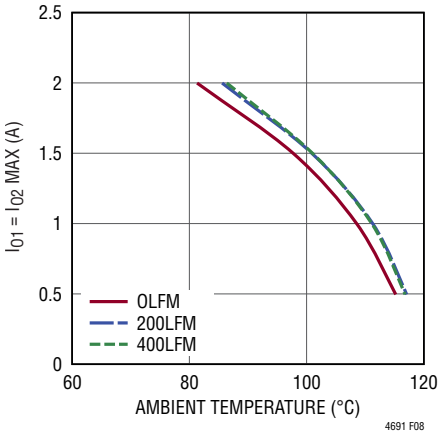

Figure 8. 3.3V_{IN} to 2.5V_{OUT} Derating Curve, No Heat Sink

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As an example, in Figure 6 the ambient temperature is derated to 84.7°C when each channel is running at maximum of 2A of load current with no forced air or heat sink to prevent the junction temperature from exceeding 125°C. For the $3.3V_{IN}$ to $1V_{OUT}$ at 4A the total power loss for both channels is 0.914W, considering the 1.15 multiplying factor the total power loss to be 1.05W. If the 84.7°C ambient temperature is subtracted from the 125°C junction temperature, then the difference of 40.3°C divided by 1.05W equals a 38.4°C/W for θ_{JA} the system equivalent thermal resistance. Table 1 specifies a 40°C/W value which is very close. Table 2 and Table 3 provide equivalent thermal resistances for 1.5V and 2.5V outputs with and without airflow. The derived thermal resistances in Table 1 to Table 3 for the various conditions can be multiplied by the calculated power loss as a function of ambient temperature to derive temperature rise above ambient, thus maximum junction temperature. Room temperature power loss can be derived from the efficiency curves in the Typical Performance Characteristics section and adjusted with the above temperature multiplicative factors. The referenced printed circuit board is a 1.6mm thick four layer board with two ounce copper for the two outer layers and one ounce copper for the two inner layers. The PCB dimensions are 95mm × 76mm.

Safety Considerations

The LTM4691 modules do not provide galvanic isolation from V_{IN} to V_{OUT}. There is no internal fuse. If required, a slow blow fuse with a rating twice the maximum input current needs to be provided to protect each unit from catastrophic failure. The device does support thermal shutdown and over current protection.

Layout Checklist/Example

The high integration of LTM4691 makes the PCB board layout very simple and easy. However, to optimize its electrical and thermal performance, some layout considerations are still necessary.

- Use large PCB copper areas for high current paths, including V_{IN}, GND and V_{OUT}. It helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the V_{IN}, GND and V_{OUT} pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the unit.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.
- Do not put via directly on the pad, unless they are capped or plated over.
- Use a separated SGND ground copper area for components connected to signal pins. Connect the SGND to GND underneath the unit.
- Bring out test points on the signal pins for monitoring.

Figure 9 gives a good example of the recommended layout.

APPLICATIONS INFORMATION

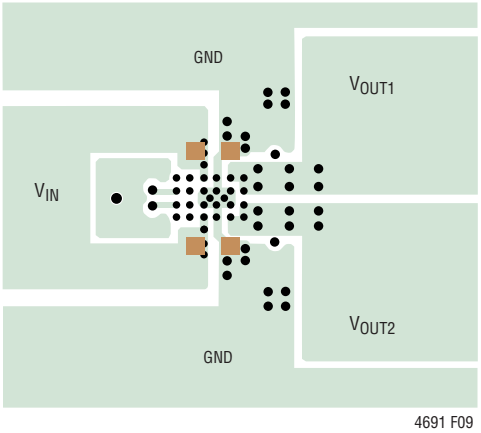


Figure 9. Recommended PCB Layout

Table 1. 1.0V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figure 6	3.3	Figure 5	0	None	40°C
Figure 6	3.3	Figure 5	200	None	35°C
Figure 6	3.3	Figure 5	400	None	34°C

Table 2. 1.5V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figure 7	3.3	Figure 5	0	None	39°C
Figure 7	3.3	Figure 5	200	None	34°C
Figure 7	3.3	Figure 5	400	None	33°C

Table 3. 2.5V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figure 8	3.3	Figure 5	0	None	40°C
Figure 8	3.3	Figure 5	200	None	35°C
Figure 8	3.3	Figure 5	400	None	34°C

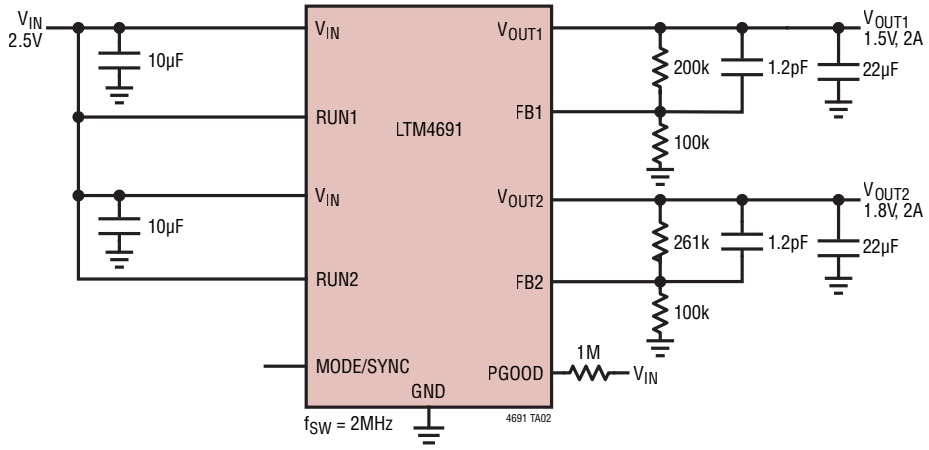
Table 4. Output Voltage Response vs Component Matrix (Refer to Front Page Application) 1A to 1.5A Load Step Typical Measured Values

C_{IN} BULK	VENDORS	PART NUMBER	C_{IN} CERAMIC	VENDORS	PART NUMBER	C_{OUT} CERAMIC	VENDORS	PART NUMBER
220µF, 6.3V	PANASONIC	6TPE220MI	10µF, 6.3V	KEMET	C0402C106M9PACTU	22µF, 6.3V	Murata	GRM188C80J226ME15D

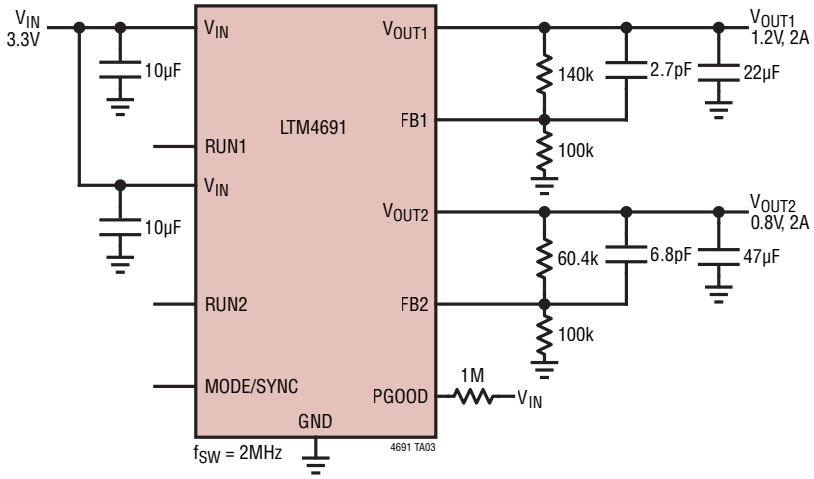
V_{OUT} (V)	C_{IN} (CERAMIC) (µF)	C_{IN} (BULK) (µF)	C_{OUT1} (CERAMIC) (µF)	C_{OUT2} (CERAMIC) (µF)	C_{FF} (pF)	V_{IN} (V)	DROOP (mV)	P-P DERIVATION (mV)	RECOVERY TIME (µs)	LOAD STEP (A)	LOAD STEP SLEW RATE (A/µs)
1.0	10 ×2	220	22	22	2.7	2.25, 3.3	20	45	25	0.5	0.5
1.5	10 ×2	220	22	22	1.2	2.25, 3.3	25	50	25	0.5	0.5
1.8	10 ×2	220	22	22	1.2	2.25, 3.3	30	60	25	0.5	0.5
2.5	10 ×2	220	22	22	1	3.3	42	84	30	0.5	0.5

TYPICAL APPLICATIONS

Dual 1.5V and 1.8V 2MHz, 2A Buck Regulators, V_{IN} = 2.5V

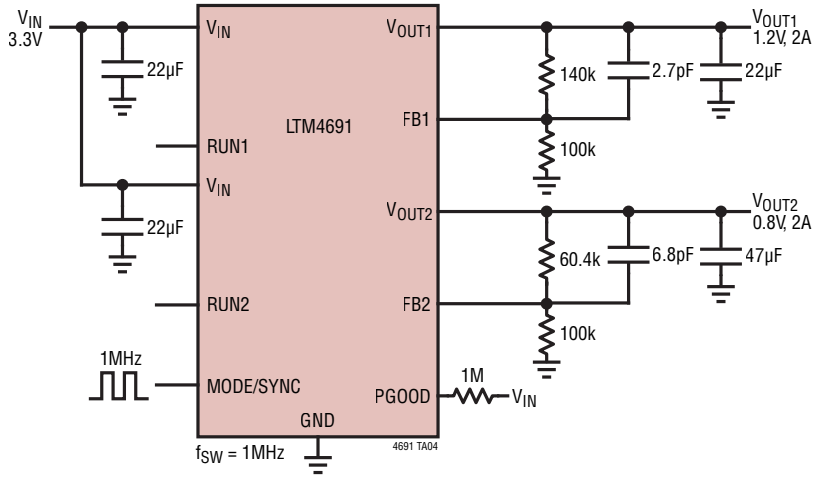


Dual 1.2V and 0.8V 2MHz, 2A Buck Regulators, V_{IN} = 3.3V

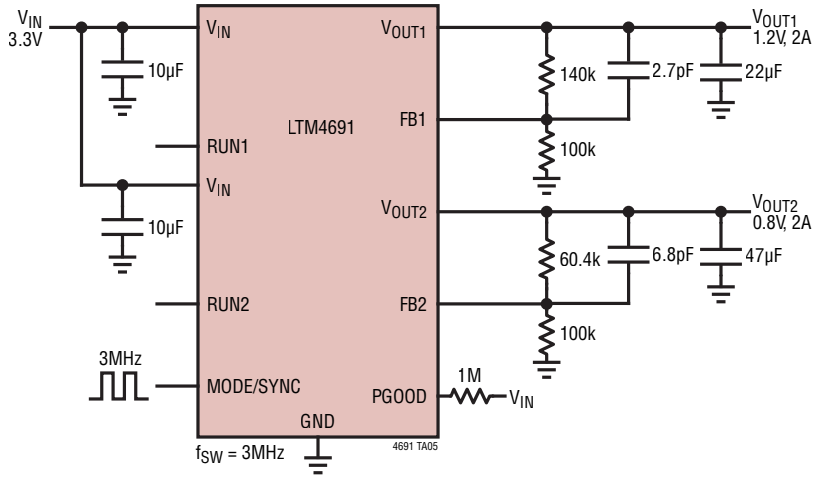


TYPICAL APPLICATIONS

Dual 1.2V and 0.8V 1MHz, 2A Buck Regulators, V_{IN} = 3.3V



Dual 1.2V and 0.8V 3MHz, 2A Buck Regulators, V_{IN} = 3.3V



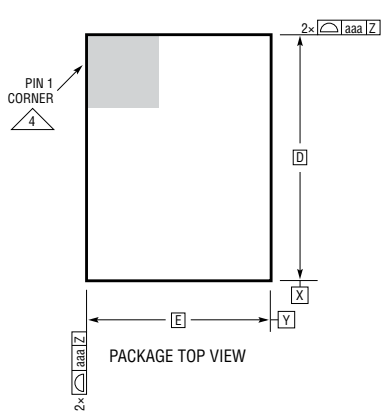
PIN CONFIGURATION TABLE

LTM4691 Component LGA and BGA Pinout

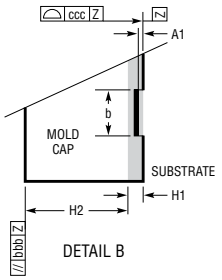
PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
A1	SGND2	A2	FB2	A3	FB1	A4	SGND1
B1	PGOOD	B2	RUN2	B3	RUN1	B4	MODE/SYNC
C1	V_{IN}	C2	GND	C3	GND	C4	V_{IN}
D1	GND	D2	GND	D3	GND	D4	GND
E1	V_{OUT2}	E2	GND	E3	GND	E4	V_{OUT1}
F1	V_{OUT2}	F2	V_{OUT2}	F3	V_{OUT1}	F4	V_{OUT1}

PACKAGE DESCRIPTION

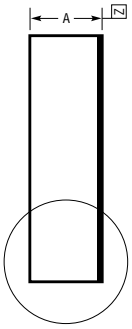
LGA Package
24-Lead (3mm × 4mm × 1.18mm)
(Reference LTC DWG# 05-08-1657 Rev A)



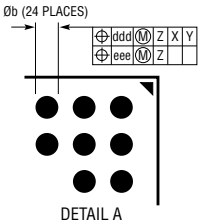
PACKAGE TOP VIEW



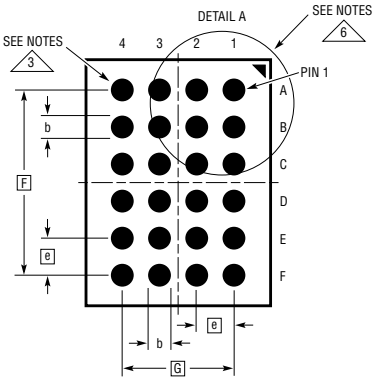
DETAIL B



DETAIL B
PACKAGE SIDE VIEW

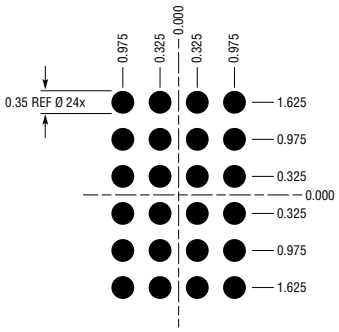


DETAIL A



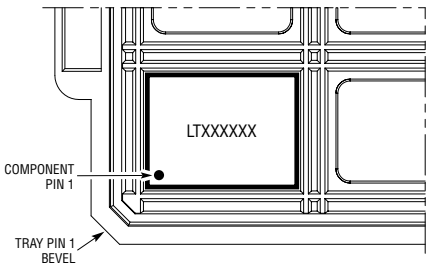
PACKAGE BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. PAD DESIGNATION PER JEP95
4. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN 1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
5. PRIMARY DATUM -Z- IS SEATING PLANE
6. ⚠ PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY



SUGGESTED PCB LAYOUT
TOP VIEW

DIMENSIONS				
SYMBOL	**MIN**	**NOM**	**MAX**	**NOTES**
A	1.08	1.18	1.28	
A1			0.03	
b	0.32	0.35	0.38	PAD DIMENSION
D		4.00		
E		3.00		
e		0.65		
F		3.25		
G		1.95		
H1		0.18 REF		SUBSTRATE THK
H2		1.00 REF		MOLD CAP HT
aaa			0.15	
bbb			0.10	
ccc			0.10	
ddd			0.15	
eee			0.08	
TOTAL NUMBER OF PADS: 24				



PACKAGE IN TRAY LOADING ORIENTATION

LGA 24 0319 REV A

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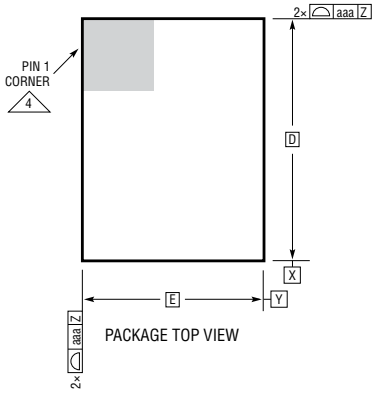
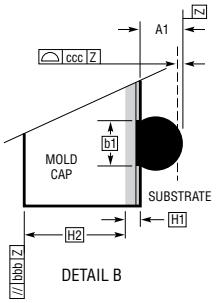
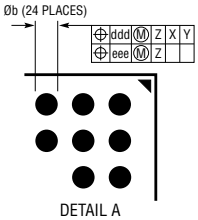
BGA Package
24-Lead (4mm × 3mm × 1.48mm)
(Reference LTC DWG# 05-08-1658 Rev Ø)



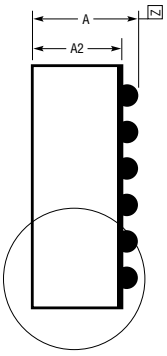
PACKAGE TOP VIEW



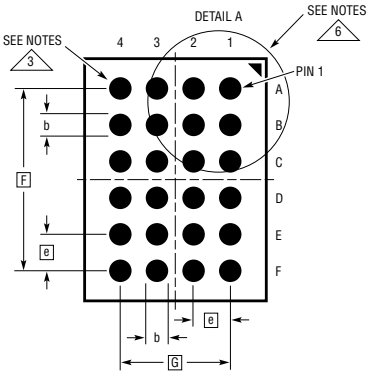
DETAIL B



DETAIL A



DETAIL B
PACKAGE SIDE VIEW



PACKAGE BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. BALL DESIGNATION PER JEP95
4. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN 1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
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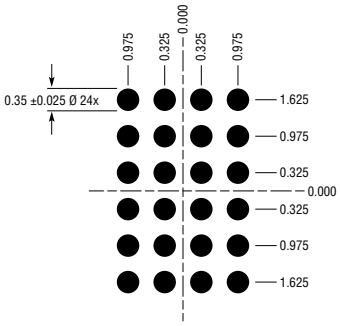
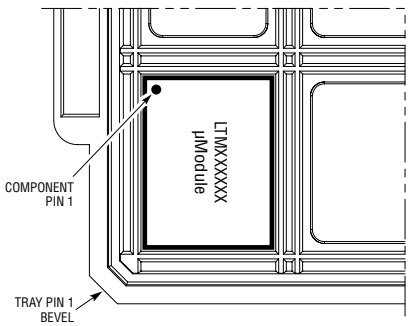


SUGGESTED PCB LAYOUT
TOP VIEW

DIMENSIONS				
SYMBOL	**MIN**	**NOM**	**MAX**	**NOTES**
A	1.32	1.48	1.64	
A1	0.23	0.30	0.37	BALL HT
A2	1.09	1.18	1.27	
b	0.35	0.40	0.45	BALL DIMENSION
b1	0.32	0.35	0.38	PAD DIMENSION
D		4.00		
E		3.00		
e		0.65		
F		3.25		
G		1.95		
H1		0.18 REF		SUBSTRATE THK
H2		1.00 REF		MOLD CAP HT
aaa			0.15	
bbb			0.10	
ccc			0.10	
ddd			0.15	
eee			0.08	
TOTAL NUMBER OF BALLS: 24				



PACKAGE IN TRAY LOADING ORIENTATION

BGA 24 0718 REV Ø

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	10/20	Add LTM4691IY#PBF order information	1, 2, 3, 21, 23, 24

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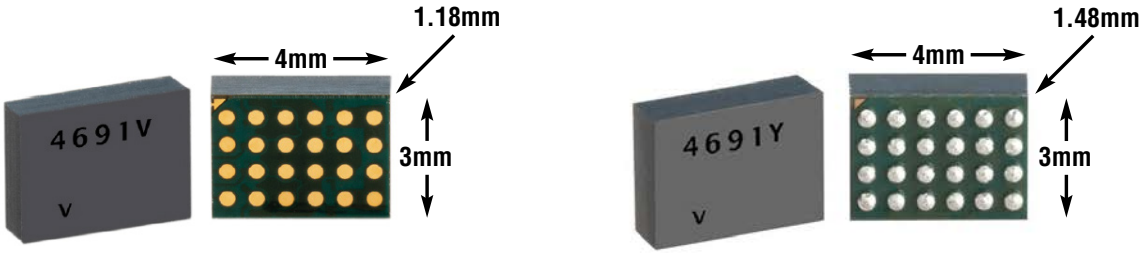
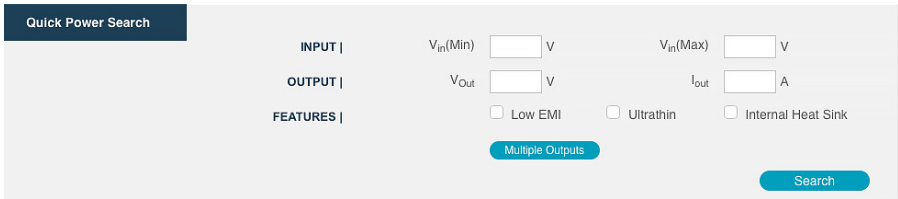
PACKAGE PHOTO



DESIGN RESOURCES

SUBJECT	DESCRIPTION	
µModule Design and Manufacturing Resources	Design: • Selector Guides • Demo Boards and Gerber Files • Free Simulation Tools	Manufacturing: • Quick Start Guide • PCB Design, Assembly and Manufacturing Guidelines • Package and Board Level Reliability
µModule Regulator Products Search	1. Sort table of products by parameters and download the result as a spread sheet. 2. Search using the Quick Power Search parametric table.  	
Digital Power System Management	Analog Devices' family of digital power supply management ICs are highly integrated solutions that offer essential functions, including power supply monitoring, supervision, margining and sequencing, and feature EEPROM for storing user configurations and fault logging.	

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM4622	Ultrathin, Dual 2.5A or Single 5A Step-Down uModule Regulator	3.6V ≤ V_{IN} ≤ 20V, 0.6V ≤ V_{OUT} ≤ 5.5V, 6.25mm x 6.25mm x 1.82mm LGA, 6.25mm x 6.25mm x 2.42mm BGA.
LTM4622A	Ultrathin, Dual 2A or Single 4A Step-Down uModule Regulator	3.6V ≤ V_{IN} ≤ 20V, 1.5V ≤ V_{OUT} ≤ 12V, 6.25mm x 6.25mm x 1.82mm LGA, 6.25mm x 6.25mm x 2.42mm BGA.
LTM4623	Ultrathin, Single 3A Step-Down µModule Regulator	4V ≤ V_{IN} ≤ 20V, 0.6V ≤ V_{OUT} ≤ 5.5V, 6.25mm x 6.25mm x 1.82mm LGA, 6.25mm x 6.25mm x 2.42mm BGA.
LTM4624	Single 4A Step-Down µModule Regulator	4V ≤ V_{IN} ≤ 14V, 0.6V ≤ V_{OUT} ≤ 5.5V, 6.25mm x 6.25mm x 5.01mm BGA.
LTM4625	Single 5A Step-Down µModule Regulator	4V ≤ V_{IN} ≤ 20V, 0.6V ≤ V_{OUT} ≤ 5.5V, 6.25mm x 6.25mm x 5.01mm BGA.
LTM4632	Ultrathin, Triple Output, ±3A Step-Down µModule Regulator for DDR Memory	3.6V ≤ V_{IN} ≤ 15V, 0.6V ≤ V_{OUT} ≤ 2.5V, 6.25mm x 6.25mm x 1.82mm LGA, 6.25mm x 6.25mm x 2.42mm BGA.
LTM4668/ LTM4668A	Quad 1.2A Step-Down µModule Regulator	2.7V ≤ V_{IN} ≤ 17V, 0.6V ≤ V_{OUT} ≤ 1.8V (LTM4668A: 0.6V ≤ V_{OUT} ≤ 5.5V, 2.25MHz) 6.25mm x 6.25mm x 2.1mm BGA.
LTM4643	Ultrathin, Quad 3A Step-Down µModule Regulator	4V ≤ V_{IN} ≤ 20V, 0.6V ≤ V_{OUT} ≤ 3.3V, 9mm x 15mm x 1.82mm LGA, 9mm x 15mm x 2.42mm BGA.
LTM4644	Quad 4A Step-Down µModule Regulator	4V ≤ V_{IN} ≤ 14V, 0.6V ≤ V_{OUT} ≤ 5.5V, 9mm x 15mm x 5.01mm BGA.

Rev. A

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