

## Silicon Digital Attenuator, 2-Bit, 100 MHz to 30 GHz

### FEATURES

- ▶ Ultra-wideband frequency range: 100 MHz to 30 GHz
- ▶ Attenuation range: 16 dB typical steps to 48 dB
- ▶ Low insertion loss
  - ▶ 1.6 dB at 8 GHz
  - ▶ 2.2 dB at 18 GHz
  - ▶ 2.9 dB at 30 GHz
- ▶ Attenuation accuracy
  - ▶  $\pm (0.25 + 3.6 \% \text{ of attenuation state})$  dB typical up to 8 GHz
  - ▶  $\pm (0.10 + 1.8 \% \text{ of attenuation state})$  dB typical up to 18 GHz
  - ▶  $\pm (0.50 + 2.8 \% \text{ of attenuation state})$  dB typical up to 30 GHz
- ▶ Typical step error
  - ▶  $\pm 0.7$  dB typical up to 8 GHz
  - ▶  $\pm 1.0$  dB typical up to 18 GHz
  - ▶  $\pm 1.5$  dB typical up to 30 GHz
- ▶ High input linearity
  - ▶ P0.1dB insertion loss state: 30 dBm typical
  - ▶ P0.1dB other attenuation states: 30 dBm typical
  - ▶ IIP3: 50 dBm typical
- ▶ High RF power handling
  - ▶ 30 dBm average typical
  - ▶ 33 dBm peak typical
- ▶ RF amplitude settling time (0.1 dB of final  $RF_{OUT}$ ): 130 ns typical
- ▶ Single-supply operation supported
- ▶ Tight distribution in relative phase
- ▶ No low-frequency spurious signals
- ▶ Parallel mode control, CMOS-/LVTTTL-compatible
- ▶ 20-terminal, 3.00 mm × 3.00 mm, land grid array [LGA]

### APPLICATIONS

- ▶ Industrial scanners
- ▶ Test and instrumentation
- ▶ Cellular infrastructure: 5G millimeter wave
- ▶ Military radios, radars, electronic counter measures (ECMs)
- ▶ Microwave radios and very small aperture terminals (VSATs)

### FUNCTIONAL BLOCK DIAGRAM

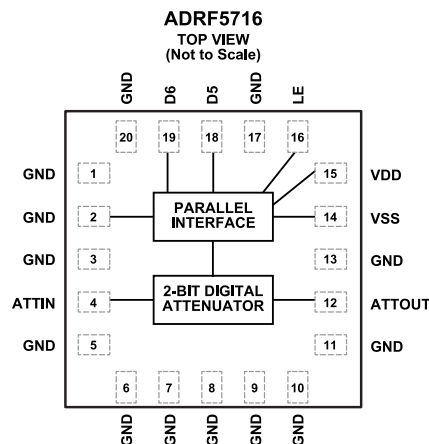


Figure 1. Functional Block Diagram

### GENERAL DESCRIPTION

The ADRF5716 is a silicon, 2-bit digital attenuator with 48 dB attenuation control range in 16 dB steps, supporting glitch-free operation.

This device operates from 100 MHz to 30 GHz with better than 2.9 dB of insertion loss and better than 1.5 dB attenuation accuracy. The ATTIN and ATTOUT ports of the ADRF5716 have an RF input power handling capability of 30 dBm average and 33 dBm peak for all states.

The ADRF5716 requires a dual-supply voltage of +3.3 V and -3.3 V. The device features parallel mode control and complementary metal-oxide semiconductor (CMOS)/low voltage transistor to transistor logic (LVTTTL)-compatible controls.

The ADRF5716 can also operate with a single positive supply voltage ( $V_{DD}$ ) applied when the negative supply voltage ( $V_{SS}$ ) is tied to ground. See the [Theory of Operation](#) section for more details.

The ADRF5716 RF ports are designed to match a characteristic impedance of 50  $\Omega$ . The ADRF5716 comes in a 20-terminal, 3.00 mm × 3.00 mm, RoHS compliant, land grid array [LGA] package and operates from -40°C to +105°C.

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**REVISION HISTORY****1/2025—Rev. A to Rev. B**

|                                 |    |
|---------------------------------|----|
| Updated Outline Dimensions..... | 15 |
|---------------------------------|----|

**5/2024—Rev. 0 to Rev. A**

|                                                              |   |
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**11/2023—Revision 0: Initial Version**

## SPECIFICATIONS

Positive supply voltage ( $V_{DD}$ ) = 3.3 V, negative supply voltage ( $V_{SS}$ ) = -3.3 V, control voltages ( $V_{CTRL}$ ) = 0 V or  $V_{DD}$ , and  $T_{CASE}$  = 25°C with a 50  $\Omega$  system, unless otherwise noted.  $V_{CTRL}$  refers to the control voltages on the LE, D5, and D6 pins.

Table 1. Specifications

| Parameter                    | Symbol | Test Conditions/Comments                                                        | Min                  | Typ                                  | Max    | Unit    |
|------------------------------|--------|---------------------------------------------------------------------------------|----------------------|--------------------------------------|--------|---------|
| FREQUENCY RANGE              | f      |                                                                                 | 100                  |                                      | 30,000 | MHz     |
| INSERTION LOSS               |        | 100 MHz to 8 GHz                                                                |                      | 1.6                                  |        | dB      |
|                              |        | 8 GHz to 18 GHz                                                                 |                      | 2.2                                  |        | dB      |
|                              |        | 18 GHz to 30 GHz                                                                |                      | 2.9                                  |        | dB      |
| RETURN LOSS                  |        | ATTIN and ATTOUT, attenuation state                                             |                      |                                      |        |         |
|                              |        | 100 MHz to 8 GHz                                                                |                      | 19                                   |        | dB      |
|                              |        | 8 GHz to 18 GHz                                                                 |                      | 21                                   |        | dB      |
|                              |        | 18 GHz to 30 GHz                                                                |                      | 17                                   |        | dB      |
| ATTENUATION                  |        |                                                                                 |                      |                                      |        |         |
| Range                        |        | Between minimum and maximum attenuation states                                  |                      | 48                                   |        | dB      |
| Step Size                    |        | Between any successive attenuation states                                       |                      | 16                                   |        | dB      |
| Accuracy                     |        | Referenced to insertion loss                                                    |                      |                                      |        |         |
|                              |        | 100 MHz to 8 GHz                                                                |                      | $\pm(0.25 + 3.6\% \text{ of state})$ |        | dB      |
|                              |        | 8 GHz to 18 GHz                                                                 |                      | $\pm(0.10 + 1.8\% \text{ of state})$ |        | dB      |
| Step Error                   |        | 18 GHz to 30 GHz                                                                |                      | $\pm(0.50 + 2.8\% \text{ of state})$ |        | dB      |
|                              |        | Between any successive attenuation states                                       |                      |                                      |        |         |
|                              |        | 100 MHz to 8 GHz                                                                |                      | $\pm 0.7$                            |        | dB      |
|                              |        | 8 GHz to 18 GHz                                                                 |                      | $\pm 1.0$                            |        | dB      |
| RELATIVE PHASE               |        | 18 GHz to 30 GHz                                                                |                      | $\pm 1.5$                            |        | dB      |
|                              |        | Referenced to insertion loss                                                    |                      |                                      |        |         |
|                              |        | 100 MHz to 8 GHz                                                                |                      | 36                                   |        | Degrees |
|                              |        | 8 GHz to 18 GHz                                                                 |                      | 80                                   |        | Degrees |
| SWITCHING                    |        | 18 GHz to 30 GHz                                                                |                      | 165                                  |        | Degrees |
|                              |        | All attenuation states at input power ( $P_{IN}$ ) = 10 dBm                     |                      |                                      |        |         |
|                              |        | Rise Time and Fall Time                                                         | $t_{RISE}, t_{FALL}$ | 20                                   |        | ns      |
|                              |        | On Time and Off Time                                                            | $t_{ON}, t_{OFF}$    | 50                                   |        | ns      |
|                              |        | RF Amplitude Settling Time                                                      |                      |                                      |        |         |
|                              |        | 0.1 dB                                                                          |                      | 130                                  |        | ns      |
|                              |        | 0.05 dB                                                                         |                      | 160                                  |        | ns      |
|                              |        | RF Phase Settling Time                                                          |                      |                                      |        |         |
| INPUT LINEARITY <sup>1</sup> |        | f = 1 GHz                                                                       |                      |                                      |        |         |
|                              |        | 50% triggered control to 5° of final $RF_{OUT}$                                 |                      | 430                                  |        | ns      |
|                              |        | 50% triggered control to 1° of final $RF_{OUT}$                                 |                      | 450                                  |        | ns      |
|                              |        | 100 MHz to 30 GHz                                                               |                      |                                      |        |         |
|                              |        | 0.1 dB Power Compression                                                        | P0.1dB               | 30                                   |        | dBm     |
| Insertion Loss State         |        |                                                                                 |                      |                                      |        |         |
|                              |        | Other Attenuation States                                                        |                      | 30                                   |        | dBm     |
|                              |        | Third-Order Intercept                                                           | IP3                  | 50                                   |        | dBm     |
|                              |        | Two-tone $P_{IN}$ = 20 dBm per tone, $\Delta f$ = 1 MHz, all attenuation states |                      |                                      |        |         |
|                              |        |                                                                                 |                      |                                      |        |         |

## SPECIFICATIONS

Table 1. Specifications (Continued)

| Parameter                           | Symbol     | Test Conditions/Comments                                                              | Min   | Typ | Max      | Unit             |
|-------------------------------------|------------|---------------------------------------------------------------------------------------|-------|-----|----------|------------------|
| DIGITAL CONTROL INPUTS              |            | LE, D5, and D6                                                                        |       |     |          |                  |
| Voltage                             |            |                                                                                       |       |     |          |                  |
| Low                                 | $V_{INL}$  |                                                                                       | 0     |     | 0.8      | V                |
| High                                | $V_{INH}$  |                                                                                       | 1.2   |     | 3.3      | V                |
| Current                             |            |                                                                                       |       |     |          |                  |
| Low                                 | $I_{INL}$  |                                                                                       |       | -33 |          | $\mu$ A          |
| High                                | $I_{INH}$  |                                                                                       |       | <1  |          | $\mu$ A          |
| SUPPLY CURRENT                      |            | VDD and VSS                                                                           |       |     |          |                  |
| Positive Supply Current             |            |                                                                                       |       |     |          |                  |
| LE, D5, and D6 = 0 V                |            |                                                                                       |       | 230 |          | $\mu$ A          |
| LE, D5, and D6 = 3.3 V <sup>2</sup> |            |                                                                                       |       | 130 |          | $\mu$ A          |
| Negative Supply Current             |            |                                                                                       |       | 500 |          | $\mu$ A          |
| RECOMMENDED OPERATING CONDITIONS    |            |                                                                                       |       |     |          |                  |
| Supply Voltage                      |            |                                                                                       |       |     |          |                  |
| Positive                            | $V_{DD}$   |                                                                                       | 3.15  |     | 3.45     | V                |
| Negative                            | $V_{SS}$   |                                                                                       | -3.45 |     | -3.15    | V                |
| Digital Control Voltage             |            |                                                                                       | 0     |     | $V_{DD}$ | V                |
| RF Power Handling <sup>3</sup>      |            | $f = 100 \text{ MHz to } 30 \text{ GHz}$ , $T_{CASE} = 85^\circ\text{C}$ <sup>4</sup> |       |     |          |                  |
| Input at ATTIN or ATTOUT            |            | Steady state average                                                                  |       |     | 30       | dBm              |
|                                     |            | Steady state peak                                                                     |       |     | 33       | dBm              |
|                                     |            | Hot switching                                                                         |       |     | 30       | dBm              |
| Case Temperature                    | $T_{CASE}$ |                                                                                       | -40   |     | +105     | $^\circ\text{C}$ |

<sup>1</sup> Input linearity performance degrades over frequency, see Figure 16 to Figure 19.

<sup>2</sup> If LE, D5, and D6 are in a different combination of states, the positive supply current is between 130  $\mu$ A and 230  $\mu$ A.

<sup>3</sup> For power derating over frequency, see Figure 2 and Figure 3. Applicable for all ATTIN and ATTOUT power specifications.

<sup>4</sup> For 105 $^\circ\text{C}$  operation, the power handling degrades from the  $T_{CASE} = 85^\circ\text{C}$  specifications by 3 dB.

## SPECIFICATIONS

## SINGLE-SUPPLY OPERATION

$V_{DD} = 3.3\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $V_{CTRL} = 0\text{ V}$  or  $V_{DD}$ , and  $T_{CASE} = 25^\circ\text{C}$  with a  $50\ \Omega$  system, unless otherwise noted. The small signal and bias characteristics are maintained for the single-supply operation.

Table 2. Single-Supply Operation Specifications

| Parameter                            | Symbol                  | Test Conditions/Comments                                                                       | Min | Typ  | Max    | Unit |
|--------------------------------------|-------------------------|------------------------------------------------------------------------------------------------|-----|------|--------|------|
| FREQUENCY RANGE                      | f                       |                                                                                                | 100 |      | 30,000 | MHz  |
| SWITCHING                            |                         |                                                                                                |     |      |        |      |
| Rise Time and Fall Time              | $t_{RISE}$ , $t_{FALL}$ | All attenuation states at $P_{IN} = 10\text{ dBm}$<br>10% to 90% of $RF_{OUT}$                 |     | 100  |        | ns   |
| On Time and Off Time                 | $t_{ON}$ , $t_{OFF}$    | 50% triggered control to 90% of $RF_{OUT}$                                                     |     | 130  |        | ns   |
| RF Amplitude Settling Time<br>0.1 dB |                         | 50% triggered control to 0.1 dB of final $RF_{OUT}$                                            |     | 400  |        | ns   |
| RF Phase Settling Time<br>5°         |                         | f = 1 GHz<br>50% triggered control to 5° of final $RF_{OUT}$                                   |     | 1.2  |        | μs   |
| 1°                                   |                         | 50% triggered control to 1° of final $RF_{OUT}$                                                |     | 1.25 |        | μs   |
| INPUT LINEARITY                      |                         | 100 MHz to 30 GHz                                                                              |     |      |        |      |
| 0.1 dB Power Compression             | P0.1dB                  |                                                                                                |     | 21   |        | dBm  |
| Insertion Loss State                 |                         |                                                                                                |     | 21   |        | dBm  |
| Other Attenuation States             |                         |                                                                                                |     |      |        |      |
| Third-Order Intercept                | IP3                     | Two-tone $P_{IN} = 20\text{ dBm}$ per tone, $\Delta f = 1\text{ MHz}$ , all attenuation states |     | 35   |        | dBm  |
| Insertion Loss State                 |                         |                                                                                                |     | 36   |        | dBm  |
| Other Attenuation States             |                         |                                                                                                |     |      |        |      |
| RECOMMENDED OPERATING CONDITIONS     |                         |                                                                                                |     |      |        |      |
| RF Power Handling                    |                         | f = 100 MHz to 30 GHz, $T_{CASE} = 85^\circ\text{C}$                                           |     |      |        |      |
| Input at ATTIN and ATTOUT            |                         | Average                                                                                        |     |      | 18     | dBm  |
|                                      |                         | Peak                                                                                           |     |      | 18     | dBm  |
|                                      |                         | Hot switching                                                                                  |     |      | 18     | dBm  |
| Case Temperature                     | $T_{CASE}$              |                                                                                                | -40 |      | +105   | °C   |

## ABSOLUTE MAXIMUM RATINGS

For recommended operating conditions, see Table 1 and Table 2.

Table 3. Absolute Maximum Ratings

| Parameter                                                                                                           | Rating                     |
|---------------------------------------------------------------------------------------------------------------------|----------------------------|
| $V_{DD}$                                                                                                            | -0.3 V to +3.6 V           |
| $V_{SS}$                                                                                                            | -3.6 V to +0.3 V           |
| Digital Control Inputs                                                                                              |                            |
| Voltage                                                                                                             | -0.3 V to $V_{DD} + 0.3$ V |
| Current                                                                                                             | 3 mA                       |
| RF Input Power <sup>1</sup>                                                                                         |                            |
| Dual Supply ( $V_{DD} = 3.3$ V, $V_{SS} = -3.3$ V, $f = 100$ MHz to 30 GHz, and $T_{CASE} = 85^{\circ}\text{C}^2$ ) |                            |
| Average                                                                                                             | 31 dBm                     |
| Peak                                                                                                                | 34 dBm                     |
| Hot Switching                                                                                                       | 31 dBm                     |
| Single Supply ( $V_{DD} = 3.3$ V, $V_{SS} = 0$ V, $f = 100$ MHz to 30 GHz, and $T_{CASE} = 85^{\circ}\text{C}^2$ )  |                            |
| Average                                                                                                             | 19 dBm                     |
| Peak                                                                                                                | 19 dBm                     |
| Hot Switching                                                                                                       | 19 dBm                     |
| Unbiased Condition ( $V_{DD}$ and $V_{SS} = 0$ V)                                                                   | 15 dBm                     |
| Temperature                                                                                                         |                            |
| Junction                                                                                                            | 135°C                      |
| Storage                                                                                                             | -65°C to +150°C            |
| Reflow                                                                                                              | 260°C                      |

<sup>1</sup> For power derating over frequency, see Figure 2 and Figure 3. Applicable for all ATTIN and ATTOUT power specifications.

<sup>2</sup> For 105°C operation, the power handling degrades from the  $T_{CASE} = 85^{\circ}\text{C}$  specification by 3 dB.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

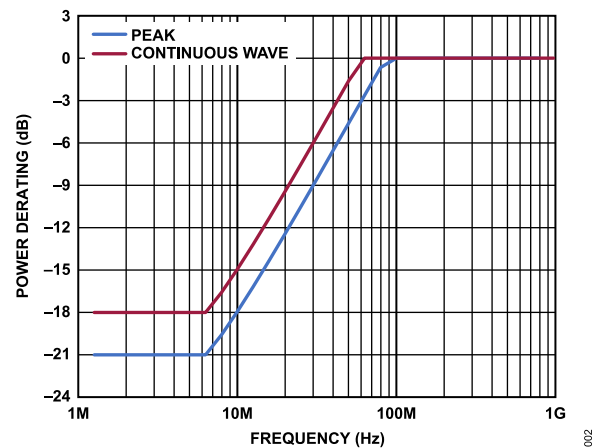
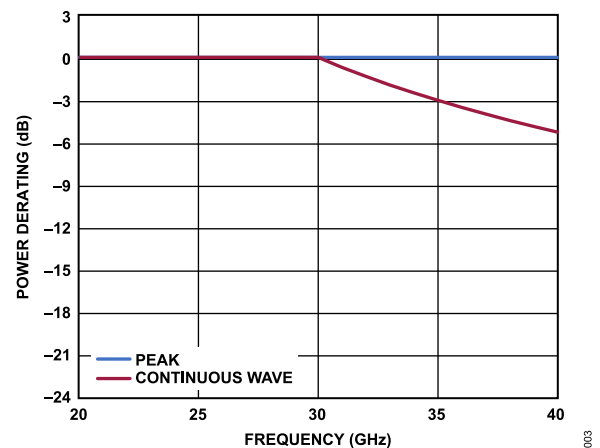
$\theta_{JC}$  is the junction to case bottom (channel to package bottom) thermal resistance.

Table 4. Thermal Resistance

| Package Type | $\theta_{JC}$ <sup>1</sup> | Unit |
|--------------|----------------------------|------|
| CC-20-9      | 50                         | °C/W |

<sup>1</sup>  $\theta_{JC}$  was determined by simulation under the following conditions: the heat transfer is due solely to thermal conduction from the channel through the ground pad to the PCB, and the ground pad is held constant at the operating temperature of 85°C.

## POWER DERATING CURVES

Figure 2. Power Derating vs. Frequency, Low Frequency Detail,  $T_{CASE} = 85^{\circ}\text{C}$ Figure 3. Power Derating vs. Frequency, High Frequency Detail,  $T_{CASE} = 85^{\circ}\text{C}$

**ABSOLUTE MAXIMUM RATINGS****ELECTROSTATIC DISCHARGE (ESD) RATINGS**

The following ESD information is provided for handling of ESD sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

**ESD Ratings for ADRF5716**

*Table 5. ADRF5716, 20-Terminal LGA*

| ESD Model               | Withstand Threshold (V) | Class |
|-------------------------|-------------------------|-------|
| HBM                     |                         |       |
| ATTIN and ATTOUT Pins   | 1000                    | 1C    |
| Supply and Control Pins | 2000                    | 2     |
| CDM                     | 500                     | C2A   |

**ESD CAUTION**

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

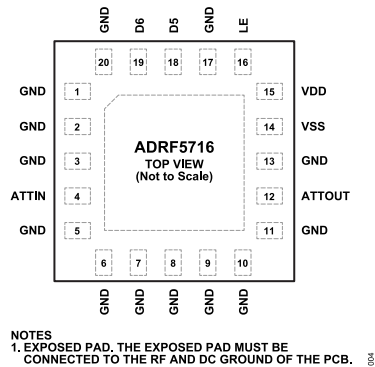


Figure 4. Pin Configuration

Table 6. Pin Function Descriptions

| Pin No.                     | Mnemonic | Description                                                                                                                                           |
|-----------------------------|----------|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1 to 3, 5 to 11, 13, 17, 20 | GND      | Ground. The GND pins must be connected to the RF and DC ground of the PCB.                                                                            |
| 4                           | ATTIN    | Attenuator Input. No DC blocking capacitor is necessary when the RF line potential is equal to 0 V DC. See Figure 5 for the interface schematic.      |
| 12                          | ATTOUT   | Attenuator Output. No DC blocking capacitor is necessary when the RF line potential is equal to 0 V DC. See Figure 5 for the interface schematic.     |
| 14                          | VSS      | Negative Supply Input. See Figure 8 for the interface schematic.                                                                                      |
| 15                          | VDD      | Positive Supply Input. See Figure 7 for the interface schematic.                                                                                      |
| 16                          | LE       | Latch Enable Input. See the Theory of Operation section for more information. See Figure 6 for the interface schematic.                               |
| 18                          | D5       | Parallel Control Input for 16 dB Attenuation Bit. See the Theory of Operation section for more information. See Figure 6 for the interface schematic. |
| 19                          | D6       | Parallel Control Input for 32 dB Attenuation Bit. See the Theory of Operation section for more information. See Figure 6 for the interface schematic. |
|                             | EPAD     | Exposed Pad. The exposed pad must be connected to the RF and DC ground of the PCB.                                                                    |

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

## INTERFACE SCHEMATICS

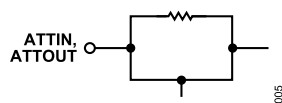


Figure 5. ATTIN Pin and ATTOUT Pin Interface Schematic

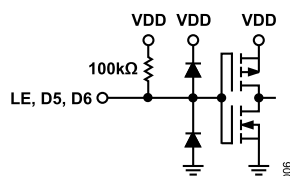


Figure 6. LE Pin, D5 Pin, and D6 Pin Interface Schematic

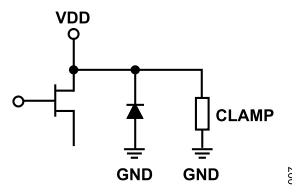


Figure 7. VDD Pin Interface Schematic

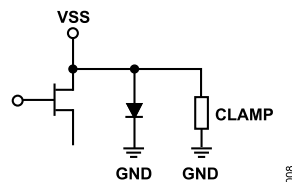


Figure 8. VSS Pin Interface Schematic

## TYPICAL PERFORMANCE CHARACTERISTICS

## INSERTION LOSS, RETURN LOSS, STATE ERROR, STEP ERROR, AND RELATIVE PHASE

$V_{DD} = 3.3\text{ V}$ ,  $V_{SS} = -3.3\text{ V}$ ,  $V_{CTRL} = 0\text{ V}$  or  $V_{DD}$ , and  $T_{CASE} = 25^\circ\text{C}$  with a  $50\ \Omega$  system, unless otherwise noted.

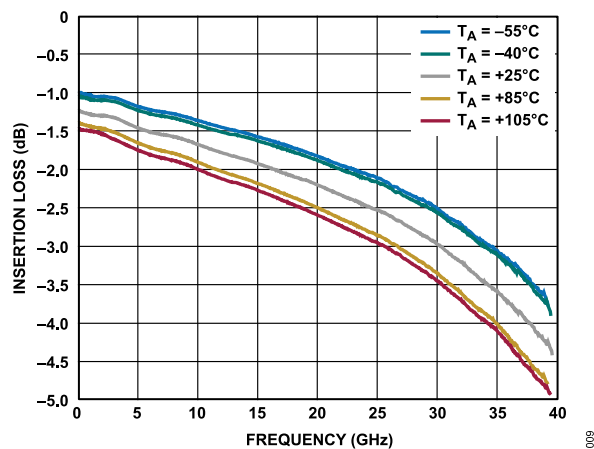


Figure 9. Insertion Loss vs. Frequency over Temperature

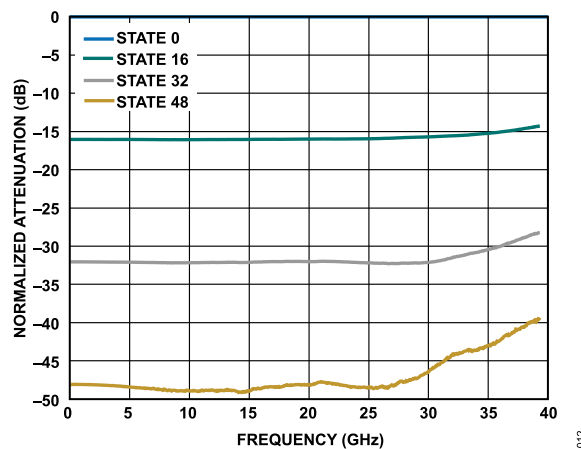


Figure 12. Normalized Attenuation vs. Frequency for All States

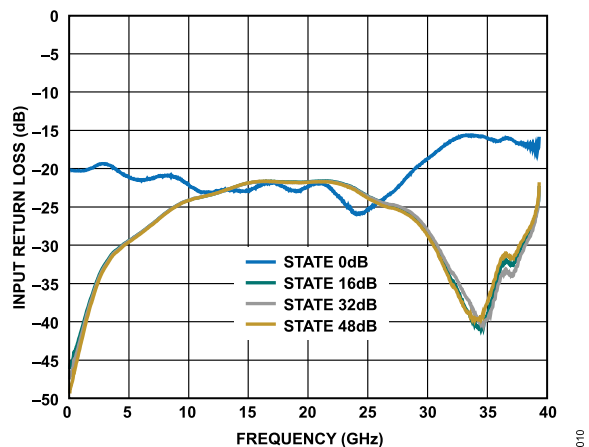


Figure 10. Input Return Loss vs. Frequency

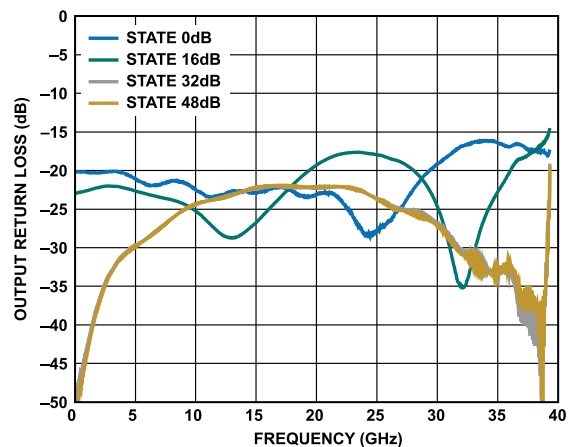


Figure 13. Output Return Loss vs. Frequency

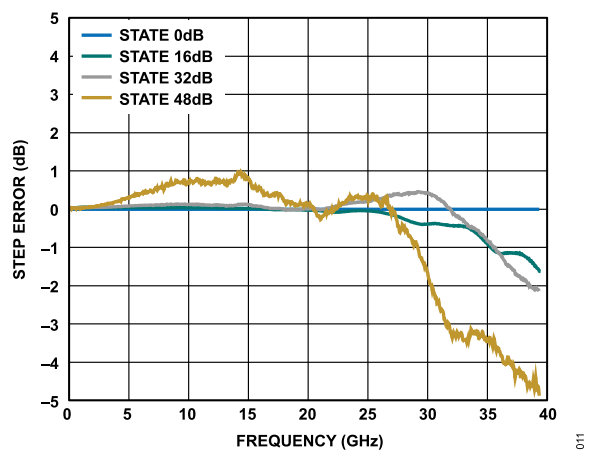


Figure 11. Step Error vs. Frequency

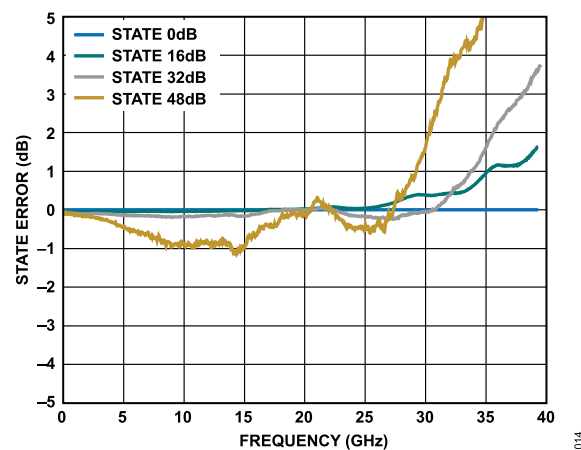


Figure 14. State Error vs. Frequency

## TYPICAL PERFORMANCE CHARACTERISTICS

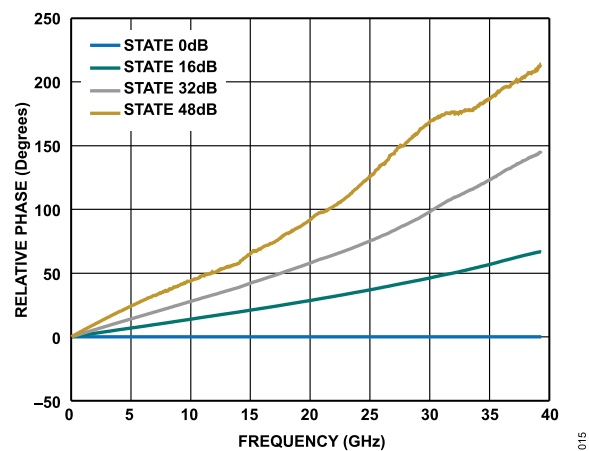


Figure 15. Relative Phase vs. Frequency

## TYPICAL PERFORMANCE CHARACTERISTICS

## INPUT POWER COMPRESSION AND THIRD-ORDER INTERCEPT

$V_{DD} = 3.3\text{ V}$ ,  $V_{SS} = -3.3\text{ V}$ ,  $V_{CTRL} = 0\text{ V}$  or  $V_{DD}$ , and  $T_{CASE} = 25^\circ\text{C}$  with a  $50\ \Omega$  system, unless otherwise noted.

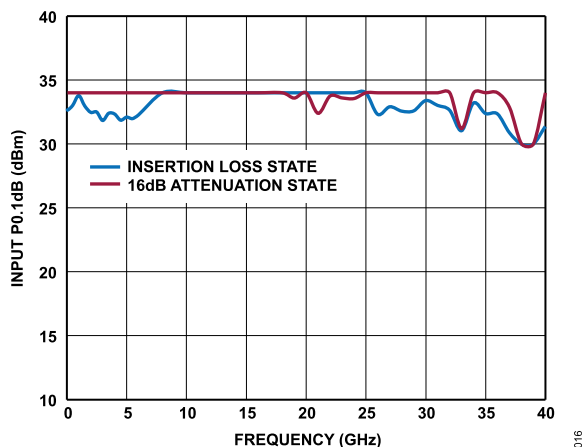


Figure 16. Input P0.1dB vs. Frequency

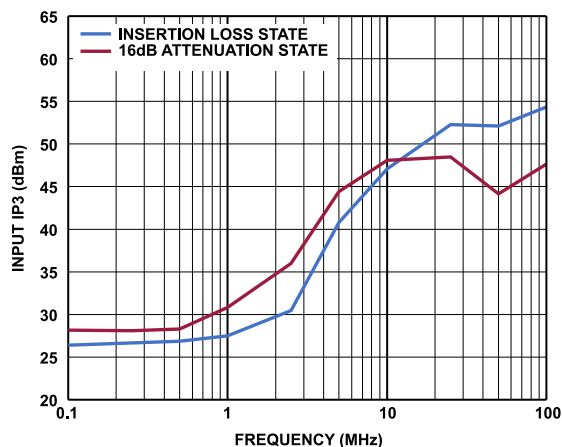


Figure 19. Input IP3 vs. Frequency, Low Frequency Detail

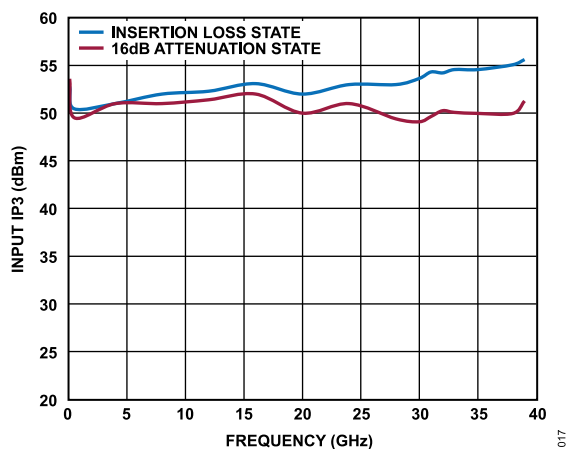


Figure 17. Input IP3 vs. Frequency

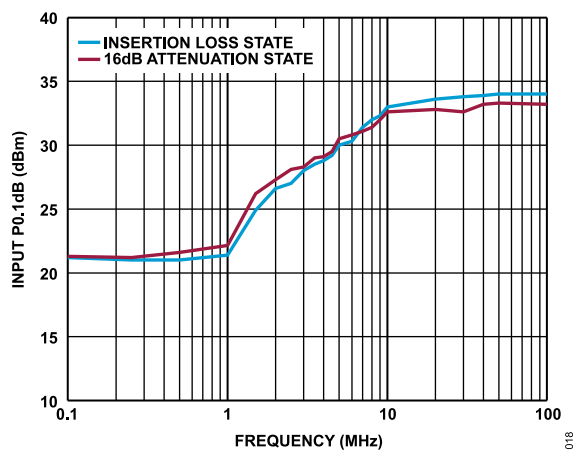


Figure 18. Input P0.1dB vs. Frequency, Low Frequency Detail

THEORY OF OPERATION

The ADRF5716 incorporates a 2-bit fixed attenuator array that offers an attenuation range of 48 dB in 16 dB steps. An integrated driver provides parallel mode control of the attenuator array.

The ADRF5716 has two digital control inputs, D5 (LSB) and D6 (MSB), to select the desired attenuation state in parallel mode, as shown in Figure 20. See Table 7 for the truth table.

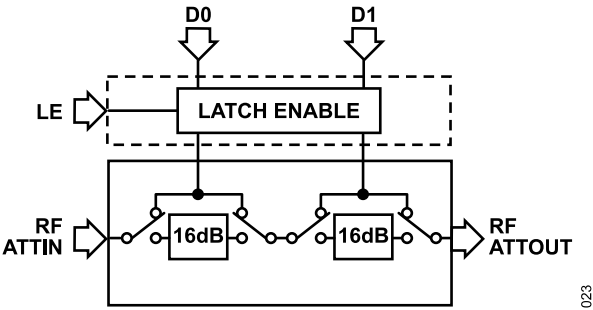


Figure 20. Simplified Circuit Diagram

Table 7. Truth Table

| Digital Control Input |      | Attenuation State (dB) |
|-----------------------|------|------------------------|
| D5                    | D6   |                        |
| Low                   | Low  | 0 (reference)          |
| High                  | Low  | 16                     |
| Low                   | High | 32                     |
| High                  | High | 48                     |

RF INPUT AND OUTPUT

Both RF ports (ATTIN and ATTOUT) are DC-coupled to 0 V. No DC blocking is required at the RF ports when the RF line potential is equal to 0 V.

The RF ports are internally matched to 50 Ω. Therefore, external matching components are not required.

The ADRF5716 supports bidirectional operation at the same power level. The power handling of the ATTIN and ATTOUT ports are the same. Refer to the RF input power specifications in Table 1.

The ADRF5716 can operate with a single positive supply voltage applied to the VDD pin and the VSS pin connected to ground. However, some performance degradations can occur in the input compression and input third-order intercept (see Table 2).

POWER SUPPLY

The ADRF5716 requires a positive supply voltage applied to the VDD pin and a negative supply voltage applied to the VSS pin. Bypassing capacitors are recommended on the supply lines to filter high-frequency noise.

The ideal power-up sequence is as follows:

1. Connect GND.
2. Power up VDD and VSS. Power up VSS after VDD to avoid current transients on VDD during ramp up.
3. Apply the digital control input. Powering the digital control input before the VDD supply can inadvertently forward bias and damage the internal ESD protection structures. To avoid this damage, use a series 1 kΩ resistor to limit the current flowing into the control pin. Use pull-up or pull-down resistors if the controller output is in a high-impedance state after VDD is powered up and the control pins are not driven to a valid logic state.
4. Apply an RF input signal to ATTIN or ATTOUT.

The ideal power-down sequence is the reverse order of the power-up sequence.

PARALLEL MODE INTERFACE

There are two modes of parallel operation: direct and latched.

Direct Parallel Mode

To enable direct parallel mode, the LE pin must be kept high. To change the attenuation state, use the control voltage inputs (D5 and D6) directly.

Latched Parallel Mode

To enable latched parallel mode, keep the LE pin low when changing the control voltage inputs (D5 and D6) to set the attenuation state. When the desired state is set, toggle LE high to transfer the data to the bypass switches of the attenuator array, and then toggle LE low to latch the change into the device until the next desired attenuation change.

The RF transmission lines are designed using a coplanar waveguide (CPWG) model, with a trace width of 16 mil and ground clearance of 6 mil for a characteristic impedance of 50  $\Omega$ . For optimal RF and thermal grounding, arrange as many through vias as possible around the transmission lines and under the exposed pad of the package.

Figure 21 shows the simplified application circuit for the ADRF5716.

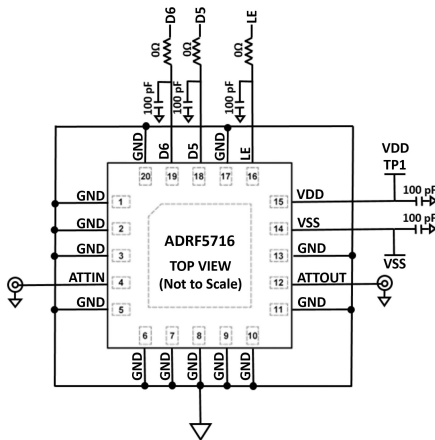


**Figure 21. Simplified Application Circuit**

The RF ports are matched to 50  $\Omega$  internally, and the pinout is designed to mate a CPWG with a 50  $\Omega$  characteristic impedance on the PCB. [Figure 22](#) shows the referenced CPWG RF trace design for an RF substrate with 12 mil thick Rogers RO4003 dielectric material. The RF trace with a 16 mil width and a 6 mil clearance is recommended for 2.2 mil finished copper thickness.

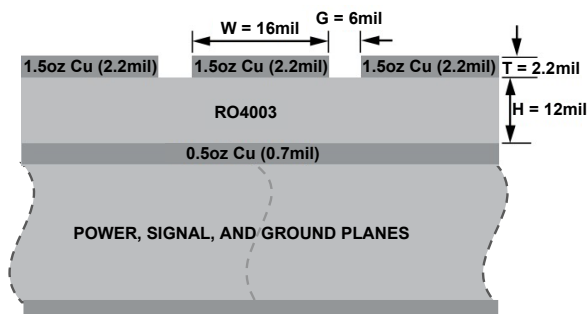


**Figure 22. Example PCB Stackup**

Figure 23 shows the routing of the RF traces, supply, and control signals from the ADRF5716. The ground planes are connected with as many filled through vias as allowed for optimal RF and thermal

performance. The primary thermal path for the device is the bottom side.

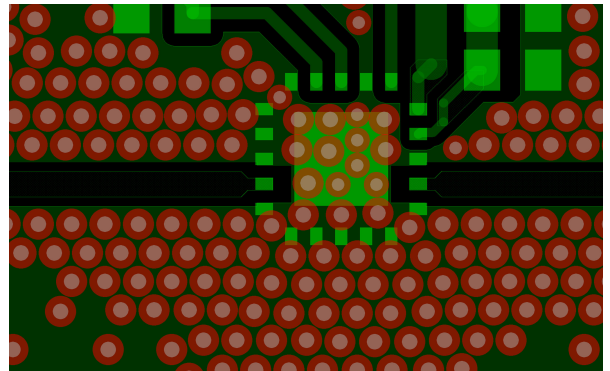


**Figure 23. PCB Routings**

**Figure 24** shows the recommended layout from the AT TIN and ATTOUT pins of the ADRF5716 to the 50  $\Omega$  CPWG on the referenced stackup. The PCB pads are drawn 1:1 to device pads. The ground pads are drawn solder mask defined, and the signal pads are drawn as pad defined. The RF trace from the PCB pad is extended with the same width, 2 mils, and tapered with a 90° angle. The paste mask is also designed to match the pad without any aperture reduction. The paste is divided into multiple openings for the paddle.

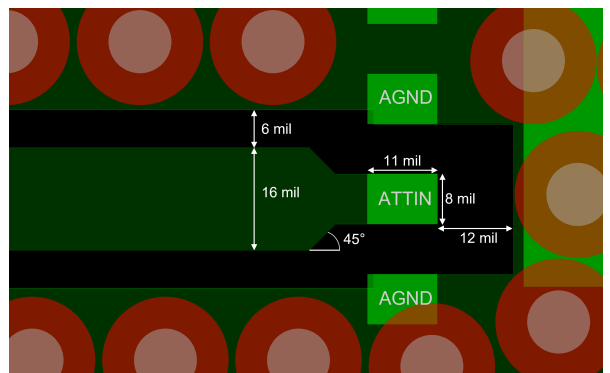


**Figure 24. Recommended ATIN Pin and ATTOUT Pin Transitions**

For alternate PCB stackups with different dielectric thickness and CPWG design, contact [Analog Devices, Inc., Technical Support Request](#) for further recommendations.

## OUTLINE DIMENSIONS

| Package Drawing (Option) | Package Type | Package Description         |
|--------------------------|--------------|-----------------------------|
| CC-20-09                 | LGA          | 20-Terminal Land Grid Array |

For the latest package outline information and land patterns (footprints), go to [Package Index](#).

Updated: May 02, 2024

## ORDERING GUIDE

| Model <sup>1</sup> | Temperature Range | Package Description     | Packing Quantity | Package Option |
|--------------------|-------------------|-------------------------|------------------|----------------|
| ADRF5716BCCZN      | -40°C to +105°C   | 20-lead LGA (3mm × 3mm) | Cut Tape, 500    | CC-20-9        |
| ADRF5716BCCZN-R7   | -40°C to +105°C   | 20-lead LGA (3mm × 3mm) | Cut Tape, 500    | CC-20-9        |

<sup>1</sup> Z = RoHS Compliant Part.

## EVALUATION BOARDS

| Model <sup>1</sup> | Description      |
|--------------------|------------------|
| ADRF5716-EVALZ     | Evaluation Board |

<sup>1</sup> Z = RoHS Compliant Part.

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