Dual, 16-Bit, 125 MSPS Serial LVDS, 1.8 V Analog-to-Digital Converter

Data Sheet **AD9655**

FEATURES

1.8 V supply operation
Low power: approximately 150 mW/channel at 125 MSPS, 2 V p-p input range (typical)
SNR/SFDR at 69.5 MHz
- **77.5 dBFS/88 dBc, 2.0 V p-p input range (typical)**
- **79.3 dBFS/84 dBc, 2.8 V p-p input range (typical)**

Linearity
- **DNL = ±0.7 LSB; INL = ±4.0 LSB (typical, 2.0 V p-p input span)**
- **DNL = ±0.7 LSB; INL = ±3.4 LSB (typical, 2.8 V p-p input span)**

Serial LVDS, two data lanes per ADC channel
500 MHz full power analog bandwidth
Serial port control
- **Full chip and individual channel power-down modes**
- **Flexible bit orientation**
- **Built-in and custom digital test pattern generation**
- **Clock divider**
- **Programmable output clock and data alignment**
- **Standby mode**

APPLICATIONS

Communications
Diversity radio systems
Multimode digital receivers
- **GSM, EDGE, W-CDMA, LTE, CDMA2000, WiMAX, TD-SCDMA**

I/Q demodulation systems
Smart antenna systems
Broadband data applications
Battery-powered instruments
Handheld scope meters
Portable medical imaging and ultrasound
Radar/LIDAR

GENERAL DESCRIPTION

The AD9655 is a dual, 16-bit, 125 MSPS analog-to-digital converter (ADC) with an on-chip sample-and-hold circuit designed for low cost, low power, small size, and ease of use. The product operates at a conversion rate of up to 125 MSPS and is optimized for outstanding dynamic performance and low power in applications where a small package size is critical.

The ADC requires a single 1.8 V power supply and an LVPECL-/CMOS-/LVDS-compatible sample rate clock for full performance operation. External reference or driver components are not required for many applications.

The ADC automatically multiplies the sample rate clock for the appropriate LVDS serial data rate. A data clock output (DCO) for capturing data on the output and a frame clock output (FCO) for signaling a new output byte are provided.

FUNCTIONAL BLOCK DIAGRAM

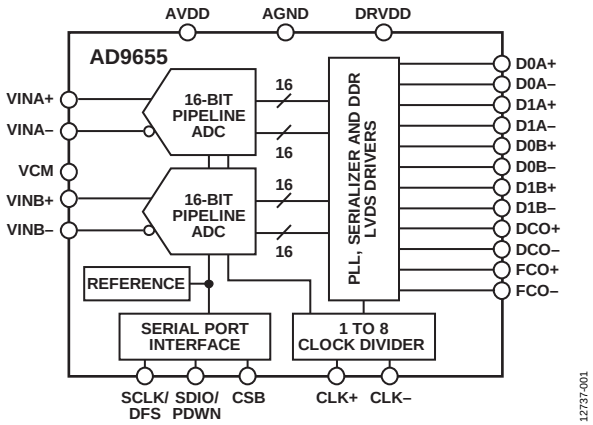

Figure 1.

Individual channel power-down is supported. The AD9655 typically consumes less than 2 mW in serial port interface (SPI) power-down mode. The available digital test pat-terns include built-in deterministic and pseudorandom patterns, along with custom user-defined test patterns entered via the SPI.

The AD9655 is available in an RoHS-compliant, 32-lead LFCSP. It is specified over the industrial temperature range of −40°C to +85°C. This device is protected by a U.S. patent.

PRODUCT HIGHLIGHTS

1. Small Footprint.
   Two ADCs are contained in a small, space-saving package.
2. Pin Compatible.
   The AD9655 is pin compatible to the AD9645 14-bit and AD9635 12-bit dual ADCs.
3. Ease of Use.
   A DCO operates at frequencies of up to 500 MHz and supports double data rate (DDR) operation.
4. User Flexibility.
   The SPI control offers a wide range of flexible features to meet specific system requirements.

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REVISION HISTORY

1/15—Revision 0: Initial Version

SPECIFICATIONS

DC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, 2 V p-p full-scale differential input mode, internal reference voltage (V_{REF}) = 1.0 V, input amplitude (A_{IN}) = −1.0 dBFS, 125 MSPS, unless otherwise noted.

Table 1.

Parameter[1]	Temperature	Min	Typ	Max	Unit
RESOLUTION		16			Bits
ACCURACY					
No Missing Codes	Full		Guaranteed[2]		
Offset Error	25°C		0.2		% FSR
Offset Matching	25°C		0.1		% FSR
Gain Error	25°C		3.4		% FSR
Gain Matching	25°C		0.4		% FSR
Differential Nonlinearity (DNL)	25°C		±0.7		LSB
Integral Nonlinearity (INL)	25°C		±4.0		LSB
TEMPERATURE DRIFT					
Gain Error	Full		−23		ppm/°C
Offset Error	Full		0.9		ppm/°C
INTERNAL VOLTAGE REFERENCE					
Output Voltage (1 V Mode)	25°C		1.0		V
Load Regulation at 1.0 mA (V_{REF} = 1 V)	25°C		2.9		mV
Input Resistance	25°C		7.5		kΩ
INPUT-REFERRED NOISE					
V_{REF} = 1.0 V	25°C		2.7		LSB rms
ANALOG INPUTS					
Differential Input Voltage (V_{REF} = 1 V)	Full		2		V p-p
Common-Mode Voltage	Full		0.9		V
Common-Mode Range	25°C	0.5		1.2	V
Differential Input Resistance	25°C		1.9		kΩ
Differential Input Capacitance	25°C		6.6		pF
POWER SUPPLY					
AVDD	Full	1.7	1.8	1.9	V
DRVDD	Full	1.7	1.8	1.9	V
I_{AVDD}[3]	25°C		93		mA
I_{DRVDD} (ANSI-644 Mode)[3]	25°C		73		mA
I_{DRVDD} (Reduced Range Mode)[3]	25°C		62		mA
TOTAL POWER CONSUMPTION					
Sine Wave Input (Two Channels, Including Output Drivers ANSI-644 Mode)	25°C		299		mW
Sine Wave Input (Two Channels, Including Output Drivers Reduced Range Mode)	25°C		279		mW
Power-Down	25°C		2		mW
Standby[4]	25°C		142		mW

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.
[2] No missing codes guaranteed if Register 0x18 = 0x04 (default, no digital scaling of the output).
[3] Measured with a low input frequency, −1 dBFS sine wave on both channels, DDR operation, and two-lane operation.
[4] Standby mode can be controlled via the SPI.

AVDD = 1.8 V, DRVDD = 1.8 V, 2.8 V p-p full-scale differential input mode, V_{REF} = 1.4 V, A_{IN} = −1.0 dBFS, 125 MSPS, unless otherwise noted.

Table 2.

Parameter[1]	Temperature	Min	Typ	Max	Unit
RESOLUTION		16			Bits
ACCURACY					
No Missing Codes	Full		Guaranteed[2]		
Offset Error	Full	−0.12	+0.2	+0.48	% FSR
Offset Matching	Full	−0.2	+0.1	+0.33	% FSR
Gain Error	Full	−2.4	+2.8	+8.2	% FSR
Gain Matching	Full	−1.2	+0.4	+1.9	% FSR
Differential Nonlinearity (DNL)	Full	−0.99		+1.43	LSB
	25°C		±0.7		LSB
Integral Nonlinearity (INL)	Full	−8.5		+8.5	LSB
	25°C		±3.4		LSB
TEMPERATURE DRIFT					
Gain Error	Full		−66		ppm/°C
Offset Error	Full		0.9		ppm/°C
INTERNAL VOLTAGE REFERENCE					
Output Voltage (1.4 V Mode)	Full	1.37	1.38	1.41	V
Load Regulation at 1.0 mA (V_{REF} = 1.4 V)	25°C		186		mV
Input Resistance	25°C		7.5		kΩ
INPUT-REFERRED NOISE					
V_{REF} = 1.4 V	25°C		2		LSB rms
ANALOG INPUTS					
Differential Input Voltage (V_{REF} = 1.4 V)	Full		2.8		V p-p
Common-Mode Voltage	Full		0.9		V
Common-Mode Range	25°C	0.7		1.0	V
Differential Input Resistance	25°C		1.9		kΩ
Differential Input Capacitance	25°C		6.6		pF
POWER SUPPLY					
AVDD	Full	1.7	1.8	1.9	V
DRVDD	Full	1.7	1.8	1.9	V
I_{AVDD}[3]	Full		101	111	mA
I_{DRVDD} (ANSI-644 Mode)[3]	Full		73	79	mA
I_{DRVDD} (Reduced Range Mode)[3]	Full		62	68	mA
TOTAL POWER CONSUMPTION					
Sine Wave Input (Two Channels, Including Output Drivers ANSI-644 Mode)	Full		313	342	mW
Sine Wave Input (Two Channels, Including Output Drivers Reduced Range Mode)	Full		293	322	mW
Power-Down	Full		2	4	mW
Standby[4]	Full		155	172	mW

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.
[2] No missing codes guaranteed if Register 0x18 = 0x04 (default, no digital scaling of the output).
[3] Measured with a low input frequency, −1 dBFS sine wave on both channels, DDR operation, and two-lane operation.
[4] Standby mode can be controlled via the SPI.

AC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, 2 V p-p full-scale differential input mode, V_{REF} = 1.0 V, A_{IN} = −1.0 dBFS, 125 MSPS, unless otherwise noted.

Table 3.

Parameter[1]	Temperature	Min	Typ	Max	Unit
SIGNAL-TO-NOISE RATIO (SNR)					
f_{IN} = 9.7 MHz	25°C		77.9		dBFS
f_{IN} = 19.7 MHz	25°C		77.9		dBFS
f_{IN} = 69.5 MHz	25°C		77.5		dBFS
f_{IN} = 100.5 MHz	25°C		76.6		dBFS
f_{IN} = 139.5 MHz	25°C		75.6		dBFS
f_{IN} = 301 MHz	25°C		71.0		dBFS
SIGNAL-TO-NOISE-AND-DISTORTION RATIO (SINAD)					
f_{IN} = 9.7 MHz	25°C		77.5		dBFS
f_{IN} = 19.7 MHz	25°C		77.1		dBFS
f_{IN} = 69.5 MHz	25°C		77.1		dBFS
f_{IN} = 100.5 MHz	25°C		76.5		dBFS
f_{IN} = 139.5 MHz	25°C		75.2		dBFS
f_{IN} = 301 MHz	25°C		68.0		dBFS
EFFECTIVE NUMBER OF BITS (ENOB)					
f_{IN} = 9.7 MHz	25°C		12.6		Bits
f_{IN} = 19.7 MHz	25°C		12.5		Bits
f_{IN} = 69.5 MHz	25°C		12.5		Bits
f_{IN} = 100.5 MHz	25°C		12.4		Bits
f_{IN} = 139.5 MHz	25°C		12.2		Bits
f_{IN} = 301 MHz	25°C		11		Bits
SPURIOUS-FREE DYNAMIC RANGE (SFDR)					
f_{IN} = 9.7 MHz	25°C		88		dBc
f_{IN} = 19.7 MHz	25°C		86		dBc
f_{IN} = 69.5 MHz	25°C		88		dBc
f_{IN} = 100.5 MHz	25°C		91		dBc
f_{IN} = 139.5 MHz	25°C		85		dBc
f_{IN} = 301 MHz	25°C		70		dBc
WORST HARMONIC (SECOND OR THIRD)					
f_{IN} = 9.7 MHz	25°C		−88		dBc
f_{IN} = 19.7 MHz	25°C		−86		dBc
f_{IN} = 69.5 MHz	25°C		−88		dBc
f_{IN} = 100.5 MHz	25°C		−91		dBc
f_{IN} = 139.5 MHz	25°C		−85		dBc
f_{IN} = 301 MHz	25°C		−70		dBc
WORST OTHER (EXCLUDING SECOND OR THIRD HARMONIC)					
f_{IN} = 9.7 MHz	25°C		−95		dBc
f_{IN} = 19.7 MHz	25°C		−99		dBc
f_{IN} = 69.5 MHz	25°C		−92		dBc
f_{IN} = 100.5 MHz	25°C		−91		dBc
f_{IN} = 139.5 MHz	25°C		−89		dBc
f_{IN} = 301 MHz	25°C		−80		dBc
TWO-TONE INTERMODULATION DISTORTION (IMD)—A_{IN1} AND A_{IN2} = −7.0 dBFS					
f_{IN1} = 100.1 MHz, f_{IN2} = 102.1 MHz	25°C		90		dBc
CROSSTALK[2]	25°C		−104		dB
CROSSTALK (OVERRANGE CONDITION)[3]	25°C		−100		dB
ANALOG INPUT BANDWIDTH, FULL POWER	25°C		500		MHz

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.
[2] Crosstalk is measured at 69.5 MHz with −1.0 dBFS analog input on one channel and no input on the adjacent channel. Measurements are taken using a less dense board to demonstrate the AD9655 crosstalk performance, not board limitations.
[3] Overrange condition is specified as being 3 dB above the full-scale input range.

AVDD = 1.8 V, DRVDD = 1.8 V, 2.8 V p-p full-scale differential input mode, V_{REF} = 1.4 V, A_{IN} = −1.0 dBFS, 125 MSPS, unless otherwise noted.

Table 4.

Parameter[1]	Temperature	Min	Typ	Max	Unit
SIGNAL-TO-NOISE RATIO (SNR)					
f_{IN} = 9.7 MHz	25°C		79.6		dBFS
f_{IN} = 19.7 MHz	25°C		79.4		dBFS
f_{IN} = 69.5 MHz	Full	78.0	79.3		dBFS
f_{IN} = 100.5 MHz	25°C		78.0		dBFS
f_{IN} = 139.5 MHz	25°C		76.5		dBFS
f_{IN} = 301 MHz	25°C		55.0		dBFS
SIGNAL-TO-NOISE-AND-DISTORTION RATIO (SINAD)					
f_{IN} = 9.7 MHz	25°C		79.1		dBFS
f_{IN} = 19.7 MHz	25°C		78.3		dBFS
f_{IN} = 69.5 MHz	Full	77.2	77.8		dBFS
f_{IN} = 100.5 MHz	25°C		77.0		dBFS
f_{IN} = 139.5 MHz	25°C		75.8		dBFS
f_{IN} = 301 MHz	25°C		54.8		dBFS
EFFECTIVE NUMBER OF BITS (ENOB)					
f_{IN} = 9.7 MHz	25°C		12.8		Bits
f_{IN} = 19.7 MHz	25°C		12.7		Bits
f_{IN} = 69.5 MHz	Full	12.5	12.6		Bits
f_{IN} = 100.5 MHz	25°C		12.5		Bits
f_{IN} = 139.5 MHz	25°C		12.3		Bits
f_{IN} = 301 MHz	25°C		8.8		Bits
SPURIOUS-FREE DYNAMIC RANGE (SFDR)					
f_{IN} = 9.7 MHz	25°C		88		dBc
f_{IN} = 19.7 MHz	25°C		85		dBc
f_{IN} = 69.5 MHz	Full	80	84		dBc
f_{IN} = 100.5 MHz	25°C		83		dBc
f_{IN} = 139.5 MHz	25°C		82		dBc
f_{IN} = 301 MHz	25°C		68		dBc
WORST HARMONIC (SECOND OR THIRD)					
f_{IN} = 9.7 MHz	25°C		−88		dBc
f_{IN} = 19.7 MHz	25°C		−85		dBc
f_{IN} = 69.5 MHz	Full		−84	−80	dBc
f_{IN} = 100.5 MHz	25°C		−83		dBc
f_{IN} = 139.5 MHz	25°C		−82		dBc
f_{IN} = 301 MHz	25°C		−68		dBc
WORST OTHER (EXCLUDING SECOND OR THIRD HARMONIC)					
f_{IN} = 9.7 MHz	25°C		−97		dBc
f_{IN} = 19.7 MHz	25°C		−98		dBc
f_{IN} = 69.5 MHz	Full		−93	−85	dBc
f_{IN} = 100.5 MHz	25°C		−91		dBc
f_{IN} = 139.5 MHz	25°C		−89		dBc
f_{IN} = 301 MHz	25°C		−72		dBc
TWO-TONE INTERMODULATION DISTORTION (IMD)—A_{IN1} AND A_{IN2} = −7.0 dBFS					
f_{IN1} = 100.1 MHz, f_{IN2} = 102.1 MHz	25°C		85		dBc
CROSSTALK[2]	25°C		−104		dB
CROSSTALK (OVERRANGE CONDITION)[3]	25°C		−103		dB
ANALOG INPUT BANDWIDTH, FULL POWER	25°C		500		MHz

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.
[2] Crosstalk is measured at 69.5 MHz with −1.0 dBFS analog input on one channel and no input on the adjacent channel. Measurements are taken using a less dense board to demonstrate AD9655 crosstalk performance, not board limitations.
[3] Overrange condition is specified as being 3 dB above the full-scale input range.

DIGITAL SPECIFICATIONS

AVDD = 1.8 V and DRVDD = 1.8 V, unless otherwise noted.

Table 5.

Parameter[1]	Temperature	Min	Typ	Max	Unit
CLOCK INPUTS (CLK+, CLK−)					
Logic Compliance			CMOS/LVDS/LVPECL		
Differential Input Voltage[2]	Full	0.2		3.6	V p-p
Input Voltage Range	Full	AGND − 0.2		AVDD + 0.2	V
Input Common-Mode Voltage	Full		0.9		V
Input Resistance (Differential)	25°C		15		kΩ
Input Capacitance	25°C		4		pF
LOGIC INPUTS (SCLK/DFS)					
Logic 1 Voltage	Full	1.2		AVDD + 0.2	V
Logic 0 Voltage	Full	0		0.8	V
Input Resistance	25°C		30		kΩ
Input Capacitance	25°C		2		pF
LOGIC INPUT (CSB)					
Logic 1 Voltage	Full	1.2		AVDD + 0.2	V
Logic 0 Voltage	Full	0		0.8	V
Input Resistance	25°C		26		kΩ
Input Capacitance	25°C		2		pF
LOGIC INPUT (SDIO/PDWN)					
Logic 1 Voltage	Full	1.2		AVDD + 0.2	V
Logic 0 Voltage	Full	0		0.8	V
Input Resistance	25°C		26		kΩ
Input Capacitance	25°C		5		pF
LOGIC OUTPUT (SDIO/PDWN)[3]					
Logic 1 Voltage (I_{OH} = 800 µA)	Full		1.79		V
Logic 0 Voltage (I_{OL} = 50 µA)	Full			0.05	V
DIGITAL OUTPUTS (D0x±, D1x±), ANSI-644					
Logic Compliance			LVDS		
Differential Output Voltage (V_{OD})	Full	±298	±350	±400	mV
Output Offset Voltage (V_{OS})	Full	1.15	1.22	1.30	V
Output Coding (Default)			Twos complement		
DIGITAL OUTPUTS (D0x±, D1x±), LOW POWER, REDUCED SIGNAL OPTION					
Logic Compliance			LVDS		
Differential Output Voltage (V_{OD})	Full	±170	±200	±231	mV
Output Offset Voltage (V_{OS})	Full	1.15	1.22	1.30	V
Output Coding (Default)			Twos complement		

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.
[2] Specified for LVDS and LVPECL only.
[3] Specified for 13 SDIO/PDWN pins sharing the same connection.

SWITCHING SPECIFICATIONS

AVDD = 1.8 V and DRVDD = 1.8 V, unless otherwise noted.

Table 6.

Parameter[1, 2]	Temperature	Min	Typ	Max	Unit
CLOCK[3]					
Input Clock Rate	Full	20		1000	MHz
Conversion Rate	Full	20		125	MSPS
Clock Pulse Width High (t_{EH})	Full	4.00			ns
Clock Pulse Width Low (t_{EL})	Full	4.00			ns
OUTPUT PARAMETERS[3]					
Propagation Delay (t_{PD})[4]	Full	(t_{SAMPLE}/4) + 5	(t_{SAMPLE}/4) + 6.1	(t_{SAMPLE}/4) + 7	ns
Rise Time (t_R)[5] (20% to 80%)	Full		170		ps
Fall Time (t_F)[5] (20% to 80%)	Full		160		ps
FCO Propagation Delay (t_{FCO})[4]	Full	(t_{SAMPLE}/4) + 5	(t_{SAMPLE}/4) + 6.1	(t_{SAMPLE}/4) + 7	ns
DCO Propagation Delay (t_{CPD})[4]	Full		t_{FCO} + (t_{SAMPLE}/16) + 0.2		ns
DCO to Data Delay (t_{DATA})[4, 6]	Full	(t_{SAMPLE}/16) − 500		(t_{SAMPLE}/16) + 100	ps
FCO to DCO Delay (t_{FRAME})[4, 7]	Full	(t_{SAMPLE}/16) + 10		(t_{SAMPLE}/16) + 330	ps
Data to Data Skew	Full		±37	±80	ps
Wake-Up Time (Standby)	25°C		250		ns
Wake-Up Time (Power-Down)[8]	25°C		250		ms
Pipeline Latency	Full		16		Clock cycles
APERTURE					
Aperture Delay (t_A)[9]	25°C		1		ns
Aperture Uncertainty (Jitter, t_J[5, 9])	25°C		80		fs rms
Out-of-Range Recovery Time	25°C		1		Clock cycles

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.
[2] Measured on standard FR-4 material.
[3] The Output parameters can be adjusted via the SPI. The conversion rate is the clock rate after the divider. Valid for 2-lane operation.
[4] $t_{SAMPLE} = t_{EH} + t_{EL} = 1/f_S$. t_{CPD}, t_{DATA} and t_{FRAME} are adjustable with SPI Register 0x16.
[5] This term does not appear in the Timing Diagrams section, which includes Figure 2 and Figure 3.
[6] t_{DATA} is the time from DCO rise or fall to output data rise or fall.
[7] t_{FRAME} is the time from FCO rise to DCO rise.
[8] Wake-up time from power-down is defined as the time required to return to normal operation from SPI power-down mode. The value of 250 ms assumes a sample rate of 125 MSPS. About 31×10^6 sample clock cycles are required.
[9] t_A and t_J are with Register 0x09 = 0x04 (default, duty cycle stabilizer and clock divider are bypassed).

TIMING SPECIFICATIONS

Table 7.

Parameter	Description	Limit	Unit
SPI TIMING REQUIREMENTS	See Figure 68, unless otherwise noted		
t_{DS}	Setup time between the data and the rising edge of SCLK	4	ns min
t_{DH}	Hold time between the data and the rising edge of SCLK	2	ns min
t_{CLK}	Period of the SCLK	40	ns min
t_S	Setup time between CSB and SCLK	2	ns min
t_H	Hold time between CSB and SCLK	2	ns min
t_{HIGH}	SCLK pulse width high	10	ns min
t_{LOW}	SCLK pulse width low	10	ns min
t_{EN_SDIO}[1]	Time required for the SDIO pin to switch from an input to an output relative to the SCLK falling edge	10	ns min
t_{DIS_SDIO}[1]	Time required for the SDIO pin to switch from an output to an input relative to the SCLK rising edge	10	ns min

[1] This parameter is not shown in Figure 68.

Timing Diagrams

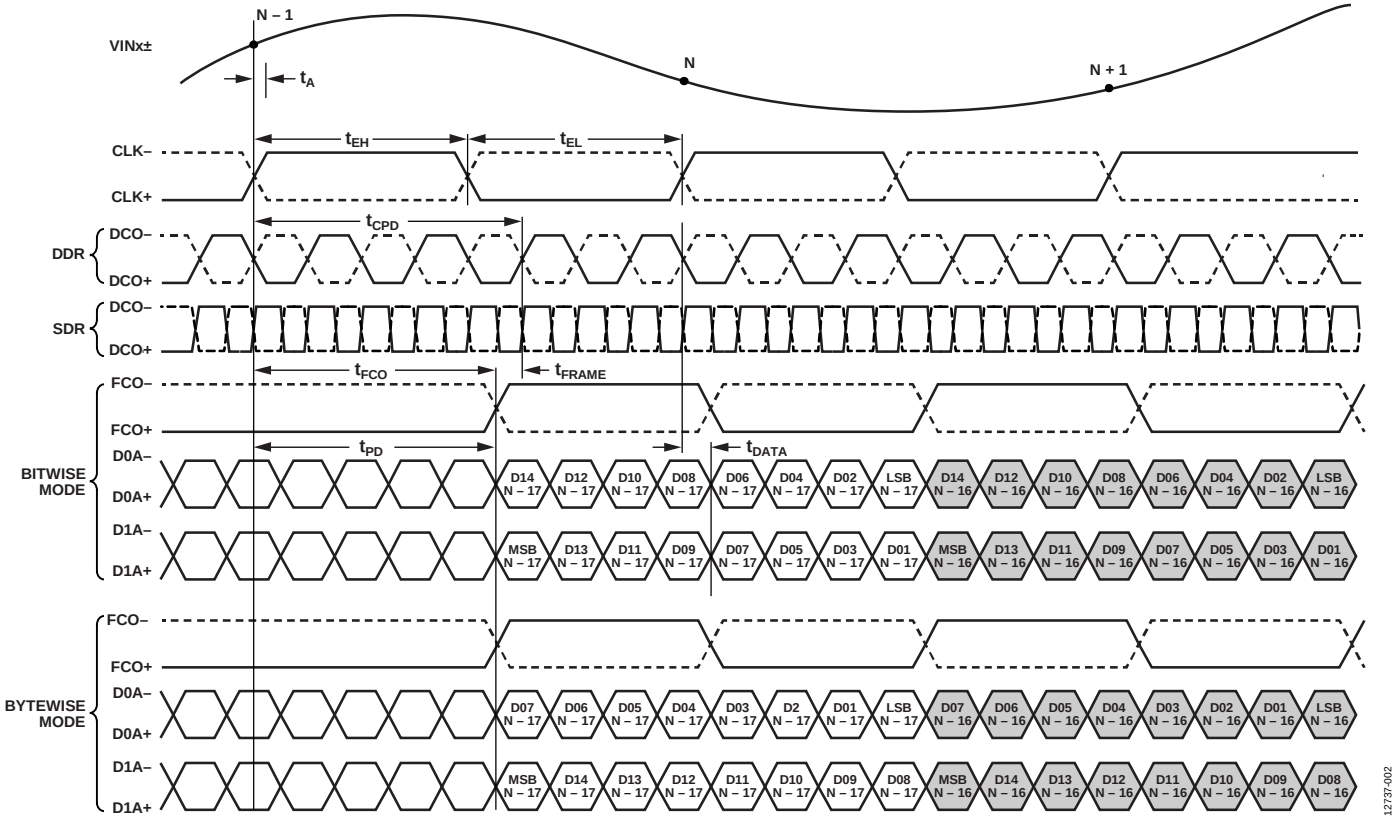


Figure 2. 16-Bit DDR/Single Data Rate (SDR), Two-Lane, 1× Frame Mode (Default)

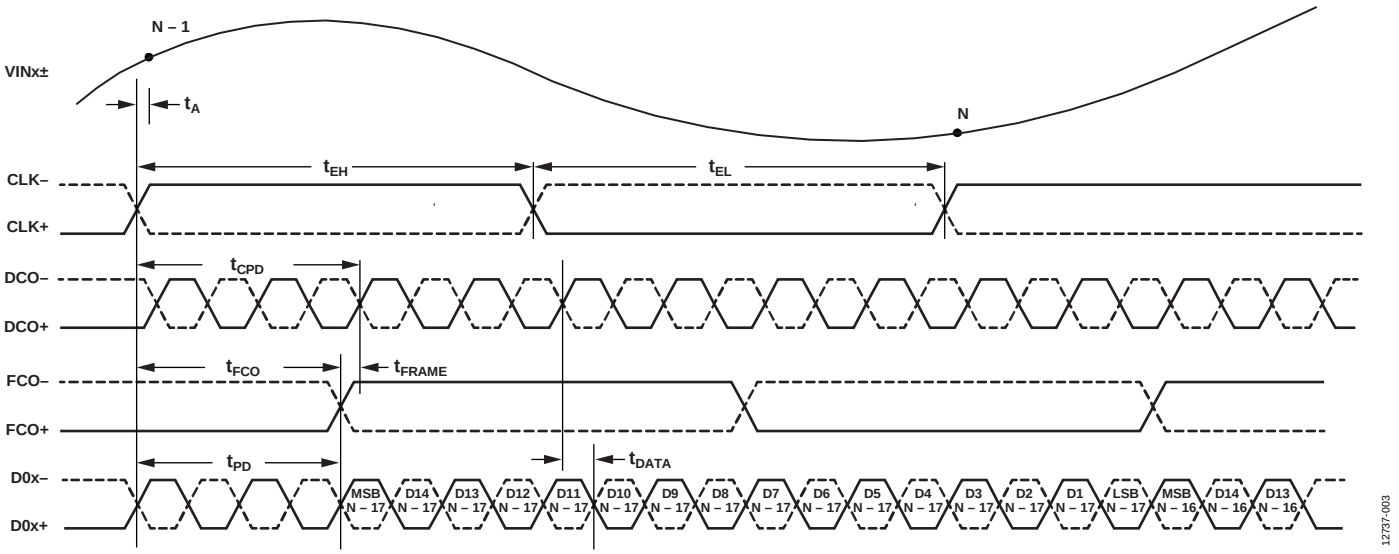


Figure 3. Wordwise DDR, One-Lane, 1× Frame, 16-Bit Output Mode

ABSOLUTE MAXIMUM RATINGS

Table 8.

Parameter	Rating
Electrical	
AVDD to AGND	−0.3 V to +2.0 V
DRVDD to AGND	−0.3 V to +2.0 V
Digital Outputs (D0x±, D1x±, DCO±, FCO±) to AGND	−0.3 V to +2.0 V
CLK+, CLK− to AGND	−0.3 V to +2.0 V
VINx+, VINx− to AGND	−0.3 V to +2.0 V
SCLK/DFS, SDIO/PDWN, CSB to AGND	−0.3 V to +2.0 V
RBIAS to AGND	−0.3 V to +2.0 V
VREF to AGND	−0.3 V to +2.0 V
VCM to AGND	−0.3 V to +2.0 V
Environmental	
Operating Temperature Range (Ambient)	−40°C to +85°C
Maximum Junction Temperature	150°C
Lead Temperature (Soldering, 10 sec)	300°C
Storage Temperature Range (Ambient)	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

The exposed pad is the only ground connection for the chip. The exposed pad must be soldered to the AGND plane of the circuit board. Soldering the exposed pad to the board also increases the reliability of the solder joints and maximizes the thermal capability of the package.

Table 9. Thermal Resistance

Package Type	Airflow Velocity (m/sec)	θ_{JA}[1, 2]	θ_{JC}[1, 3]	θ_{JB}[1, 4]	Ψ_{JT}[1, 2]	Unit
32-Lead LFCSP, 5 mm × 5 mm	0	37.1	3.1	20.7	0.3	°C/W
	1.0	32.4	N/A[5]	N/A[5]	0.5	°C/W
	2.5	29.1	N/A[5]	N/A[5]	0.8	°C/W

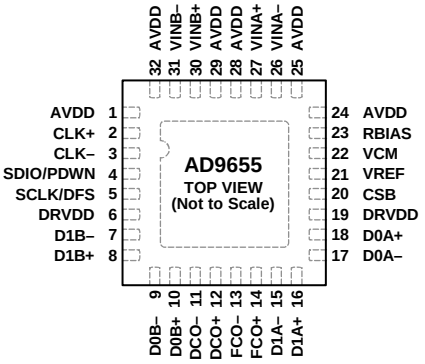
[1] Per JEDEC 51-7, plus JEDEC 51-5 2S2P test board.
[2] Per JEDEC JESD51-2 (still air) or JEDEC JESD51-6 (moving air).
[3] Per MIL-Std 883, Method 1012.1.
[4] Per JEDEC JESD51-8 (still air).
[5] N/A means not applicable.

Typical θ_{JA} is specified for a 4-layer printed circuit board (PCB) with a solid ground plane. As shown in Table 9, airflow improves heat dissipation, which reduces θ_{JA}. In addition, metal in direct contact with the package leads from metal traces, through holes, ground, and power planes reduces θ_{JA}.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. THE EXPOSED PAD IS THE ONLY GROUND CONNECTION ON THE CHIP. IT MUST BE SOLDERED TO THE ANALOG GROUND OF THE PCB TO ENSURE PROPER FUNCTIONALITY AND HEAT DISSIPATION, NOISE, AND MECHANICAL STRENGTH BENEFITS.

Figure 4. Pin Configuration, Top View

Table 10. Pin Function Descriptions

Pin No.	Mnemonic	Description
0, Exposed Pad	AGND, Exposed Pad	Exposed Pad. The exposed pad is the only ground connection on the chip. It must be soldered to the analog ground of the PCB to ensure proper functionality and heat dissipation, noise, and mechanical strength benefits.
1, 24, 25, 28, 29, 32	AVDD	1.8 V Supply Pins for the ADC Core Domain.
2, 3	CLK+, CLK–	Differential Encode Clock. These pins are PECL-, LVDS-, or 1.8 V CMOS-compatible inputs.
4	SDIO/PDWN	SPI Data Input/Output (SDIO). This pin is a bidirectional SPI data input/output with a 31 kΩ internal pull-down resistor.
		Non-SPI Mode Power-Down (PDWN). This pin provides static control of chip power-down, and has a 31 kΩ internal pull-down resistor.
5	SCLK/DFS	SPI Clock Input in SPI Mode (SCLK). This pin has a 30 kΩ internal pull-down resistor.
		Non-SPI Mode Data Format Select (DFS). This provides static control of the data output format. This pin has a 30 kΩ internal pull-down resistor. Pull DFS high for a twos complement output; pull DFS low for an offset binary output.
6, 19	DRVDD	1.8 V Supply Pins for Output Driver Domain.
7, 8	D1B–, D1B+	Channel B Lane 1 Digital Outputs.
9, 10	D0B–, D0B+	Channel B Lane 0 Digital Outputs.
11, 12	DCO–, DCO+	Data Clock Outputs.
13, 14	FCO–, FCO+	Frame Clock Outputs.
15, 16	D1A–, D1A+	Channel A Lane 1 Digital Outputs.
17, 18	D0A–, D0A+	Channel A Lane 0 Digital Outputs.
20	CSB	SPI Chip Select. Active low enable; this pin has a 15 kΩ internal pull-up resistor.
21	VREF	1.0 V to 1.4 V Voltage Reference Output. Bypass this pin to ground with a 1.0 µF capacitor in parallel with a 0.1 µF capacitor; this pin internally provides reference voltage to the ADC. This pin can be disabled via Register 0x114 if external V_{REF} is desired.
22	VCM	Analog Output Voltage at Mid AVDD Supply. Bypass this pin to ground with a 0.1 µF capacitor; this pin can be used to set the common mode of the analog inputs externally.
23	RBIAS	Sets Analog Current Bias. Connect this pin to a 10.0 kΩ (1% tolerance) resistor to ground.
26, 27	VINA–, VINA+	Channel A ADC Analog Inputs.
30, 31	VINB+, VINB–	Channel B ADC Analog Inputs.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{REF} = 1.0 V

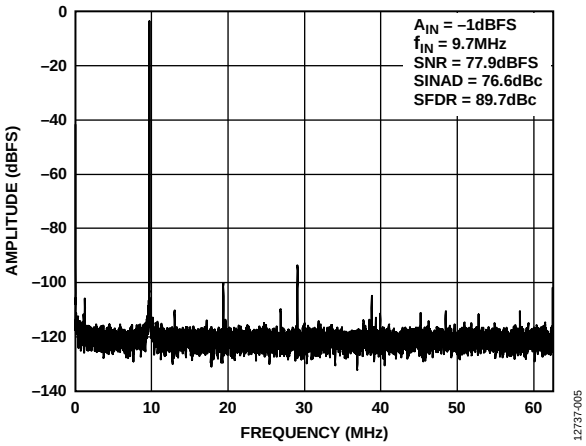


Figure 5. Single-Tone 32k FFT with f_{IN} = 9.7 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.0 V

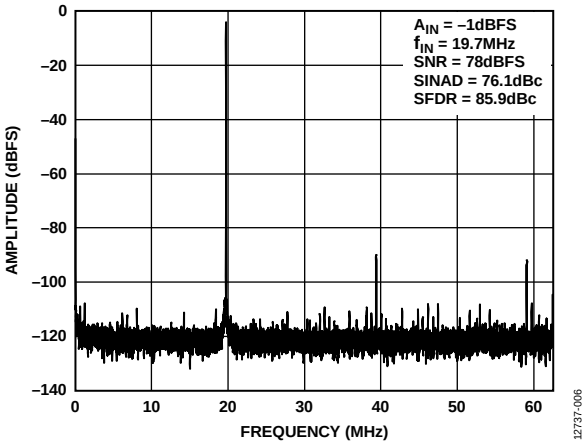


Figure 6. Single-Tone 32k FFT with f_{IN} = 19.7 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.0 V

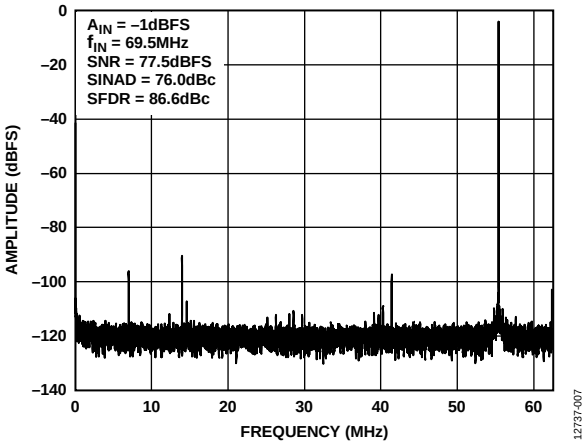


Figure 7. Single-Tone 32k FFT with f_{IN} = 69.5 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.0 V

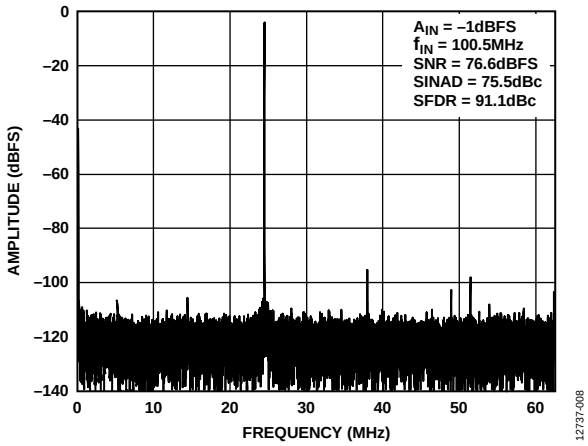


Figure 8. Single-Tone 32k FFT with f_{IN} = 100.5 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.0 V

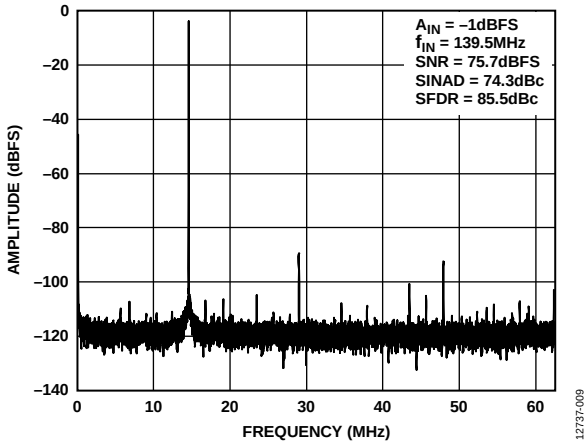


Figure 9. Single-Tone 32k FFT with f_{IN} = 139.5 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.0 V

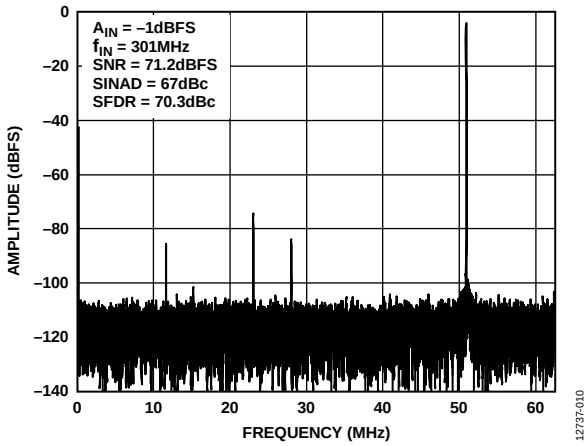


Figure 10. Single-Tone 32k FFT with f_{IN} = 301 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.0 V

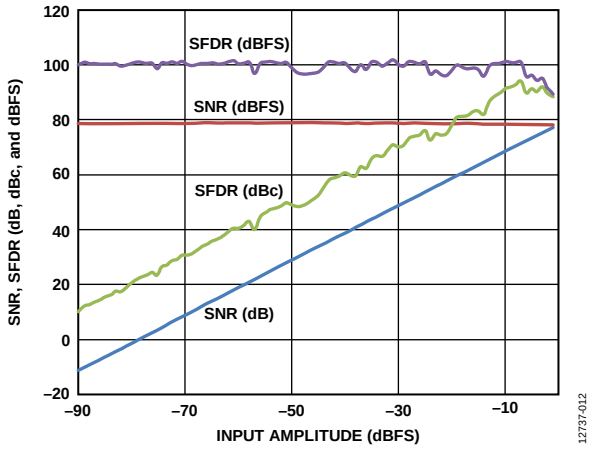


Figure 11. SNR, SFDR vs. Input Amplitude; f_{IN} = 9.7 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.0 V

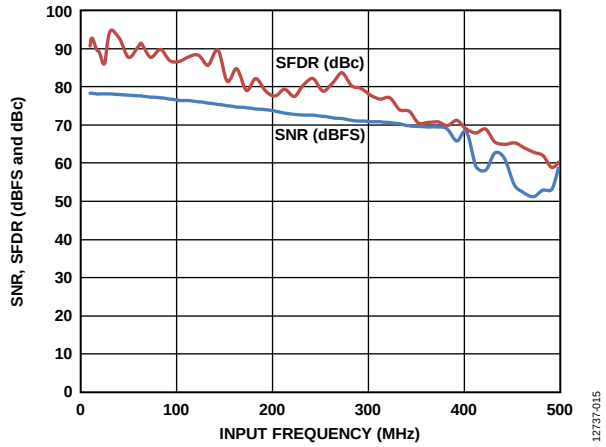


Figure 14. SNR, SFDR vs. Input Frequency (f_{IN}); f_{SAMPLE} = 125 MSPS, V_{REF} = 1.0 V

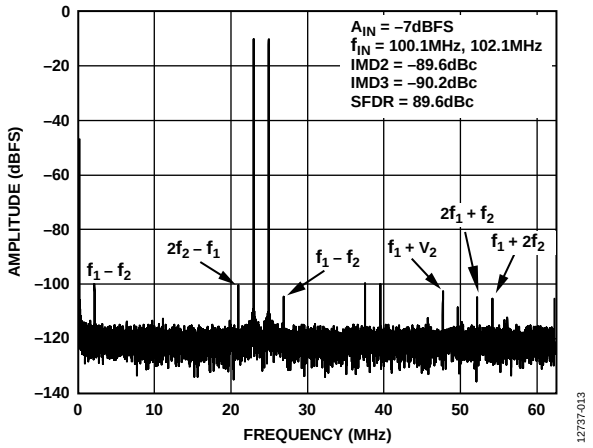


Figure 12. Two-Tone 32k FFT with f_{IN1} = 100.1 MHz and f_{IN2} = 102.1 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.0 V

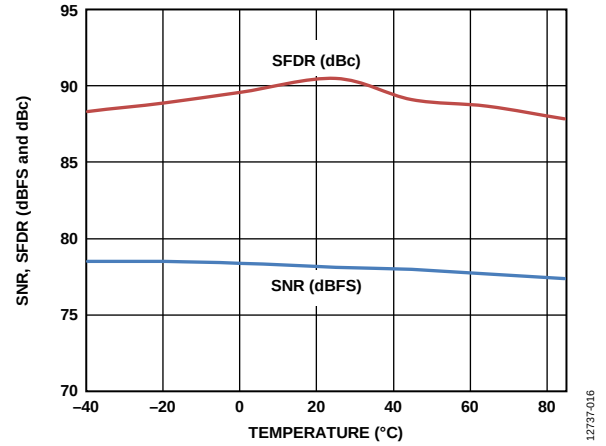


Figure 15. SNR, SFDR vs. Temperature; f_{IN} = 9.7 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.0 V

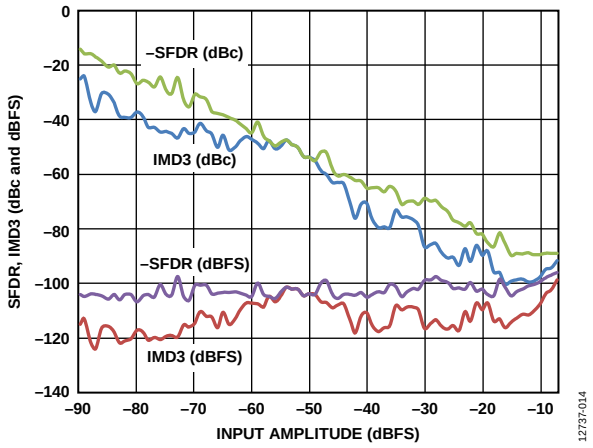


Figure 13. Two-Tone SFDR, IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 100.1 MHz and f_{IN2} = 102.1 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.0 V

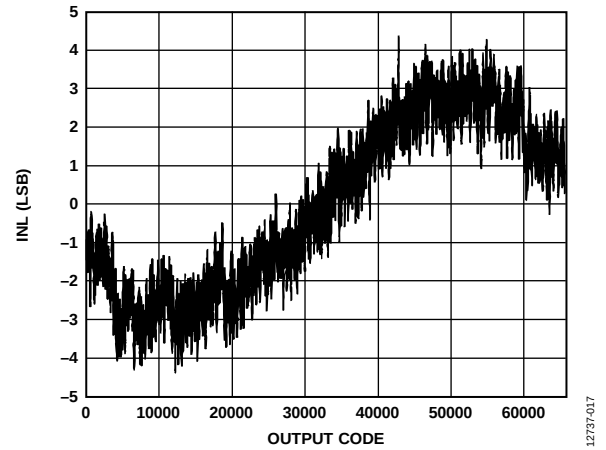


Figure 16. INL; f_{IN} = 9.7 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.0 V

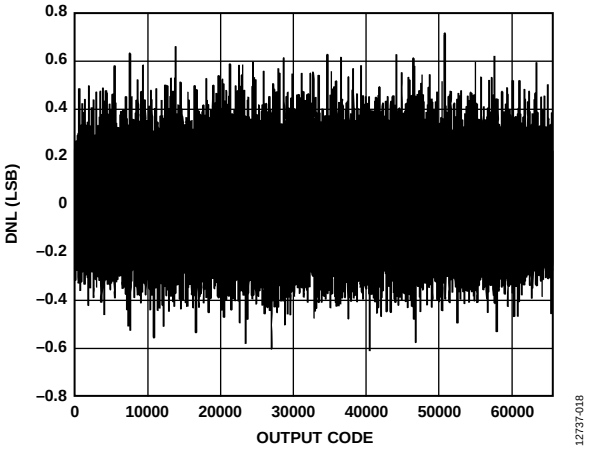


Figure 17. DNL; f_{IN} = 9.7 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.0 V

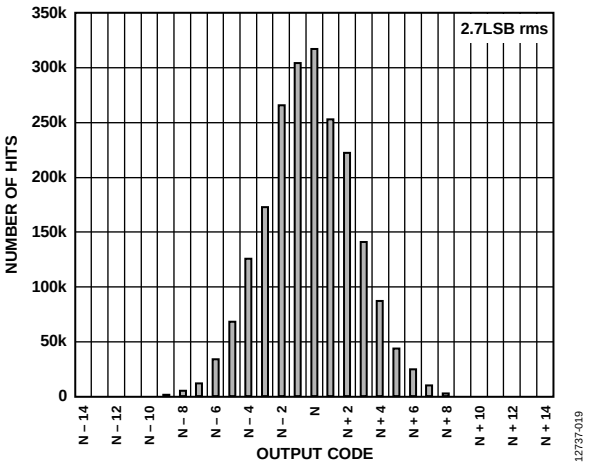


Figure 18. Input Referred Noise Histogram; f_{SAMPLE} = 125 MSPS, V_{REF} = 1.0 V

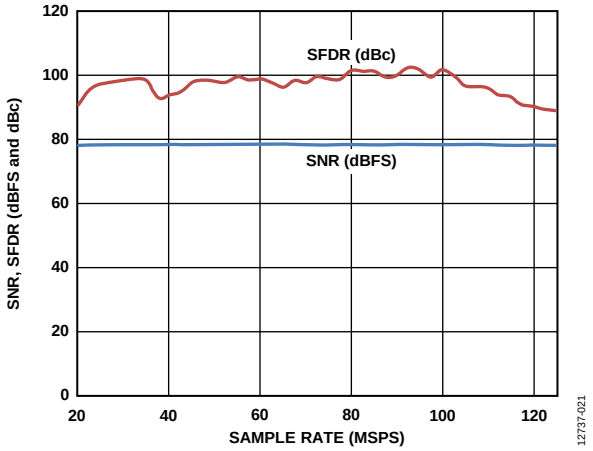


Figure 19. SNR, SFDR vs. Sample Rate; f_{IN} = 9.7 MHz, V_{REF} = 1.0 V

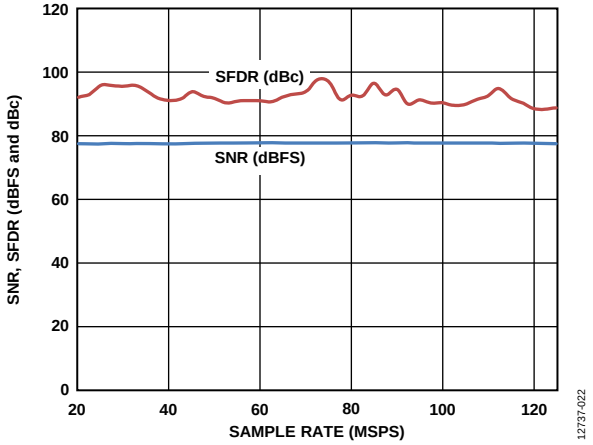


Figure 20. SNR, SFDR vs. Sample Rate; f_{IN} = 69.5 MHz, V_{REF} = 1.0 V, Clock Divider = 4

V_{REF} = 1.4 V

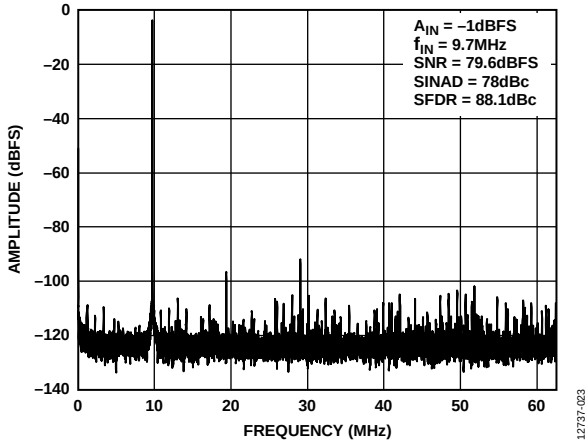


Figure 21. Single-Tone 32k FFT with f_{IN} = 9.7 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.4 V

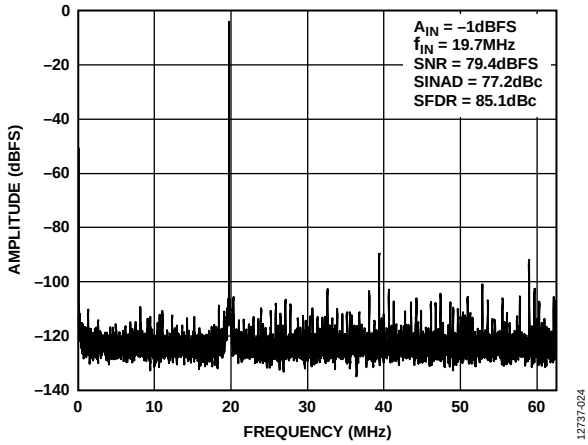


Figure 22. Single-Tone 32k FFT with f_{IN} = 19.7 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.4 V

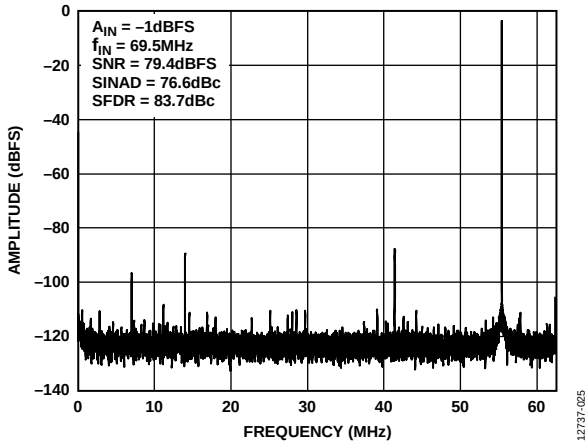


Figure 23. Single-Tone 32k FFT with f_{IN} = 69.5 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.4 V

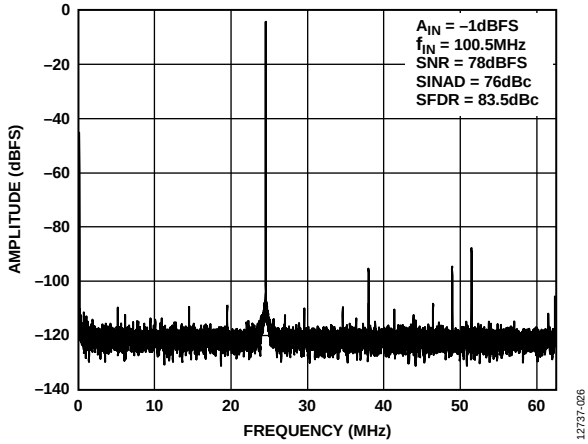


Figure 24. Single-Tone 32k FFT with f_{IN} = 100.5 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.4 V

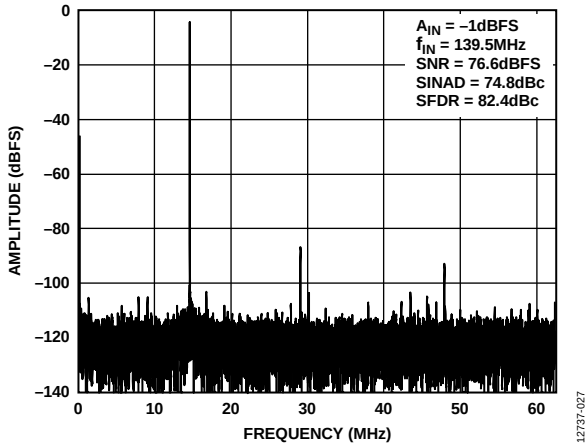


Figure 25. Single-Tone 32k FFT with f_{IN} = 139.5 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.4 V

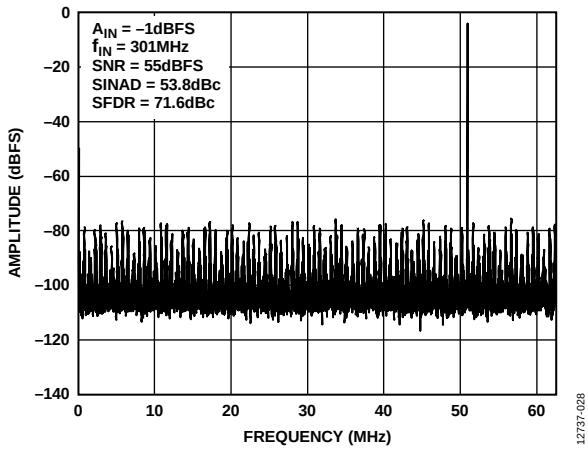


Figure 26. Single-Tone 32k FFT with f_{IN} = 301 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.4 V

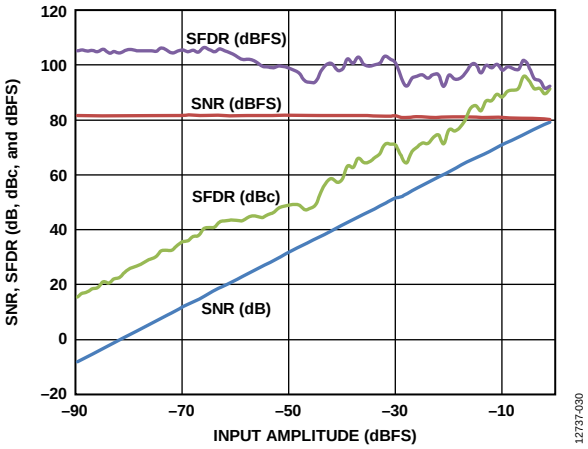


Figure 27. SNR, SFDR vs. Input Amplitude; f_{IN} = 9.7 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.4 V

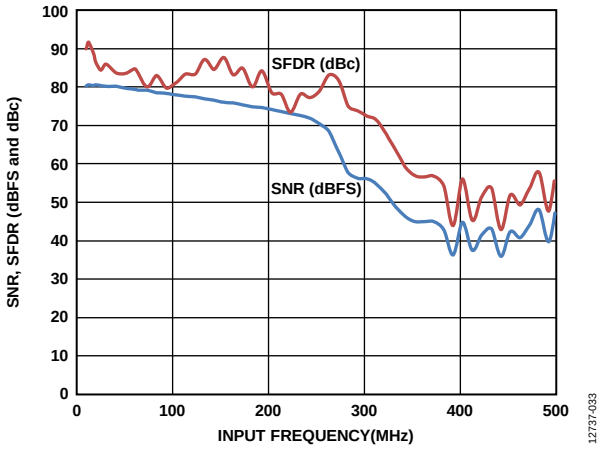


Figure 30. SNR, SFDR vs. Input Frequency (f_{IN}); f_{SAMPLE} = 125 MSPS, V_{REF} = 1.4 V

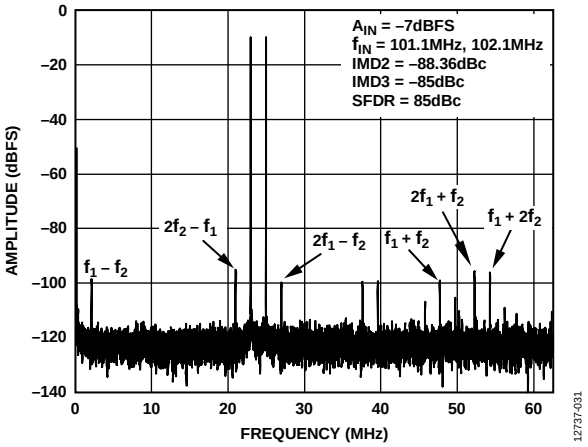


Figure 28. Two-Tone 32k FFT with f_{IN1} = 100.1 MHz and f_{IN2} = 102.1 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.4 V

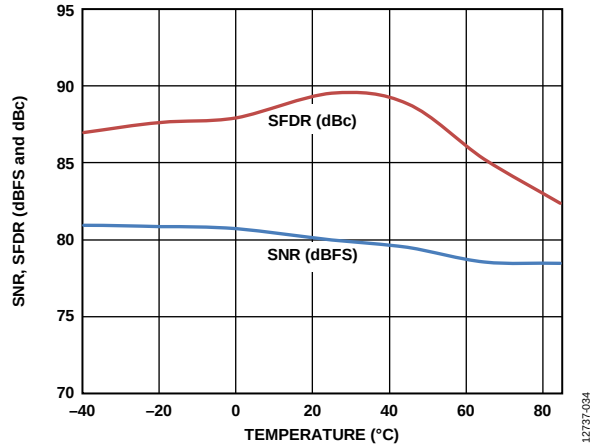


Figure 31. SNR, SFDR vs. Temperature; f_{IN} = 9.7 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.4 V

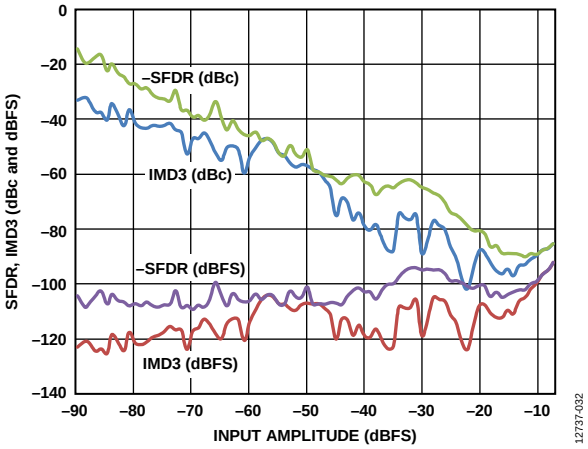


Figure 29. Two-Tone SFDR, IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 100.1 MHz and f_{IN2} = 102.1 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.4 V

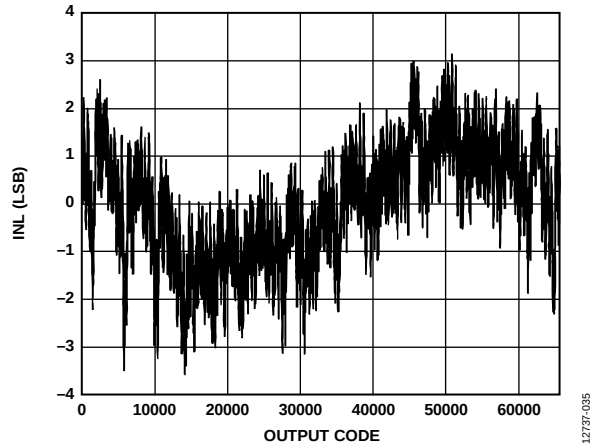


Figure 32. INL; f_{IN} = 9.7 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.4 V

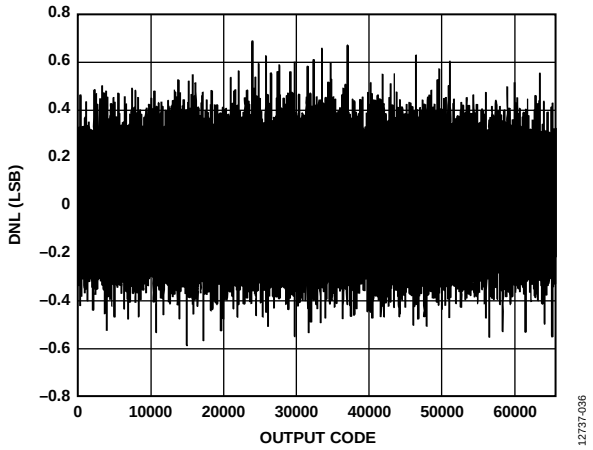


Figure 33. DNL; f_{IN} = 9.7 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.4 V

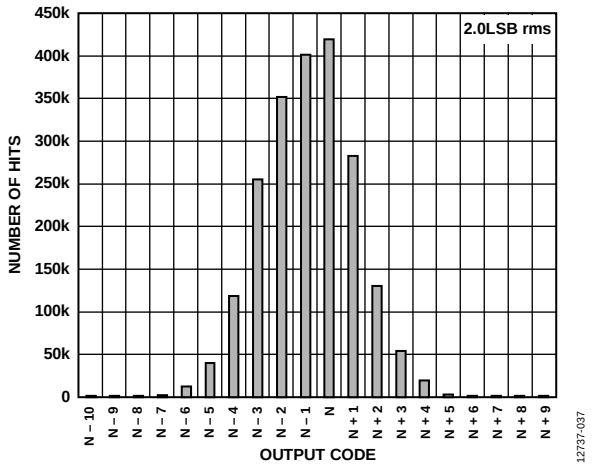


Figure 34. Input Referred Noise Histogram; f_{SAMPLE} = 125 MSPS, V_{REF} = 1.4 V

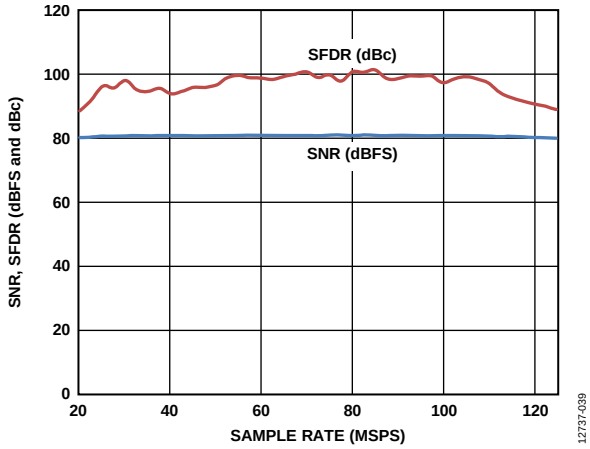


Figure 35. SNR, SFDR vs. Sample Rate; f_{IN} = 9.7 MHz, V_{REF} = 1.4 V

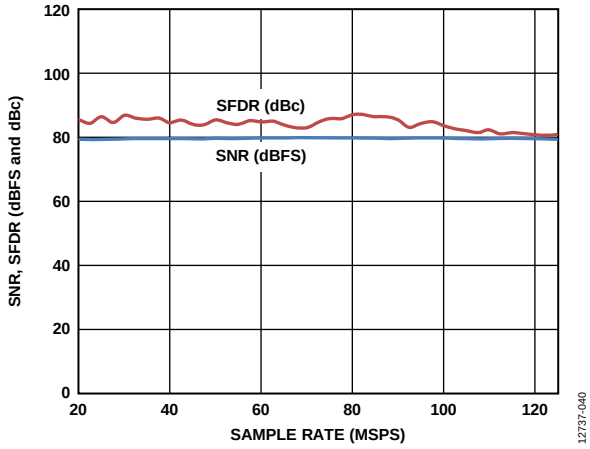


Figure 36. SNR, SFDR vs. Sample Rate; f_{IN} = 69.5 MHz, V_{REF} = 1.4 V, Clock Divider = 4

EQUIVALENT CIRCUITS

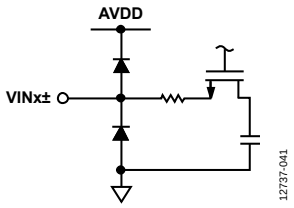


Figure 37. Equivalent Analog Input Circuit

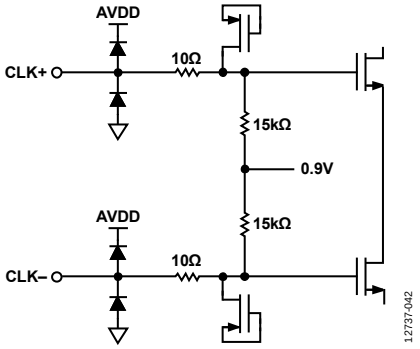


Figure 38. Equivalent Clock Input Circuit

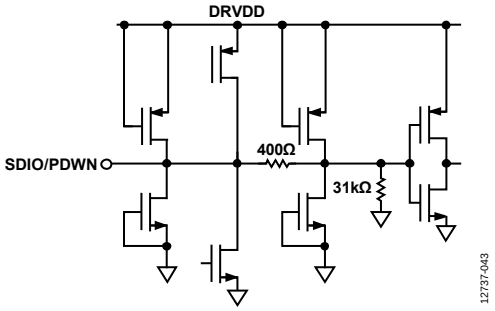


Figure 39. Equivalent SDIO/PDWN Input Circuit

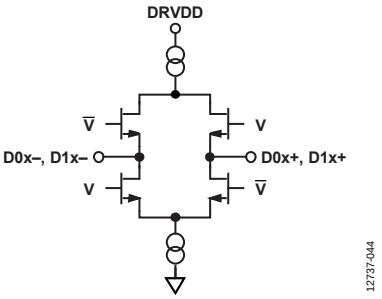


Figure 40. Equivalent Digital Output Circuit

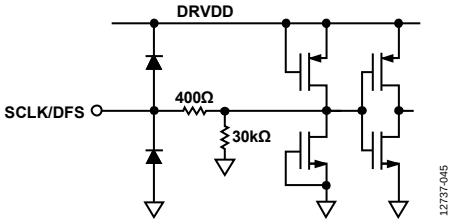


Figure 41. Equivalent SCLK/DFS Input Circuit

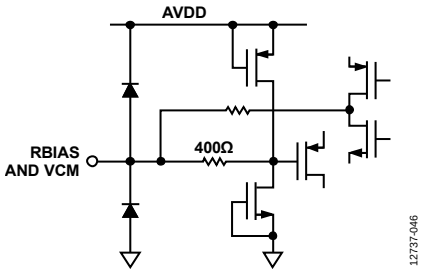


Figure 42. Equivalent RBIAS and VCM Circuit

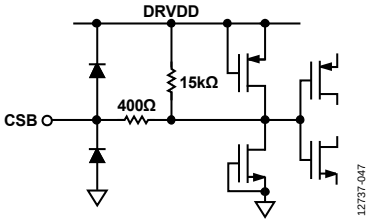


Figure 43. Equivalent CSB Input Circuit

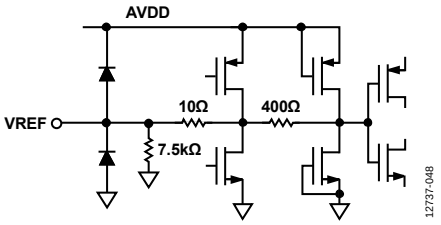


Figure 44. Equivalent VREF Circuit

THEORY OF OPERATION

The AD9655 is a multistage, pipelined ADC. Each stage provides sufficient overlap to correct for flash errors in the preceding stage. The quantized outputs from each stage are combined into a final 16-bit result in the digital correction logic. The serializer transmits this converted data in a 16-bit output. The pipelined architecture permits the first stage to operate with a new input sample while the remaining stages operate with preceding samples. Sampling occurs on the rising edge of the clock.

Each stage of the pipeline, excluding the last, consists of a low resolution flash ADC connected to a switched capacitor DAC and an interstage residue amplifier, for example, a multiplying digital-to-analog converter (MDAC). The residue amplifier magnifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy in each stage facilitates digital correction of flash errors. The last stage consists of a flash ADC.

The output staging block aligns the data, corrects errors, and passes the data to the output buffers. Then, the data is serialized and aligned to the frame and data clocks.

ANALOG INPUT CONSIDERATIONS

The analog input to the AD9655 is a differential switched capacitor circuit designed for processing differential input signals. This circuit can support a wide common-mode range while maintaining excellent performance. By using an input common-mode voltage of midsupply, users can minimize signal dependent errors and achieve optimum performance.

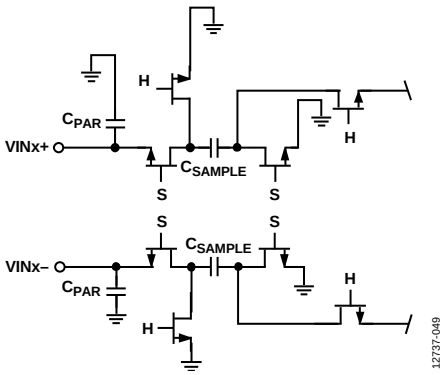


Figure 45. Switched Capacitor Input Circuit

The clock signal alternately switches the input circuit between sample mode and hold mode (see Figure 45). When the input circuit switches to sample mode, the signal source must be capable of charging the sample capacitors and settling within one half of a clock cycle.

A small resistor in series with each input can help reduce the peak transient current injected from the output stage of the driving source. A differential capacitor, two single-ended capacitors, or a combination of these capacitors can be placed on the inputs to provide a matching passive network. This ultimately creates a low-pass filter at the input to limit unwanted broadband noise. See the AN-742 Application Note, the AN-827 Application Note, and the *Analog Dialogue* article "Transformer-Coupled Front-End for Wideband A/D Converters" (Volume 39, April 2005) for more information. In general, the precise values depend on the application.

Input Common Mode

The AD9655 analog inputs are not internally dc-biased. Therefore, in ac-coupled applications, the user must provide this bias externally. Setting the device so that V_{CM} = AVDD/2 is recommended for optimum performance, but the device can function over a wider range with reasonable performance, as shown in Figure 46 and Figure 47.

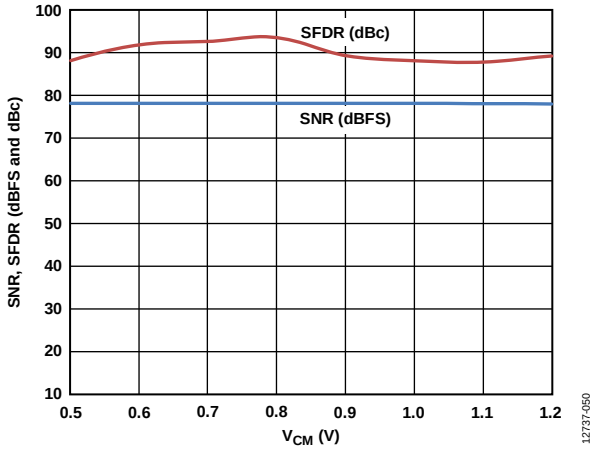


Figure 46. SNR, SFDR vs. Input Common-Mode Voltage (V_{CM}), f_{IN} = 9.7 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.0 V

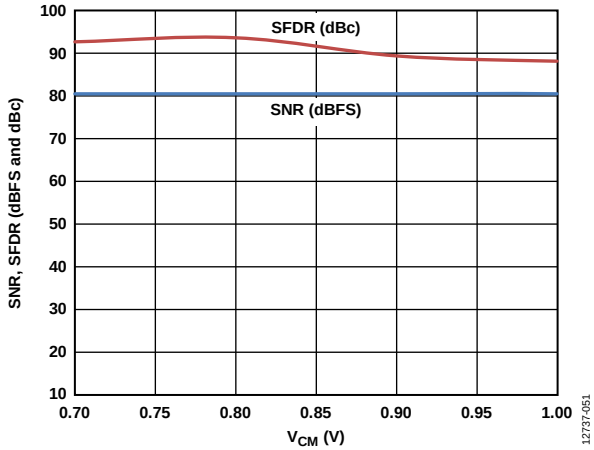


Figure 47. SNR, SFDR vs. Input Common-Mode Voltage (V_{CM}), f_{IN} = 9.7 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.4 V

An on-chip, common-mode dc voltage reference is included in the design and is available from the VCM pin. The VCM pin must be bypassed to ground by a 0.1 µF capacitor, as described in the Applications Information section. VCM error vs. load current is shown in Figure 48.

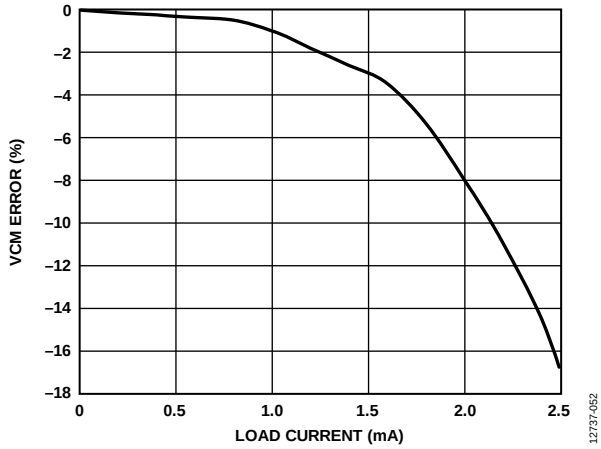


Figure 48. VCM Error vs. Load Current

Differential Input Configurations

There are several ways to drive the AD9655 either actively or passively. However, optimum performance is achieved by driving the analog inputs differentially. Using a differential double balun configuration to drive the AD9655 provides excellent performance and a flexible interface to the ADC for baseband applications (see Figure 53).

For applications where SNR is a key parameter, differential transformer coupling is the recommended input configuration (see Figure 54) because the noise performance of most amplifiers is not adequate to achieve the true performance of the AD9655.

Regardless of the configuration, the value of the shunt capacitor, C, is dependent on the input frequency and may need to be reduced or removed.

It is not recommended to drive the AD9655 inputs single-ended.

VOLTAGE REFERENCE

A stable and accurate 1.0 V to 1.4 V dc voltage reference is built into the AD9655. Externally bypass the VREF pin to ground with a low ESR, 1.0 µF capacitor in parallel with a low ESR, 0.1 µF ceramic capacitor.

Maximum SNR performance is achieved by setting the ADC to the largest span in a differential configuration. In the case of the AD9655, the largest input span available is 2.8 V p-p, which is achieved by setting V_{REF} to 1.4 V.

If the internal reference of the AD9655 is used to drive multiple converters to improve gain matching, the loading of the reference by the other converters must be considered. Figure 49 and Figure 50 show how the internal reference voltage is affected by loading. It is recommended that VREF not be used to drive the reference voltage of other devices at 1.4 V. Figure 51 and Figure 52 show the typical drift characteristics of the internal reference.

The internal buffer generates the positive and negative full-scale references for the ADC core. A digital reset using Register 0x08 must follow any programmatic change in internal analog V_{REF}.

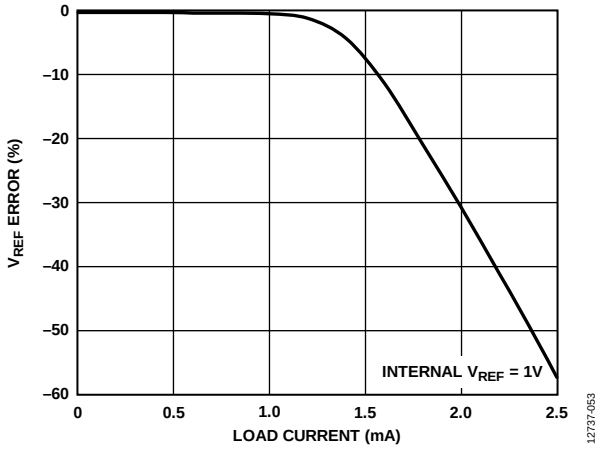


Figure 49. V_{REF} Error vs. Load Current, V_{REF} = 1.0 V

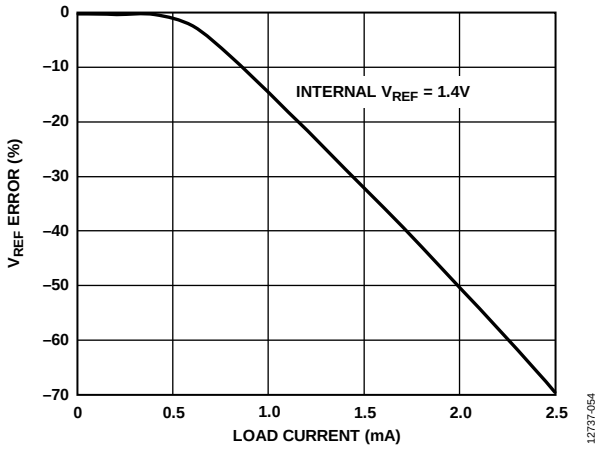


Figure 50. V_{REF} Error vs. Load Current, V_{REF} = 1.4 V

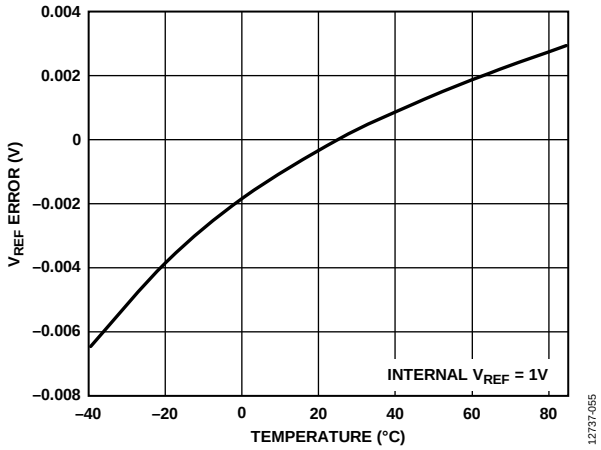


Figure 51. Typical V_{REF} Drift, V_{REF} = 1.0 V

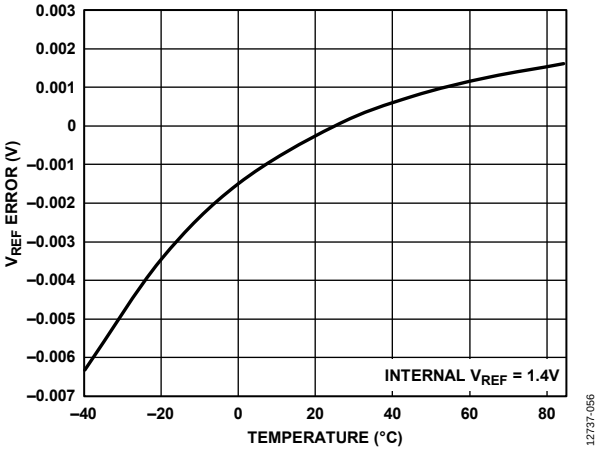


Figure 52. Typical V_{REF} Drift, V_{REF} = 1.4 V

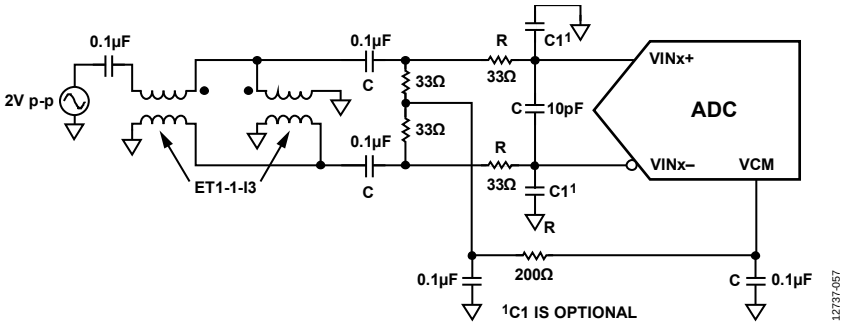


Figure 53. Differential Double Balun Input Configuration for Baseband Applications

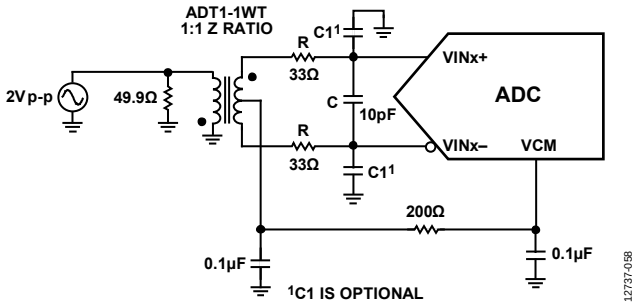


Figure 54. Differential Transformer Coupled Configuration for Baseband Applications

CLOCK INPUT CONSIDERATIONS

For optimum performance, clock the AD9655 sample clock inputs, CLK+ and CLK−, with a differential signal. The signal is typically ac-coupled into the CLK+ and CLK− pins via a transformer or capacitors. These pins are biased internally (see Figure 38) and require no external bias.

Clock Input Options

The AD9655 has a flexible clock input structure. The clock input can be a CMOS, LVDS, LVPECL, or sine wave signal. Regardless of the type of signal used, clock source jitter is an important consideration, as described in the Jitter Considerations section.

Figure 55 and Figure 56 show two preferred methods for clocking the AD9655 at clock rates up to 1 GHz prior to the internal clock divider. A low jitter clock source is converted from a single-ended signal to a differential signal using either a radio frequency (RF) transformer or an RF balun.

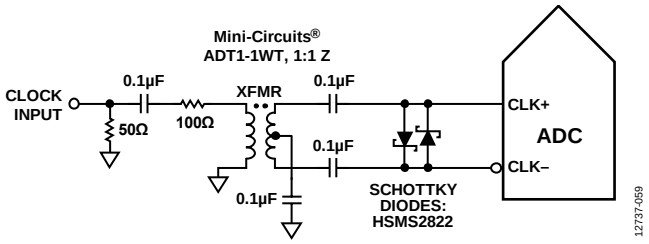


Figure 55. Transformer Coupled Differential Clock (Up to 200 MHz)

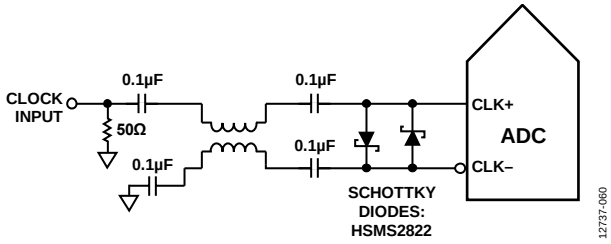


Figure 56. Balun-Coupled Differential Clock (Up to 1 GHz)

The RF balun configuration is recommended for clock frequencies between 125 MHz and 1 GHz, and the RF transformer configuration is recommended for clock frequencies from 20 MHz to 200 MHz. The antiparallel Schottky diodes across the transformer/balun secondary winding limit clock excursions into the AD9655 to approximately 0.8 V p-p differential.

This limit helps prevent the large voltage swings of the clock from feeding through to other portions of the AD9655 while preserving the fast rise and fall times of the signal that are critical to achieving low jitter performance. However, the diode capacitance comes into play at frequencies above 500 MHz. Care must be taken when choosing the appropriate signal limiting diode.

If a low jitter clock source is not available, another option is to ac couple a differential PECL signal to the sample clock input pins, as shown in Figure 57. The AD9510/AD9511/AD9512/AD9513/AD9514/AD9515/AD9516/AD9517 clock drivers, noted as AD951x in Figure 57, Figure 58, and Figure 59, offer excellent jitter performance.

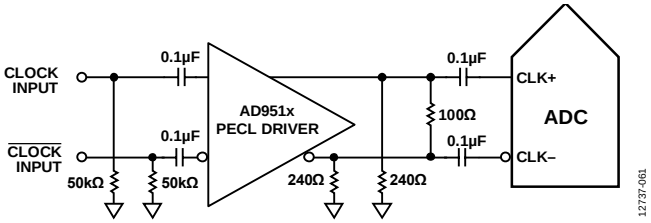


Figure 57. Differential PECL Sample Clock (Up to 1 GHz)

A third option is to ac couple a differential LVDS signal to the sample clock input pins, as shown in Figure 58. The AD9510/AD9511/AD9512/AD9513/AD9514/AD9515/AD9516/AD9517 clock drivers offer excellent jitter performance.

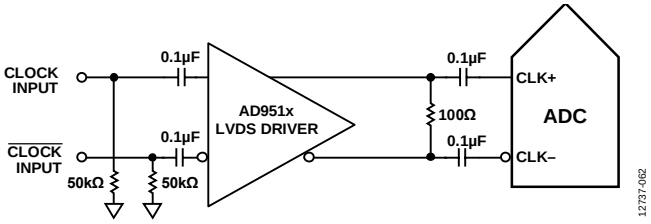


Figure 58. Differential LVDS Sample Clock (Up to 1 GHz)

In some applications, it may be acceptable to drive the sample clock inputs with a single-ended 1.8 V CMOS signal. In such applications, drive the CLK+ pin directly from a CMOS gate, and bypass the CLK− pin to ground with a 0.1 µF capacitor (see Figure 59).

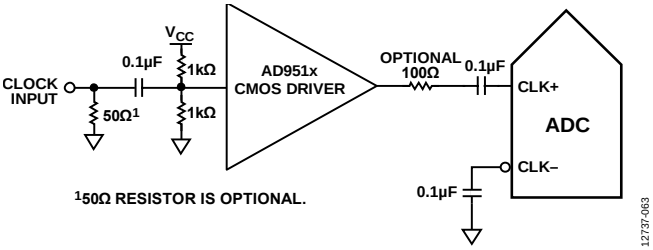


Figure 59. Single-Ended 1.8 V CMOS Input Clock (Up to 200 MHz)

Input Clock Divider

The AD9655 contains an input clock divider that can divide the input clock by integer values from 1 to 8. To achieve a given sample rate, the frequency of the externally applied clock must be multiplied by the divide value. The increased rate of the external clock normally results in lower clock jitter, which is beneficial for intermediate frequency (IF) undersampling applications.

Clock Duty Cycle

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals and, as a result, may be sensitive to the clock duty cycle. Commonly, a ±5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics.

The AD9655 contains a duty cycle stabilizer (DCS) that retimes the nonsampling (falling) edge, providing an internal clock signal with a nominal 50% duty cycle. This allows the user to provide a wide range of clock input duty cycles without affecting the performance of the AD9655. Noise and distortion performance are nearly flat for a wide range of duty cycles with the DCS on.

Jitter in the rising edge of the clock is still of concern and is not easily reduced by the internal stabilization circuit. The duty cycle control loop does not function for clock rates of less than 20 MHz, nominally. The loop has a time constant associated with it that must be considered in applications in which the clock rate can change dynamically. A wait time of 1.5 µs to 5 µs is required after a dynamic clock frequency increase or decrease before the DCS loop is relocked to the input signal.

Jitter Considerations

High speed, high resolution ADCs are sensitive to the quality of the clock input. The following equation shows how SNR degrades at a given input frequency (f_A) due only to aperture jitter (t_J):

$$SNR\ Degradation = 20\log_{10}\left(\frac{1}{2\pi \times f_A \times t_J}\right)$$

In this equation, the rms aperture jitter represents the root sum square of all jitter sources, including the clock input, analog input signal, and ADC aperture jitter specifications. IF under-sampling applications are particularly sensitive to jitter. The effect of jitter alone on SNR, with no other noise contributors, is shown in Figure 60.

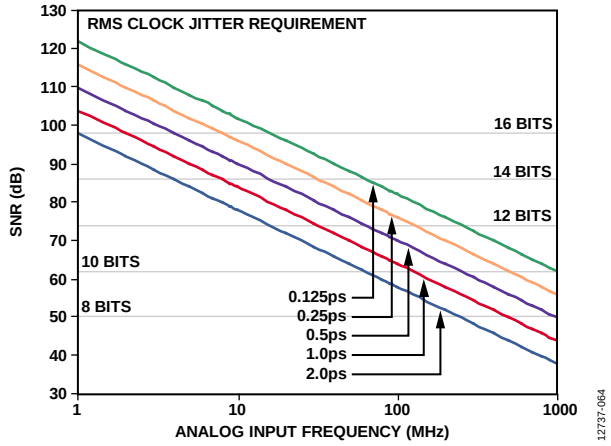


Figure 60. Ideal SNR vs. Analog Input Frequency and Jitter

Treat the clock input as an analog signal when aperture jitter may affect the dynamic range of the AD9655. Separate clock driver power supplies from the ADC output driver supplies to avoid modulating the clock signal with digital noise. Low jitter, crystal controlled oscillators are the best clock sources. If the clock is generated from another type of source (by gating, dividing, or other methods), it is recommended that the clock be retimed by the original clock as the last step.

See the AN-501 Application Note and the AN-756 Application Note for more information about jitter performance as it relates to ADCs.

POWER DISSIPATION AND POWER-DOWN MODE

As shown in Figure 61, the power dissipated by the AD9655 is proportional to its sample rate. The AD9655 is placed in power-down mode either by the SPI port or by asserting the SDIO/PDWN pin high when in non-SPI mode. In this state, the ADC typically dissipates 2 mW. During power-down, the output drivers are placed in a high impedance state. In non-SPI mode, asserting the SDIO/PDWN pin low returns the AD9655 to its normal operating mode. Note that SDIO/PDWN is referenced to the digital output driver supply (DRVDD) and must not exceed that supply voltage.

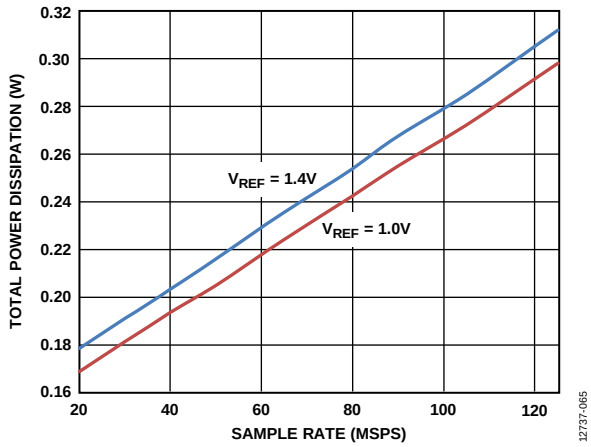


Figure 61. Total Power Dissipation vs. Sample Rate (f_{SAMPLE}) for f_{IN} = 9.7 MHz, V_{REF} = 1.0 V and V_{REF} = 1.4 V

The AD9655 achieves low power dissipation in power-down mode by shutting down the reference, reference buffer, biasing networks, and clock. When using the SPI port interface, the user can place the ADC in power-down mode or standby mode. Standby mode allows the user to keep the internal reference circuitry powered when faster wake-up times are required. Do not invoke standby mode while foreground calibration is in progress. Foreground calibration is invoked automatically at power-up, and by executing a digital reset with Register 0x08. Completion is indicated by the contents of Register 0x107 = 0x00. See the Memory Map section for more details on using these features.

DIGITAL OUTPUTS AND TIMING

The AD9655 differential outputs conform to the ANSI-644 LVDS standard on default power-up. This default setting can be changed to a low power, reduced signal option (similar to the IEEE 1596.3 standard) via the SPI. The LVDS driver current is derived on chip and sets the output current at each output equal to a nominal 3.5 mA. A 100 Ω differential termination resistor placed at the LVDS receiver inputs results in a nominal 350 mV swing (or 700 mV p-p differential) at the receiver.

When operating in reduced range mode, the output current reduces to 2 mA. This results in a 200 mV swing (or 400 mV p-p differential) across a 100 Ω termination at the receiver.

The LVDS outputs facilitate interfacing with LVDS receivers in custom ASICs and FPGAs for superior switching performance in noisy environments. Single point-to-point net topologies are recommended with a 100 Ω termination resistor placed as close as possible to the receiver. Timing errors may result if there is no far-end receiver termination, or if there is poor differential trace routing. To avoid such timing errors, ensure that the trace length is less than 24 inches and that the differential output traces are close together and at equal lengths.

Figure 62 shows an example of the FCO and data stream with proper trace length and position.

Figure 63 shows the LVDS output timing example in reduced range mode.

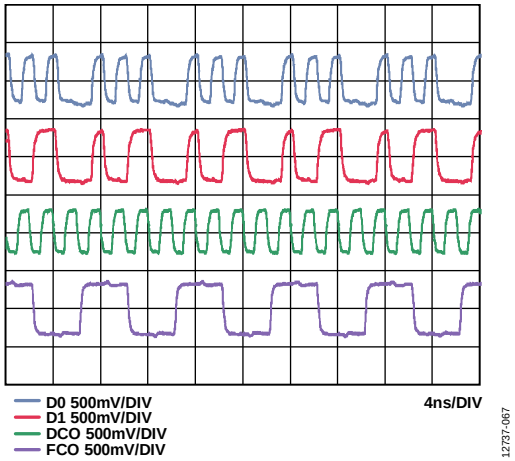


Figure 62. LVDS Output Timing Example in ANSI-644 Mode (Default)

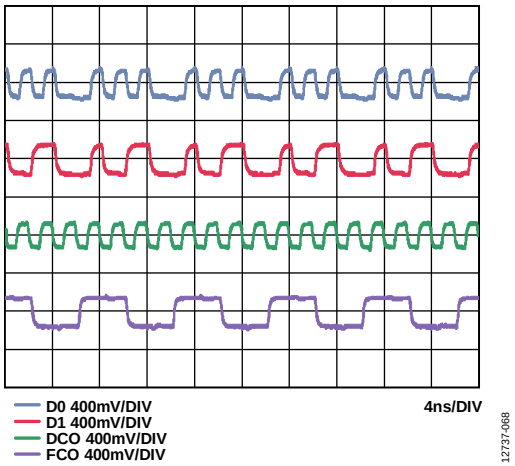


Figure 63. LVDS Output Timing Example in Reduced Range Mode

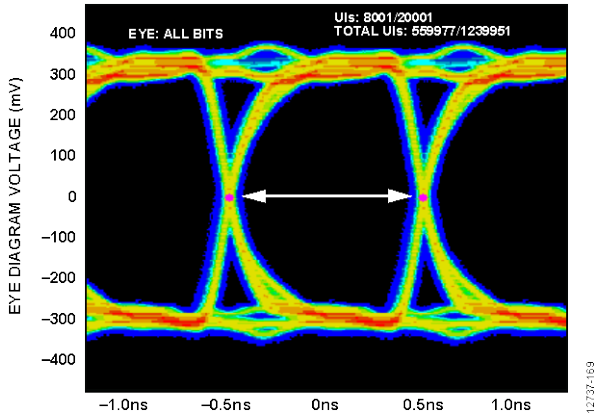


Figure 64. Data Eye for LVDS Outputs in ANSI-644 Mode with Trace Lengths of Less Than 24 Inches (Approximate 6 Inch Trace Length Result Shown) on Standard FR-4 Material, External 100 Ω Far-End Termination Only

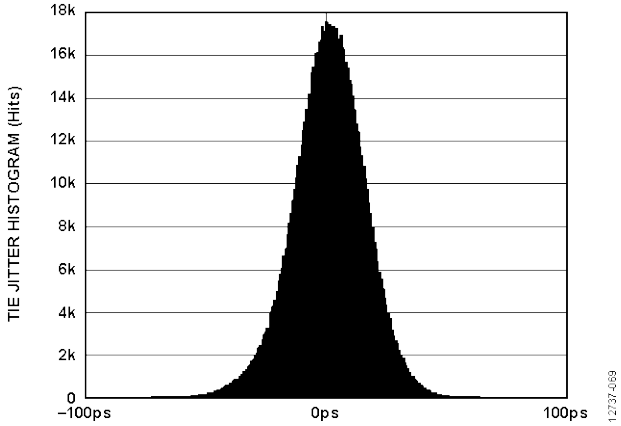


Figure 65. TIE Jitter Histogram for Trace Lengths Less Than 24 Inches (Approximate 6 Inch Trace Length Result Shown)

Figure 64 shows an example of the LVDS output data eye using the ANSI-644 standard (default), and Figure 65 shows a time interval error (TIE) jitter histogram with trace lengths of less than 24 inches on standard FR-4 material.

Figure 66 shows an example of the LVDS output data eye using the ANSI-644 standard (default), and Figure 67 shows a time interval error (TIE) jitter histogram with trace lengths greater than 24 inches on standard FR-4 material. Note that the TIE jitter histogram reflects the decrease of the data eye opening as the edge deviates from the ideal position. It is the responsibility of the user to determine if the waveforms meet the timing budget of the design.

The format of the output data is twos complement by default. See Table 11 for an example of the output coding format. To change the output data format to offset binary, see the Memory Map section.

Data from each ADC is serialized and provided on a separate channel in two lanes in DDR mode. The data rate for each serial stream is equal to (16 bits × the sample clock rate)/2 lanes, with a maximum of 1 Gbps/lane (16 bits × 125 MSPS)/(2 lanes) = 1 Gbps/lane). The minimum conversion rate is 20 MSPS.

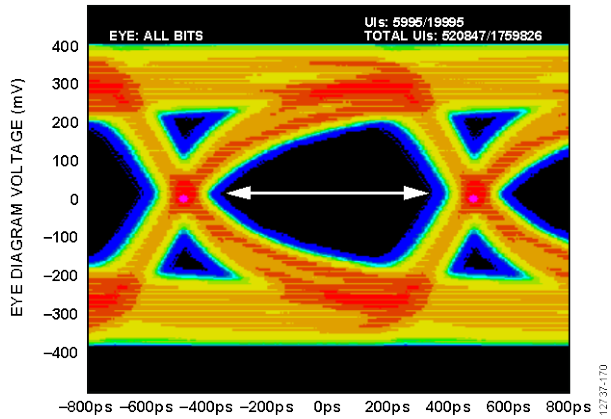


Figure 66. Data Eye for LVDS Outputs in ANSI-644 Mode with Trace Lengths Greater Than 24 Inches (Approximate 36 Inch Trace Length Result Shown) on Standard FR-4 Material, External 100 Ω Far-End Termination Only

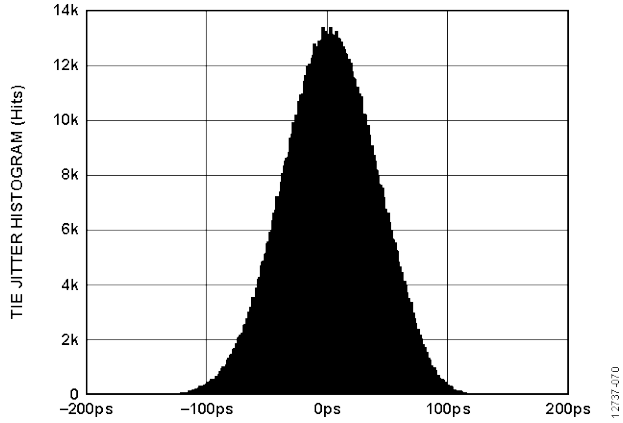


Figure 67. TIE Jitter Histogram for Trace Lengths Greater Than 24 Inches (Approximate 36 Inch Trace Length Result Shown)

Two output clocks assist in capturing data from the AD9655. The DCO clocks the output data and is equal to 4× the sample clock (CLK) rate for the default mode of operation. Data is clocked out of the AD9655 and must be captured on the rising and falling edges of the DCO that supports DDR capturing. The FCO signals the start of a new output byte and is equal to the sample clock rate in 1× frame mode. See the Timing Diagrams section for more information.

When the SPI is used, the DCO phase can be adjusted in approximately 60° increments relative to one data cycle (30° relative to one DCO cycle). This allows the user to refine system timing margins if required. The example DCO+ and DCO– timing, as shown in Figure 2, is 180° relative to one data cycle (90° relative to one DCO cycle).

In default mode, as shown in Figure 2, the MSB is first in the data output serial stream. This can be inverted by using the SPI so that the LSB is first in the data output serial stream.

Table 11. Digital Output Coding

Input (V)	Condition (V)	Offset Binary Output Mode	Twos Complement Mode
VINx+ – VINx–	<–V_{REF} – 0.5 LSB	0000 0000 0000 0000	1000 0000 0000 0000
VINx+ – VINx–	– V_{REF}	0000 0000 0000 0000	1000 0000 0000 0000
VINx+ – VINx–	0 V	1000 0000 0000 0000	0000 0000 0000 0000
VINx+ – VINx–	+ V_{REF} – 1.0 LSB	1111 1111 1111 1111	0111 1111 1111 1111
VINx+ – VINx–	>+ V_{REF} – 0.5 LSB	1111 1111 1111 1111	0111 1111 1111 1111

Table 12. Flexible Output Test Modes

Output Test Mode Bit Sequence	Pattern Name	Digital Output Word 1	Digital Output Word 2	Subject to Data Format Select	Notes
0000	Off (default)	Not applicable	Not applicable	Not applicable	
0001	Midscale short	12-bit: 1000 0000 0000 16-bit: 1000 0000 0000 0000	Not applicable	Yes	Offset binary code shown
0010	+Full-scale short	12-bit: 1111 1111 1111 16-bit: 1111 1111 1111 1111	Not applicable	Yes	Offset binary code shown
0011	–Full-scale short	12-bit: 0000 0000 0000 16-bit: 0000 0000 0000 0000	Not applicable	Yes	Offset binary code shown
0100	Checkerboard	12-bit: 1010 1010 1010 16-bit: 1010 1010 1010 1010	12-bit: 0101 0101 0101 16-bit: 0101 0101 0101 0101	No	
0101	PN sequence long[1]	Not applicable	Not applicable	Yes	PN23 ITU 0.150 $x^{23} + x^{18} + 1$
0110	PN sequence short[1]	Not applicable	Not applicable	Yes	PN9 ITU 0.150 $x^9 + x^5 + 1$
0111	One-/zero-word toggle	12-bit: 1111 1111 1111 16-bit: 111 1111 1111 1111	12-bit: 0000 0000 0000 16-bit: 0000 0000 0000 0000	No	
1000	User input	Register 0x19 and Register 0x1A	Register 0x1B and Register 0x1C	No	
1001	1-/0-bit toggle	12-bit: 1010 1010 1010 16-bit: 1010 1010 1010 1010	Not applicable	No	
1010	1× sync	12-bit: 0000 0000 1111 16-bit: 0000 0000 1111 1111	Not applicable	No	
1011	One bit high	12-bit: 1000 0000 0000 16-bit: 1000 0000 0000 0000	Not applicable	No	Pattern associated with the external pin
1100	Mixed frequency	12-bit: 1010 0001 1001 16-bit: 1010 0001 1001 1100	Not applicable	No	

[1] All test mode options except PN sequence short and PN sequence long can support 12-bit to 16-bit word lengths to verify data capture to the receiver.

There are 12 digital output test pattern options available that can be initiated through the SPI. This is a useful feature when validating receiver capture and timing. See Table 12 for the available output bit sequencing options. Some test patterns have two serial sequential words and can be alternated in various ways, depending on the test pattern chosen.

Note that some patterns do not adhere to the data format select option. In addition, custom user defined test patterns can be assigned in Register 0x19, Register 0x1A, Register 0x1B, and Register 0x1C.

The pseudorandom number (PN) sequence short pattern produces a pseudorandom bit sequence that repeats itself every $2^9 - 1$ or 511 bits. A description of the PN sequence and how it is generated can be found in Section 5.1 of the ITU-T 0.150 (05/96) standard. The seed value is all 1s (see Table 13 for the initial values). The output is a parallel representation of the serial PN9 sequence in MSB first format. The first output word is the first 16 bits of the PN9 sequence in MSB aligned form.

Table 13. PN Sequence

Sequence	Initial Value	Next Three Output Samples (MSB First), Twos Complement
PN Sequence Short	0x7F83	0x5F17, 0xB209, 0xCED1
PN Sequence Long	0x7FFF	0x7E00, 0x807C, 0x801F

The PN sequence long pattern produces a pseudorandom bit sequence that repeats itself every $2^{23} - 1$ or 8,388,607 bits. A description of the PN sequence and how it is generated can be found in Section 5.6 of the ITU-T 0.150 (05/96) standard. The seed value is all 1s (see Table 13 for the initial values) and the AD9655 inverts the bit stream in relation to the ITU standard. The output is a parallel representation of the serial PN23 sequence in MSB first format. The first output word is the first 16 bits of the PN23 sequence in MSB aligned form.

See the Memory Map section for information on how to change these additional digital output timing features through the SPI.

SDIO/PDWN Pin

For applications that do not require SPI mode operation, the CSB pin is tied to DRVDD, and the SDIO/PDWN pin controls the power-down mode according to Table 14.

Table 14. Power-Down Mode Pin Settings

SDIO/PDWN Pin Voltage	Device Mode
AGND (Default)	Run device, normal operation
DRVDD	Power down device

SCLK/DFS Pin

The SCLK/DFS pin is used for output format selection in applications that do not require SPI mode operation. This pin determines the digital output format when the CSB pin is held high during device power-up. When SCLK/DFS is tied to DRVDD, the ADC output format is twos complement; when SCLK/DFS is tied to AGND, the ADC output format is offset binary.

Table 15. Digital Output Format

SCLK/DFS Voltage	Output Format
AGND	Offset binary
DRVDD	Twos complement

CSB Pin

Tie the CSB pin to DRVDD for applications that do not require SPI mode operation. By tying CSB high, all SCLK and SDIO information is ignored.

RBIAS Pin

To set the internal core bias current of the ADC, place a 10.0 kΩ, 1% tolerance resistor to ground at the RBIAS pin.

OUTPUT TEST MODES

The output test options are described in Table 12 and are controlled by the output test mode bits at Register 0x0D. When an output test mode is enabled, the analog section of the ADC is disconnected from the digital back-end blocks and the test pattern is run through the output formatting block. Some of the test patterns are subject to output formatting, and some are not. The PN generators from the PN sequence tests can be reset by setting Bit 4 or Bit 5 of Register 0x0D. These tests can be performed with or without an analog signal (if present, the analog signal is ignored), but they do require an encode clock. For general information, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

SERIAL PORT INTERFACE (SPI)

The AD9655 SPI allows the user to configure the converter for specific functions or operations through a structured register space provided inside the ADC. The SPI offers the user added flexibility and customization, depending on the application. Addresses are accessed via the serial port and can be written to or read from via the port. Memory is organized into bytes that can be further divided into fields, which are documented in the Memory Map section. Information specific to the AD9655 is contained in this data sheet, and takes precedence over the the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*, which provides general information.

CONFIGURATION USING THE SPI

Three pins define the SPI of this ADC: the SCLK/DFS pin, the SDIO/PDWN pin, and the CSB pin (see Table 16). SCLK/DFS (a serial clock when CSB is low) synchronizes the read and write data presented from and to the ADC. SDIO/PDWN (serial data input/output when CSB is low) is a dual-purpose pin that allows data to be sent to and read from the internal ADC memory map registers. CSB (chip select bar) is an active low control that enables or disables the SPI read and write cycles.

Table 16. Serial Port Interface Pins

Pin	Function
SCLK/DFS	Serial clock when CSB is low. The serial shift clock input, which synchronizes serial interface reads and writes.
SDIO/PDWN	Serial data input/output when CSB is low. A dual-purpose pin that typically serves as an input or an output, depending on the instruction sent and the relative position in the timing frame.
CSB	Chip select bar. An active low control that enables the SPI mode read and write cycles.

The falling edge of CSB, in conjunction with the rising edge of SCLK/DFS, determines the start of the framing. An example of the serial timing is shown in Figure 68. See Table 7 for definitions of the timing parameters.

Other modes involving the CSB pin are available. CSB can be held low indefinitely, which permanently enables SPI mode; this is called streaming. CSB can stall high between bytes to allow for additional external timing. When the CSB pin is tied high at power-up, SPI functions are placed in high impedance mode. This mode turns on the secondary functions of the SPI pins. Note that, when SPI mode is entered, that is, CSB is taken low, these secondary functions cannot be invoked without power cycling the device.

During the instruction phase of an SPI operation, a 16-bit instruction is transmitted. Data follows the instruction phase, and the length of this data is determined by the W0 and W1 bits (see Figure 68).

In addition to word length, the instruction phase determines whether the serial frame is a read or write operation, allowing the serial port to be used both to program the chip and to read the contents of the on-chip memory. The first bit of the first byte in a multibyte serial data transfer frame indicates whether a read command or a write command is issued. If the instruction is a readback operation, performing a readback causes the serial data input/output SDIO/PDWN pin to change direction from an input to an output at the appropriate point in the serial frame.

All data is composed of 8-bit words. Data can be sent in MSB first mode or in LSB first mode. MSB first mode is the default on power-up and can be changed via the SPI port configuration register. For more information about this and other features, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

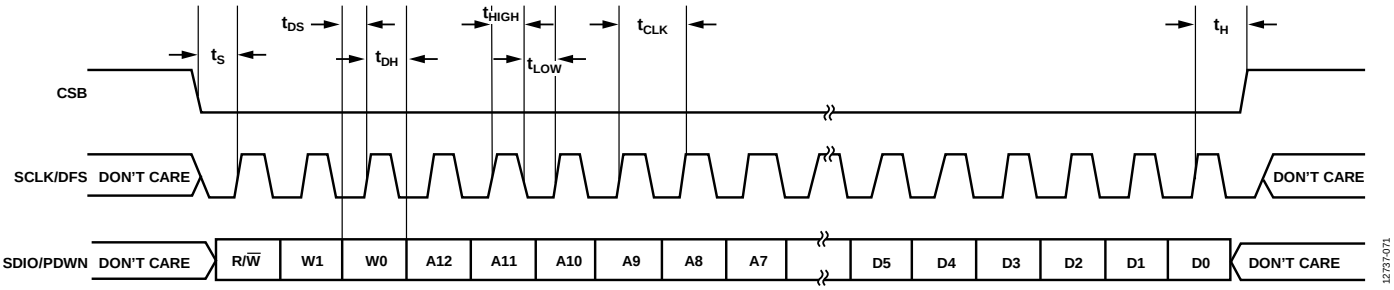


Figure 68. Serial Port Interface Timing Diagram

HARDWARE INTERFACE

The pins described in Table 16 comprise the physical interface between the user programming device and the serial port of the AD9655. The SCLK/DFS pin and the CSB pin function as inputs when using the SPI interface. The SDIO/PDWN pin is bidirectional, functioning as an input during write phases and as an output during readback.

The SPI interface is flexible enough to be controlled by either FPGAs or microcontrollers. One method for SPI configuration is described in detail in the AN-812 Application Note, *Microcontroller-Based Serial Port Interface (SPI) Boot Circuit*.

It is recommended that the SPI port not be active during periods when the full dynamic performance of the converter is required. Because the SCLK/DFS signal, the CSB signal, and the SDIO/PDWN signal are typically asynchronous to the ADC clock, noise from these signals can degrade converter performance. If the on-board SPI bus is used for other devices, it may be necessary to provide buffers between this bus and the AD9655 to prevent these signals from transitioning at the converter inputs during critical sampling periods.

The SCLK/DFS and SDIO/PDWN pins serve a dual function when the SPI interface is not in use. When the pins are strapped to DRVDD or ground during device power-on, they are associated with a specific function. Table 14 and Table 15 describe the strappable functions supported on the AD9655.

CONFIGURATION WITHOUT THE SPI

In applications that do not interface to the SPI control registers, the SCLK/DFS pin and the SDIO/PDWN pin serve as standalone CMOS-compatible control pins. When the device is powered up, it is assumed that the user intends to use the pins as static control lines for the output data format and power-down feature control. In this mode, connect CSB to DRVDD, which disables the serial port interface.

SPI ACCESSIBLE FEATURES

Table 17 provides a brief description of the general features accessible via the SPI. These features are described in general in the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*. The AD9655 device-specific features are described in detail following Table 18, the external memory map register table.

Table 17. Features Accessible Using the SPI

Feature Name	Description
Power Mode	Allows the user to set either power-down mode or standby mode
Clock	Allows the user to access the DCS, set the clock divider, and set the clock divider phase
Offset	Allows the user to digitally adjust the converter offset
Test I/O	Allows the user to set test modes to have known data on output bits
Output Mode	Allows the user to set the output mode
Output Phase	Allows the user to set the output clock polarity
ADC Resolution	Allows power consumption scaling with respect to sample rate

MEMORY MAP

READING THE MEMORY MAP REGISTER TABLE

Each row in the memory map register table (see Table 18) has eight bit locations. The memory map is roughly divided into three sections: the chip configuration registers (Address 0x00 to Address 0x02); the device index register (Address 0x05); and the global ADC function registers, including setup, control, and test registers (Address 0x08 and beyond).

The memory map register table lists the default hexadecimal value for each hexadecimal address shown. The column with the heading Bit 7 (MSB) contains the most significant bit of the default hexadecimal value given. For example, Address 0x05, the device index register, has a hexadecimal default value of 0x33. This means that in Address 0x05, Bits[7:6] = 00, Bits[5:4] = 11, Bits[3:2] = 00, and Bits[1:0] = 11 (in binary). This setting is the default channel index setting. The default value results in both ADC channels receiving the next write command. For more information on this function and others, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*. This application note documents the functions controlled by Register 0x00 to Register 0xFF. Specific register functions for the AD9655 are documented in the Memory Map Register Descriptions section.

Open Locations

All address and bit locations not included in Table 18 are not currently supported for this device. Write unused bits of a valid address location with 0s. Writing to these locations is required only when part of an address location is open (for example, Address 0x05). If the entire address location is open or not listed in Table 18 (for example, Address 0x13), this address location must not be written.

Default Values

After the AD9655 is soft reset by Register 0x00, critical registers are loaded with default values. The default values for the registers are given in the memory map register table, Table 18.

Logic Levels

An explanation of logic level terminology is as follows:

- "Bit is set" is synonymous with "bit is set to Logic 1" or "writing Logic 1 for the bit."
- "Clear a bit" is synonymous with "bit is set to Logic 0" or "writing Logic 0 for the bit."

Channel Specific Registers

Some channel setup functions can be programmed individually for each channel. In these cases, channel address locations are internally duplicated for each channel. These registers and bits are designated in Table 18 as local. These local registers and bits can be accessed by setting the appropriate data channel bits (Channel A or Channel B) and the clock channel DCO bit (Bit 5) and clock channel FCO bit (Bit 4) in Register 0x05. If all the bits are set, the subsequent write affects the registers of both channels and the DCO/FCO clock channels. In a read cycle, only set one channel (Channel A or Channel B) to read one of the two registers. If all the bits are set during an SPI read cycle, the device returns the value for Channel A. Registers and bits that are designated as global in Table 18 affect the entire device and channel features for which independent settings are not allowed between channels. The settings in Register 0x05 do not affect the global registers and bits.

MEMORY MAP REGISTER TABLE

The AD9655 uses a 3-wire interface and 16-bit addressing; therefore, Bit 0 and Bit 7 in Register 0x00 are set to 0, and Bit 3 and Bit 4 are set to 1.

When Bit 5 in Register 0x00 is set high, the SPI enters a soft reset, where all of the user registers revert to their default values and Bit 2 is automatically cleared.

Table 18.

Addr. (Hex)	Parameter Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)	Comments
Chip Configuration Registers											
0x00	SPI port configuration	0 = SDO active	LSB first	Soft reset	1 = 16-bit address	1 = 16-bit address	Soft reset	LSB first	0 = SDO active	0x18	Nibbles are mirrored to allow a given register value to perform the same function for either MSB first or LSB first mode.
0x01	Chip ID (global)	8-bit chip ID, Bits[7:0] 0xC2 = AD9655, dual, 16-bit, 125 MSPS, serial LVDS								0xC2	Unique chip ID used to differentiate devices; read only.
0x02	Chip grade (global)	Open	Speed grade ID, Bits[6:4] 110 = 125 MSPS			Revision, Bits[3:0]				0x62	Unique speed grade ID used to differentiate graded devices; read only.
Device Index Register											
0x05	Device index	Open		Clock channel DCO	Clock channel FCO	Open		Data Channel B	Data Channel A	0x33	Bits are set to determine which device on chip receives the next write command. Default is all devices on chip.
Global ADC Function Registers											
0x08	Power modes (global)	Open						Power mode 00 = chip run 01 = full power-down 10 = standby 11 = digital reset		0x00	Determines various generic modes of chip operation.
0x09	Clock (global)	Open					DCS bypass 0 = inactive 1 = active	Open	DCS 0 = off 1 = on	0x04	DCS controls. Bit 2 = 1 bypasses the clock divider as well as DCS.
0x0B	Clock divide (global)	Open					Clock divide ratio, Bits[2:0] 000 = divide by 1 001 = divide by 2 010 = divide by 3 011 = divide by 4 100 = divide by 5 101 = divide by 6 110 = divide by 7 111 = divide by 8			0x00	Setting Register 0x09, Bit 2 = 1 bypasses the clock divider as well as DCS.
0x0C	Enhancement control	Open					Chop mode 0 = off 1 = on	Open		0x00	Enables/ disables chop mode.

Addr. (Hex)	Parameter Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)	Comments
0x0D	Test mode (local except for PN sequence resets)	User input test mode 00 = single 01 = alternate 10 = single once 11 = alternate once (Bits[7:6] affect user input, test mode only, Bits[3:0] = 1000)		Reset PN long gen-erator	Reset PN short generator	Output test mode, Bits[3:0] (local) 0000 = off (default) 0001 = midscale short 0010 = positive FS 0011 = negative FS 0100 = alternating checkerboard 0101 = PN23 sequence 0110 = PN9 sequence 0111 = one-/zero-word toggle 1000 = user input 1001 = 1-/0-bit toggle 1010 = 1× sync 1011 = one bit high 1100 = mixed bit frequency				0x00	When set, the test data is placed on the output pins in place of normal data.
0x10	Offset adjust (local)	8-bit device offset adjustment, Bits[7:0] (local); offset adjust in LSBs from −128 to +127 (twos complement format)								0x00	Device offset trim.
0x14	Output mode	0	LVDS-ANSI/ LVDS-IEEE option 0 = LVDS-ANSI 1 = LVDS-IEEE reduced range link (global); see Table 19	0	0	0	Output invert (local)	Open	Output format 0 = offset binary 1 = twos comple-ment (global)	0x01	Configures the outputs and format of the data.
0x16	Output phase	Open	Input clock phase adjust, Bits[6:4] (value is number of input clock cycles of phase delay); see Table 20			Output clock phase adjust, Bits[3:0] (0000 through 1011); see Table 21				0x03	On devices using global clock divide, Bits[6:4] determine which phase of the divider output supplies the output clock. Internal latching is unaffected.
0x18	V_{REF}	Open					Internal V_{REF} adjustment digital scaling, Bits[2:0] 000 = 1.0 V p-p (1.4 V p-p) 001 = 1.14 V p-p (1.6 V p-p) 010 = 1.33 V p-p (1.86 V p-p) 011 = 1.6 V p-p (2.24 V p-p) 100 = 2.0 V p-p (2.8 V p-p)			0x04	Digitally adjusts full-scale input voltage. Does not affect analog input swing. Values shown are for V_{REF} = 1.0 V (1.4 V).
0x19	USER_PATT1_LSB (global)	B7	B6	B5	B4	B3	B2	B1	B0	0x00	User Defined Pattern 1 (8 LSBs).
0x1A	USER_PATT1_MSB (global)	B15	B14	B13	B12	B11	B10	B9	B8	0x00	User Defined Pattern 1 (8 MSBs).
0x1B	USER_PATT2_LSB (global)	B7	B6	B5	B4	B3	B2	B1	B0	0x00	User Defined Pattern 2 (8 LSBs).
0x1C	USER_PATT2_MSB (global)	B15	B14	B13	B12	B11	B10	B9	B8	0x00	User Defined Pattern 2 (8 MSBs).

Addr. (Hex)	Parameter Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)	Comments
0x21	Serial output data control (global)	LVDS output 0 = MSB first (default) 1 = LSB first	SDR/DDR one-lane/two-lane, bitwise/bytewise, Bits[6:4] 000 = SDR two-lane, bitwise 001 = SDR two-lane, bytewise 010 = DDR two-lane, bitwise 011 = DDR two-lane, bytewise (default) 100 = DDR one-lane, wordwise			0	0 = 1× frame (default) 1 = 2× frame	Serial output number of bits 00 = 16 bits (default) 01 = 14 bits 10 = 12 bits 11 = 10 bits		0x30	Serial stream control.
0x22	Serial channel status (local)	Open						Channel output reset	Channel power-down	0x00	Used with Register 0x05 to power down individual sections of a converter.
0x101	User Input/Output Control 2	Open							Disable SDIO pull-down	0x00	Disables SDIO pull-down resistor.
0x102	User Input/Output Control 3	Open				VCM power-down	0	0	0	0x00	VCM control.
0x107	Foreground calibrations status	Open						Bit 1 = 1 during foreground calibration, Bit 1 = 0 after calibration is complete	Bit 0 = 1 during foreground calibration, Bit 0 = 0 after calibration is complete	0x00	Read only.
0x112	Clock monitor control	Open	0	Recovery mode 000 = recovery off (default) 101 = recovery on			1	1	1	0x07	Select clock recovery mode.
0x114	V_{REF} control	Open					Drive V_{REF} external 0 = no 1 = yes	V_{REF} 00 = 1.0 V 01 = 1.2 V 10 = 1.3 V 11 = 1.4 V		0x00	Bits[1:0] set the internal reference voltage. Bit 2 disables the reference if an external source is desired.

MEMORY MAP REGISTER DESCRIPTIONS

For general information about the functions controlled in Register 0x00 to Register 0xFF, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

Device Index (Register 0x05)

There are certain features in the map that can be set independently for each channel, whereas other features apply globally to all channels (depending on context), regardless of which channel is selected. Bits[1:0] in Register 0x05 can be used to select which individual data channel is affected by the next SPI action. The output clock channels can be selected in Register 0x05, as well. A smaller subset of the independent feature list can be applied to those devices.

Refer to the following sequence of SPI writes for an example of how to use Register 0x5 to power down Channel B while keeping Channel A active:

1. SPI_Write (0x05, 0x02)—designates Channel B to be affected by the next local SPI register instruction.
2. SPI_Write (0x22, 0x01)—powers down the Channel previously designated.
3. SPI_Write (0x05, 0x31)—designates DCO, FCO and Channel A to be affected by future local SPI register instruction (optional).
4. SPI_Write (0x08, 0x03)—digital reset.
5. SPI_Write (0x08, 0x00)—takes the device back to normal operation.

Power Modes (Register 0x08)

Bits[7:2]—Open

Bits[1:0]—Power Mode

In normal operation (Bits[1:0] = 00), both ADC channels are active.

In power-down mode (Bits[1:0] = 01), the digital datapath clocks are disabled while the digital datapath is reset. Outputs are disabled.

In standby mode (Bits[1:0] = 10), the digital datapath clocks and the outputs are disabled. Do not invoke standby mode while foreground calibration is in progress. Foreground calibration is invoked automatically at power-up and by executing a digital reset with Register 0x08. Foreground calibration completion is indicated by the contents of Register 0x107 = 0x00.

During a digital reset (Bits[1:0] = 11), a foreground calibration is invoked, all the digital datapath clocks and the outputs (where applicable) on the chip are reset, except the SPI port. Note that the SPI is always left under control of the user; that is, it is never automatically disabled or in reset (except by power-on reset).

Enhancement Control (Register 0x0C)

Bits[7:3]—Open

Bit 2—Chop Mode

For applications sensitive to offset voltages and other low frequency noise, such as homodyne or direct conversion receivers, chopping in the first stage of the AD9655 is an available feature, enabled by setting Bit 2. In the frequency domain, chopping translates offsets and other low frequency noise to $f_{CLK}/2$, where it can be filtered.

Bits[1:0]—Open

Output Mode (Register 0x14)

Bit 7—0

Bit 6—LVDS-ANSI/LVDS-IEEE Option

Setting this bit selects the LVDS-IEEE (reduced range) option.

The default setting is LVDS-ANSI. When LVDS-ANSI or the LVDS-IEEE reduced range link is selected, the driver current is automatically selected to give the proper output swing.

Table 19. LVDS-ANSI/LVDS-IEEE Options

Output Mode, Bit 6	Output Mode	Output Driver Current
0	LVDS-ANSI	Automatically selected to give proper swing
1	LVDS-IEEE reduced range link	Automatically selected to give proper swing

Bits[5:3]—000

Bit 2—Output Invert

Setting this bit inverts the output bit stream.

Bit 1—Open

Bit 0—Output Format

By default, this bit is set to send the data output in twos complement format. Clearing this bit to 0 changes the output mode to offset binary.

Output Phase (Register 0x16)

Bit 7—Open

Bits[6:4]—Input Clock Phase Adjust

When the clock divider (Register 0x0B) is used, the applied clock is at a higher frequency than the internal sampling clock. Bits[6:4] determine at which phase of the external clock sampling occurs. This is applicable only when the clock divider is used. Selecting a value for Bits[6:4] greater than Register 0x0B, Bits[2:0] is prohibited. See Table 20 for details.

Table 20. Input Clock Phase Adjust Options

Input Clock Phase Adjust, Bits[6:4]	Number of Input Clock Cycles of Phase Delay
000 (Default)	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

Bits[3:0]—Output Clock Phase Adjust

See Table 21 for details.

Table 21. Output Clock Phase Adjust Options

Output Clock (DCO), Phase Adjust, Bits[3:0]	DCO Phase Adjustment (Approximate Degrees Relative to the D0x±/D1x± Edge)
0000	0
0001	60
0010	120
0011 (Default)	180
0100	240
0101	300
0110	360
0111	420
1000	480
1001	540
1010	600
1011 through 1111	660

Serial Output Data Control (Register 0x21)

The serial output data control register to programs the AD9655 in various output data modes, depending on the data capture solution. Table 22 describes the various serialization options available in the AD9655. Note that, in single data rate (SDR) mode, the DCO frequency is double that of the frequency in DDR mode for a given sample rate. In SDR mode, to stay within the capability of the DCO LVDS driver, the ADC sample rate must be reduced to ≤62.5 MSPS to keep the DCO frequency at ≤500 MHz.

User I/O Control 2 (Register 0x101)

Bits[7:1]—Open

Bit 0—Disable SDIO Pull-Down

Bit 0 can be set to disable the internal 31 kΩ pull-down resistor on the SDIO/PWDN pin, which limits the loading when many devices are connected to the SPI bus.

User I/O Control 3 (Register 0x102)

Bits[7:4]—Open

Bit 3—VCM Power-Down

Bit 3 can be set high to power down the internal VCM generator. This feature is used when applying an external reference.

Bits[2:0]—000

Clock Monitor Control (Register 0x112)

Bit 7—Open

Bit 6—0 (Reserved)

Bits[5:3]—Recovery Mode

By default (Bits[5:3] = 000), recovery mode is off. In this condition, the AD9655 does not automatically recover from a state change or corruption due to a clock glitch or irregularity. With recovery mode off, a digital reset (Register 0x08 = 0x03, then Register 0x08 = 0x00) is needed to restore the AD9655 to proper operation in case of disruption due to clock instability.

With clock recovery mode on (Bits[5:3] = 101), AD9655 automatically recovers from corruption due to a clock glitch or irregularity. After the corruption is autodetected, 31×10^6 clock cycles are needed to restore proper operation.

Bits[2:0]— Recovery Mode Setup

Recovery mode is set up for correct operation by default (Bits[2:0] = 111).

V_{REF} Control (Register 0x114)

This register adjusts the internal analog V_{REF} value. A digital reset using Register 0x08 must follow any change in analog V_{REF}.

Table 22. SPI Register 0x21 Options

Register 0x21 Contents	Serialization Options Selected			DCO Multiplier	Timing Diagram
	Serial Output Number of Bits (SONB)	Frame Mode	Serial Data Mode		
0x30	16-bit	1×	DDR two-lane bytewise	$4 \times f_S$	See Figure 2 (default setting)
0x20	16-bit	1×	DDR two-lane bitwise	$4 \times f_S$	See Figure 2
0x10	16-bit	1×	SDR two-lane bytewise	$8 \times f_S$	See Figure 2
0x00	16-bit	1×	SDR two-lane bitwise	$8 \times f_S$	See Figure 2
0x40	16-bit	1×	DDR one-lane wordwise	$8 \times f_S$	See Figure 3

APPLICATIONS INFORMATION

DESIGN GUIDELINES

Before starting design and layout of the AD9655 as a system, it is recommended that the designer become familiar with these guidelines, which describe the special circuit connections and layout requirements needed for certain pins.

POWER AND GROUND GUIDELINES

When connecting power to the AD9655, it is recommended that two separate 1.8 V supplies be used. Use one supply for analog (AVDD); use a separate supply for the digital outputs (DRVDD). For both AVDD and DRVDD, use several different bypass capacitor values to cover both high and low frequencies. Place these capacitors close to the point of entry at the PCB level and close to the pins of the device, with minimal trace length.

A single PCB ground plane is sufficient when using the AD9655. With proper bypassing and smart partitioning of the PCB analog, digital, and clock sections, optimum performance is easily achieved.

CLOCK STABILITY CONSIDERATIONS

When powered on, the AD9655 enters an initialization phase during which an internal state machine sets up the biases and the registers for proper operation. During the initialization process, the AD9655 needs a stable clock. If the ADC clock source is not present or not stable during ADC power-up, it disrupts the state machine and causes the ADC to start up in an unknown state. To correct this, reinvoke an initialization sequence after the ADC clock is stable by issuing a digital reset via Register 0x08. In the default configuration (internal V_{REF}, ac-coupled input) where V_{REF} and V_{CM} are supplied by the ADC, a stable clock during power-up is sufficient. When V_{CM} is supplied by an external source, this, too, must be stable at power-up; otherwise, a subsequent digital reset via Register 0x08 is needed. Clock instability during normal operation may also necessitate digital reset to restore proper operation.

The pseudo code sequence for a digital reset is as follows:

1. SPI_Write (0x08, 0x03)—digital reset.
2. SPI_Write (0x08, 0x00)—normal operation.

EXPOSED PAD THERMAL HEAT SLUG RECOMMENDATIONS

It is required that the exposed pad on the underside of the ADC be connected to analog ground (AGND) to achieve the best electrical and thermal performance of the AD9655. It is recommended that an exposed continuous copper plane on the PCB mate to the AD9655 exposed pad, Pin 0. It is also recommended that this copper plane have several vias to achieve the lowest possible resistive thermal path for heat dissipation to flow through the bottom of the PCB. Solder-fill or plug these vias.

To maximize the coverage and adhesion between the ADC and PCB, partition the continuous copper plane by overlaying a silkscreen or solder mask on the PCB into several uniform sections. This provides several tie points between the ADC and PCB during the reflow process, whereas using one continuous plane with no partitions only guarantees one tie point. See Figure 69 for a PCB layout example. For detailed information on packaging and the PCB layout of chip scale packages, see the AN-772 Application Note, *A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)*.

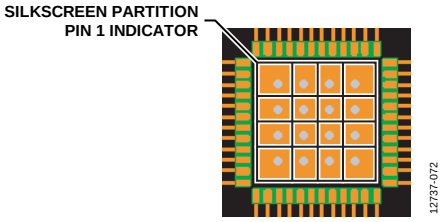


Figure 69. Typical PCB Layout

VCM

Bypass the VCM pin to ground with a 0.1 µF capacitor.

REFERENCE BYPASSING

Externally bypass the VREF pin to ground with a low ESR, 1.0 µF capacitor in parallel with a low ESR, 0.1 µF ceramic capacitor.

SPI PORT

The SPI port must not be active during periods when the full dynamic performance of the converter is required. Because the SCLK, CSB, and SDIO signals are typically asynchronous to the ADC clock, noise from these signals can degrade converter performance. If the on-board SPI bus is used for other devices, it may be necessary to provide buffers between this bus and the AD9655 to prevent these signals from transitioning at the converter inputs during critical sampling periods.

OUTLINE DIMENSIONS

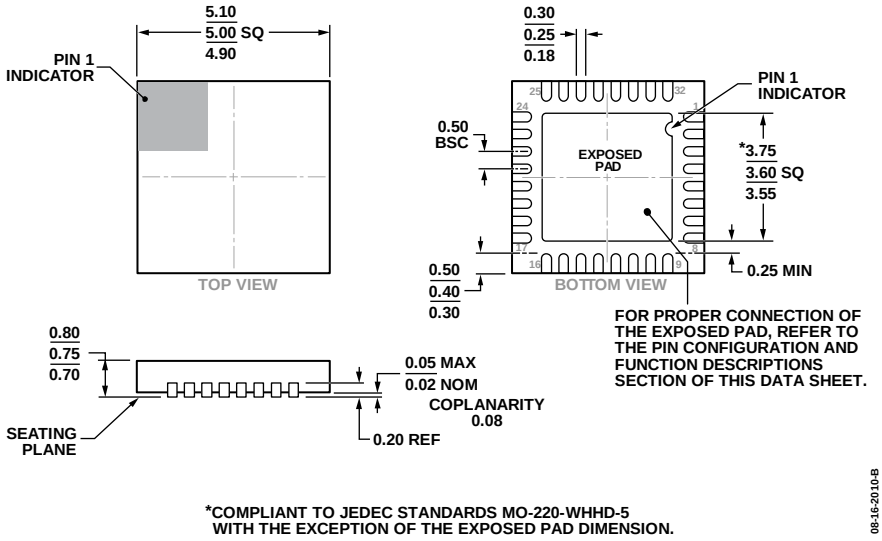


Figure 70. 32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
5 mm × 5 mm Body, Very Very Thin Quad
(CP-32-12)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD9655BCPZ-125	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package (LFCSP_WQ)	CP-32-12
AD9655BCPZRL7-125	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package (LFCSP_WQ)	CP-32-12
AD9655-125EBZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

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