# 10.7 GHz to 12.7 GHz, SATCOM, Microwave Downconverter

## FEATURES

- X/Ku band to IF downconverter with integrated PLL
- RF input frequency range: 10.7 GHz to 12.7 GHz
- Internal LO frequency range: 8.7 GHz to 10.7 GHz
- Noise figure: 5.2 dB, minimum attenuation, LNA low gain mode
- Matched, 50 Ω, single-ended RF input and IF output
- On-chip temperature sensor
- On-chip ADC
- Receiver synthesizer lock detect pin
- Programmable at 20 MHz via 4-wire SPI interface
- Receiver standby function
- 40-lead, 6 mm × 6 mm LFCSP package

## APPLICATIONS

- SATCOM user terminals

## FUNCTIONAL BLOCK DIAGRAM

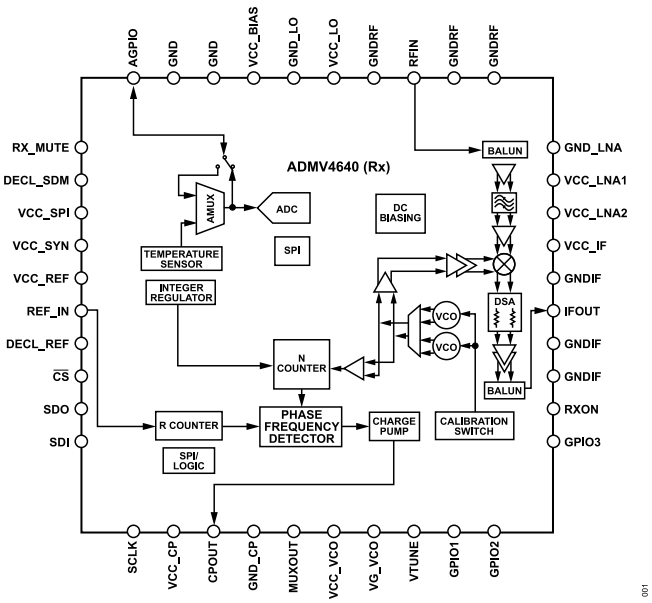


*Figure 1.*

## GENERAL DESCRIPTION

The ADMV4640 is a microwave downconverter optimized for various satellite communication (SATCOM) user terminals operating in the 10.7 GHz to 12.7 GHz RF range.

The ADMV4640 local oscillator (LO) signal is generated internally via the on-chip Integer N (INT) synthesizer. The internal synthesizer enables LO frequency coverage from 8.7 GHz to 10.7GHz. The input RF signals from 10.7 GHz to 12.7 GHz are downconverted to an output intermediate frequency (IF) of 1.4 GHz to 2.2 GHz. The chip includes filtering to reject the image band of 6.7 GHz to 8.7 GHz. The on-chip low noise amplifier includes a 6 dB step attenuator before the mixer to allow the user to trade off between lower noise figure and higher linearity. In addition, the chip includes a digital step attenuator at the IF output to provide up to 31 dB of gain control range with 1 dB steps to adjust for subsequent cable losses.

The digital serial peripheral interface (SPI) allows easy programming of the device. In addition to the digital SPI control, an analog control pin (RX_MUTE) quickly powers down all circuits and places the receiver in standby mode for power saving. An analog general-purpose input-output (AGPIO) pin can be used either as an input to be read by the on-chip analog-to-digital converter (ADC) or as an output for internal analog proportional to absolute temperature (PTAT) voltage. There are also three digital GPIO pins to output logic levels to control external devices using the SPI.

The ADMV4640 downconverter comes in a compact, thermally enhanced, 6 mm × 6 mm, 40-lead, lead frame chip scale package (LFCSP). The ADMV4640 operates over the −40°C to +85°C case temperature range.



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## REVISION HISTORY

**2/2024—Rev. A to Rev. B**

Changed Master to Controller (Throughout) ... 1
Changes to RF Input Frequency Range Parameter, IF Output Frequency Range Parameter, IF Downconverter Performance Parameter, and Image Rejection Parameter, Table 1 ... 3
Changes to Table 4 ... 6

**7/2022—Revision A: Initial Version**

...

## SPECIFICATIONS

$T_A$ = 25°C, IF = 2 GHz, VCC = VCC_SPI = VCC_SYN = VCC_REF = VCC_CP = VCC_VCO = VCC_IF = VCC_LNA2 = VCC_LNA1 = VCC_LO = VCC_BIAS = 3.3 V, digital signal attenuation (DSA) Register 0x300 = 31, clock reference input power = 3 dBm, upper sideband selected, unless otherwise noted. VCC refers to the voltage of all VCC_xxx pins.

*Table 1.*

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| RF INPUT FREQUENCY RANGE | | 10.7 | | 12.75 | GHz |
| LO FREQUENCY RANGE | | 8.7 | | 10.7 | GHz |
| LO Lock Time | | | | 370 | µs |
| LO REFERENCE FREQUENCY | | | 25 | | MHz |
| SPI FREQUENCY | | | 20 | | MHz |
| CLOCK REFERENCE INPUT POWER | | 0 | | 5 | dBm |
| LO PHASE NOISE PERFORMANCE | | | | | |
| 1 kHz Offset from Carrier | | | −85 | | dBc/Hz |
| 10 kHz Offset from Carrier | | | −90 | | dBc/Hz |
| 100 kHz Offset from Carrier | | | −95 | | dBc/Hz |
| 1 MHz Offset from Carrier | | | −124 | | dBc/Hz |
| 10 MHz Offset from Carrier | | | −138 | | dBc/Hz |
| 100 MHz Offset from Carrier | As measured at the IF output | | −142 | | dBc/Hz |
| Integrated Single Sideband Phase Noise Performance | 1 kHz to 125 MHz | | −40 | | dBc/Hz |
| IF OUTPUT FREQUENCY RANGE | | 0.95 | | 2.2 | GHz |
| IF Channel Bandwidth | | | ±125 | | MHz |
| IF DOWNCONVERTER PERFORMANCE | IF = 1.85 GHz to 2.1 GHz, unless otherwise noted | | | | |
| Maximum Conversion Gain | Minimum attenuation, low noise amplifier (LNA) high gain mode | 24 | 27 | 30 | dB |
| Minimum Conversion Gain | Minimum attenuation, LNA low gain mode | 18 | 21 | | dB |
| Gain Control Range | | | 31 | | dB |
| Gain Flatness | Over 230 MHz bandwidth | −0.36 | | +0.36 | dB/230 MHz[1] |
| Noise Figure | Minimum attenuation, LNA high gain mode | | 4.2 | 6.2 | dB |
| | Minimum attenuation, LNA low gain mode | | 5.2 | 7.4 | dB |
| Input Third-Order Intercept (IP3) | Input power ($P_{IN}$) = −33 dBm per tone, minimum attenuation, LNA high gain mode | −7.9 | −6 | | dBm |
| | $P_{IN}$ = −33 dBm per tone, minimum attenuation, LNA low gain mode | −4.7 | −1 | | dBm |
| Input 1 dB Compression Point (P1dB) | Minimum attenuation, LNA high gain mode | −18 | −15 | | dBm |
| | Minimum attenuation, LNA low gain mode | −13 | −11 | | dBm |
| LO to RF Feedthrough | | | −50 | −30 | dBm |
| Image Rejection | | 10.5 | | | |
| | RF = 10.7 GHz to 12.45 GHz, IF = 1.85 GHz to 2.1 GHz | 17 | 30 | | dBc |
| | RF = 12.45 GHz to 12.7 GHz, IF = 1.85 GHz to 2.1 GHz | 10.5 | 17 | | dBc |
| | IF = 950 MHz to 1.4 GHz | | 14 | | dBc |
| ADC PERFORMANCE | | | | | |
| ADC Bits Resolution | | | 8 | | Bits |
| ADC Sampling Rate | | | 100 | | kHz |
| POWER INTERFACE | | | | | |
| Power Supply Voltage (VCC_xxx)[2] | | 3.15 | 3.3 | 3.45 | V |
| VCC_SPI | | | 2 | | mA |

## SPECIFICATIONS

*Table 1. (Continued)*

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| VCC_SYN Supply Current | | | 56 | | mA |
| VCC_REF Supply Current | | | 1 | | mA |
| VCC_CP Supply Current | | | 16 | | mA |
| VCC_VCO Supply Current | | | 80 | | mA |
| VCC_IF Supply Current | | | 68 | | mA |
| VCC_LNA2 Supply Current | | | 42 | | mA |
| VCC_LNA1 Supply Current | | | 30 | | mA |
| VCC_LO Supply Current | | | 48 | | mA |
| VCC_BIAS Supply Current | | | 15 | | mA |
| VCC Total Current | | | 358 | | mA |
| Total Power | | | 1.35 | 1.5 | W |
| Unmute Time | | | | 15 | µ |
| Mute Time | | | | 15 | µ |

[1] dB/230 MHz is gain flatness over 230 MHz bandwidth.

[2] VCC_xx = VCC_SPI = VCC_SYN = VCC_REF = VCC_CP = VCC_VCO = VCC_IF = VCC_LNA2 = VCC_LNA1 = VCC_LO = VCC_BIAS = 3.3 V.

## ABSOLUTE MAXIMUM RATINGS

*Table 2.*

| Parameter | Rating |
|---|---|
| Supply Voltage | |
| VCC_SPI, VCC_SYN, VCC_REF, VCC_CP, VCC_VCO, VCC_IF, VCC_LNA2, VCC_LNA1, VCC_LO, VCC_BIAS | 4.3 V |
| RF Input Power | 0 dBm |
| Reference Clock Input Power | 12 dBm |
| Maximum Junction Temperature | 125°C |
| Moisture Sensitivity Level (MSL)[1] | 3 |
| Peak Reflow Temperature | 260°C |
| Operating Case Temperature Range | −40°C to +85°C |
| Storage Temperature Range | −55°C to +125°C |
| ESD Sensitivity | |
| Human Body Model (HBM) | 2000 V |
| Field Induced Charged Device Model (FICDM) | 250 V |

[1] Based on IPC/JEDEC J-STD-20 MSL classifications.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

$\theta_{JA}$ is the junction to ambient (or die to ambient) thermal resistance measured in a one cubic foot, sealed enclosure, and $\theta_{JC}$ is the junction to case (or die to package) thermal resistance.

*Table 3. Thermal Resistance*

| Package Type | $\theta_{JA}$[1] | $\theta_{JC}$[1, 2] | Unit |
|---|---|---|---|
| CP-40-7[1] | 30.7 | 1.1 | °C/W |

[1] The thermal impedance simulated values are based on a JEDEC 2S2P test board with 6 mm × 6 mm thermal vias. Refer to JEDEC standard JESD51-2 for additional information.

[2] The cold plate of the $\theta_{JC}$ bottom is attached to the bottom side of the PCB using a 100 µm thermal interface material (TIM) (3.56 W/mK).

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device**. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

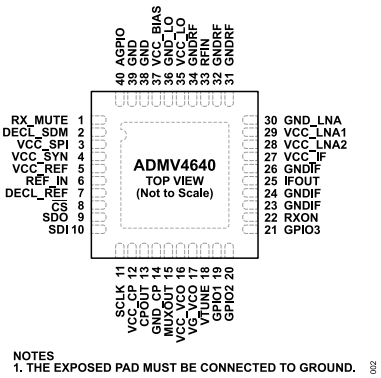



*Figure 2. Pin Configuration*

*Table 4. Pin Function Descriptions*

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | RX_MUTE | Receiver Chip Disable Pin. Drive the RX_MUTE pin to a logic low level in normal operation. Pull the RX_MUTE pin to a logic high level to disable the receiver. |
| 2 | DECL_SDM | Internal Low Drop Out (LDO) Decoupling Pin. Decouple the DECL_SDM pin with 100 pF and 0.47 µF as close as possible to the pin. |
| 3 | VCC_SPI | 3.3 V Power Supply Connections for SPI Control. Decouple the VCC_SPI pin with 100 pF and 1000 pF as close as possible to the pin. |
| 4 | VCC_SYN | 3.3 V Power Supply Connections for the Synthesizer. Decouple the VCC_SYN pin with 100 pF and 1000 pF as close as possible to the pin. |
| 5 | VCC_REF | 3.3 V Power Supply Connections for Reference. Decouple the VCC_REF pin with 100 pF and 1000 pF as close as possible to the pin. |
| 6 | REF_IN | Reference Frequency Input. |
| 7 | DECL_REF | Reference Decoupling Pin. Decouple the DECL_REF pin with 0.47 µF and 1000 pF as close as possible to the pin. |
| 8 | $\overline{CS}$ | Chip Select Pin. |
| 9 | SDO | Serial Data Output. The SDO pin provides an SPI readback capability. |
| 10 | SDI | Serial Data Input. Serial data applied to the SDI pin is loaded into the SPI register upon completion of a write command. The first MSB is a control bit that determines whether data is written to the register (logic high) or read from the serial data output pin (logic low). |
| 11 | SCLK | Serial Clock. This pin is the clock input for the SPI interface. |
| 12 | VCC_CP | 3.3 V Power Supply Connections for the Charge Pump (CP). Decouple the VCC_CP pin with 10 pF and 1000 pF as close as possible to the pin. |
| 13 | CPOUT | CP Output Pin. |
| 14, 23, 24, 26, 30, 31, 32, 34, 36, 38, 39 | GND_CP, GNDIF, GND_LNA, GNDRF, GNDLO, GND | Grounds. Connect these pins to a low impedance ground plane. |
| 15 | MUXOUT | Multiplex Output. See the MUXOUT Select Register section (Register 0x24E). |
| 16 | VCC_VCO | 3.3 V Power Supply Connections for the Voltage Controlled Oscillator (VCO). Apply the low noise source power supply to the VCC_VCO pin and decouple the VCC_VCO pin with 10 pF and 1000 pF as close as possible to the pin. |
| 17 | VG_VCO | VCO Internal Node for DC Decoupling. Decouple the VG_VCO pin with 0.1 µF as close as possible to the pin. |
| 18 | VTUNE | VCO Tuning Voltage. This pin is driven by the output of the loop filter. |
| 19 | GPIO1 | General-Purpose Input/Output. This pin provides an additional digital control line and can be configured to be an input or output, high (3.3 V) or low logic level (0 V). |
| 20 | GPIO2 | General-Purpose Input/Output. This pin provides an additional digital control line and can be configured to be an input or output, high (3.3 V) or low logic level (0 V). |

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

*Table 4. Pin Function Descriptions (Continued)*

| Pin No. | Mnemonic | Description |
|---|---|---|
| 21 | GPIO3 | General-Purpose Input/Output. This pin provides an additional digital control line and can be configured to be an input or output, high (3.3 V) or low logic level (0 V). |
| 22 | RXON | Power-Up Pin for Receiver Chip. Pull the RXON pin to a logic high level in normal operation. Drive the RXON pin to a logic low level to disable the chip. |
| 25 | IFOUT | Intermediate Frequency (IF) Output. |
| 27 | VCC_IF | 3.3 V Power Supply Connections for IF Section. Decouple the VCC_IF pin with 10 pF and 1000 pF as close as possible to the pin. |
| 28 | VCC_LNA2 | 3.3 V Power Supply Connections for the Second Stage Low Noise Amplifier (LNA2). Decouple the VCC_LNA2 pin with 10 pF and 1000 pF as close as possible to the pin. |
| 29 | VCC_LNA1 | 3.3 V Power Supply Connections for First Stage Low Noise Amplifier (LNA1). Decouple the VCC_LNA2 pin with 10 pF and 1000 pF as close as possible to the pin. |
| 33 | RFIN | RF Inputs. This pin must be ac-coupled. |
| 35 | VCC_LO | 3.3 V Power Supply Connections for LO Amplifiers. Decouple the VCC_LO pin with 10 pF and 1000 pF as close as possible to the pin. |
| 37 | VCC_BIAS | 3.3 V Power Supply Connections for Bias Current Generator. Decouple the VCC_BIAS pin with 10 pF and 1000 pF as close as possible to the pin. |
| 40 | AGPIO | Bidirectional Analog General-Purpose Input/Output. This pin can be configured to be the input or to be the output of the internal analog-to-digital converter (ADC). See the AGPIO Control Register section (Register 0x301). |
| | EPAD | Exposed Pad. The exposed pad must be connected to ground. |

## TYPICAL PERFORMANCE CHARACTERISTICS

### MINIMUM ATTENUATION PERFORMANCE: DSA (REGISTER 0X300) = 31

$T_A$ = 25°C, IF = 2 GHz, VCC = 3.3 V, clock reference input power = 3 dBm, upper sideband selected, unless otherwise noted.

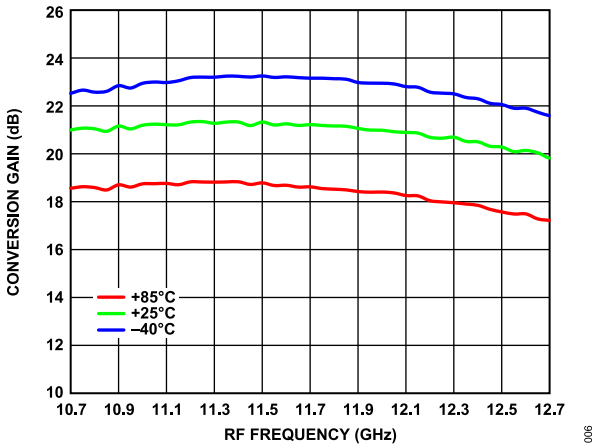



*Figure 3. Conversion Gain vs. RF Frequency over Temperature, LNA Low Gain Mode*

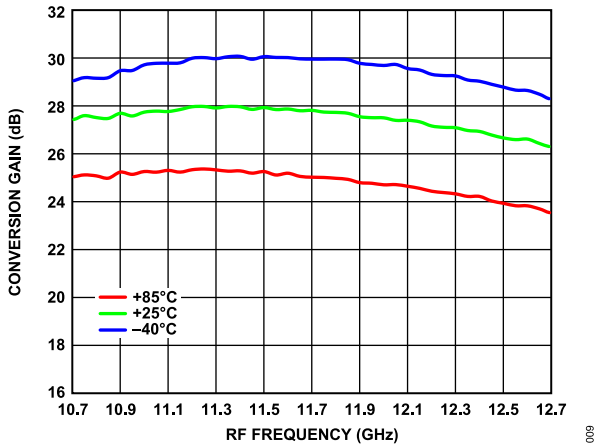



*Figure 6. Conversion Gain vs. RF Frequency over Temperature, LNA High Gain Mode*

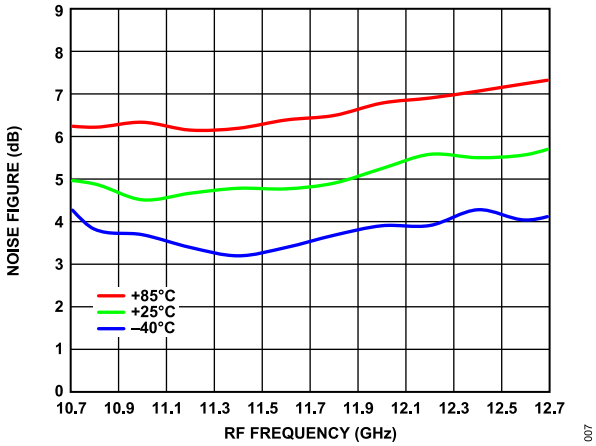



*Figure 4. Noise Figure vs. RF Frequency over Temperature, LNA Low Gain Mode*

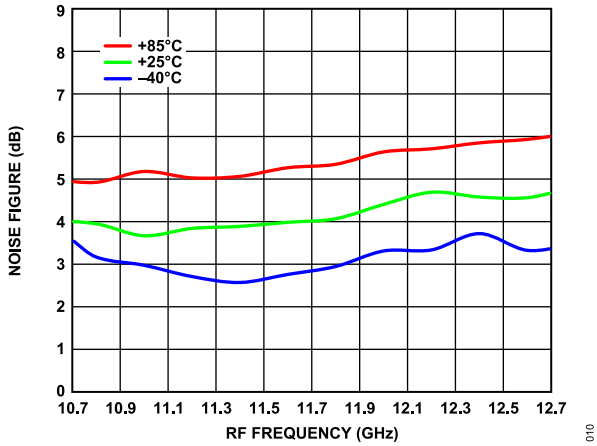



*Figure 7. Noise Figure vs. RF Frequency over Temperature, LNA High Gain Mode*

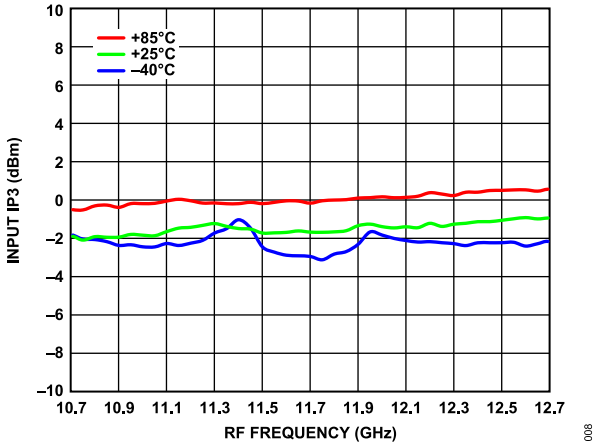



*Figure 5. Input IP3 vs. RF Frequency over Temperature, LNA Low Gain Mode*

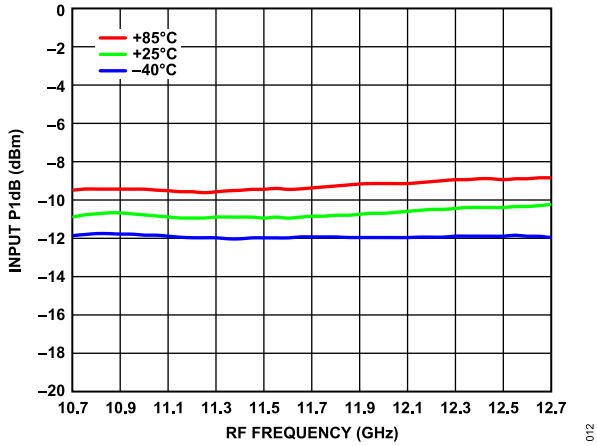



*Figure 8. Input P1dB vs. RF Frequency over Temperature, LNA Low Gain Mode*

## TYPICAL PERFORMANCE CHARACTERISTICS

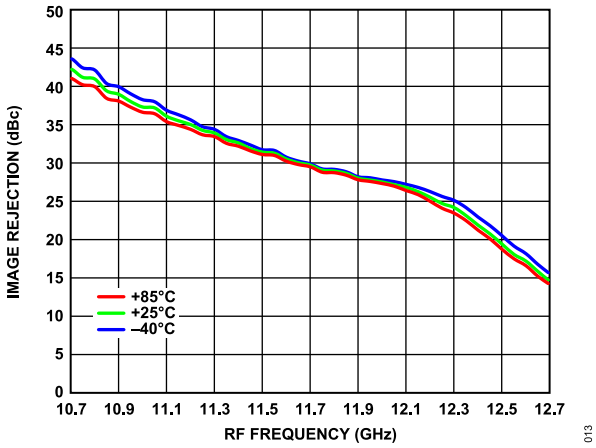



*Figure 9. Image Rejection vs. RF Frequency over Temperature, LNA Low Gain Mode*

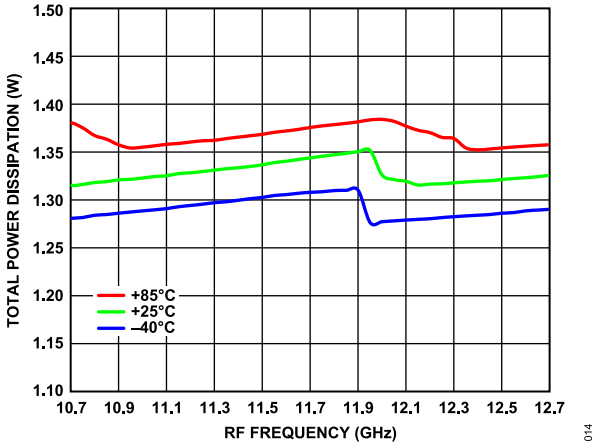



*Figure 10. Total Power Dissipation vs. RF Frequency over Temperature, LNA Low Gain Mode*

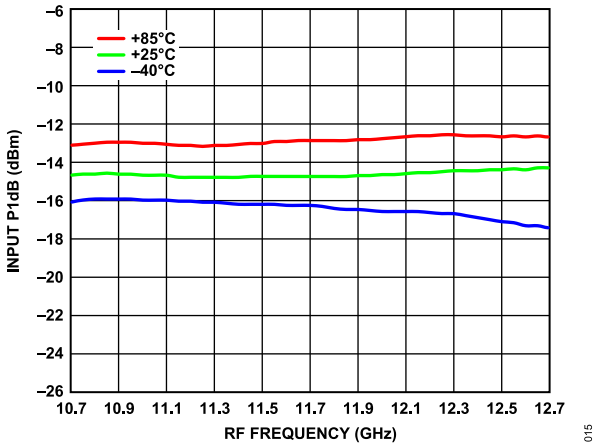



*Figure 11. Input P1dB vs. RF Frequency over Temperature, LNA High Gain Mode*

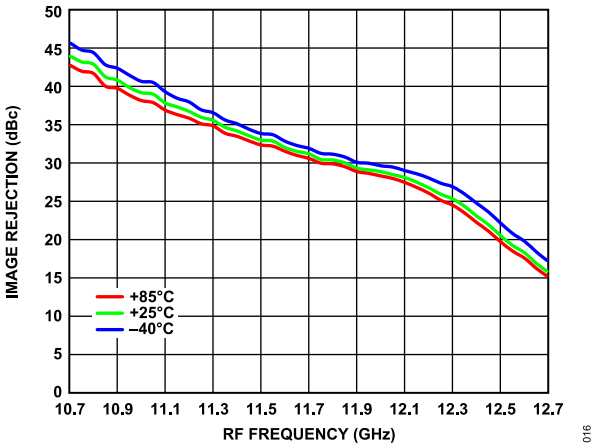



*Figure 12. Image Rejection vs. RF Frequency over Temperature, LNA High Gain Mode*

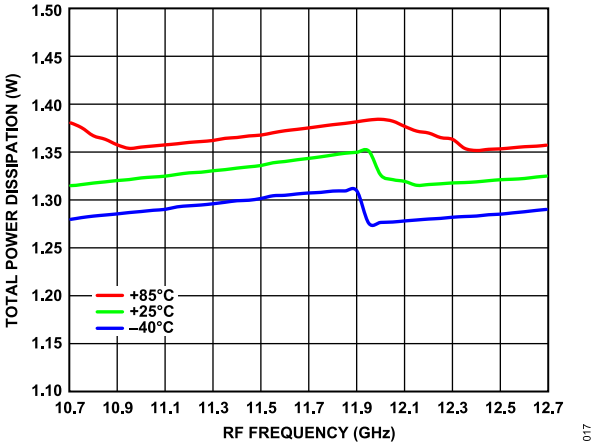



*Figure 13. Total Power Dissipation vs. RF Frequency over Temperature, LNA High Gain Mode*

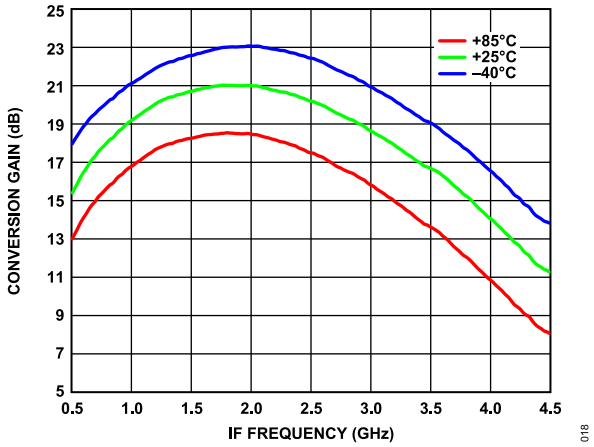



*Figure 14. Conversion Gain vs. IF Frequency over Temperature, LO Frequency = 10 GHz, LNA Low Gain Mode*

## TYPICAL PERFORMANCE CHARACTERISTICS

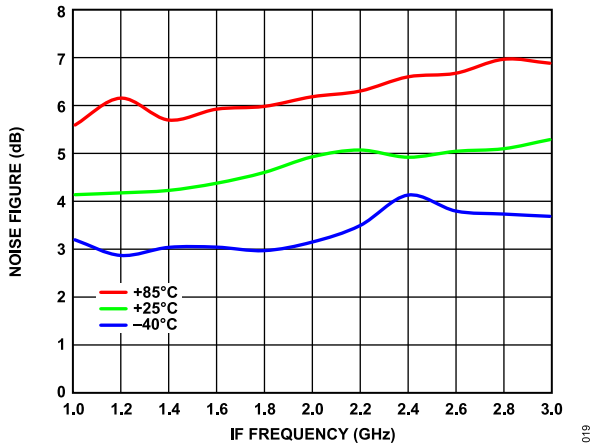



*Figure 15. Noise Figure vs. IF Frequency over Temperature, LO Frequency = 10 GHz, LNA Low Gain Mode*

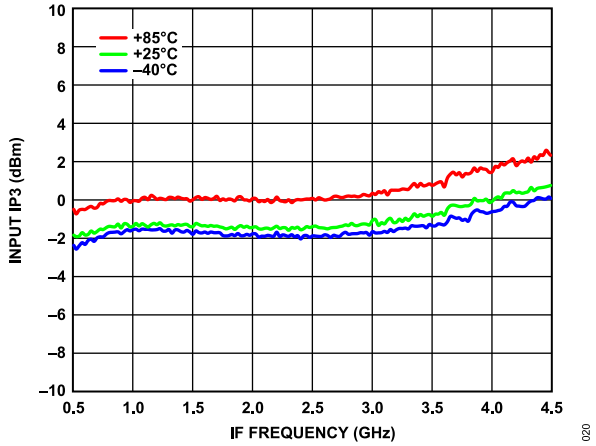



*Figure 16. Input IP3 vs. IF Frequency over Temperature, LO Frequency = 10 GHz, LNA Low Gain Mode*

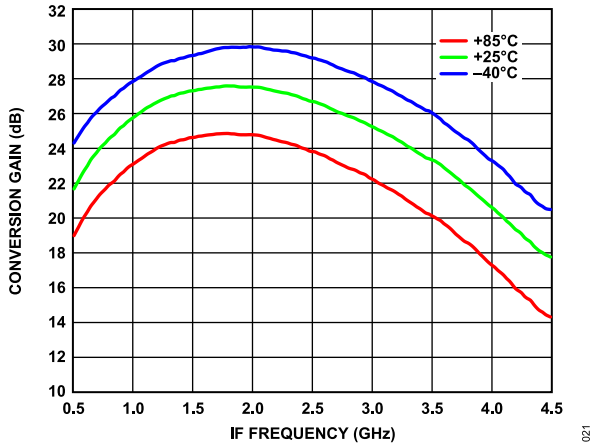



*Figure 17. Conversion Gain vs. IF Frequency over Temperature, LO Frequency = 10 GHz, LNA High Gain Mode*

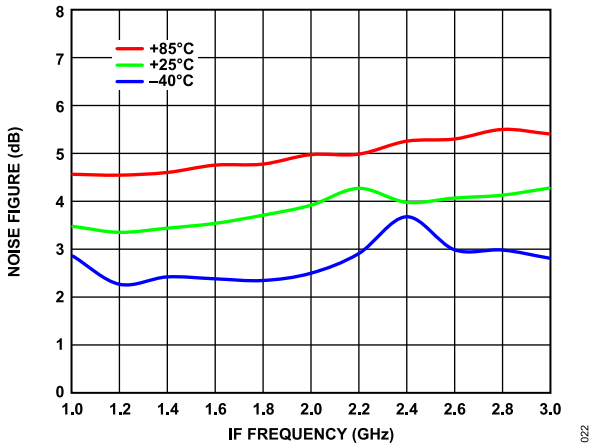



*Figure 18. Noise Figure vs. IF Frequency over Temperature, LO Frequency = 10 GHz, LNA High Gain Mode*

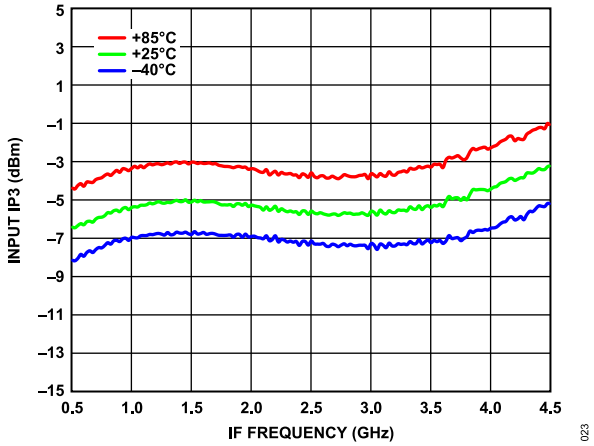



*Figure 19. Input IP3 vs. IF Frequency over Temperature, LO Frequency = 10 GHz, LNA High Gain Mode*

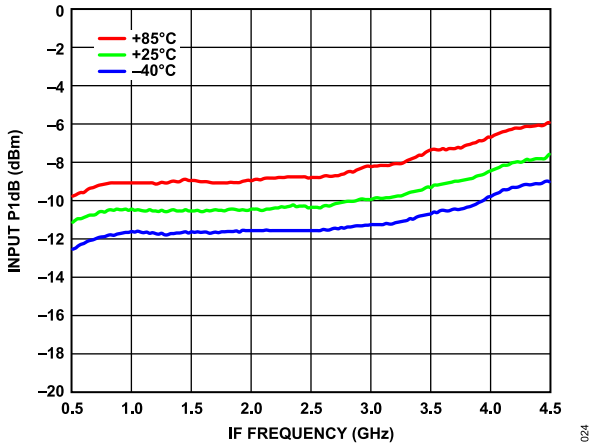



*Figure 20. Input P1dB vs. IF Frequency over Temperature, LO Frequency = 10 GHz, LNA Low Gain Mode*

## TYPICAL PERFORMANCE CHARACTERISTICS

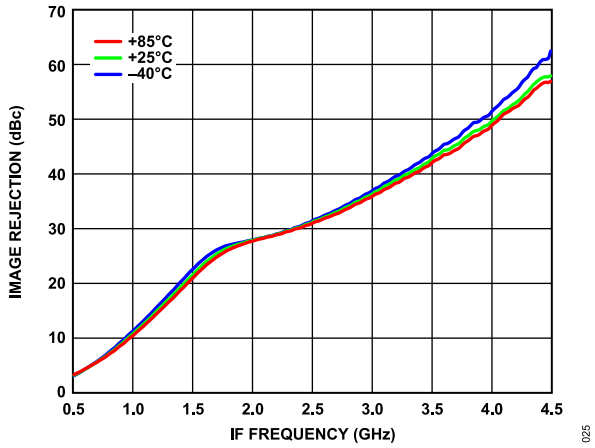



*Figure 21. Image Rejection vs. IF Frequency over Temperature, LO Frequency = 10 GHz, LNA Low Gain Mode*

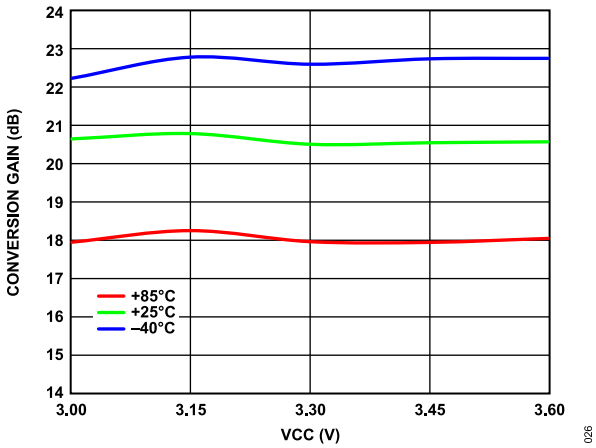



*Figure 22. Conversion Gain vs. VCC over Temperature, LO Frequency = 10 GHz, LNA Low Gain Mode*

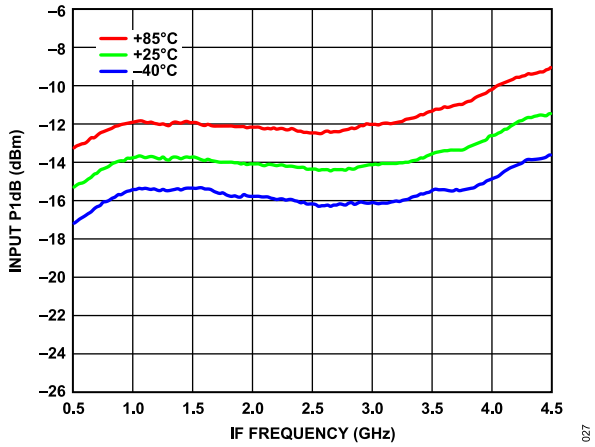



*Figure 23. Input P1dB vs. IF Frequency over Temperature, LO Frequency = 10 GHz, LNA High Gain Mode*

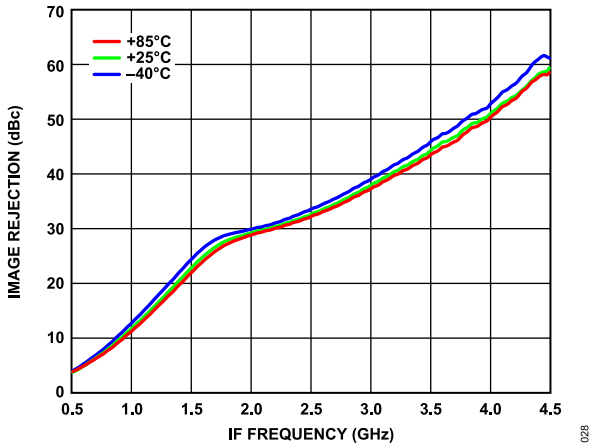



*Figure 24. Image Rejection vs. IF Frequency over Temperature, LO Frequency = 10 GHz, LNA High Gain Mode*

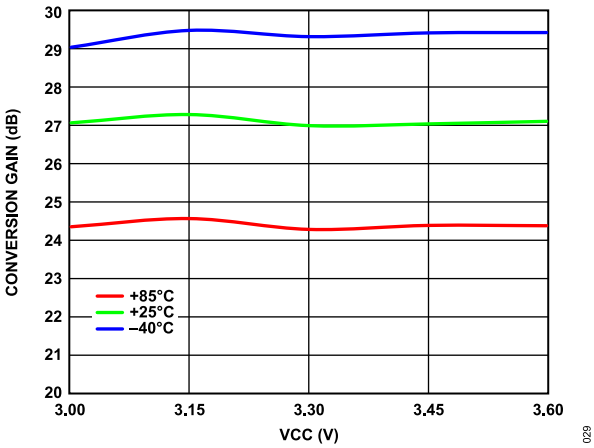



*Figure 25. Conversion Gain vs. VCC over Temperature, LO Frequency = 10 GHz, LNA High Gain Mode*

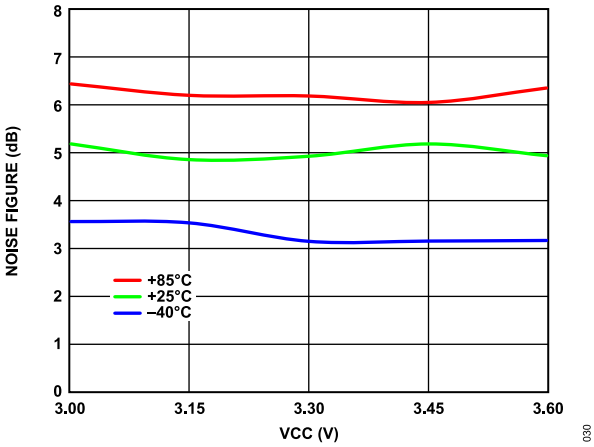



*Figure 26. Noise Figure vs. VCC over Temperature, LO Frequency = 10 GHz, LNA Low Gain Mode*

## TYPICAL PERFORMANCE CHARACTERISTICS

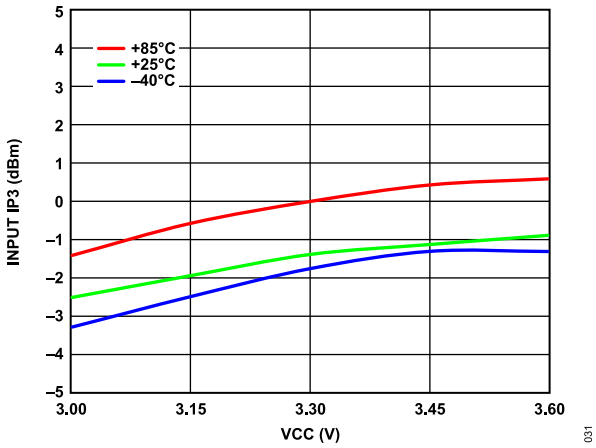



*Figure 27. Input IP3 vs. VCC over Temperature, LO Frequency = 10 GHz, LNA Low Gain Mode*

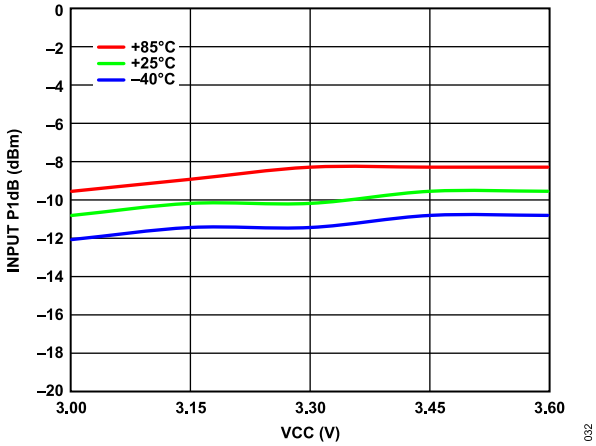



*Figure 28. Input P1dB vs. VCC over Temperature, LO Frequency = 10 GHz, LNA Low Gain Mode*

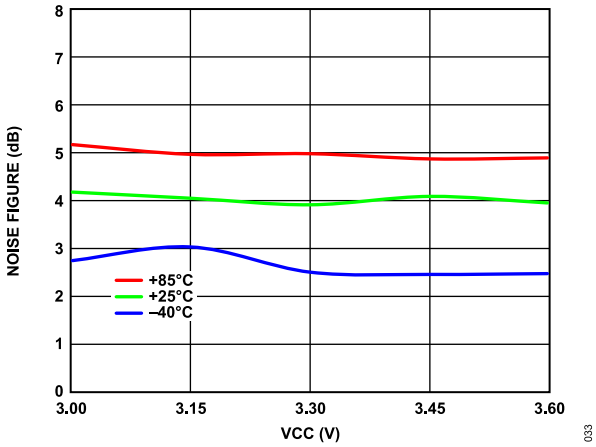



*Figure 29. Noise Figure vs. VCC over Temperature, LO Frequency = 10 GHz, LNA High Gain Mode*

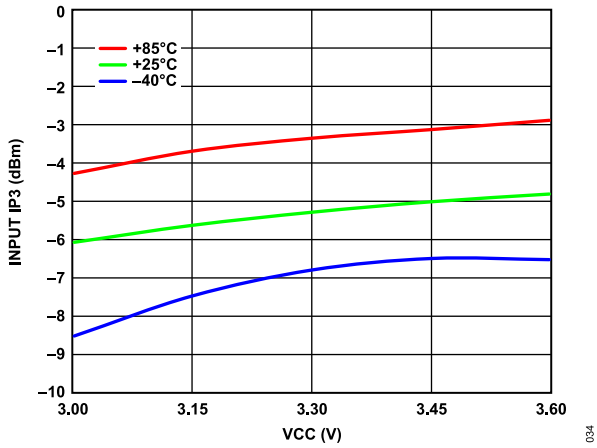



*Figure 30. Input IP3 vs. VCC over Temperature, LO Frequency = 10 GHz, LNA High Gain Mode*

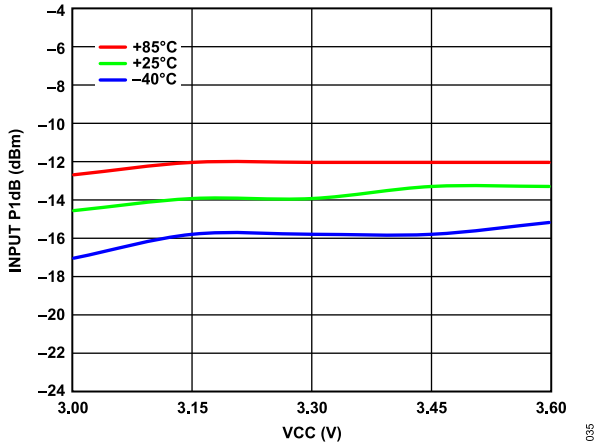



*Figure 31. Input P1dB vs. VCC over Temperature, LO Frequency = 10 GHz, LNA High Gain Mode*

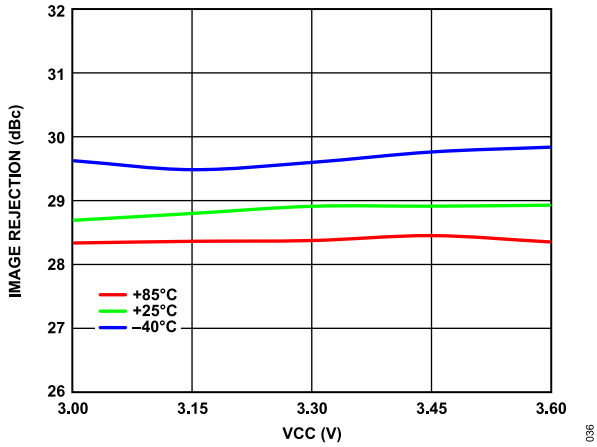



*Figure 32. Image Rejection vs. VCC over Temperature, LO Frequency = 10 GHz, LNA Low Gain Mode*

## TYPICAL PERFORMANCE CHARACTERISTICS

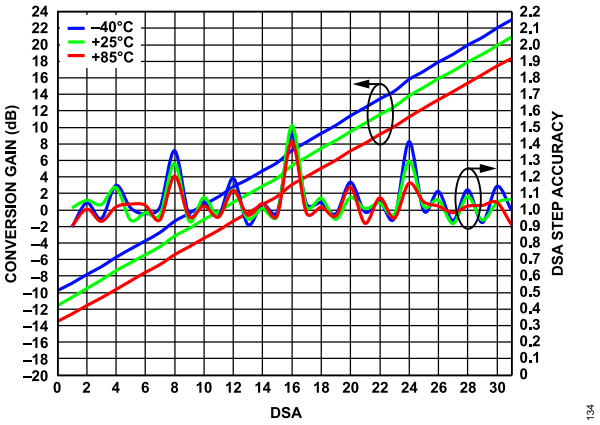



*Figure 33. Conversion Gain and DSA Step Accuracy vs. DSA over Temperature, LO Frequency = 10 GHz, LNA Low Gain Mode*

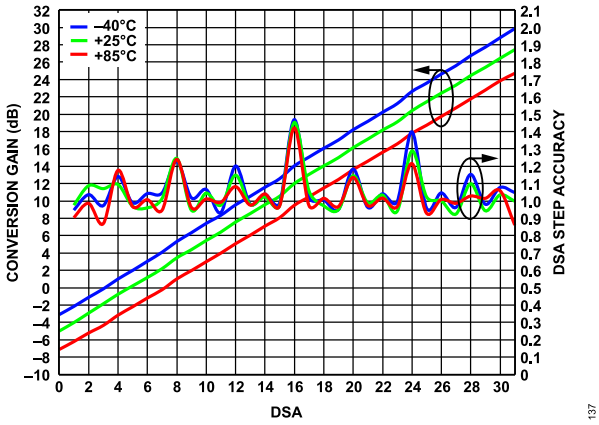



*Figure 36. Conversion Gain and DSA Step Accuracy vs. DSA over Temperature, LO Frequency = 10 GHz, LNA High Gain Mode*

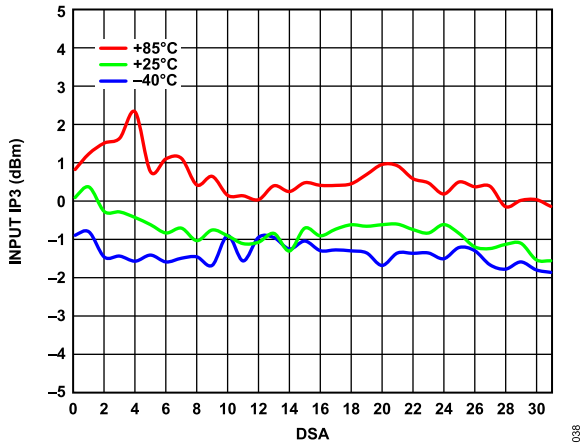



*Figure 34. Input IP3 vs. DSA over Temperature, LO Frequency = 10 GHz, LNA Low Gain Mode*

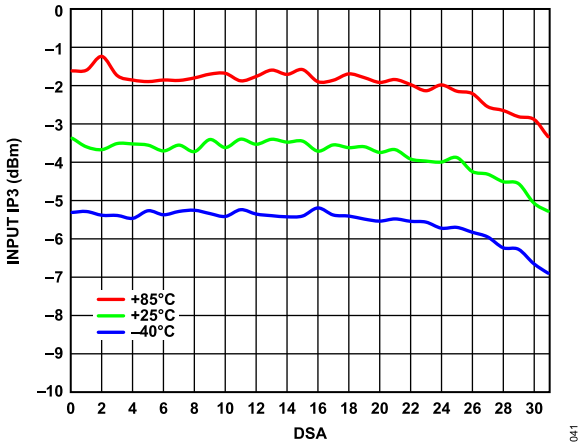



*Figure 37. Input IP3 vs. DSA over Temperature, LO Frequency = 10 GHz, LNA High Gain Mode*

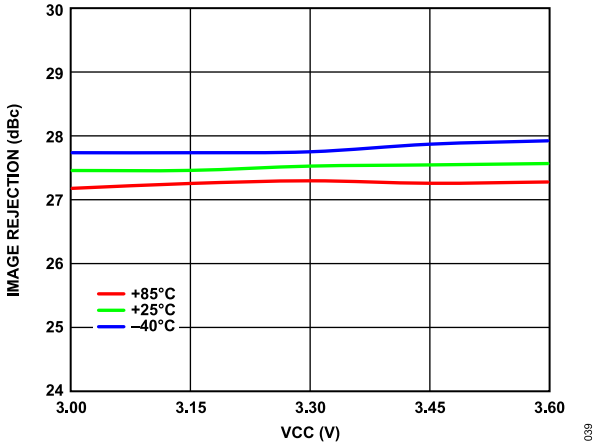



*Figure 35. Image Rejection vs. VCC over Temperature, LO Frequency = 10 GHz, LNA High Gain Mode*

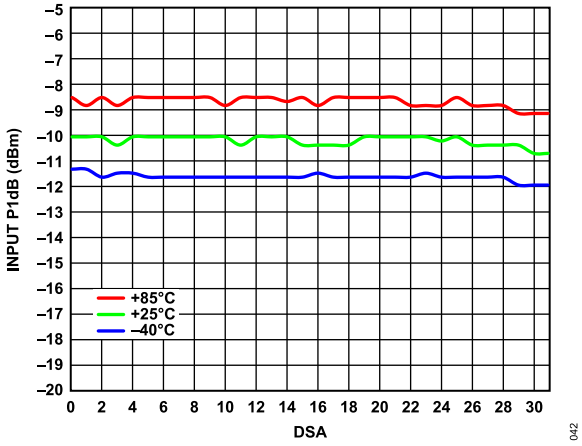



*Figure 38. Input P1dB vs. DSA over Temperature, LO Frequency = 10 GHz, LNA Low Gain Mode*

## TYPICAL PERFORMANCE CHARACTERISTICS

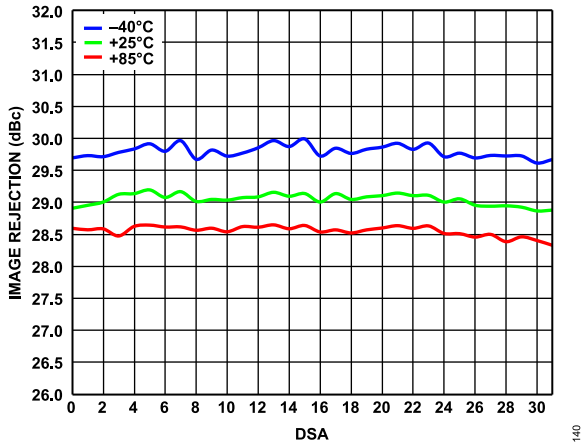



*Figure 39. Image Rejection vs. DSA over Temperature, LO Frequency = 10 GHz, LNA Low Gain Mode*

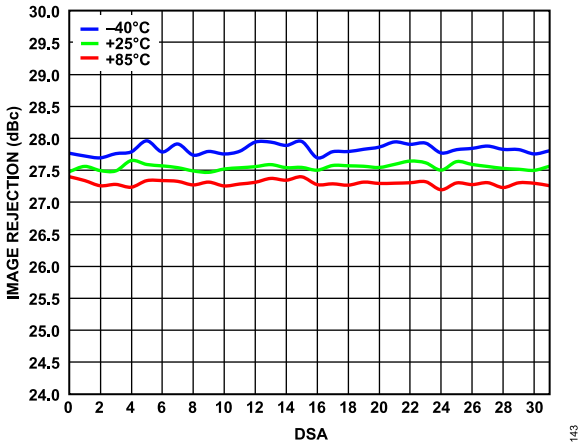



*Figure 42. Image Rejection vs. DSA over Temperature, LO Frequency = 10 GHz, LNA High Gain Mode*

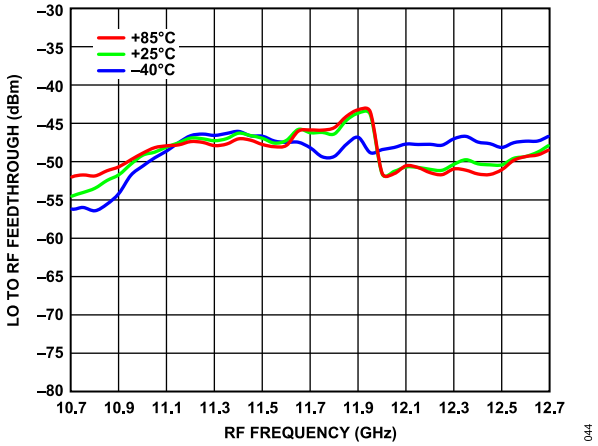



*Figure 40. LO to RF Feedthrough vs. RF Frequency over Temperature, LNA Low Gain Mode*

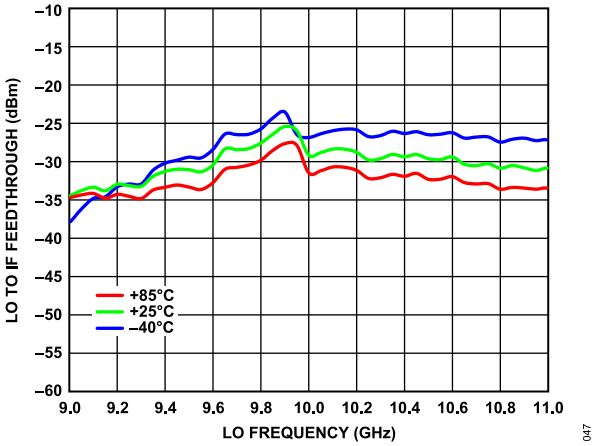



*Figure 43. LO to IF Feedthrough vs. LO Frequency over Temperature, LNA Low Gain Mode*

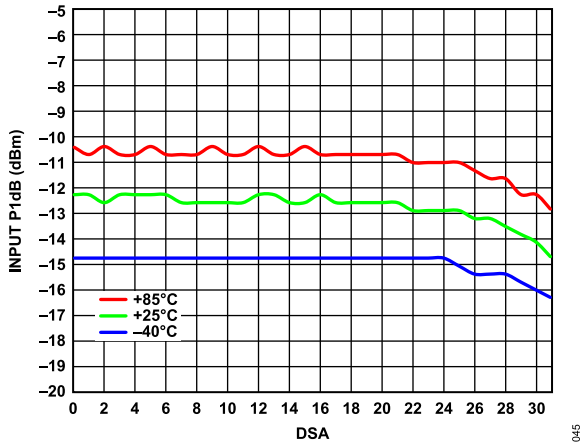



*Figure 41. Input P1dB vs. DSA over Temperature, LO Frequency = 10 GHz, LNA High Gain Mode*

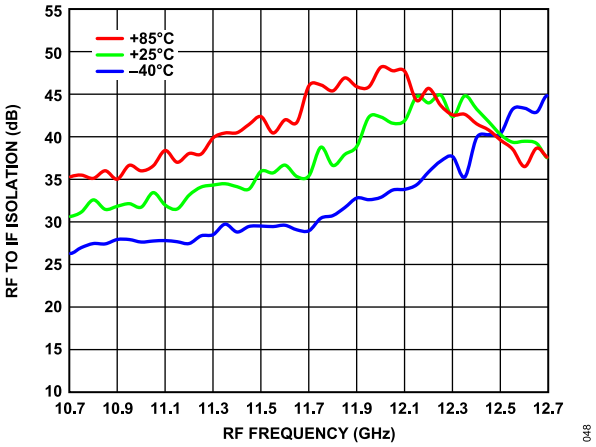



*Figure 44. RF to IF Isolation vs. RF Frequency over Temperature, LNA Low Gain Mode*

## TYPICAL PERFORMANCE CHARACTERISTICS

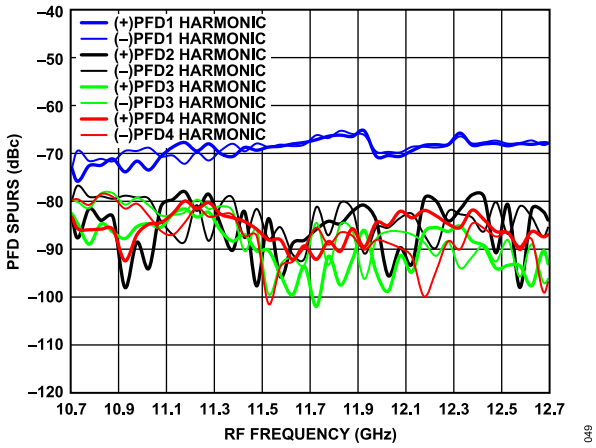



*Figure 45. Phase Frequency Detector (PFD) Spurs vs. RF Frequency, LNA Low Gain Mode, Measured from IF Output Power Level*

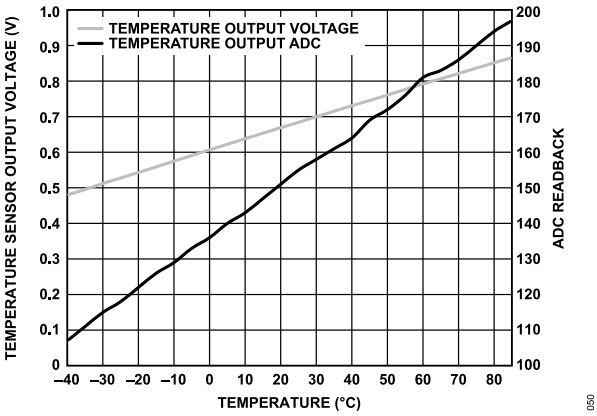



*Figure 46. Temperature Sensor Output Voltage and ADC Readback vs. Temperature, LO Frequency = 10 GHz*

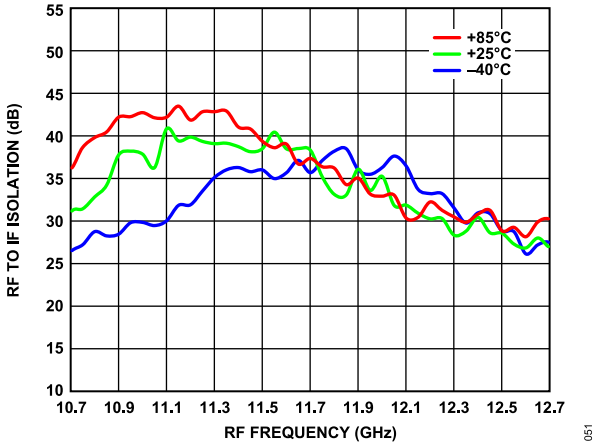



*Figure 47. RF to IF Isolation vs. RF Frequency over Temperature, LNA High Gain Mode*

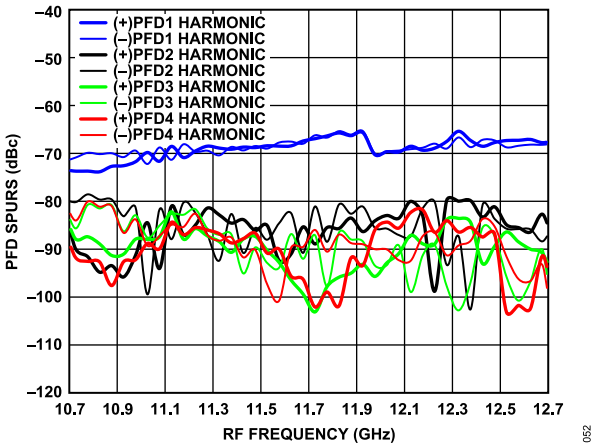



*Figure 48. PFD Spurs vs. RF Frequency, LNA High Gain Mode, Measured from IF Output Power Level*

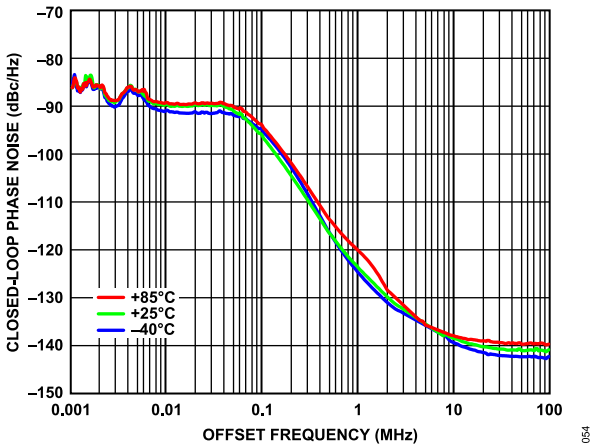



*Figure 49. Closed-Loop Phase Noise vs. Offset Frequency over Temperature, LO = 10 GHz*

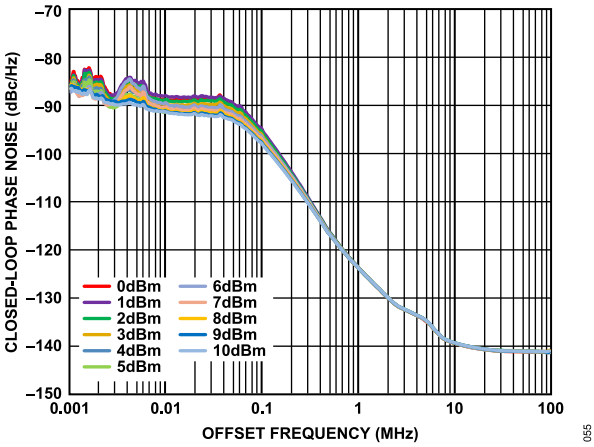



*Figure 50. Closed-Loop Phase Noise vs. Offset Frequency over Reference Input Power*

## TYPICAL PERFORMANCE CHARACTERISTICS

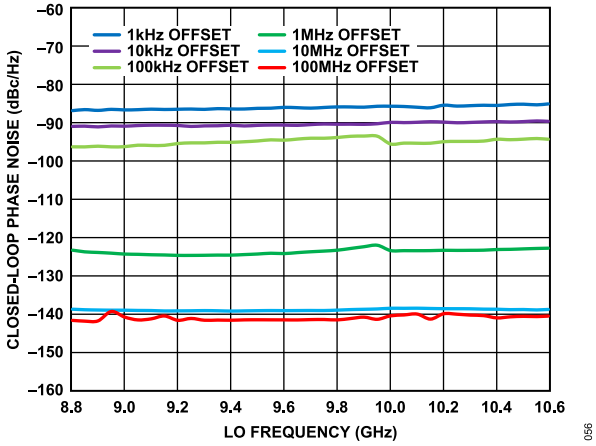



*Figure 51. Closed-Loop Phase Noise vs. LO Frequency over Offset Frequency*

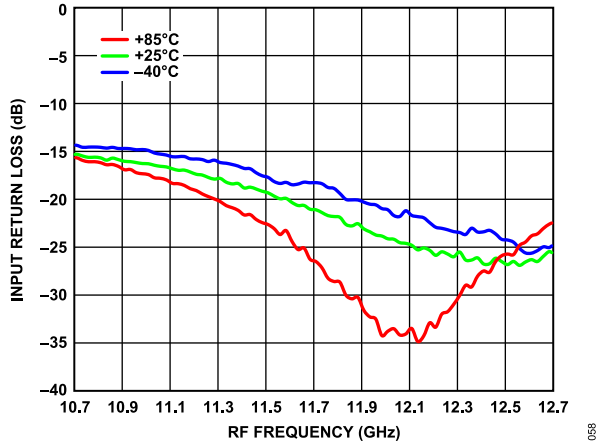



*Figure 53. Input Return Loss vs. RF Frequency over Temperature, LO Frequency = 10 GHz*

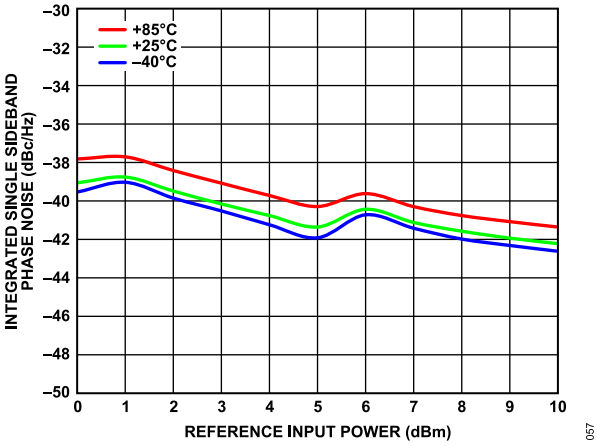



*Figure 52. Integrated Single Sideband Phase Noise vs. Reference Input Power over Temperature, Offset Frequency = 1 kHz to 125 MHz*

## TYPICAL PERFORMANCE CHARACTERISTICS

### MAXIMUM ATTENUATION PERFORMANCE: DSA (REGISTER 0X300) = 0

$T_A$ = 25°C, IF = 2 GHz, VCC = 3.3 V, clock reference input power = 3 dBm, upper sideband selected, unless otherwise noted.

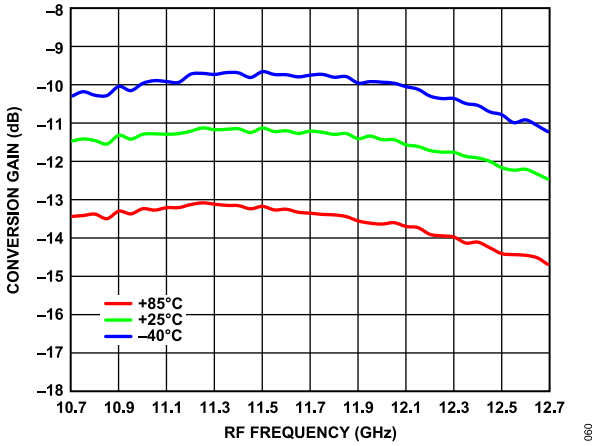



*Figure 54. Conversion Gain vs. RF Frequency over Temperature, LNA Low Gain Mode*

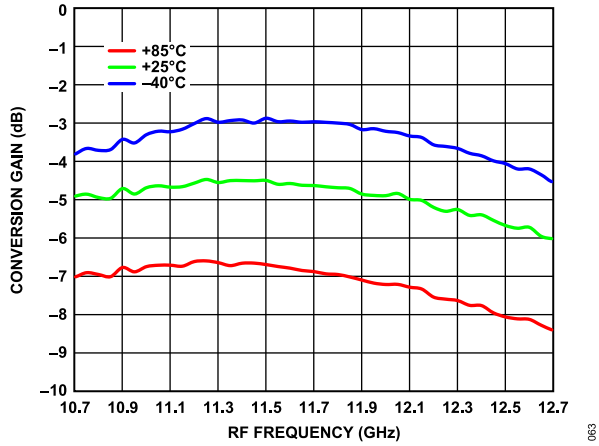



*Figure 57. Conversion Gain vs. RF Frequency over Temperature, LNA High Gain Mode*

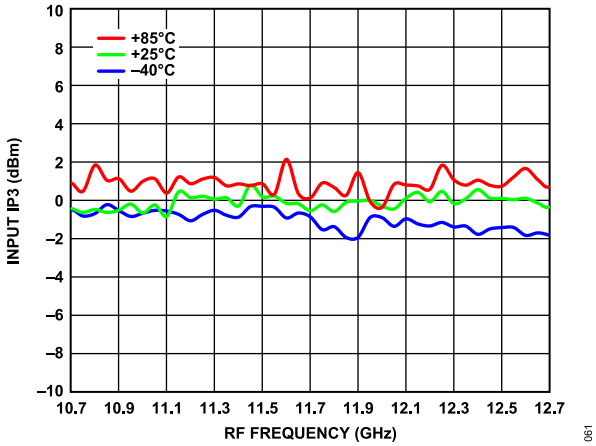



*Figure 55. Input IP3 vs. RF Frequency over Temperature, LNA Low Gain Mode*

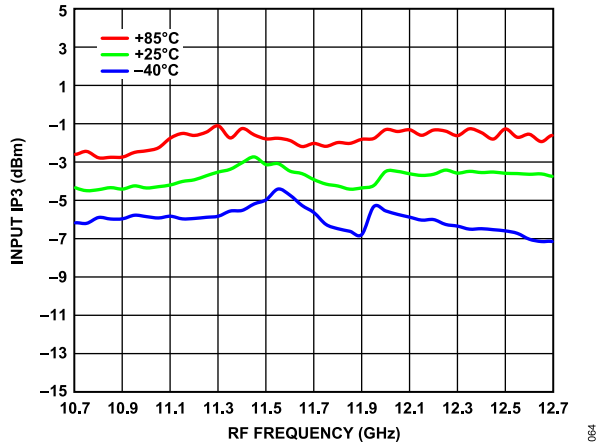



*Figure 58. Input IP3 vs. RF Frequency over Temperature, LNA High Gain Mode*

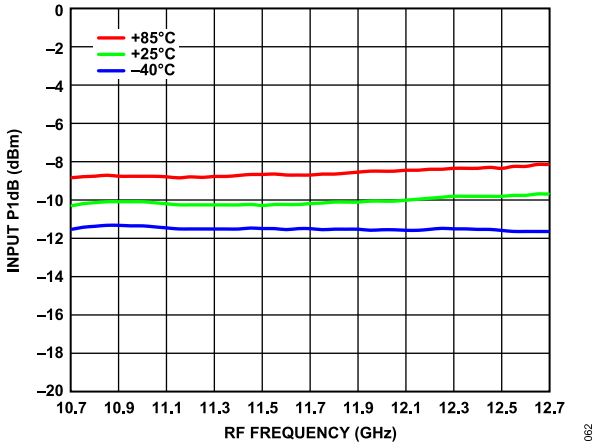



*Figure 56. Input P1dB vs. RF Frequency over Temperature, LNA Low Gain Mode*

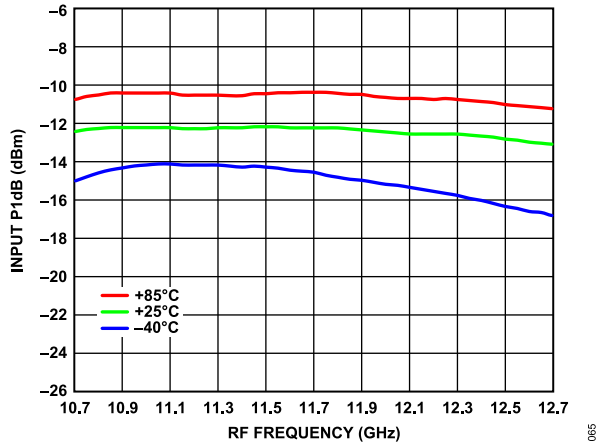



*Figure 59. Input P1dB vs. RF Frequency over Temperature, LNA High Gain Mode*

## TYPICAL PERFORMANCE CHARACTERISTICS

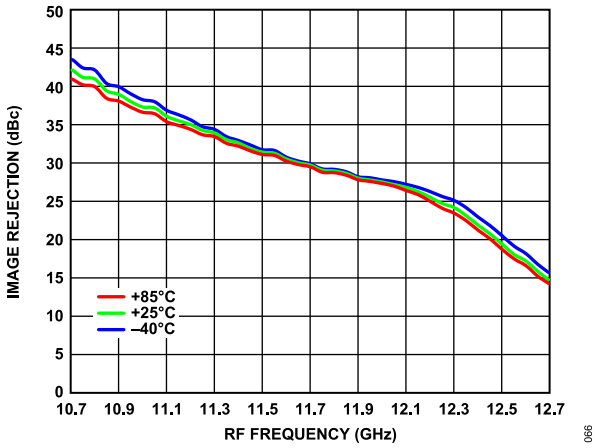



*Figure 60. Image Rejection vs. RF Frequency over Temperature, LNA Low Gain Mode*

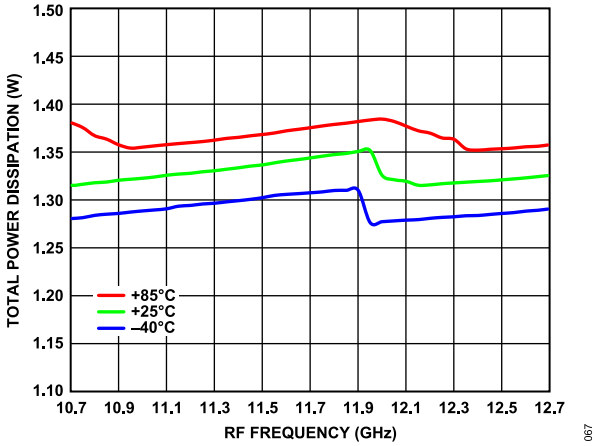



*Figure 61. Total Power Dissipation vs. RF Frequency over Temperature, LNA Low Gain Mode*

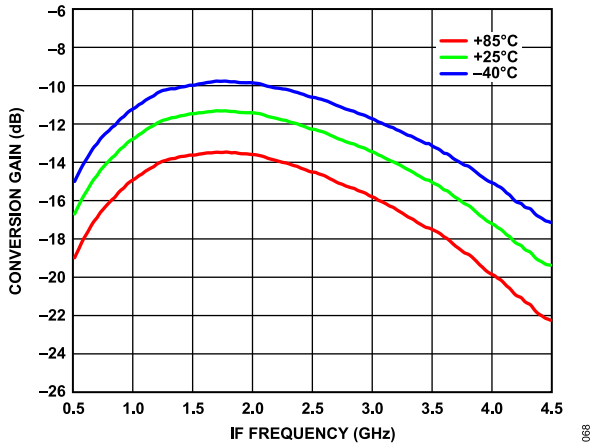



*Figure 62. Conversion Gain vs. IF Frequency over Temperature, LNA Low Gain Mode*

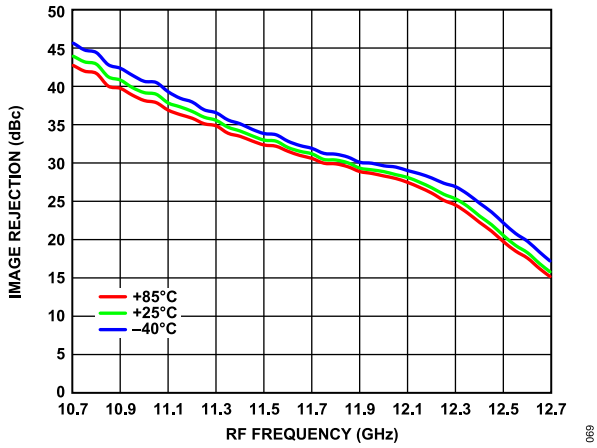



*Figure 63. Image Rejection vs. RF Frequency over Temperature, LNA High Gain Mode*

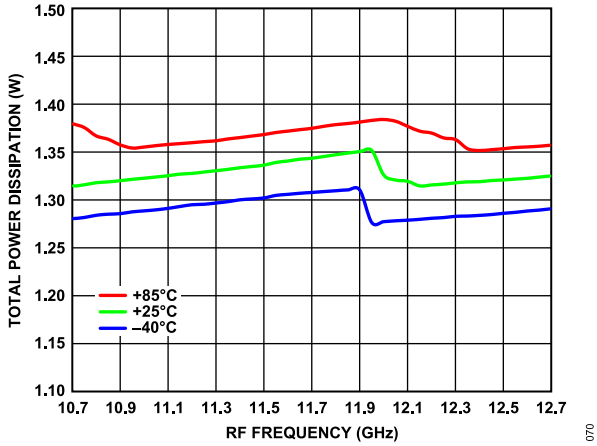



*Figure 64. Total Power Dissipation vs. RF Frequency over Temperature, LNA High Gain Mode*

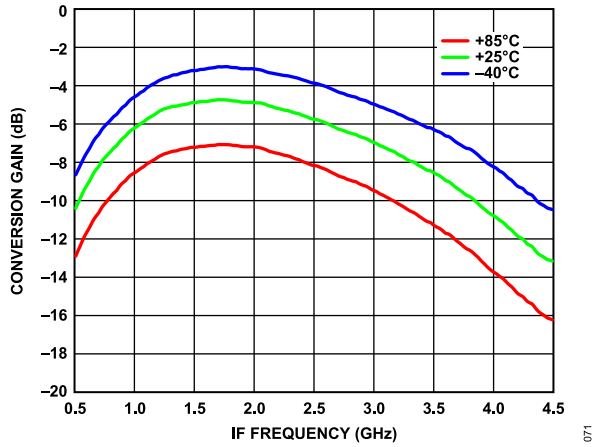



*Figure 65. Conversion Gain vs. IF Frequency over Temperature, LNA High Gain Mode*

## TYPICAL PERFORMANCE CHARACTERISTICS

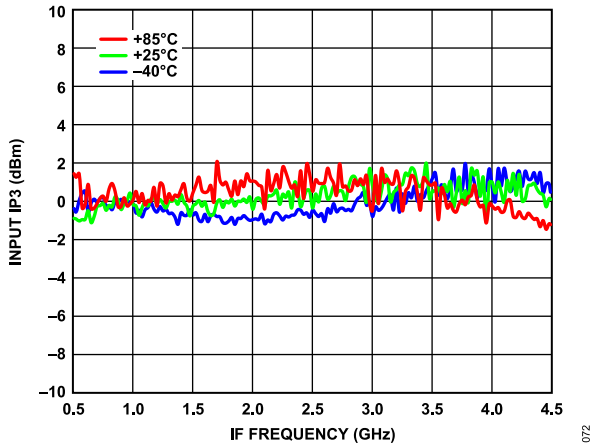



*Figure 66. Input IP3 vs. IF Frequency over Temperature, LNA Low Gain Mode*

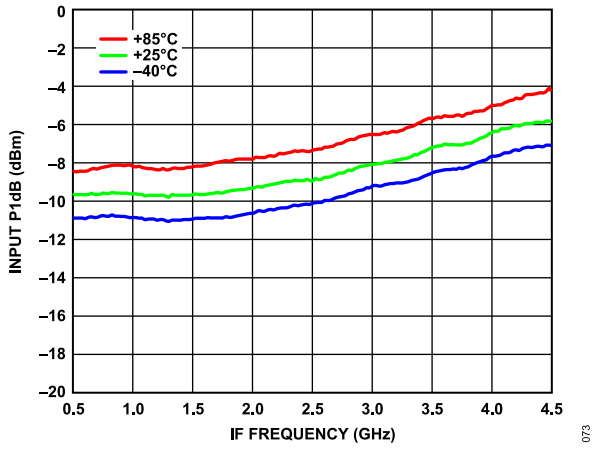



*Figure 67. Input P1dB vs. IF Frequency over Temperature, LNA Low Gain Mode*

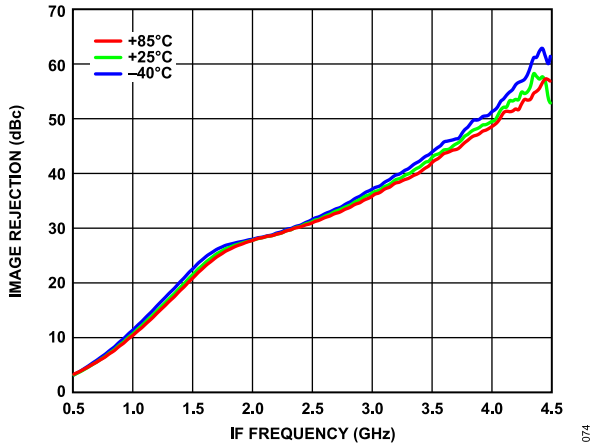



*Figure 68. Image Rejection vs. IF Frequency over Temperature, LNA Low Gain Mode*

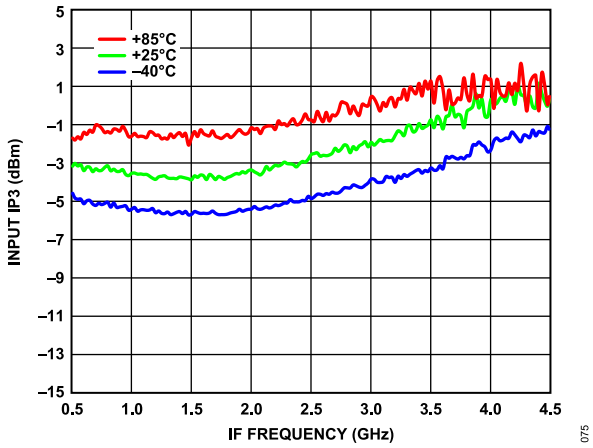



*Figure 69. Input IP3 vs. IF Frequency over Temperature, LNA High Gain Mode*

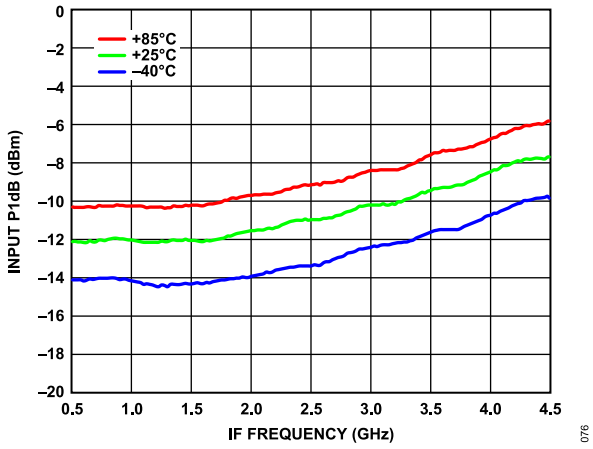



*Figure 70. Input P1dB vs. IF Frequency over Temperature, LNA High Gain Mode*

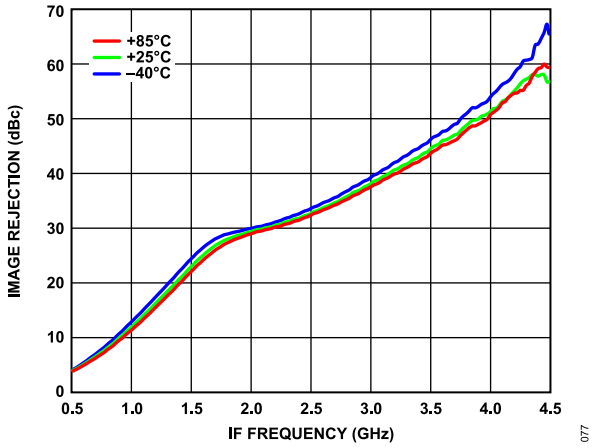



*Figure 71. Image Rejection vs. IF Frequency over Temperature, LNA High Gain Mode*

## TYPICAL PERFORMANCE CHARACTERISTICS

### SPURIOUS PERFORMANCE

$T_A$ = 25°C, IF = 2 GHz, VCC = 3.3 V, minimum attenuation (DSA Register 0x300 = 31), clock reference input power = 3 dBm, upper sideband selected. Mixer spurious products are measured in dBc from the IF output power level. Spur values are (M × RF) − (N × LO).

### M × N Spurious Outputs, RF = 10.7 GHz, LO = 8.7 GHz, LNA Low Gain Mode

| | | N × LO | | | | | |
|---|---|---|---|---|---|---|---|
| | | 0 | 1 | 2 | 3 | 4 | 5 |
| M × RF | 0 | N/A | 18 | 27 | 35 | ≥100 | ≥100 |
| | 1 | 52 | 0 | 46 | 60 | 92 | ≥100 |
| | 2 | 83 | 92 | 67 | 79 | 78 | ≥100 |
| | 3 | ≥100 | ≥100 | ≥100 | ≥100 | ≥100 | ≥100 |
| | 4 | ≥100 | ≥100 | ≥100 | ≥100 | ≥100 | 88 |
| | 5 | ≥100 | ≥100 | ≥100 | ≥100 | ≥100 | 98 |

### M × N Spurious Outputs, RF = 10.7 GHz, LO = 8.7 GHz, LNA High Gain Mode

| | | N × LO | | | | | |
|---|---|---|---|---|---|---|---|
| | | 0 | 1 | 2 | 3 | 4 | 5 |
| M × RF | 0 | N/A | 33 | 34 | 41 | ≥100 | ≥100 |
| | 1 | 59 | 0 | 44 | 62 | 88 | ≥100 |
| | 2 | 81 | 82 | 60 | 80 | 72 | ≥100 |
| | 3 | ≥100 | ≥100 | ≥100 | 78 | 83 | ≥100 |
| | 4 | ≥100 | ≥100 | ≥100 | ≥100 | ≥100 | 90 |
| | 5 | ≥100 | ≥100 | ≥100 | ≥100 | ≥100 | ≥100 |

### M × N Spurious Outputs, RF = 11.7 GHz, LO = 9.7 GHz, LNA Low Gain Mode

| | | N × LO | | | | | |
|---|---|---|---|---|---|---|---|
| | | 0 | 1 | 2 | 3 | 4 | 5 |
| M × RF | 0 | N/A | 18 | 39 | ≥100 | ≥100 | ≥100 |
| | 1 | 58 | 0 | 53 | 57 | ≥100 | ≥100 |
| | 2 | 81 | 86 | 69 | 79 | 81 | ≥100 |
| | 3 | ≥100 | ≥100 | ≥100 | 91 | ≥100 | ≥100 |
| | 4 | ≥100 | ≥100 | ≥100 | ≥100 | ≥100 | 99 |
| | 5 | ≥100 | ≥100 | ≥100 | ≥100 | ≥100 | 95 |

### M × N Spurious Outputs, RF = 11.7 GHz, LO = 9.7 GHz, LNA High Gain Mode

| | | N × LO | | | | | |
|---|---|---|---|---|---|---|---|
| | | 0 | 1 | 2 | 3 | 4 | 5 |
| M × RF | 0 | N/A | 25 | 44 | ≥100 | ≥100 | ≥100 |
| | 1 | 67 | 0 | 51 | 58 | ≥100 | ≥100 |
| | 2 | 77 | 80 | 62 | 71 | 73 | ≥100 |
| | 3 | ≥100 | ≥100 | ≥100 | 75 | 86 | ≥100 |
| | 4 | ≥100 | ≥100 | ≥100 | ≥100 | ≥100 | ≥100 |
| | 5 | ≥100 | ≥100 | ≥100 | ≥100 | ≥100 | ≥100 |

### M × N Spurious Outputs, RF = 12.7 GHz, LO = 10.7 GHz, LNA Low Gain Mode

| | | N × LO | | | | | |
|---|---|---|---|---|---|---|---|
| | | 0 | 1 | 2 | 3 | 4 | 5 |
| M × RF | 0 | N/A | 21 | 43 | ≥100 | ≥100 | ≥100 |
| | 1 | 58 | 0 | 60 | 65 | ≥100 | ≥100 |
| | 2 | 87 | 87 | 73 | 87 | 97 | ≥100 |
| | 3 | ≥100 | ≥100 | ≥100 | 86 | ≥100 | ≥100 |
| | 4 | ≥100 | ≥100 | ≥100 | ≥100 | ≥100 | 85 |
| | 5 | ≥100 | ≥100 | ≥100 | ≥100 | ≥100 | 97 |

### M × N Spurious Outputs, RF = 12.7 GHz, LO = 10.7 GHz, LNA High Gain Mode

| | | N × LO | | | | | |
|---|---|---|---|---|---|---|---|
| | | 0 | 1 | 2 | 3 | 4 | 5 |
| M × RF | 0 | N/A | 27 | 48 | ≥100 | ≥100 | ≥100 |
| | 1 | 52 | 0 | 59 | 67 | ≥100 | ≥100 |
| | 2 | 84 | 82 | 69 | 99 | 88 | ≥100 |
| | 3 | ≥100 | ≥100 | ≥100 | 76 | 96 | ≥100 |
| | 4 | ≥100 | ≥100 | ≥100 | ≥100 | ≥100 | 89 |
| | 5 | ≥100 | ≥100 | ≥100 | ≥100 | ≥100 | ≥100 |

## THEORY OF OPERATION

The ADMV4640 is a microwave downconverter optimized for various SATCOM user terminals operating in the 10.7 GHz to 12.7 GHz frequency range. See Figure 1 for a functional block diagram of the device. The ADMV4640 digital settings are controlled via the SPI.

### REFERENCE INPUT STAGE

The reference input stage, as shown in Figure 72, can be driven by an external, singled-ended 25 MHz source. Ensure the external dc block is used at the reference input.

### REFERENCE DOUBLER, R COUNTER, AND REFERENCE DIVIDE BY 2

An internal, reference doubler (×2 doubler block, see Figure 72) generates higher phase frequency detector frequencies ($f_{PFD}$). Use the DOUBLER_EN bit (Register 0x20E, Bit 3) to enable the reference doubler.

There are two frequency dividers: a 5-bit R divider counter (1 to 32 allowed) and a divide by 2 (÷2 block, see Figure 72). These dividers divide the input reference frequency ($f_{REF}$) down to produce a lower $f_{PFD}$. Use the R_DIV bits in Register 0x20C, Bits[4:0] to set the R counter.

The reference divide by 2 block is enabled by using the RDIV2_SEL bit (Register 0x20E, Bit 0).

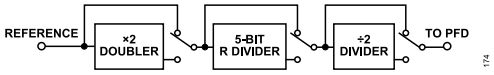



*Figure 72. Reference Input Path Block Diagram*

### INT MODE AND N COUNTER

The ADMV4640 synthesizer operates in INT mode.

The N counter allows a division ratio in the phase-locked loop (PLL) feedback path from the VCO. The division ratio is determined by the INT bit value. Use Register 0x200 and Register 0x201 to set the INT bit values.

The INT bit value, in conjunction with the reference path, allows VCO frequencies spaced by the resolution of the $f_{PFD}$ to be generated.

To calculate $f_{PFD}$ with $f_{REF}$ and the reference path configuration parameters, use the following equation:

$$f_{PFD} = f_{REF} \times \frac{1 + D}{R \times (1 + T)} \quad (1)$$

where:
*D* is the reference doubler bit (0 or 1).
*R* is the reference divide ratio of the binary, 5-bit programmable counter (1 to 31).
*T* is the reference divide by 2 bit (0 or 1).

To calculate the VCO frequency ($f_{VCO}$), use the following equation:

$$f_{VCO} = \frac{f_{LO}}{2} = f_{PFD} \times N \quad (2)$$

where:
$f_{LO}$ is the frequency of the LO driving the mixer.
*N* is the desired value of INT, where INT is the 16-bit integer value (0 to 65,535).

### PHASE FREQUENCY DETECTOR (PFD) AND CP

The PFD takes inputs from the R counter and N counter to produce an output that is proportional to the phase and frequency differences between them. This proportional information is output to a CP circuit that generates current to drive an external loop filter. The loop filter is used to appropriately increase or decrease the VTUNE tuning voltage.

Figure 73 shows a simplified schematic of the PFD and CP. U1 and U2 are two D type flip flops and U3 is an AGND gate. The PFD has a fixed delay element that is used to ensure that there is no dead zone in the PFD transfer function for consistent reference spur levels.

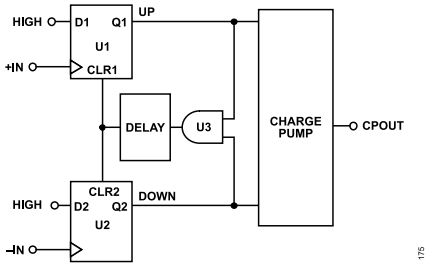



*Figure 73. PFD and CP Simplified Schematic*

### LOOP FILTER AND CP CURRENT

Defining a loop filter for a PLL depends on the PFD frequency, the N counter value, the tuning sensitivity characteristics ($k_{VCO}$) of the VCO, and the selected CP current. A lower $f_{PFD}$ allows the PLL to operate in INT mode, which can eliminate integer boundary spurs at the expense of higher in-band phase noise performance. Take care with frequency planning and $f_{PFD}$ selection to ensure that the appropriate in band phase noise performance is met with acceptable spur levels for the end application.

The loop filter, as implemented on the ADMV4640-EVALZ evaluation board, is shown in Figure 74. The CP current ($I_{CP}$) is set by Register 0x22E. The default register value of 0x0E is recommended.

For additional guidance with loop filter simulations on the ADMV4640, contact Analog Devices, Inc., for technical support.

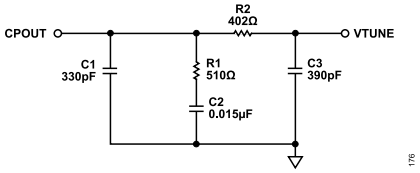



*Figure 74. Recommended Loop Filter Schematic*

## THEORY OF OPERATION

### ON-CHIP MUXOUT PIN

The MUXOUT pin allows access to various internal signals and provides a digital lock detect function. A diagram of the MUXOUT pin is shown in Figure 75. The state of the MUXOUT pin is determined from the MUX_SEL value in Register 0x24E.

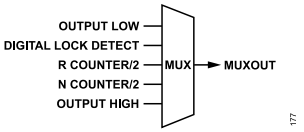



*Figure 75. MUXOUT Pin Diagram*

### ANALOG MUX BLOCK, AGPIO PIN, AND ADC

The on-chip AGPIO pin can be used either as an external analog input or output of the device analog multiplexer (mux) signal. The analog mux is a block inside the ADMV4640. When the AGPIO signal is used as an input, the signal is transferred to the on-chip analog mux. The analog mux selects between the temperature sensor and the AGPIO signal. An on-chip ADC samples the signals from the analog mux.

To enable the ADC to sample the analog mux signal, take the following steps:

1. Make sure the reference input is fed to ADMV4640.
2. Set Register 0x301, Bits[2:0] to 6 or 7 to select between the temperature sensor and AGPIO signal as the analog mux output. If the AGPIO signal is selected, set Register 0x301, Bit 3 to 1 so that AGPIO becomes the external signal input.
3. Set Register 0x302, Bits[3:0] to 0x00 to disable the ADC log scale and reset ADC.
4. Set Register 0x302 Bits[1:0] to 0x03 to enable and start ADC sampling.
5. Wait for 1ms.
6. Set Register 0x302, Bit 1 to 0.
7. Read the ADC value from Register 0x304.
8. Set Register 0x302, Bits[1:0] to 0x00 to turn off the ADC.

The default ADC input voltage range is 0 V to 1.1 V. If a higher input range is required, set Register 0x302, Bit 2 to 1 to halve the input voltage before sampling. The voltage range is then 0 V to 2.2 V.

Enable or disable the ADC output log scale by setting Register 0x302, Bit 3 to 1 or 0.

The AGPIO pin can also be used as an output to transfer the analog mux signal to the AGPIO pin. To set the AGPIO pin as the output, take the following steps:

1. Set Register 0x301, Bit 3 to 0 to set the AGPIO pin to be the output of the internal analog mux signal.
2. Set the value of Register 0x301, Bits[2:0] to 110 to select the temperature sensor as the analog mux output.
3. Set Register 0x302, Bit 0 to 0 to turn off the ADC.

### GPIOX PINS

There are three GPIOx pins for input/output (I/O) control. Use Register 0x307 to set the GPIO settings and see the Register Details section for more details.

### DIGITAL LOCK DETECT AND MUTE_IF_UNLOCKED BIT

The digital lock detect function is output on the MUXOUT pin and has two adjustable settings in Register 0x214. The first setting, LD_BIAS, adjusts an internal precision window. The second setting, LD_COUNT, adjusts the consecutive cycle count to declare the PLL lock. Keep the default register value for these two settings. The lock detect status can also be obtained from Register 0x24D, Bit 0.

The MUTE_IF_UNLOCKED bit (Register 0x103, Bit 0) allows the output to be muted if the PLL is unlocked. Set the bit to 1 to enable this function.

### SIGNAL CHAIN BIAS REGISTER, MASK REGISTER, RX_MUTE PIN, AND RXON PIN

RXON and RX_MUTE are two on-chip pins. These pins are signal masks that command the chip to block certain stages. These two pins can be pulled to high (3.3 V) or low (ground). Use the mute-mask control register (Register 0x101) and the on-mask control register (Register 0x102) to determine which stages in the signal path are masked by these two pins.

Register 0x100 (bias control), 0x101 (mute-mask control), and 0x102 (on-mask control) control the on/off status for each stage in the signal path.

Register 0x100 is a bias control register. Set each bit in this register to 1 or 0 to enable or disable the corresponding stage bias.

Register 0x101 is a mute-mask control register. Set each bit in this register to 1 to enable the RX_MUTE pin to mask the corresponding stage.

For example, when the LO amplifier mute-mask control bit is on (Register 0x101, Bit 1 = 1) and the RX_MUTE pin on the chip is pulled high, the LO amplifier is blocked.

Table 5 shows the truth table detailing how the RX_MUTE pin and the mute-mask control register work together to block signal stages. The MUTE_IF_UNLOCKED bit (Register 0x103, Bit 0) has the same muting effect as the RX_MUTE pin when enabled.

Register 0x102 is an on-mask control register. Set each bit in this register to 1 to enable the RX_ON pin to mask the corresponding stage. For the RX_ON pin to work, the corresponding stage bias control in Register 0x100 must be on and the RX_MUTE pin and mute-mask control register must be disabled.

For example, when the LO amplifier on-mask control bit is on (Register 0x102, Bit 1 = 1) and the RX_ON pin on the chip is pulled low, the LO amplifier is blocked.

## THEORY OF OPERATION

Table 6 shows the truth table detailing how the RX_ON pin and the on-mask control register work together to block signal stages.

### SPI CONFIGURATION

The ADMV4640 SPI configures the device for specific functions or operations via the 4-pin SPI port. This interface provides users with added flexibility and customization. The SPI consists of the following four control lines: SCLK, SDI, SDO, and $\overline{CS}$. The ADMV4640 protocol consists of a write or read bit followed by 15 register address bits and eight data bits. The address field and data field are organized LSB first and end with the MSB.

Set the MSB to 0 for a write operation and set the MSB to 1 for a read operation.

The write cycle sampling must be performed on the rising edge of the SCLK control line. The 24 bits of the serial write address and data are shifted in on the SDI control line, MSB to LSB. The ADMV4640 input logic level for the write cycle supports a 3.3 V interface.

For a read cycle, the read/write (R/W) bit and the 15 bits of address shift in on the rising edge of the SCLK pin on the SDI control line. Then, eight bits of serial read data shift out on the SDO pin LSB first and on the falling edge of SCLK. The output logic level for a read cycle is 3.3 V. The output drivers of the SDO pin are enabled after the last rising edge of SCLK of the instruction cycle and remain active until the end of the read cycle. When the $\overline{CS}$ control line is deasserted in a read operation, the SDO pin returns to high impedance until the next read transaction. The $\overline{CS}$ pin is active low and must be deasserted at the end of the write or read sequence.

An active low input on the $\overline{CS}$ pin starts and gates a communication cycle. The $\overline{CS}$ pin allows multiple ADMV4640 devices to be used on the same serial communications lines. The SDO pin goes to a high impedance state when the $\overline{CS}$ pin is high. During the communication cycle, the $\overline{CS}$ pin must stay low.

The SPI communications protocol follows the Analog Devices SPI standard. For more information, see the ADI-SPI Serial Control Interface Standard (Rev 1.0) guide.

### VCO AUTOCALIBRATION AND AUTOMATIC LEVEL CONTROL

The multicore VCO uses an internal autocalibration and automatic level control (ALC) routine that optimizes the VCO settings for a user defined frequency, and locks the PLL after the lower portion of the N counter integer value (Register 0x200) is programmed.

### DOUBLE BUFFERED REGISTERS

Register 0x20C, Register 0x20E, and Register 0x201 are double buffered registers that take effect only after a write to the lower portion of the integer value (INT_L, Register 0x200). Register 0x200 applies any changes to these double buffered registers and initiates the autocalibration routine.

The recommended programming sequence for double buffered registers is as follows:

1. Program R_DIV.
2. Program RDIV2_SEL.
3. Program DOUBLER_EN.
4. Program INT_H.
5. Program INT_L.

### INITIALIZATION REGISTERS

The recommended programming sequence when initializing the device is as follows:

1. Register 0x000 = 0x99
2. Register 0x000 = 0x18
3. Register 0x103 = 0x00
4. Register 0x22B = 0x0B
5. Register 0x22F = 0x27
6. Register 0x308 = 0x02
7. Register 0x309 = 0x33
8. Register 0x30A = 0x48
9. Register 0x30D = 0x09
10. Register 0x30E = 0x09
11. Register 0x300 = 0x1F

*Table 5. Signal Stage Status Truth Table Using RX_MUTE and Mute-Mask Control*

| RX_MUTE Pin \|\| MUTE_IF_UNLOCKED Bit[1] | Mute-Mask Control Register 0x101[1] | RXON Pin[1] | On-Mask Control Register 0x102[1] | Bias Control Register 0x100[1] | Result (1 is On, 0 is Off)[1] |
|---|---|---|---|---|---|
| 1 | 1 | 0 or 1 | 0 or 1 | 0 or 1 | 0 |
| 1 | 0 | Controlled by RXON pin | | | |
| 0 | 1 | Controlled by RXON pin | | | |

[1] The 0 and 1 settings apply to all user specified bits in the listed register.

## THEORY OF OPERATION

*Table 6. Signal Stage Status Truth Table Using RX_ON and On-Mask Control*

| RX_MUTE Pin \|\| MUTE_IF_UNLOCKED Bit[1] | Mute-Mask Control Register 0x101[1] | RXON Pin[1] | On-Mask Control Register 0x102[1] | Bias Control Register 0x100[1] | Result (1 is On, 0 is Off)[1] |
|---|---|---|---|---|---|
| 0 or 1 | 0 | 0 or 1 | 0 | 0 | 0 |
| 0 or 1 | 0 | 0 or 1 | 0 | 1 | 1 |
| 0 or 1 | 0 | 0 | 1 | 0 or 1 | 0 |
| 0 or 1 | 0 | 1 | 1 | 0 | 0 |
| 0 or 1 | 0 | 1 | 1 | 1 | 1 |
| 0 | 0 or 1 | 0 or 1 | 0 | 0 | 0 |
| 0 | 0 or 1 | 0 or 1 | 0 | 1 | 1 |
| 0 | 0 or 1 | 0 | 1 | 0 or 1 | 0 |
| 0 | 0 or 1 | 1 | 1 | 0 | 0 |
| 0 | 0 or 1 | 1 | 1 | 1 | 1 |

[1] The 0 and 1 settings apply to all user specified bits in the listed register.

## REGISTER SUMMARY

*Table 7. Register Summary*

| Reg | Name | Bits | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Reset | RW |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x000 | SPI_ CONFIG_1 | [7:0] | SOFT-RESET_ | LSB_ FIRST_ | ENDIAN_ | SDO_ ACTIVE_ | SDO_ ACTIVE_ | ENDIAN | LSB_FIRST | SOFT-RESET | 0x00 | R/W |
| 0x004 | PRODUCT_ ID_L | [7:0] | PRODUCT_ID_L | | | | | | | | 0x40 | R |
| 0x005 | PRODUCT_ ID_H | [7:0] | PRODUCT_ID_H | | | | | | | | 0x46 | R |
| 0x100 | SIGCHAIN_ ENABLE | [7:0] | RF_ CONTROLL ER_ BIAS_ CONTROL | SYNTH_ BIAS_ CONTROL | RESERVED | ATT6DB_ BIAS_ CONTROL | LNASTG2_ BIAS_ CONTROL | LNASTG1_ BIAS_ CONTROL | AMPLO_ BIAS_ CONTROL | AMPIF_ BIAS_ CONTROL | 0xDF | R/W |
| 0x101 | MUTE_ MASK_ CONTROL | [7:0] | BIASRF_ MUTE_ MASK_ CONTROL | SYNTH_ MUTE_ MASK_ CONTROL | RESERVED | ATT6DB_ MUTE_ MASK_ CONTROL | LNASTG2_ MUTE_ MASK_ CONTROL | LNASTG1_ MUTE_ MASK_ CONTROL | AMPLO_ MUTE_ MASK_ CONTROL | AMPIF_ MUTE_ MASK_ CONTROL | 0xBF | R/W |
| 0x102 | ON_MASK_ CONTROL | [7:0] | RF_ CONTROLL ER_ ON_MASK_ CONTROL | SYNTH_ ON_MASK_ CONTROL | RESERVED | ATT6DB_ ON_MASK_ CONTROL | LNASTG2_ ON_MASK_ CONTROL | LNASTG1_ ON_MASK_ CONTROL | AMPLO_ ON_MASK_ CONTROL | RESERVED | 0xFF | R/W |
| 0x103 | MUTE_ UNLOCK | [7:0] | RESERVED | | | | | | | MUTE_IF_ UNLOCKED | 0x01 | R/W |
| 0x200 | INT_L | [7:0] | INT[7:0] | | | | | | | | 0x90 | R/W |
| 0x201 | INT_H | [7:0] | INT[15:8] | | | | | | | | 0x01 | R/W |
| 0x20B | SYNTH | [7:0] | RESERVED | | | | | | PRE_SEL | EN_FBDIV | 0x01 | R/W |
| 0x20C | R_DIV | [7:0] | RESERVED | | | R_DIV | | | | | 0x01 | R/W |
| 0x20E | REFERENCE | [7:0] | RESERVED | | | | DOUBLER_ EN | RESERVED | | RDIV2_SEL | 0x04 | R/W |
| 0x214 | LOCK_ DETECT_ CONFIG | [7:0] | LD_BIAS | | LD_COUNT | | | RESERVED | | | 0x48 | R/W |
| 0x218 | SYNTH_ LOCK_ TIMEOUT | [7:0] | RESERVED | | | SYNTH_LOCK_TIMEOUT | | | | | 0x1F | R/W |
| 0x21C | VCO_ TIMEOUT_L | [7:0] | VCO_TIMEOUT[7:0] | | | | | | | | 0x19 | R/W |
| 0x21D | VCO_ TIMEOUT_H | [7:0] | RESERVED | | | | | | VCO_TIMEOUT[9:8] | | 0x00 | R/W |
| 0x21E | VCO_BAND_ DIV | [7:0] | VCO_BAND_DIV | | | | | | | | 0x10 | R/W |
| 0x22B | MULTI_ FUNC_ SYNTH_ CTRL_022B | [7:0] | RESERVED | | | | | | RF_PBS | | 0x09 | R/W |
| 0x22E | CP_CURR | [7:0] | RESERVED | | | | CP_CURRENT | | | | 0x0E | R/W |
| 0x22F | BICP | [7:0] | BICP | | | | | | | | 0x08 | R/W |
| 0x24D | LOCK_ DETECT | [7:0] | RESERVED | | | | | | | LOCK_ DETECT | 0x00 | R |
| 0x24E | MUXOUT | [7:0] | MUX_SEL | | | | | | | | 0x00 | R/W |
| 0x300 | DSA_ CONTROL | [7:0] | RESERVED | | | SEL_DSA_ATTEN | | | | | 0x00 | R/W |

## REGISTER SUMMARY

*Table 7. Register Summary (Continued)*

| Reg | Name | Bits | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Reset | RW |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x301 | AGPIO_ CONTROL | [7:0] | RESERVED | | | | SEL_AGPIO | SEL_ADC_INPUT | | | 0x00 | R/W |
| 0x302 | ADC_ CONTROL | [7:0] | SEL_ADC_CLKDIV | | | | SEL_ ADCLOG-SCALE | SEL_ADC-HALF | ADC_START | EN_ADC | 0xCA | R/W |
| 0x303 | ADC_ STATUS | [7:0] | RESERVED | | | | | ADC_LATCH-DATA | ADC_BUSY | ADC_EOC | 0x01 | R |
| 0x304 | ADC_DATA | [7:0] | ADC_DATA | | | | | | | | 0xE1 | R |
| 0x305 | GPIO_ WRITEVALS | [7:0] | RESERVED | | | | GPIO_WRITEVALS | | | RESERVED | 0x00 | R/W |
| 0x306 | GPIO_ READVALS | [7:0] | RESERVED | | | | GPIO_READVALS | | | RESERVED | 0x0E | R |
| 0x307 | GPIO_ CONTROL | [7:0] | RESERVED | EN_GPIO_OUT | | | SEL_GPIO_LEVELS | | | RESERVED | 0x00 | R/W |
| 0x308 | RFBIAS_ CONTROL1 | [7:0] | RESERVED | | | | SEL_BIAS_AMPIF | | | | 0x08 | R/W |
| 0x309 | RFBIAS_ CONTROL2 | [7:0] | SEL_BIAS_LNASTG2 | | | | SEL_BIAS_LNASTG1 | | | | 0x88 | R/W |
| 0x30A | RFBIAS_ CONTROL3 | [7:0] | SEL_BIAS_AMPLO2 | | | | SEL_BIAS_AMPLO1 | | | | 0x88 | R/W |
| 0x30D | MIXER_ CONTROL1 | [7:0] | RESERVED | | | SEL_MIXLOCM_COARSE_P | | | | | 0x08 | R/W |
| 0x30E | MIXER_ CONTROL2 | [7:0] | RESERVED | | | SEL_MIXLOCM_COARSE_N | | | | | 0x08 | R/W |

## REGISTER DETAILS

### SPI CONFIGURATION REGISTER

**Address: 0x000, Reset: 0x00, Name: SPI_CONFIG_1**

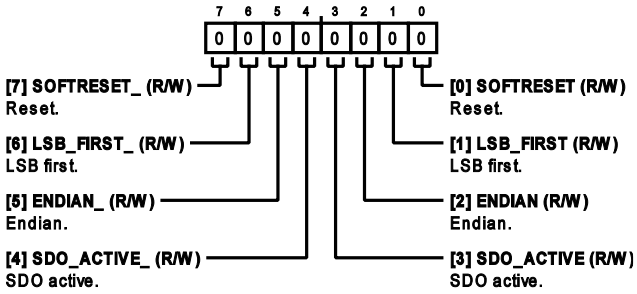
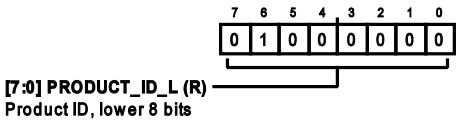



*Table 8. Bit Descriptions for SPI_CONFIG_1*

| Bits | Bit Name | Description | Reset | Access |
|---|---|---|---|---|
| 7 | SOFTRESET_ | Reset.<br>0: reset not asserted.<br>1: reset asserted. | 0x0 | R/W |
| 6 | LSB_FIRST_ | LSB first.<br>0: LSB first.<br>1: MSB first. | 0x0 | R/W |
| 5 | ENDIAN_ | Endian.<br>1: big endian.<br>0: little endian. | 0x0 | R/W |
| 4 | SDO_ACTIVE_ | SDO active.<br>0: SDO inactive.<br>1: SDO active. | 0x0 | R/W |
| 3 | SDO_ACTIVE | SDO active.<br>0: SDO inactive.<br>1: SDO active. | 0x0 | R/W |
| 2 | ENDIAN | Endian.<br>0: little endian.<br>1: big endian. | 0x0 | R/W |
| 1 | LSB_FIRST | LSB first.<br>0: LSB first.<br>1: MSB first. | 0x0 | R/W |
| 0 | SOFTRESET | Reset.<br>0: reset not asserted.<br>1: reset asserted. | 0x0 | R/W |

### Product ID Register Product ID (Lower Eight Bits of 16-Bit Register)

**Address: 0x004, Reset: 0x40, Name: PRODUCT_ID_L**



## REGISTER DETAILS

*Table 9. Bit Descriptions for PRODUCT_ID_L*

| Bits | Bit Name | Description | Reset | Access |
|---|---|---|---|---|
| [7:0] | PRODUCT_ID_L | Product ID, lower eight bits. | 0x40 | R |

### Product ID Register (Upper Eight Bits of 16-Bit Register)

#### Address: 0x005, Reset: 0x46, Name: PRODUCT_ID_H

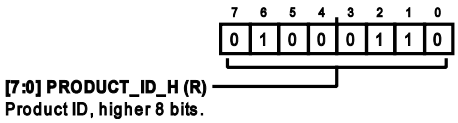



*Table 10. Bit Descriptions for PRODUCT_ID_H*

| Bits | Bit Name | Description | Reset | Access |
|---|---|---|---|---|
| [7:0] | PRODUCT_ID_H | Product ID, higher eight bits. | 0x46 | R |

### Bias Control Register

#### Address: 0x100, Reset: 0xDF, Name: SIGCHAIN_ENABLE

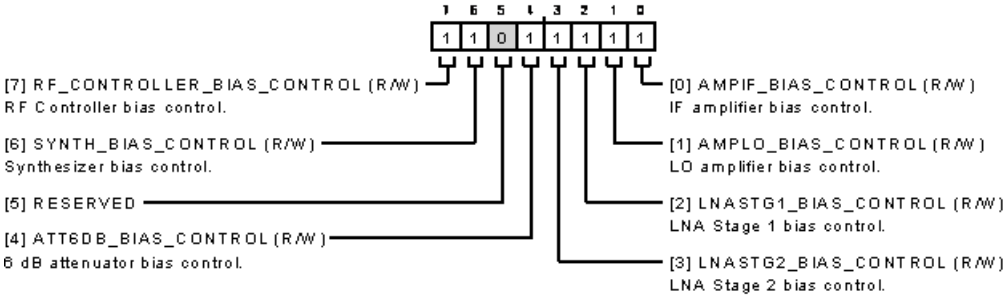



*Table 11. Bit Descriptions for SIGCHAIN_ENABLE*

| Bits | Bit Name | Description | Reset | Access |
|---|---|---|---|---|
| 7 | RF_CONTROLLER_BIAS_CONTROL | RF controller bias control.<br>0: disable.<br>1: enable. | 0x1 | R/W |
| 6 | SYNTH_BIAS_CONTROL | Synthesizer bias control.<br>1: enable.<br>0: disable. | 0x1 | R/W |
| 5 | RESERVED | Reserved. | 0x0 | R |
| 4 | ATT6DB_BIAS_CONTROL | 6 dB attenuator bias control.<br>1: enable.<br>0: disable. | 0x1 | R/W |
| 3 | LNASTG2_BIAS_CONTROL | LNA Stage 2 bias control.<br>1: enable.<br>0: disable. | 0x1 | R/W |
| 2 | LNASTG1_BIAS_CONTROL | LNA Stage 1 bias control.<br>1: enable.<br>0: disable. | 0x1 | R/W |

## REGISTER DETAILS

*Table 11. Bit Descriptions for SIGCHAIN_ENABLE (Continued)*

| Bits | Bit Name | Description | Reset | Access |
|---|---|---|---|---|
| 1 | AMPLO_BIAS_CONTROL | LO amplifier bias control.<br>1: enable.<br>0: disable. | 0x1 | R/W |
| 0 | AMPIF_BIAS_CONTROL | IF amplifier bias control.<br>1: enable.<br>0: disable. | 0x1 | R/W |

### Mute Mask Control Register

**Address: 0x101, Reset: 0xBF, Name: MUTE_MASK_CONTROL**

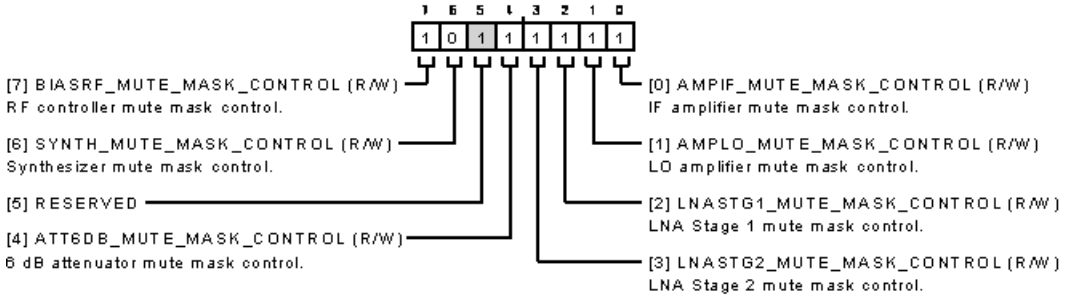



*Table 12. Bit Descriptions for MUTE_MASK_CONTROL*

| Bits | Bit Name | Description | Reset | Access |
|---|---|---|---|---|
| 7 | BIASRF_MUTE_MASK_CONTROL | RF controller mute mask control.<br>0: disable mute mask.<br>1: enable mute mask. | 0x1 | R/W |
| 6 | SYNTH_MUTE_MASK_CONTROL | Synthesizer mute mask control.<br>0: disable mute mask.<br>1: enable mute mask. | 0x0 | R/W |
| 5 | RESERVED | Reserved. | 0x1 | R/W |
| 4 | ATT6DB_MUTE_MASK_CONTROL | 6 dB attenuator mute mask control.<br>0: disable mute mask.<br>1: enable mute mask. | 0x1 | R/W |
| 3 | LNASTG2_MUTE_MASK_CONTROL | LNA Stage 2 mute mask control.<br>0: disable mute mask.<br>1: enable mute mask. | 0x1 | R/W |
| 2 | LNASTG1_MUTE_MASK_CONTROL | LNA Stage 1 mute mask control.<br>0: disable mute mask.<br>1: enable mute mask. | 0x1 | R/W |
| 1 | AMPLO_MUTE_MASK_CONTROL | LO amplifier mute mask control.<br>0: disable mute mask.<br>1: enable mute mask. | 0x1 | R/W |
| 0 | AMPIF_MUTE_MASK_CONTROL | IF amplifier mute mask control.<br>0: disable mute mask.<br>1: enable mute mask. | 0x1 | R/W |

## REGISTER DETAILS

### On Mask Control Register

#### Address: 0x102, Reset: 0xFF, Name: ON_MASK_CONTROL

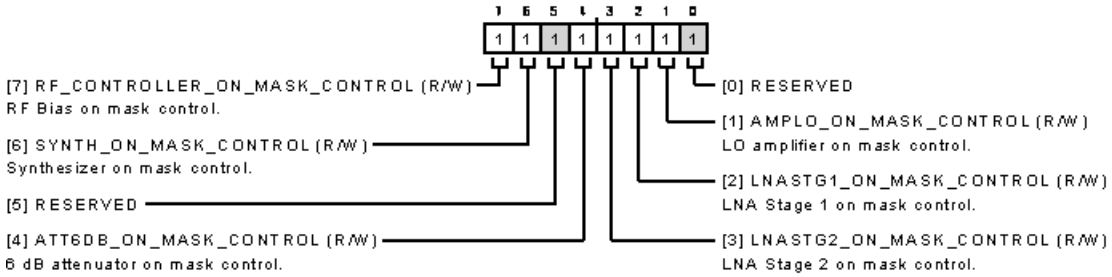



*Table 13. Bit Descriptions for ON_MASK_CONTROL*

| Bits | Bit Name | Description | Reset | Access |
|---|---|---|---|---|
| 7 | RF_CONTROLLER_ON_MASK_CONTROL | RF bias on mask control.<br>0: disable on mask.<br>1: enable on mask. | 0x1 | R/W |
| 6 | SYNTH_ON_MASK_CONTROL | Synthesizer on mask control.<br>0: disable on mask.<br>1: enable on mask. | 0x1 | R/W |
| 5 | RESERVED | Reserved. | 0x1 | R/W |
| 4 | ATT6DB_ON_MASK_CONTROL | 6 dB attenuator on mask control.<br>0: disable on mask.<br>1: enable on mask. | 0x1 | R/W |
| 3 | LNASTG2_ON_MASK_CONTROL | LNA Stage 2 on mask control.<br>0: disable on mask.<br>1: enable on mask. | 0x1 | R/W |
| 2 | LNASTG1_ON_MASK_CONTROL | LNA Stage 1 on mask control.<br>0: disable on mask.<br>1: enable on mask. | 0x1 | R/W |
| 1 | AMPLO_ON_MASK_CONTROL | LO amplifier on mask control.<br>0: disable on mask.<br>1: enable on mask. | 0x1 | R/W |
| 0 | RESERVED | Reserved. | 0x1 | R/W |

### Mute IF Unlock Register

#### Address: 0x103, Reset: 0x01, Name: MUTE_UNLOCK

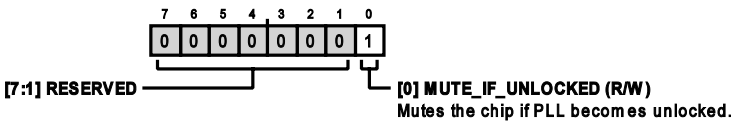



*Table 14. Bit Descriptions for MUTE_UNLOCK*

| Bits | Bit Name | Description | Reset | Access |
|---|---|---|---|---|
| [7:1] | RESERVED | Reserved. | 0x0 | R |
| 0 | MUTE_IF_UNLOCKED | Mutes the chip if PLL becomes unlocked. | 0x1 | R/W |

## REGISTER DETAILS

*Table 14. Bit Descriptions for MUTE_UNLOCK (Continued)*

| Bits | Bit Name | Description | Reset | Access |
|---|---|---|---|---|
| | | 1: enable.<br>0: disable. | | |

### Integer Register (Lower Eight Bits)

#### Address: 0x200, Reset: 0x90, Name: INT_L

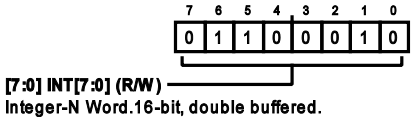



*Table 15. Bit Descriptions for INT_L*

| Bits | Bit Name | Description | Reset | Access |
|---|---|---|---|---|
| [7:0] | INT[7:0] | Integer-N Word, 16-bit, double buffered. | 0x90 | R/W |

### Integer Register (Upper Eight Bits)

#### Address: 0x201, Reset: 0x01, Name: INT_H

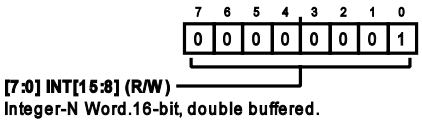



*Table 16. Bit Descriptions for INT_H*

| Bits | Bit Name | Description | Reset | Access |
|---|---|---|---|---|
| [7:0] | INT[15:8] | Integer-N Word, 16-bit, double buffered. | 0x1 | R/W |

### Synthesizer Configuration Register

#### Address: 0x20B, Reset: 0x01, Name: SYNTH

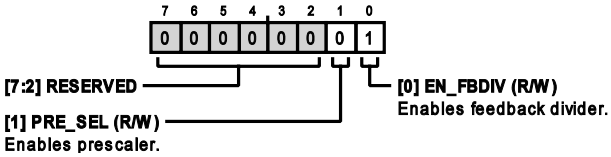



*Table 17. Bit Descriptions for SYNTH*

| Bits | Bit Name | Description | Reset | Access |
|---|---|---|---|---|
| [7:2] | RESERVED | Reserved. | 0x0 | R |
| 1 | PRE_SEL | Enables prescaler.<br>0: disable.<br>1: enable. | 0x0 | R/W |
| 0 | EN_FBDIV | Enables feedback divider.<br>0: disable.<br>1: enable. | 0x1 | R/W |

## REGISTER DETAILS

### Reference Input Divider Register

#### Address: 0x20C, Reset: 0x01, Name: R_DIV

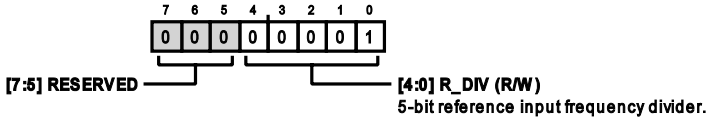



*Table 18. Bit Descriptions for R_DIV*

| Bits | Bit Name | Description | Reset | Access |
|---|---|---|---|---|
| [7:5] | RESERVED | Reserved. | 0x0 | R |
| [4:0] | R_DIV | 5-bit reference input frequency divider. | 0x1 | R/W |

### Reference Input Configuration Register

#### Address: 0x20E, Reset: 0x04, Name: REFERENCE

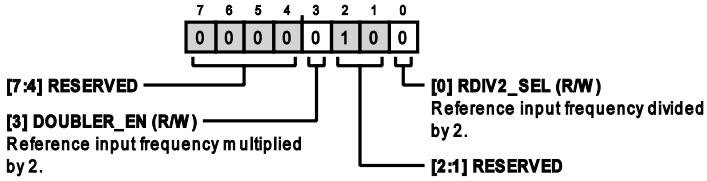



*Table 19. Bit Descriptions for REFERENCE*

| Bits | Bit Name | Description | Reset | Access |
|---|---|---|---|---|
| [7:4] | RESERVED | Reserved. | 0x0 | R |
| 3 | DOUBLER_EN | Reference input frequency multiplied by 2.<br>0: disable.<br>1: enable. | 0x0 | R/W |
| [2:1] | RESERVED | Reserved. | 0x2 | R/W |
| 0 | RDIV2_SEL | Reference input frequency divided by 2.<br>0: disable.<br>1: enable. | 0x0 | R/W |

### Lock Detect Configuration Register

#### Address: 0x214, Reset: 0x48, Name: LOCK_DETECT_CONFIG

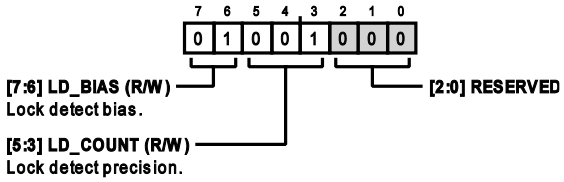



*Table 20. Bit Descriptions for LOCK_DETECT_CONFIG*

| Bits | Bit Name | Description | Reset | Access |
|---|---|---|---|---|
| [7:6] | LD_BIAS | Lock detect bias.<br>00: 40 µA.<br>01: 30 µA. | 0x1 | R/W |

## REGISTER DETAILS

*Table 20. Bit Descriptions for LOCK_DETECT_CONFIG (Continued)*

| Bits | Bit Name | Description | Reset | Access |
|---|---|---|---|---|
| | | 10: 20 µA.<br>11: 10 µA. | | |
| [5:3] | LD_COUNT | Lock detect precision.<br>000: check 1024 consecutive PFD cycles for lock.<br>001: check 2048 consecutive PFD cycles for lock.<br>010: check 4096 consecutive PFD cycles for lock.<br>011: check 8192 consecutive PFD cycles for lock. | 0x1 | R/W |
| [2:0] | RESERVED | Reserved. | 0x0 | R/W |

### Synthesizer Lock Timeout Register

**Address: 0x218, Reset: 0x1F, Name: SYNTH_LOCK_TIMEOUT**

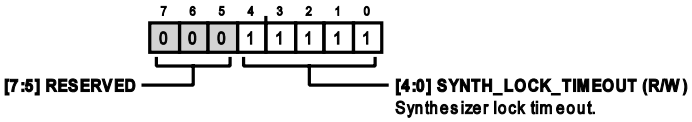



*Table 21. Bit Descriptions for SYNTH_LOCK_TIMEOUT*

| Bits | Bit Name | Description | Reset | Access |
|---|---|---|---|---|
| [7:5] | RESERVED | Reserved. | 0x0 | R |
| [4:0] | SYNTH_LOCK_TIMEOUT | Synthesizer lock timeout. | 0x1F | R/W |

### VCO Timeout Register (Lower Eight Bits)

**Address: 0x21C, Reset: 0x19, Name: VCO_TIMEOUT_L**

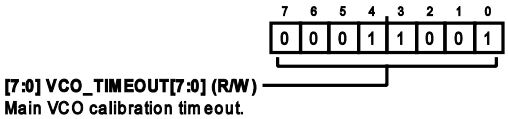



*Table 22. Bit Descriptions for VCO_TIMEOUT_L*

| Bits | Bit Name | Description | Reset | Access |
|---|---|---|---|---|
| [7:0] | VCO_TIMEOUT[7:0] | Main VCO calibration timeout. | 0x19 | R/W |

### VCO Timeout Register (Upper Eight Bits)

**Address: 0x21D, Reset: 0x00, Name: VCO_TIMEOUT_H**

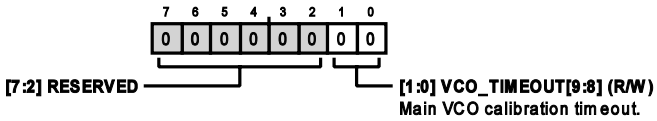



*Table 23. Bit Descriptions for VCO_TIMEOUT_H*

| Bits | Bit Name | Description | Reset | Access |
|---|---|---|---|---|
| [7:2] | RESERVED | Reserved. | 0x0 | R |
| [1:0] | VCO_TIMEOUT[9:8] | Main VCO calibration timeout. | 0x0 | R/W |

## REGISTER DETAILS

### VCO Band Divider Register

**Address: 0x21E, Reset: 0x10, Name: VCO_BAND_DIV**

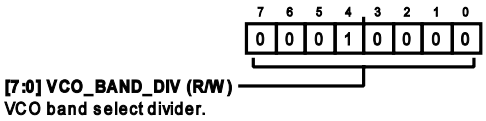



*Table 24. Bit Descriptions for VCO_BAND_DIV*

| Bits | Bit Name | Description | Reset | Access |
|---|---|---|---|---|
| [7:0] | VCO_BAND_DIV | VCO band select divider. | 0x10 | R/W |

### Multifunction Synthesizer Configuration Register

**Address: 0x22B, Reset: 0x09, Name: MULTI_FUNC_SYNTH_CTRL_022B**

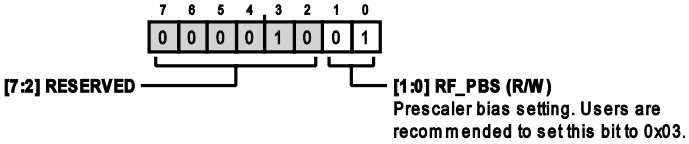



*Table 25. Bit Descriptions for MULTI_FUNC_SYNTH_CTRL_022B*

| Bits | Bit Name | Description | Reset | Access |
|---|---|---|---|---|
| [7:2] | RESERVED | Reserved. | 0x2 | R |
| [1:0] | RF_PBS | Prescaler bias setting. Users are recommended to set this bit to 0x03. | 0x1 | R/W |

### Charge Pump Current Register

**Address: 0x22E, Reset: 0x0E, Name: CP_CURR**

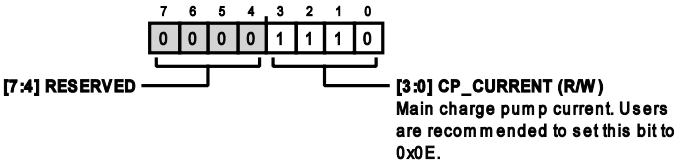



*Table 26. Bit Descriptions for CP_CURR*

| Bits | Bit Name | Description | Reset | Access |
|---|---|---|---|---|
| [7:4] | RESERVED | Reserved. | 0x0 | R |
| [3:0] | CP_CURRENT | Main charge pump current. Users are recommended to set this bit to 0x0E. | 0xE | R/W |

### Bleed Current Register

**Address: 0x22F, Reset: 0x08, Name: BICP**

## REGISTER DETAILS

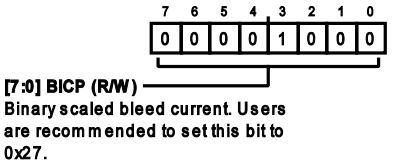



*Table 27. Bit Descriptions for BICP*

| Bits | Bit Name | Description | Reset | Access |
|---|---|---|---|---|
| [7:0] | BICP | Binary scaled bleed current. Users are recommended to set this bit to 0x27. | 0x8 | R/W |

### Lock Detect Register

**Address: 0x24D, Reset: 0x00, Name: LOCK_DETECT**

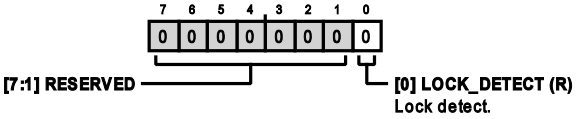



*Table 28. Bit Descriptions for LOCK_DETECT*

| Bits | Bit Name | Description | Reset | Access |
|---|---|---|---|---|
| [7:1] | RESERVED | Reserved. | 0x0 | R |
| 0 | LOCK_DETECT | Lock detect.<br>1: PLL locks.<br>0: PLL does not lock. | 0x0 | R |

### MUXOUT Select Register

**Address: 0x24E, Reset: 0x00, Name: MUXOUT**

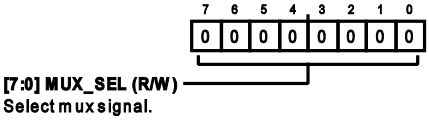



*Table 29. Bit Descriptions for MUXOUT*

| Bits | Bit Name | Description | Reset | Access |
|---|---|---|---|---|
| [7:0] | MUX_SEL | Select mux signal.<br>0001: digital lock detect.<br>0000: output low.<br>0100: R counter/2.<br>0101: N counter/2.<br>1110: output high. | 0x0 | R/W |

### DSA Control Register

**Address: 0x300, Reset: 0x00, Name: DSA_CONTROL**

## REGISTER DETAILS

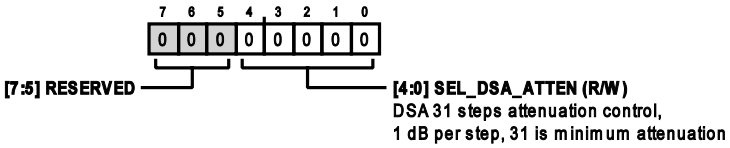



*Table 30. Bit Descriptions for DSA_CONTROL*

| Bits | Bit Name | Description | Reset | Access |
|---|---|---|---|---|
| [7:5] | RESERVED | Reserved. | 0x0 | R |
| [4:0] | SEL_DSA_ATTEN | DSA 31 steps attenuation control, 1 dB per step, 31 dB is minimum attenuation | 0x0 | R/W |

### AGPIO Control Register

#### Address: 0x301, Reset: 0x00, Name: AGPIO_CONTROL

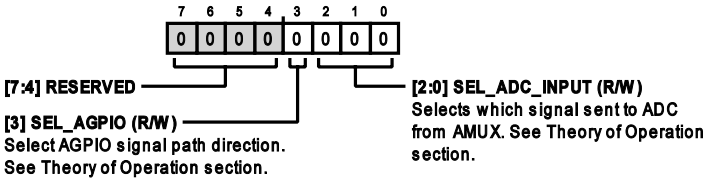



*Table 31. Bit Descriptions for AGPIO_CONTROL*

| Bits | Bit Name | Description | Reset | Access |
|---|---|---|---|---|
| [7:4] | RESERVED | Reserved. | 0x0 | R |
| 3 | SEL_AGPIO | Select AGPIO signal path direction. See the Theory of Operation section.<br>0: analog mux output to AGPIO. AGPIO is output.<br>1: AGPIO signal sent to analog mux. AGPIO is external signal input. | 0x0 | R/W |
| [2:0] | SEL_ADC_INPUT | Selects which signal sent to ADC from analog mux. See the Theory of Operation section.<br>110: temperature sensor.<br>111: AGPIO, must also set SEL_AGPIO to 1. | 0x0 | R/W |

### ADC Control Register

#### Address: 0x302, Reset: 0xCA, Name: ADC_CONTROL

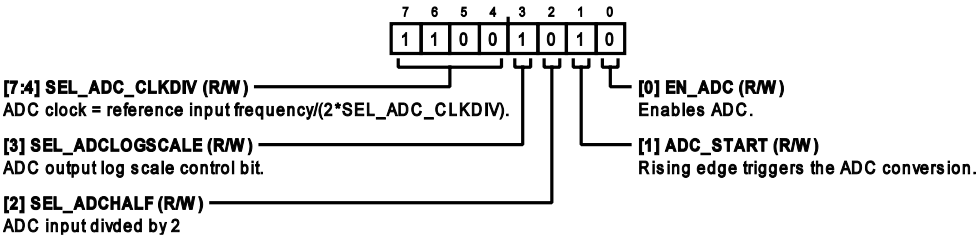



*Table 32. Bit Descriptions for ADC_CONTROL*

| Bits | Bit Name | Description | Reset | Access |
|---|---|---|---|---|
| [7:4] | SEL_ADC_CLKDIV | ADC clock = reference input frequency/(2 × SEL_ADC_CLKDIV). | 0xC | R/W |
| 3 | SEL_ADCLOGSCALE | ADC output log scale control bit.<br>1: enable.<br>0: disable. | 0x1 | R/W |

## REGISTER DETAILS

*Table 32. Bit Descriptions for ADC_CONTROL (Continued)*

| Bits | Bit Name | Description | Reset | Access |
|---|---|---|---|---|
| 2 | SEL_ADCHALF | ADC input divided by 2.<br>1: enable.<br>0: disable. | 0x0 | R/W |
| 1 | ADC_START | Rising edge triggers the ADC conversion. | 0x1 | R/W |
| 0 | EN_ADC | Enables ADC.<br>1: enable.<br>0: disable. | 0x0 | R/W |

### ADC Status Register

**Address: 0x303, Reset: 0x01, Name: ADC_STATUS**

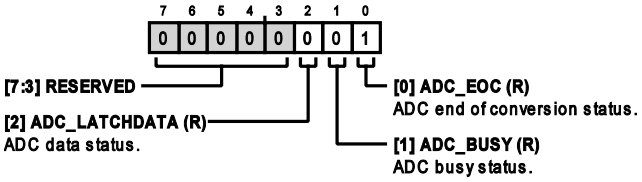



*Table 33. Bit Descriptions for ADC_STATUS*

| Bits | Bit Name | Description | Reset | Access |
|---|---|---|---|---|
| [7:3] | RESERVED | Reserved. | 0x0 | R |
| 2 | ADC_LATCHDATA | ADC data status.<br>1: ready.<br>0: not ready. | 0x0 | R |
| 1 | ADC_BUSY | ADC busy status.<br>1: busy.<br>0: bot busy. | 0x0 | R |
| 0 | ADC_EOC | ADC end of conversion status.<br>1: complete.<br>0: not complete. | 0x1 | R |

### ADC Data Register

**Address: 0x304, Reset: 0xE1, Name: ADC_DATA**

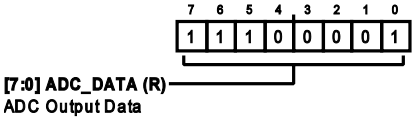



*Table 34. Bit Descriptions for ADC_DATA*

| Bits | Bit Name | Description | Reset | Access |
|---|---|---|---|---|
| [7:0] | ADC_DATA | ADC output data. | 0xE1 | R |

### GPIO Write Register

**Address: 0x305, Reset: 0x00, Name: GPIO_WRITEVALS**

## REGISTER DETAILS

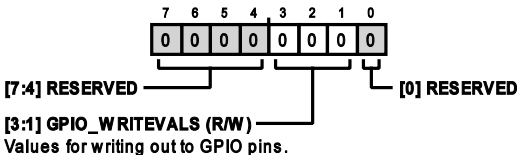



*Table 35. Bit Descriptions for GPIO_WRITEVALS*

| Bits | Bit Name | Description | Reset | Access |
|---|---|---|---|---|
| [7:4] | RESERVED | Reserved. | 0x0 | R |
| [3:1] | GPIO_WRITEVALS | Values for writing out to GPIO pins. | 0x0 | R/W |
| 0 | RESERVED | Reserved. | 0x0 | R |

### GPIO Read Register

#### Address: 0x306, Reset: 0x0E, Name: GPIO_READVALS

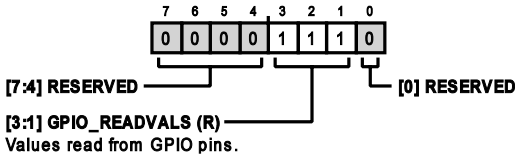



*Table 36. Bit Descriptions for GPIO_READVALS*

| Bits | Bit Name | Description | Reset | Access |
|---|---|---|---|---|
| [7:4] | RESERVED | Reserved. | 0x0 | R |
| [3:1] | GPIO_READVALS | Values read from GPIO pins. | 0x7 | R |
| 0 | RESERVED | Reserved. | 0x0 | R |

### GPIO Control Register

#### Address: 0x307, Reset: 0x00, Name: GPIO_CONTROL

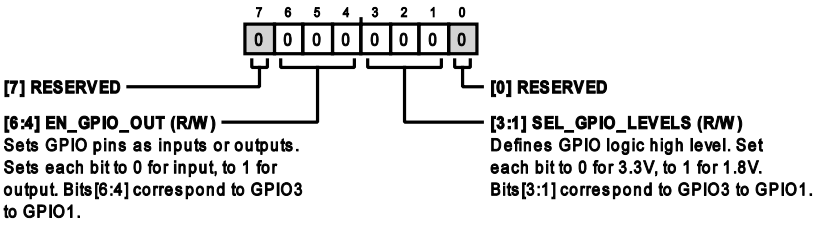



*Table 37. Bit Descriptions for GPIO_CONTROL*

| Bits | Bit Name | Description | Reset | Access |
|---|---|---|---|---|
| 7 | RESERVED | Reserved. | 0x0 | R |
| [6:4] | EN_GPIO_OUT | Sets GPIO pins as inputs or outputs. Sets each bit to 0 for input, or to 1 for output. Bits[6:4] correspond to GPIO3 to GPIO1. | 0x0 | R/W |
| [3:1] | SEL_GPIO_LEVELS | Defines GPIO logic high level. Set each bit to 0 for 3.3 V, or to 1 for 1.8 V. Bits[3:1] correspond to GPIO3 to GPIO1. | 0x0 | R/W |
| 0 | RESERVED | Reserved. | 0x0 | R |

## REGISTER DETAILS

### RF Bias Control 1 Register

**Address: 0x308, Reset: 0x08, Name: RFBIAS_CONTROL1**

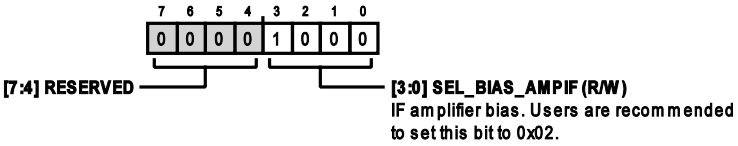



*Table 38. Bit Descriptions for RFBIAS_CONTROL1*

| Bits | Bit Name | Description | Reset | Access |
|---|---|---|---|---|
| [7:4] | RESERVED | Reserved. | 0x0 | R |
| [3:0] | SEL_BIAS_AMPIF | IF amplifier bias. Users are recommended to set this bit to 0x02. | 0x8 | R/W |

### RF Bias Control 2 Register

**Address: 0x309, Reset: 0x88, Name: RFBIAS_CONTROL2**

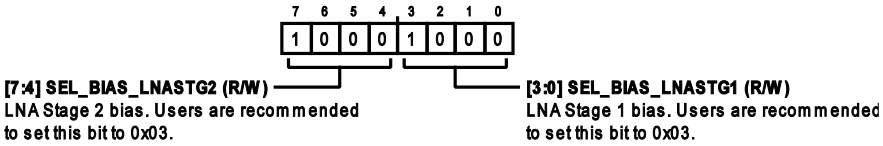



*Table 39. Bit Descriptions for RFBIAS_CONTROL2*

| Bits | Bit Name | Description | Reset | Access |
|---|---|---|---|---|
| [7:4] | SEL_BIAS_LNASTG2 | LNA Stage 2 bias. Users are recommended to set this bit to 0x03. | 0x8 | R/W |
| [3:0] | SEL_BIAS_LNASTG1 | LNA Stage 1 bias. Users are recommended to set this bit to 0x03. | 0x8 | R/W |

### RF Bias Control 3 Register

**Address: 0x30A, Reset: 0x88, Name: RFBIAS_CONTROL3**

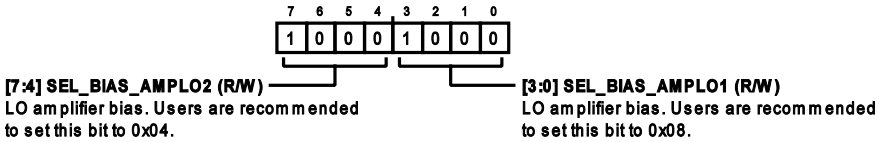
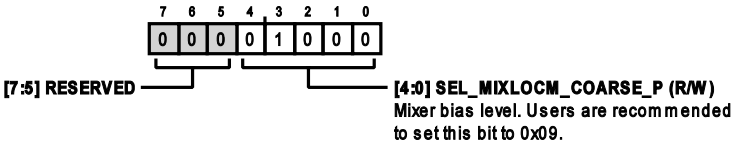



*Table 40. Bit Descriptions for RFBIAS_CONTROL3*

| Bits | Bit Name | Description | Reset | Access |
|---|---|---|---|---|
| [7:4] | SEL_BIAS_AMPLO2 | LO amplifier bias. Users are recommended to set this bit to 0x04. | 0x8 | R/W |
| [3:0] | SEL_BIAS_AMPLO1 | LO amplifier bias. Users are recommended to set this bit to 0x08. | 0x8 | R/W |

### Mixer Bias Control 1 Register

**Address: 0x30D, Reset: 0x08, Name: MIXER_CONTROL1**



## REGISTER DETAILS

*Table 41. Bit Descriptions for MIXER_CONTROL1*

| Bits | Bit Name | Description | Reset | Access |
|---|---|---|---|---|
| [7:5] | RESERVED | Reserved. | 0x0 | R |
| [4:0] | SEL_MIXLOCM_COARSE_P | Mixer bias level. Users are recommended to set this bit to 0x09. | 0x8 | R/W |

### Mixer Bias Control 2 Register

**Address: 0x30E, Reset: 0x08, Name: MIXER_CONTROL2**

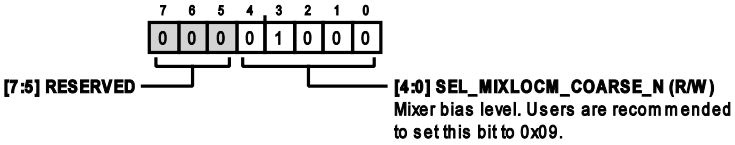



*Table 42. Bit Descriptions for MIXER_CONTROL2*

| Bits | Bit Name | Description | Reset | Access |
|---|---|---|---|---|
| [7:5] | RESERVED | Reserved. | 0x0 | R |
| [4:0] | SEL_MIXLOCM_COARSE_N | Mixer bias level. Users are recommended to set this bit to 0x09. | 0x8 | R/W |

## OUTLINE DIMENSIONS

| Package Drawing (Option) | Package Type | Package Description |
|---|---|---|
| CP-40-7 | LFCSP | 40-Lead, Lead Frame Chip Scale Package |

For the latest package outline information and land patterns (footprints), go to Package Index.

Updated: February 23, 2024

## ORDERING GUIDE

| Model[1] | Temperature Range | Package Description | Packing Quantity | Package Option |
|---|---|---|---|---|
| ADMV4640BCPZN | -40°C to +85°C | 40-Lead LFCSP (6mm x 6mm w/ EP) | Reel, 500 | CP-40-7 |
| ADMV4640BCPZN-RL7 | -40°C to +85°C | 40-Lead LFCSP (6mm x 6mm w/ EP) | Reel, 750 | CP-40-7 |

[1] Z = RoHS Compliant Part.

## EVALUATION BOARDS

| Model[1] | Description |
|---|---|
| EVAL-ADMV4640Z | Evaluation Assembly Board |

[1] Z = RoHS Compliant Part.

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