High Linearity, Silicon SP4T Switch, 1.8 GHz to 3.8 GHz

FEATURES

- Low insertion loss
  - 0.35 dB to 2.8 GHz typical
  - 0.42 dB to 3.8 GHz typical
- High input linearity, IP3: 84 dBm typical
- High power handling at T_{CASE} = 105°C
  - Long-term (>10 years) average
    - Continuous wave power: 39 dBm
    - LTE signal
      - Average power: 39 dBm
      - Peak power: 49 dBm
- Fast 0.1 dB settling time : 720 ns typical
- ESD ratings
  - HBM: 1000 V, Class 1B
  - CDM: 750 V, Class C4
- Positive control, LVCMOS-/LVTTL- compatible
- 4 mm x 4 mm, 20-terminal LGA package

APPLICATIONS

- 5G antenna tilting and beamforming
- Wireless infrastructure
- Military and high reliability applications
- Test equipment
- Pin diode replacement

FUNCTIONAL BLOCK DIAGRAM

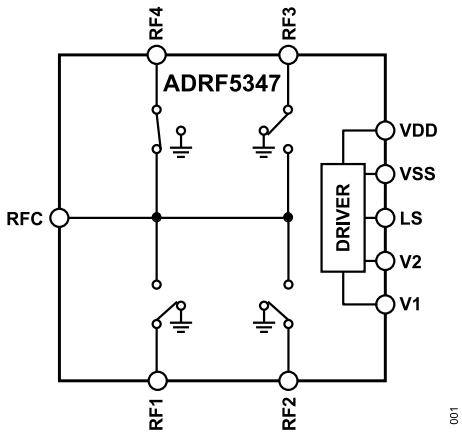

Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

The ADRF5347 is a high linearity, reflective, single-pole, four-throw (SP4T) switch manufactured in the silicon process.

The ADRF5347 operates from 1.8 GHz to 3.8 GHz with a typical insertion loss lower than 0.42 dB and a typical input IP3 of 84 dBm. The device has an RF input power handling capability of 39 dBm for continuous wave signals and 39 dBm average and 49 dBm peak for long-term evolution (LTE) signals.

The ADRF5347 draws a current of 2.5 mA on the positive supply of +5.0 V and 0.4 mA on the negative supply of −3.4 V. The device employs low voltage complementary metal-oxide semiconductor (LVCMOS)-/low voltage transistor-to-transistor logic (LVTTL)- compatible controls.

The ADRF5347 comes in a 4 mm × 4 mm, 20-terminal, RoHS-compliant, land grid array (LGA) package and operates between −40°C to +105°C.

Excellent return loss and IP3 enable ADRF5347 to be used in back-to-back configuration for phase shifting architectures. See the Back-to-Back Phase Shifter Reference Design section for more information.

DOCUMENT FEEDBACK
TECHNICAL SUPPORT

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SPECIFICATIONS

Supply voltages (V_{DD}) = 5 V, (V_{SS}) = −3.4 V, control voltage (V_{CTL}) = 0 V or 3.3 V, T_A = 25°C, and it is a 50 Ω system, unless otherwise noted.

Table 1. Specifications

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE		1.8		3.8	GHz
INSERTION LOSS					
Between RFC and RF1 to RF4 (On)	2.3 GHz to 2.8 GHz		0.35		dB
	3.3 GHz to 3.8 GHz		0.42		dB
ISOLATION					
Between RFC and RF1 to RF4 (Off)	2.3 GHz to 2.8 GHz		30		dB
	3.3 GHz to 3.8 GHz		27		dB
RETURN LOSS					
RFC and RF1 to RF4 (On)	2.3 GHz to 2.8 GHz		25		dB
	3.3 GHz to 3.8 GHz		25		dB
TRANSMISSION PHASE[1]					
RFC to RF1/RF4	at 3.8 GHz		-63		Degrees
RFC to RF2/RF3	at 3.8 GHz		-66		Degrees
RELATIVE PHASE VARIANCE	T_{CASE} = -40°C to 105°C			2	Degrees
SWITCHING					
Rise and Fall Time (t_{RISE}, t_{FALL})	90% to 10% of RF output (RF_{OUT})		300		ns
On and Off Time (t_{ON}, t_{OFF})	50% V_{CTL} to 10% to 90% of RF_{OUT}		650		ns
0.1 dB Settling Time	50% V_{CTL} to 0.1 dB of final RF_{OUT}[2]		720		ns
INPUT LINEARITY					
0.1 dB Power Compression (P0.1dB)	LTE (10 dB peak average ratio (PAR))		>50		dBm
Third-Order Intercept (IP3)					
Continuous Wave	Two-tone input power = 30 dBm continuous wave per tone		84		dBm
LTE Signal	Two LTE 10 MHz E-TM 1.1 carriers, each having 34 dBm		96		dBc
Harmonic Distortion					
Second Harmonic	Single LTE 10 MHz E-TM 1.1 carrier having 37dBm		100		dBc
Third Harmonic	Single LTE 10 MHz E-TM 1.1 carrier having 37dBm		87		dBc
SUPPLY CURRENT	V_{DD} and V_{SS}				
Positive Supply Current (I_{DD})			2.4		mA
Negative Supply Current (I_{SS})			0.4		mA
DIGITAL CONTROL INPUTS					
Voltage		0		0.7	V
Low Voltage (V_{IL})					
High Voltage (V_{IH})		1.07		3.45	V
Current					
Low (I_{INL})	LS		<1		µA
	V1 and V2		<1		µA
High (I_{INH})	LS		6.6		µA
	V1 and V2		6.6		µA
RECOMMENDED OPERATING CONDITIONS					
Positive Supply Voltage (V_{DD})		4.75	5.0	5.25	V
Negative Supply Voltage (V_{SS})		-3.6	-3.4	-3.2	V
Control Voltage (V_{CTL})		0		3.45	V
RF Input Power					
Through Power	T_{CASE} = 105°C, life time				
Continuous Wave				39	dBm
LTE Signal	10 dB PAR				

SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Average				39	dBm
Peak				49	dBm
Reflected Power	T_{CASE} = 105°C, life time				
Continuous Wave				27	dBm
LTE Signal	Input signal is 37 dBm LTE 10 MHz E-TM 1.1 carrier with 8 dB PAR				
Average				27	dBm
Peak				35	dBm
Hot Switching Power	T_{CASE} = 105°C, life time				
Continuous Wave				37	dBm
LTE Signal					
Average				37	dBm
Peak				47	dBm
Through Power	T_{CASE} = 105°C, single event (<10 sec)				
Continuous Wave				40	dBm
LTE Signal	10 dB PAR				
Average				40	dBm
Peak				50	dBm
Reflected Power	T_{CASE} = 105°C, single event (<10 sec)				
Continuous Wave				32	dBm
LTE Signal	Input signal is 37 dBm LTE 10 MHz E-TM 1.1 carrier with 8 dB PAR				
Average				32	dBm
Peak				40	dBm
Case Temperature (T_{CASE})		–40		+105	°C

[1] See Figure 7 and Figure 10 for frequency behavior.

[2] 50% V_{CTL} to gain settled to IL +/- 0.1 dB for an LTE signal of 37 dBm(avg.)/45 dBm(peak).

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
V_{DD}	–0.3 V to +5.5 V
V_{SS}	–3.8 V to +0.3 V
V_{CTL}	–0.3 V to +3.6 V
RFC, RF1, RF2, RF3, RF4	–2.0 V to +2.0 V
RF Input Power[1] (T_{CASE} = 105°C)	
Through Power	
Average	40.5 dBm
Peak	50.5 dBm
Reflected Power	
Average	32.5 dBm
Peak	40.5 dBm
Hot Switching Power	
Average	39.5 dBm
Peak	49.5 dBm
Temperature	
Junction to Maintain 0.6 Million Hours Mean Time to Failure [2] (MTTF)	135°C
Storage	–65°C to +150°C
Reflow	260°C

[1] For recommended operating conditions, see Table 1.

[2] For 55°C paddle temperature and incident RF power of 37 dBm(avg)/47 dBm(peak) LTE, FIT rate is 17.7. This FIT rate is not degraded under 7.88e9 hot switching at 10 years lifetime.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

Table 3. Thermal Resistance

Package Type	θ_{JC}[1]	Unit
CC-20-14	37	°C/W

[1] θ_{JC} is the junction to case bottom (channel to package bottom) thermal resistance. θ_{JC} *is determined by simulation under the following conditions: the heat transfer is due solely to the thermal conduction from the channel through the ground pad to the PCB, and the ground pad is held constant at the operating temperature of 105°C.*

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for the ADRF5347

Table 4. ADRF5347, 20-Terminal LGA

ESD Model	Withstand Threshold (V)	Class
HBM	1000	1B
CDM	750	C4

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

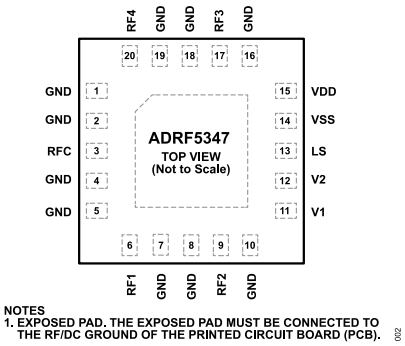

Figure 2. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 4, 5, 7 ,8, 10, 16, 18, 19	GND	Ground.
3	RFC	RF Common Port. The RFC Pin is AC Matched to 50 Ω.
6	RF1	RF Throw Port 1. The RF1 Pin is AC Matched to 50 Ω.
9	RF2	RF Throw Port 2. The RF2 Pin is AC Matched to 50 Ω.
11	V1	Control Input 1. See Table 6.
12	V2	Control Input 2. See Table 6.
13	LS	Logic Select. See Table 6.
14	VSS	Negative Supply Voltage.
15	VDD	Positive Supply Voltage.
17	RF3	RF Throw Port 3. The RF3 Pin is AC Matched to 50 Ω.
20	RF4	RF Throw Port 4. The RF4 Pin is AC Matched to 50 Ω.
	EPAD	Exposed Pad. The Exposed Pad Must be Connected to the RF and DC Ground of the PCB.

INTERFACE SCHEMATICS

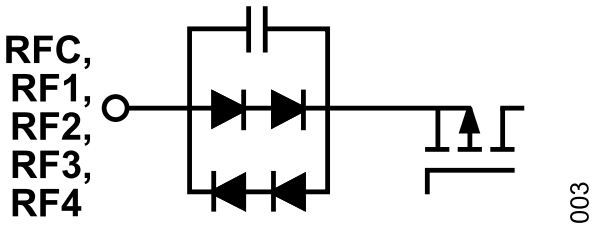

Figure 3. RF Interface Schematic

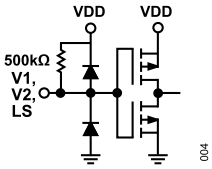

Figure 4. V1, V2, and LS Control Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

INSERTION LOSS, RETURN LOSS, AND ISOLATION

V_{DD} = 5 V, V_{SS} = −3.4 V, V_{CTRL} = 0 V or 3.3 V, and T_{CASE} = 25°C on a 50 Ω system, unless otherwise noted.

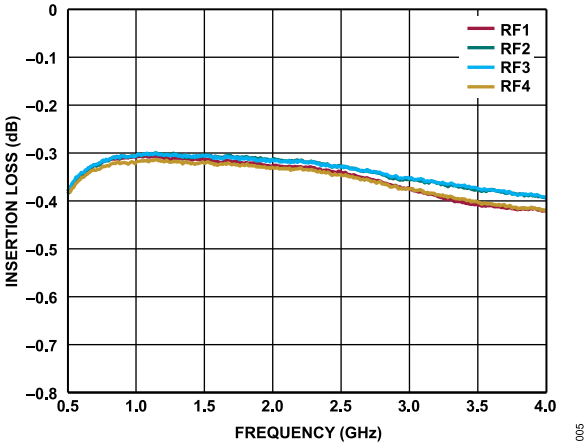

Figure 5. Insertion Loss for RFC to RFx Selected vs. Frequency

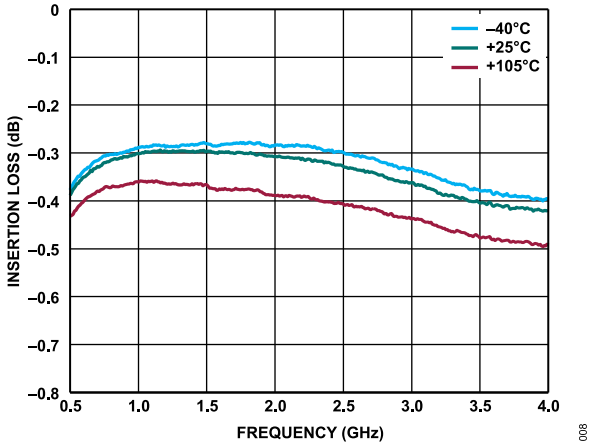

Figure 8. Insertion Loss for RFC to RF1 vs. Frequency over Temperature

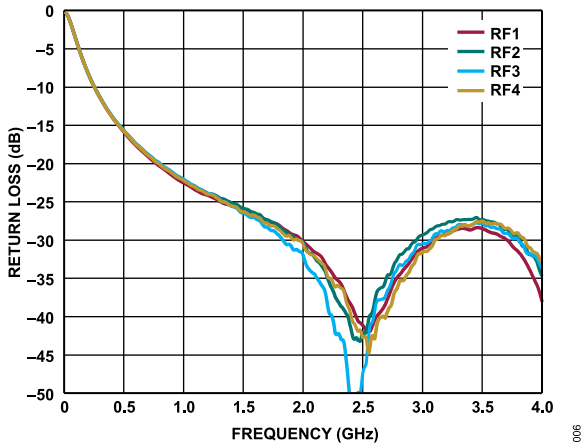

Figure 6. Return Loss for RFC when RFx Selected vs. Frequency

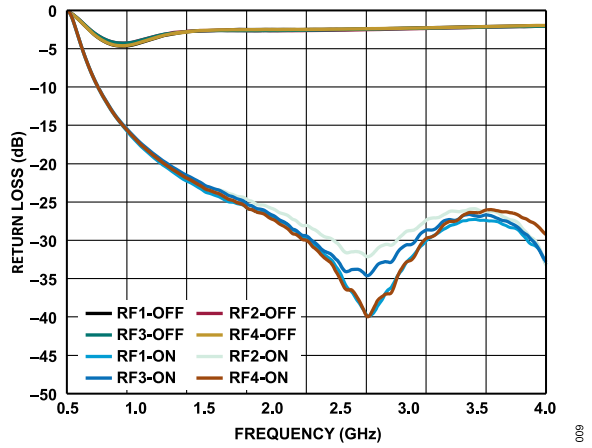

Figure 9. Return Loss for RFx Unselected and Selected

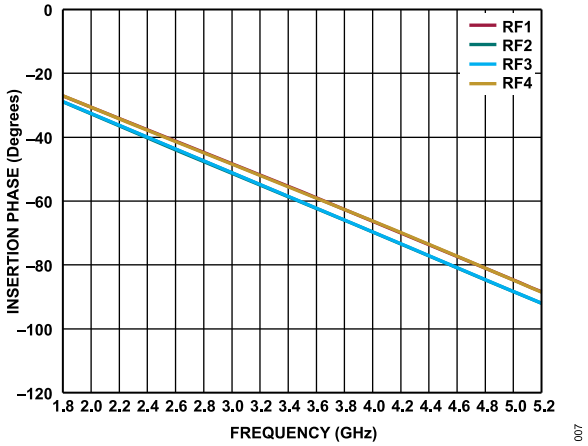

Figure 7. Insertion Phase RFC - RFx Selected vs. Frequency

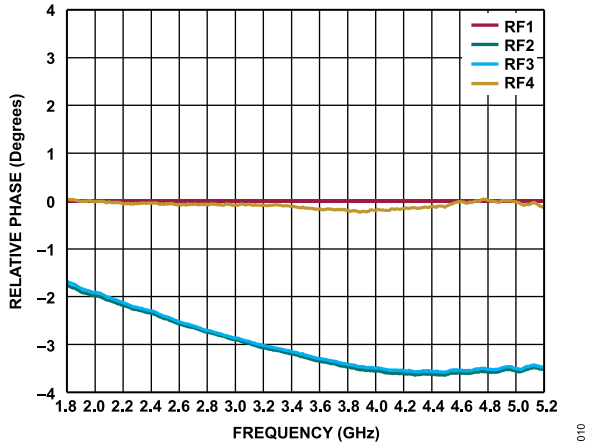

Figure 10. Relative Phase RFC - RFx Normalized to RFC - RF1

TYPICAL PERFORMANCE CHARACTERISTICS

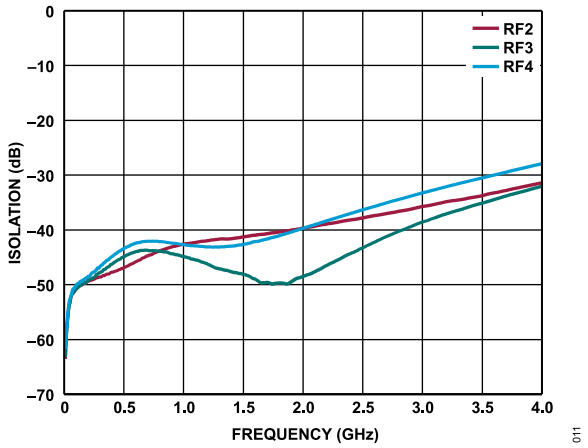

Figure 11. RFC to RF2, RF3, and RF4 Isolation vs. Frequency, RF1 Selected

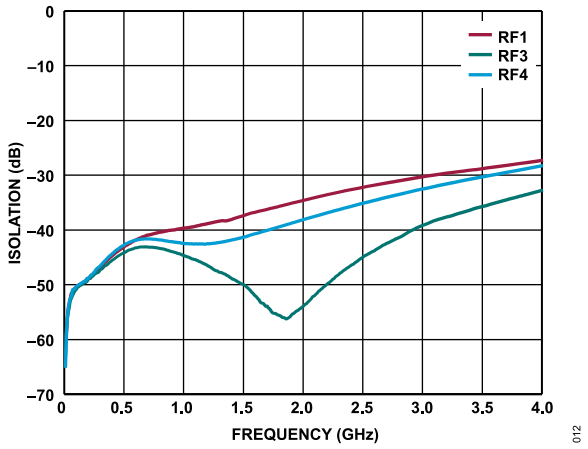

Figure 12. RFC to RF1, RF3, and RF4 Isolation vs. Frequency, RF2 Selected

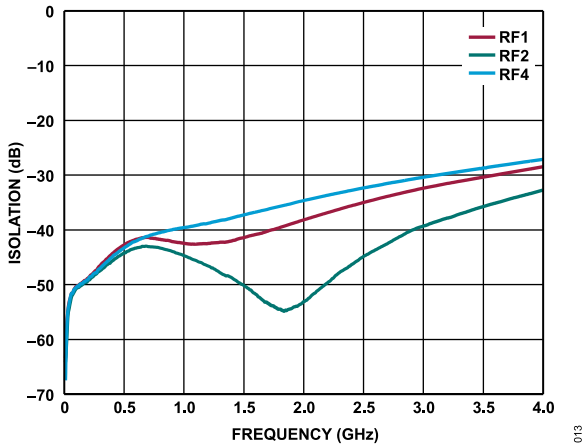

Figure 13. RFC to RF1, RF2, and RF4 Isolation vs. Frequency, RF3 Selected

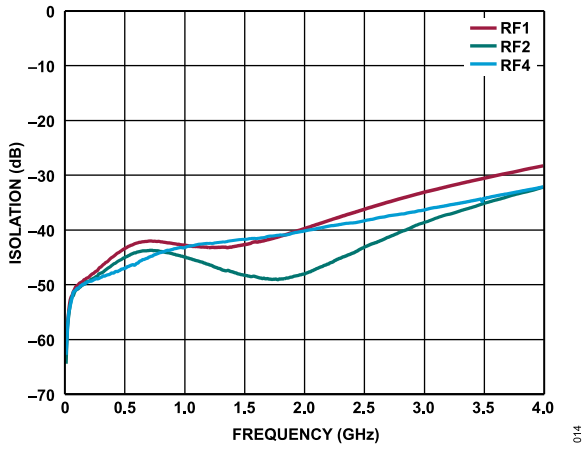

Figure 14. RFC to RF1, RF2, RF3 Isolation vs. Frequency, RF4 Selected

TYPICAL PERFORMANCE CHARACTERISTICS

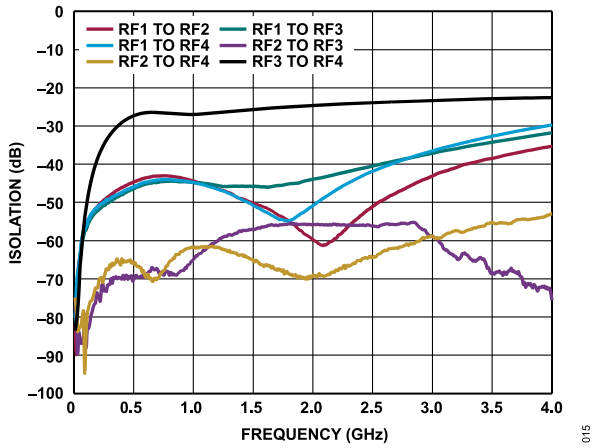

Figure 15. Channel-to-Channel Isolation vs. Frequency, RFC to RF1 Path Selected

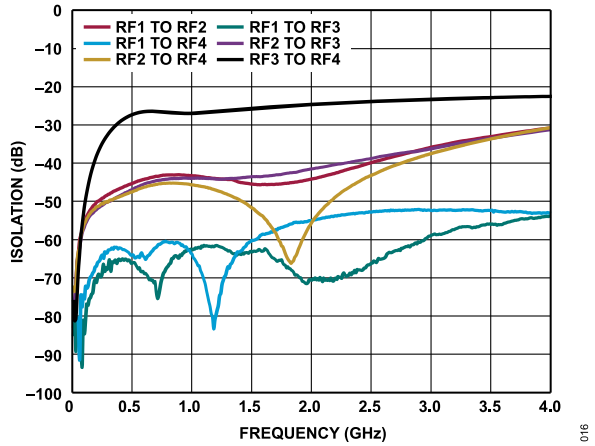

Figure 16. Channel-to-Channel Isolation vs. Frequency, RFC to RF2 Path Selected

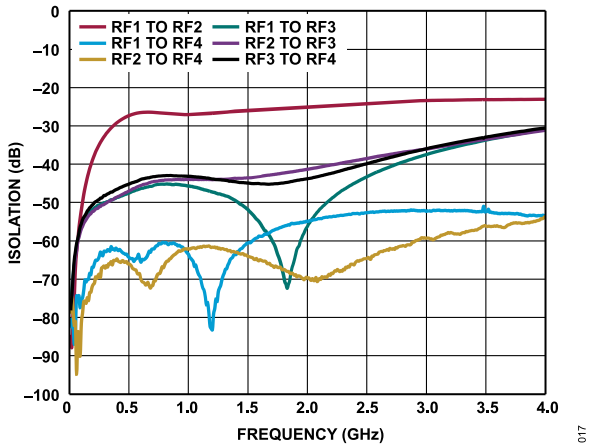

Figure 17. Channel-to-Channel Isolation vs. Frequency, RFC to RF3 Path Selected

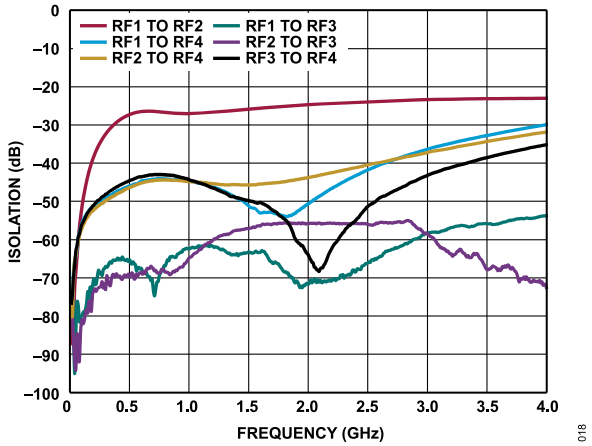

Figure 18. Channel-to-Channel Isolation vs. Frequency, RFC to RF4 Path Selected

TYPICAL PERFORMANCE CHARACTERISTICS

INPUT THIRD-ORDER INTERCEPT

V_{DD} = 5 V, V_{SS} = −3.4 V, V_{CTRL} = 0 V or 3.3 V, and T_{CASE} = 25°C on a 50 Ω system, unless otherwise noted.

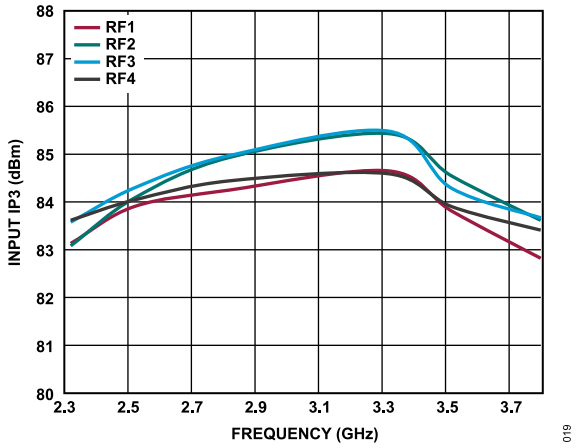

Figure 19. Input IP3 for RFC to RFx Selected vs. Frequency

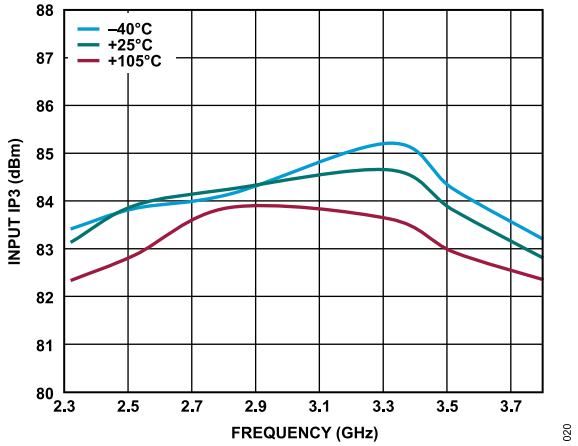

Figure 20. Input IP3 for RF1 vs. Frequency over Various Temperatures

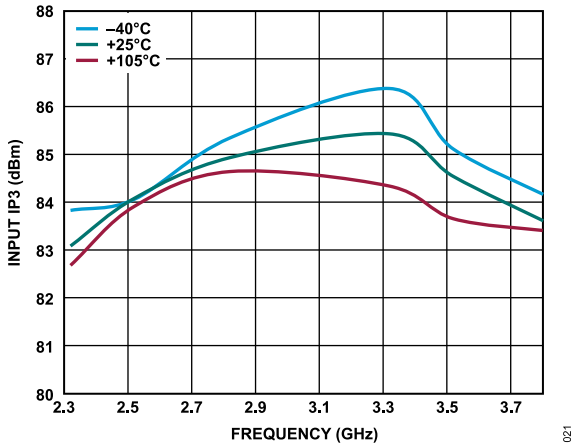

Figure 21. Input IP3 for RF2 vs. Frequency over Various Temperatures

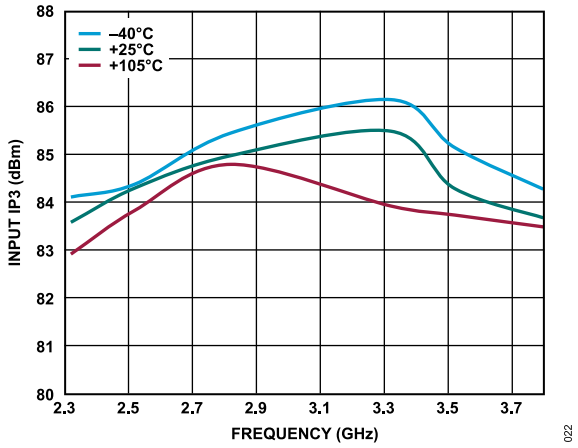

Figure 22. Input IP3 for RF3 vs. Frequency over Various Temperatures

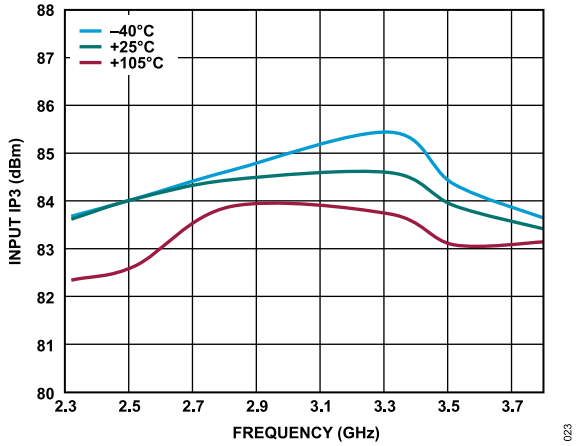

Figure 23. Input IP3 for RF4 vs. Frequency over Various Temperatures

THEORY OF OPERATION

The ADRF5347 integrates a driver to perform logic functions internally and to provide the advantage of a simplified LVCMOS-/LVTTL-compatible control interface. The driver features three digital control input pins (LS, V1, and V2) that control the state of the RFx paths. See Table 6.

POWER SUPPLY

The ADRF5347 requires a positive supply voltage applied to the V_{DD} pin and a negative voltage applied to the V_{SS} pin. Bypass capacitors are recommended on the supply and control lines to minimize RF coupling.

The ideal power-up sequence is as follows:

1. Connect GND.
2. Power up V_{DD} and V_{SS} voltages. Power up V_{SS} after V_{DD} to avoid current transients on V_{DD} during ramp up.
3. Apply the digital control inputs: LS, V1, and V2. Applying digital control inputs before the V_{DD} supply can inadvertently forward bias and damage the internal ESD protection structures. A series 1 kΩ resistor can be used to limit the current flowing into the control pin in such cases. If the control pins are not driven to a valid logic state (that is, controller output is in high impedance state) after V_{DD} is powered up, it is recommended to use pull-up and power-down resistors.
4. Apply an RF input signal.

The ideal power-down sequence is the reverse order of the power-up sequence.

RF INPUT AND OUTPUT

All of the RF ports (RFC and RF1 to RF4) are DC-coupled to 0 V, and no DC blocking is required at the RF ports when the RF line potential is equal to 0 V. The RF ports are internally matched to 50 Ω. Therefore, external matching networks are not required.

The insertion loss path conducts the RF signal between the selected RF throw port and the RF common port. The switch design is bidirectional with equal power handling. The RF input signal can be applied to the RFC port or the selected RF throw port. The isolation paths provide high loss between the insertion loss path and the unselected RF throw ports.

The logic select (LS) input allows to define the control input logic sequence for the RF path selections. The logic levels applied to the V1 and V2 pins determine which RFx port is in the insertion loss state while the other three paths are in the isolation state.

Table 6. Control Voltage Truth Table

Digital Control Inputs			RFx Paths			
LS	**V1**	**V2**	**RF1 to RFC**	**RF2 to RFC**	**RF3 to RFC**	**RF4 to RFC**
Low	Low	Low	Insertion loss (on)	Isolation (off)	Isolation (off)	Isolation (off)
Low	High	Low	Isolation (off)	Insertion loss (on)	Isolation (off)	Isolation (off)
Low	Low	High	Isolation (off)	Isolation (off)	Insertion loss (on)	Isolation (off)
Low	High	High	Isolation (off)	Isolation (off)	Isolation (off)	Insertion loss (on)
High	Low	Low	Isolation (off)	Isolation (off)	Isolation (off)	Insertion loss (on)
High	High	Low	Isolation (off)	Isolation (off)	Insertion loss (on)	Isolation (off)
High	Low	High	Isolation (off)	Insertion loss (on)	Isolation (off)	Isolation (off)
High	High	High	Insertion loss (on)	Isolation (off)	Isolation (off)	Isolation (off)

THEORY OF OPERATION

TIMING SPECIFICATIONS

ADRF5347's integrated control circuitry is triggered whenever any control inputs (V1, V2, and LS) are changed and switching is initiated. After the trigger instance, the control inputs must settle their final values within t_{PROG} and hold for t_{HOLD}. Switching completes after $t_{ON/OFF}$ and full RF power can be applied afterwards.

The switch state is defined after t_{PROG} and any further change on the control inputs is not processed by the control circuitry until t_{DEAD} elapses. Within the t_{DEAD} duration, control inputs can still be programmed and the control circuitry is triggered once the switch is ready for a new state if the programmed state is different than the existing state.

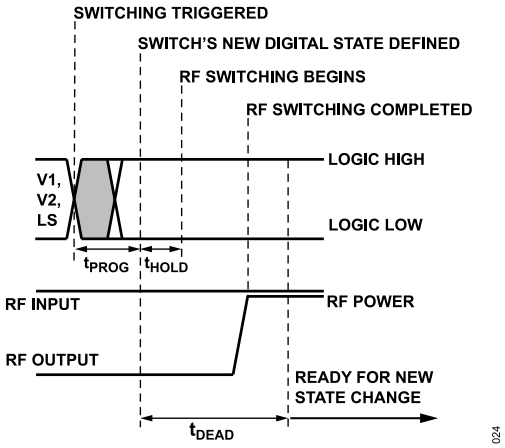

Figure 24. Timing Diagram

Table 7. Timing Specifications

Parameter	Description	Min	Typ	Max	Unit
t_{PROG}	Programming time			10	ns
t_{HOLD}	Hold time	20			ns
t_{DEAD}	Dead time	1.3		2	us

APPLICATION INFORMATION

The ADRF5347 has two power-supply pins (V_{DD} and V_{SS}) and three control pins (V1, V2, and LS). Figure 25 shows the external components and connections for the supply and control pins. The V_{DD} and V_{SS} pins are decoupled with a 100 pF and 4.7 µF multilayer ceramic capacitors. The control pins V1 and V2 are decoupled with 100 pF multilayer ceramic capacitors, while the LS control pin can be left floating or tied to ground. The device pinout allows to place the decoupling capacitors close to the device. No other external components are needed for bias and operation, except DC blocking capacitors on the RF pins when the RF lines are biased at a voltage different than 0 V. For more details, see the Table 5 section.

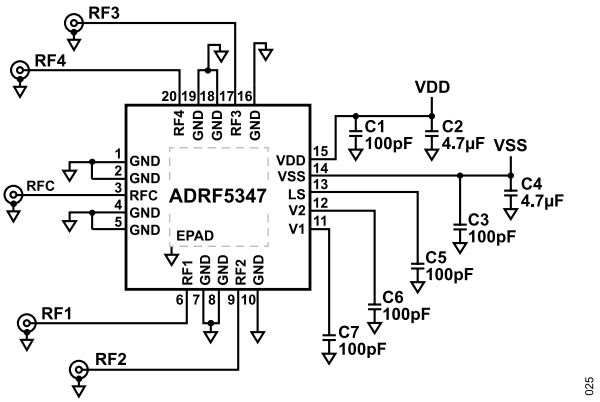

Figure 25. Recommended Schematic

RECOMMENDATIONS FOR PCB DESIGN

The RF ports are matched to 50 Ω internally and the pinout is designed to mate a coplanar waveguide (CPWG) with 50 Ω characteristic impedance on the PCB. Figure 26 shows the referenced CPWG RF trace design for an RF substrate with 10 mil thick Rogers RO4350 dielectric material. An RF trace with 18 mil width and 13 mil clearance is recommended for the 2.7 mil finished copper thickness.

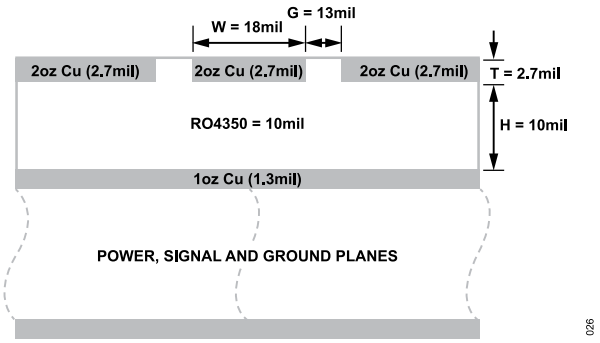

Figure 26. Example PCB Stack-Up

Figure 27 shows the routing of the RF traces, supply, and control signals from the device. The ground planes are connected with as many filled, through vias as allowed for optimal RF and thermal performance. The primary thermal path for the device is the bottom side.

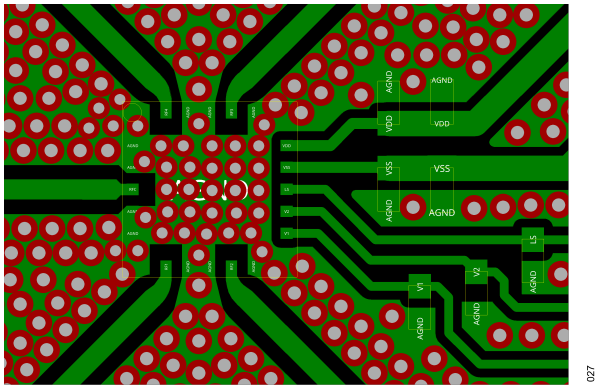

Figure 27. PCB Routings

Figure 28 shows the recommended layout from the device RF pins to the 50 Ω CPWG on the referenced stack-up. The ground pads are drawn as solder mask defined and the signal pads are drawn as pad defined. The RF trace from the PCB pad is extended with the same width and tapered to the RF trace with a 45° angle. The paste mask is also designed to match the pad without any aperture reduction. The paste is divided into multiple openings for the paddle.

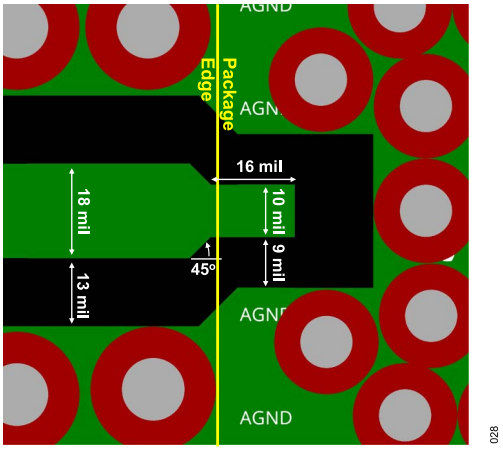

Figure 28. Recommended RF Pin Transitions

For alternate PCB stack-ups with different dielectric thickness and CPWG design, contact Analog Devices Technical Support for further recommendations.

APPLICATION INFORMATION

BACK-TO-BACK PHASE SHIFTER REFERENCE DESIGN

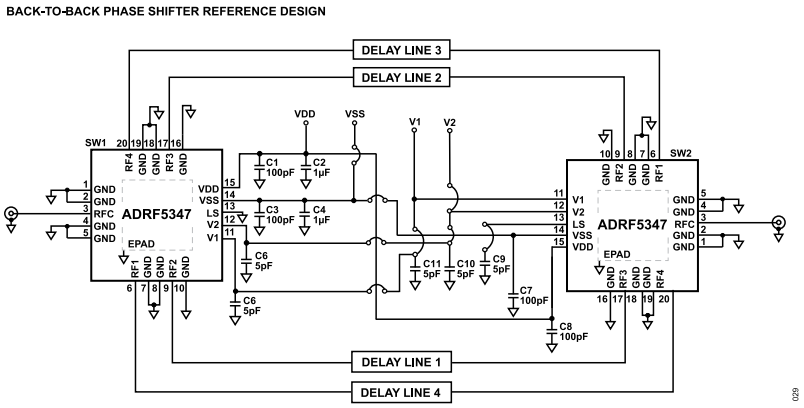

Figure 29. Back-to-Back Configuration Schematic

A typical application of the ADRF5347 is a four-step phase shifter achieved by connecting the SP4T switches back to back. Each RF arm may have a different delay line (Figure 29).

The switch control inputs, V1 and V2, can be connected together to configure the back-to-back phase shifter, which is achieved by applying inverted logic to the LS pin of SW1 and SW2. The LS pins do not require additional routing due to the internal pull-up. Therefore, the LS pin of ADRF5347 can be directly tied to ground or left floating.

Figure 30, Figure 31 and Figure 32 show a reference four-step phase shifter design with 0°, 30°, 60°, and 90° phases at 3.6 GHz. The plots represent the performance from the first switch's RFC terminal to the second switch's RF terminal, with reference planes at the package boundary. The design is implemented on a low loss, low passive intermodulation substrate Aerowave-300. Contact Analog Devices Technical Support for design files and further recommendations.

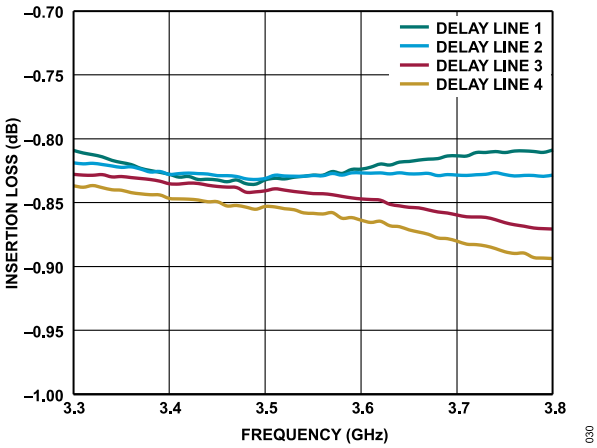

Figure 30. Back-to-Back Insertion Loss vs. Frequency

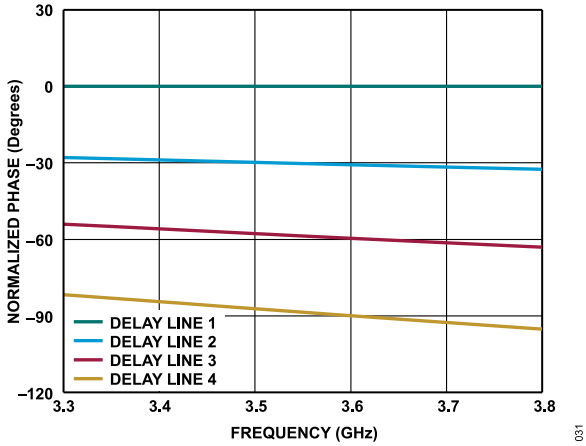

Figure 31. Back-to-Back Normalized Phase vs. Frequency

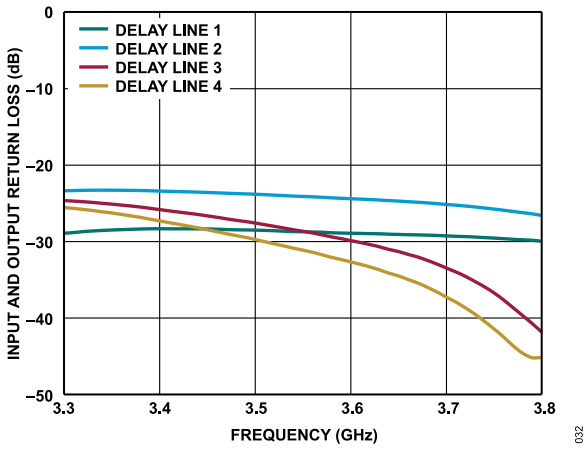

Figure 32. Input and Output Return Loss vs. Frequency

OUTLINE DIMENSIONS

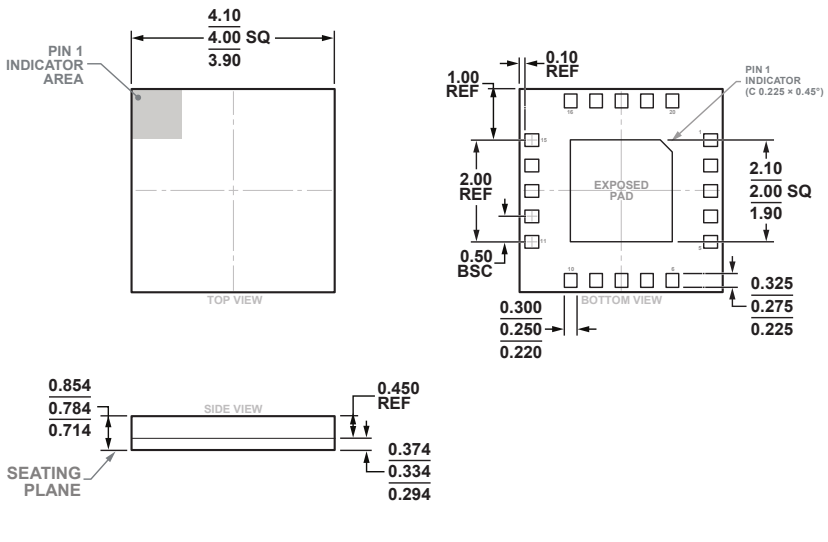

Figure 33. 20-Terminal Land Grid Array [LGA]
4 mm × 4 mm Body and 0.78 mm Package Height
(CC-20-14)
Dimensions shown in millimeters

Updated: June 15, 2023

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADRF5347BCCZN	-40°C to +105°C	20-Terminal Land Grid Array (LGA)	Cut Tape, 1	CC-20-14
ADRF5347BCCZN-R7	-40°C to +105°C	20-Terminal Land Grid Array (LGA)	7” Tape and Reel, 750	CC-20-14
ADRF5347BCCZN-RL	-40°C to +105°C	20-Terminal Land Grid Array (LGA)	13” Tape and Reel, 5000	CC-20-14

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Table 8. Evaluation Boards

Model[1]	Description
ADRF5347-EVALZ	Evaluation Board

[1] Z = RoHS-Compliant Part.

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