Data Sheet

AD4130-8

32 µA, Ultra Low Power, 24-Bit Sigma-Delta ADC with Integrated PGA and FIFO

FEATURES

- Ultralow current consumption (typical):
  - 32 µA: continuous conversion mode (gain = 128)
  - 5 µA: duty cycling mode (ratio = 1/16)
  - 0.5 µA: standby mode
  - 0.1 µA: power-down mode
- Built-in features for system level power savings:
  - Current saving duty cycle ratio: 1/4 or 1/16
  - Smart sequencer and per channel configuration minimizes host processor load
  - Deep embedded FIFO minimizes host processor load (depth of 256 samples)
  - Autonomous FIFO interrupt functionality, threshold detection
  - Single supply as low as 1.71 V increasing battery length
- RMS noise: 25 nV rms at 1.17 SPS (gain = 128) – 48 nV/√Hz
- Up to 22 noise free bits (gain = 1)
- Output data rate: 1.17 SPS to 2.4 kSPS
- Operates from 1.71 V to 3.6 V single supply or ±1.8 V split supplies
- Band gap reference with 15 ppm/°C maximum drift
- PGA with rail-to-rail analog input
- Adaptable sensor interfacing functionality:
  - Matched programmable excitation currents for RTDs
  - On-chip bias voltage generator for thermocouples
  - Low-side power switch for bridge transducers
  - Sensor open wire detection
- Internal temperature sensor and oscillator
- Self and system calibration
- Flexible filter options
- Simultaneous 50 Hz/60 Hz rejection (on selected filter options)
- General-purpose outputs
- Diagnostic functionality
- Crosspoint multiplexed inputs
  - 8 differential/16 pseudo differential inputs
- 5 MHz SPI (3-wire or 4-wire)
- Available in 35-ball, 2.74 mm × 3.6 mm WLCSP and 32-lead, 5 mm × 5 mm LFCSP
- Temperature range: −40°C to +105°C (WLCSP), −40°C to +125°C (LFCSP)
- AD4130-8 LFCSP pin compatible with AD7124-8 LFCSP

APPLICATIONS

- Smart transmitters
- Wireless battery and harvester powered sensor nodes
- Portable instrumentation
- Temperature measurement: thermocouple, RTD, thermistors
- Pressure measurement: bridge transducers
- Healthcare and wearables

FUNCTIONAL BLOCK DIAGRAM

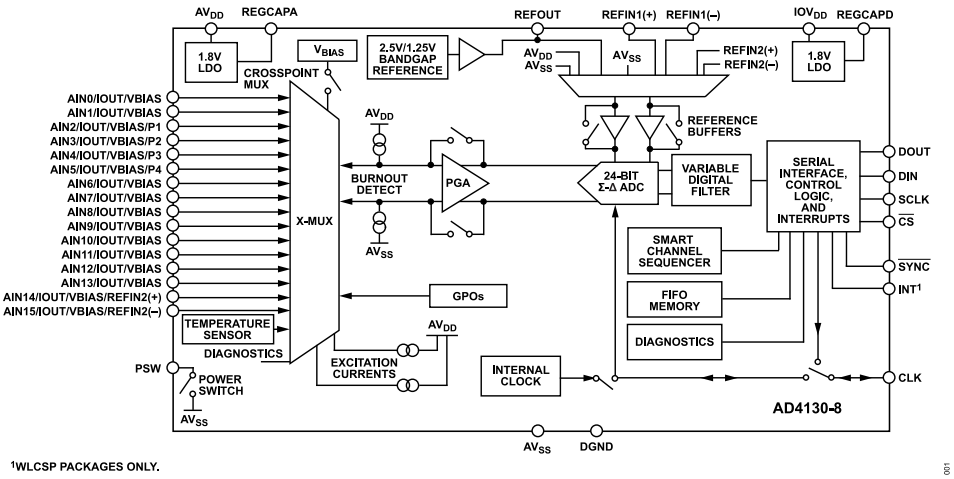

Figure 1. Functional Block Diagram

Analog Devices is in the process of updating documentation to provide terminology and language that is culturally appropriate. This is a process with a wide scope and will be phased in as quickly as possible. Thank you for your patience.

Rev. A

DOCUMENT FEEDBACK

TECHNICAL SUPPORT

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TABLE OF CONTENTS

Features ... 1
Applications ... 1
Functional Block Diagram ... 1
General Description ... 5
  Companion Products ... 5
Specifications ... 6
  ADC and AFE Specifications ... 6
  Analog Input Specifications ... 7
  Reference Specifications ... 7
  Sensor Biasing Specifications ... 8
  Diagnostics Specifications ... 9
  Rejection Specifications ... 9
  Logic Input and Output Specifications ... 11
  Power Specifications ... 11
  Timing Specifications ... 13
Absolute Maximum Ratings ... 18
  Thermal Characteristics ... 18
  Electrostatic Discharge (ESD) Ratings ... 18
  ESD Caution ... 18
Pin Configuration and Function Descriptions ... 19
Typical Performance Characteristics ... 26
  Offset Error and Gain Error ... 26
  INL Error and Oscillator ... 27
  Noise ... 28
  Analog Input Currents ... 29
  Supply Currents ... 31
  Reference Input Currents ... 32
  Internal Reference and Temperature Sensor ... 33
  Excitation Currents ... 34
  Resolution ... 35
  FFT ... 36
Terminology ... 37
Noise and Resolution ... 39
  2.5 V Reference ... 39
  1.25 V Reference ... 41
  Noise Spectral Density ... 44
Theory of Operation ... 45
  Overview ... 45
  ADC Core ... 45
  ADC Master Clock ... 46
  ADC Reference ... 46
  Analog Front End ... 47
  Programmable Gain Amplifier ... 48
  Other Features ... 49
  Power Supplies ... 49
  Power-Down Modes ... 50
Digital Interface ... 51
  Accessing the Register Map ... 51
  Device Reset ... 52
ADC Configuration and Operations ... 53
  Bipolar/Unipolar Configuration ... 53
  Status Bits ... 53
  Smart Channel Sequencer ... 54
  ADC Conversion Modes ... 55
  Data Ready Signal ... 57
  Continuous Read Mode ... 57
  System Synchronization ... 59
  ADC Calibration ... 59
Digital Filters ... 62
  $Sinc^3$ and $Sinc^4$ Filters ... 62
  Averaging Filters ... 62
  Post Filters ... 62
  Output Data Rate ... 63
  50 Hz and 60 Hz Rejection ... 64
  Sequencer ... 65
Diagnostics ... 69
  Signal Chain Check ... 69
  Reference Detection ... 69
  ADC Errors ... 69
  Overvoltage/Undervoltage Detection ... 69
  Power Supply Monitors ... 70
  Master Clock Counter ... 70
  SPI Diagnostics ... 70
  CRC Protection ... 70
  FIFO Diagnostics ... 71
  Burnout Currents ... 71
  Temperature Sensor ... 72
  Diagnostics and Standby Mode ... 72
FIFO ... 73
  FIFO Modes ... 73
  FIFO Readback ... 74
  FIFO Interrupt ... 77
  Clearing the FIFO ... 78
Applications Information ... 79
  Power Schemes ... 79
  Recommended Decoupling ... 79
  Input Filters ... 79
  Microprocessor Interfacing ... 79
  Unused Pins ... 79
  Power-Up and Initialization ... 80
  Layout and Grounding ... 80
  Assembly Guidelines ... 80
AD4130-8 Registers ... 82
  AD4130-8 Register Summary ... 82
  Registers Details ... 84
Outline Dimensions ... 112
  Ordering Guide ... 113
  Evaluation Boards ... 113

TABLE OF CONTENTS

REVISION HISTORY

6/2023—Rev. 0 to Rev. A

Added 32-Lead LFCSP (Universal) 1
Changes to Features Section 1
Changes to Companion Products Section 5
Changes to Gain Error Drift vs. Temperature Parameter, Table 1 6
Change to Table 2 7
Change to Table 3 7
Changes to Current Drift Matching Parameter, Table 4 8
Changes to REFIN1(+) Overvoltage Detect Level Parameter, REFIN1(−) Undervoltage Detect Level Parameter, A_{IN} OV Detect Level Parameter, and A_{IN} UV Detect Level Parameter, Table 5 9
Changes to Power Supply Rejection (AV_{DD}) Parameter and At DC Parameter, Table 6 9
Changes to Table 8 11
Changes to Figure 2 14
Changes to Figure 3 to Figure 6 15
Changes to Figure 7 to Figure 9 16
Changes to Figure 10 17
Changes to Figure 11 to Figure 13 17
Changes to Table 12 18
Added Table 14; Renumbered Sequentially 18
Changes to Table 15 19
Added Figure 15; Renumbered Sequentially 22
Added Table 16 22
Changes to Typical Performance Characteristics Section 26
Changes to Table 17 and Table 18 39
Changes to Table 19 to Table 22 40
Changes to Table 23 to Table 26 41
Changes to Table 27 41
Changes to Table 28 42
Changes to Table 29 42
Changes to Table 30 to Table 34 43
Changes to Table 35 and Table 36 44
Changes to Digital Interface Section 51
Changes to Figure 74 and Figure 75 51
Change to Table 44 51
Changes to Figure 76 52
Changes to Status Bits Section 53
Changes to Data Ready Signal Section and Table 55 57
Changes to Figure 82 and Figure 83 58
Changes to Figure 86 and Figure 87 63
Changes to Figure 100 and Figure 101 71
Changes to FIFO Readback Section 74
Changes to FIFO Ready Signal Section 74
Changes to Figure 104 to Figure 107 76
Changes to Table 72 77
Changes to Assembly Guidelines Section 80
Changes to Table 73 82
Changes to Table 77 86

TABLE OF CONTENTS

Changes to Table 79 89
Changes to Identification Register Section and Table 81 92
Updated Outline Dimensions 112
Changes to Ordering Guide 113
Changes to Evaluation Boards 113

5/2022—Revision 0: Initial Version

GENERAL DESCRIPTION

The AD4130-8 is an ultra low power, high precision, measurement solution for low bandwidth battery operated applications. The fully integrated analog front end (AFE) includes a multiplexer for up to 16 single-ended or eight differential inputs, programmable gain amplifier (PGA), 24-bit sigma-delta (Σ-Δ) analog-to-digital converter (ADC), on-chip reference and oscillator, selectable filter options, smart sequencer, sensor biasing and excitation options, diagnostics, and newly added features to improve the battery-operated lifetime (more than 5 years on a coin cell), that is, a first in, first out (FIFO) buffer and duty cycling.

The AD4130-8 allows users to measure low frequency signals with a current consumption of 28.5 µA (gain = 1) and 32.5 µA (gain = 128) while continuously converting, and even lower average currents when using one of the duty cycling options. The AD4130-8 can be configured to have 8 differential inputs or 16 single-ended or pseudo differential inputs, which connect to a crosspoint multiplexer, where any input pair can become a measurement channel input to the PGA and ADC.

The AD4130-8 is designed to allow the user to operate from a single analog supply voltage from 1.71 V to 3.6 V. In battery applications, operation as low as 1.71 V can extend the system lifetime as the AFE can continue its operation, even as the battery voltage dissipates. The digital supply can be separate and range from 1.65 V to 3.6 V.

Together with the reduced current consumption, the integration of an on-chip FIFO buffer can be used in tandem with the smart sequencer, to enable the AD4130-8 to become an autonomous measurement system, which allows the microcontroller to sleep for extended periods.

Intelligent interrupt functionality gives the user a greater confidence in both error detection and safety. The user can enable an interrupt signal to trigger when the samples in the FIFO reach a predefined value or when a user programmable threshold is exceeded.

The following key analog functions are offered on the AD4130-8 to allow simple and effective connection to transducers used for measuring temperature, load, and pressure:

- PGA. Due to the programmable gain (from 1 to 128) and the high input impedance with low input current, the PGA allows direct interfacing to transducers with low output amplitudes like resistive bridges, thermocouples, and resistance temperature detectors (RTDs).
- The capacitive PGA allows full common-mode input range, giving designers greater margin for widely varying input common modes. A wider common-mode input range improves the overall resolution and is highly effective in ratio metric measurements.
- Low drift precision current sources. The IEXC0 and IEXC1 current source can be used to excite 2-, 3-, and 4-wire RTDs. Excitation current output options include 100 nA, 10 µA, 20 µA, 50 µA, 100 µA, 150 µA, and 200 µA.
- The low-side power switch (PDSW) can be used to power down bridge sensors between conversions. The PDSW can be controlled within the sequencer on a per channel basis, allowing optimum timing and energy savings in the overall system. The PDSW can also allow higher powered analog sensors to be used in a low power system.
- Voltage bias for thermocouples (the VBIAS source sets the common-mode voltage of a channel to $AV_{DD}/2$).
- The smart sequencer allows the conversion of each enabled preconfigured channel in a predetermined order, allowing a mix of transducer, system checks, and diagnostic measurements to be interleaved. The sequencer eliminates need for repetitive serial interface communication with the device. Sixteen channels can be configured in the sequence, each of them selecting from eight predefined ADC setups that allow selection of gain, filter type, output data rate, buffering, timing, and reference source.

High levels of integrated front-end functionality coupled with small package options allow smaller end solutions. For example, the AD4130-8 integrates a low thermal drift band gap reference in addition to accepting an external differential reference, which can be internally buffered.

In safety critical applications the AD4130-8 includes diagnostic functionality such as open wire detection via burnout currents, internal temperature sensor, reference detection, and analog input overvoltage and undervoltage detection. Added diagnostics are included on the digital interface like cyclic redundancy check (CRC) and serial interface checks for a robust communication link.

COMPANION PRODUCTS

- Low Noise, Low Dropout Regulators: ADP150ACBZ-3.3 and ADP150ACBZ-1.8
- Regulated Charge-Pump Inverters: LTC1983ES6-3 and ADP7182AUJZ-1.8
- Voltage Reference: ADR391 or ADR3625
- Low Power Microcontrollers: MAX32670 (precision), MAX32655 (BLE), MAX32663A (ECG)

SPECIFICATIONS

AV_{DD} = 1.71 V to 3.6 V, IOV_{DD} = 1.65 V to 3.6 V, AV_{SS} = DGND = 0 V, REFIN1(+) = 2.5 V (for $AV_{DD} - AV_{SS} \geq 2.7$ V), REFIN1(+) = 1.25 V (for $AV_{DD} - AV_{SS} < 2.7$ V), REFIN1(−) = AV_{SS}, internal master clock (MCLK) (MCLK frequency (f_{MCLK}) = 76.8 kHz), PGA enabled (default), reference buffers bypassed (default), temperature range = T_{MIN} to T_{MAX}, and decoupling as per the Recommended Decoupling section, unless otherwise noted.

ADC AND AFE SPECIFICATIONS

Table 1. ADC and AFE Specifications

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
SAMPLING DYNAMICS					
Output Data Rate (ODR)	1.17		2400	SPS	See the Output Data Rate section
Active Time[2]		100%			Continuous conversion mode
		25%			DUTY_CYC_RATIO = 1/4[3]
		6.25%			DUTY_CYC_RATIO = 1/16[3]
STATIC PERFORMANCE					
No Missing Codes[2]	24			Bits	FS[4] > 2, sinc[4] filter
	24			Bits	FS[4] > 8, sinc[3] filter
Resolution and Update Rate[2]					See the Noise and Resolution section
RMS Noise and Update Rate[2]					See the Noise and Resolution section
Noise Spectral Density[2]					See the Noise and Resolution section
Integral Nonlinearity (INL)[2]	−5	±2	+5	ppm of FSR[1]	Gain = 1
	−15	±4	+15	ppm of FSR[1]	Gain > 1[5]
Offset Error[6]					
Before Calibration		±2		µV	Gain = 1, PGA bypass[7]
		±10		µV	Gain = 1 to 16
		±2		µV	Gain = 32 to 128
After Internal and System Calibration		In order of noise			
Offset Error Drift vs. Temperature[8]		3	30	nV/°C	Gain = 1, PGA bypass[7]
		120/gain	(140/gain) + 90	nV/°C	Gain = 1 to 128
Gain Error[6, 9]					
Before Calibration	−0.015		+0.015	%	Gain = 1[10], T_A = 25°C
		0.5		%	Gain = 1, PGA bypass[7]
		0.5		%	Gain > 1
After Internal Calibration[11]	−0.12	+0.01	+0.12	%	
After System Calibration[11]		In order of noise			
Gain Error Drift vs. Temperature		0.1	1	ppm/°C	Gain = 1, PGA bypass[7]
		0.1	2	ppm/°C	Gain = 1 to 16, T_A = −40°C to +105°C
		0.1	3	ppm/°C	T_A = −40°C to +125°C (LFCSP only)
		0.1	3	ppm/°C	Gain = 32 to 128, T_A = −40°C to +105°C
		0.1	4	ppm/°C	T_A = −40°C to +125°C (LFCSP only)

1 See the Terminology section.

2 These specifications are not production tested but are supported by characterization data at the initial product release.

3 Duty cycling mode is enabled by setting MODE = 0b1001 in the ADC_CONTROL register. The DUTY_CYC_RATIO bit can be found in the same register. See the Duty Cycling Mode and Duty Cycling Mode Timing sections.

4 FS is the decimal equivalent of the FS, Bits[10:0] in the filter registers.

5 The nonlinearity for gain > 1 is production tested for gain = 32 and voltage reference (V_{REF}) = 2.5 V. For the other conditions, this specification is supported by characterization data at the initial product release.

6 Following a system or internal zero-scale calibration, the offset error is in the order of the noise for the programmed gain and output data rate selected. A system full-scale calibration reduces the gain error to the order of the noise for the programmed gain and output data rate.

7 PGA_BYP_n = 1. The PGA_BYP_n bit can be found in each CONFIG_n register. See the Programmable Gain Amplifier section for more details.

SPECIFICATIONS

[8] Recalibration at any temperature removes these errors.

[9] Gain error applies to both positive and negative full scale. A factory calibration is performed at gain = 1 and T_A = 25°C (PGA_BYP_n = 0).

[10] This gain error is factory calibrated at ambient temperature and at a gain of 1 (PGA_BYP_n = 0).

[11] CAL_RANGE_X2 = 1 for V_{REF} > 2 V. The CAL_RANGE_X2 bit can be found in the MISC register. See the Internal Gain Calibration section for more details.

ANALOG INPUT SPECIFICATIONS

Table 2. Analog Input Specifications

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments[2]
ANALOG INPUT VOLTAGE[3]					V_{REF} = REFIN1(+) – REFIN1(−), or internal reference
Differential Input Voltage Ranges			±V_{REF}/gain	V	PGA on[4]
Absolute Analog Input (A_{IN}) Voltage Limits	AV_{SS} − 0.05		AV_{DD} + 0.05	V	
ANALOG INPUT CURRENT[3]					
Absolute Input Current					
Gain = 1	−3	±0.5	+3	nA	
Gain = 1		±2.5		nA	PGA bypass[5]
Gain > 1	−1	±0.5	+1	nA	
Differential Input Current					
Gain = 1	−3	±0.5	+3	nA	
Gain = 1		±1.5		nA	PGA bypass[5]
Gain > 1	−1	±0.5	+1	nA	
Analog Input Current Drift					
Gain = 1, Gain > 1		2	15	pA/°C	
Gain = 1		2		pA/°C	PGA bypass[5]
SYSTEM CALIBRATION[3]					
Calibration Limits					
Full Code			1.05 × V_{REF}/gain	V	DATA = 0xFFFFFF
Zero Code	−1.05 × V_{REF}/gain			V	DATA = 0x000000
Input Span	0.8 × V_{REF}/gain		2.1 × V_{REF}/gain	V	

[1] See the Terminology section.

[2] T_A = −40°C to +105°C.

[3] These specifications are not production tested but are supported by characterization data at the initial product release.

[4] PGA_BYP_n = 0, when V_{REF} > (AV_{DD} − AV_{SS} – 200 mV), the input differential range cannot exceed (AV_{DD} − AV_{SS} – 200 mV)/gain.

[5] PGA_BYP_n = 1. The PGA_BYP_n bit can be found in each CONFIG_n register. See the Programmable Gain Amplifier section for more details.

REFERENCE SPECIFICATIONS

Table 3. Reference Specifications

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments[2]
REFERENCE OUTPUT					Internal reference enabled, load capacitance (C_L) = 1 nF
Initial Accuracy	2.5 – 0.2%	2.5	2.5 + 0.2%	V	T_A = 25°C
	1.25 – 0.45%	1.25	1.25 + 0.45%	V	T_A = 25°C
Temperature Coefficient (TC) (Drift)[3]		2	15	ppm/°C	T_A = −40°C to +105°C, V_{REF} = 2.5 V
		2	15	ppm/°C	T_A = −40°C to +105°C, V_{REF} = 1.25 V
Output Current Load Capability		±1		mA	
Load Regulation Sourcing and Sinking		90		µV/mA	Change in output voltage (ΔV_{OUT})/change in output current (ΔI_{LOAD})
Power Supply Rejection		95		dB	

SPECIFICATIONS

Table 3. Reference Specifications (Continued)

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments[2]
Output Voltage Noise (0.1 Hz to 10 Hz)		40		µV p-p	T_A = 25°C
Output Voltage Noise Density		800		nV/√Hz	T_A = 25°C
Turn On Settling Time		280		µs	T_A = 25°C
REFERENCE INPUTS					Reference input (REFIN) = REFIN1(+) – REFIN1(−)
External REFIN Voltage[3]	0.5		AV_{DD} − AV_{SS}	V	
Absolute REFINx pins Voltage Limits[3]	AV_{SS} − 0.05		AV_{DD} + 0.05	V	Reference buffers disabled[4]
	AV_{SS} + 0.1		AV_{DD} – 0.1	V	Reference buffers enabled[4]
Reference Input Current					
Absolute Input Current	−11	±7	+11	nA	Reference buffers disabled[4]
	−4	±0.2	+4	nA	Reference buffers enabled[4]
Reference Input Current Drift[3]		10	21	pA/°C	Reference buffers disabled[4]
		1.6	20	pA/°C	Reference buffers enabled[4]
Normal Mode Rejection					Same as for analog inputs
Common-Mode Rejection		90		dB	

1 See the Terminology section.

2 T_A = −40°C to +105°C.

3 These specifications are not production tested but are supported by characterization data at the initial product release.

4 The REF_BUFP_n and REF_BUFM_n bits can be found in each CONFIG_n register. See the Reference Buffers section for more details.

SENSOR BIASING SPECIFICATIONS

Table 4. Sensor Biasing Specifications

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
EXCITATION CURRENT SOURCES (IEXC0 and IEXC1)					Available on any analog input pin
Output Current		10/20/50/100/150/200/0.1		µA	Selectable on a per channel basis
Initial Tolerance		±1		%	T_A = 25°C
Current Drift[2]		50		ppm/°C	
Current Matching[2, 3]	−1.6	±0.5	+1.6	%	10 µA/20 µA/50 µA/100 µA/150 µA/200 µA
	−3.2	±1	+3.2	%	100 nA
Current Drift Matching[2]		3	25	ppm/°C	10 µA/20 µA/50 µA/100 µA/150 µA/200 µA, T_A = −40°C to +105°C
			32		T_A = −40°C to +125°C (LFCSP only)
		5	60	ppm/°C	100 nA, T_A = −40°C to +105°C
			78		T_A = −40°C to +125°C (LFCSP only)
Line Regulation		0.1		%/V	10 µA/20 µA/50 µA/100 µA/150 µA/200 µA
		0.3		%/V	100 nA
Load Regulation		0.1		%/V	10 µA/20 µA/50 µA/100 µA/150 µA/200 µA
		2.5		%/V	100 nA
Output Compliance	AV_{SS} + 0.05		AV_{DD} − 0.27	V	2% accuracy
BIAS VOLTAGE (V_{BIAS}) GENERATOR					Available on any analog input pin
V_{BIAS}		(AV_{DD} + AV_{SS})/2		V	
Start-Up Time					Dependent on the capacitance connected to AINx
		3.7		µs/nF	AV_{DD} = 3.3 V, AV_{SS} = DGND
		6.7		µs/nF	AV_{DD} = 1.8 V, AV_{SS} = DGND
LOW-SIDE POWER SWITCH[2]					
On Resistance (R_{ON})		10	15	Ω	

SPECIFICATIONS

Table 4. Sensor Biasing Specifications (Continued)

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
Allowable Current			30	mA	Continuous current

1 See the Terminology section.

2 These specifications are not production tested but are supported by characterization data at the initial product release.

3 Matching between IOUT0 and IOUT1, V_{OUT} = 0 V.

DIAGNOSTICS SPECIFICATIONS

Table 5. Diagnostics Specifications

Parameter[1, 2]	Min	Typ	Max	Unit	Test Conditions/Comments
TEMPERATURE SENSOR					2.5 V external reference, gain = 1
Accuracy		±1		°C	After calibration at 25°C
Nominal Sensitivity[3]		860.66		µV/K	
Reading at 25°C		258		mV	
REFERENCE					REFIN = REFIN1(+) – REFIN1(−)
Reference Detect Threshold	0.7		1	V	
REFIN1(+) Overvoltage Detect Level	AV_{DD} + 0.13		AV_{DD} + 0.03	V	
REFIN1(−) Undervoltage Detect Level	AV_{SS} − 0.03		AV_{SS} − 0.13	V	
A_{IN} OVERVOLTAGE (OV) AND UNDERVOLTAGE (UV)					
A_{IN} OV Detect Level	AV_{DD} + 0.13		AV_{DD} + 0.03	V	
A_{IN} UV Detect Level	AV_{SS} − 0.03		AV_{SS} − 0.13	V	
BURNOUT CURRENTS					
A_{IN} Current		0.5, 2, 4		µA	

1 See the Terminology section.

2 These specifications are not production tested but are supported by characterization data at the initial product release.

3 Guaranteed by design.

REJECTION SPECIFICATIONS

Table 6. Rejection Specifications

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
POWER SUPPLY REJECTION (AV_{DD})					External MCLK, f_{MCLK} = 76.8 kHz, A_{IN} = 1 V/gain
	96			dB	Gain = 1, gain = 1 and PGA bypass[2], T_A = −40°C to +105°C
	79				T_A = −40°C to +125°C (LFCSP only)
	94			dB	Gain = 2 to 16, T_A = −40°C to +105°C
	90				T_A = −40°C to +125°C (LFCSP only)
	102			dB	Gain = 32 to 128, T_A = −40°C to +105°C
	96				T_A = −40°C to +125°C (LFCSP only)
COMMON-MODE REJECTION[3, 4, 5]					
At DC	86	90		dB	A_{IN} = 1 V, gain = 1, T_A = −40°C to +105°C
	85				T_A = −40°C to +125°C (LFCSP only)
	112	135		dB	A_{IN} = 1 V/gain, gain = 2 to 16
	108	122		dB	A_{IN} = 1 V/gain, gain = 32 to 128
$Sinc^3$ Filter					Input frequency (f_{IN}) = notch frequency (f_{NOTCH}) ± 1 Hz
At 50 Hz and 60 Hz	115			dB	10 SPS (FS = 240)
At 50 Hz	115			dB	50 SPS (FS = 48)
At 60 Hz	115			dB	60 SPS (FS = 40)
$Sinc^3$ + REJ60 Filter					f_{IN} = f_{NOTCH} ± 1 Hz

SPECIFICATIONS

Table 6. Rejection Specifications (Continued)

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
At 50 Hz and 60 Hz	115			dB	50 SPS (FS = 48)
Sinc^3 + Sinc^1 Averaging Filter					$f_{IN} = f_{NOTCH} \pm 1$ Hz
At 50 Hz	120			dB	40 SPS (FS = 6, first notch at 50 Hz)
At 60 Hz	120			dB	48 SPS (FS = 5, first notch at 60 Hz)
Sinc^4 + Sinc^1 Averaging Filter					$f_{IN} = f_{NOTCH} \pm 1$ Hz
At 50 Hz	115			dB	36.36 SPS (FS = 6, first notch at 60 Hz)
At 60 Hz	115			dB	43.63 SPS (FS = 5, first notch at 50 Hz)
Post Filters					$f_{IN} = f_{NOTCH} \pm 1$ Hz
At 50 Hz and 60 Hz	125			dB	Post Filter 1, ODR = 26.087 SPS
	125			dB	Post Filter 2, ODR = 24 SPS
	125			dB	Post Filter 3, ODR = 19.355 SPS
	120			dB	Post Filter 4, ODR = 16.21 SPS
NORMAL MODE REJECTION[3, 4]					
Sinc^3 Filter					$f_{IN} = f_{NOTCH} \pm 1$ Hz
External Clock					
At 50 Hz and 60 Hz	100			dB	10 SPS (FS = 240)
	65			dB	50 SPS (FS = 48), Sinc^3 + REJ60 filter
At 50 Hz	95			dB	50 SPS (FS = 48)
At 60 Hz	98			dB	60 SPS (FS = 40)
Internal Clock					
At 50 Hz and 60 Hz	84			dB	10 SPS (FS = 240)
	58			dB	50 SPS (FS = 48), Sinc^3 + REJ60 filter
At 50 Hz	79			dB	50 SPS (FS = 48)
At 60 Hz	81			dB	60 SPS (FS = 40)
Averaging Filters					$f_{IN} = f_{NOTCH} \pm 0.5$ Hz
External Clock					
At 50 Hz	40			dB	FS = 6
At 60 Hz	42			dB	FS = 5
Internal Clock					
At 50 Hz	30			dB	
At 60 Hz	31			dB	
Post Filters					$f_{IN} = f_{NOTCH} \pm 1$ Hz
External Clock					
At 50 Hz and 60 Hz	46			dB	Post Filter 1, ODR = 26.087 SPS
	62			dB	Post Filter 2, ODR = 24 SPS
	86			dB	Post Filter 3, ODR = 19.355 SPS
	91			dB	Post Filter 4, ODR = 16.21 SPS
Internal Clock					
At 50 Hz and 60 Hz	40			dB	Post Filter 1, ODR = 26.087 SPS
	54			dB	Post Filter 2, ODR = 24 SPS
	73			dB	Post Filter 3, ODR = 19.355 SPS
	77			dB	Post Filter 4, ODR = 16.21 SPS

1 See the Terminology section.

2 PGA_BYP_n = 1. The PGA_BYP_n bit can be found in each CONFIG_n register. See Programmable Gain Amplifier section for more details.

3 These specifications are not production tested but are supported by characterization data at the initial product release.

4 FS is the decimal equivalent of the FS, Bits[10:0] in the filter registers.

5 When gain > 1, the common-mode voltage is between (AV_{SS} + 0.1 + 0.5/gain) and (AV_{DD} − 0.1 − 0.5/gain).

SPECIFICATIONS

LOGIC INPUT AND OUTPUT SPECIFICATIONS

Table 7. Logic Input and Output Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC INPUTS[1, 2]					
Input Low Voltage (V_{INL})	0		0.3 × IOV_{DD}	V	1.65 V ≤ IOV_{DD} < 3.6 V
Input High Voltage (V_{INH})	0.7 × IOV_{DD}		IOV_{DD}	V	1.65 V ≤ IOV_{DD} < 3.6 V
Voltage Hysteresis		0.5		V	1.65 V ≤ IOV_{DD} < 3.6 V
Current	−1		+1	µA	Input voltage (V_{IN}) = IOV_{DD} or DGND
Pin Capacitance		10		pF	Per digital pin
LOGIC OUTPUTS[1, 2] (INCLUDING CLK)					
Output Low Voltage (V_{OL})	0		0.4	V	Sink current (I_{SINK}) = 100 µA
Output High Voltage (V_{OH})	IOV_{DD} – 0.35		IOV_{DD}	V	Source current (I_{SOURCE}) = 100 µA
Floating State Leakage Current	−1		+1	µA	
Floating State Output Capacitance		10		pF	
Data Output Coding[3]		Offset binary			Bipolar bit = 0b1, default setting
		Straight binary			Bipolar bit = 0b0
CLOCK					
Internal Cock					
Frequency	76.8 – 2%	76.8	76.8 + 2%	kHz	
Duty Cycle[2]		50:50		%	
Wake-Up Time[2, 4]		850		µs	
External Clock[2]					
Frequency		76.8		kHz	
Duty Cycle		45:55 to 55:45		%	
DIGITAL OUTPUTS (P1 to P4)[5]					
Output Low Voltage (V_{OL})[2]	0		0.4	V	I_{SINK} = 100 µA
Output High Voltage (V_{OH})[2]	AV_{DD} – 0.6		AV_{DD}	V	I_{SOURCE} = 100 µA

1 See Pin Configuration and Function Descriptions section.

2 These specifications are not production tested but are supported by characterization data at the initial product release.

3 The bipolar bit can be found in the ADC_CONTROL register. See the Data Output Coding section for more details.

4 See also Out of Standby Mode Timing section for further details.

5 General-purpose output pins used as digital pins require AV_{SS} = DGND and AV_{DD} = IOV_{DD}. See the General-Purpose Output section.

POWER SPECIFICATIONS

Table 8. Power Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER SUPPLY VOLTAGE					
AV_{DD} to AV_{SS}	1.71		3.6	V	
IOV_{DD} to DGND	1.65		3.6	V	
AV_{SS} to DGND	–1.8		0	V	
AV_{DD} to DGND	0.9			V	
IOV_{DD} to AV_{SS}			5.4	V	
POWER SUPPLY CURRENTS[1]					
AV_{DD} Current					Internal oscillator enabled
External Reference					
Gain = 1		20	23	µA	PGA bypass[2]
			24	µA	T_{MAX} = 125°C
Gain = 1 to 16		25	30	µA	Continuous conversion mode current

SPECIFICATIONS

Table 8. Power Specifications (Continued)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
			32	µA	T_{MAX} = 125°C
		7.5		µA	DUTY_CYC_RATIO = 1/4[3]
		2.5		µA	DUTY_CYC_RATIO = 1/16[3]
Gain = 32 to 128		29	35	µA	Continuous conversion mode current
			38	µA	T_{MAX} = 125°C
		8.5		µA	DUTY_CYC_RATIO = 1/4[3]
		3		µA	DUTY_CYC_RATIO = 1/16[3]
Increase due to Reference Buffer[4],		0.25		µA	Per reference buffer
Increase due to Internal Reference[4]		6.5	8	µA	Continuous conversion mode current
		1.75		µA	DUTY_CYC_RATIO = 1/4[3]
		0.45		µA	DUTY_CYC_RATIO = 1/16[3]
Increase due to V_{BIAS} on[4]		1	1.2	µA	
IOV_{DD} Current		3.5	6.9	µA	Continuous conversion mode current
			12.5	µA	T_{MAX} = 125°C
		1.8		µA	DUTY_CYC_RATIO = 1/4[3]
		1.4		µA	DUTY_CYC_RATIO = 1/16[3]
Increase due to FIFO		50		nA	
POWER-DOWN CURRENTS[1]					
Standby Mode Current					
AV_{DD}		0.2	1.3	µA	Analog low dropout (LDO) regulator on
			2.5	µA	T_{MAX} = 125°C
IOV_{DD}		0.35	3.5	µA	Digital LDO regulator on
			11	µA	T_{MAX} = 125°C
Power-Down Mode Current					
AV_{DD}		0.01	1	µA	Analog LDO regulator off
			1.2	µA	T_{MAX} = 125°C
IOV_{DD}		0.13	1	µA	Digital LDO regulator off
OPERATING TEMPERATURE RANGE					
T_{MIN}	−40			°C	
T_{MAX}			105	°C	Wafer level chip scale package (WLCSP)
			125	°C	Lead frame chip scale package (LFCSP)

1 The digital inputs are equal to IOV_{DD} or DGND with excitation currents disabled.

2 PGA_BYP_n = 1. The PGA_BYP_n bit can be found in each CONFIG_n register. See the Programmable Gain Amplifier section for more details.

3 Duty cycling mode is enabled by setting MODE = 0b1001 in the ADC_CONTROL register. The DUTY_CYC_RATIO bit can be found in the same register. See the Duty Cycling Mode and Duty Cycling Mode Timing sections.

4 These specifications are not production tested but are supported by characterization data at the initial product release.

SPECIFICATIONS

TIMING SPECIFICATIONS

AV_{DD} = 1.71 V to 3.6 V, IOV_{DD} = 1.65 V to 3.6 V, AV_{SS} = DGND = 0 V, Input Logic 0 = DGND = 0 V, Input Logic 1 = IOV_{DD}, internal MCLK (f_{MCLK} = 76.8 kHz), temperature range = T_{MIN} to T_{MAX}, and decoupling as outlined in the Recommended Decoupling section, unless otherwise noted. All digital input signals are specified with rise time (t_R) = fall time (t_F) = 5 ns (10% to 90% of IOV_{DD} and timed from a voltage level of IOV_{DD}/2).

Table 9. Timing Specifications

Parameter[1]	Symbol	Min	Max	Unit
REGISTER ACCESS IN 3-WIRE MODE[2, 3, 4]				
SCLK Cycle Time	t_{SCK}	200		ns
SCLK High Pulse Width	t_{SCKH}	90		ns
SCLK Low Pulse Width	t_{SCKL}	90		ns
DIN Data Setup Time	t_{DIN_SET}	10		ns
DIN Data Hold Time	t_{DIN_HOL}	10		ns
SCLK Falling Edge to DOUT Becomes Available	t_{DOUT_VALID}		80	ns
SCLK Falling Edge to DOUT Remains Available	t_{DOUT_HOL}	10		ns
SCLK Rising Edge to DOUT Disable Delay[5]	$t_{DOUT_DIS_DEL}$			
DOUT_DIS_DEL = 0[6]		10		ns
DOUT_DIS_DEL = 1[6]		100		ns
Delay Between Consecutive Write Operations[7] (Last SCLK Rising to First SCLK Falling)	t_{WR_DEL}	3/f_{MCLK}	4/f_{MCLK}	sec
Data Ready[8] High Time if Data Ready is Low and the Next Conversion is Available	t_{RDYH}	4/f_{MCLK}		sec
Last SCLK Rising for SW Reset Serial Peripheral Interface (SPI) Transaction to First SCLK Falling for Next SPI Transaction	t_{RESET_DELAY}	160/f_{MCLK}		sec
REGISTER ACCESS IN 4-WIRE MODE[2, 3, 9]				
$\overline{CS}$ Falling Edge to DOUT Enable Time[10]	t_{DOUT_EN}		80	ns
$\overline{CS}$ Setup Time: $\overline{CS}$ Falling Edge to First SCLK Falling Edge	t_{CS_SET}	0		ns
$\overline{CS}$ Hold Time: Last SCK Rising Edge to $\overline{CS}$ Rising Edge Delay	t_{CS_HOL}	0		ns
$\overline{CS}$ Rising Edge to DOUT Disable Time[10]	t_{DOUT_DIS}		80	ns
$\overline{CS}$ High Pulse Width (Between Read/Write Operations)	t_{CS_PW}	20		ns
$\overline{CS}$ Rising Edge for SW Reset SPI Transaction to $\overline{CS}$ Falling Edge for Next SPI Transaction	t_{RESET_DELAY}	160/f_{MCLK}		sec
CONTINUOUS READ MODE[11]				
Data Ready[8] Falling Edge to First SCLK Falling Edge	t_{RDYL_SCKL}	20		ns
SCLK Falling Edge to New DOUT Becomes Available	t_{DOUT_VALID}		80	ns
SYNCHRONIZATION MODE[12]				
$\overline{SYNC}$ Low Pulse Width	t_{SYNC_PW}	4/f_{MCLK}		sec
STANDBY MODE				
Wake-Up Time from SPI Write to Exit Standby Mode[13]	t_{WU_STBY}		36/f_{MCLK}	sec
DUTY CYCLING				
Wake Up Time	t_{WU_DUTY}		32/f_{MCLK}	sec

1 These specifications are not production tested but are supported by characterization data at the initial product release.

2 The device operates with SPI Mode 3: SCLK idles high, the falling edge of SCLK is the drive edge for DOUT, and the rising edge of SCLK is the sample edge for DIN.

3 CSB_EN = 0b0 (default) in the ADC_CONTROL register (3-wire mode). Change this bit to 1 to enable 4-wire mode.

4 See the 3-Wire Mode Timing Diagrams section.

5 $\overline{CS}$ pin held low.

6 This bit can be found in the ADC_CONTROL register and it is only active if CSB_EN = 0b0 in the same register.

7 Applies only when $\overline{SYNC}$ is high, or MM_CRC_ERR_EN = 0b1 and only for ADC_CONTROL and error register writes.

8 For the data ready signal related timing specifications, the INT pin is considered (INT_PIN_SEL = 0b00 in the IO_CONTROL register). See the Data Ready Signal section.

9 See the 4-Wire Mode Timing Diagrams section.

SPECIFICATIONS

[10] In 4-wire mode (CSB_EN = 0b1), the DOUT pin changes from tristate ($\overline{CS}$ pin high) to enabled after the $\overline{CS}$ falling edge, then changes back to tristate following the $\overline{CS}$ rising edge. In 3-wire mode, $\overline{CS}$ pin can still be used to enable ($\overline{CS}$ pin low) and disable ($\overline{CS}$ pin high) the DOUT pin.

[11] Set CONT_READ = 0b1 in the ADC_CONTROL register to enable continuous read mode. See the Continuous Read Mode Timing Diagram and Continuous Read Mode sections for details.

[12] See the System Synchronization section.

[13] Internal oscillator is kept alive. See the internal clock wake-up time specification in Table 7 and the Out of Standby Mode Timing section for further details.

Table 10. FIFO Timing Specifications

Parameter[1]	Symbol	Min	Max	Unit
FIFO RELATED[2]				
FIFO Ready Signal[3] High Time when FIFO Is Busy	t_{BSY}	$4/f_{MCLK}$		sec
FIFO Interrupt Signal[4] Rising Edge to FIFO Read Start ($\overline{CS}$ Falling Edge or SCLK Falling Edge)[5]	t_{INT_RD}	$1.5/f_{MCLK}$		sec
FIFO Quiet Time Between Write and Read Access (FIFO Ready Signal[3] Falling Edge to FIFO Read Start[6])	t_{QUIET1}	0		ns
SCLK Falling Edge to DOUT Becomes Available	t_{DOUT_VALID}		80	ns
SCLK Falling Edge to DOUT Remains Available	t_{DOUT_HOL}	10		ns
FIFO Quiet Time Between Read and Write Access (FIFO Read End[7] to FIFO Ready Signal[3] Rising Edge)	t_{QUIET2}	$4/f_{MCLK}$		sec
FIFO Clear Delay (After $\overline{SYNC}$ Low or After Write to FIFO_CONTROL Register)[8]	t_{CLR}[9]		$8/f_{MCLK}$	sec
$\overline{SYNC}$ Low Pulse Width to Clear FIFO	t_{SYNC_PW}	$4/f_{MCLK}$		sec

[1] These specifications are not production tested but are supported by characterization data at the initial product release.

[2] See the FIFO Timing Diagrams and FIFO sections.

[3] For the FIFO ready signal related timing specifications, the DOUT pin is considered.

[4] For the FIFO interrupt signal related timing specifications, the INT pin is considered (INT_PIN_SEL = 0b00 in the IO_CONTROL register).

[5] This specification applies to the FIFO watermark interrupt.

[6] $\overline{CS}$ falling edge (4-wire mode) or SCLK falling edge (3-wire mode and $\overline{CS}$ tied low).

[7] $\overline{CS}$ rising edge (4-wire mode) or SCLK rising edge (3-wire mode and $\overline{CS}$ tied low).

[8] See the Clearing the FIFO section.

[9] Guaranteed by design.

3-Wire Mode Timing Diagrams

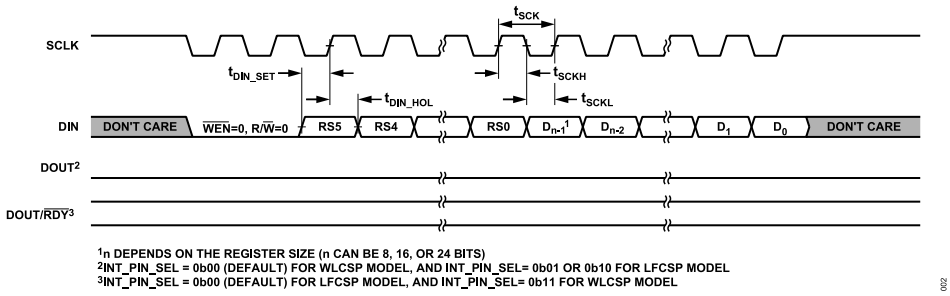


Figure 2. Write Cycle Timing Diagram, 3-Wire Mode (CSB_EN Bit Set to 0), $\overline{CS}$ Pin Tied Low

SPECIFICATIONS

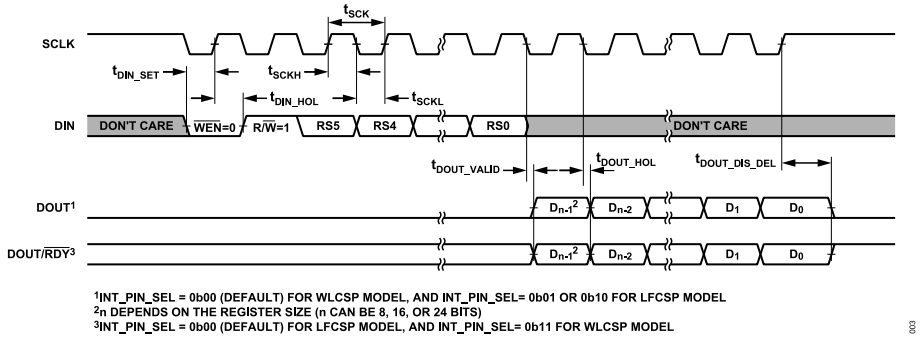


Figure 3. Read Cycle Timing Diagram, 3-Wire Mode (CSB_EN Bit Set to 0), $\overline{CS}$ Pin Tied Low

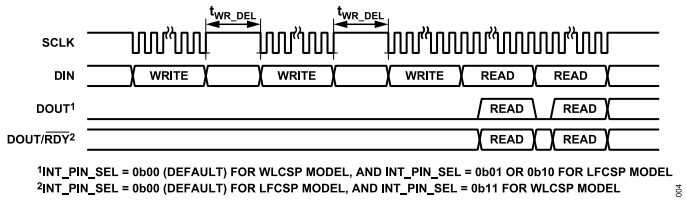


Figure 4. Delay Between Consecutive Serial Operations, 3-Wire Mode (CSB_EN Bit Set to 0), $\overline{CS}$ Pin Tied Low

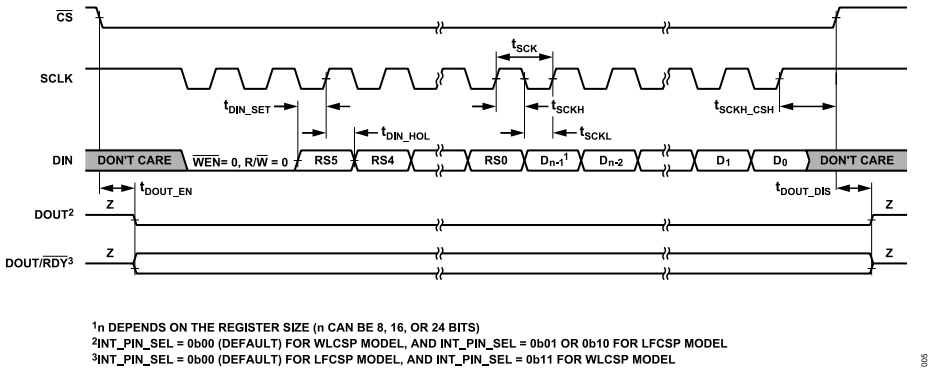


Figure 5. Write Cycle Timing Diagram, 3-Wire Mode (CSB_EN Bit Set to 0), $\overline{CS}$ Pin Used to Tristate the DOUT Pin

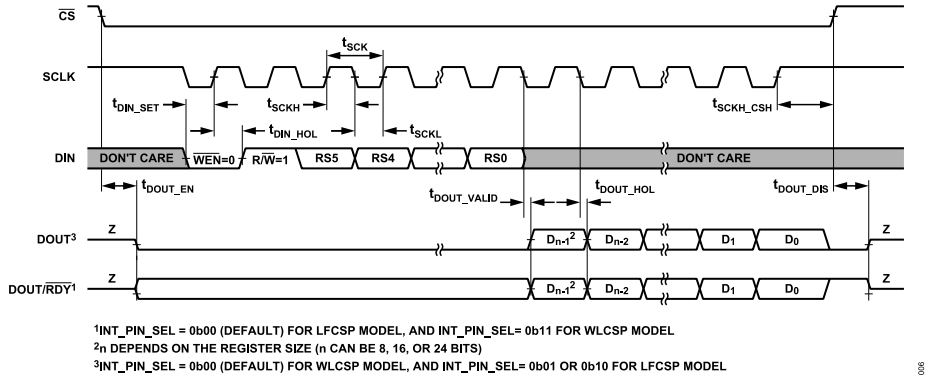
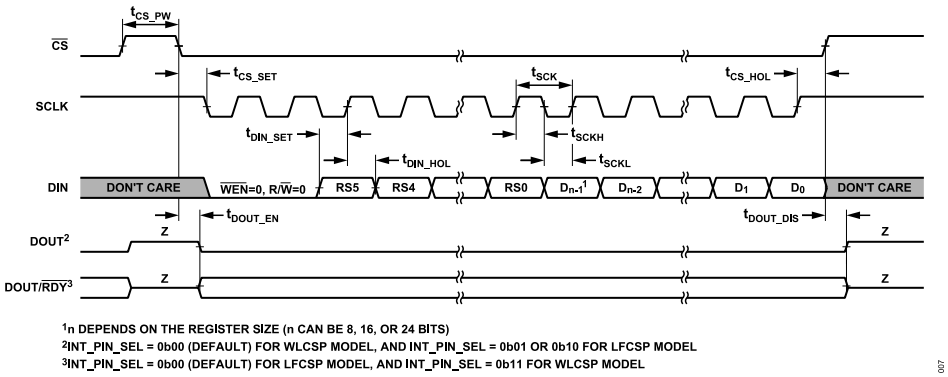


Figure 6. 3-Wire Mode Read Cycle Timing Diagram, 3-Wire Mode (CSB_EN Bit Set to 0), $\overline{CS}$ Pin Used to Tristate the DOUT Pin

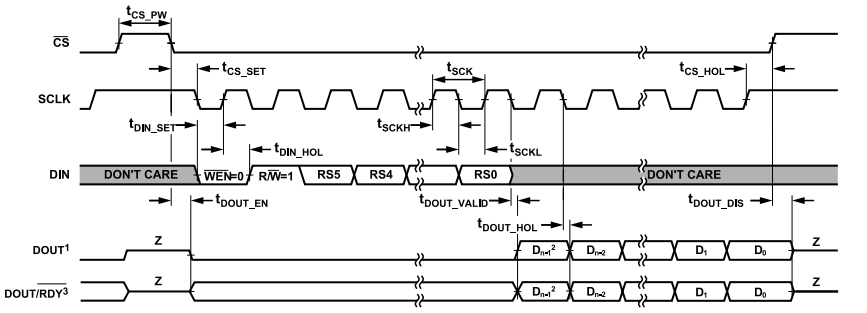
SPECIFICATIONS

4-Wire Mode Timing Diagrams



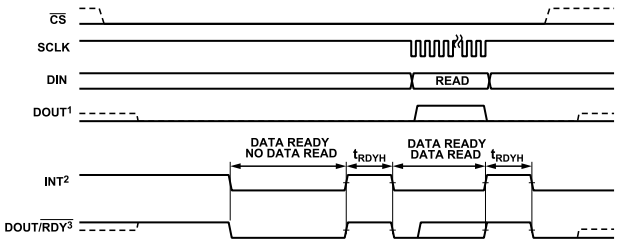
[1]n DEPENDS ON THE REGISTER SIZE (n CAN BE 8, 16, OR 24 BITS)
[2]INT_PIN_SEL = 0b00 (DEFAULT) FOR WLCSP MODEL, AND INT_PIN_SEL = 0b01 OR 0b10 FOR LFCSP MODEL
[3]INT_PIN_SEL = 0b00 (DEFAULT) FOR LFCSP MODEL, AND INT_PIN_SEL = 0b11 FOR WLCSP MODEL

Figure 7. Write Cycle Timing Diagram, 4-Wire Mode (CSB_EN Bit Set to 1)



[1]INT_PIN_SEL = 0b00 (DEFAULT) FOR WLCSP MODEL, AND INT_PIN_SEL = 0b01 OR 0b10 FOR LFCSP MODEL
[2]n DEPENDS ON THE REGISTER SIZE (n CAN BE 8, 16, OR 24 BITS)
[3]INT_PIN_SEL = 0b00 (DEFAULT) FOR LFCSP MODEL, AND INT_PIN_SEL = 0b11 FOR WLCSP MODEL

Figure 8. Read Cycle Timing Diagram, 4-Wire Mode (CSB_EN Bit Set to 1)



[1]INT_PIN_SEL = 0b00 (DEFAULT) FOR WLCSP MODEL, AND INT_PIN_SEL = 0b01 FOR LFCSP MODEL
[2]INT_PIN_SEL = 0b00 (DEFAULT) FOR WLCSP MODEL, INT_PIN AS DATA READY SIGNAL
[3]INT_PIN_SEL = 0b00 (DEFAULT) FOR LFCSP MODEL, AND INT_PIN_SEL = 0b11 FOR WLCSP MODEL

Figure 9. Data Ready High Time when Data Ready is Initially Low and the Next Conversion is Available

SPECIFICATIONS

Continuous Read Mode Timing Diagram

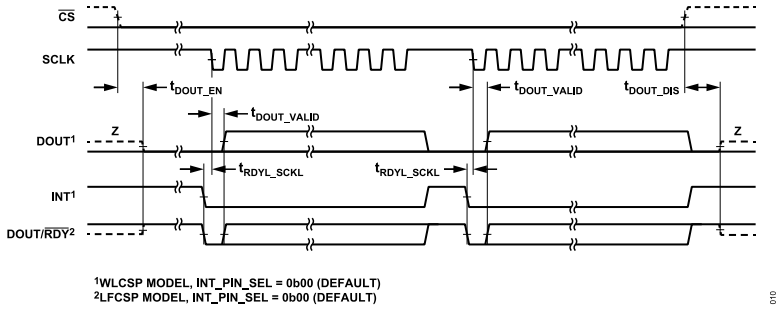


Figure 10. Continuous Read Mode Timing

FIFO Timing Diagrams

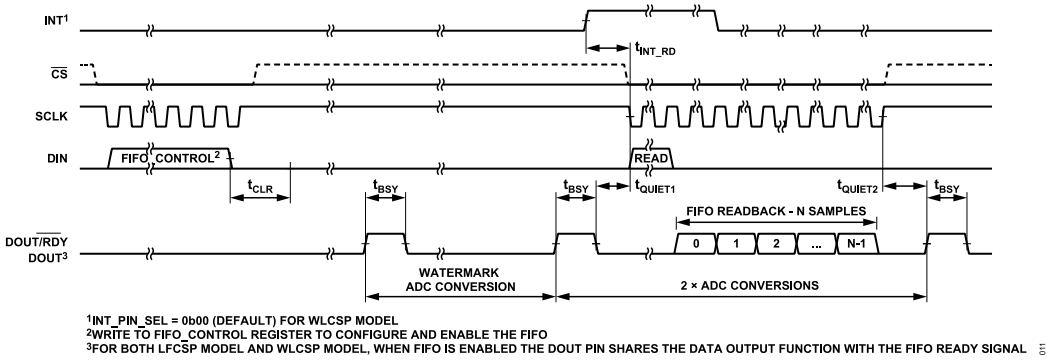


Figure 11. FIFO Timing with Watermark Interrupt

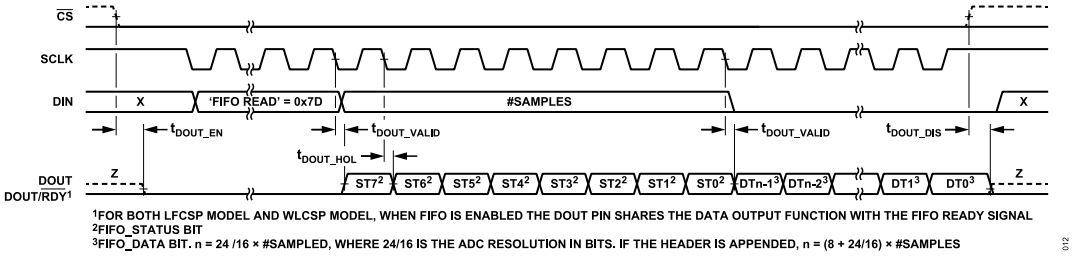


Figure 12. FIFO Readback Timing Diagram

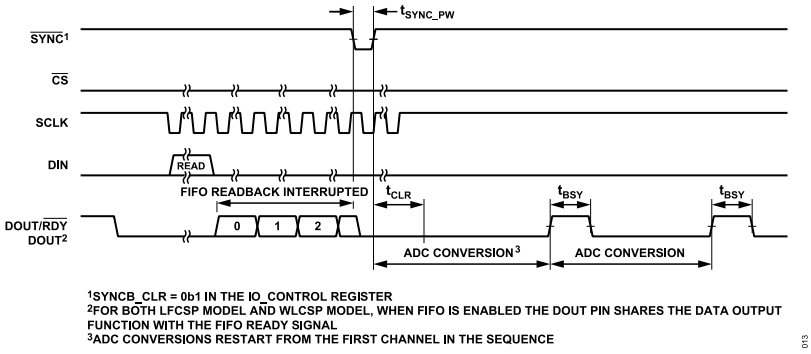


Figure 13. FIFO Clear Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 11. Absolute Maximum Ratings

Parameter	Rating
AV_{DD} to AV_{SS}	−0.3 V to +3.96 V
IOV_{DD} to DGND	−0.3 V to +3.96 V
IOV_{DD} to AV_{SS}	−0.3 V to +5.94 V
AV_{SS} to DGND	−1.98 V to +0.3 V
AINx to AV_{SS}	−0.3 V to AV_{DD} + 0.3 V
REFIN1(+), REFIN1(−) to AV_{SS}	−0.3 V to AV_{DD} + 0.3 V
Digital Inputs[1] to DGND	−0.3 V to IOV_{DD} + 0.3 V
Digital Outputs[1] to DGND	−0.3 V to IOV_{DD} + 0.3 V
AINx/Digital Input Current	10 mA
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J)	150°C
Lead Temperature, Soldering Reflow	260°C, as per JEDEC J-STD-020

[1] See the Pin Configuration and Function Descriptions section for a list of the digital input and digital output pins.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Absolute maximum ratings are tested individually only, not in combination, and they all apply for any given configuration.

THERMAL CHARACTERISTICS

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

Thermal resistance values specified in Table 12 were calculated based on JEDEC specifications and must be used in compliance with JESD51-12.

Table 12. Thermal Resistance

Package Type[1]	θ_{JA}	θ_{JB}	θ_{JC_TOP}	Ψ_{JB}	Ψ_{JT}	Unit
CB-35-3	46.2	11	0.32	4.4	0.2	°C/W
CP-32-12	40.7	12.1	16	N/A	N/A	°C/W

[1] The values in Table 12 were calculated based on the standard JEDEC 2S2P thermal test board with 6 × 11 thermal vias. See the JEDEC JESD51 series.

θ_{JA}, θ_{JB}, and θ_{JC} are mainly used to compare the thermal performance of the package of the device with other semiconductor packages when all test conditions listed are similar. θ_{JA}, θ_{JB}, and θ_{JC} can be used for first order approximation of the junction temperature in the system environment.

For WLCSP devices, using Ψ_{JB} or Ψ_{JT} is a more appropriate way to estimate the worst-case junction temperature of the device in the system environment if an accurate thermal measurement of the board temperature near the device under test (DUT) or directly on the package top surface operating in the system environment is available.

Using the parameters listed in Table 12 in accordance with JEDEC standards in the JESD51 series is recommended.

The AD4130-8 can be damaged when T_J limits are exceeded. See Table 11 for the absolute maximum junction temperature specification. Monitoring the ambient temperature does not guarantee that T_J is within the specified maximum temperature limits. In applications with high power dissipation and/or poor thermal resistance, T_J must be monitored using the internal temperature sensor.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Field induced charged device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

Machine model (MM) per ANSI/ESD STM5.2. MM voltage values are for characterization only.

ESD Ratings for AD4130-8

Table 13. AD4130-8, 35-Ball WLCSP

ESD Model	Withstand Threshold (V)	Class
HBM	4000	3A
FICDM	500	C2a
MM	400	C

Table 14. AD4130-8, 32-Lead LFCSP

ESD Model	Withstand Threshold (V)	Class
HBM	4000	3A
FICDM	1000	C3
MM	400	C

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

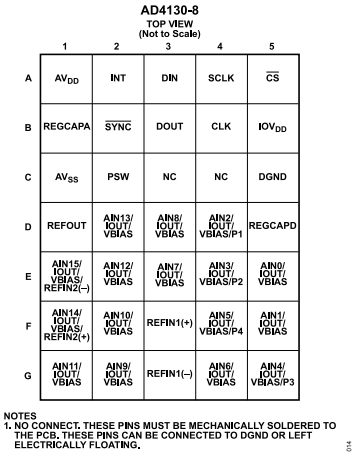


Figure 14. WLCSP Pin Configuration

Table 15. WLCSP Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
A1	AV_{DD}	S	Analog Supply Voltage, Relative to AV_{SS}. See the Power Supplies section.
A2	INT	DO	Interrupt Pin. The INT pin functions as a data ready signal by default when the FIFO is disabled. See the Data Ready Signal section. When the FIFO is enabled, the INT pin can be configured to a FIFO interrupt signal (see the FIFO Interrupt section).
A3	DIN	DI	Serial Data Logic Input. Data on the DIN pin is transferred to the control registers within the ADC, with the register selection bits (RS, Bits[5:0]) of the COMMS register identifying the appropriate register. See the Digital Interface section.
A4	SCLK	DI	Serial Clock Logic Input. This serial clock input is for data transfers to and from the ADC. The serial clock can be continuous with all data transmitted in a continuous train of pulses. Alternatively, SCLK can be a gated clock with the information transmitting to or from the ADC in smaller batches of data. See the Digital Interface section.
A5	$\overline{CS}$	DI	Chip Select Active Low Logic Input. Use $\overline{CS}$ to select the ADC in systems with more than one device on the serial bus, or as a frame synchronization signal in communicating with the device. $\overline{CS}$ can be hardwired low if the SPI diagnostics are unused, allowing the ADC to operate in 3-wire mode with SCLK, DIN, and DOUT interfacing with the device. See the Digital Interface section.
B1	REGCAPA	S	Analog LDO Regulator Output. Decouple the REGCAPA pin to AV_{SS} with a 0.1 µF capacitor. It is not recommended to connect any additional load to the REGCAPA pin. See the Internal LDOs section.
B2	$\overline{SYNC}$	DI	Synchronization Logic Input. The $\overline{SYNC}$ pin is a logic input that allows synchronization of the digital filters and analog modulators when using multiple AD4130-8 devices. See the System Synchronization section. The $\overline{SYNC}$ pin can also be used to clear the FIFO. See the Clearing the FIFO section.
B3	DOUT (WLCSP)	DO	Serial Data Logic Output. The DOUT pin functions as a serial data output pin to readback the content of any register with read access. See the Digital Interface section.
B4	CLK	DI/O	Clock Input and Clock Logic Output. The internal clock can be made available at this pin. Alternatively, the internal clock can be disabled, and the ADC can be driven by an external clock. See the ADC Master Clock section. The CLK pin can also be used as the interrupt source for the data ready signal or FIFO interrupt (see the Data Ready Signal section and FIFO Interrupt section). If not in use, tie the CLK pin to DGND.
B5	IOV_{DD}	S	Serial Interface Supply Voltage, 1.65 V to 3.6 V. See the Power Supplies section.
C1	AV_{SS}	S	Analog Supply Voltage Reference. The voltage on AV_{DD} is referenced to AV_{SS}. AV_{SS} is either tied to DGND or it can be taken below 0 V to provide a dual power supply to the AD4130-8. The minimum AV_{SS} is −1.8 V and the differential between AV_{DD} and AV_{SS} must be between 1.71 V and 3.6 V. See the Power Supplies section.
C2	PSW	AI	Low-Side Power Switch to AV_{SS}. See the Power-Down Switch section.
C3, C4	NC	N/A[2]	No Connect. These pins must be mechanically soldered to the PCB. These pins can be connected to DGND or left electrically floating.
C5	DGND	S	Digital/Common Ground Reference Point. See the Power Supplies section.
D1	REFOUT	AO	Internal Reference Output. The buffered output of the internal voltage reference is available on the REFOUT pin. A 1 nF capacitor is required on the REFOUT pin when the internal reference is active. See the ADC Reference section.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 15. WLCSP Pin Function Descriptions (Continued)

Pin No.	Mnemonic	Type[1]	Description
D2	AIN13/IOUT/VBIAS	AI/O	Analog Input 13 (AIN13) (Default)/Output of Internal Excitation Current Source/Bias Voltage. Output of Internal Excitation Current Source (IOUT). The internal programmable excitation current source can be made available at the IOUT pin. Either IOUT1 or IOUT0 can be switched to this output. Bias Voltage (VBIAS). A bias voltage midway between the analog power supply rails can be generated at the VBIAS pin.
D3	AIN8/IOUT/VBIAS	AI/O	Analog Input 8 (AIN8) (Default)/Output of Internal Excitation Current Source/Bias Voltage. Output of Internal Excitation Current Source (IOUT). The internal programmable excitation current source can be made available at the IOUT pin. Either IOUT1 or IOUT0 can be switched to this output. Bias Voltage (VBIAS). A bias voltage midway between the analog power supply rails can be generated at the VBIAS pin.
D4	AIN2/IOUT/VBIAS/P1	AI/O	Analog Input 2 (AIN2) (Default)/Output of Internal Excitation Current Source/Bias Voltage/General Purpose Output 1. Output of Internal Excitation Current Source (IOUT). The internal programmable excitation current source can be made available at the IOUT pin. Either IOUT1 or IOUT0 can be switched to this output. Bias Voltage (VBIAS). A bias voltage midway between the analog power supply rails can be generated at the VBIAS pin. General-Purpose Output 1 (P1). The P1 pin can be used as a general-purpose output, referenced between AV_{SS} and AV_{DD}. When AV_{SS} is tied to DGND and IOV_{DD} is tied to AV_{DD}, the P1 pin can operate like a digital output.
D5	REGCAPD	S	Digital LDO Regulator Output. Decouple the REGCAPD pin to DGND with a 0.1 µF capacitor. It is not recommended to connect any additional load to the REGCAPD pin. See the Internal LDOs section.
E1	AIN15/IOUT/ VBIAS/ REFIN2(−)	AI/O	Analog Input 15 (AIN15) (Default)/Output of Internal Excitation Current Source/Bias Voltage/Negative Reference Input. Output of Internal Excitation Current Source (IOUT). The internal programmable excitation current source can be made available at the IOUT pin. Either IOUT1 or IOUT0 can be switched to this output. Bias Voltage (VBIAS). A bias voltage midway between the analog power supply rails can be generated at the VBIAS pin. Negative Reference Input (REFIN2(−)). The REFIN2(−) pin can be anywhere between AV_{SS} and AV_{DD} – 0.5 V.
E2	AIN12/IOUT/VBIAS	AI/O	Analog Input 12 (AIN12) (Default)/Output of Internal Excitation Current Source/Bias Voltage. Output of Internal Excitation Current Source (IOUT). The internal programmable excitation current source can be made available at the IOUT pin. Either IOUT1 or IOUT0 can be switched to this output. Bias Voltage (VBIAS). A bias voltage midway between the analog power supply rails can be generated at the VBIAS pin.
E3	AIN7/IOUT/VBIAS	AI/O	Analog Input 7 (AIN7) (Default)/Output of Internal Excitation Current Source/Bias Voltage. Output of Internal Excitation Current Source (IOUT). The internal programmable excitation current source can be made available at the IOUT pin. Either IOUT1 or IOUT0 can be switched to this output. Bias Voltage (VBIAS). A bias voltage midway between the analog power supply rails can be generated at the VBIAS pin.
E4	AIN3/IOUT/VBIAS/P2	AI/O	Analog Input 3 (AIN3) (Default)/Output of Internal Excitation Current Source/Bias Voltage/General Purpose Output 2. Output of Internal Excitation Current Source (IOUT). The internal programmable excitation current source can be made available at the IOUT pin. Either IOUT1 or IOUT0 can be switched to this output. Bias Voltage (VBIAS). A bias voltage midway between the analog power supply rails can be generated at the VBIAS pin. General-Purpose Output 2 (P2). The P2 pin can be used as a general-purpose output, referenced between AV_{SS} and AV_{DD}. When AV_{SS} is tied to DGND and IOV_{DD} is tied to AV_{DD}, the P2 pin can operate like a digital output.
E5	AIN0/IOUT/VBIAS	AI/O	Analog Input 0 (AIN0) (Default)/Output of Internal Excitation Current Source/Bias Voltage. Output of Internal Excitation Current Source (IOUT). The internal programmable excitation current source can be made available at the IOUT pin. Either IOUT1 or IOUT0 can be switched to this output. Bias Voltage (VBIAS). A bias voltage midway between the analog power supply rails can be generated at the VBIAS pin.
F1	AIN14/IOUT/ VBIAS/ REFIN2(+)	AI/O	Analog Input 14 (AIN14) (Default)/Output of Internal Excitation Current Source/Bias Voltage/Positive Reference Input.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 15. WLCSP Pin Function Descriptions (Continued)

Pin No.	Mnemonic	Type[1]	Description
			Output of Internal Excitation Current Source (IOUT). The internal programmable excitation current source can be made available at the IOUT pin. Either IOUT1 or IOUT0 can be switched to this output. Bias Voltage (VBIAS). A bias voltage midway between the analog power supply rails can be generated at the VBIAS pin. Positive Reference Input (REFIN2(+)). An external reference can be applied between REFIN2(+) and REFIN2(−). REFIN2(+) can be anywhere between AV_{DD} and AV_{SS} + 0.5 V. The nominal reference voltage (REFIN2(+) to REFIN2(−)) is 2.5 V, but the device functions with a reference from 0.5 V to AV_{DD}.
F2	AIN10/IOUT/VBIAS	AI/O	Analog Input 10 (AIN10) (Default)/Output of Internal Excitation Current Source/Bias Voltage. Output of Internal Excitation Current Source (IOUT). The internal programmable excitation current source can be made available at the IOUT pin. Either IOUT1 or IOUT0 can be switched to this output. Bias Voltage (VBIAS). A bias voltage midway between the analog power supply rails can be generated at the VBIAS pin.
F3	REFIN1(+)	AI	Positive Reference Input. An external reference can be applied between REFIN1(+) and REFIN1(−). The REFIN1(+) pin can be anywhere between AV_{DD} and AV_{SS} + 0.5 V. The device functions with a reference from 0.5 V to AV_{DD}. See the ADC Reference section.
F4	AIN5/IOUT/VBIAS/P4	AI/O	Analog Input 5 (AIN5) (Default)/Output of Internal Excitation Current Source/Bias Voltage/General-Purpose Output 4. Output of Internal Excitation Current Source (IOUT). The internal programmable excitation current source can be made available at the IOUT pin. Either IOUT1 or IOUT0 can be switched to this output. Bias Voltage (VBIAS). A bias voltage midway between the analog power supply rails can be generated at the VBIAS pin. General-Purpose Output 4 (P4). The P4 pin can be used as a general-purpose output, referenced between AV_{SS} and AV_{DD}. When AV_{SS} is tied to DGND and IOV_{DD} is tied to AV_{DD}, the P4 pin can operate like a digital output.
F5	AIN1/IOUT/VBIAS	AI/O	Analog Input 1 (AIN1) (Default)/Output of Internal Excitation Current Source/Bias Voltage. Output of Internal Excitation Current Source (IOUT). The internal programmable excitation current source can be made available at the IOUT pin. Either IOUT1 or IOUT0 can be switched to this output. Bias Voltage (VBIAS). A bias voltage midway between the analog power supply rails can be generated at the VBIAS pin.
G1	AIN11/IOUT/VBIAS	AI/O	Analog Input 11 (AIN11) (Default)/Output of Internal Excitation Current Source/Bias Voltage. Output of Internal Excitation Current Source (IOUT). The internal programmable excitation current source can be made available at the IOUT pin. Either IOUT1 or IOUT0 can be switched to this output. Bias Voltage (VBIAS). A bias voltage midway between the analog power supply rails can be generated at the VBIAS pin.
G2	AIN9/IOUT/VBIAS	AI/O	Analog Input 9 (AIN9) (Default)/Output of Internal Excitation Current Source/Bias Voltage. Output of Internal Excitation Current Source (IOUT). The internal programmable excitation current source can be made available at the IOUT pin. Either IOUT1 or IOUT0 can be switched to this output. Bias Voltage (VBIAS). A bias voltage midway between the analog power supply rails can be generated at the VBIAS pin.
G3	REFIN1(−)	AI	Negative Reference Input. The REFIN1(−) pin can be anywhere between AV_{SS} and AV_{DD} − 0.5 V. See the ADC Reference section.
G4	AIN6/IOUT/VBIAS	AI/O	Analog Input 6 (AIN6) (Default)/Output of Internal Excitation Current Source/Bias Voltage. Output of Internal Excitation Current Source (IOUT). The internal programmable excitation current source can be made available at the IOUT pin. Either IOUT1 or IOUT0 can be switched to this output. Bias Voltage (VBIAS). A bias voltage midway between the analog power supply rails can be generated at the VBIAS pin.
G5	AIN4/IOUT/VBIAS/P3	AI/O	Analog Input 4 (AIN4) (Default)/Output of Internal Excitation Current Source/Bias Voltage/General Purpose Output 3. Output of Internal Excitation Current Source (IOUT). The internal programmable excitation current source can be made available at the IOUT pin. Either IOUT1 or IOUT0 can be switched to this output. Bias Voltage (VBIAS). A bias voltage midway between the analog power supply rails can be generated at the VBIAS pin.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 15. WLCSP Pin Function Descriptions (Continued)

Pin No.	Mnemonic	Type[1]	Description
			General-Purpose Output 3 (P3). The P3 pin can be used as a general-purpose output, referenced between AV_{SS} and AV_{DD}. When AV_{SS} is tied to DGND and IOV_{DD} is tied to AV_{DD}, the P3 pin can operate like a digital output.

[1] AO is analog output, S is supply, AI is analog input, AI/O is analog input or output, DI is digital input, DO is digital output, and DI/O is digital input or output.

[2] N/A means not applicable.

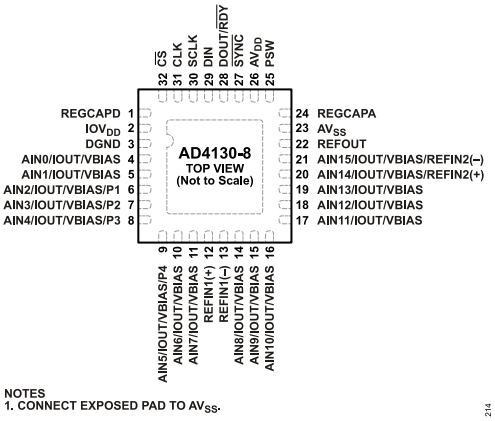


Figure 15. LFCSP Pin Configuration

Table 16. LFCSP Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1	REGCAPD	S	Digital LDO Regulator Output. Decouple the REGCAPD pin to DGND with a 0.1 µF capacitor. It is not recommended to connect any additional load to the REGCAPD pin. See the Internal LDOs section.
2	IOV_{DD}	S	Serial Interface Supply Voltage, 1.65 V to 3.6 V. See the Power Supplies section.
3	DGND	S	Digital/Common Ground Reference Point. See the Power Supplies section.
4	AIN0/IOUT/VBIAS	AI/O	Analog Input 0 (AIN0) (Default)/Output of Internal Excitation Current Source/Bias Voltage. Output of Internal Excitation Current Source (IOUT). The internal programmable excitation current source can be made available at the IOUT pin. Either IOUT1 or IOUT0 can be switched to this output. Bias Voltage (VBIAS). A bias voltage midway between the analog power supply rails can be generated at the VBIAS pin.
5	AIN1/IOUT/VBIAS	AI/O	Analog Input 1 (AIN1) (Default)/Output of Internal Excitation Current Source/Bias Voltage. Output of Internal Excitation Current Source (IOUT). The internal programmable excitation current source can be made available at the IOUT pin. Either IOUT1 or IOUT0 can be switched to this output. Bias Voltage (VBIAS). A bias voltage midway between the analog power supply rails can be generated at the VBIAS pin.
6	AIN2/IOUT/VBIAS/P1	AI/O	Analog Input 2 (AIN2) (Default)/Output of Internal Excitation Current Source/Bias Voltage/General Purpose Output 1. Output of Internal Excitation Current Source (IOUT). The internal programmable excitation current source can be made available at the IOUT pin. Either IOUT1 or IOUT0 can be switched to this output. Bias Voltage (VBIAS). A bias voltage midway between the analog power supply rails can be generated at the VBIAS pin. General-Purpose Output 1 (P1). The P1 pin can be used as a general-purpose output, referenced between AV_{SS} and AV_{DD}. When AV_{SS} is tied to DGND and IOV_{DD} is tied to AV_{DD}, the P1 pin can operate like a digital output.
7	AIN3/IOUT/VBIAS/P2	AI/O	Analog Input 3 (AIN3) (Default)/Output of Internal Excitation Current Source/Bias Voltage/General Purpose Output 2. Output of Internal Excitation Current Source (IOUT). The internal programmable excitation current source can be made available at the IOUT pin. Either IOUT1 or IOUT0 can be switched to this output. Bias Voltage (VBIAS). A bias voltage midway between the analog power supply rails can be generated at the VBIAS pin.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 16. LFCSP Pin Function Descriptions (Continued)

Pin No.	Mnemonic	Type[1]	Description
			General-Purpose Output 2 (P2). The P2 pin can be used as a general-purpose output, referenced between AV_{SS} and AV_{DD}. When AV_{SS} is tied to DGND and IOV_{DD} is tied to AV_{DD}, the P2 pin can operate like a digital output.
8	AIN4/IOUT/VBIAS/P3	AI/O	Analog Input 4 (AIN4) (Default)/Output of Internal Excitation Current Source/Bias Voltage/General Purpose Output 3. Output of Internal Excitation Current Source (IOUT). The internal programmable excitation current source can be made available at the IOUT pin. Either IOUT1 or IOUT0 can be switched to this output. Bias Voltage (VBIAS). A bias voltage midway between the analog power supply rails can be generated at the VBIAS pin. General-Purpose Output 3 (P3). The P3 pin can be used as a general-purpose output, referenced between AV_{SS} and AV_{DD}. When AV_{SS} is tied to DGND and IOV_{DD} is tied to AV_{DD}, the P3 pin can operate like a digital output.
9	AIN5/IOUT/VBIAS/P4	AI/O	Analog Input 5 (AIN5) (Default)/Output of Internal Excitation Current Source/Bias Voltage/General-Purpose Output 4. Output of Internal Excitation Current Source (IOUT). The internal programmable excitation current source can be made available at the IOUT pin. Either IOUT1 or IOUT0 can be switched to this output. Bias Voltage (VBIAS). A bias voltage midway between the analog power supply rails can be generated at the VBIAS pin. General-Purpose Output 4 (P4). The P4 pin can be used as a general-purpose output, referenced between AV_{SS} and AV_{DD}. When AV_{SS} is tied to DGND and IOV_{DD} is tied to AV_{DD}, the P4 pin can operate like a digital output.
10	AIN6/IOUT/VBIAS	AI/O	Analog Input 6 (AIN6) (Default)/Output of Internal Excitation Current Source/Bias Voltage. Output of Internal Excitation Current Source (IOUT). The internal programmable excitation current source can be made available at the IOUT pin. Either IOUT1 or IOUT0 can be switched to this output. Bias Voltage (VBIAS). A bias voltage midway between the analog power supply rails can be generated at the VBIAS pin.
11	AIN7/IOUT/VBIAS	AI/O	Analog Input 7 (AIN7) (Default)/Output of Internal Excitation Current Source/Bias Voltage. Output of Internal Excitation Current Source (IOUT). The internal programmable excitation current source can be made available at the IOUT pin. Either IOUT1 or IOUT0 can be switched to this output. Bias Voltage (VBIAS). A bias voltage midway between the analog power supply rails can be generated at the VBIAS pin.
12	REFIN1(+)	AI	Positive Reference Input. An external reference can be applied between REFIN1(+) and REFIN1(−). The REFIN1(+) pin can be anywhere between AV_{DD} and AV_{SS} + 0.5 V. The device functions with a reference from 0.5 V to AV_{DD}. See the ADC Reference section.
13	REFIN1(−)	AI	Negative Reference Input. The REFIN1(−) pin can be anywhere between AV_{SS} and AV_{DD} − 0.5 V. See the ADC Reference section.
14	AIN8/IOUT/VBIAS	AI/O	Analog Input 8 (AIN8) (Default)/Output of Internal Excitation Current Source/Bias Voltage. Output of Internal Excitation Current Source (IOUT). The internal programmable excitation current source can be made available at the IOUT pin. Either IOUT1 or IOUT0 can be switched to this output. Bias Voltage (VBIAS). A bias voltage midway between the analog power supply rails can be generated at the VBIAS pin.
15	AIN9/IOUT/VBIAS	AI/O	Analog Input 9 (AIN9) (Default)/Output of Internal Excitation Current Source/Bias Voltage. Output of Internal Excitation Current Source (IOUT). The internal programmable excitation current source can be made available at the IOUT pin. Either IOUT1 or IOUT0 can be switched to this output. Bias Voltage (VBIAS). A bias voltage midway between the analog power supply rails can be generated at the VBIAS pin.
16	AIN10/IOUT/VBIAS	AI/O	Analog Input 10 (AIN10) (Default)/Output of Internal Excitation Current Source/Bias Voltage. Output of Internal Excitation Current Source (IOUT). The internal programmable excitation current source can be made available at the IOUT pin. Either IOUT1 or IOUT0 can be switched to this output. Bias Voltage (VBIAS). A bias voltage midway between the analog power supply rails can be generated at the VBIAS pin.
17	AIN11/IOUT/VBIAS	AI/O	Analog Input 11 (AIN11) (Default)/Output of Internal Excitation Current Source/Bias Voltage. Output of Internal Excitation Current Source (IOUT). The internal programmable excitation current source can be made available at the IOUT pin. Either IOUT1 or IOUT0 can be switched to this output.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 16. LFCSP Pin Function Descriptions (Continued)

Pin No.	Mnemonic	Type[1]	Description
			Bias Voltage (VBIAS). A bias voltage midway between the analog power supply rails can be generated at the VBIAS pin.
18	AIN12/IOUT/VBIAS	AI/O	Analog Input 12 (AIN12) (Default)/Output of Internal Excitation Current Source/Bias Voltage. Output of Internal Excitation Current Source (IOUT). The internal programmable excitation current source can be made available at the IOUT pin. Either IOUT1 or IOUT0 can be switched to this output. Bias Voltage (VBIAS). A bias voltage midway between the analog power supply rails can be generated at the VBIAS pin.
19	AIN13/IOUT/VBIAS	AI/O	Analog Input 13 (AIN13) (Default)/Output of Internal Excitation Current Source/Bias Voltage. Output of Internal Excitation Current Source (IOUT). The internal programmable excitation current source can be made available at the IOUT pin. Either IOUT1 or IOUT0 can be switched to this output. Bias Voltage (VBIAS). A bias voltage midway between the analog power supply rails can be generated at the VBIAS pin.
20	AIN14/IOUT/ VBIAS/ REFIN2(+)	AI/O	Analog Input 14 (AIN14) (Default)/Output of Internal Excitation Current Source/Bias Voltage/Positive Reference Input. Output of Internal Excitation Current Source (IOUT). The internal programmable excitation current source can be made available at the IOUT pin. Either IOUT1 or IOUT0 can be switched to this output. Bias Voltage (VBIAS). A bias voltage midway between the analog power supply rails can be generated at the VBIAS pin. Positive Reference Input (REFIN2(+)). An external reference can be applied between REFIN2(+) and REFIN2(−). REFIN2(+) can be anywhere between AV_{DD} and AV_{SS} + 0.5 V. The nominal reference voltage (REFIN2(+) to REFIN2(−)) is 2.5 V, but the device functions with a reference from 0.5 V to AV_{DD}.
21	AIN15/IOUT/ VBIAS/ REFIN2(−)	AI/O	Analog Input 15 (AIN15) (Default)/Output of Internal Excitation Current Source/Bias Voltage/Negative Reference Input. Output of Internal Excitation Current Source (IOUT). The internal programmable excitation current source can be made available at the IOUT pin. Either IOUT1 or IOUT0 can be switched to this output. Bias Voltage (VBIAS). A bias voltage midway between the analog power supply rails can be generated at the VBIAS pin. Negative Reference Input (REFIN2(−)). The REFIN2(−) pin can be anywhere between AV_{SS} and AV_{DD} – 0.5 V.
22	REFOUT	AO	Internal Reference Output. The buffered output of the internal voltage reference is available on the REFOUT pin. A 1 nF capacitor is required on the REFOUT pin when the internal reference is active. See the ADC Reference section.
23	AV_{SS}	S	Analog Supply Voltage Reference. The voltage on AV_{DD} is referenced to AV_{SS}. AV_{SS} is either tied to DGND or it can be taken below 0 V to provide a dual power supply to the AD4130-8. The minimum AV_{SS} is −1.8 V and the differential between AV_{DD} and AV_{SS} must be between 1.71 V and 3.6 V. See the Power Supplies section.
24	REGCAPA	S	Analog LDO Regulator Output. Decouple the REGCAPA pin to AV_{SS} with a 0.1 µF capacitor. It is not recommended to connect any additional load to the REGCAPA pin. See the Internal LDOs section.
25	PSW	AI	Low-Side Power Switch to AV_{SS}. See the Power-Down Switch section.
26	AV_{DD}	S	Analog Supply Voltage, Relative to AV_{SS}. See the Power Supplies section.
27	$\overline{SYNC}$	DI	Synchronization Logic Input. The $\overline{SYNC}$ pin is a logic input that allows synchronization of the digital filters and analog modulators when using multiple AD4130-8 devices. See the System Synchronization section. The $\overline{SYNC}$ pin can also be used to clear the FIFO. See the Clearing the FIFO section.
28	DOUT/$\overline{RDY}$ (LFCSP)	DO	Serial Data Logic Output. The DOUT/$\overline{RDY}$ pin functions as a serial data output pin to readback the content of any register with read access. See the Digital Interface section.
29	DIN	DI	Serial Data Logic Input. Data on the DIN pin is transferred to the control registers within the ADC, with the register selection bits (RS, Bits[5:0]) of the COMMS register identifying the appropriate register. See the Digital Interface section.
30	SCLK	DI	Serial Clock Logic Input. This serial clock input is for data transfers to and from the ADC. The serial clock can be continuous with all data transmitted in a continuous train of pulses. Alternatively, SCLK can be a gated clock with the information transmitting to or from the ADC in smaller batches of data. See the Digital Interface section.
31	CLK	DI/O	Clock Input and Clock Logic Output. The internal clock can be made available at this pin. Alternatively, the internal clock can be disabled, and the ADC can be driven by an external clock. See the ADC Master Clock section. The CLK pin can also be used as the interrupt source for the data ready signal or FIFO interrupt (see the Data Ready Signal section and FIFO Interrupt section). If not in use, tie the CLK pin to DGND.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 16. LFCSP Pin Function Descriptions (Continued)

Pin No.	Mnemonic	Type[1]	Description
32	$\overline{CS}$	DI	Chip Select Active Low Logic Input. Use $\overline{CS}$ to select the ADC in systems with more than one device on the serial bus, or as a frame synchronization signal in communicating with the device. $\overline{CS}$ can be hardwired low if the SPI diagnostics are unused, allowing the ADC to operate in 3-wire mode with SCLK, DIN, and DOUT interfacing with the device. See the Digital Interface section.

[1] AO is analog output, S is supply, AI is analog input, AI/O is analog input or output, DI is digital input, DO is digital output, and DI/O is digital input or output.

TYPICAL PERFORMANCE CHARACTERISTICS

AV_{DD} = 3.3 V, IOV_{DD} = 1.8 V, AV_{SS} = DGND = 0 V, V_{REF} = 2.5 V (internal), internal MCLK, T_A = 25°C, $sinc^3$ filter, FS = 48, gain = 1, PGA enabled, reference buffers bypassed, and decoupling, as outlined in the Recommended Decoupling section, unless otherwise noted.

OFFSET ERROR AND GAIN ERROR

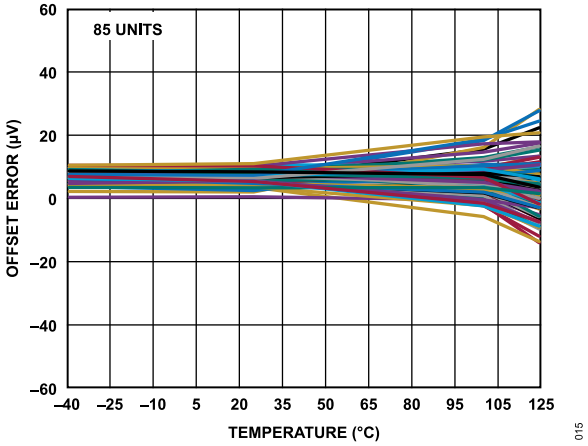


Figure 16. Offset Error vs. Temperature (Gain = 1, Before Calibration)

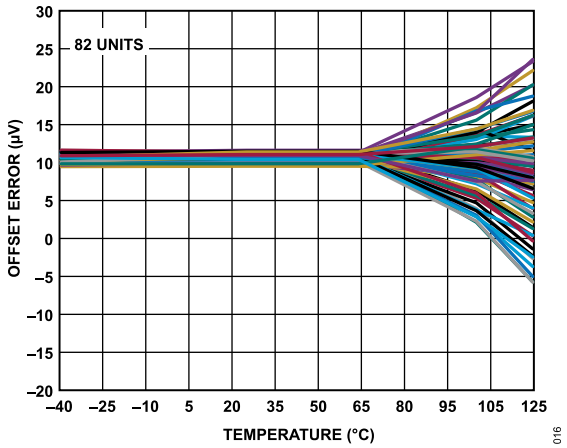


Figure 17. Offset Error vs. Temperature (Gain = 8, Before Calibration)

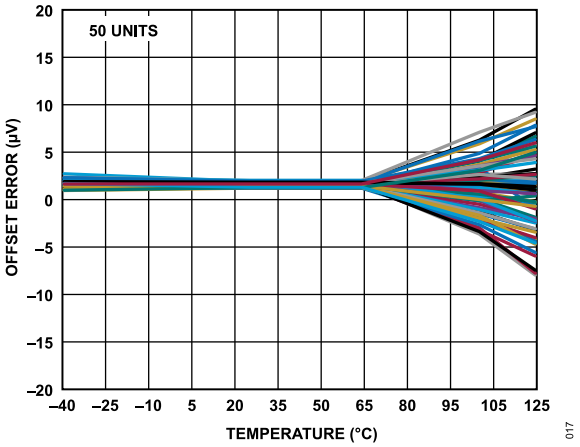


Figure 18. Offset Error vs. Temperature (Gain = 32, Before Calibration)

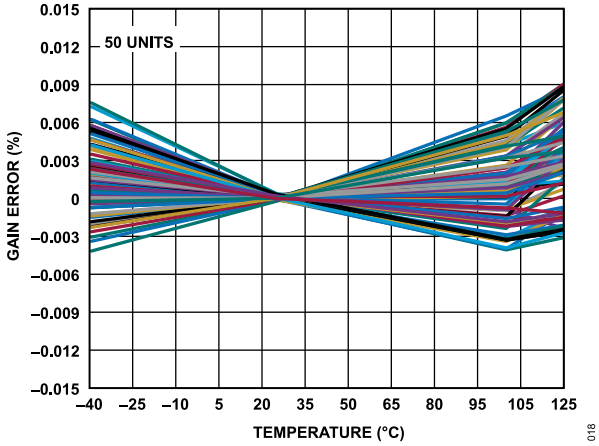


Figure 19. Gain Error vs. Temperature (Gain = 1, Factory Calibrated)

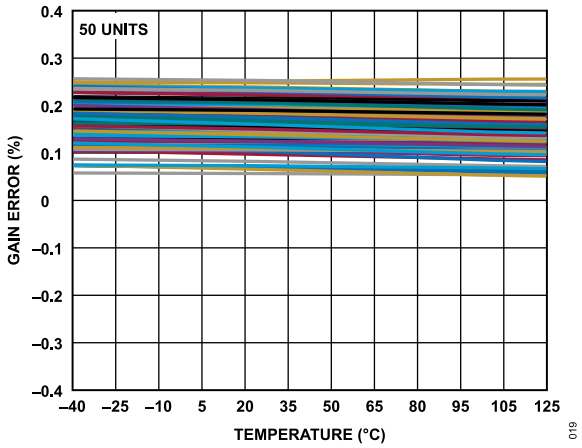


Figure 20. Gain Error vs. Temperature (Gain = 8, Before Calibration)

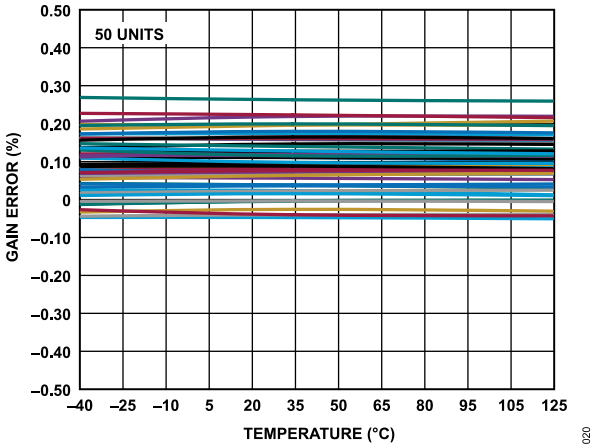


Figure 21. Gain Error vs. Temperature (Gain = 32, Before Calibration)

TYPICAL PERFORMANCE CHARACTERISTICS

INL ERROR AND OSCILLATOR

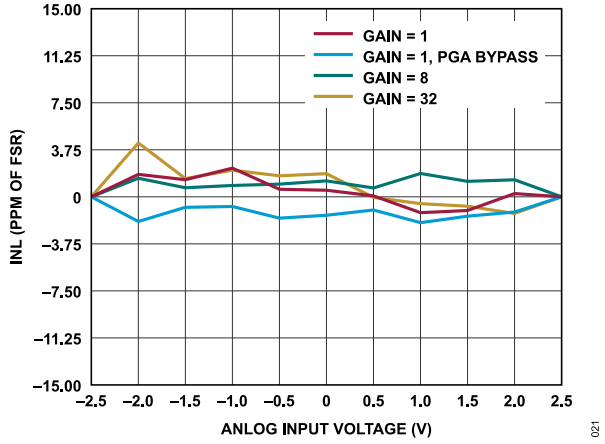


Figure 22. INL Error vs. Differential Input Amplitude for Various Gains (Sinc^3 Filter, ODR = 50 SPS, Internal 2.5 V Reference)

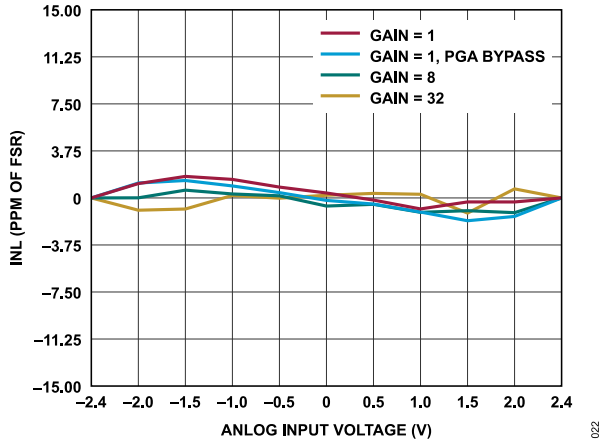


Figure 23. INL Error vs. Differential Input Amplitude for Various Gains (Sinc^3 Filter, ODR = 50 SPS, External 2.5 V Reference)

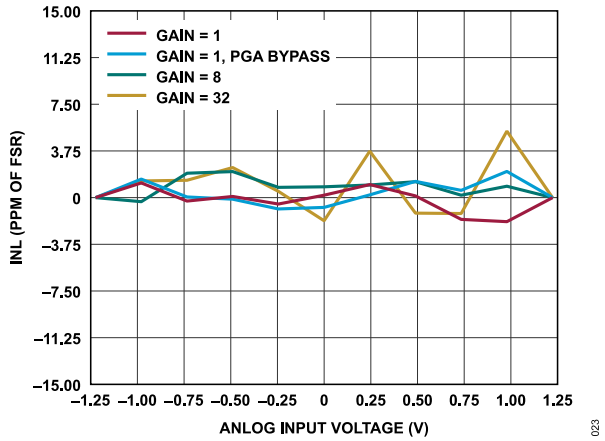


Figure 24. INL Error vs. Differential Input Amplitude for Various Gains (Sinc^3 Filter, ODR = 50 SPS, AV_{DD} = 1.8 V, Internal 1.25 V Reference)

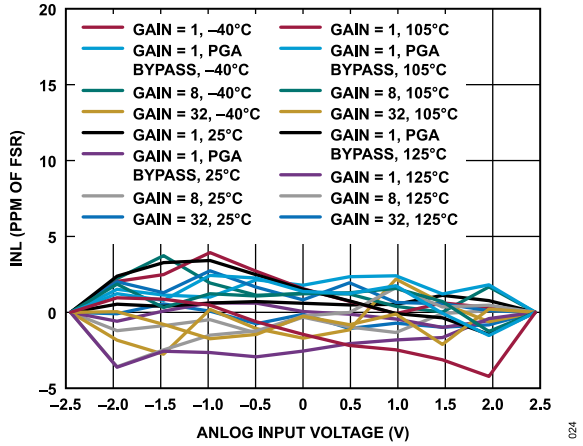


Figure 25. INL Error vs. Differential Input Amplitude for Various Gains and Temperatures (Sinc^3 Filter, ODR = 50 SPS, Internal 2.5 V Reference)

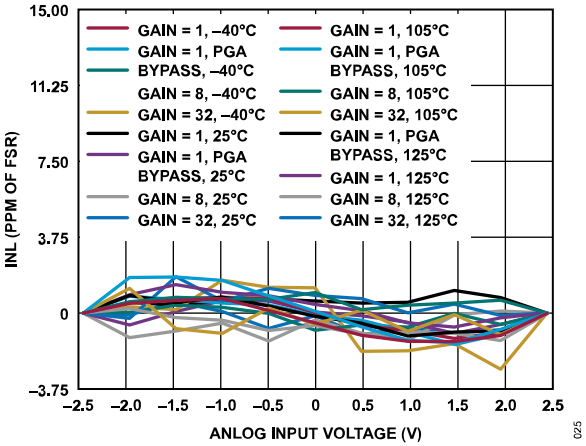


Figure 26. INL Error vs. Differential Input Amplitude for Various Gains and Temperatures (Sinc^3 Filter, ODR = 50 SPS, External 2.5 V Reference)

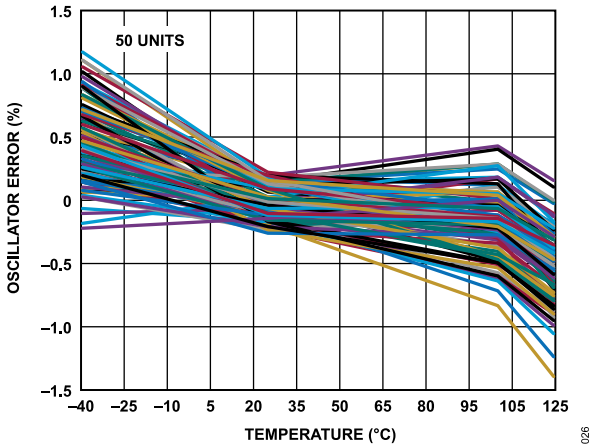


Figure 27. Internal Oscillator Error vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

NOISE

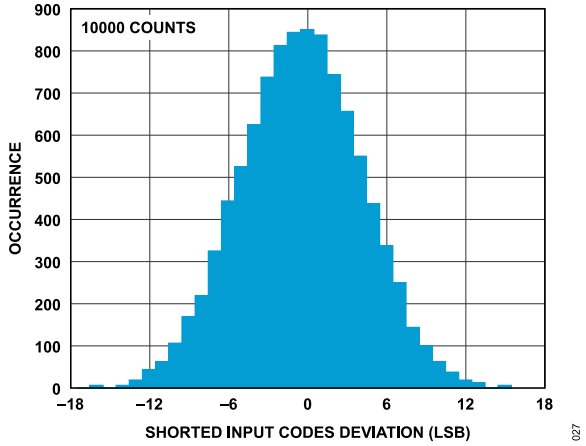


Figure 28. Noise Histogram Plot (Sinc^3 Filter, ODR = 50 SPS, Gain = 1, Internal 2.5 V Reference)

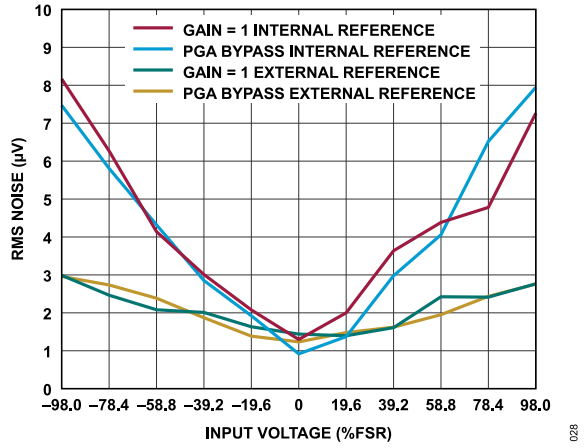


Figure 29. RMS Noise vs. Analog Input Voltage (Sinc^3 Filter, ODR = 50 SPS, Gain = 1 and Gain = 1 with PGA Bypass, 2.5 V Reference)

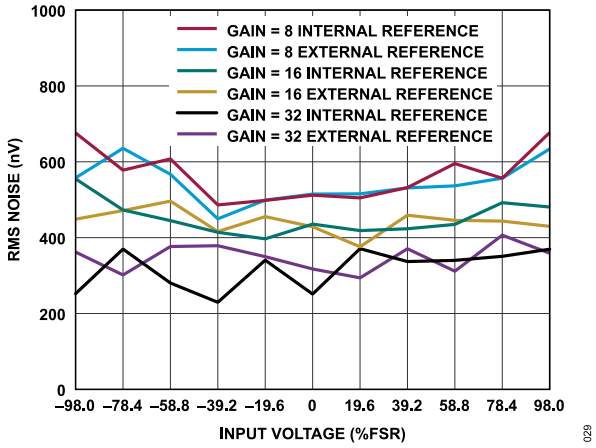


Figure 30. RMS Noise vs. Analog Input Voltage (Sinc^3 Filter, ODR = 50 SPS, Gain = 8, Gain = 16 and Gain = 32, 1.25 V Reference)

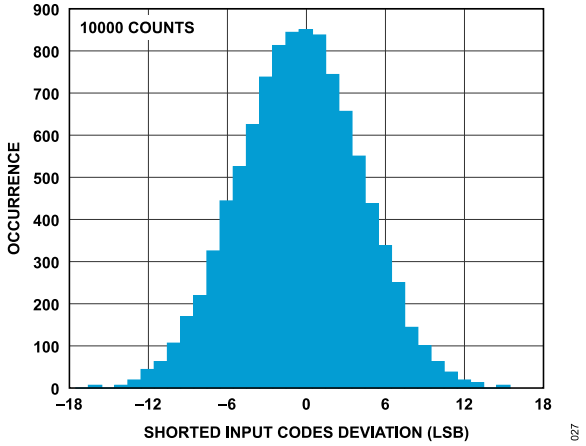


Figure 31. Noise Histogram Plot (Sinc^4 Filter, ODR = 240 SPS, Gain = 1, Internal 1.25 V Reference)

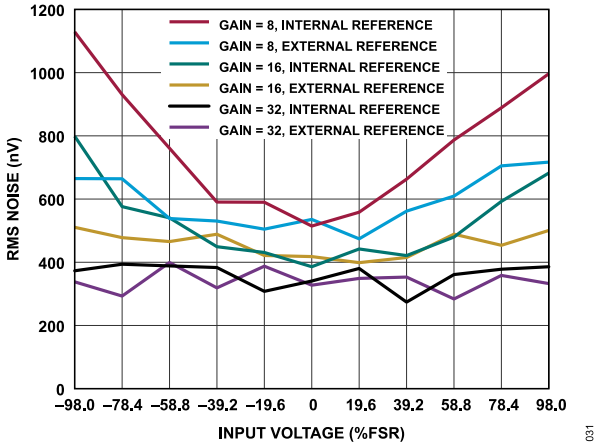


Figure 32. RMS Noise vs. Analog Input Voltage (Sinc^3 Filter, ODR = 50 SPS, Gain = 8, Gain = 16 and Gain = 32, 2.5 V Reference)

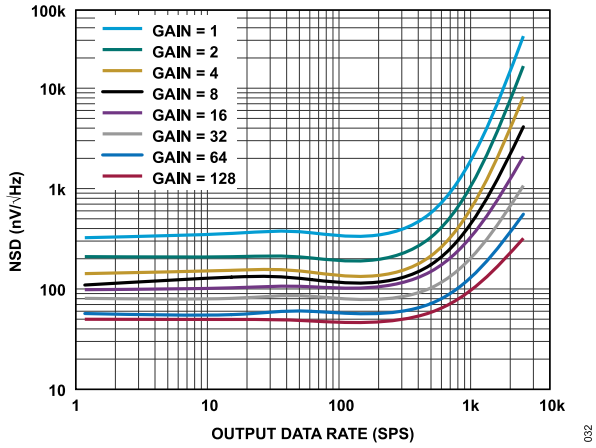


Figure 33. NSD vs. Output Data Rate for Various Gains (Sinc^3 Filter, External 2.5 V Reference)

TYPICAL PERFORMANCE CHARACTERISTICS

ANALOG INPUT CURRENTS

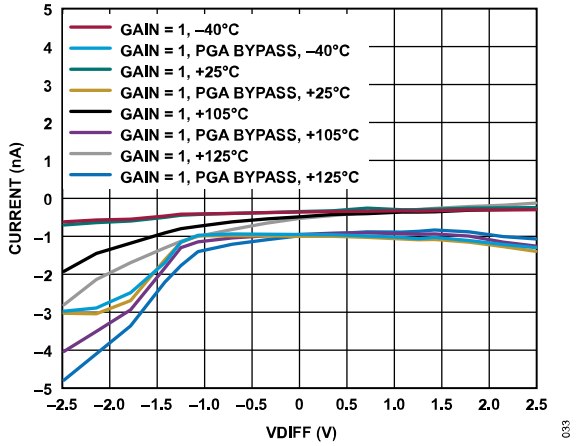


Figure 34. Absolute AINP Current vs. Differential AIN Voltage (VDIFF) for Various Temperatures (Gain = 1, VCM = $AV_{DD}/2$)

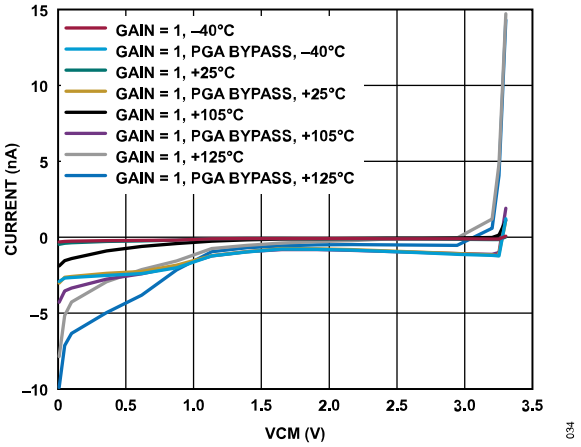


Figure 35. Absolute AINP Current vs. AIN Common-Mode Voltage (VCM) for Various Temperatures (Gain = 1, VDIFF = 0 V)

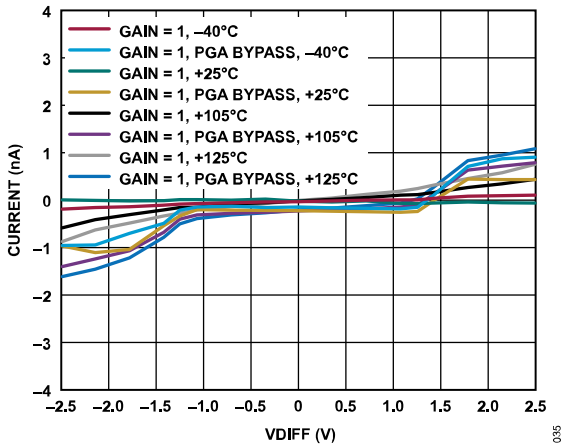


Figure 36. Differential AIN Current vs. VDIFF for Various Temperatures (Gain = 1, VCM = $AV_{DD}/2$)

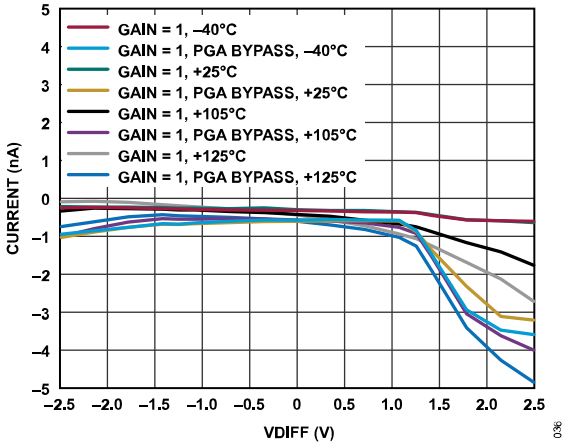


Figure 37. Absolute AINM Current vs. VDIFF for Various Temperatures (Gain = 1, VCM = $AV_{DD}/2$)

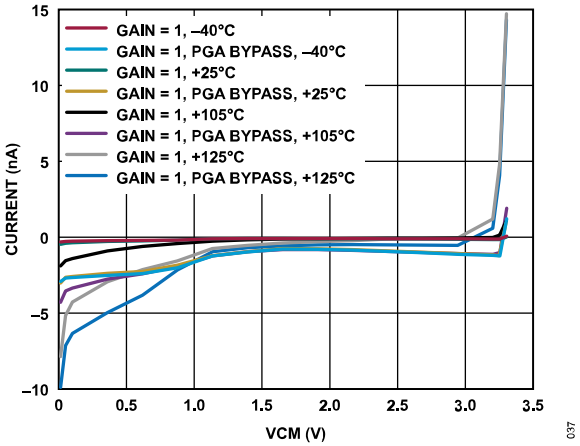


Figure 38. Absolute AINM Current vs. VCM for Various Temperatures (Gain = 1, VDIFF = 0 V)

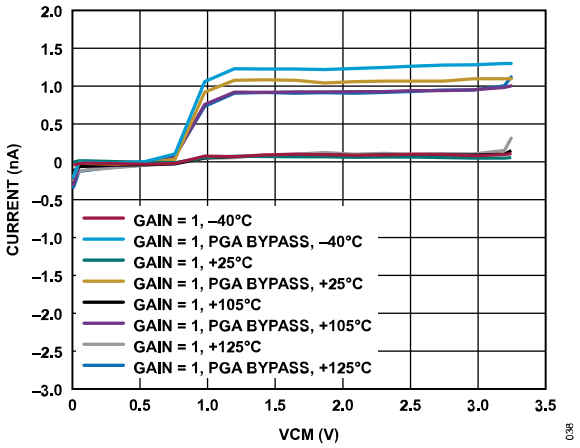


Figure 39. Differential AIN Current vs. VCM for Various Temperatures (Gain = 1, VCM = $AV_{DD}/2$)

TYPICAL PERFORMANCE CHARACTERISTICS

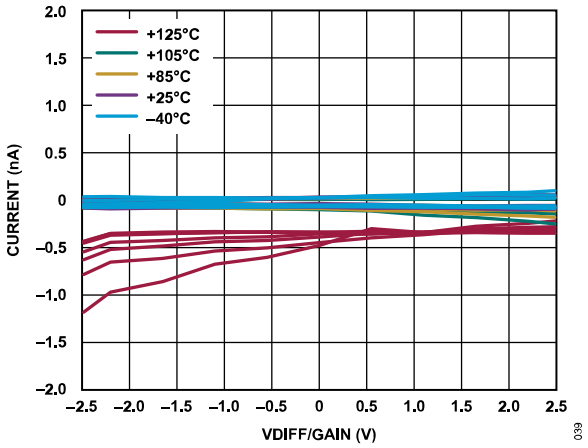


Figure 40. Absolute AINP Current vs. Normalized Differential AIN Voltage (VDIFF/Gain) for Various Temperatures (Gain = 2 to 128, VCM = $AV_{DD}/2$)

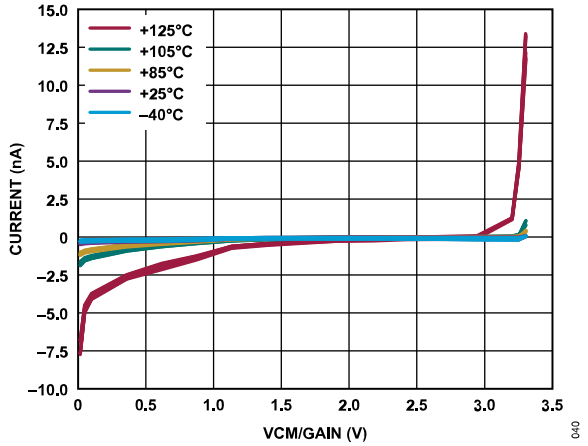


Figure 41. Absolute AINP Current vs. Normalized AIN Common-Mode Voltage (VCM/Gain) for Various Temperatures (Gain = 2 to 128, VDIFF = 0 V)

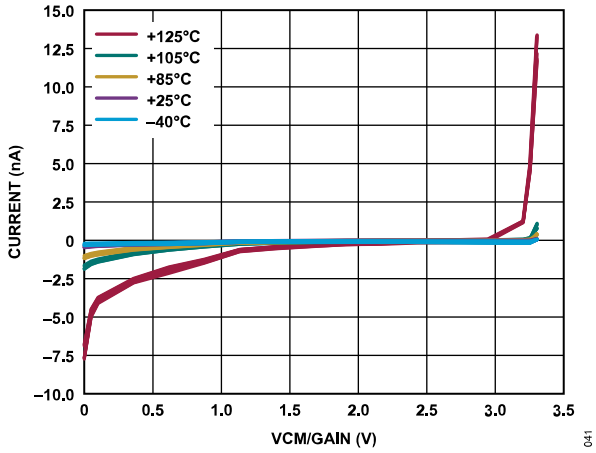


Figure 42. Differential AIN Current vs. VDIFF/Gain for Various Temperatures (Gain = 2 to 128, VCM = $AV_{DD}/2$)

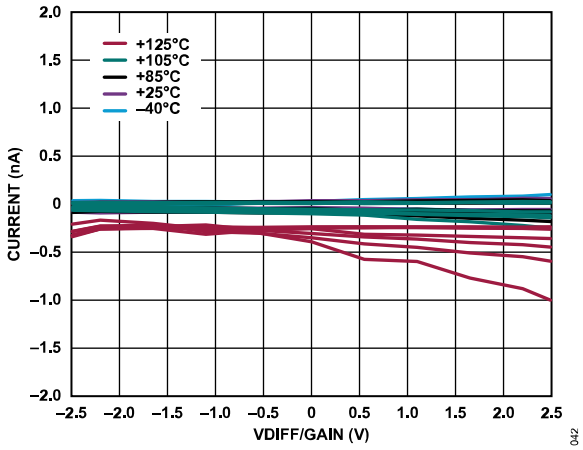


Figure 43. Absolute AINM Current vs. VDIFF/Gain for Various Temperatures (Gain = 2 to 128, VCM = $AV_{DD}/2$)

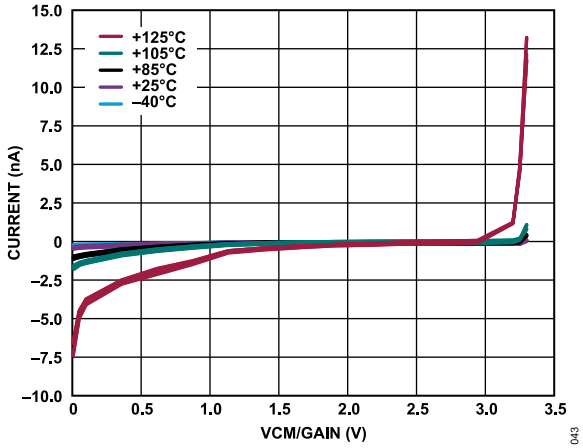


Figure 44. Absolute AINM Current vs. VCM/Gain for Various Temperatures (Gain = 2 to 128, VDIFF = 0 V)

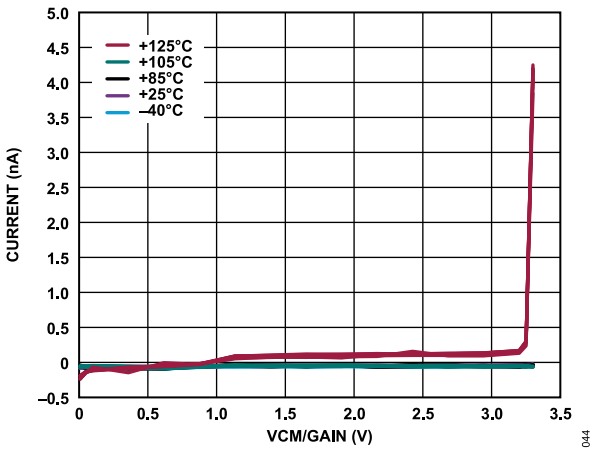


Figure 45. Differential AIN Current vs. VCM/Gain for Various Temperatures (Gain = 2 to 128, VDIFF = 0 V)

TYPICAL PERFORMANCE CHARACTERISTICS

SUPPLY CURRENTS

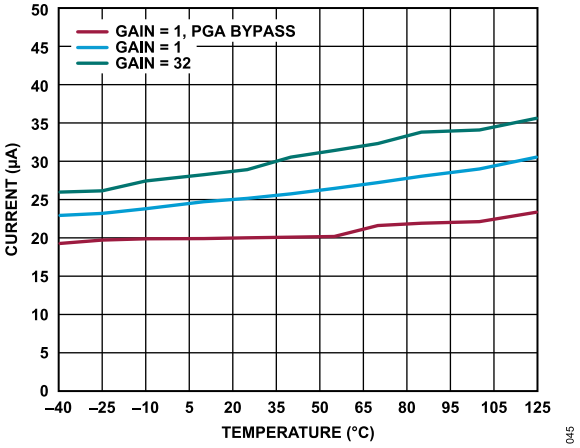


Figure 46. AV_{DD} Current vs. Temperature for Various Gains

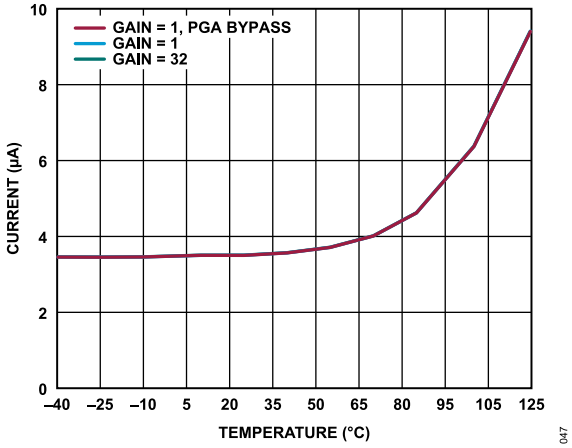


Figure 48. IOV_{DD} Current vs. Temperature

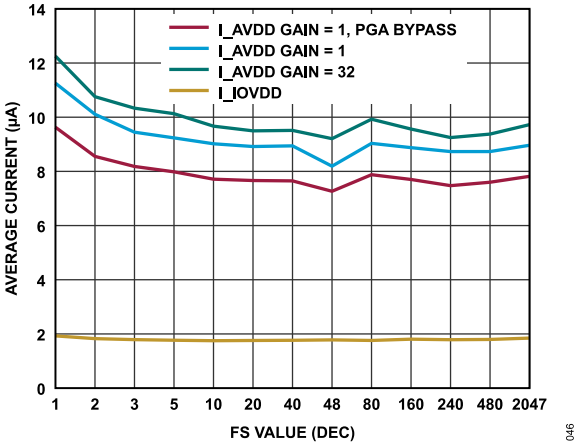


Figure 47. Duty Cycling Current Consumption (AV_{DD} and IOV_{DD}), DUTY_CYC_RATIO = 1/4 (I_AVDD is AV_{DD} Current, I_IOVDD is IOV_{DD} Current)

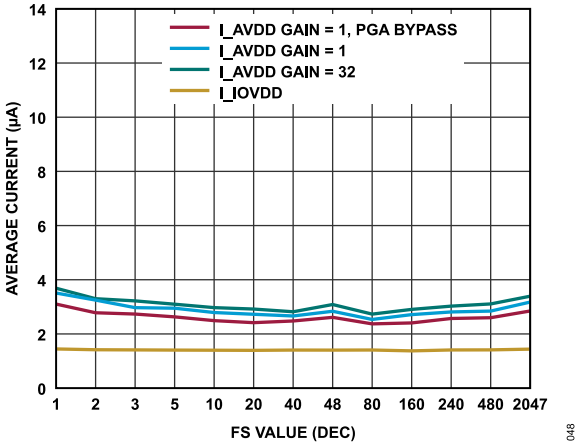


Figure 49. Duty Cycling Current Consumption (AV_{DD} and IOV_{DD}), DUTY_CYC_RATIO = 1/16

TYPICAL PERFORMANCE CHARACTERISTICS

REFERENCE INPUT CURRENTS

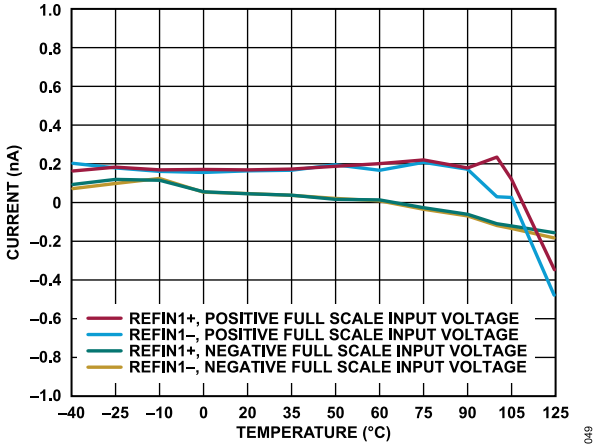


Figure 50. Reference Input Current vs. Temperature (Reference Buffer On, External 2.5 V Reference)

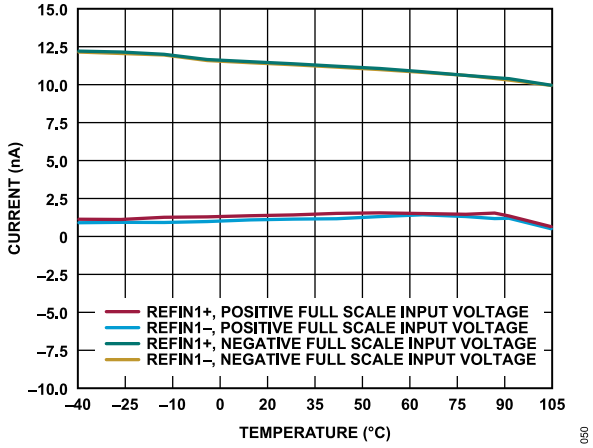


Figure 51. Reference Input Current vs. Temperature (Reference Buffer Bypass, External 2.5 V Reference)

TYPICAL PERFORMANCE CHARACTERISTICS

INTERNAL REFERENCE AND TEMPERATURE SENSOR

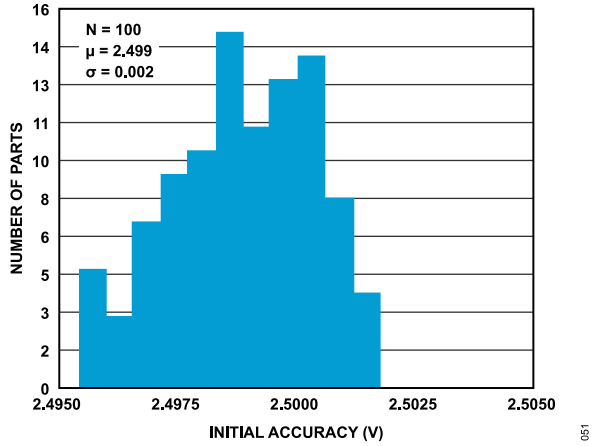


Figure 52. 2.5 V Internal Reference Voltage Histogram

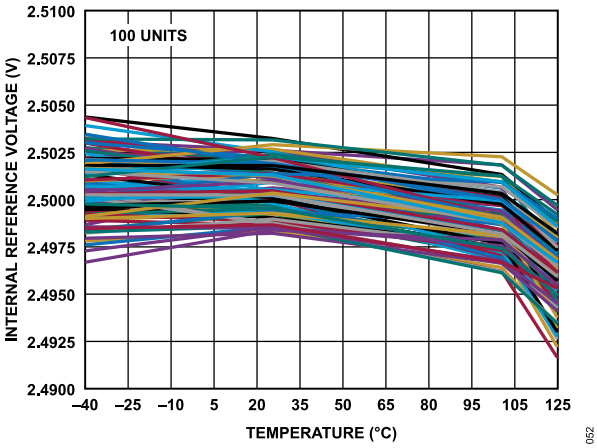


Figure 53. 2.5 V Internal Reference Voltage vs. Temperature

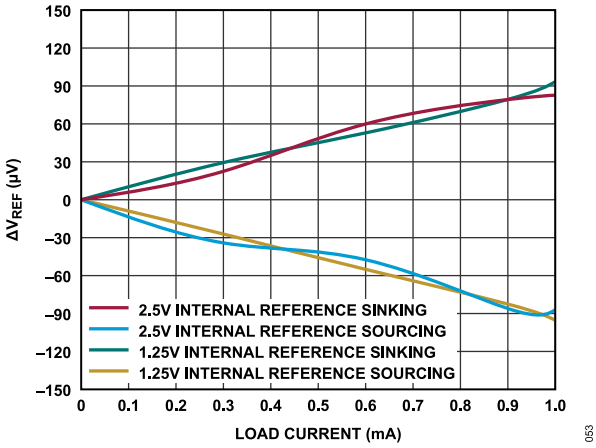


Figure 54. 1.25 V (AV_{DD} = 1.8 V) and 2.5 V (AV_{DD} = 3.3 V) Internal Reference Voltage vs. Load Current

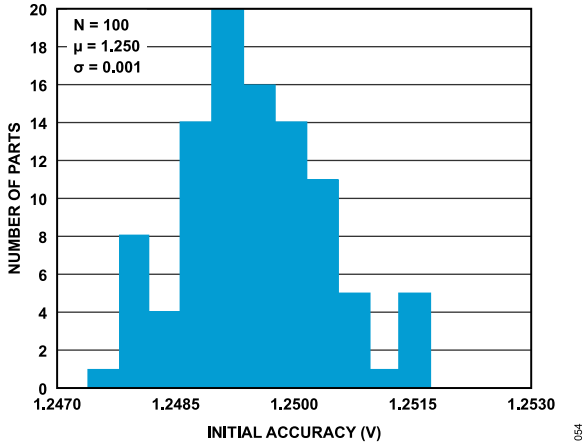


Figure 55. 1.25 V Internal Reference Voltage Histogram

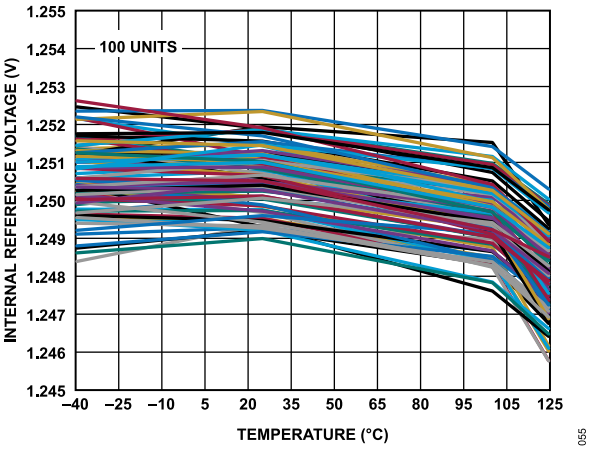


Figure 56. 1.25 V Internal Reference Voltage vs. Temperature

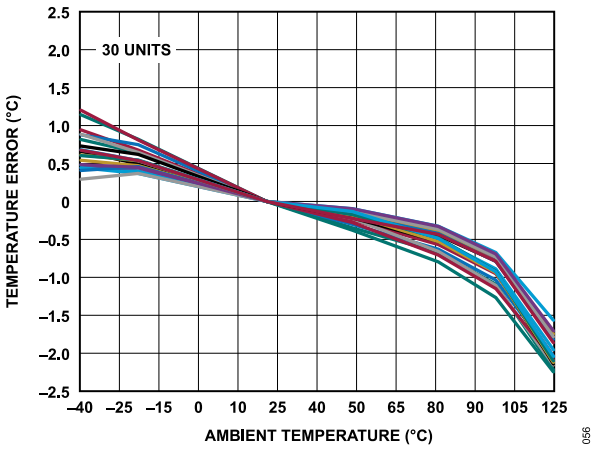


Figure 57. Temperature Sensor Error vs. Ambient Temperature after Calibration at 25°C

TYPICAL PERFORMANCE CHARACTERISTICS

EXCITATION CURRENTS

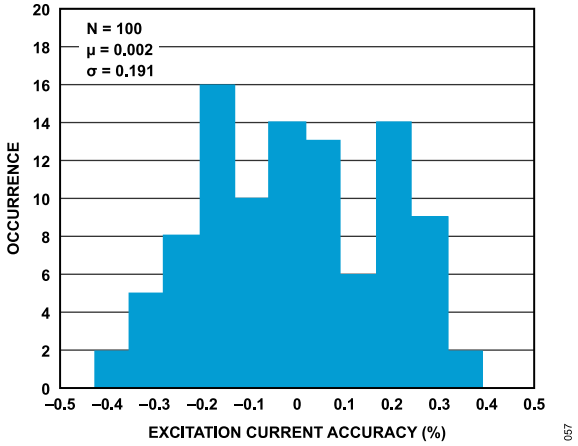


Figure 58. Excitation Current Initial Accuracy Histogram (100 μA)

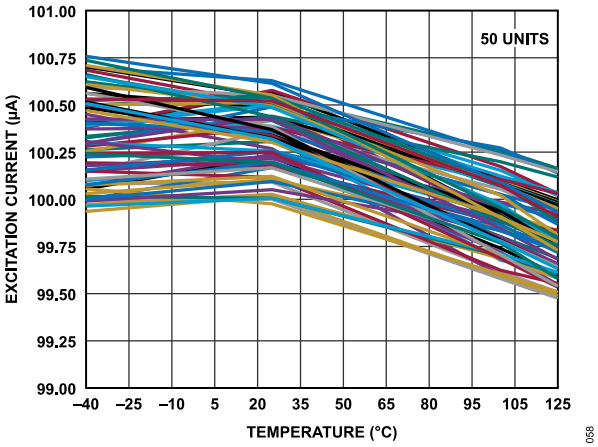


Figure 59. Excitation Current vs. Temperature (100 μA)

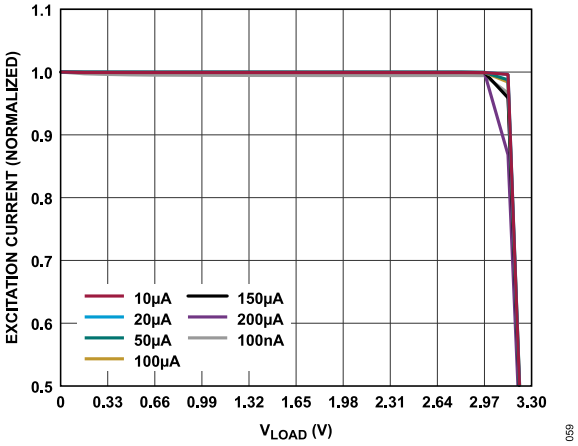


Figure 60. Output Compliance for Various IEXC Sources (AV_{DD} = 3.3 V, V_{LOAD} is Load Voltage)

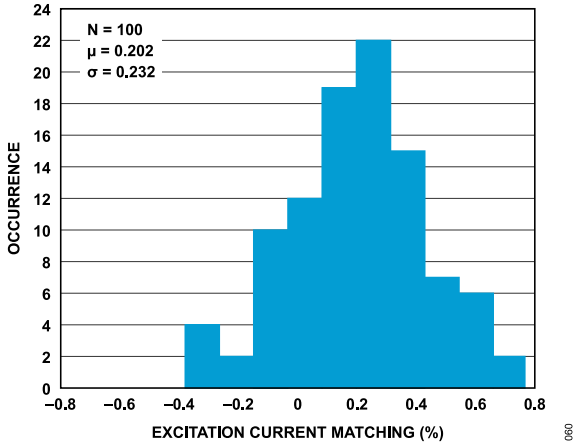


Figure 61. Excitation Current Initial Matching Histogram (100 μA)

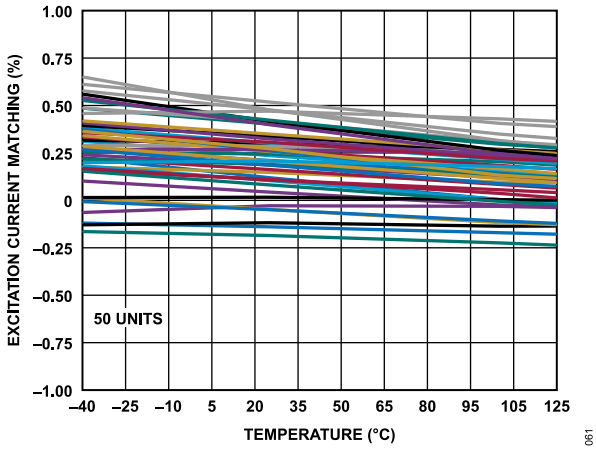


Figure 62. Excitation Current Matching vs. Temperature (100 μA)

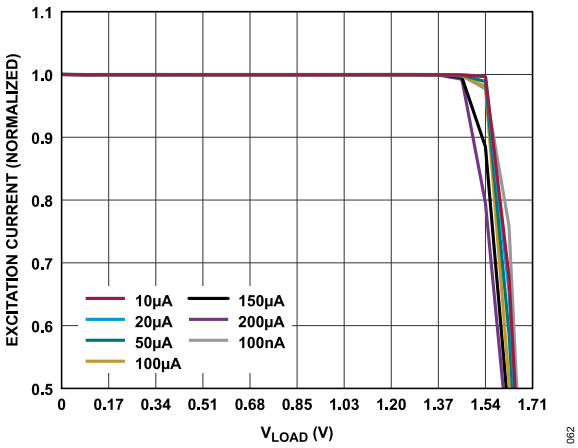


Figure 63. Output Compliance for Various IEXC Sources (AV_{DD} = 1.71 V)

TYPICAL PERFORMANCE CHARACTERISTICS

RESOLUTION

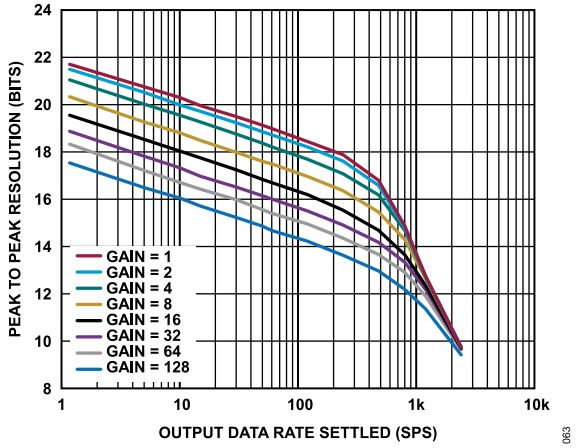


Figure 64. Peak-to-Peak Resolution vs. Output Data Rate (Settled) for Various Gains (Sinc^3 Filter)

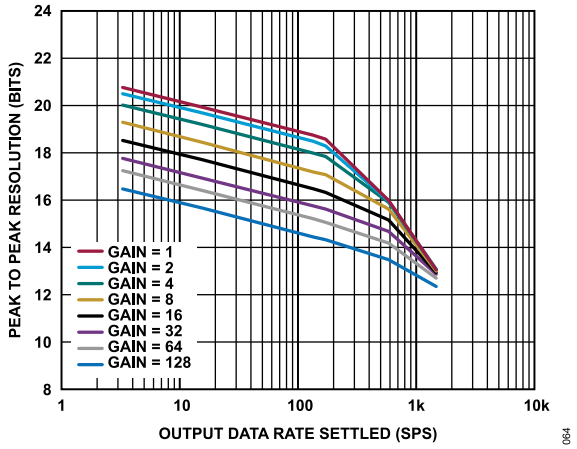


Figure 65. Peak-to-Peak Resolution vs. Output Data Rate (Settled) for Various Gains (Sinc^3 + Sinc^1 Filter)

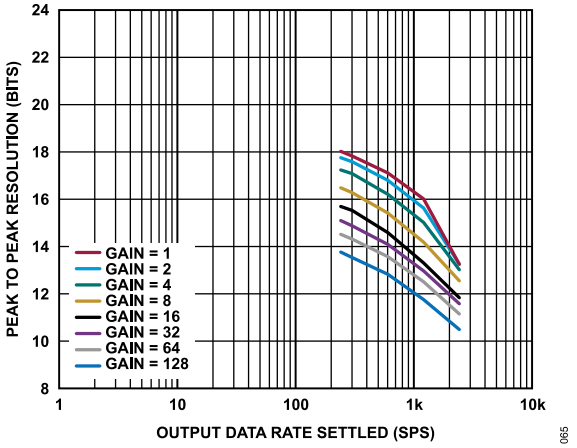


Figure 66. Peak-to-Peak Resolution vs. Output Data Rate (Settled) for Various Gains (Sinc^4 Filter)

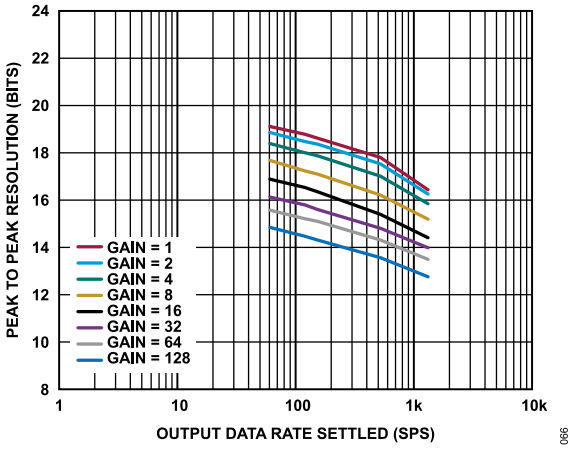


Figure 67. Peak-to-Peak Resolution vs. Output Data Rate (Settled) for Various Gains (Sinc^4 + Sinc^1 Filter)

TYPICAL PERFORMANCE CHARACTERISTICS

FFT

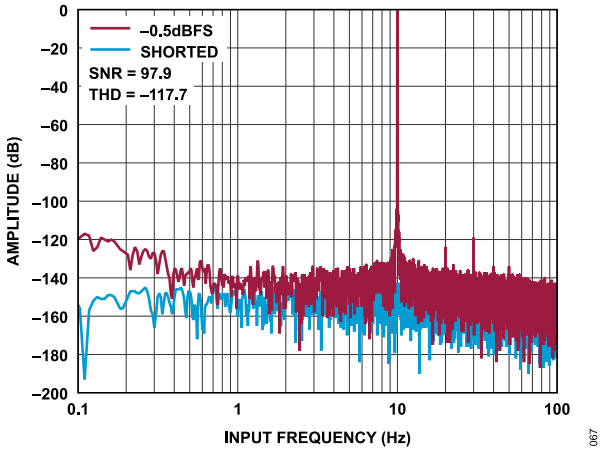


Figure 68. FFT, −0.5 dBFS vs. Shorted Inputs, 10 Hz Input Tone, Sinc^3 Filter, ODR = 240 SPS, Gain = 1, Internal Reference

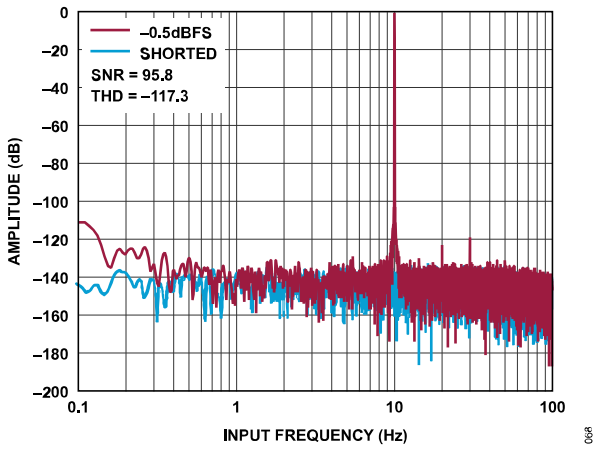


Figure 69. FFT, −0.5 dBFS vs. Shorted Inputs, 10 Hz Input Tone, Sinc^3 Filter, ODR = 240 SPS, Gain = 1, External Reference

TERMINOLOGY

ANALOG INPUT

AINP

AINP refers to the positive analog input.

AINM

AINM refers to the negative analog input.

Input Span

The input span specification defines the minimum and maximum input voltages from zero to full scale that the analog input can accept and still calibrate gain accurately.

ADC

Integral Nonlinearity (INL) Error

INL is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale (not to be confused with bipolar zero), a point 0.5 LSB below the first code transition (000 ... 000 to 000 ... 001), and full scale, a point 0.5 LSB above the last code transition (111 ... 110 to 111 ... 111). The error is expressed in ppm of the full-scale range.

Offset Error

Offset error is the difference between the ideal midscale input voltage (0 V) and the actual voltage producing the midscale output code.

Offset Calibration Range

In the system calibration modes, the AD4130-8 calibrates offset with respect to the analog input. The offset calibration range specification defines the range of voltages that the AD4130-8 can accept and still calibrate offset accurately.

Gain Error

Full-Scale Range (FSR)

The full-scale range is the input range the AD4130-8 can accept based on the choice of reference voltage and gain value. For a differential input signal, FSR = 2 × V_{REF}/gain.

Full-Scale Calibration Range

The full-scale calibration range is the range of voltages that the AD4130-8 can accept in the system calibration mode and still calibrate full scale correctly.

Output Data Rate (ODR)

The output data rate is the rate at which ADC conversions are available on a single settled channel when the ADC is continuously converting.

Same Conversion Output Data Rate (1CNV_ODR)

The same conversion output data rate is the rate at which ADC conversions are available using multiple channels with the same filter settings and taking one sample per channel.

REFERENCE

Line Regulation

Line regulation refers to the change in output voltage in response to a given change in supply voltage and is expressed in µV/V.

Load Regulation

Load regulation refers to the change in output voltage in response to a given change in load current and is expressed in µV/mA.

Voltage Reference (V_{REF}) Temperature Coefficient (TC)

V_{REF} TC is a measure of the change in the reference output voltage with a change in the ambient temperature of the device, normalized by the output voltage at 25°C. V_{REF} TC is specified using the box method, which defines TC as the maximum change in the reference output over a given temperature range expressed in ppm/°C, as follows:

$$V_{REF} \quad TC = \left(\frac{V_{REF_MAX} - V_{REF_MIN}}{V_{REF_NOM} \times TEMP_RANGE}\right) \times 10^6 ppm/°C$$

where:
V_{REF_MAX} is the maximum reference voltage output measured over the full temperature range.
V_{REF_MIN} is the minimum reference voltage output measured over the full temperature range.
V_{REF_NOM} is the nominal reference voltage output at ambient temperature (25°C).
TEMP_RANGE is the difference between the maximum and minimum operating temperature of the reference.

Voltage Reference (V_{REF}) Noise Spectral Density (NSD)

V_{REF} NSD is a measurement of the internally generated thermal noise characterized as a spectral density nV/√Hz.

TEMPERATURE SENSOR

Accuracy

The temperature sensor accuracy is the deviation of the internal measured temperature vs. the real ambient temperature normalized to a 25°C measurement. Temperature sensor accuracy is measured in °C.

TERMINOLOGY

Sensitivity

The temperature sensor sensitivity is the output voltage change due to a change in ambient temperature and is expressed in µV/K or LSB/K.

NOISE AND RESOLUTION

Table 17 through Table 36 show the RMS and peak-to-peak noise, effective resolution, and noise-free (peak-to-peak) resolution of the AD4130-8 for various output data rates, gain settings, and filters. The numbers represent the bipolar input range with an external reference of 2.5 V for the 3.3 V operations and 1.25 V for the 1.8 V operations, with the reference buffers in bypass mode. These numbers are typical and are generated with a differential input voltage of 0 V when the ADC is continuously converting on a single channel. It is important to note that the effective resolution is calculated using the RMS noise, whereas the peak-to-peak resolution (shown in parentheses) is calculated based on peak-to-peak noise (shown in parentheses). The peak-to-peak resolution represents the resolution without a code flicker.

Effective Resolution = Log_2(Input Range/RMS Noise)

Peak-to-Peak Resolution = Log_2(Input Range/Peak-to-Peak Noise)

2.5 V REFERENCE

Sinc^3

Table 17. RMS Noise (Peak-to-Peak Noise) vs. Gain and Output Data Rate, Expressed in µVRMS (µV_{P-P})

FS (Dec.)	ODR (SPS)	f_{3dB} (Hz)	Gain = 1 PGA_BYP = 1	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
2047	1.17	0.3	0.19 (1.19)	0.22 (1.29)	0.13 (0.84)	0.09 (0.55)	0.07 (0.46)	0.06 (0.42)	0.05 (0.32)	0.04 (0.23)	0.03 (0.19)
480	5	1.3	0.35 (2.19)	0.43 (2.58)	0.25 (1.64)	0.18 (1.09)	0.15 (0.92)	0.13 (0.86)	0.10 (0.62)	0.08 (0.51)	0.06 (0.40)
240	10	2.6	0.49 (3.08)	0.59 (3.78)	0.36 (2.29)	0.25 (1.64)	0.21 (1.40)	0.18 (1.15)	0.14 (0.88)	0.11 (0.75)	0.09 (0.60)
160	15	3.92	0.57 (3.68)	0.75 (4.97)	0.44 (2.93)	0.30 (1.86)	0.26 (1.60)	0.22 (1.41)	0.18 (1.21)	0.13 (0.87)	0.11 (0.71)
80	30	7.86	0.83 (5.46)	1.03 (6.76)	0.62 (3.87)	0.43 (2.66)	0.37 (2.32)	0.30 (2.16)	0.25 (1.56)	0.18 (1.24)	0.15 (0.96)
48	50	13.15	1.08 (7.05)	1.32 (8.35)	0.80 (5.32)	0.56 (3.58)	0.48 (3.24)	0.40 (2.61)	0.33 (2.17)	0.25 (1.50)	0.20 (1.24)
40	60	15.78	1.17 (7.55)	1.46 (8.74)	0.88 (5.66)	0.62 (4.07)	0.51 (3.35)	0.44 (2.89)	0.36 (2.22)	0.27 (1.70)	0.23 (1.42)
20	120	31.8	1.59 (10.13)	2.13 (14.31)	1.25 (8.49)	0.89 (5.81)	0.74 (4.72)	0.63 (3.86)	0.51 (3.29)	0.37 (2.24)	0.31 (1.95)
10	240	64.8	2.49 (15.90)	3.13 (20.66)	1.89 (11.38)	1.37 (8.67)	1.12 (6.82)	1.00 (6.70)	0.77 (5.12)	0.56 (3.54)	0.47 (2.98)
5	480	133.44	5.76 (33.78)	6.65 (43.32)	3.86 (24.94)	2.55 (16.49)	2.10 (13.59)	1.80 (11.71)	1.28 (7.90)	0.91 (6.06)	0.74 (4.37)
3	800	231.2	25.44 (149.22)	25.34 (155.38)	13.34 (85.49)	7.20 (45.70)	4.72 (30.04)	3.69 (23.55)	2.29 (15.36)	1.54 (9.50)	1.27 (7.51)
2	1200	361.2	108.05 (667.42)	109.77 (658.78)	55.46 (355.07)	28.45 (179.07)	14.81 (94.36)	9.07 (57.71)	5.10 (33.51)	3.10 (19.22)	2.25 (14.91)
1	2400	626.4	873.32 (5423.90)	890.93 (5424.10)	440.53 (2516.04)	221.90 (1317.65)	110.41 (763.43)	57.08 (361.40)	29.00 (189.77)	14.90 (88.22)	8.66 (57.57)

Table 18. Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate, Expressed in Bits

FS (Dec.)	ODR (SPS)	Gain = 1 PGA_BYP = 1	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
2047	1.17	24 (22)	24 (21.7)	24 (21.5)	23.8 (21)	23.1 (20.3)	22.3 (19.6)	21.6 (18.9)	21.1 (18.3)	20.3 (17.5)
480	5	23.8 (21.1)	23.5 (20.8)	23.2 (20.5)	22.7 (20)	22 (19.3)	21.3 (18.5)	20.5 (17.8)	19.9 (17.2)	19.2 (16.5)
240	10	23.3 (20.6)	23 (20.3)	22.7 (20)	22.3 (19.6)	21.5 (18.8)	20.8 (18)	20 (17.3)	19.4 (16.7)	18.8 (16)
160	15	23.1 (20.3)	22.7 (20)	22.4 (19.7)	22 (19.3)	21.2 (18.5)	20.5 (17.7)	19.7 (17)	19.1 (16.4)	18.4 (15.7)
80	30	22.5 (19.8)	22.2 (19.5)	22 (19.2)	21.5 (18.8)	20.7 (18)	20 (17.2)	19.2 (16.5)	18.7 (16)	18 (15.2)
48	50	22.1 (19.4)	21.9 (19.1)	21.6 (18.9)	21.1 (18.4)	20.3 (17.6)	19.6 (16.8)	18.9 (16.1)	18.3 (15.6)	17.6 (14.9)
40	60	22 (19.3)	21.7 (19)	21.4 (18.7)	20.9 (18.2)	20.2 (17.5)	19.4 (16.7)	18.7 (16)	18.1 (15.4)	17.4 (14.7)
20	120	21.6 (18.9)	21.2 (18.4)	20.9 (18.2)	20.4 (17.7)	19.7 (17)	18.9 (16.2)	18.2 (15.5)	17.7 (15)	16.9 (14.2)
10	240	20.9 (18.2)	20.6 (17.9)	20.3 (17.6)	19.8 (17.1)	19.1 (16.4)	18.3 (15.5)	17.6 (14.9)	17.1 (14.4)	16.4 (13.6)
5	480	19.7 (17)	19.5 (16.8)	19.3 (16.6)	18.9 (16.2)	18.2 (15.5)	17.4 (14.7)	16.9 (14.2)	16.4 (13.7)	15.7 (13)
3	800	17.6 (14.9)	17.6 (14.9)	17.5 (14.8)	17.4 (14.7)	17 (14.3)	16.4 (13.6)	16.1 (13.3)	15.6 (12.9)	14.9 (12.2)
2	1200	15.5 (12.8)	15.5 (12.8)	15.5 (12.7)	15.4 (12.7)	15.4 (12.6)	15.1 (12.4)	14.9 (12.2)	14.6 (11.9)	14.1 (11.4)
1	2400	12.5 (9.8)	12.5 (9.7)	12.5 (9.7)	12.5 (9.7)	12.5 (9.7)	12.4 (9.7)	12.4 (9.7)	12.4 (9.6)	12.1 (9.4)

NOISE AND RESOLUTION

Sinc^4

Table 19. RMS Noise (Peak-to-Peak Noise) vs. Gain and Output Data Rate, Expressed in μV_{RMS} (μV_{P-P})

FS (Dec.)	ODR (SPS)	f_{3dB} (Hz)	Gain = 1 PGA_BYP = 1	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
10	240	55.68	2.28 (15.00)	2.88 (18.38)	1.73 (10.83)	1.24 (8.07)	1.04 (6.95)	0.90 (5.97)	0.68 (4.03)	0.51 (3.24)	0.43 (2.75)
8	300	70.2	2.61 (17.58)	3.30 (22.25)	1.95 (12.22)	1.38 (9.61)	1.20 (7.79)	1.01 (6.36)	0.79 (5.18)	0.58 (3.75)	0.50 (3.18)
4	600	144	4.16 (28.81)	5.42 (33.28)	3.36 (21.01)	2.52 (15.70)	2.18 (13.45)	1.93 (12.52)	1.36 (8.88)	0.98 (6.44)	0.82 (5.18)
2	1200	301.2	8.81 (55.63)	11.56 (78.78)	7.54 (48.28)	5.74 (37.16)	5.09 (34.30)	4.68 (31.83)	2.95 (20.42)	2.03 (13.39)	1.71 (10.61)
1	2400	544.8	71.51 (430.67)	77.87 (459.58)	38.91 (227.06)	22.80 (138.04)	15.77 (101.41)	12.93 (79.89)	7.70 (47.71)	5.19 (32.50)	4.08 (26.55)

Table 20. Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate, Expressed in Bits

FS (Dec.)	ODR (SPS)	Gain = 1 PGA_BYP = 1	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
10	240	21.1 (18.3)	20.7 (18)	20.5 (17.7)	19.9 (17.2)	19.2 (16.5)	18.4 (15.7)	17.8 (15.1)	17.2 (14.5)	16.5 (13.8)
8	300	20.9 (18.2)	20.5 (17.8)	20.3 (17.6)	19.8 (17.1)	19 (16.3)	18.2 (15.5)	17.6 (14.9)	17 (14.3)	16.3 (13.5)
4	600	20.2 (17.5)	19.8 (17.1)	19.5 (16.8)	18.9 (16.2)	18.1 (15.4)	17.3 (14.6)	16.8 (14.1)	16.3 (13.6)	15.5 (12.8)
2	1200	19.1 (16.4)	18.7 (16)	18.3 (15.6)	17.7 (15)	16.9 (14.2)	16 (13.3)	15.7 (13)	15.2 (12.5)	14.5 (11.8)
1	2400	16.1 (13.4)	16 (13.2)	16 (13.2)	15.7 (13)	15.3 (12.6)	14.6 (11.8)	14.3 (11.6)	13.9 (11.2)	13.2 (10.5)

Sinc^3 + Sinc^1 (Averaging Filter)

Table 21. RMS Noise (Peak-to-Peak Noise) vs. Gain and Output Data Rate, Expressed in μV_{RMS} (μV_{P-P})

FS (Dec.)	ODR (SPS)	f_{3dB} (Hz)	Gain = 1 PGA_BYP = 1	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
96	2.5	1.36	0.36 (2.38)	0.44 (2.78)	0.27 (1.64)	0.18 (1.17)	0.15 (0.93)	0.13 (0.81)	0.11 (0.71)	0.08 (0.54)	0.07 (0.47)
30	8	4.36	0.63 (3.97)	0.79 (5.26)	0.46 (3.08)	0.33 (2.11)	0.27 (1.66)	0.23 (1.43)	0.20 (1.21)	0.14 (0.96)	0.12 (0.77)
6	40	21.85	1.41 (9.04)	1.78 (11.82)	1.06 (7.30)	0.75 (4.82)	0.65 (4.02)	0.53 (3.46)	0.44 (2.66)	0.32 (2.10)	0.27 (1.72)
5	48	26.22	1.60 (9.93)	2.00 (13.21)	1.22 (8.34)	0.83 (6.03)	0.70 (4.20)	0.59 (3.79)	0.48 (3.06)	0.35 (2.37)	0.29 (1.85)
2	120	65.7	11.42 (74.40)	11.93 (77.28)	6.09 (39.49)	3.16 (19.49)	1.92 (11.57)	1.32 (8.21)	0.92 (6.09)	0.65 (4.09)	0.53 (3.56)
1	240	130.8	89.40 (518.14)	90.32 (537.21)	44.72 (266.52)	22.48 (146.02)	11.75 (74.63)	6.13 (37.84)	3.21 (19.99)	1.80 (11.39)	1.15 (7.30)

Table 22. Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate, Expressed in Bits

FS (Dec.)	ODR (SPS)	Gain = 1 PGA_BYP = 1	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
96	2.5	23.7 (21.0)	23.4 (20.7)	23.2 (20.4)	22.7 (20.0)	22.0 (19.2)	21.2 (18.5)	20.4 (17.7)	19.9 (17.2)	19.2 (16.4)
30	8	22.9 (20.2)	22.6 (19.9)	22.4 (19.6)	21.9 (19.1)	21.1 (18.4)	20.4 (17.7)	19.6 (16.9)	19.1 (16.4)	18.4 (15.6)
6	40	21.8 (19.0)	21.4 (18.7)	21.2 (18.4)	20.7 (17.9)	19.9 (17.2)	19.2 (16.4)	18.4 (15.7)	17.9 (15.2)	17.1 (14.4)
5	48	21.6 (18.9)	21.3 (18.5)	21.0 (18.2)	20.5 (17.8)	19.8 (17.0)	19.0 (16.3)	18.3 (15.6)	17.8 (15.0)	17.0 (14.3)
2	120	18.7 (16.0)	18.7 (16.0)	18.6 (15.9)	18.6 (15.9)	18.3 (15.6)	17.9 (15.1)	17.4 (14.6)	16.9 (14.2)	16.2 (13.5)
1	240	15.8 (13.1)	15.8 (13.0)	15.8 (13.0)	15.8 (13.0)	15.7 (13.0)	15.6 (12.9)	15.6 (12.9)	15.4 (12.7)	15.1 (12.3)

NOISE AND RESOLUTION

Sinc^4 + Sinc^1 (Averaging Filter)

Table 23. RMS Noise (Peak-to-Peak Noise) vs. Gain and Output Data Rate, Expressed in μV_{RMS} (μV_{P-P})

FS (Dec.)	ODR (SPS)	f_{3dB} (Hz)	Gain = 1 PGA_BYP = 1	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
10	21.82	13.02	1.10 (6.85)	1.37 (8.54)	0.82 (5.26)	0.57 (3.70)	0.46 (2.96)	0.40 (2.42)	0.34 (2.14)	0.25 (1.57)	0.20 (1.41)
6	36.36	21.7	1.36 (8.94)	1.73 (12.22)	1.07 (7.25)	0.74 (4.79)	0.63 (4.11)	0.51 (3.26)	0.42 (2.82)	0.32 (2.17)	0.26 (1.77)
5	43.64	26.04	1.53 (10.53)	1.93 (13.41)	1.15 (7.15)	0.81 (5.04)	0.69 (4.28)	0.58 (3.62)	0.48 (3.18)	0.34 (2.35)	0.30 (1.80)
2	109.1	62.25	2.61 (17.58)	3.39 (20.96)	2.05 (12.81)	1.47 (9.24)	1.27 (8.57)	1.12 (6.97)	0.84 (5.27)	0.59 (3.96)	0.50 (3.10)
1	218.18	129.9	7.94 (47.28)	8.72 (57.42)	4.95 (31.89)	3.28 (20.51)	2.57 (15.10)	2.21 (13.14)	1.48 (9.52)	1.04 (7.12)	0.86 (5.77)

Table 24. Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate, Expressed in Bits

FS (Dec.)	ODR (SPS)	Gain = 1 PGA_BYP = 1	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
10	21.82	22.1 (19.4)	21.8 (19.1)	21.5 (18.8)	21.1 (18.4)	20.4 (17.6)	19.6 (16.9)	18.8 (16.1)	18.3 (15.5)	17.5 (14.8)
6	36.36	21.8 (19.1)	21.5 (18.7)	21.2 (18.4)	20.7 (18)	19.9 (17.2)	19.2 (16.5)	18.5 (15.8)	17.9 (15.2)	17.2 (14.4)
5	43.64	21.6 (18.9)	21.3 (18.6)	21.1 (18.3)	20.6 (17.8)	19.8 (17.1)	19 (16.3)	18.3 (15.6)	17.8 (15.1)	17 (14.3)
2	109.1	20.9 (18.1)	20.5 (17.8)	20.2 (17.5)	19.7 (17)	18.9 (16.2)	18.1 (15.4)	17.5 (14.8)	17 (14.3)	16.3 (13.5)
1	218.18	19.3 (16.5)	19.1 (16.4)	18.9 (16.2)	18.5 (15.8)	17.9 (15.2)	17.1 (14.4)	16.7 (14)	16.2 (13.5)	15.5 (12.7)

Post Filters

Table 25. RMS Noise (Peak-to-Peak Noise) vs. Gain and Output Data Rate, Expressed in μV_{RMS} (μV_{P-P})

Filter Type	ODR (SPS)	f_{3dB} (Hz)	Gain = 1 PGA_BYP = 1	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
Post Filter 4	16.21	12.54	1.06 (7.05)	1.34 (8.74)	0.78 (5.02)	0.57 (3.90)	0.46 (2.87)	0.39 (2.43)	0.33 (2.03)	0.24 (1.48)	0.20 (1.29)
Post Filter 3	19.355	13.08	1.13 (7.55)	1.36 (8.54)	0.81 (5.02)	0.57 (3.70)	0.48 (3.08)	0.40 (2.68)	0.33 (2.20)	0.24 (1.58)	0.20 (1.37)
Post Filter 2	24	14.7	1.36 (8.94)	1.60 (10.33)	0.92 (6.11)	0.64 (4.20)	0.52 (3.34)	0.44 (3.05)	0.35 (2.37)	0.26 (1.72)	0.21 (1.43)
Post Filter 1	26.087	16.68	1.22 (8.15)	1.53 (10.23)	0.92 (6.11)	0.65 (4.52)	0.54 (3.71)	0.45 (2.86)	0.38 (2.33)	0.28 (1.85)	0.23 (1.52)

Table 26. Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate, Expressed in Bits

Filter Type	ODR (SPS)	Gain = 1 PGA_BYP = 1	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
Post Filter 4	16.21	22.2 (19.5)	21.8 (19.1)	21.6 (18.9)	21.1 (18.4)	20.4 (17.7)	19.6 (16.9)	18.9 (16.2)	18.3 (15.6)	17.6 (14.8)
Post Filter 3	19.355	22.1 (19.4)	21.8 (19.1)	21.6 (18.8)	21.1 (18.3)	20.3 (17.6)	19.6 (16.8)	18.9 (16.1)	18.3 (15.6)	17.6 (14.8)
Post Filter 2	24	22 (19.3)	21.6 (18.9)	21.4 (18.6)	20.9 (18.2)	20.2 (17.5)	19.4 (16.7)	18.8 (16)	18.2 (15.5)	17.5 (14.8)
Post Filter 1	26.087	21.8 (19.1)	21.6 (18.9)	21.4 (18.7)	20.9 (18.1)	20.1 (17.4)	19.4 (16.7)	18.6 (15.9)	18.1 (15.4)	17.4 (14.6)

1.25 V REFERENCE

Sinc^3

Table 27. RMS Noise (Peak-to-Peak Noise) vs. Gain and Output Data Rate, Expressed in μV_{RMS} (μV_{P-P})

FS (Dec.)	ODR (SPS)	f_{3dB} (Hz)	Gain = 1 PGA_BYP = 1	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
2047	1.17	0.3	0.16 (0.99)	0.21 (1.34)	0.13 (0.82)	0.09 (0.57)	0.07 (0.50)	0.06 (0.36)	0.05 (0.33)	0.04 (0.25)	0.03 (0.22)
480	5	1.3	0.33 (2.09)	0.43 (2.88)	0.26 (1.69)	0.18 (1.22)	0.15 (0.94)	0.13 (0.83)	0.10 (0.67)	0.08 (0.55)	0.06 (0.44)
240	10	2.6	0.47 (2.98)	0.61 (4.17)	0.36 (2.29)	0.25 (1.53)	0.21 (1.42)	0.18 (1.18)	0.15 (1.08)	0.11 (0.74)	0.09 (0.58)

NOISE AND RESOLUTION

Table 27. RMS Noise (Peak-to-Peak Noise) vs. Gain and Output Data Rate, Expressed in μV_{RMS} (μV_{P-P}) (Continued)

FS (Dec.)	ODR (SPS)	f_{3dB} (Hz)	Gain = 1 PGA_BYP = 1	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
160	15	3.92	0.57 (3.87)	0.70 (4.47)	0.44 (2.68)	0.31 (1.97)	0.26 (1.78)	0.22 (1.43)	0.19 (1.25)	0.13 (0.90)	0.11 (0.76)
80	30	7.86	0.81 (5.51)	1.03 (6.86)	0.62 (3.70)	0.44 (2.99)	0.36 (2.19)	0.31 (2.14)	0.26 (1.66)	0.19 (1.12)	0.16 (0.96)
48	50	13.15	1.07 (7.05)	1.34 (8.54)	0.80 (5.09)	0.57 (3.74)	0.49 (3.58)	0.41 (2.71)	0.33 (2.20)	0.25 (1.64)	0.21 (1.41)
40	60	15.78	1.17 (7.50)	1.45 (9.09)	0.85 (5.91)	0.63 (4.17)	0.52 (3.23)	0.45 (3.10)	0.37 (2.44)	0.27 (1.71)	0.23 (1.57)
20	120	31.8	1.66 (11.08)	2.07 (14.31)	1.26 (8.07)	0.90 (5.71)	0.74 (4.53)	0.65 (4.34)	0.53 (3.47)	0.39 (2.41)	0.32 (2.02)
10	240	64.8	2.37 (15.75)	3.07 (21.01)	1.86 (11.47)	1.33 (8.79)	1.12 (7.66)	0.99 (7.02)	0.78 (5.07)	0.58 (3.46)	0.47 (2.91)
5	480	133.44	4.23 (27.32)	5.18 (31.84)	3.16 (21.04)	2.23 (13.62)	1.95 (12.25)	1.67 (11.30)	1.25 (8.59)	0.94 (5.99)	0.78 (5.01)
3	800	231.2	13.79 (91.65)	14.57 (97.41)	7.78 (48.81)	4.82 (31.51)	3.73 (21.97)	3.12 (18.61)	2.11 (13.12)	1.53 (10.30)	1.25 (8.08)
2	1200	361.2	56.65 (348.62)	58.95 (383.78)	29.90 (170.04)	15.07 (88.48)	9.35 (59.43)	6.32 (38.24)	3.93 (25.58)	2.62 (16.29)	2.11 (14.12)
1	2400	626.4	451.81 (2831.34)	441.73 (2720.87)	225.95 (1360.33)	114.08 (712.09)	59.38 (378.43)	31.81 (190.83)	16.53 (97.28)	9.33 (58.10)	6.16 (38.91)

Table 28. Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate, Expressed in Bits

FS (Dec.)	ODR (SPS)	Gain = 1 PGA_BYP = 1	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
2047	1.17	24 (21.1)	23.5 (20.8)	23.2 (20.5)	22.8 (20.1)	22 (19.3)	21.3 (18.6)	20.5 (17.8)	20 (17.2)	19.2 (16.5)
480	5	22.8 (20.1)	22.5 (19.8)	22.2 (19.5)	21.7 (19)	21 (18.3)	20.2 (17.5)	19.5 (16.8)	19 (16.2)	18.2 (15.5)
240	10	22.3 (19.6)	22 (19.3)	21.7 (19.0)	21.3 (18.6)	20.5 (17.8)	19.7 (17)	19 (16.3)	18.4 (15.7)	17.7 (14.9)
160	15	22.1 (19.3)	21.8 (19.0)	21.5 (18.7)	21 (18.2)	20.2 (17.5)	19.5 (16.7)	18.7 (15.9)	18.1 (15.4)	17.4 (14.7)
80	30	21.6 (18.8)	21.2 (18.5)	20.9 (18.2)	20.4 (17.7)	19.7 (17)	18.9 (16.2)	18.2 (15.5)	17.6 (14.9)	16.9 (14.2)
48	50	21.2 (18.4)	20.8 (18.1)	20.6 (17.9)	20.1 (17.4)	19.3 (16.6)	18.6 (15.8)	17.8 (15.1)	17.3 (14.5)	16.5 (13.8)
40	60	21.0 (18.3)	20.7 (18.0)	20.5 (17.8)	19.9 (17.2)	19.2 (16.5)	18.4 (15.7)	17.7 (15)	17.1 (14.4)	16.4 (13.7)
20	120	20.5 (17.8)	20.2 (17.5)	19.9 (17.2)	19.4 (16.7)	18.7 (16)	17.9 (15.2)	17.2 (14.5)	16.6 (13.9)	15.9 (13.2)
10	240	20.0 (17.3)	19.6 (16.9)	19.4 (16.6)	18.8 (16.1)	18.1 (15.4)	17.3 (14.5)	16.6 (13.9)	16 (13.3)	15.3 (12.6)
5	480	19.2 (16.4)	18.9 (16.2)	18.6 (15.9)	18.1 (15.4)	17.3 (14.6)	16.5 (13.8)	15.9 (13.2)	15.3 (12.6)	14.6 (11.9)
3	800	17.5 (14.7)	17.4 (14.7)	17.3 (14.6)	17 (14.3)	16.4 (13.6)	15.6 (12.9)	15.2 (12.5)	14.6 (11.9)	13.9 (11.2)
2	1200	15.4 (12.7)	15.4 (12.7)	15.4 (12.6)	15.3 (12.6)	15 (12.3)	14.6 (11.9)	14.3 (11.6)	13.9 (11.1)	13.2 (10.5)
1	2400	12.4 (9.7)	12.5 (9.7)	12.4 (9.7)	12.4 (9.7)	12.4 (9.6)	12.3 (9.5)	12.2 (9.5)	12 (9.3)	11.6 (8.9)

Sinc^4

Table 29. RMS Noise (Peak-to-Peak Noise) vs. Gain and Output Data Rate, Expressed in μV_{RMS} (μV_{P-P})

FS (Dec.)	ODR (SPS)	f_{3dB} (Hz)	Gain = 1 PGA_BYP = 1	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
10	240	55.68	2.22 (14.21)	2.78 (18.88)	1.71 (11.62)	1.23 (7.99)	1.05 (6.90)	0.88 (5.80)	0.72 (4.84)	0.54 (3.29)	0.43 (2.88)
8	300	70.2	2.51 (15.65)	3.12 (18.33)	1.91 (12.20)	1.42 (9.21)	1.18 (7.54)	1.02 (6.34)	0.82 (4.99)	0.61 (4.14)	0.50 (3.24)
4	600	144	3.76 (24.79)	4.90 (33.03)	3.14 (20.04)	2.34 (16.72)	2.05 (13.35)	1.83 (11.89)	1.39 (9.32)	0.99 (6.47)	0.82 (5.37)
2	1200	301.2	6.49 (42.42)	9.25 (60.21)	6.45 (40.81)	5.07 (33.67)	4.57 (29.84)	4.25 (28.16)	2.86 (18.03)	2.00 (13.35)	1.68 (11.20)
1	2400	544.8	36.27 (207.89)	41.37 (247.28)	23.57 (142.32)	15.13 (100.89)	12.30 (77.83)	11.32 (71.09)	7.06 (48.19)	4.80 (32.89)	3.98 (24.31)

NOISE AND RESOLUTION

Table 30. Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate, Expressed in Bits

FS (Dec.)	ODR (SPS)	Gain = 1 PGA_BYP = 1	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
10	240	20.1 (17.4)	19.8 (17.1)	19.5 (16.8)	19 (16.2)	18.2 (15.5)	17.4 (14.7)	16.7 (14)	16.2 (13.4)	15.5 (12.7)
8	300	19.9 (17.2)	19.6 (16.9)	19.3 (16.6)	18.7 (16)	18 (15.3)	17.2 (14.5)	16.5 (13.8)	16 (13.2)	15.2 (12.5)
4	600	19.3 (16.6)	19 (16.2)	18.6 (15.9)	18 (15.3)	17.2 (14.5)	16.4 (13.7)	15.8 (13.1)	15.3 (12.6)	14.5 (11.8)
2	1200	18.6 (15.8)	18 (15.3)	17.6 (14.8)	16.9 (14.2)	16.1 (13.3)	15.2 (12.4)	14.7 (12)	14.3 (11.5)	13.5 (10.8)
1	2400	16.1 (13.4)	15.9 (13.2)	15.7 (13)	15.3 (12.6)	14.6 (11.9)	13.8 (11)	13.4 (10.7)	13 (10.3)	12.3 (9.5)

$Sinc^3 + Sinc^1$ (Averaging Filter)

Table 31. RMS Noise (Peak-to-Peak Noise) vs. Gain and Output Data Rate, Expressed in μV_{RMS} (μV_{P-P})

FS (Dec.)	ODR (SPS)	f_{3dB} (Hz)	Gain = 1 PGA_BYP = 1	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
96	2.5	1.36	0.35 (2.09)	0.43 (3.13)	0.26 (1.69)	0.19 (1.22)	0.15 (1.02)	0.13 (0.86)	0.11 (0.78)	0.08 (0.48)	0.07 (0.44)
30	8	4.36	0.61 (4.17)	0.77 (4.62)	0.47 (3.08)	0.33 (2.19)	0.28 (1.91)	0.23 (1.48)	0.19 (1.28)	0.15 (0.98)	0.12 (0.81)
6	40	21.85	1.39 (9.04)	1.78 (12.42)	1.07 (6.66)	0.76 (4.61)	0.64 (4.29)	0.53 (3.54)	0.44 (2.79)	0.33 (2.14)	0.27 (1.72)
5	48	26.22	1.57 (10.08)	1.95 (11.72)	1.17 (7.52)	0.82 (5.66)	0.71 (4.56)	0.59 (3.96)	0.47 (3.07)	0.36 (2.23)	0.30 (1.95)
2	120	65.7	6.32 (42.07)	6.57 (40.63)	3.54 (22.20)	2.09 (13.48)	1.47 (9.39)	1.17 (7.37)	0.87 (5.38)	0.64 (4.41)	0.52 (3.37)
1	240	130.8	45.47 (299.49)	47.55 (293.18)	23.49 (143.39)	12.20 (74.61)	6.32 (43.04)	3.65 (24.18)	2.11 (13.76)	1.33 (8.83)	1.00 (6.17)

Table 32. Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate, Expressed in Bits

FS (Dec.)	ODR (SPS)	Gain = 1 PGA_BYP = 1	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
96	2.5	22.8 (20.0)	22.5 (19.7)	22.2 (19.5)	21.7 (18.9)	21.0 (18.2)	20.2 (17.4)	19.4 (16.7)	18.9 (16.2)	18.1 (15.4)
30	8	22.0 (19.2)	21.6 (18.9)	21.3 (18.6)	20.9 (18.1)	20.1 (17.4)	19.3 (16.6)	18.6 (15.9)	18.0 (15.3)	17.3 (14.6)
6	40	20.8 (18.1)	20.4 (17.7)	20.2 (17.4)	19.7 (16.9)	18.9 (16.2)	18.2 (15.4)	17.4 (14.7)	16.9 (14.2)	16.1 (13.4)
5	48	20.6 (17.9)	20.3 (17.6)	20.0 (17.3)	19.5 (16.8)	18.8 (16.0)	18.0 (15.3)	17.3 (14.6)	16.7 (14.0)	16.0 (13.3)
2	120	18.6 (15.9)	18.5 (15.8)	18.4 (15.7)	18.2 (15.5)	17.7 (15.0)	17.0 (14.3)	16.4 (13.7)	15.9 (13.2)	15.2 (12.5)
1	240	15.8 (13.0)	15.7 (13.0)	15.7 (13.0)	15.6 (12.9)	15.6 (12.9)	15.4 (12.7)	15.2 (12.5)	14.8 (12.1)	14.3 (11.5)

$Sinc^4 + Sinc^1$ (Averaging Filter)

Table 33. RMS Noise (Peak-to-Peak Noise) vs. Gain and Output Data Rate, Expressed in μV_{RMS} (μV_{P-P})

FS (Dec.)	ODR (SPS)	f_{3dB} (Hz)	Gain = 1 PGA_BYP = 1	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
10	21.82	13.02	1.08 (6.80)	1.37 (9.19)	0.79 (4.92)	0.57 (3.79)	0.49 (3.38)	0.41 (2.53)	0.34 (2.35)	0.25 (1.49)	0.21 (1.36)
6	36.36	21.7	1.39 (8.89)	1.72 (11.13)	1.04 (6.53)	0.75 (4.93)	0.62 (3.93)	0.54 (3.38)	0.44 (2.66)	0.32 (1.93)	0.27 (1.74)
5	43.64	26.04	1.54 (9.49)	1.89 (11.92)	1.17 (7.47)	0.82 (5.38)	0.69 (4.47)	0.58 (3.76)	0.48 (3.01)	0.36 (2.26)	0.29 (1.81)
2	109.1	62.25	2.49 (15.05)	3.22 (21.85)	1.99 (12.19)	1.43 (10.28)	1.21 (8.00)	1.05 (7.08)	0.82 (5.56)	0.60 (4.01)	0.51 (3.26)
1	218.18	129.9	4.96 (31.89)	6.16 (40.03)	3.81 (24.76)	2.62 (16.96)	2.28 (14.48)	1.99 (12.96)	1.47 (9.18)	1.04 (6.90)	0.86 (5.31)

Table 34. Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate, Expressed in Bits

FS (Dec.)	ODR (SPS)	Gain = 1 PGA_BYP = 1	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
30	21.82	21.1 (18.4)	20.8 (18.1)	20.6 (17.9)	20.1 (17.3)	19.3 (16.6)	18.6 (15.8)	17.8 (15.1)	17.3 (14.5)	16.5 (13.8)
6	36.36	20.8 (18.1)	20.5 (17.7)	20.2 (17.5)	19.7 (16.9)	18.9 (16.2)	18.1 (15.4)	17.4 (14.7)	16.9 (14.2)	16.1 (13.4)
5	43.64	20.6 (17.9)	20.3 (17.6)	20 (17.3)	19.5 (16.8)	18.8 (16.1)	18 (15.3)	17.3 (14.6)	16.7 (14)	16 (13.3)
2	109.1	19.9 (17.2)	19.6 (16.8)	19.3 (16.5)	18.7 (16)	18 (15.3)	17.2 (14.5)	16.5 (13.8)	16 (13.3)	15.2 (12.5)

NOISE AND RESOLUTION

Table 34. Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate, Expressed in Bits (Continued)

FS (Dec.)	ODR (SPS)	Gain = 1 PGA_BYP = 1	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
1	218.18	18.9 (16.2)	18.6 (15.9)	18.3 (15.6)	17.9 (15.1)	17.1 (14.3)	16.3 (13.5)	15.7 (13)	15.2 (12.5)	14.5 (11.8)

Post Filters

Table 35. RMS Noise (Peak-to-Peak Noise) vs. Gain and Output Data Rate, Expressed in μV_{RMS} (μV_{P-P})

Filter Type	ODR (SPS)	f_{3dB} (Hz)	Gain = 1 PGA_BYP = 1	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
Post Filter 4	16.21	12.54	1.03 (6.36)	1.33 (8.39)	0.79 (5.49)	0.55 (3.60)	0.47 (3.09)	0.39 (2.46)	0.33 (2.12)	0.25 (1.62)	0.21 (1.35)
Post Filter 3	19.355	13.08	1.09 (6.95)	1.36 (8.34)	0.82 (5.09)	0.56 (3.61)	0.48 (2.93)	0.40 (2.69)	0.34 (2.15)	0.26 (1.66)	0.21 (1.36)
Post Filter 2	24	14.7	1.18 (7.40)	1.50 (10.33)	0.88 (5.69)	0.62 (3.91)	0.51 (3.19)	0.43 (2.72)	0.36 (2.33)	0.26 (1.76)	0.22 (1.44)
Post Filter 1	26.087	16.68	1.24 (8.49)	1.53 (9.24)	0.90 (5.79)	0.65 (4.32)	0.54 (3.59)	0.47 (3.05)	0.39 (2.40)	0.28 (2.02)	0.24 (1.63)

Table 36. Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate, Expressed in Bits

Filter Type	ODR (SPS)	Gain = 1 PGA_BYP = 1	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
Post Filter 4	16.21	21.2 (18.5)	20.8 (18.1)	20.6 (17.9)	20.1 (17.4)	19.3 (16.6)	18.6 (15.9)	17.9 (15.2)	17.3 (14.6)	16.5 (13.8)
Post Filter 3	19.355	21.1 (18.4)	20.8 (18.1)	20.5 (17.8)	20.1 (17.4)	19.3 (16.6)	18.6 (15.8)	17.8 (15.1)	17.2 (14.5)	16.5 (13.8)
Post Filter 2	24	21 (18.3)	20.7 (17.9)	20.4 (17.7)	19.9 (17.2)	19.2 (16.5)	18.5 (15.8)	17.7 (15)	17.2 (14.5)	16.4 (13.7)
Post Filter 1	26.087	20.9 (18.2)	20.6 (17.9)	20.4 (17.7)	19.9 (17.1)	19.1 (16.4)	18.3 (15.6)	17.6 (14.9)	17.1 (14.4)	16.3 (13.6)

NOISE SPECTRAL DENSITY

The noise spectral density is derived from the 2.5 V reference rms noise values for the $sinc^3$ filter at a lower ODR, divided by 1.15 times the square root of the input bandwidth.

Table 37. Input Referred Noise Spectral Density, Expressed in nV/√Hz

Gain = 1 PGA_BYP = 1	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
303	369	214	152	123	99	85	64	48

THEORY OF OPERATION

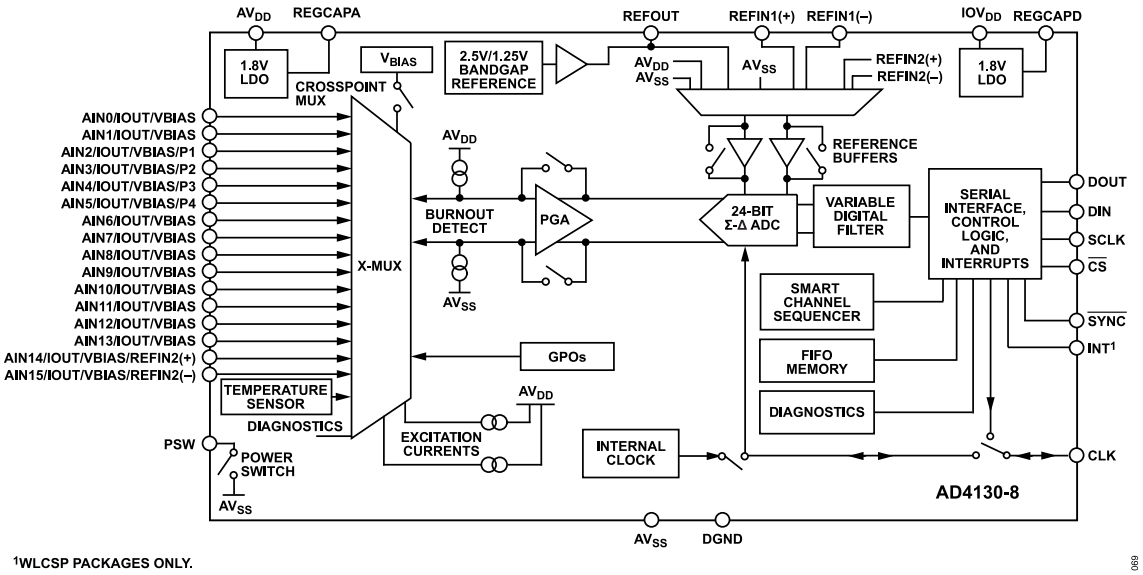


Figure 70. Detailed Block Diagram

OVERVIEW

The AD4130-8 is an ultra low power, 24-bit ADC that incorporates a Σ-Δ modulator, an input crosspoint multiplexer (X-MUX), a PGA stage, an internal reference and reference buffers, and on-chip digital filtering, which is intended for the measurement of high dynamic range, low frequency signals, such as those in pressure transducers, weigh scales, and temperature measurement applications. Each block of the AD4130-8 and its functionality is optimized for low power operations in battery-powered applications. Included on chip is a suite of integrated functions to connect and power multiple sensors, such as excitation currents, a low-side power switch, bias voltage, and burnout currents. The combination of a smart sequencer, duty cycling ability, and FIFO buffer allows the rest of the system to sleep while the AD4130-8 autonomously gathers measurements according to the predefined configuration. User defined interrupt functionality allows the microcontroller to wake when a problem occurs, or the FIFO is ready to be read.

ADC CORE

The AD4130-8 contains a Σ-Δ-based ADC core, composed of a MASH22 Σ-Δ modulator (f_{MOD} = 38.4 kHz), followed by a digital filter. The ADC core inherently rejects frequencies at 38.4 kHz. The Σ-Δ ADC highly digital architecture is ideally suited for modern fine-line CMOS processes, thereby allowing easy addition of digital functionality without significantly increasing the cost. Using oversampling, quantization noise shaping, digital filtering, and decimation, a Σ-Δ ADC offers several advantages over the other architectures, especially for high resolution, low frequency applications. Refer to MT-022 and MT-023 for a deep dive in Σ-Δ ADC theory.

Digital Filter

The AD4130-8 offers several digital filter options. The option selected affects the input bandwidth, output data rate, achievable noise performance, settling time, and 50 Hz and 60 Hz rejection. The device filter options are listed in Table 38. See the Digital Filters section for full details.

THEORY OF OPERATION

Table 38. AD4130-8 Filter Options

Filter Type	FS Range (Hex)	Output Data Rate (SPS)[1]	Comments
$Sinc^4$	0x01 to 0xA	2400 to 240	ADC frequency (f_{ADC}) = f_{MCLK} / 32 / FS.
$Sinc^4$ + $Sinc^1$	0x01 to 0xA	218.18 to 21.8	Averaging filter. $Sinc^4$ plus averaging by 8. $f_{ADC} = f_{MCLK} / (32 \times FS \times (4 + AVG - 1))$, where AVG = 8.
$Sinc^3$	0x01 to 0x7FF	2400 to 1.17	$f_{ADC} = f_{MCLK}/32/FS$.
$Sinc^3$ + REJ60	0x01 to 0x7FF	2400 to 1.17	FS = 0d48 can be set to simultaneously reject 50 Hz and 60 Hz at 50 SPS ODR.
$Sinc^3$ + $Sinc^1$	0x01 to 0x7FF	240 to 0.117 (Dec.: 1 to 2047)	Averaging filter. $Sinc^3$ plus averaging by 8. Recommended for FS from 0x01 to 0xCC only (minimum ODR = 1.17). $f_{ADC} = f_{MCLK}/(32 \times FS \times (3 + AVG - 1))$, where AVG = 8.
$Sinc^3$ + Post Filters	N/A[2]	16.21, 19.355, 24, 26.087	Low latency with good 50 Hz and 60 Hz rejection.

[1] Assuming accurate f_{MCLK} = 76.8 kHz.

[2] N/A means not applicable.

ADC MASTER CLOCK

The Σ-Δ ADC core needs a 76.8 kHz MCLK to operate the internal modulator ($f_{MOD} = f_{MCLK}/2$ = 38.4 kHz). The device has an internal oscillator to generate the MCLK. The internal clock is selected by default and can be made available at the CLK pin if a clock source is required for external circuitry. An external clock applied to the CLK pin can also be selected as the MCLK source for the device. Using an external clock can enable several ADCs to be driven from a common clock, allowing simultaneous conversions to be performed. The external clock can be either 76.8 kHz or 153.6 kHz when the internal divide by two option is selected.

Use the MCLK_SEL bits in the ADC_CONTROL register to select the appropriate option according to Table 39 (see the ADC Control Register section). Refer to Figure 70 for a block diagram of the AD4130-8 ADC clock connection scheme.

Table 39. MCLK Source Options

MCLK_SEL	MCLK Source	Source Clock Frequency (kHz)
0b00 (Default)	Internal, output off	76.8
0b01	Internal, output on	76.8
0b10	External, divider off	76.8
0b11	External, divider on	153.6

The CLK pin, if not used, can instead be selected as the interrupt source using the INT_PIN_SEL bit in the IO_CONTROL register (see the Input/Output Control Register section for details). Note that the interrupt setting takes priority on the CLK_SEL bit setting in the ADC_CONTROL register.

ADC REFERENCE

The AD4130-8 requires a precision reference voltage for the ADC core. The reference source for the AD4130-8 can be selected for each ADC setup (see the ADC Configuration and Operations section for full details) using the REF_SEL bits in each the CONFIG_n register (see Table 50).

The AD4130-8 integrates a band gap voltage reference that can be configured to give a 1.25 V or a 2.5 V low noise voltage reference (see the specifications in Table 3). The internal reference is disabled by default. To enable the internal reference, set the INT_REF_EN bit in the ADC_CONTROL register to 1. The 2.5 V internal reference is selected by default. A 1 nF capacitor is required on the REFOUT pin when the internal reference is active. Note that when the AV_{DD} supply is set to below 2.5 V, the internal reference of 1.25 V is selected by setting the INT_REF_VAL bit in the ADC_CONTROL register to 1. This bit has effect only when the internal reference is enabled. The internal reference value is set to 2.5 V by default.

When entering and exiting standby mode (that is, while using duty cycling mode) while using the internal reference, and providing that the reference is not loaded by any external circuitry other than its decoupling, it is recommended to set the STBY_REFHOL_EN bit to 1 in the MISC register. This enables the reference holder that is designed to reduce the supply current consumption (IDD) contribution of the internal reference continuously turning on and off. In the scenario that duty cycling is used and the internal reference is used to power a sensor, it is recommended to keep the reference on during the standby phase by enabling the STBY_REFCORE_EN bit to 1 in the MISC register. See the Standby Mode section for more details on the blocks that can be kept active when in standby during duty cycling.

An external voltage reference can be supplied at the two external reference input options: REFIN1(±) or REFIN2(±). The external reference option can be useful when ratio-metric measurement is required on some channels, such as when interfacing to an RTD temperature sensor.

Refer to Figure 70 for a simplified schematic of the AD4130-8 ADC reference connection scheme.

Reference Buffers

Reference buffers are also included on chip, and they can be used with the internal reference or an externally applied reference. The buffers bypass option allows full rail-to-rail reference input up to the analog supply value, whereas the buffers enabled option allows for a lower reference input current. Both options have similar AV_{DD} current. See Table 3 for related specifications. Reference

THEORY OF OPERATION

buffers can be enabled on a per channel basis, in each CONFIG_n register.

ANALOG FRONT END

Analog Input Multiplexer

The device can have 8 differential or 16 pseudo differential analog inputs. The AD4130-8 uses flexible multiplexing; thus, any analog input pin can be selected as a positive input (AINP) and any analog input pin can be selected as a negative input (AINM), as described in Figure 71. This feature allows the user to perform diagnostics, such as checking that pins are connected. This feature also simplifies PCB design. For example, the same PCB can accommodate 2-wire, 3-wire, and 4-wire RTDs.

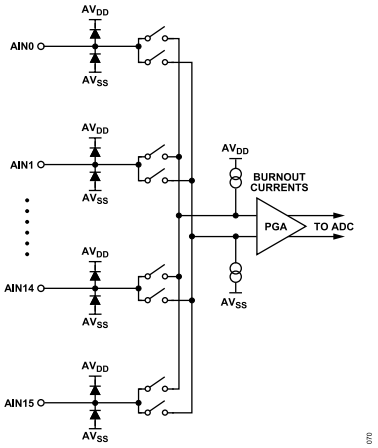


Figure 71. Analog Input Multiplexer Circuit

The on-chip multiplexer increases the channel count of the device and guarantees that all channel changes are synchronized with the conversion process.

The channel inputs are configured using the AINP_m, Bits[4:0] and the AINM_m, Bits[4:0] in the CHANNEL_m registers. The device can be configured to have 8 differential inputs, 16 pseudo differential inputs, or a combination of both.

When using differential inputs, use adjacent analog input pins to form the input pair. Using adjacent pins minimizes any mismatch between the channels.

Excitation Currents

The device contains two excitation currents, IEXC0 and IEXC1, that can be set independently to 100 nA, 10 µA, 20 µA, 50 µA, 100 µA, 150 µA, and 200 µA by setting the I_OUT0_n and I_OUT1_n bitfields in the CONFIG_n registers. See Table 4 for excitation currents specifications.

IEXC0 and IEXC1 can be configured to operate on any channel by setting the I_OUT0_CH_m and I_OUT1_CH_m bitfields in the CHANNEL_m registers. In addition, both currents can be output to the same analog input pin. The user can select the front-end settling time (SETTLE_n bits in the FILTER_n register) when multiplexing between channels, after which the conversion process begins.

The user can decide to turn off the excitation currents automatically when the device is in standby mode by setting the STB_EN_IEXC bit to 1 in the MISC register.

Note that the on-chip reference does not need to be enabled when using the excitation currents.

Bias Voltage Generator

A bias voltage generator is included on the AD4130-8. The bias voltage is selectable on all analog input channels. It biases the selected input pin to $(AV_{DD} - AV_{SS})/2$. This function is useful in thermocouple applications, as the voltage generated by the thermocouple must be biased around some dc voltage if the ADC operates from a single power supply. The bias voltage generator is controlled using the V_BIAS bitfield in the VBIAS_CONTROL register. The power-up time of the bias voltage generator is dependent on the load capacitance. See Table 4 for more details.

Secondary Reference Input

Two of the AD4130-8 inputs can be reconfigured to become the reference inputs instead.

General-Purpose Output

The AD4130-8 has four general-purpose outputs (GPOs), the P1 to P4 pins. These outputs are enabled using the GPO_CTRL_Px bits in the IO_CONTROL register (see Table 41). The pins can be pulled high or low using the GPO_DATA_Px bits in the register; that is, the value at the pin is determined by the setting of the GPO_DATA_Px bits. These pins can be used as general-purpose outputs, referenced between AV_{SS} and AV_{DD}.

When AV_{SS} is tied to DGND and IOV_{DD} is tied to AV_{DD}, these pins can operate as digital outputs with logic levels determined by AV_{DD} rather than by IOV_{DD}. In this configuration, some GPOs can be repurposed for different uses. The P2 (AIN3) pin can be selected to function as the interrupt source (see the Data Ready Signal section). The P4 pin (AIN5) can be selected to flag when the device is in standby mode (see the Power-Down Modes section).

Power-Down Switch

A low-side power switch (PSW) allows the user to power-down bridges that are interfaced to the ADC. In bridge applications such as strain gauges and load cells, the bridge itself consumes the majority of the current in the system. For example, a 350 Ω load cell requires 8.6 mA of current when excited with a 3 V supply. To minimize the current consumption of the system, the bridge can be disconnected, when not being used, using the bridge power-down switch. See Table 4 for the switch specifications. The control of the PSW can be automated by using the channel sequencer. Every

THEORY OF OPERATION

channel configuration has a dedicated PDSW_m bitfield in the CHANNEL_m register.

PROGRAMMABLE GAIN AMPLIFIER

When the gain stage is enabled, the output from the multiplexer is applied to the input of the PGA. The presence of the PGA means that signals of small amplitude can be gained within the AD4130-8 and still maintain excellent noise performance. The PGA can be programmed to have a gain of 1, 2, 4, 8, 16, 32, 64, or 128 by using the PGA bits in the respective CONFIG_n register.

It is also possible to bypass the PGA by enabling the PGA_BYP_n bit in each CONFIG_n register. Once this bit is set to 1, the PGA is bypassed, so the gain control is not available and a gain of 1 is used. PGA bypass mode can be used to save power and reduce the noise even further, at the expense of higher analog input current. See the Power Specifications section and the Analog Input Currents section for further details.

The analog input range is $\pm V_{REF}$/gain. See Table 40.

Table 40. Absolute Input Range Examples

PGA Gain	2.5 V Reference		1.25 V Reference	
	Unipolar	Bipolar	Unipolar	Bipolar
1	0 to 2.5 V	±2.5 V	0 to 1.25 V	±1.25 V
32	0 to 78.12 mV	±78.12 mV	0 to 39.06 mV	±39.06 mV
128	0 to 19.53 mV	±19.53 mV	0 to 9.76 mV	±9.76 mV

For high reference values, for example, $V_{REF} = AV_{DD}$, the analog input range must be limited. Consult Table 2 for more details on these limits.

Table 41. IO_CONTROL Register

Addr.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x03	IO_CONTROL	[15:8]	RESERVED					SYNCB_CLEAR	INT_PIN_SEL		0x0000	R/W
		[7:0]	GPO_DATA_P4	GPO_DATA_P3	GPO_DATA_P2	GPO_DATA_P1	GPO_CTRL_P4	GPO_CTRL_P3	GPO_CTRL_P2	GPO_CTRL_P1		

THEORY OF OPERATION

OTHER FEATURES

Calibration

Both internal calibration and system calibration are available on chip; therefore, the user has the option of removing offset or gain errors internal to the device only, or removing the offset or gain errors of the complete end system. See the ADC Calibration section.

Sequencer

The AD4130-8 allows up to 16 channels, and up to eight different ADC setups to be preconfigured and selected for each channel. The sequencer automatically converts all enabled channels. See the Smart Channel Sequencer section for full details.

Diagnostics

The AD4130-8 includes numerous diagnostics features that allow a high level of fault coverage in an application, such as:

- Reference detection
- Overvoltage/undervoltage detection
- ADC functionality checks
- CRC on SPI communications
- CRC on the memory map
- SPI read/write checks

See the Diagnostics section for full details.

FIFO Buffer

The AD4130-8 has an on-chip FIFO buffer to facilitate storage of up to 256 conversion results. See the FIFO section for full details.

POWER SUPPLIES

The device has two independent power supply pins: AV_{DD} and IOV_{DD}.

AV_{DD} is referred to AV_{SS} and powers the internal analog regulator that supplies the ADC. The $AV_{DD} - AV_{SS}$ supply range is from 1.71 V to 3.6 V.

AV_{SS} is either tied to DGND or it can be taken below 0 V to provide a dual power supply to the AD4130-8. For example, AV_{SS} can be tied to −1.8 V and AV_{DD} can be tied to +1.8 V, providing a ±1.8 V supply to the ADC. The AV_{SS} supply range is from −1.8 V to 0 V with respect to DGND.

IOV_{DD} is referred to DGND and sets the interface logic levels on the SPI, and powers an internal regulator for operation of the digital processing. The digital IOV_{DD} supply can vary between 1.65 V to 3.6 V with respect to DGND.

The low supply range option is advantageous for battery-powered operation, with the AD4130-8 performance still achievable with a single supply for both AV_{DD} and IOV_{DD} as low as 1.71 V.

See the Power Schemes section and Recommended Decoupling section.

Internal LDOs

The two internal LDOs power the analog and digital domains separately. A decoupling capacitor of 0.1 µF is required on the REGCAPA and REGCAPD pins, which are the outputs of the AV_{DD} and IOV_{DD} LDOs, respectively.

Power-On Reset

The AD4130-8 is designed to generate a power-on reset (POR) signal when the IOV_{DD} voltage is first applied, as shown in Figure 72. A POR resets the state of the user configuration registers. If IOV_{DD} and the digital LDOs drops below its specified operating range, a POR occurs. A drop on AV_{DD} and the analog LDO does not trigger a reset of the device.

The POR_FLAG in the status register (see Table 48) is set to 1 if IOV_{DD} or the digital LDO supply dips below the threshold, and is cleared when the user reads the status register.

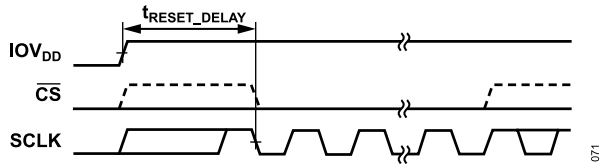


Figure 72. POR Timing Diagram

After power-on or software reset, the AD4130-8 default configuration is as follows:

- Channel: in the CHANNEL_0 register, the channel is enabled, AIN0 is selected as the positive input, and AIN1 is selected as the negative input. SETUP_m = 0 is selected.
- ADC setup (SETUP_m bitfield): in the CONFIG_0 register, the excitation and burnout currents are off, the reference buffers are disabled, the external reference is selected, and the PGA gain is set to 1. In the FILTER_0 register, the $sinc^3$ standalone filter is selected with FS, Bits[10:0] = 0x30.
- ADC control: in the ADC_CONTROL register (see Table 47), the AD4130-8 is in continuous conversion mode with continuous read disabled and the data coding set to offset binary, and the internal oscillator is enabled and selected as the master clock source. The internal reference is disabled, the $\overline{CS}$ pin is disabled (3-wire mode), and the status register content is not appended to the data output.
- Diagnostics: the only diagnostic enabled is the SPI_IGNORE_ERR function.

THEORY OF OPERATION

Note that only a few of the register setting options are shown; this list is just an example. For full register information, see the AD4130-8 Registers section.

POWER-DOWN MODES

The AD4130-8 has multiple power-down modes that can be selected using the MODE bits in the ADC_CONTROL register (see Table 47). The MODE bits also select the different ADC conversion modes. In Table 42, only the power-down mode options are listed.

Table 42. Power-Down Mode Options

MODE	ADC Conversion Mode
0b0010	Standby
0b0011	Power-down
0b0100	Idle

Power-Down Mode

Power-down mode is the lowest power mode of the AD4130-8. All blocks are powered down, with no register information retained. To go to power-down mode, the device must be in standby mode. Otherwise, the device goes to continuous conversion mode. This procedure serves as a safety feature to prevent accidental/unwanted transitions to power-down mode.

To exit power-down mode, the user must reset the device. See the Device Reset section.

Idle Mode

The modulator and digital filter are held in reset in idle mode. All user registers retain their content as previously configured. Note that in idle mode, there is no significant change in current consumption with respect to continuous conversion mode.

To exit idle mode, write to the MODE bits in the ADC_CONTROL register to select a different mode of operation.

Standby Mode

In standby mode and in standby during duty cycling, the register contents are retained, and the RDYB bit in the status register (see Table 48) is set to 1. The same standby signal can be driven to the P4 pin (AIN5) by setting the STBY_OUT_EN bit in the MISC register to 1.

In the MISC register, the user can select which functionality is kept enabled in standby mode, as follows:

- The diagnostic functionality can be kept enabled by setting the STBY_EN_DIAGNOSTICS bit to 1. Some diagnostics also require the internal oscillator to be enabled. Therefore, if those errors are enabled in the ERROR_EN register and STBY_EN_DIAGNOSTICS = 1, the internal oscillator is kept enabled.
- The GPO signals can be kept enabled by setting the STBY_GPO_EN bit to 1.
- The power-down switch can be kept enabled by setting the STBY_PDSW_EN bit to 1.
- The burnout currents can be kept enabled by setting the STBY_BURNOUT_EN bit to 1.
- The VBIAS can be kept enabled by setting the STBY_VBIAS_EN bit to 1.
- The excitation currents can be kept enabled by setting the STBY_IEXC_EN bit to 1.
- The internal reference can be kept enabled by setting the STBY_REFHOL_EN bit and the STBY_INTREF_EN bit to 1.

To exit standby mode, write to the MODE bits in the ADC_CONTROL register to select a different mode of operation. See the Out of Standby Mode Timing section for further details.

DIGITAL INTERFACE

The AD4130-8 has a 4-wire ($\overline{CS}$, SCLK, DIN, and DOUT) or 3-wire (SCLK, DIN, and DOUT) SPI that is compatible with QSPI™ and MICROWIRE™ interface standards, as well as most digital signal processors (DSPs). The interface operates in SPI Mode 3 and can be operated with $\overline{CS}$ tied low (3-wire). In SPI Mode 3, SCLK idles high, the falling edge of SCLK is the drive edge, and the rising edge of SCLK is the sample edge as described in Figure 73. This means that data on DIN is clocked in on the rising edge of SCLK, and data on DOUT is clocked out on the falling edge of SCLK. To readback DOUT, use the rising edge of SCLK or follow the t_{DOUT_VALID} timing to sample the DOUT signal. The SCLK pin has a Schmitt-triggered input, making the interface suitable for opto-isolated applications. Additional interface pins are INT (WLCSP models only) and $\overline{SYNC}$.

Timing specifications can be found in Table 9 and Table 10.

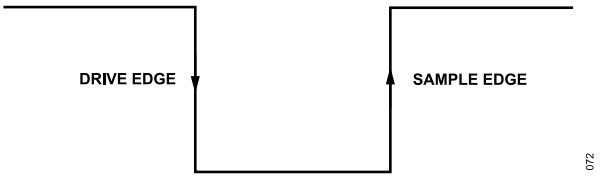


Figure 73. SPI Mode 3, SCLK Edges

The logic level of the AD4130-8 digital interface is set by the IOV_{DD} voltage, and can range from 1.65 V to 3.6 V.

ACCESSING THE REGISTER MAP

The communications register (COMMS) controls access to the full register map of the ADC. This register is an 8-bit, write only register (see Table 43). On power-up or after a software reset, the digital interface defaults to a state where it expects a write to the communications register. Therefore, all communications to the device must start with a write operation to the communications register.

The data written to the communications register determines whether the next operation is a read or write operation (R/$\overline{W}$ bit), and which register is accessed (RS, Bits[5:0]). The MSB in the 8-bit COMMS register must be set to 0 to enable a write ($\overline{WEN}$ bit). If $\overline{WEN}$ is set to 1 during the transaction, the device does not clock on to subsequent bits in the register.

In situations where the interface synchronization is lost, if $\overline{CS}$ is used, returning $\overline{CS}$ high resets the digital interface to its default state and aborts any current operation. This operation does not reset the device registers to their default value (see the Device Reset section).

When the read or write operation to the selected register is complete, the interface returns to its default state, where it expects a write operation to the communications register.

Figure 74 and Figure 75 show writing to and reading from a register by first writing the 8-bit command to the communications register, followed by the data for the addressed register. The data length on DOUT varies from 8-bit, 16-bit, 24-bit, and 32-bit, depending on the register selected and the SPI CRC being enabled.

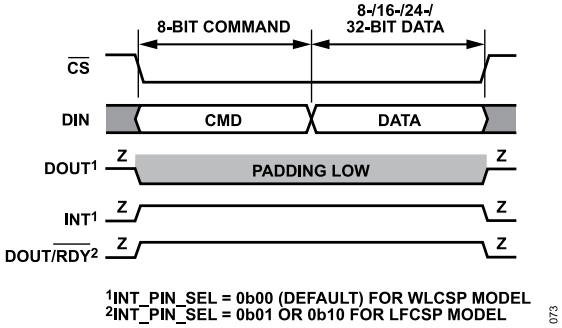


Figure 74. Writing to a Register (8-Bit Command with Register Address Followed by Data)

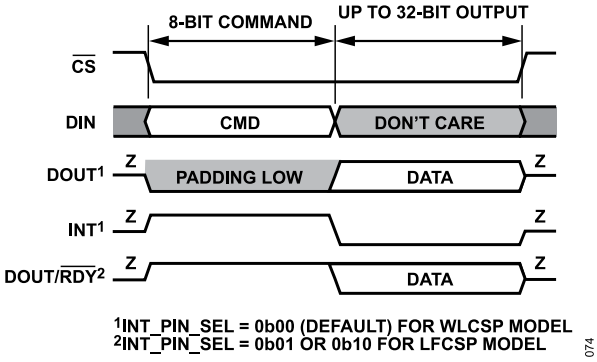


Figure 75. Reading from a Register (8-Bit Command with Register Address Followed by Data)

Device Identification

Reading the ID register is the recommended method for verifying the correct communication with the device. The ID register is a read-only register. The communication register and ID register details are described in Table 44 and in the Identification Register section.

Table 43. Communications Register

Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x00	COMMS	[7:0]	$\overline{WEN}$	R/$\overline{W}$	RS[5:0]						0x00	W

Table 44. ID Register

Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x05	ID	[7:0]	RESERVED				SILICON_ID		MODEL_ID		0x0X[1]	R

DIGITAL INTERFACE

[1] See Identification Register section for details.

DEVICE RESET

The circuitry and serial interface of the AD4130-8 can be reset by writing 64 consecutive 1s to the device. This action resets the logic, the digital filter, and the analog modulator, and all on-chip registers are reset to their default values. A reset is useful if the serial interface becomes asynchronous due to noise on the SCLK line.

Figure 76 shows a software reset timing diagram.

The AD4130-8 requires a minimum delay between any reset event and a register read/write transaction.

This delay is shown in Figure 76, and represented by t_{RESET_DELAY} in Table 9. If the digital host attempts to perform an SPI transaction before the device is ready, the transaction may not succeed and the SPI_IGNORE_ERR bit in the error register is set. The SPI_IGNORE_ERR is a read and write 1 to clear (R/W1C) type of bit. The POR_FLAG bit in the status register (see Table 48) is set to 1 when the reset is initiated, and then is set to 0 when the bit is read.

A reset is automatically performed at power-up as shown in Figure 72.

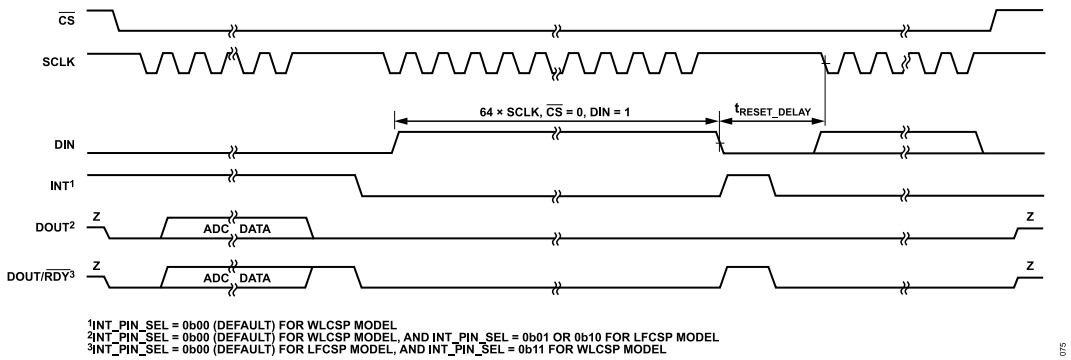


Figure 76. Software Reset Timing Diagram

ADC CONFIGURATION AND OPERATIONS

The AD4130-8 is flexible in its configurability and modes of operations.

BIPOLAR/UNIPOLAR CONFIGURATION

The analog inputs to the AD4130-8 can accept either unipolar or bipolar input voltage ranges. Unipolar and bipolar signals on the AINP input are referenced to the voltage on the AINM input. The input voltages on AINP and AINM need to be between AV_{DD} and AV_{SS}, following the specifications in Table 2.

Data Output Coding

The bipolar bit in the ADC_CONTROL register (see Table 47) determines the data output coding of the ADC data, and how the device applies the offset and gain coefficients in the postprocessing. See the ADC Calibration section.

By default, the bipolar bit is set to 1, which corresponds to offset binary coding. This configuration is better used to represent bipolar input voltages from $-V_{REF}$/gain to V_{REF}/gain. If the bipolar bit is set to 1 for a unipolar input configuration, the input (AINP − AINM with AINP ≥ AINM) is represented by an output code between 0x800000 (zero scale) and 0xFFFFFF (full scale).

When the bipolar bit is set to 0, the data output coding changes to natural (straight) binary. This configuration is better used to represent unipolar input voltages from 0 V to V_{REF}/gain. If the bipolar bit is set to 0 for a bipolar input configuration, all cases where AINP < AINM are clamped at 0x000000 (zero scale).

Note that the value of the bipolar bit also affects the way the device interprets threshold values in the FIFO settings.

Table 45 shows the data output coding options and respective output code equations for any analog input voltage.

Table 45. ADC Data Output Coding Options

Bipolar Bit	Data Output Coding	Output Code Equation[1]
0b0	Straight binary	$Code = (2^N \times V_{IN} \times Gain)/V_{REF}$
0b1 (default)	Offset binary	$Code = 2^{N-1} \times ((V_{IN} \times Gain/V_{REF}) + 1)$

[1] $N = 24$, V_{IN} is the differential input voltage, and *Gain* is the gain setting (1 to 128).

Table 46 shows the expected correspondence between input signals and the relative output coding depending on the choice for the bipolar bit in the ADC_CONTROL register.

Table 46. Ideal Output Codes for a Given Input Differential Signal

AINP − AINM	Bipolar Bit = 0b0	Bipolar Bit = 0b1
Negative Full Scale	0x000000	0x000000
Zero Scale	0x000000	0x800000
Mid Scale	0x800000	N/A[1]
(Positive) Full Scale	0xFFFFFF	0xFFFFFF

[1] N/A means not applicable.

STATUS BITS

The contents of the status register (see Table 48) can be appended to each conversion on the AD4130-8. This function is useful if several channels are enabled. Each time a conversion is output, the contents of the status register are appended and the format for reading the data register becomes: DATA[23:0], STATUS[7:0]. The four LSBs of the status register (CH_ACTIVE bitfield) indicate to which channel the conversion corresponds. In addition, check the POR_FLAG bit and determine if any errors are being flagged through the MASTER_ERR bit. To append the status register contents to every conversion, set the DATA_STATUS bit in the ADC_CONTROL register to 1 (see Table 47).

Table 47. ADC_CONTROL Register

Addr.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x01	ADC_CONTROL	[15:8]	RESERVED	BIPOLAR	INT_REF_VAL	DOUT_DIS_DEL	CONT_READ	DATA_STATUS	CSB_EN	INT_REF_EN	0x4000	R/W
		[7:0]	RESERVED	DUTY_CYC_RATIO	MODE				CLK_SEL			

Table 48. Status Register

Addr.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x00	STATUS	[7:0]	$\overline{RDY}$	MASTER_ERR	RESERVED	POR_FLAG	CH_ACTIVE				0x10	R

Table 49. CHANNEL_m Register (m = 0 to 15)

Addr.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x09 to 0x18	CHANNEL_m (m = 0 to 15)	[23:16]	ENABLE_m	SETUP_m			PDSW_m	THRES_EN_m	AINP_m[4:3]		0xXXXXXX[1]	R/W
		[15:8]	AINP_m[2:0]			AINM_m						
		[7:0]	I_OUT1_CH_m				I_OUT0_CH_m					

ADC CONFIGURATION AND OPERATIONS

[1] The CHANNEL_0 default value is 0x800100. The default value of all other channels is 0x000100.

SMART CHANNEL SEQUENCER

The AD4130-8 allows up to 16 channels to be configured and enabled in the CHANNEL_m registers. Each enabled channel becomes part of an automatic sequence that can be left running while the host processor sleeps.

The CHANNEL_m registers allow the user to do the following:

- Select the plus and minus inputs (AINP_m and AINM_m bitfields)
- Assign the excitation currents to specific pins (I_OUT0_CH_m and I_OUT1_CH_m bitfields)
- Select the ADC setup (SETUP_m bitfield)
- Enable the power-down switch and thresholds (PDSW_m and THRES_EN_m bitfields)
- Enable the channel to become part of the sequence (ENABLE_m bitfield).

See Table 49 for details.

When multiple channels are enabled with different configurations selected, the AD4130-8 automatically cycles through the channels in all conversion modes. Sequencing starts from the lowest enabled channel in increasing order up to the largest enabled channel. When each enabled channel is selected, the time required to start the first conversion is equal to the front-end settling time for the selected channel (SETTLE_n bits in the FILTER_n register). See Figure 95 for an example.

ADC Setups

For each channel, a predefined ADC setup can be selected (SETUP_m bits in the CHANNEL_m registers). The AD4130-8 allows up to eight different ADC setups, with each ADC setup consisting of configuration, filter, gain, and offset settings.

For example, SETUP_m = 0 (ADC Setup 0) consists of the CONFIG_0 register, FILTER_0 register, OFFSET_0 register, and GAIN_0 register. Figure 77 shows the grouping of these registers. Table 50 through Table 53 show the four registers that are associated with each ADC setup.

Table 50. CONFIG_n Register (n = 0 to 7)

Addr.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x19 to 0x20	CONFIG_n (n = 0 to 7)	[15:8]	I_OUT1_n			I_OUT0_n			BURNOUT_n		0x0000	R/W
		[7:0]	REF_BUFP_n	REF_BUFM_n	REF_SEL_n		PGA_n			PGA_BYP_n		

Table 51. FILTER_n Register (n = 0 to 7)

Addr.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x21 to 0x28	FILTER_n (n = 0 to 7)	[23:16]	SETTLE_n			REPEAT_n					0x002030	R/W
		[15:8]	FILTER_MODE_n				RESERVED	FS_n[10:8]				
		[7:0]	FS_n[7:0]									

Table 52. OFFSET_n Register (n = 0 to 7)

Addr.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x29 to 0x30	OFFSET_n (n = 0 to 7)	[23:16]	OFFSET_n[23:16]								0x800000	R/W
		[15:8]	OFFSET_n[15:8]									
		[7:0]	OFFSET_n[7:0]									

Table 53. GAIN_n Register (n = 0 to 7)

Addr.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x31 to 0x38	GAIN_n (n = 0 to 7)	[23:16]	GAIN_n[23:16]								0xXXXXXX	R/W
		[15:8]	GAIN_n[15:8]									
		[7:0]	GAIN_n[7:0]									

ADC CONFIGURATION AND OPERATIONS

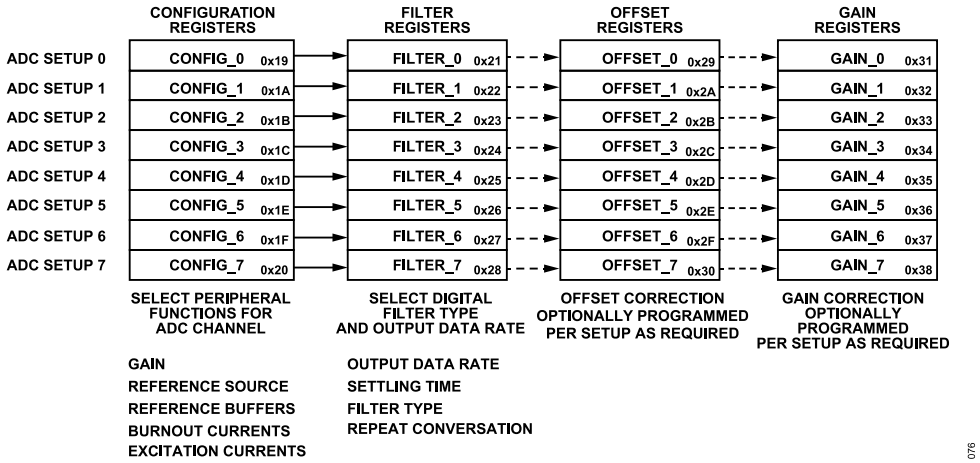


Figure 77. ADC Setup Register Grouping

Configuration Registers

The CONFIG_n registers allow the user to do the following:

- Set the PGA gain (PGA_n bitfield)
- Set the PGA mode (PGA_BYP_n bitfield)
- Select the reference source (REF_SEL_n bitfield)
- Enable the reference buffers (REF_BUFP_n and REF_BUFM_n bitfields)
- Enable and select the burnout currents (BURNOUT_n bitfield)
- Enable and select the excitation currents (I_OUT1_n and I_OUT2_n bitfields)

See Table 50 for details.

Filter Registers

The FILTER_n registers allow the user to do the following:

- Select the digital filter at the output of the ADC modulator (FILTER_MODE_n bitfield)
- Select the FS value applied to the filter (FS_n, Bits[10:0])
- Select how many times to convert on this ADC setup, from 1 to 32 times (REPEAT_n bitfield)
- Set the front-end settling time (SETTLE_n bitfield), to allow the sensor output to reach a settled value before conversion starts.

See Table 51 for details.

Offset and Gain Registers

Offset and gain settings are used to make adjustments to the data output after a calibration on the channel associated to that ADC setup is performed. Programming the gain and offset registers is optional for any use case, as indicated by the dashed lines between the register blocks in Figure 77. If an internal or system offset or full-scale calibration is performed, the gain and offset registers for the selected channel are automatically updated. See the ADC Calibration section for more details. See Table 52 and Table 53.

ADC CONVERSION MODES

There are multiple conversion modes available on the AD4130-8 that can be selected using the MODE bits in the ADC_CONTROL register (see Table 47). The MODE bits also select the different power-down modes. In Table 54, only the ADC conversion mode options are listed.

Table 54. ADC Conversion Mode Options

MODE	ADC Conversion Mode
0b0000 (Default)	Continuous conversion
0b0001	Single sequence
0b1001	Duty cycling
0b1010	Single sequence + idle by $\overline{\text{SYNC}}$
0b1011	Single sequence + STBY by $\overline{\text{SYNC}}$

Continuous Conversion Mode

Continuous conversion mode is the default mode. The ADC continuously converts on each enabled channel. When the sequence is complete, the ADC starts again with the lowest enabled channel.

Single Sequence Modes

In single sequence mode, the AD4130-8 performs a single sequence of conversions and is placed in standby mode after the conversions are complete. If more than one channel is enabled, the ADC automatically sequences through the enabled channels once, before entering standby mode. Select MODE = 0b0001 to enable the single sequence mode. When the AD4130-8 is converting in single sequence mode, SPI writes are ignored.

The single sequence conversion can also be controlled externally using the $\overline{\text{SYNC}}$ pin. Select MODE = 0b1010 in the ADC_CONTROL register to enable the single sequence + idle by $\overline{\text{SYNC}}$ mode. In this mode, the $\overline{\text{SYNC}}$ pin can be pulsed low to take the device out of idle mode and initiate a new single sequence. In idle mode, the modulator and digital filter are held in reset.

ADC CONFIGURATION AND OPERATIONS

Select MODE = 0b1011 in the ADC_CONTROL register to enable the single sequence + STBY by $\overline{\text{SYNC}}$ mode. In this mode, the SYNC pin can be pulsed low to take the device out of standby and initiate a new sequence of conversions. In standby, the register content is retained. When in single sequence + standby by $\overline{\text{SYNC}}$ mode, the REPEAT_n bits functionality is available. See the System Synchronization section.

Note that the time in between $\overline{\text{SYNC}}$ pin pulses must be greater than the single sequence conversions time to allow the device to go into idle or standby mode in between $\overline{\text{SYNC}}$ pin pulses and avoid timing issues, as shown in Figure 78 or Figure 80. The $\overline{\text{SYNC}}$ pin rate can be used to determine the sample rate per channel in the sequence. See the System Synchronization section.

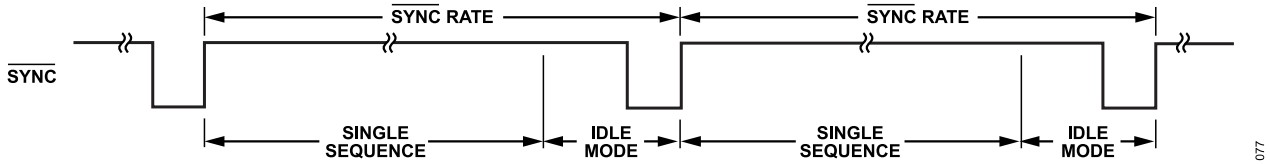


Figure 78. Example of Single Sequence + Idle by $\overline{\text{SYNC}}$ Mode Diagram

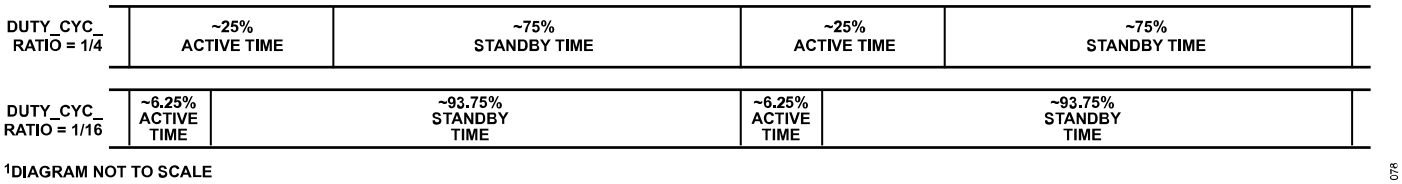


Figure 79. Duty Cycling Mode Diagram

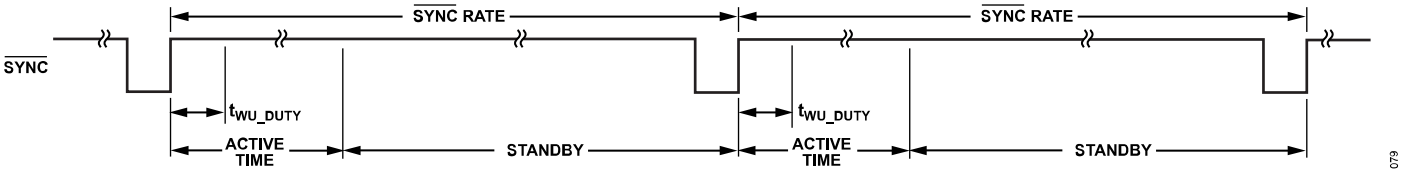


Figure 80. Example of Single Sequence + STBY by $\overline{\text{SYNC}}$ Mode Diagram

ADC CONFIGURATION AND OPERATIONS

Duty Cycling Mode

In duty cycling mode, the device continuously cycles autonomously between active and standby modes for added savings in power consumption. The ADC converts on each enabled channel and then enters standby mode. When a cycle is complete, the cycle begins again with an ADC conversion on the lowest enabled channel. Set the MODE bitfield in the ADC_CONTROL register to 1001 to enable autonomous duty cycling mode. In this mode, the duty cycling ratio is set to 1/4 by default, which means that the device is active ~25% of the time and in standby the rest of the time. The autonomous duty cycle ratio can be changed to 1/16 by setting the DUTY_CYC_RATIO bitfield value in the ADC_CONTROL register to 1. See Figure 79.

When in duty cycling mode, the REPEAT_n bits functionality is not available. See the Duty Cycling Mode Timing section.

When using the internal reference for conversions on some or all of the channels in the duty cycling sequence, it is recommended to set the STBY_REFHOL_EN bit to 1 in the MISC register, to reduce the impact of the internal reference continuously turning on and off. See the Standby Mode section for more details on the blocks that can be kept active when in standby during duty cycling.

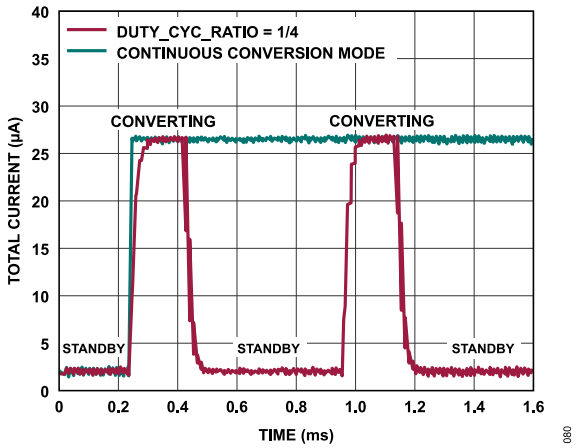


Figure 81. Example of Duty Cycling Mode vs. Continuous Conversion Mode Current Consumption

DATA READY SIGNAL

When an ADC conversion completes, the RDYB bit in the status register (see Table 48) changes from 1 to 0. A data ready signal indicating that the ADC result is in the data register and ready to be readback can also be generated internally and directed to a pin of choice by configuring the INT_PIN_SEL bits in the IO_CONTROL register (see Table 41), as per Table 55. By default, the AD4130-8 for the LFCSP devices, the data output pin shares this functionality (DOUT/$\overline{\text{RDY}}$) while the WLCSP has a dedicated INT pin for the data ready signal. The data ready signal returns high after a read of the ADC.

Table 55. Ready Interrupt Pin Options[1]

INT_PIN_SEL	LFCSP	WLCSP
0b00 (Default)	DOUT/$\overline{\text{RDY}}$	INT
0b01	CLK	CLK
0b10	P2	P2
0b11	DOUT/$\overline{\text{RDY}}$	DOUT[2]

[1] FIFO disabled. When the FIFO is enabled, the INT_PIN_SEL bitfield is used to assign the selected FIFO interrupt to a pin as per Table 72.

[2] Pin behaves as a shared DOUT and data ready signal functionality.

If the ADC result in the data register is not read, the data ready signal stays low until the next conversion is about to become available. The minimum data ready high time if data ready is low and the next conversion is available is called t_{RDYH} and can be found in Table 9 and Figure 9.

When the continuous read mode is disabled (see the Continuous Read Mode section) the same data can be read again, if required, while the data ready signal is high, although subsequent reads must not occur close to the next output update. When continuous read mode is enabled, an ADC result can be read only once.

Configuring a pin as a data ready interrupt takes priority over other pin control on that pin. For example, enabling the CLK pin as CLK via the CLK_SEL bit in the ADC_CONTROL register (see Table 47) is ignored if the CLK pin is enabled as interrupt.

Enabling the P2 pin as a GPO via the GPO_CTRL_P2 bit in the IO_CONTROL register is ignored if P2 is enabled as an interrupt. When P2 is enabled as a data ready signal, all GPO pins are automatically kept enabled in standby mode.

When the FIFO is enabled, the data ready signal becomes a FIFO ready signal that refers to the FIFO being ready to be read (low) or busy while being accessed by the device (high). This signal appears automatically on DOUT (WLCSP) or DOUT/$\overline{\text{RDY}}$ (LFCSP) when the FIFO is enabled and cannot be redirected to other pins. See the FIFO Ready Signal section.

CONTINUOUS READ MODE

Continuous read mode is a different interface mode to access ADC data. In continuous read mode, it is not required to write to the COMMS register to read the data register. In this mode, the data ready signal acts as a framing signal for the output data. SCLKs are ignored until the data ready signal goes low to indicate the end of a conversion. Apply the required number of SCLKs after the data ready signal goes low to read the conversion result in the data register. When the conversion result is read, the data ready signal returns high until the next conversion result is available. In this mode, the data can be read only once. Ensure that each sample data is read before the next conversion is complete. If the user has not read the previous conversion result before the completion of the next conversion, or if insufficient serial clocks are applied to read the result, the serial output register is reset when the next

ADC CONFIGURATION AND OPERATIONS

conversion is complete, and the new conversion result is placed in the output serial register.

To enable continuous read mode, set the CONT_READ bit in the ADC_CONTROL register (see Table 47). When this bit is set, the only serial interface operations possible are reads from the data register. Therefore, the write to this register is the last in the sequence of configuration writes to the device.

To exit continuous read mode, write a read data command (0x42) while the data ready signal is low. If CRC is enabled, a presumed CRC command byte of 0x42 precedes the data and must be considered when validating CRC, but no CRC is needed when sending the 0x42 command. Alternatively, to exit continuous read mode, apply a software reset, that is, 64 SCLKs with $\overline{CS}$ = 0 and DIN = 1 (see Figure 76). This resets the ADC and all register contents. These are the only commands that the interface recognizes after it is placed in continuous read mode. DIN must be held low in continuous read mode until an instruction is to be written to the device.

If multiple ADC channels are enabled, each channel is output in turn, with the status register content being appended to the data if DATA_STATUS bit is set in the ADC_CONTROL register. The status register includes the channel to which the conversion corresponds.

The continuous read mode is disabled when the FIFO is enabled.

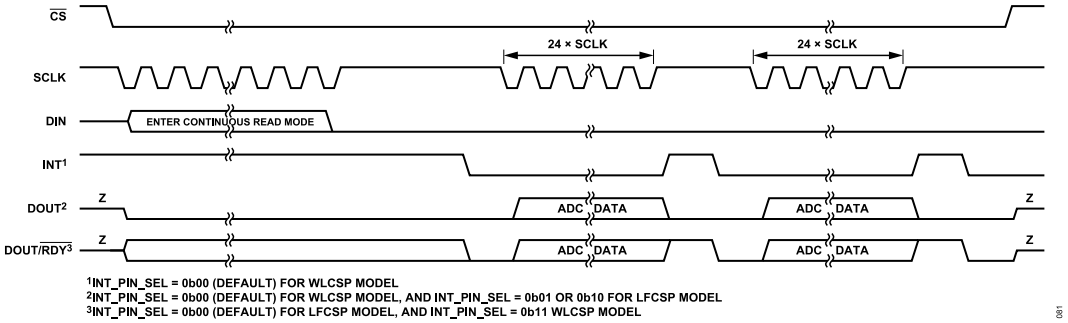


Figure 82. Enter Continuous Read Mode Diagram (DATA_STATUS = 0)

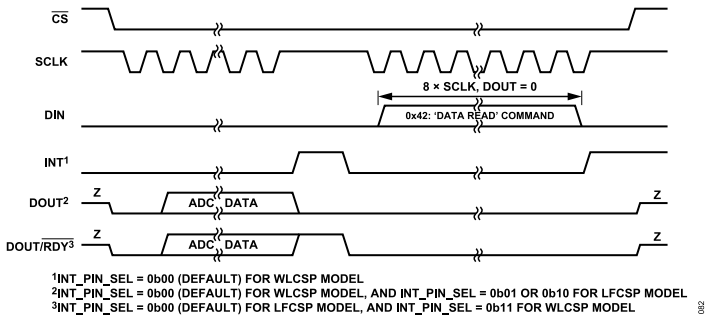


Figure 83. Exit Continuous Read Mode Diagram (CRC Disabled)

ADC CONFIGURATION AND OPERATIONS

SYSTEM SYNCHRONIZATION

The $\overline{SYNC}$ pin input can facilitate several operations. By default, if held low, this pin can keep the modulator, the digital filter, and the calibration control logic in a reset state, without affecting any of the configuration conditions on the device. This allows the user to start gathering samples of the analog input from a known point in time, that is, the rising edge of $\overline{SYNC}$. Take $\overline{SYNC}$ low for at least t_{SYNC_PW} to implement the synchronization function (see the Timing Specifications section). $\overline{SYNC}$ does not affect the digital interface but does reset the data ready signal to a high state if it is low. A falling edge on the $\overline{SYNC}$ pin resets the digital filter and the analog modulator and places the AD4130-8 into a consistent, known state. While the $\overline{SYNC}$ pin is low, the AD4130-8 is maintained in this state. On the $\overline{SYNC}$ rising edge, the modulator and filter exit this reset state, and the device starts to gather input samples again. The $\overline{SYNC}$ pin is sampled on the falling edge of MCLK. Therefore, for applications where deterministic timing is required, it is recommended that the $\overline{SYNC}$ pin changes value on the external MCLK (CLK) rising edge.

Initiate Conversions

The $\overline{SYNC}$ pin can be used as a start conversion command. Hold $\overline{SYNC}$ pin low at power-up and while configuring the AD4130-8. Then, when ready, use the rising edge of $\overline{SYNC}$ to start the conversion or series of conversions depending on the ADC mode selected. The falling edges of the data ready signal indicate when each conversion is complete, and the ADC result can be read from the data register.

Synchronize Multiple AD4130-8 Devices

The $\overline{SYNC}$ pin can be used to synchronize multiple AD4130-8 devices operated from a common external MCLK, so that their data registers are updated simultaneously. This functionality is available at power-up by default. A low pulse on the $\overline{SYNC}$ pin connected to multiple devices is normally issued after each AD4130-8 performs its own calibration or has calibration coefficients loaded into its calibration registers. The conversions from the AD4130-8 devices are then synchronized.

The device exits reset on the MCLK falling edge following the $\overline{SYNC}$ low to high transition. Therefore, when multiple devices are being synchronized, pull the $\overline{SYNC}$ pin high on the MCLK rising edge to ensure that all devices begin sampling on the MCLK falling edge. If the $\overline{SYNC}$ pin is not taken high in sufficient time, it is possible to have a difference of one master clock cycle between the devices; that is, the instant at which conversions are available differs from device to device by a maximum of one master clock cycle.

Other Synchronization Modes

The $\overline{SYNC}$ pin functionality can be changed to take the device out of idle when in single sequence + idle by $\overline{SYNC}$ mode, or take the device out of standby when in single sequence + STBY by $\overline{SYNC}$ mode. See the ADC Conversion Modes section for more details.

The $\overline{SYNC}$ pin can also be used to clear the FIFO instead by setting the SYNCB_CLEAR bit in the IO_CONTROL register to 1 (see Table 41). See the Clearing the FIFO section for more details.

ADC CALIBRATION

After each conversion, the ADC conversion result is scaled using the ADC calibration coefficients stored in the OFFSET_n and GAIN_n registers before being written to the data register. The postprocessing time needed for this activity is called digital postprocessing (DPP) time. The default value of the OFFSET_n registers is 0x800000 and the nominal value of the GAIN_n registers is 0x555555.

Both internal calibration and system calibration are available in the AD4130-8 to update the OFFSET_n and GAIN_n registers; therefore, the user has the option of removing offset or gain errors internal to the device only and removing the offset or gain errors of the complete end system.

The AD4130-8 provides four calibration modes as shown in Table 56 that can be used to eliminate the offset and gain errors on a per ADC setup basis.

Table 56. ADC Calibration Mode Options

MODE	ADC Calibration Mode
0b0101	Internal offset calibration (zero scale)
0b0110	Internal gain calibration (full scale)
0b0111	System offset calibration (zero scale)
0b1000	System gain calibration (full scale)

An internal or system offset calibration reduces the offset error to the order of the noise. The gain error is factory calibrated at ambient temperature and at a gain of 1 with PGA_BYP_n = 0. Therefore, internal gain calibrations at a gain of 1 with PGA_BYP_n = 0 are not supported on the AD4130-8. For other gain values, a system gain calibration reduces the gain error to the order of the noise.

Only one channel can be active during calibration. From an operational point of view, treat a calibration like another ADC conversion. Set the system software to monitor the RDYB bit in the status register (see Table 48) or the data ready signal to determine the end of a calibration via a polling sequence or an interrupt driven routine. To start a calibration, write the relevant value to the MODE bits in the ADC_CONTROL register (see Table 47). The data ready signal goes high and the RDYB bit in the status register is set to 1 when the calibration initiates. When the calibration is complete, the content of the corresponding OFFSET_n or GAIN_n registers is updated, the RDYB bit in the status register is set to 0, the data ready signal returns low (if $\overline{CS}$ is low), and the AD4130-8 reverts to idle mode.

A calibration can be performed at any output data rate. Using lower output data rates results in better calibration accuracy also for higher output data rates. A new calibration is required for a

given channel if the reference source or the gain for that channel is changed (using the PGA_n bitfields of the CONFIG_n registers).

The following equations show the calculations that are used to scale data based on offset and gain calibration coefficients.

In unipolar mode (bipolar bit = 0b0 in the ADC_CONTROL register):

$$DATA = \left(\frac{0.75 \times V_{IN}}{V_{REF}} \times 2^{N-1} - (OFFSET_n - 0x800000)\right) \times \frac{GAIN_n}{0x400000} \times 2$$

In bipolar mode (bipolar bit = 0b1 in the ADC_CONTROL register):

$$DATA = \left(\frac{0.75 \times V_{IN}}{V_{REF}} \times 2^{N-1} - (OFFSET_n - 0x800000)\right) \times \frac{GAIN_n}{0x400000} + 0x800000$$

where:
DATA is the code written in the data register after postprocessing.
V_{IN} is the differential voltage at the input of the converted channel (AINP − AINM).
N is the number of bits of the ADC (24).
OFFSET_n is the hexadecimal code written in the relative OFFSET_n register of the converted channel.
GAIN_n is the hexadecimal code written in the relative GAIN_n register of the converted channel.

The AD4130-8 provides the user with access to the on-chip calibration registers, allowing the microprocessor to read the calibration coefficients of the device or to write its own calibration coefficients. A read or write of the OFFSET_n and GAIN_n registers can be performed at any time except during an internal or system calibration. The values in the calibration registers are 24 bits wide. The input span and offset of the device can also be manipulated using these registers. See the System Calibration Span and Offset Limits section for more details.

The AD4130-8 can run background checks during calibration. To enable this functionality, set the ADC_ERR_EN bit in the ERROR_EN register to 1. If an error occurs, the ADC_ERR bit in the error register is set. See the ADC Errors section for more details.

If the user is concerned about verifying that a valid reference is in place every time a calibration is performed, check the status of the REF_DETECT_ERR bit at the end of the calibration cycle.

Internal Gain Calibration

To perform an internal gain calibration, a full-scale input voltage generated internally, is automatically connected to the PGA inputs. A gain calibration is recommended each time the gain of a channel is changed to minimize the full-scale error caused by the new gain setting. When performing internal calibrations, the internal gain calibration must be performed before the internal offset calibration. Therefore, write the value 0x800000 to the OFFSET_n register of the selected channel before performing the internal gain calibration, which ensures that the OFFSET_n register is at its default value. If the reference voltage is higher than 2 V, set the CAL_RANGE_X2 bit in the MISC register to 1 to improve the outcome of the internal gain calibration. The AD4130-8 is factory calibrated at ambient temperature and with a gain of 1 with PGA_BYP_n = 0, and the resulting gain coefficients are loaded to the GAIN_n registers of the device as default value. The device does not support further internal gain calibrations at a gain of 1 (PGA_BYP_n = 0). An internal gain calibration requires a time equal to four first conversions of the selected configuration on that channel to be completed.

Internal Offset Calibration

During an internal offset calibration, the selected positive analog input pin is disconnected, and it is connected internally to the selected negative analog input pin. For this reason, it is necessary to ensure that the voltage on the selected negative analog input pin does not exceed the allowed limits and is free from excessive noise and interference. When performing internal calibrations, the internal gain calibration must be performed before the internal offset calibration. An internal offset calibration requires a time equal to the first conversion of the selected configuration on that channel to be completed.

System Offset Calibration

A system offset calibration expects the system zero-scale voltages to be applied to the ADC pins before enabling the calibration mode. As a result, offset errors external to the ADC are removed. When performing system calibrations, system offset calibration must be performed before the system gain calibration. Internal calibrations must be performed before completing system calibrations. A system offset calibration requires a time equal to the first conversion of the selected configuration on that channel to be completed.

System Gain Calibration

A system gain calibration expects the system full-scale voltages to be applied to the ADC pins before enabling the calibration mode. As a result, gain errors external to the ADC are removed. When performing system calibrations, system offset calibration must be performed before the system gain calibration. Internal calibrations must be performed before completing system calibrations. A system gain calibration requires a time equal to the first conversion of the selected configuration on that channel to be completed.

System Calibration Span and Offset Limits

System calibration can be used to compensate for offset or gain errors in the external circuit and to manipulate the input span and offset of the device. Whenever system calibration is performed, the amount of input offset and span adjustments that can be accommodated is limited.

The input span is the difference between the input voltage that corresponds to full code and the input voltage that corresponds

ADC CONFIGURATION AND OPERATIONS

to zero code. The range of input span achievable with system calibration has a minimum value of 0.8 × V_{REF}/gain and a maximum value of 2.1 × V_{REF}/gain.

The input span and offset adjustment must also account for the limitation on the positive full code voltage (1.05 × V_{REF}/gain) and negative zero code voltage (−1.05 × V_{REF}/gain). See Table 2.

Therefore, in determining the limits for system offset (zero scale) and gain (full scale) calibrations, the user must ensure that the offset after adjustment plus the maximum positive span range after adjustment does not exceed 1.05 × V_{REF}/gain.

The amount of offset and span adjustment that can be accommodated depends also on whether the configuration is unipolar or bipolar. This is best illustrated by looking at a few examples.

If the device is used in unipolar configuration (AINP ≥ AINM), with a required span of 0.8 × V_{REF}/gain, the offset range that the system calibration can handle is from −1.05 × V_{REF}/gain to +0.25 × V_{REF}/gain, as shown in Figure 84.

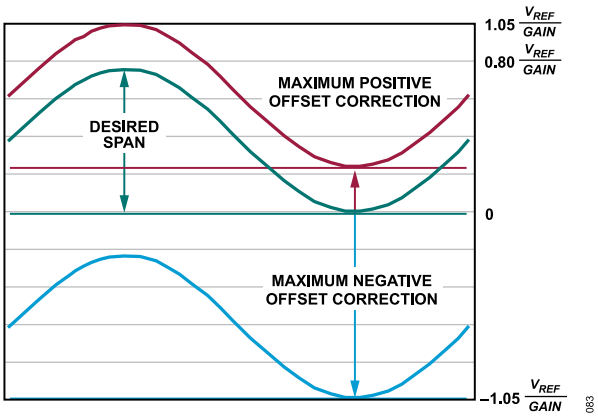


Figure 84. Example of Unipolar Span and Offset Calibration Limits

If the device is used in unipolar configuration with a required span of V_{REF}/gain, the offset range that the system calibration can handle is from −1.05 × V_{REF}/gain to +0.05 × V_{REF}/gain. Similarly, if the device is used in unipolar configuration and required to remove an offset of 0.2 × V_{REF}/gain, the span range that the system calibration can handle is 0.85 × V_{REF}/gain.

If the device is used in bipolar configuration, with a required span of ±0.4 × V_{REF}/gain, the offset range that the system calibration can handle is from −0.65 × V_{REF}/gain to +0.65 × V_{REF}/gain, as shown in Figure 85.

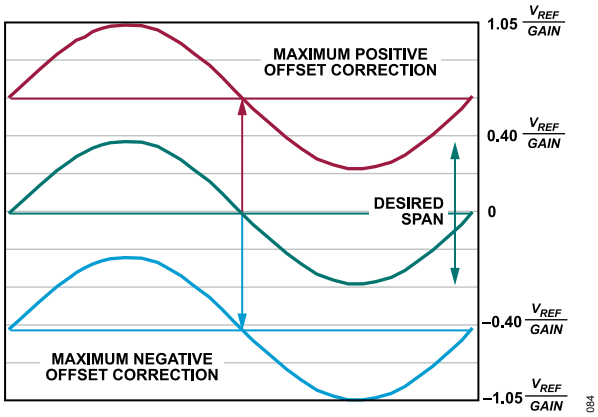


Figure 85. Example of Bipolar Span and Offset Calibration Limits

If the device is used in bipolar configuration with a required span of ±V_{REF}/gain, the offset range the system calibration can handle is from −0.05 × V_{REF}/gain to +0.05 × V_{REF}/gain. Similarly, if the device is used in bipolar configuration and required to remove an offset of ±0.2 × V_{REF}/gain, the span range that the system calibration can handle is ±0.85 × V_{REF}/gain.

DIGITAL FILTERS

The AD4130-8 offers great flexibility in the digital filter scheme. The device has several filter options. The option selected affects the output data rate, first conversion time, input bandwidth, and 50 Hz and 60 Hz rejection. The FILTER_MODE_n bits in each FILTER_n register select between the filter types as shown in Table 58.

Depending on the filter selected, only certain FS values are allowed. The FS value determines the output data rate for all filters except the post filters. See Table 58 for a list of allowed FS values for the correspondent selected filter. See the Output Data Rate section for more details.

SINC^3 AND SINC^4 FILTERS

When the AD4130-8 is powered up, the sinc^3 filter is selected by default. This filter allows the full range of ODR values, gives good noise performance, short first conversion time, and can offer 50 Hz and 60 Hz (±1 Hz) rejection.

A sinc^4 filter can be used instead of the sinc^3 filter. This filter is only available for ODR from 240 SPS to 2.4 kSPS, so it cannot achieve natural 50 Hz and/or 60 Hz rejection, but the filter has excellent noise performance with a slightly longer conversion time.

By programming the correct FS, the sinc standalone filters can achieve good rejection at the respective notch frequency (f_{NOTCH_STD}). The sinc^3 and sinc^4 filters place the first notch at

$$f_{NOTCH_STD} = f_{MCLK}/(32 \times FS[10:0])$$

where:
f_{MCLK} is the master clock frequency (76.8 kHz).
FS[10:0] is the decimal equivalent of the FS_n bits in the FILTER_n register.

AVERAGING FILTERS

In averaging mode, a sinc^1 filter is included after the sinc^3 or sinc^4 filter. The sinc^1 filter averages by 8 (average). Both standalone filters can be used in averaging mode selecting sinc^3 + sinc^1 or sinc^4 + sinc^1 in the FILTER_MODE_n bitfield of the FILTER_n register. The sinc^1 filter places additional notches starting at

$$f_{NOTCH_AVG} = f_{NOTCH_STD}/Avg$$

where:
f_{NOTCH_STD} is the first notch from sinc^3 or sinc^4 standalone filters.
Avg = 8.

In averaging mode, there is almost no difference in the first conversion time on a new channel and subsequent conversions time on the same channel. The conversion time is near constant when converting on a single channel or when converting on several channels using the same filter.

POST FILTERS

The post filters can be applied after the sinc^3 filter to provide rejection of 50 Hz and 60 Hz simultaneously and allow the user to trade off first conversion time and rejection. Each post filter operates at a specific ODR and can achieve simultaneous 50 Hz and 60 Hz rejection, as shown in Table 57. These filters can be selected in each FILTER_MODE_n bitfield. The FS, Bits[10:0] do not influence the ODR when the post filters are selected.

Table 57. Post Filters: Output Data Rate and Rejection

Post Filter	ODR (SPS)	Rejection[1]
1	26.087	53 dB at 50 Hz, 58 dB at 60 Hz
2	24	70 dB at 50 Hz, 70 dB at 60 Hz
3	19.355	99 dB at 50 Hz, 103 dB at 60 Hz
4	16.21	103 dB at 50 Hz, 109 dB at 60 Hz

[1] The 50 Hz/60 Hz rejection is measured with a stable f_{MCLK} = 76.8 kHz, in a band of ±0.5 Hz around 50 Hz and 60 Hz.

Table 58. FILTER_MODE_n Bits and Filter Types

FILTER_ MODE_n	Filter Type	FS Range (Hex)	ODR Range (SPS)	Comments
0000	Sinc^4	0x01 to 0xA (Dec.: 1 to 10)	2400 to 240	Excellent noise performance, long first conversion time, no natural 50/60 Hz rejection. FS > 0d10 is forced to FS = 0d10.
0001	Sinc^4 + sinc^1	0x01 to 0xA (Dec.: 1 to 10)	218.18 to 21.8	Sinc^4 plus averaging by 8 filter. No first conversion delay. FS > 0d10 is forced to FS = 0d10.
0010 (Default)	Sinc^3	0x01 to 0x7FF (Dec.: 1 to 2047)	2400 to 1.17	Good noise performance, moderate 50 Hz/ 60 Hz rejection, moderate first conversion time.
0011	Sinc^3 + REJ60	0x01 to 0x7FF (Dec.: 1 to 2047)	2400 to 1.17	With FS = 0d48, achieves simultaneous 50 Hz and 60 Hz rejection at 50 SPS ODR.
0100	Sinc^3 + sinc^1	0x01 to 0x7FF (Dec.: 1 to 2047)	240 to 0.117	Sinc^3 plus averaging by 8 filter. No first conversion delay. Recommended for FS from 0x01 to 0xCC only (minimum ODR = 1.17).
0101	Sinc^3 + Post Filter 1	Not applicable	26.087	No first conversion delay, good 50 Hz and 60 Hz rejection. FS value does not apply.
0110	Sinc^3 + Post Filter 2	Not applicable	24	
0111	Sinc^3 + Post Filter 3	Not applicable	19.355	
1000	Sinc^3 + Post Filter 4	Not applicable	16.21	

DIGITAL FILTERS

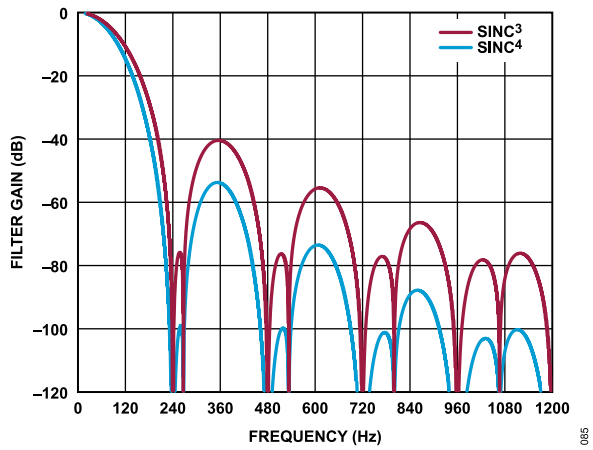


Figure 86. Sinc³ and Sinc⁴ Filter Response (FS = 0d10)

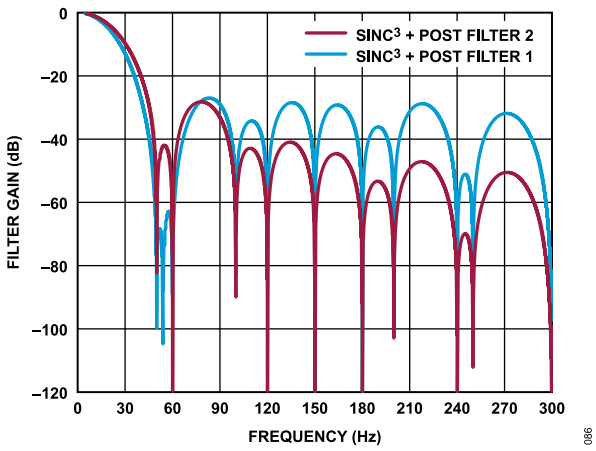


Figure 87. Post Filter 1 and Post Filter 2 Response

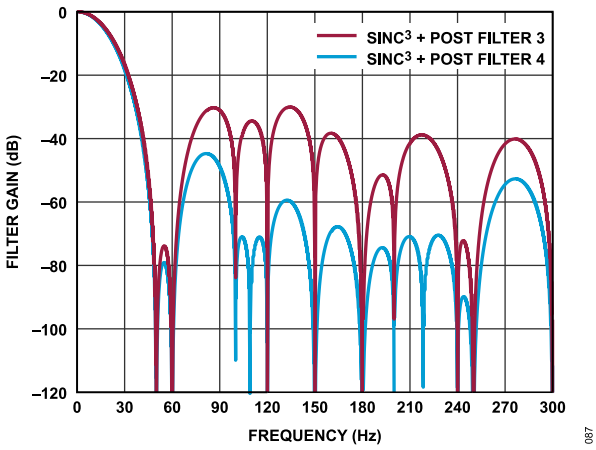


Figure 88. Post Filter 3 and Post Filter 4 Response

OUTPUT DATA RATE

The ODR is the rate at which ADC conversions are available on a single settled channel when the ADC is continuously converting. The ODR corresponds, for example, to the case where the REPEAT_n function (CONFIG_n register) is used, or when in continuous conversion mode with only one channel enabled. When expressed in Hz, the ODR is called f_{ADC} (f_{ADC} = 1 Hz, ODR = 1 SPS), where:

$$f_{ADC} = 1/t_{CNV}$$

where:
t_{CNV} is the conversion time on a settled channel (after the first conversion on a new channel for subsequent conversions on the same channel, that channel is considered settled).
t_{CNV} is also the time between subsequent data ready signal high to low transitions on a settled channel.

The DPP time needed for each conversion is already accounted for in the t_{CNV} for a settled channel.

Table 59. Conversion Time and ODR on Settled Channels

Filter Type	t_{CNV} (MCLK Cycles)[1]	ODR (SPS)[1]
Sinc⁴	32 × FS	2400/FS
Sinc⁴ + sinc¹	352 × FS	218.18/FS
Sinc³	32 × FS	2400/FS
Sinc³ + REJ60	32 × FS	2400/FS
Sinc³ + sinc¹	320 × FS	240/FS
Sinc³ + Post Filter 1	2944	26.087
Sinc³ + Post Filter 2	3200	24
Sinc³ + Post Filter 3	3968	19.355
Sinc³ + Post Filter 4	4736	16.21

[1] FS is the decimal equivalent of the FS, Bits[10:0] binary value.

Filters Bandwidth

The 3 dB bandwidth (f_{3dB}) depends on the type of filter selected and its settings. See the Noise and Resolution section for a list of f_{3dB} values for different FS values. Table 58 lists the allowed FS values for each filter type.

Step Change on a Single Channel

When conversions are performed on a single channel and a step change occurs, the ADC does not detect the change in the analog input straight away, but it continues to output conversions at the programmed output data rate as shown in Figure 89. The filter type determines how many conversions are needed before the output data accurately reflects the analog input.

Table 60 shows the minimum number of conversions needed to settle a step change when converting the same channel. This number applies if the step change is synchronized with the conversion. If the step change occurs while the ADC is processing a conversion, the ADC takes an additional conversion after the step change to generate a fully settled result.

DIGITAL FILTERS

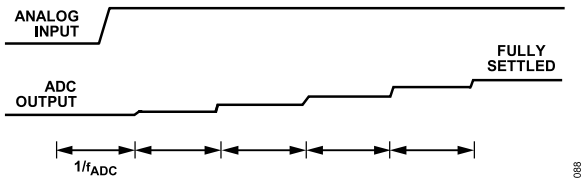


Figure 89. Effect of an Asynchronous Step Change in the Analog Input on the ADC Output

Table 60. Number of Intermediate Conversions Needed to Settle a Step Change when Converting the Same Channel

Filter Type	Minimum	Maximum
Sinc^4	3	4
Sinc^3 and sinc^3 + REJ60	2	3
Sinc^4 + sinc^1 and sinc^3 + sinc^1	1	2
Sinc^3 + post filters	0	1

50 HZ AND 60 HZ REJECTION

By programming the correct FS, the standalone sinc filters can achieve good rejection at the respective notch frequency (f_{NOTCH_STD}). The sinc^4 filter has limited FS options and cannot achieve natural 50 Hz and/or 60 Hz rejection.

See the Rejection Specifications section.

Sinc^3 and Sinc^3 + REJ60 Rejection

By programming the FS to 0d48 for a sinc^3 filter, it is possible to achieve a notch at 50 Hz. ODR in this case is 50 SPS.

Sinc^3 simultaneous 50 Hz/60 Hz rejection is also achieved when FS, Bits[10:0] is set to 0d240. Notches are placed at 10 Hz and multiples of 10 Hz, thereby giving simultaneous 50 Hz and 60 Hz rejection. ODR in this case is 10 SPS. See Table 61 and Figure 90.

Table 61. Sinc^3 Filter Rejection Performance

Filter Type	FS (Dec.)	ODR (SPS)	Rejection (dB)[1]
Sinc^3	240	10	100 (50 Hz and 60 Hz)
	48	50	95 (50 Hz only)
	40	60	98 (60 Hz only)
Sinc^3 + REJ60	48	50	80 (50 Hz)
			65 (60 Hz)

[1] The 50 Hz/60 Hz rejection is measured with a stable f_{MCLK} = 76.8 kHz, in a band of ±1 Hz around 50 Hz and/or 60 Hz.

For the sinc^3 filter, there is the option to select additional rejection by setting FILTER_TYPE to sinc^3 + REJ60 (0b0011). When sinc^3 + REJ60 filter is selected, an additional notch is added at 6/5 of the main notch:

$$f_{NOTCH_REJ60} = 6/5 \times f_{NOTCH_STD}$$

where f_{NOTCH_STD} is the first notch from sinc^3 filter.

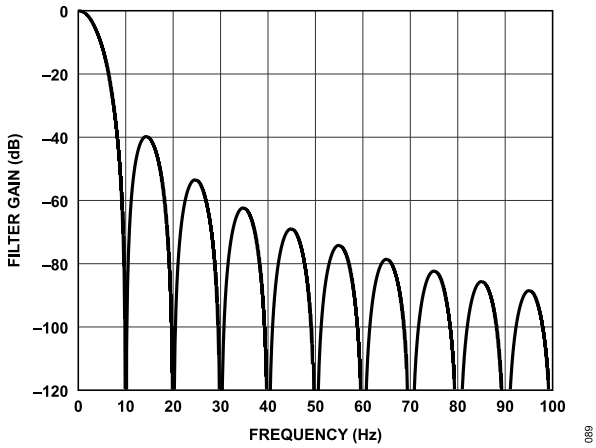


Figure 90. Simultaneous 50 Hz and 60 Hz Rejection for Sinc^3 with ODR = 10 SPS

If the FS value for sinc^3 + REJ60 filter is selected to be 0d48 for an ODR = 50 SPS, the first main notch is a 50 Hz and the first additional notch is at 60 Hz. This configuration allows to achieve simultaneous 50 Hz and 60 Hz rejection. Figure 91 shows the frequency response of the sinc^3 filter with this configuration.

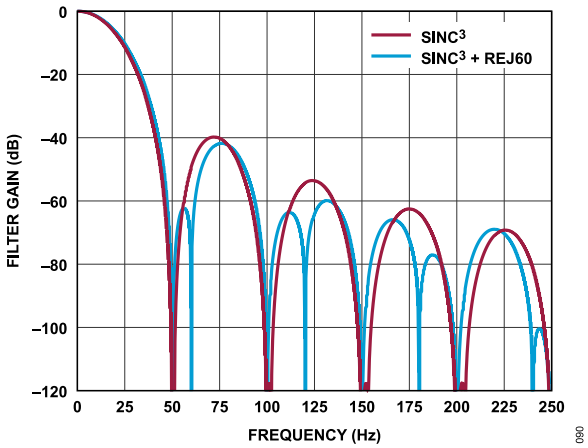


Figure 91. Sinc^3 and Sinc^3 + REJ60 Filter Response (50 SPS ODR)

Post Filters Rejection

Post filters offer good simultaneous rejection at 50 Hz and 60 Hz. See Table 57 and the Rejection Specifications section.

DIGITAL FILTERS

Averaging Filters Rejection

The sinc[1] filter places additional notches at multiples of:

$f_{NOTCH_AVG} = f_{NOTCH_STD}/Avg$

where:
f_{NOTCH_STD} is the first notch from the sinc[3] or sinc[4] filter.
Avg is the averaging factor (average = 8).

So, programming the FS to 0d6 for the sinc[4] + sinc[1] or sinc[3] + sinc[1] averaging filter, to achieve a f_{NOTCH_STD} at 400 Hz, the sinc[1] filter places an f_{NOTCH_AVG} at 50 Hz. This can be achieved with both the sinc[4] + sinc[1] and sinc[3] + sinc[1] filters. See Figure 92 and Table 62.

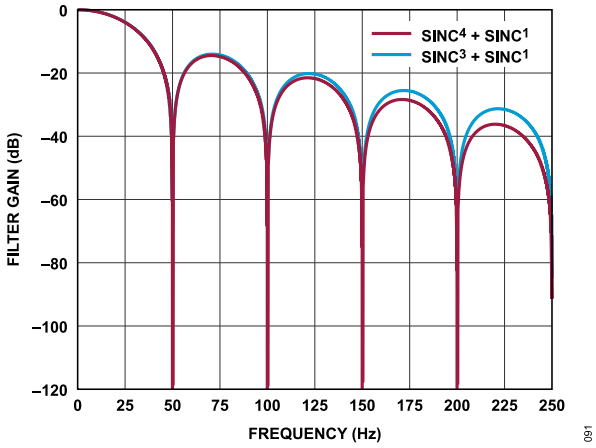


Figure 92. Sinc[3] + Sinc[1] and Sinc[4] + Sinc[1] Filter Response (FS = 6)

Table 62. Averaging Filters Rejection Performance

Filter Type	FS (Dec.)	ODR (SPS)	Rejection (dB)[1]
Sinc[3] + sinc[1]	6	40	40 (50 Hz only)
	5	48	42 (60 Hz only)
Sinc[4] + sinc[1]	6	36.36	40 (50 Hz only)
	5	43.64	42 (60 Hz only)

[1] The 50 Hz/60 Hz rejection is measured with a stable f_{MCLK} = 76.8 kHz, in a band of ±0.5 Hz around 50 Hz and/or 60 Hz.

SEQUENCER

When multiple channels are enabled, the on-chip sequencer is automatically used. The device automatically sequences between all enabled channels. There can be cases where the conversions on a channel are repeated using the repeat function, and channels that are converted only once.

First Conversion on a New Channel

When a channel change occurs, the modulator and filter reset, the X-MUX needs to switch to the new channel, and the new filter needs to settle before being able to generate the first conversion result.

In each specific application, a user might want to allow an adjustable front-end settling time (SETTLE_n bits in the FILTER_n registers) to allow for the excitation current to settle or a sensor to power up. This time cannot be less than 32 MCLK cycles to allow for the X-MUX to settle. In addition,

- Sinc[4] filter requires 4 times t_{CNV} and a certain processing time due to FS value to output the first result.
- Sinc[3] and sinc[3] + REJ60 filters require 3 times t_{CNV} and a certain processing time due to FS value to output the first result.
- Averaging and post filters require the same t_{CNV} and a certain processing time due to FS value to output the first result. These filters operate with a minimum first conversion delay with respect to subsequent conversions, compared to standalone filters.

The subsequent conversions on the same channel occur in $t_{CNV} = 1/f_{ADC}$, and the processing time is already accounted for. There is always a delay in the first data ready event on a new channel with respect to the subsequent data ready events on the same channel.

The predefined front-end settling time (t_{SETTLE}), the ideal first conversion time, and the processing time add up to determine the conversion time of the first conversion:

$t_{1st_CNV} = t_{SETTLE} + t_{1st_CNV_IDEAL} + DPP\ Time$

where:
t_{1st_CNV} is the first conversion time on a new channel.
t_{SETTLE} is the front-end settling time before the first conversion on a new channel due to the SETTLE_n bits selection, as per Table 63.
$t_{1st_CNV_IDEAL}$ is the ideal conversion time on a new channel. For the standalone filters, the first conversion time differs from the settled conversion time as shown in Table 64.
DPP Time is the digital postprocessing time expressed in MCLK cycles and it depends on the filter type and FS value, except for the post filters where it is a constant, as per Table 65.

Table 63. Programmable t_{SETTLE} Values

SETTLE_n	MCLK Cycles Before First Conversion Starts	t_{SETTLE}
0b000 (Default)	32	416.6 µs
0b001	64	833.3 µs
0b010	128	1.66 ms
0b011	256	3.33 ms
0b100	512	6.66 ms
0b101	1024	13.33 ms
0b110	2048	26.66 ms
0b111	4096	53.33 ms

Table 64. Conversion and First Conversion Time (MCLK Cycles)

Filter Type[1]	t_{CNV} (MCLK Cycles)	$t_{1st_CNV_IDEAL}$ (MCLK Cycles)
Sinc[4]	32 × FS	4 × t_{CNV}
Sinc[4] + sinc[1]	352 × FS	t_{CNV}
Sinc[3]	32 × FS	3 × t_{CNV}
Sinc[3] + REJ60	32 × FS	3 × t_{CNV}
Sinc[3] + sinc[1]	320 × FS	t_{CNV}

DIGITAL FILTERS

Table 64. Conversion and First Conversion Time (MCLK Cycles) (Continued)

Filter Type[1]	t_{CNV} (MCLK Cycles)	$t_{1st_CNV_IDEAL}$ (MCLK Cycles)
Sinc^3 + Post Filter 1	2944	t_{CNV}
Sinc^3 + Post Filter 2	3200	t_{CNV}
Sinc^3 + Post Filter 3	3968	t_{CNV}
Sinc^3 + Post Filter 4	4736	t_{CNV}

[1] FS is the decimal equivalent of the FS, Bits[10:0] binary value.

Table 65. DPP Time (MCLK Cycles)

Filter Type	FS[1] = 1 (or FS = 0)	FS > 1
Sinc^4	28 (364.6 µs)	62
Sinc^4 + sinc^1	62 (807.3 µs)	62
Sinc^3	28	62
Sinc^3 + REJ60	28	62
Sinc^3 + sinc^1	62	62
Sinc^3 + Post Filters	69 (898.4 µs)	69

[1] FS is the decimal equivalent of the FS, Bits[10:0] binary value.

Sequencer Timing

When in a sequence, different channels can have different configurations. A channel switch occurs after the actual conversion is completed (Figure 95), whereas the data ready signal high to low transitions always follow the additional DPP time needed to postprocess the converted data. In practice, there is an overlap of the new channel t_{SETTLE} and the previous channel DPP time. Therefore, the conversion time of the current channel (intended as the time between two data ready signal high to low transitions) can be calculated as per t_{1st_CNV} on that channel minus the DPP time of the previous channel, as shown in Figure 95.

A special case (shown in Figure 94) occurs if all channels in the sequence share the same ADC Setup n (in particular SETTLE_n, FILTER_MODE_n, and FS_n bitfields in the FILTER_n register), and only one sample per channel is collected before switching to the next channel (REPEAT_n set to 0 in the FILTER_n register). In this case, after the first conversion, the same conversion output data rate (1CNV_ODR) settles to a fixed value determined by 1/t_{1CNV}, where:

$$t_{1CNV} = t_{SETTLE} + t_{1st_CNV_IDEAL}$$

In this configuration, when continuous conversion mode is enabled, it is possible to calculate the sample rate per channel by dividing the 1CNV_ODR by the number of enabled channels sharing the same configuration in the sequence.

Note that the filter behavior is still dictated by the FILTER_MODE_n and FS_n bitfields. Therefore, the filter profile and rejection does not change with the 1CNV_ODR or sample rate per channel values.

Table 66. First Conversion Time and Conversion Time on a Settled Channel, by Filter Types[1]

Filter type	t_{1st_CNV}	t_{CNV}
Sinc^4	t_{SETTLE} + (4 × 32 × FS + DPP Time)/f_{MCLK}	(32 × FS)/f_{MCLK}
Sinc^4 + sinc^1	t_{SETTLE} + ((4 + Avg – 1) × 32 × FS + DPP Time)/f_{MCLK}	((4 + Avg – 1) × 32 × FS)/f_{MCLK}
Sinc^3 and sinc^3 + REJ60	t_{SETTLE} + (3 × 32 × FS + DPP Time)/f_{MCLK}	(32 × FS)/f_{MCLK}
Sinc^3 + sinc^1	t_{SETTLE} + ((3 + Avg – 1) × 32 × FS + DPP Time)/f_{MCLK}	((3 + Avg – 1) × 32 × FS)/f_{MCLK}
Sinc^3 + Post Filter 1	t_{SETTLE} + 38.33 ms + DPP Time/f_{MCLK}	38.33 ms
Sinc^3 + Post Filter 2	t_{SETTLE} + 41.67 ms + DPP Time/f_{MCLK}	41.67 ms
Sinc^3 + Post Filter 3	t_{SETTLE} + 51.67 ms + DPP Time/f_{MCLK}	51.67 ms
Sinc^3 + Post Filter 4	t_{SETTLE} + 61.67 ms + DPP Time/f_{MCLK}	61.67 ms

[1] t_{SETTLE} is the front-end settling time of a new channel due to the SETTLE_n bits selection. f_{MCLK} is the master clock frequency (76.8 kHz). Avg is 8. FS is the decimal equivalent of the FS, Bits[10:0] in the filter register. DPP Time is the digital postprocessing time expressed in MCLK cycles.

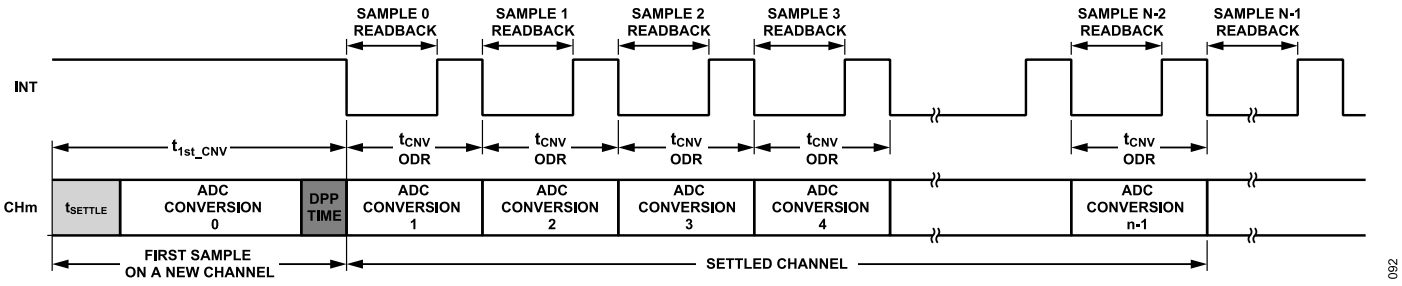


Figure 93. Example of Repeat Conversion on the Same Channel

DIGITAL FILTERS

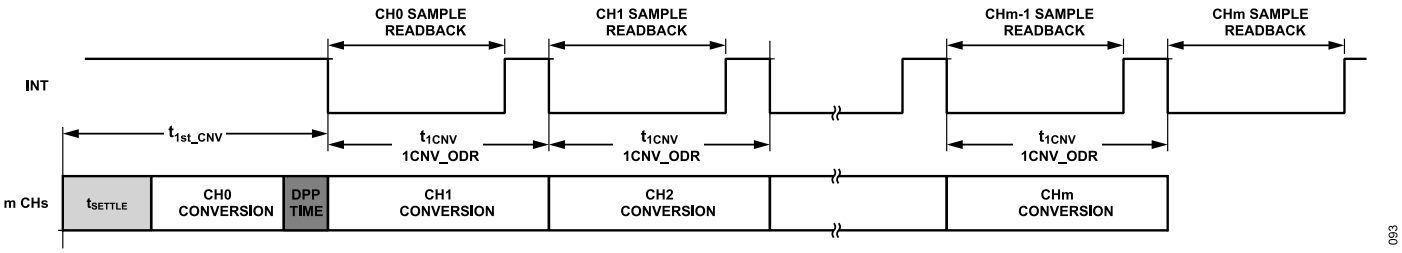


Figure 94. Example of Standard Sequencing Through Multiple Channels with Same Configuration and No Repeat Conversion

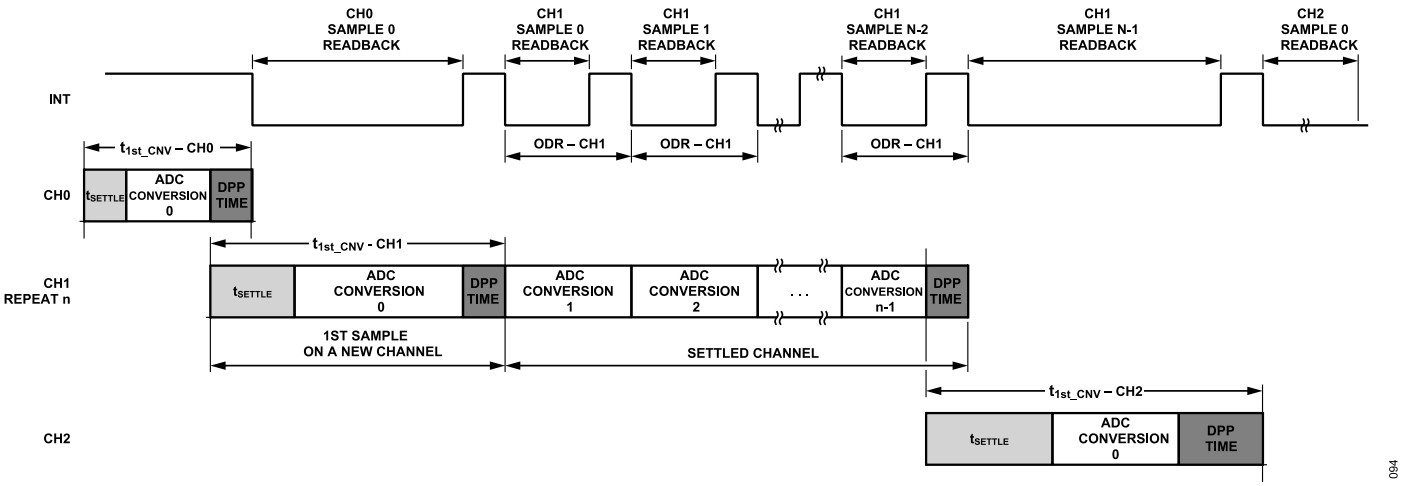


Figure 95. Example of Smart Sequencing

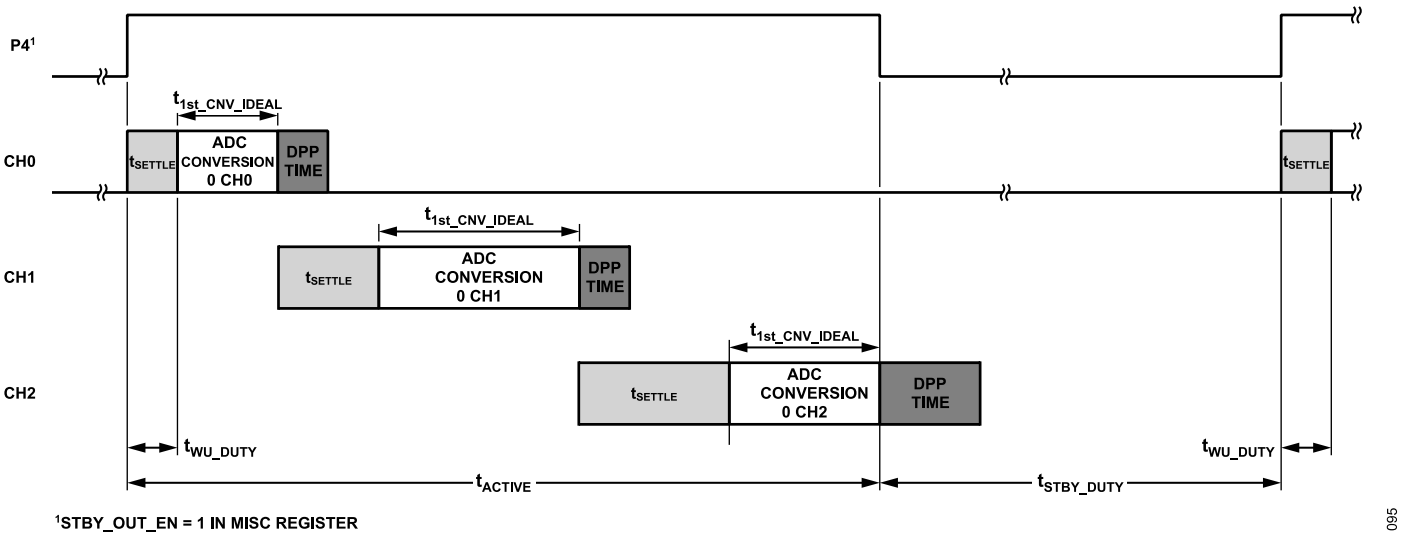


Figure 96. Example of Autonomous Duty Cycling Mode

DIGITAL FILTERS

Duty Cycling Mode Timing

The autonomous duty cycling mode on the AD4130-8 uses the conversion time of the sequence and the DUTY_CYC_RATIO bitfield settings to calculate the standby time.

The effective active time depends on the enabled channels in the sequence and their chosen configuration as follows:

$$t_{ACTIVE} - \sum_{0}^{n}\left(t_{SETTLEn} + t_{1st_CNV_IDEAL}\right)$$

where:
t_{ACTIVE} is the effective active time during duty cycling.
n is the number of channels enabled.
t_{SETTLE} is the front-end settling time before the first conversion on a new channel due to the SETTLE_n bits selection, as per Table 63.
$t_{1st_CNV_IDEAL}$ is the ideal conversion time on a new channel. For the standalone filters, the first conversion time differs from the settled conversion time as shown in Table 64. See Figure 96.

DPP time does not contribute to the effective active time in duty cycling mode. This applies also to the DPP time associated with the last enabled channel. The duty cycling wake-up time (t_{WU_DUTY}) does not affect the active time and can be visualized as overlapping with the first t_{SETTLE} of the active sequence, as shown in Figure 96.

The standby time during autonomous duty cycling mode corresponds to the P4 pin low in Figure 96 and is calculated by the device as follows:

$$t_{STBY_DUTY} = \left(Standby \quad Ratio \times \sum_{0}^{n} \quad t_{1st_CNV_IDEALn}\right) - t_{WU_DUTY}$$

where:
t_{STBY_DUTY} is the time that the device spends in standby when autonomous duty cycling mode is enabled.
Standby Ratio is 3 for 1/4 duty cycle and 15 for 1/16 duty cycle, depending on the DUTY_CYC_RATIO bit in the ADC_CONTROL register.
n is the number of channels enabled.
$t_{1st_CNV_IDEAL}$ is the ideal conversion time on a new channel. For the standalone filters, the first conversion time differs from the settled conversion time as shown in Table 64.
t_{WU_DUTY} is the duty cycling wake-up time (see Table 9).

Out of Standby Mode Timing

By default, the internal oscillator is powered down in standby mode, and reenabled when exiting standby mode. The internal oscillator takes some time to wake up and settle to the correct frequency, as shown in Figure 97 (see also Table 7). t_{SETTLE} can be used to adjust the time allowed for the input signal to settle before the signal acquisition starts.

When the internal oscillator is kept alive in standby mode, the standby mode wake-up time corresponds to t_{WU_STBY} in Table 9.

The internal oscillator is kept alive by default when selecting the duty cycling mode.

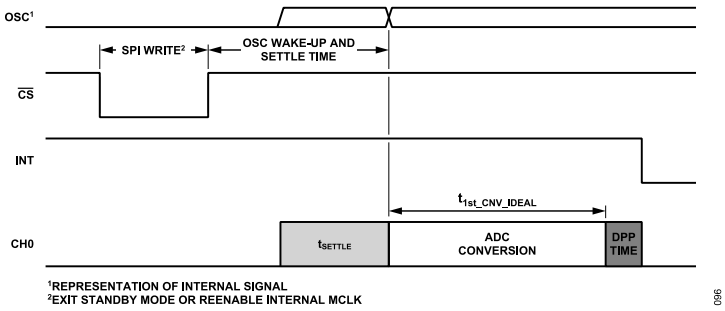


Figure 97. Out of Standby Mode Diagram

DIAGNOSTICS

The AD4130-8 has numerous diagnostic functions on chip. Use these features to ensure among others:

- Read/write operations are to valid registers only
- Only valid data is written to the on-chip registers
- The external reference, if used, is present
- The ADC modulator and filter are working within specification

SIGNAL CHAIN CHECK

Functions such as the reference and power supply voltages can be selected as inputs to the ADC. The AD4130-8 can therefore check the voltages connected to the device. The AD4130-8 also generates an internal signal of around 10 mV that can be applied internally to a channel by selecting the V_MV_P to V_MV_M option in the CHANNEL_m register. The PGA can be checked using this function. As the PGA setting is increased, for example, the signal as a percent of the analog input range is reduced by a factor of two. This allows the user to check that the PGA is functioning correctly.

REFERENCE DETECTION

The AD4130-8 includes on-chip circuitry (simplified in Figure 98) to detect if there is a valid reference for conversions or calibrations when the user selects an external reference as the reference source. This feature is valuable in applications such as RTDs or strain gauges where the reference is derived externally.

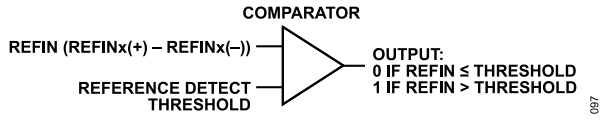


Figure 98. Reference Detect Circuitry

The reference detect threshold value can be found in Table 5. This feature is enabled when the REF_DETECT_ERR_EN bit in the ERROR_EN register is set to 1. If the voltage between the selected REFINx(+) and REFINx(−) pins goes below the threshold in Table 5, or either the REFINx(+) or REFINx(−) inputs are open circuit, the AD4130-8 detects that it no longer has a valid reference. In this case, the REF_DETECT_ERR bit in the error register is set to 1. The MASTER_ERR bit in the status register is also set to 1 (see Table 48).

If the user is concerned about verifying that a valid reference is in place every time a calibration is performed, check the status of the REF_DETECT_ERR bit at the end of the calibration cycle.

The reference detect flag may be set when the device exits of standby mode. Therefore, read the error register after exiting standby mode and write 1 to clear the REF_DETECT_ERR bit if set.

ADC ERRORS

The ADC conversion process and calibration process can also be monitored by theAD4130-8. These diagnostics check the analog input used as well as the modulator and digital filter during conversions or calibration. The functions can be enabled using the ADC_ERR_EN bit in the ERROR_EN register. With these functions enabled, the ADC_ERR bit is set to 1 if an error occurs.

The ADC_ERR flag is set for one or more of the following:

- Conversion error when there is an overflow or underflow in the digital filter. In this case, the ADC conversion also clamps to all 0s or all 1s.
- Modulator saturation error when the modulator outputs 20 consecutive 1s or 0s.
- Calibration error when during offset calibration, the resulting offset coefficient are outside the 0x07FFFF to 0xF7FFFF range. In this case, the OFFSET_n register is not updated and the ADC_ERR flag is set to 1. Also, during a gain calibration, overflow of the digital filter is checked. If an overflow occurs, the error flag is set to 1, and the GAIN_n register is not updated.

The ADC_ERR flag is updated with the update of the data register and can be cleared only by writing a 1 to it.

OVERVOLTAGE/UNDERVOLTAGE DETECTION

The overvoltage/undervoltage monitors check the absolute voltage on the AINx analog input pins and the REFINx input pins.

For the AINx pins, the absolute voltage must be within specification to meet the data sheet specifications. If the ADC is operated outside the data sheet limits, linearity degrades. Figure 99 shows the simplified block diagram of the AINx circuitry to detect overvoltage and undervoltage.

The positive (AINP) and negative (AINM) analog inputs can be separately checked for overvoltages and undervoltages. The AINP_OV_UV_ERR_EN and AINM_OV_UV_ERR_EN bits in the ERROR_EN register enable the overvoltage/undervoltage diagnostics respectively on AINP and AINM. An overvoltage is flagged when the voltage on AINx exceeds AV_{DD} while an undervoltage is flagged when the voltage on AINx goes below AV_{SS}.

The error flags are AINP_OV_UV_ERR and AINM_OV_UV_ERR bits in the error register and they flag an overvoltage and/or undervoltage error on any enabled AINP and AINM respectively.

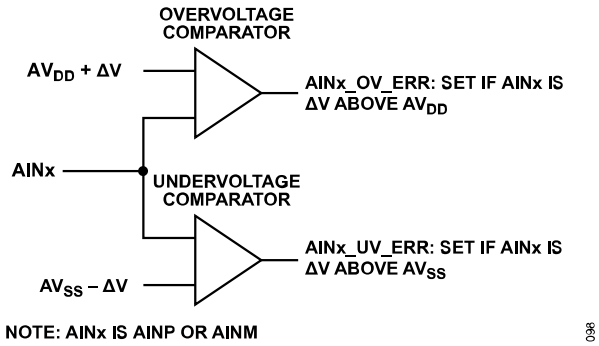


Figure 99. Analog Input Overvoltage/Undervoltage Monitors

The ΔV threshold value can be found in Table 5.

DIAGNOSTICS

The external reference voltage can also be monitored for overvoltage/undervoltage enabling the REF_OV_UV_ERR_EN bit in the ERROR_EN register. An overvoltage is flagged when the voltage on REFINx(+) exceeds AV_{DD} while an undervoltage is flagged when the voltage on REFINx(−) goes below AV_{SS}. The error flag REF_OV_UV_ERR in the error register is set to 1 in any of the two conditions.

When this function is enabled, the corresponding flags can be set in the error register. These bits are R/W1C.

POWER SUPPLY MONITORS

Along with converting external voltages, the ADC can monitor the voltage on the AV_{DD} pin and the IOV_{DD} pin. When the inputs of AV_{DD} to AV_{SS} or IOV_{DD} to DGND are selected, the voltage (AV_{DD} to AV_{SS} or IOV_{DD} to DGND) is internally attenuated by 6, and the resulting voltage is applied to the Σ-Δ modulator. This is useful to monitor variations in the power supply voltage.

MASTER CLOCK COUNTER

A stable MCLK to the ADC is important as the output data rate, filter first conversion time, and the filter notch frequencies are dependent on the master clock. The AD4130-8 allows the user to monitor the master clock. When the MCLK_CNT_EN bit in the ERROR_EN register is set, the MCLK_COUNT register increments by 1 every 131 master clock cycles. The user can monitor this register over a fixed period. The master clock frequency can be determined from the result in the MCLK_COUNT register. The MCLK_COUNT register wraps around after it reaches its maximum value.

SPI DIAGNOSTICS

SPI Clock Counter

The SPI SCLK counter counts the number of SCLK pulses used in each read and write operation. $\overline{CS}$ must frame every read and write operation when this function is used. All read and write operations are multiples of eight SCLK pulses. If the SCLK counter counts the SCLK pulses and the result is not a multiple of eight, an error is flagged. The SPI_SCLK_CNT_ERR bit in the error register is set to 1. If a write operation is being performed and the SCLK contains an insufficient number of SCLK pulses, the value is not written to the addressed register and the write operation is aborted.

The SCLK counter is enabled by setting the SPI_SCLK_CNT_ERR_EN bit in the ERROR_EN register.

SPI Read/Write Errors

Along with the SCLK counter, the AD4130-8 can also check the read and write operations to ensure that valid registers are being addressed.

When the SPI_READ_ERR_EN bit in the ERROR_EN register is set to 1, attempts to read registers at addresses not listed in Table 73 cause the SPI_READ_ERR bit to be set to 1 and the readback data for that register is all 0s.

When the SPI_WRITE_ERR_EN bit in the ERROR_EN register is set to 1, attempts to write to read-only registers and to registers at addresses not listed in Table 73 cause the SPI_WRITE_ERR bit to be set to 1, and the write transaction is aborted.

This function, along with the SCLK counter and the CRC protection, makes the serial interface more robust. Invalid registers are not written to or read from. An incorrect number of SCLK pulses can cause the serial interface to go asynchronous and incorrect registers to be accessed. The AD4130-8 protects against these issues via the diagnostics.

SPI Ignore Error

At certain times, the on-chip registers are not accessible. During power-up, when the on-chip registers are set to their default values, they cannot be accessed via SPI. The user must wait t_{RESET_DELAY} until this operation is complete before writing to registers. When offset or gain calibrations are being performed, registers cannot be accessed. When in single sequence mode, during conversion and before the last conversion finishes, registers cannot be accessed.

The SPI_IGNORE_ERR bit in the error register indicates when the on-chip registers cannot be written to. This diagnostic is enabled by default. The function can be disabled using the SPI_IGNORE_ERR_EN bit in the ERROR_EN register.

Any write operations performed when SPI_IGNORE_ERR is set to 1 in the error register are ignored. This bit is R/W1C.

CRC PROTECTION

The AD4130-8 features optional CRC to provide error detection on interface transactions, memory map content, and read-only memory (ROM) content.

CRC Calculation

The AD4130-8 uses the CRC-8 standard with the following polynomial:

$$x^8 + x^2 + x + 1$$

To generate the checksum, the data is left shifted by eight bits to create a number ending in eight Logic 0s. The polynomial is aligned so that its MSB is adjacent to the leftmost Logic 1 of the data. An XOR (exclusive OR) function is applied to the data to produce a new, shorter number. The polynomial is again aligned so that its MSB is adjacent to the leftmost Logic 1 of the new result, and the procedure is repeated. This process is repeated until the original data is reduced to a value less than the polynomial. This is the 8-bit checksum.

DIAGNOSTICS

SPI CRC Protection

The AD4130-8 has a CRC mode that can be used to improve interface robustness. Using the CRC ensures that only valid data is written to a register and allows data read from a register to be validated. If an error occurs during a register write, the CRC_ERR bit is set to 1 in the error register and the write transaction is aborted. However, to ensure that the register write was successful, read back the register and verify the checksum. The CRC_ERR_EN bit in the ERROR_EN register enables and disables the SPI CRC.

The SPI checksum is appended to the end of each read and write transaction. For a write transaction, the checksum is calculated using the 8-bit command word and the 8-bit to 24-bit data. For a read transaction, the checksum is calculated using the 8-bit command word and the 8-bit to 32-bit data output. Figure 100 and Figure 101 show SPI write and read transactions with CRC enabled, respectively.

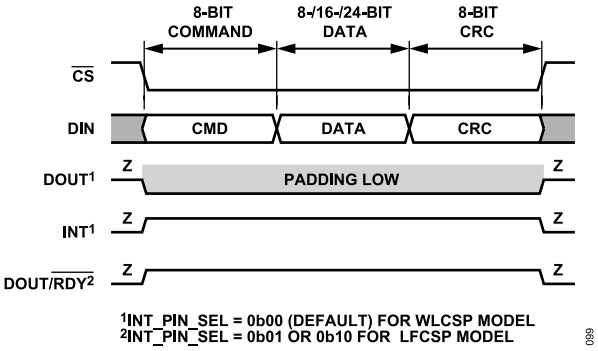


Figure 100. SPI Write Transaction with CRC

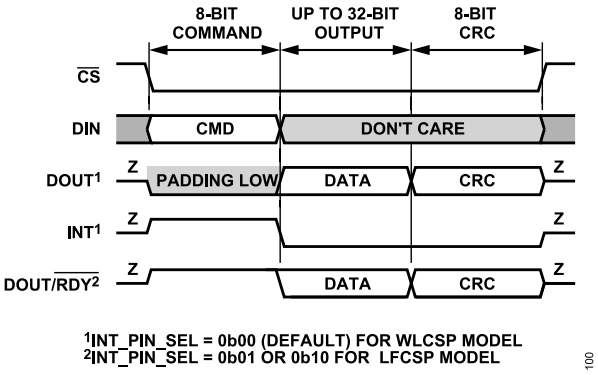


Figure 101. SPI Read Transaction with CRC

If SPI CRC is enabled when continuous read mode is active, there is an implied read data command of 0x42 before every data transmission that must be accounted for when calculating the checksum value. This ensures a nonzero checksum value even if the ADC data equals 0x000000.

See the CRC on FIFO Data section.

Memory Map CRC Protection

For added robustness, a CRC calculation is performed on the on-chip registers as well. The status register, data register, ID register, error register, MCLK_COUNT register, FIFO_STATUS register, and FIFO_DATA register are not included in this check because their contents change continuously, or they are read-only registers. The CRC is performed at a rate of 1/300 seconds. Each time that the memory map is accessed, the CRC is recalculated. Events that cause the CRC to be recalculated are

- A user write command
- An offset/full-scale calibration
- When the device is operated in single sequence mode and the ADC goes into standby mode following the completion of the conversion
- When exiting continuous read mode (the CONT_READ bit in the ADC_CONTROL register is set to 0)

The memory map CRC function is enabled by setting the MM_CRC_ERR_EN bit in the ERROR_EN register to 1. If an error occurs, the MM_CRC_ERR bit in the error register is set to 1.

ROM CRC Protection

On power-up, all registers are set to default values. These default values are held in ROM. For added robustness, at power-up, a CRC calculation is performed on the ROM contents as well.

The ROM CRC function is enabled by setting the ROM_CRC_ERR_EN bit in the ERROR_EN register to 1. If an error occurs, the ROM_CRC_ERR bit in the error register is set to 1.

When this function is enabled, the internal master clock, if enabled, remains active in the standby mode.

FIFO DIAGNOSTICS

On power-up, the FIFO is disabled. When enabled, the FIFO_STATUS register (see Table 71) and/or the FIFO_HEADER can be used to track the status of the FIFO and flag a number of errors on write/read operations, thresholds and watermark being reached, and overrun and empty flags. For more details, see the FIFO section.

BURNOUT CURRENTS

The AD4130-8 contains two constant current generators that can be programmed to 0.5 µA, 2 µA, or 4 µA. One generator sources current from AV_{DD} to AINP, and one sinks current from AINM to AV_{SS}, as shown in Figure 102. These currents enable open wire detection to check if a sensor is connected.

DIAGNOSTICS

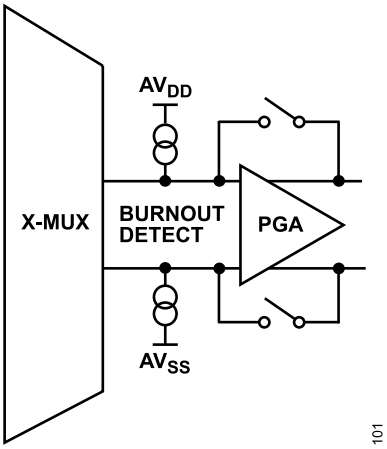


Figure 102. Burnout Currents

The currents are switched to the selected analog input pair. Both currents are either on or off. The burnout bits in the configuration register enable/disable the burnout currents along with setting the amplitude. Use these currents to verify that an external transducer is still operational before attempting to take measurements on that channel. After the burnout currents are turned on, they flow in the external transducer circuit, and a measurement of the input voltage on the analog input channel can be taken.

If the resulting voltage measured is near full scale, the user must verify why this is the case. A near full-scale reading can mean that the front-end sensor is open circuit. It can also mean that the front-end sensor is overloaded and is justified in outputting full scale, or that the reference may be absent and the REF_DETECT_ERR bit is set, thus clamping the data to all 1s. When a conversion is close to full scale, the user must check these three cases before making a judgment.

If the voltage measured is 0 V, it may indicate that the transducer has short circuited.

For normal operations, these burnout currents are turned off by setting the burnout bits to zero. The current sources work over the normal absolute input voltage range specifications with buffers on.

TEMPERATURE SENSOR

The AD4130-8 has an integrated temperature sensor that is useful to monitor the die temperature at which the device is operating. This can be used for diagnostic purposes or as an indicator of when the application circuit needs to rerun a calibration routine to take into account a shift in operating temperature.

The temperature sensor is accessible through the X-MUX as an internal channel and can be selected using the AINP, Bits[4:0] and AINM, Bits[4:0] in each CHANNEL_m register.

The equation for the temperature sensor is as follows:

Temperature (°C) = (*Conversion* (µV) / *Sensitivity (µV/*K)) – 273.15

where:
Conversion (µV) is the conversion result from the temperature sensor converted to Volts using the equations in Table 45.
Sensitivity (V/°C) is the sensitivity of the temperature sensor. The nominal sensitivity can be found in Table 5.

To improve the temperature sensor accuracy, operate the device in a known temperature (25°C) and take a conversion as a reference point. The difference between the nominal sensitivity and the one measured for the device can be used to calibrate the temperature sensor to higher accuracy.

The temperature sensor specifications can be found in Table 5 and Figure 58. See the Terminology section.

DIAGNOSTICS AND STANDBY MODE

The diagnostic functionality can be disabled when in standby mode by setting the STB_EN_DIAGNOSTICS bit in the MISC register to 1. Some diagnostics also require the internal oscillator to be enabled, so if those errors are enabled in the ERROR_EN register and the STB_EN_DIAGNOSTICS = 1, the internal oscillator is kept enabled. See the Standby Mode section.

FIFO

The AD4130-8 has ultra low power performance. Further system power saving can be achieved by putting the host processor and other peripherals to sleep when not in use. The AD4130-8 has an on-chip FIFO buffer to facilitate storage of up to 256 conversion results. Data can be collected continuously using the FIFO and the processor can be awakened via an interrupt from the AD4130-8 when data exceeds a specified threshold, when the FIFO has reached a predefined number of samples, or when the FIFO is full. The FIFO data is saved in 32-bit format, made of an 8-bit data for the FIFO_HEADER followed by a 24-bit data for the FIFO_DATA (conversion result). Figure 103 shows the basic structure of the FIFO.

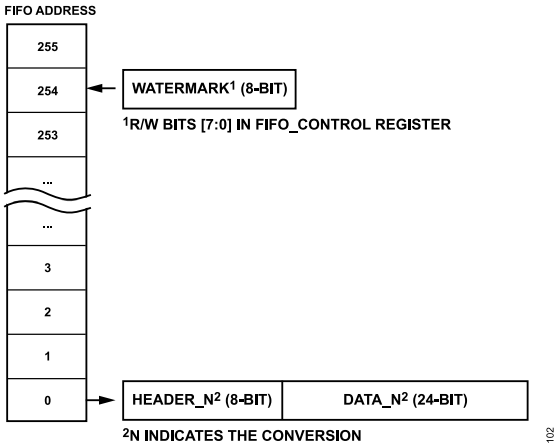


Figure 103. FIFO Structure

FIFO MODES

The FIFO can be set to one of the three modes described in this section by selecting the correspondent FIFO_MODE bits value in the FIFO_CONTROL register.

Disabled

The FIFO is disabled by default. When the FIFO is disabled, it is held in reset, so any old data is lost. The FIFO is disabled by setting the FIFO_MODE bits in the FIFO_CONTROL register to 0b00.

Write FIFO_MODE = 0b00 to exit any of the other FIFO modes.

Watermark Mode

In watermark mode, the FIFO collects data until the watermark level is reached. The watermark level specifies the number of conversions to store in the FIFO and is set by writing to the watermark bitfield in the FIFO_CONTROL register. The watermark bitfield default value is 0, which corresponds to 256 samples to fill the FIFO. Once the watermark is reached, the user must read all the data from the FIFO before the next ADC result is written to the FIFO. Otherwise, a FIFO write error occurs (FIFO_WRITE_ERR bit is set to 1 in the FIFO_STATUS register, see Table 71) and conversion results are lost. The FIFO is not updated with new ADC data until the FIFO is completely read, as shown in Table 67. Clearing the FIFO is recommended after reading the FIFO in watermark mode.

See the FIFO Readback section for details on how to calculate the time needed to readback the FIFO. Depending on the channels and smart sequencer configuration, and the SCLK speed for the FIFO readback, the watermark value may have to be limited to avoid data loss.

See the FIFO Watermark Interrupt section.

Streaming Mode

In streaming mode, the FIFO always contains the most recent ADC data. Unlike the watermark mode, the FIFO continues to store ADC results even when the watermark level is reached, and FIFO is not read. When the FIFO is filled with 256 conversions, the older conversions are overwritten with new ADC results, as shown in Table 68. In this mode, data can be read back at any time unless the FIFO is being updated with new ADC result. In streaming mode, the FIFO is eventually overrun and the OVERRUN_FLAG bit in the FIFO_STATUS register is set to 1 (see Table 71).

Table 67. Example of FIFO Buffer Filling Up with Conversion Results in Watermark Mode with Watermark = 0 (256 Samples) and Data Not Read Back When Full

FIFO Address	Conversion 1	Conversion 2	...	Conversion 255	Conversion 256	Conversion 257	Conversion 258	...
255	Empty	Empty	...	Empty	(FIFO_HEADER (256), FIFO_DATA (256))	(FIFO_HEADER (256), FIFO_DATA (256))	(FIFO_HEADER (256), FIFO_DATA (256))	...
254	Empty	Empty	...	(FIFO_HEADER (255), FIFO_DATA (255))	(FIFO_HEADER (255), FIFO_DATA (255))	(FIFO_HEADER (255), FIFO_DATA (255))	(FIFO_HEADER (255), FIFO_DATA (255))	...
...	...	...	...	...	...	...	...	...
1	Empty	(FIFO_HEADER (2), FIFO_DATA (2))	...	(FIFO_HEADER (2), FIFO_DATA (2))	(FIFO_HEADER (2), FIFO_DATA (2))	(FIFO_HEADER (2), FIFO_DATA (2))	(FIFO_HEADER (2), FIFO_DATA (2))	...
0	(FIFO_HEADER (1), FIFO_DATA (1))	(FIFO_HEADER (1), FIFO_DATA (1))	...	(FIFO_HEADER (1), FIFO_DATA (1))	(FIFO_HEADER (1), FIFO_DATA (1))	(FIFO_HEADER (1), FIFO_DATA (1))	(FIFO_HEADER (1), FIFO_DATA (1))	...

FIFO

Table 68. Example of FIFO Buffer Filling Up with Conversion Results in Streaming Mode with Watermark = 0 (256 Samples) and Data Not Read Back When Full

FIFO Address	Conversion 1	Conversion 2	…	Conversion 255	Conversion 256	Conversion 257	Conversion 258	…
255	Empty	Empty	…	Empty	(FIFO_HEADER (256), FIFO_DATA (256))	(FIFO_HEADER (257), FIFO_DATA (257))	(FIFO_HEADER (258), FIFO_DATA (258))	…
254	Empty	Empty	…	(FIFO_HEADER (255), FIFO_DATA (255))	(FIFO_HEADER (255), FIFO_DATA (255))	(FIFO_HEADER (256), FIFO_DATA (256))	(FIFO_HEADER (257), FIFO_DATA (257))	…
…	…	…	…	…	…	…	…	…
1	Empty	(FIFO_HEADER (2), FIFO_DATA (2))	…	(FIFO_HEADER (2), FIFO_DATA (2))	(FIFO_HEADER (2), FIFO_DATA (2))	(FIFO_HEADER (3), FIFO_DATA (3))	(FIFO_HEADER (4), FIFO_DATA (4))	…
0	(FIFO_HEADER (1), FIFO_DATA (1))	(FIFO_HEADER (1), FIFO_DATA (1))	…	(FIFO_HEADER (1), FIFO_DATA (1))	(FIFO_HEADER (1), FIFO_DATA (1))	(FIFO_HEADER (2), FIFO_DATA (2))	(FIFO_HEADER (3), FIFO_DATA (3))	…

Table 69. FIFO_CONTROL Register

Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x3A	FIFO_CONTROL	[23:16]	RESERVED				ADD_FIFO_STATUS	ADD_FIFO_HEADER	FIFO_MODE		0x040200	R/W
		[15:8]	RESERVED	FIFO_WRITE_ERR_INT_EN	FIFO_READ_ERR_INT_EN	THRES_HIGH_INT_EN	THRES_LOW_INT_EN	OVERRUN_INT_EN	WATERMARK_INT_EN	EMPTY_INT_EN		
		[7:0]	WATERMARK									

FIFO READBACK

The FIFO buffer is read by using the COMMS register to read Address 0x3D. The complete FIFO read command is 0x7D. This is followed by an 8-bit field, # samples (N), to indicate the number of samples to be read, where 0x00 corresponds to 256 samples. The FIFO content then appears on the DOUT (WLCSP) or DOUT/$\overline{RDY}$ (LFCSP) pin once the appropriate number of SCLKs is provided. When reading the last value in the FIFO, the EMPTY_FLAG bit in the FIFO_HEADER and in the FIFO_STATUS register is set to 1 (see Table 71). If attempts to read the FIFO continue, the EMPTY_FLAG bit remains set and the data read is all 0s. The FIFO read is terminated by toggling $\overline{CS}$ high or when the number of samples read reaches the specified amount in the FIFO command.

By default, the FIFO_HEADER is enabled and the FIFO_STATUS append is disabled, so the FIFO readback diagram looks like Figure 104. If the FIFO_STATUS append is enabled, the FIFO readback diagram looks like Figure 105.

The time available to the user to read the FIFO depends on the time the next two ADC conversions in the sequence take.

$$t_{FIFO_READ} = \Sigma\ ConvTime_n - (t_{BSY} + t_{QUIET1} + t_{QUIET2})$$

where:
t_{FIFO_READ} is the maximum time available for the FIFO readback that avoids data loss.
Σ ConvTime_n with (n = 0 − 1) is the conversion time of the next two conversions in the sequence. Note that the conversion time can be different based on the channels enabled. See the 50 Hz and 60 Hz Rejection section for more details on how to calculate the ADC conversion time for a given channel in the sequence.

$t_{BSY} + t_{QUIET1} + t_{QUIET2}$ is 8 MCLK cycles as a minimum. See Figure 12 and Table 10.

The number of SCLK cycles needed to complete a FIFO readback is equal to:

 # SCLK cycles = FIFO read command length +

 # samples (N) × samples length

where:
FIFO read command length is equal to 16 SCLK cycles.
 # samples (N) is the number of FIFO samples to read specified in the FIFO read command.
samples length is equal to 24 SCLK cycles if the FIFO_HEADER is disabled, or 32 SCLK cycles if the FIFO_HEADER is enabled.

When the SPI takes control of the FIFO for the readback, the device does not have access to the FIFO to write new data to it. If the FIFO readback takes longer than t_{FIFO_READ} to complete, there can be data loss from the converted sequence.

FIFO Ready Signal

When the FIFO is enabled, a FIFO ready signal is automatically shared to the DOUT (WLCSP) or redirected to the DOUT/$\overline{RDY}$ (LFCSP) pin. When this signal is high, it indicates that the FIFO is busy. The ADC is accessing the FIFO to write new data to it. When this signal is low, it indicates that the FIFO is available to be read by the user. When in watermark mode, the FIFO ready signal remains high until the number of samples stored in the FIFO reaches the watermark value. Then, the FIFO ready signal goes low to flag the user that a read command can be sent. When in streaming mode, the FIFO ready signal flags when the FIFO is busy after every conversion.

FIFO

Table 70. FIFO Header Format

Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
FIFO_HEADER	[7:0]	RESERVED	THRESHOLD_FLAG	WATERMARK_FLAG	EMPTY_FLAG	CH[3]	CH[2]	CH[1]	CH[0]	0x00	R

Table 71. FIFO_STATUS Register

Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x3B	FIFO_STATUS	[7:0]	MASTER_ ERR	FIFO_WRITE_ ERR	FIFO_READ_ ERR	THRES_HIGH _FLAG	THRES_LOW _FLAG	OVERRUN_ FLAG	WATERMARK_ FLAG	EMPTY_ FLAG	0x01	R

FIFO Header

FIFO_HEADER is enabled by default and is stored with each conversion result in the FIFO with the format shown in Table 70. FIFO_HEADER can be disabled by setting the ADD_FIFO_HEADER bit in FIFO_CONTROL register to 0. Figure 106 shows reading the data with FIFO_HEADER disabled.

FIFO_HEADER has the following bits of information:

- The CH, Bits[3:0] hold the channel number for the data FIFO_HEADER is appended to.
- The EMPTY_FLAG bit is set to 1 in the FIFO_HEADER associated with the last data sample from the FIFO being read so it can be interpreted as the trigger to stop reading back the FIFO.
- The WATERMARK_FLAG bit is set to 1 in the FIFO_STATUS register when the FIFO contains a number of samples greater than or equal to the indicated samples in the watermark field of the FIFO_CONTROL register. Therefore, it is flagged in FIFO_HEADER for every sample stored in excess of and equal to the watermark value.
- The THRESHOLD_FLAG bit is set to 1 if the THRES_EN_m bit is set to 1 in the relative CHANNEL_m register, and the ADC conversion result for that channel exceeds threshold values specified by the threshold range using the THRES_HIGH_VAL and THRES_LOW_VAL bitfields in the FIFO_THRESHOLD register. The THRESHOLD_FLAG bit in FIFO_HEADER is non sticky. Therefore, it is relevant for every sample.

FIFO Status

The FIFO_STATUS register content (see Table 71) can be enabled to be added and read before the FIFO_DATA and during the # samples (N) byte (see Figure 105), by setting ADD_FIFO_STATUS bit to 1 in the FIFO_CONTROL register (see Table 69). This way, the user can detect an error earlier on and abort the FIFO_DATA readback.

The FIFO_STATUS register contains errors and flags to help with the FIFO operations when the FIFO is enabled.

A FIFO empty flag is triggered (EMPTY_FLAG bit is set to 1) in the FIFO_STATUS register as the first bit of the last data sample from the FIFO is being read. If attempting to read an empty FIFO, this flag is set to 1 in the FIFO_STATUS register. This flag clears when the FIFO is written with at least one ADC conversion.

A FIFO watermark flag is triggered (WATERMARK_FLAG set to 1) in the FIFO_STATUS register when the FIFO contains a number of samples greater than or equal to the indicated samples in the watermark field of the FIFO_CONTROL register. The watermark flag clears as soon as the remaining samples in the FIFO are detected to be less than the value in the watermark field.

A FIFO overrun flag (OVERRUN_FLAG bit is set to 1) occurs if ADC data is lost and is not stored in the FIFO. In watermark mode, this occurs when the FIFO is not emptied out before a new sample must be stored. In streaming mode, ADC data is lost when oldest data in the FIFO is discarded to make way for new data as the FIFO was already full. The overrun flag clears when the FIFO is emptied by reading all the content or clearing the FIFO.

A FIFO threshold flag is triggered (THRES_HIGH_FLAG and/or THRES_LOW_FLAG bitfields is set to 1) if the ADC conversion result exceeds the threshold values specified. Unlike THRESHOLD_FLAG in FIFO_HEADER, the THRES_HIGH_FLAG and THRES_LOW_FLAG bitfields are sticky. That is, once these bitfields are set, they remain set despite the next ADC conversion result. The threshold flags can be cleared by reading all the data in the FIFO, or by clearing the FIFO.

A FIFO read error (FIFO_READ_ERR set to 1) only occurs when attempts are made to read the FIFO data while the ADC is updating internally (writing to the FIFO). The FIFO_DATA transmitted is all 0s when reading from the FIFO, the FIFO_HEADER information is also all 0s if this error occurred. This error clears when a FIFO read request is successfully granted or the FIFO is emptied.

A FIFO write error (FIFO_WRITE_ERR set to 1) occurs when conversion data is not written to the FIFO due to ongoing read of the FIFO by the user. An ADC FIFO write can be delayed by up to one conversion cycle if the user is still reading the FIFO data. However, if the user is still reading data following one conversion delay, a FIFO write error is asserted. When in watermark mode, a FIFO write error can occur if the FIFO reaches a number of entries equal to the watermark specified and an attempt to write new data to it is made. This error clears when all the content of the FIFO is read or by clearing the FIFO.

The master error bit in the FIFO_STATUS register is shared with the STATUS register and follows the same behavior.

FIFO

CRC on FIFO Data

When reading back FIFO data, a 16-bit CRC can be enabled by setting the SPI_CRC_ERR to 1 in the error register. This is only possible when FIFO_STATUS is disabled (ADD_FIFO_STATUS = 0) and FIFO_HEADER is enabled (ADD_FIFO_HEADER = 1) in the FIFO_CONTROL register (default settings). See Table 69 and Figure 107.

CRC data is sent after reading out samples of data equal to the watermark specified. Thus, in watermark mode, the CRC check is performed on all data as the FIFO length equals the watermark. While in streaming mode, the CRC is calculated on blocks of watermark samples.

The CRC on FIFO data is calculated as follows:

- First CRC sent is computed based on: (1) FIFO read command (0x7d) plus number of data to read; (2) ADC data read out
- Succeeding CRC is solely based on ADC data read out

The 16-bit CRC polynomial to be used for checks is

$x^{16} + x^{15} + x^{13} + x^{9} + x^{7} + x^{6} + x^{5} + x^{3} + x^{1} + 1$

The CRC can detect up to 3-bit errors for up to 32571 bits and can be used for the full FIFO depth of 256. The CRC must be initialized to 0xFFFF.

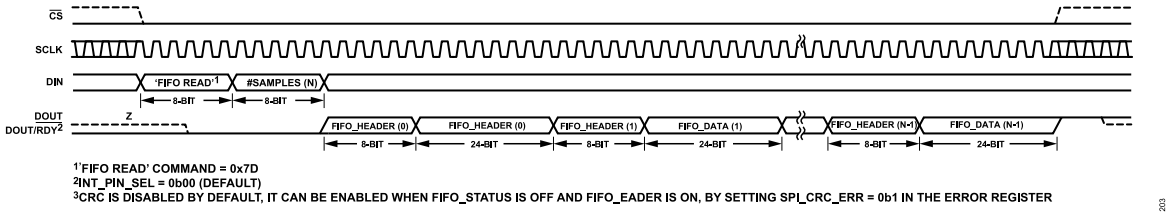


Figure 104. FIFO Readback Default (FIFO_STATUS Append Off and FIFO_HEADER Append On)

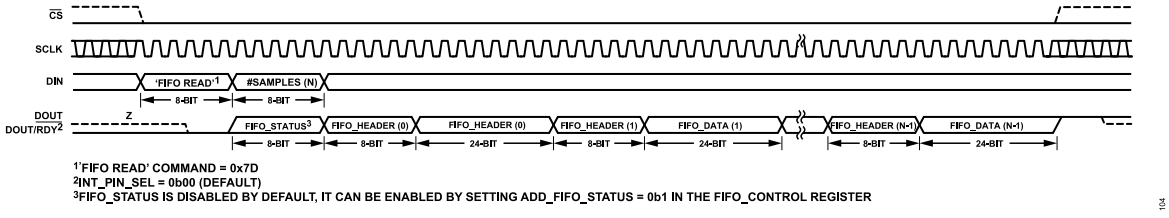


Figure 105. FIFO Readback (FIFO_STATUS Append On and FIFO_HEADER Append On)

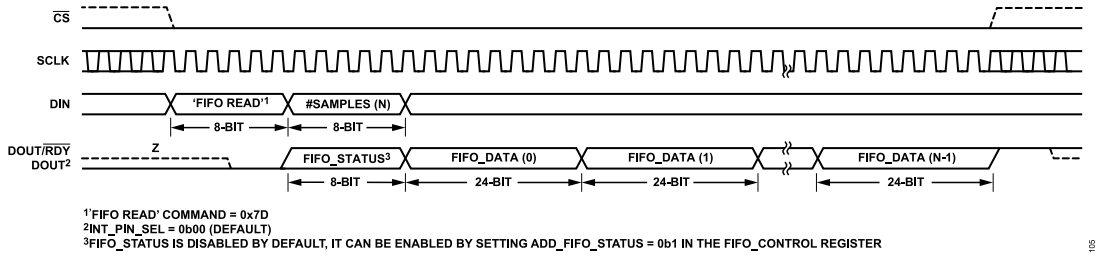


Figure 106. FIFO Readback (FIFO_STATUS Append On and FIFO_HEADER Append Off)

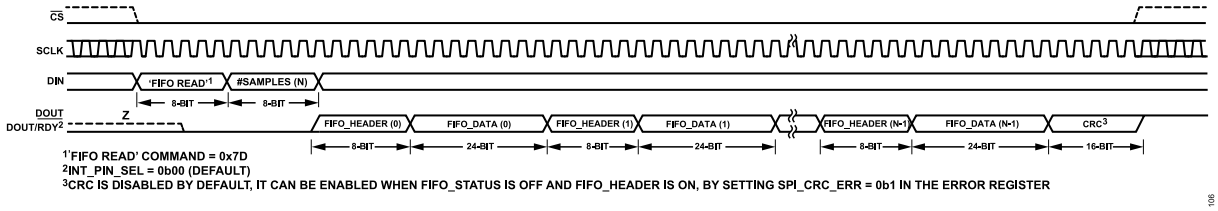


Figure 107. FIFO Readback (FIFO_STATUS Append Off and FIFO_HEADER Append On, CRC On)

FIFO

FIFO INTERRUPT

The AD4130-8 FIFO buffer can adopt multiple interrupt modes by configuring the FIFO_CONTROL register. The interrupt signal sent to the FIFO interrupt pin is the logic OR of all the enabled interrupt options in the FIFO_CONTROL register. See the FIFO Interrupt Pin section on how to select the pin to direct the interrupt signal to.

FIFO Watermark Interrupt

The FIFO watermark interrupt is enabled by default and can be disabled by setting the WATERMARK_INT_EN bit to 0 in the FIFO_CONTROL register. The number of samples needed to trigger a FIFO watermark interrupt is equal to the value specified in the watermark bitfield. The exception is the value 0, which is the default value. In this case, the FIFO needs to be filled to the maximum depth of 256 entries before triggering an interrupt. The FIFO watermark interrupt signal is active high and stays asserted while the number of samples in the FIFO is equal or greater than the value specified in the watermark register. The FIFO watermark interrupt signal is deasserted when the flag is cleared as soon as the remaining samples in the FIFO are detected to be less than watermark entries.

FIFO Data Threshold Interrupt

The THRES_HIGH_FLAG and THRES_LOW_FLAG bits in the FIFO_STATUS register (see Table 71) can be enabled to trigger a FIFO data threshold interrupt by setting the THRES_HIGH_INT_EN bit and/or the THRES_LOW_INT_EN bit to 1 in the FIFO_CONTROL register. Both options are disabled by default and can be enabled separately.

The threshold values for the FIFO data threshold interrupt can be specified in the THRES_HIGH_VAL and THRES_LOW_VAL bitfields in the FIFO_THRESHOLD register. These values need to be consistent with polarity setting specified by the bipolar bit in the ADC_CONTROL register.

After updating the threshold values, it is recommended to clear the FIFO by writing to FIFO_CONTROL register, so that the next set of conversions in the FIFO assume the updated threshold values. Doing this also clears the FIFO data threshold interrupt signal and the THRES_HIGH_FLAG and THRES_LOW_FLAG bits in the FIFO_STATUS register.

Note that threshold comparison has hysteresis of 1 LSB with respect to the threshold value set. When a conversion triggers THRES_HIGH_FLAG or THRES_LOW_FLAG to be set to 1, succeeding conversions must have DATA, Bits[23:12] at least 2 LSBs greater than the THRES_LOW_VAL bitfield, and 2 LSBs lower than THRES_HIGH_VAL bitfield for the THRES_LOW_FLAG and THRES_HIGH_FLAG bits to return to 0.

FIFO Empty Interrupt

The EMPTY_FLAG bit in the FIFO_STATUS register (see Table 71) can be enabled to trigger a FIFO empty interrupt by setting the EMPTY_INT_EN bit to 1 in the FIFO_CONTROL register. This option is disabled by default. The FIFO empty interrupt clears when the FIFO empty error clears in the FIFO_STATUS register, which is when the FIFO is written with at least one ADC conversion.

FIFO Write/Read Error Interrupt

The FIFO_WRITE_ERR and FIFO_READ_ERR bits in the FIFO_STATUS register (see Table 71) can be enabled to trigger a FIFO write interrupt and/or a FIFO read interrupt by setting the FIFO_WRITE_ERR_INT_EN and/or FIFO_READ_ERR_ INT_EN bits to 1 in the FIFO_CONTROL register. This option is disabled by default.

The FIFO write/read error interrupt signals are deasserted as soon as the error flags clear in the FIFO_STATUS register.

FIFO Overrun Interrupt

The OVERRUN_FLAG bit in the FIFO_STATUS register (see Table 71) can be enabled to trigger an interrupt by setting the OVERRUN_INT_EN bit to 1 in the FIFO_CONTROL register. This option is disabled by default.

The FIFO overrun interrupt signal is deasserted as soon as the error flag clears in the FIFO_STATUS register, which is when the FIFO is emptied.

FIFO Interrupt Pin

When the FIFO is enabled, a FIFO interrupt signal can be generated internally and directed to a pin of choice by configuring the INT_PIN_SEL bits in the IO_CONTROL register (see Table 41) as per Table 72.

Configuring a pin as interrupt takes priority over other pin controls on that pin. That is, enabling the CLK pin as a CLK input via the CLK_SEL bit in the ADC_CONTROL register is ignored if the CLK pin is enabled as an interrupt. Enabling the P2 pin as a GPO output via the GPO_CTRL_P2 bit in the IO_CONTROL is ignored if P2 is enabled as an interrupt. When P2 is enabled as an interrupt pin, the GPO pins are also automatically enabled in standby mode.

Table 72. FIFO Interrupt Pin Options

INT_PIN_SEL	LFCSP	WLCSP[1]
0b00 (Default)	N/A[2]	INT
0b01	CLK	CLK
0b10	P2	P2
0b11	N/A[2]	N/A[2]

[1] FIFO enabled. When the FIFO is disabled, the INT_PIN_SEL bitfield is used to assign the ready signal to a pin as per Table 55.

[2] N/A means not applicable.

FIFO

CLEARING THE FIFO

When the FIFO is enabled, any write to the FIFO_CONTROL register clears the FIFO. It is also possible to use the $\overline{\text{SYNC}}$ pin to initiate a FIFO clear by setting the SYNCB_CLEAR bit to 1 in the IO_CONTROL register (see Table 41). Clearing the FIFO using the $\overline{\text{SYNC}}$ pin guarantees that the sequencer restarts from the first channel. See Figure 11, Figure 13, and Table 10.

APPLICATIONS INFORMATION

POWER SCHEMES

The AD4130-8 allows for different power schemes depending on the requirements.

Single-Supply Operation (AV_{SS} = DGND)

When the AD4130-8 is powered from a single supply that is connected to AV_{DD} and IOV_{DD}, AV_{SS} and DGND can be shorted together on one single ground plane. With this setup, an external level shifting circuit is required when using truly bipolar inputs to shift the common-mode voltage. Recommended regulators include the ADP150, which has a 3.3 V output and low quiescent current.

When AV_{DD} and IOV_{DD} are connected to the same source, their minimum value is limited by the minimum AV_{DD} = 1.71 V.

Split Supply Operation (AV_{SS} ≠ DGND)

The AD4130-8 can operate with AV_{SS} set to a negative voltage, allowing true bipolar inputs to be applied. This allows a truly fully differential input signal centered around 0 V to be applied to the AD4130-8 without the need for an external level shifting circuit. For example, with a 3.6 V split supply, AV_{DD} = +1.8 V and AV_{SS} = −1.8 V. In this use case, the AD4130-8 internally level shifts the signals, allowing the digital output to function between DGND (nominally 0 V) and IOV_{DD}.

When using a split supply for AV_{DD} and AV_{SS}, the absolute maximum ratings must be considered (see the Absolute Maximum Ratings section).

Keep in mind that when AV_{SS} ≠ DGND, the GPOs cannot be used as digital output pins.

Separate Positive Supplies Operation

When trying to minimize the power consumption, AV_{DD} and IOV_{DD} can be connected to separate sources to be independently lowered to their minimum values. AV_{DD} can be as low as 1.71 V, while IOV_{DD} can be as low as 1.65 V. For example, IOV_{DD} can be powered by the same source of the processor interface, while AV_{DD} can have its own source.

RECOMMENDED DECOUPLING

Good decoupling is important when using high resolution ADCs. The AD4130-8 has two power supply pins, AV_{DD} and IOV_{DD}. The AV_{DD} pin is referenced to AV_{SS}, and the IOV_{DD} pin is referenced to DGND. Decouple AV_{DD} with a 1 µF tantalum capacitor in parallel with a 0.1 µF capacitor to AV_{SS}. Decouple IOV_{DD} with a 1 µF tantalum capacitor in parallel with a 0.1 µF capacitor to DGND. Place the 0.1 µF capacitors as close as possible to the device on each supply, ideally right up against the device. All analog inputs must be decoupled to AV_{SS}. If an external reference is used, decouple the REFINx(+) and REFINx(−) pins to AV_{SS}.

The AD4130-8 also has two on-board LDO regulators, one that regulates the AV_{DD} supply and one that regulates the IOV_{DD} supply. For the REGCAPA pin, it is recommended to add a 0.1 µF capacitor to AV_{SS}. Similarly, for the REGCAPD pin, it is recommended to add a 0.1 µF capacitor to DGND.

INPUT FILTERS

An external antialiasing filter is required to reject any interference at the modulator frequency ($f_{MOD} = f_{MCLK}/2$ = 38.4 kHz) and multiples of the modulator frequency. In addition, some filtering may be needed for electromagnetic interference (EMI) purposes. The analog inputs are buffered, and the reference inputs can be buffered, which allows the user to connect any RC combination to the reference or analog input pins.

MICROPROCESSOR INTERFACING

Microprocessor interfacing to the AD4130-8 is via a serial bus that uses a standard protocol compatible with DSPs and microcontrollers. The communications channel requires a 4-wire serial interface consisting of a clock signal, a data input signal, a data output signal, and a synchronization signal.

The SPI of the AD4130-8 is designed to be easily connected to industry-standard DSPs and microcontrollers. Figure 108 shows the AD4130-8 connected to the MAX32670. The MAX32670 has an integrated SPI port that can be connected directly to the SPI pins of the AD4130-8.

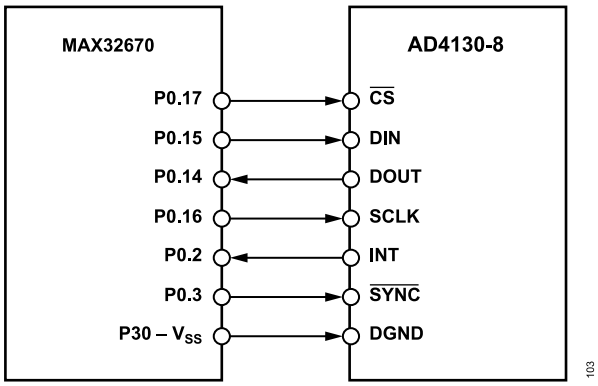


Figure 108. Example of MAX32670 µC SPI Connection to AD4130-8

Digital Pins

It is recommended that a weak pull-up resistor to IOV_{DD} is placed on $\overline{CS}$ (when in use), $\overline{SYNC}$, and SCLK lines to keep the interface disabled while powering up the device. It is recommended that a weak pull-down resistor is placed on the DIN line.

UNUSED PINS

When not in use, the following digital pins must be treated with care. Connect $\overline{SYNC}$ to IOVDD directly or with a weak pull-up resistor. Connect $\overline{CS}$ and CLK to DGND with a weak pull-down resistor.

APPLICATIONS INFORMATION

When not in use, the analog pins (AINx, REFINx(±), REFOUT, PSW) can be left electrically floating, but must be soldered to the PCB for mechanical stability.

POWER-UP AND INITIALIZATION

Power up the AD4130-8 by following the recommended power supply sequencing as follows: DGND, AV_{SS} (if different from DGND), IOV_{DD}, AV_{DD}, REFINx(+) and REFINx(−), AINx, Digital Inputs. See also Digital Pins section.

Upon power-up, wait for the t_{RESET_DELAY} timing before attempting an SPI transaction (see the Power-On Reset section). The device has a power-on reset function. However, any glitches during power-up can cause corruption of the registers. Therefore, a reset in the initialization routine is advisable. Write 64 consecutive ones to the device to perform a software reset (see the Device Reset section). If the digital host attempts to perform an SPI transaction before the device is ready, the transaction is invalid and the SPI_IGNORE_ERR bit in the ERROR register is set. The SPI_IGNORE_ERR is an R/W1C type of bit.

After the device initializes, the digital interface can be accessed to configure the device, including selecting the reference scheme according to the application. Regardless of the voltage reference scheme used, it is recommended to let the voltage reference settle after configuring the device to ensure it achieves its specifications.

The recommended configuration flow is as follows:

1. Select Interface mode: write to ADC_CONTROL register (select 3-wire or 4-wire mode, clock source, enable CRC, data + status, and so on).
2. Setup configuration: Eight possible ADC setup options. Write to the CONFIG_n and FILTER_n registers (select configuration, filter order, output data rate, and so on).
3. Channel configuration: write to the CHANNEL_m registers (select positive and negative input and setup for each ADC channel, enable open wire detection in GPIO configuration, and so on).
4. Setup ADC mode: write to the ADC_CONTROL register (select ADC operating mode, clock source, enable CRC, data + status, and so on) to start conversions.

LAYOUT AND GROUNDING

The analog inputs and reference inputs are differential and, therefore, most of the voltages in the analog modulator are common-mode voltages. The high common-mode rejection of the device removes common-mode noise on these inputs. The analog and digital supplies to the AD4130-8 are independent and separately pinned out to minimize coupling between the analog and digital sections of the device. The digital filter provides rejection of broadband noise on the power supplies, except at integer multiples of the master clock frequency.

The digital filter also removes noise from the analog and reference inputs, provided that these noise sources do not saturate the analog modulator. As a result, the AD4130-8 is more immune to noise interference than a conventional high resolution converter. However, given that the resolution of the AD4130-8 is high and the noise levels from the converter are so low, care must be taken regarding grounding and layout.

The PCB that houses the ADC must be designed so that the analog and digital sections are separated and confined to certain areas of the board. A minimum etch technique is generally best for ground planes because it results in the best shielding.

In any layout, the user must keep in mind the flow of currents in the system, ensuring that the paths for all return currents are as close as possible to the paths the currents took to reach their destinations.

Place the decoupling capacitors as close to the package as possible (ideally directly against the device).

Avoid running digital lines under the device because this couples noise onto the die and allows the analog ground plane to run under the AD4130-8 to prevent noise coupling. The power supply lines to the AD4130-8 must use as wide a trace as possible to provide low impedance paths and reduce glitches on the power supply line. Shield fast switching signals like clocks with digital ground to prevent radiating noise to other sections of the board and never run clock signals near the analog inputs. Avoid crossover of digital and analog signals. Run traces on opposite sides of the board at right angles to each other. This reduces the effects of feedthrough on the board. A microstrip technique is by far the best but is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground planes, whereas signals are placed on the solder side.

If using the AD4130-8 with split supply operation, a separate plane must be used for AV_{SS}.

ASSEMBLY GUIDELINES

For the WLCSP, heat is transferred through the solder balls to the PCB. Thermal impedance is dependent on PCB construction. More copper layers and ground via enable heat to be removed more effectively.

The PCB level reliability of the device is directly linked to the PCB type and design used. Using a PCB material that matches the coefficient of thermal expansion (CTE) of the silicon (for example, ceramic) provides the optimal mechanical performance. For organic material PCBs (for example, FR4) where the CTE is different from that of the silicon, the use of underfill can increase the mechanical performance. For organic PCB thickness >0.8 mm, consider using underfill. Particular attention must be given to the underfill material selection to match the material properties with the application use conditions.

Consider using low alpha material in the system assembly to reduce the soft error rate (SER).

APPLICATIONS INFORMATION

The AN-617 Application Note provides information on PCB layout and assembly for the WLCSP.

The AN-772 Application Note provides information on PCB layout and assembly for the LFCSP.

AD4130-8 REGISTERS

The AD4130-8 has programmable user configuration registers that are used to configure the device. Table 73 contains the complete list of the AD4130-8 user configuration registers. Table 73 shows a complete list of the user configuration registers. See the AD4130-8 Register Summary and Registers Details sections for details about the functions of each of the bits. The access column specifies whether the register comprises only read-only bits (R) or a mix of read only and read/write bits (R/W). Read-only bits cannot be overwritten by an SPI write transaction, whereas read/write bits can. Table 73 also shows if each register is a single byte or multibyte register. See the Digital Interface section for a detailed description of how to communicate with the AD4130-8.

Table 73. User Configuration Register Names and Descriptions[1]

Address	Name	Description	Length	Reset	Access
N/A[2]	COMMS	Communication register	Single byte	N/A	W
0x00	STATUS	Status register	Single byte	0x10	R
0x01	ADC_CONTROL	ADC control register	Two bytes	0x4000	R/W
0x02	DATA	Data register	Three bytes	0x000000	R
0x03	IO_CONTROL	Input/output control register	Two bytes	0x0000	R/W
0x04	VBIAS_CONTROL	VBIAS control register	Two bytes	0x0000	R/W
0x05	ID	Identification register	Single byte	0x0X[3]	R
0x06	ERROR	Error register	Two bytes	0x0000	R/W
0x07	ERROR_EN	Error enable register	Two bytes	0x0040	R/W
0x08	MCLK_COUNT	MCLK count register	Single byte	0x00	R
0x09 to 0x18 by 1	CHANNEL_m (m = 0 to 15)	Channel m configuration registers	Three bytes	0xXXXXXX[4]	R/W
0x19 to 0x20 by 1	CONFIG_n (n = 0 to 7)	Configuration registers (ADC Setup n)	Two bytes	0x0000	R/W
0x21 to 0x28 by 1	FILTER_n (n = 0 to 7)	Filter configuration registers (ADCs Setup n)	Three bytes	0x002030	R/W
0x29 to 0x30 by 1	OFFSET_n (n = 0 to 7)	Offset registers (ADC Setup n)	Three bytes	0x800000	R/W
0x31 to 0x38 by 1	GAIN_n (n = 0 to 7)	Gain registers (ADC Setup n)	Three bytes	0xXXXXXX[5]	R/W
0x39	MISC	Miscellaneous register	Two bytes	0x0000	R/W
0x3A	FIFO_CONTROL	FIFO control register	Three bytes	0x040200	R/W
0x3B	FIFO_STATUS	FIFO status register	Single byte	0x01	R
0x3C	FIFO_THRESHOLD	FIFO threshold register	Three bytes	0xFFF000	R/W
0x3D	FIFO_DATA	FIFO data register	Three bytes	0x000000	R

1 Blank cells are not applicable.

2 N/A means not applicable.

3 See Identification Register section for details.

4 CHANNEL_0 default value is 0x800100. All other channels default value is 0x000100.

5 Nominal value: 0x555555. The AD4130-8 is factory calibrated at ambient temperature and with a gain of 1 and PGA_BYP_n = 0, and the resulting gain coefficient is loaded to the GAIN_n registers of the device as default value.

AD4130-8 REGISTER SUMMARY

Table 74. User Configuration Register Summary[1]

Addr.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
N/A[2]	COMMS	[7:0]	$\overline{\text{WEN}}$	R/$\overline{\text{W}}$	RS[5:0]						N/A	W
0x00	STATUS	[7:0]	$\overline{\text{RDY}}$	MASTER_ERR	RESERVED	POR_FLAG	CH_ACTIVE				0x10	R
0x01	ADC_CONTROL	[15:8]	RESERVED	BIPOLAR	INT_REF_VAL	DOUT_DIS_DEL	CONT_READ	DATA_STATUS	CSB_EN	INT_REF_EN	0x4000	R/W
		[7:0]	RESERVED	DUTY_CYC_RATIO	MODE				CLK_SEL			
0x02	DATA	[23:16]	DATA[23:16]								0x000000	R
		[15:8]	DATA[15:8]									
		[7:0]	DATA[7:0]									

AD4130-8 REGISTERS

Table 74. User Configuration Register Summary[1] (Continued)

Addr.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x03	IO_CONTROL	[15:8]	RESERVED					SYNCB_CLEAR	INT_PIN_SEL		0x0000	R/W
		[7:0]	GPO_DATA_P4	GPO_DATA_P3	GPO_DATA_P2	GPO_DATA_P1	GPO_CTRL_P4	GPO_CTRL_P3	GPO_CTRL_P2	GPO_CTRL_P1		
0x04	VBIAS_CONTROL	[15:8]	VBIAS_15	VBIAS_14	VBIAS_13	VBIAS_12	VBIAS_11	VBIAS_10	VBIAS_9	VBIAS_8	0x0000	R/W
		[7:0]	VBIAS_7	VBIAS_6	VBIAS_5	VBIAS_4	VBIAS_3	VBIAS_2	VBIAS_1	VBIAS_0		
0x05	ID	[7:0]	RESERVED				SILICON_ID		MODEL_ID		0x0X[3]	R
0x06	ERROR	[15:8]	RESERVED				AINP_OV_UV_ERR	AINM_OV_UV_ERR	REF_OV_UV_ERR	REF_DETECT_ERR	0x0000	R/W
		[7:0]	ADC_ERR	SPI_IGNORE_ERR	SPI_SCLK_CNT_ERR	SPI_READ_ERR	SPI_WRITE_ERR	SPI_CRC_ERR	MM_CRC_ERR	ROM_CRC_ERR		
0x07	ERROR_EN	[15:8]	RESERVED			MCLK_CNT_EN	AINP_OV_UV_ERR_EN	AINM_OV_UV_ERR_EN	REF_OV_UV_ERR_EN	REF_DETECT_ERR_EN	0x0040	R/W
		[7:0]	ADC_ERR_EN	SPI_IGNORE_ERR_EN	SPI_SCLK_CNT_ERR_EN	SPI_READ_ERR_EN	SPI_WRITE_ERR_EN	SPI_CRC_ERR_EN	MM_CRC_ERR_EN	ROM_CRC_ERR_EN		
0x08	MCLK_COUNT	[7:0]	MCLK_COUNT								0x00	R
0x09 to 0x18	CHANNEL_m (m = 0 to 15)	[23:16]	ENABLE_m	SETUP_m			PDSW_m	THRES_EN_m	AINP_m[4:3]		0xXXXXXX[4]	R/W
		[15:8]	AINP_m[2:0]			AINM_m						
		[7:0]	I_OUT1_CH_m				I_OUT0_CH_m					
0x19 to 0x20	CONFIG_n (n = 0 to 7)	[15:8]	I_OUT1_n			I_OUT0_n			BURNOUT_n		0x0000	R/W
		[7:0]	REF_BUFP_n	REF_BUFM_n	REF_SEL_n		PGA_n			PGA_BYP_n		
0x21 to 0x28	FILTER_n (n = 0 to 7)	[23:16]	SETTLE_n			REPEAT_n					0x002030	R/W
		[15:8]	FILTER_MODE_n				RESERVED	FS_n[10:8]				
		[7:0]	FS_n[7:0]									
0x29 to 0x30	OFFSET_n (n = 0 to 7)	[23:16]	OFFSET_n[23:16]								0x800000	R/W
		[15:8]	OFFSET_n[15:8]									
		[7:0]	OFFSET_n[7:0]									
0x31 to 0x38	GAIN_n (n = 0 to 7)	[23:16]	GAIN_n[23:16]								0xXXXXXX[5]	R/W
		[15:8]	GAIN_n[15:8]									
		[7:0]	GAIN_n[7:0]									
0x39	MISC	[15:8]	RESERVED	PD_ALDO	CAL_RANGE_X2	RESERVED				STBY_OUT_EN	0x0000	R/W
		[7:0]	STBY_DIAGNOSTICS_EN	STBY_GPO_EN	STBY_PDSW_EN	STBY_BURNOUT_EN	STBY_VBIAS_EN	STBY_IEXC_EN	STBY_REFHOL_EN	STBY_INTREF_EN		

AD4130-8 REGISTERS

Table 74. User Configuration Register Summary[1] (Continued)

Addr.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x3A	FIFO_CONTROL	[23:16]	RESERVED				ADD_FIFO_STATUS	ADD_FIFO_HEADER	FIFO_MODE		0x040200	R/W
		[15:8]	RESERVED	FIFO_WRITE_ERR_INT_EN	FIFO_READ_ERR_INT_EN	THRES_HIGH_INT_EN	THRES_LOW_INT_EN	OVERRUN_INT_EN	WATERMARK_INT_EN	EMPTY_INT_EN		
		[7:0]	WATERMARK									
0x3B	FIFO_STATUS	[7:0]	MASTER_ERR	FIFO_WRITE_ERR	FIFO_READ_ERR	THRES_HIGH_FLAG	THRES_LOW_FLAG	OVERRUN_FLAG	WATERMARK_FLAG	EMPTY_FLAG	0x01	R
0x3C	FIFO_THRESHOLD	[23:16]	THRES_HIGH_VAL[11:4]								0xFFF000	R/W
		[15:8]	THRES_HIGH_VAL[3:0]				THRES_LOW_VAL[11:8]					
		[7:0]	THRES_LOW_VAL[7:0]									
0x3D	FIFO_DATA	[23:16]	FIFO_DATA[23:16]								0x000000	R
		[15:8]	FIFO_DATA[15:8]									
		[7:0]	FIFO_DATA[7:0]									

1 Blank cells are not applicable.

2 N/A means not applicable.

3 See Identification Register section for details.

4 CHANNEL_0 default value is 0x800100. All other channels default value is 0x000100.

5 Nominal value: 0x555555. The AD4130-8 is factory calibrated at ambient temperature and with a Gain of 1 and PGA_BYP_n = 0, and the resulting gain coefficient is loaded to the GAIN_n registers of the device as default value.

REGISTERS DETAILS

Communication Register

Address: N/A, Reset: 0x10, Name: COMMS

All communications to the device must start with a write operation to the communications register.

Table 75. Bit Descriptions for COMMS Register

Bits	Bit Name	Settings	Description
7	$\overline{WEN}$		Write Enable Bit. A 0 must be written to this bit so that the write to the communications register occurs. If a 1 is the first bit written, the device does not clock on to subsequent bits in the register. It stays at this bit location until a 0 is written to this bit. As soon as a 0 is written to the $\overline{WEN}$ bit, the next seven bits are loaded to the communications register.
		0	Communication Allowed.
		1	No Communication Allowed.
6	R/$\overline{W}$		A 0 in this bit location indicates that the next operation is a write to a specified register. A 1 in this position indicates that the next operation is a read from the designated register.
		0	Write Operation.
		1	Read Operation.
5:0	RS[5:0]		Register address bits. These address bits select which registers of the device are being selected during this serial interface communication. See Table 74 for a list of all registers and relative addresses.

AD4130-8 REGISTERS

Status Register

Address: 0x00, Reset: 0x10, Name: STATUS

ADC and interface status information register.

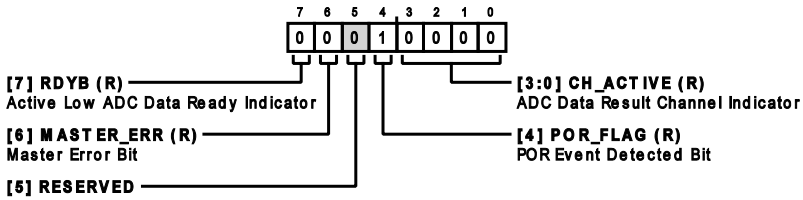


Figure 109.

Table 76. Bit Descriptions for Status Register

Bits	Bit Name	Settings	Description	Reset	Access
7	RDYB		Active Low ADC Data Ready Indicator. The RDYB bit is used to indicate availability of ADC data. Because the RDYB bit is treated as an interrupt event, when it is set to 0, the data ready pin goes low. Conversely, the data ready pin automatically clears (goes high) when the RDYB bit is set to 1.	0x0	R
		0	ADC Data Ready. The RDYB bit is set to 0 when the ADC writes a new result to the DATA register, or in any ADC calibration mode when the ADC writes to the OFFSET_n and GAIN_n registers. The RDYB bit is set back to 1 automatically by a read of the data register. A read of OFFSET_n register or GAIN_n register does not affect this bit.		
		1	Data Not Ready. The RDYB bit is set to 1 to indicate that the ADC is placed into idle or standby mode, to indicate a new calibration started, or to indicate that a new conversion started and new data is not yet available. The RDYB bit is set to 1 in continuous conversion mode. Asserting the $\overline{SYNC}$ pin (taking it low) also sets the RDYB bit to 1 if the data register is not read after a conversion result. The RDYB bit is set to 1 four MCLK cycles before the next conversion result is written to indicate that the data register is about to be updated, and therefore, is not read. If the data register is being read when an ADC result is written, that write is aborted. There is no mixing of data values, but one ADC conversion is missed.		
6	MASTER_ERR		Master Error Bit. This bit is set when any of the errors in the error register are set to 1. The MASTER_ERR bit of the FIFO_STATUS register is also set to 1 when this MASTER_ERR bit is set to 1. This bit is automatically cleared once there are no errors in the error register.	0x0	R
		0	No Error Detected.		
		1	Master Error Detected.		
5	RESERVED		Reserved.	0x0	R
4	POR_FLAG		POR Event Detected Bit. A POR is triggered at power-up or when the IOV_{DD} and/or digital LDO power supply dips below the threshold value. This bit is set to 1 when a POR event occurs and is cleared when the user reads the status register.	0x1	R
		0	No POR Event Detected.		
		1	POR Event Detected.		
[3:0]	CH_ACTIVE		ADC Data Result Channel Indicator. These bits indicate which channel was active for the ADC conversion whose result is currently in the data register. This may be different from the channel currently being converted. These values are a direct map from the CHANNEL_m register currently active. CHANNEL_0 results in CH_ACTIVE = 0b0000 while CHANNEL_15 results in CH_ACTIVE = 0b1111.	0x0	R

AD4130-8 REGISTERS

ADC Control Register

Address: 0x01, Reset: 0x4000, Name: ADC_CONTROL

Controls the operation mode of the ADC.

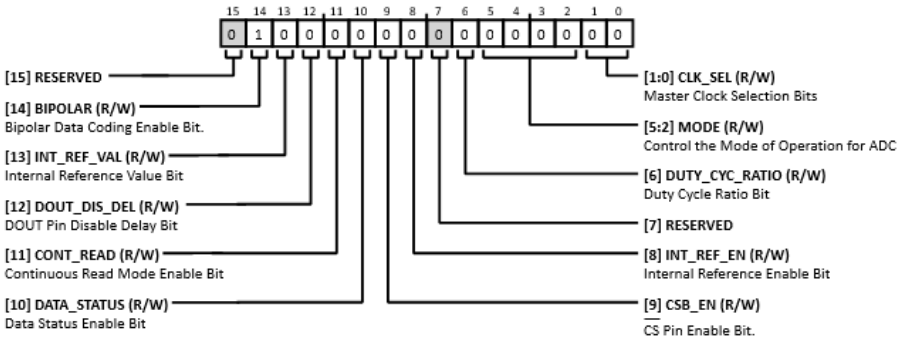


Figure 110.

Table 77. Bit Descriptions for ADC_CONTROL Register

Bits	Bit Name	Settings	Description	Reset	Access
15	RESERVED		Reserved.	0x0	R
14	BIPOLAR		Bipolar Data Coding Enable Bit. Set the output coding of the ADC. This is a digital correction–the ADC conversion is performed on a bipolar input span.	0x1	R/W
		0	Straight Binary (Unipolar) Coding. Input range: 0 V to V_{REF}/gain. V_{REF}/gain: 0xFFFFFF 0: 0x000000		
		1	Offset Binary (Bipolar) Coding. Input range: $-V_{REF}$/gain to V_{REF}/gain V_{REF}/gain: 0xFFFFFF 0: 0x800000 $-V_{REF}$/gain: 0x000000		
13	INT_REF_VAL		Internal Reference Value Bit. Specifies the voltage of the internal precision reference. This bit must be used in conjunction with the INT_REF_EN bit in this same register.	0x0	R/W
		0	2.5 V.		
		1	1.25 V.		
12	DOUT_DIS_DEL		DOUT (WLCSP) or DOUT/$\overline{RDY}$ (LFCSP) Pin Disable Delay Bit. This bit controls the SCLK inactive edge to the DOUT pin disable time when the CSB_EN bit is set to 0 in the ADC_CONTROL register.	0x0	R/W
		0	Delay = 10 ns.		
		1	Delay = 100 ns.		
11	CONT_READ		Continuous Read Mode Enable Bit. This bit enables the continuous read of the data register. In continuous read mode, it is not required to write to the COMMS register before reading ADC data. Instead, apply the required number of SCLKs after the data ready signal goes low. The data ready signal acts as a framing signal during continuous read. SCLKs are ignored until the data ready signal goes low. This means that each ADC result can be read once. In addition, if a read is still in progress four MCLK cycles before the next conversion, the read is abandoned, and the data ready signal is deasserted (set high). If CRC is active, it is possible to determine that a read is not valid. To exit continuous read mode, issue a software reset command (64 1s) or write a read data command (0x42). No CRC is required if CRC is enabled. This feature is disabled if the FIFO is enabled.	0x0	R/W
		0	Continuous Read Mode Disabled.		
		1	Continuous Read Mode Enabled.		

AD4130-8 REGISTERS

Table 77. Bit Descriptions for ADC_CONTROL Register (Continued)

Bits	Bit Name	Settings	Description	Reset	Access
10	DATA_STATUS		Data Status Enable Bit. When this bit is set to 1, the status register content is appended to the data register output so that the channel status information is transmitted with the data. Thus, the format for reading the data register becomes (DATA, Bits[23:0], STATUS, Bits[7:0]). This aids in identifying the channel associated with the conversion being read in the data register, as well as correlate statuses with the data being read.	0x0	R/W
		0	Status Not Appended.		
		1	Status Appended to Data.		
9	CSB_EN		$\overline{CS}$ Pin Enable Bit. This bit controls the $\overline{CS}$ pin functionality and the SPI mode.	0x0	R/W
		0	$\overline{CS}$ Pin Functionality Disabled. SPI interface in 3-wire mode. The interface is reset on last rising edge of SCLK. Therefore, when reading from the device, the DOUT pin (WLCSP) is disabled on the last rising edge of SCLK or DOUT/$\overline{RDY}$ pin (LFCSP) switches from data output to data ready functionality on last rising edge of SCLK (assuming that data ready signal is configured to be sent out to the DOUT (WLCSP) or DOUT/$\overline{RDY}$ (LFCSP) pin). This timing can be changed via the DOUT_DIS_DEL bit in the ADC_CONTROL register. Attention must be paid to supply the correct number of clocks for the appropriate register in a write or read command. Register sizes can be 8-bit/16-bit/24-bit and enabling CRC and appending statuses in some cases also increases the data width. The $\overline{CS}$ pin must be tied low to keep the DOUT (WLCSP) or DOUT/$\overline{RDY}$ (LFCSP) pin enabled. The $\overline{CS}$ pin can still be held high to tristate the DOUT (WLCSP) or DOUT/$\overline{RDY}$ (LFCSP) pin.		
		1	$\overline{CS}$ Pin Functionality Enabled. SPI interface in 4-wire mode. The interface is reset on the rising edge of $\overline{CS}$. Therefore, when reading from the device, the DOUT (WLCSP) or DOUT/$\overline{RDY}$ (LFCSP) pin switches from data output functionality to data ready interrupt functionality on the rising edge of $\overline{CS}$ (assuming that the data ready signal is configured to be sent out to the DOUT (WLCSP) or DOUT/$\overline{RDY}$ (LFCSP) pin). The user can enable the SPI_WRITE_ERR bit, SPI_READ_ERR bit, and SPI_SCLK_CNT_ERR bit, as these are only valid when $\overline{CS}$ is enabled. When $\overline{CS}$ is high, the DOUT (WLCSP) or DOUT/$\overline{RDY}$ (LFCSP) pin is tristated.		
8	INT_REF_EN		Internal Reference Enable Bit. When the internal precision reference is enabled, the value seen at the REFOUT pin depends on the setting of INT_REF_VAL bit in this same register.	0x0	R/W
		0	Internal Reference Disabled (Default).		
		1	Internal Reference Enabled.		
7	RESERVED		Reserved.	0x0	R
6	DUTY_CYC_RATIO		Duty Cycle Ratio Bit. This bit controls the ratio for which the device is in standby. Duty cycling mode uses the conversion time of all active channels (disregarding digital postprocessing time and wake-up time) as time reference for active time, and the standby time is derived as multiples of that. For this bit to be effective, the MODE bitfield in this register must be set to duty cycling mode (0b1001).	0x0	R/W
		0	1/4 Duty Cycle. The device is active 1/4 of the time and in standby for 3/4 of the time.		
		1	1/16 Duty Cycle. The device is active 1/16 of the time and in standby for 15/16 of the time.		
[5:2]	MODE		Control the Mode of Operation for ADC.	0x0	R/W
		0000	Continuous Conversion Mode.		
		0001	Single Sequence Mode.		
		0010	Standby Mode.		
		0011	Power-Down Mode. To go to power-down mode, the device must be in standby mode. Otherwise, the device goes to continuous conversion mode. This procedure serves as a safety feature to prevent accidental/unwanted transitions to power-down mode.		
		0100	Idle Mode. The digital filter and the modulator are held in reset. There is no change to anything else.		
		0101	Internal Offset Calibration (Zero Scale). The device returns to idle mode once calibration is completed.		
		0110	Internal Gain Calibration (Full Scale). The device returns to idle mode once calibration is completed.		
		0111	System Offset Calibration (Zero Scale). The device returns to idle mode once calibration is completed.		
		1000	System Gain Calibration (Full Scale). The device returns to idle mode once calibration is completed.		

AD4130-8 REGISTERS

Table 77. Bit Descriptions for ADC_CONTROL Register (Continued)

Bits	Bit Name	Settings	Description	Reset	Access
		1001	Duty Cycling Mode. The device cycles between converting the selected sequence and standby based on the DUTY_CYC_RATIO bit in this register.		
		1010	Single Sequence + idle by $\overline{\text{SYNC}}$ Mode. The device cycles between converting the selected sequence and idle mode based on the $\overline{\text{SYNC}}$ pin pulses from high to low.		
		1011	Single Sequence + STBY by $\overline{\text{SYNC}}$ Mode. The device cycles between converting the selected sequence and standby based on the $\overline{\text{SYNC}}$ pin pulses from high to low.		
		1100 to 1111	Reserved.		
[1:0]	MCLK_SEL		Master Clock Selection Bits.	0x0	R/W
		00	Internal 76.8 kHz–Output Off. Internal clock used as clock source, but not available at the CLK pin.		
		01	Internal 76.8 kHz–Output On. Internal clock used as clock source, and available at the CLK pin.		
		10	External 76.8 kHz. External CLK pin used as clock source.		
		11	External 153.6 kHz. External CLK pin used as clock source after being divided by 2 internally.		

ADC Conversion Result Register

Address: 0x02, Reset: 0x000000, Name: DATA

Stores latest ADC result.

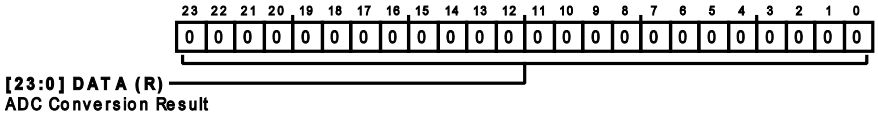


Figure 111.

Table 78. Bit Descriptions for DATA Register

Bits	Bit Name	Settings	Description	Reset	Access
[23:0]	DATA		ADC Conversion Result. This register contains the result of the latest ADC conversion.	0x0	R

Input/Output Control Register

Address: 0x03, Reset: 0x0000, Name: IO_CONTROL

Controls some of the input/output ports.

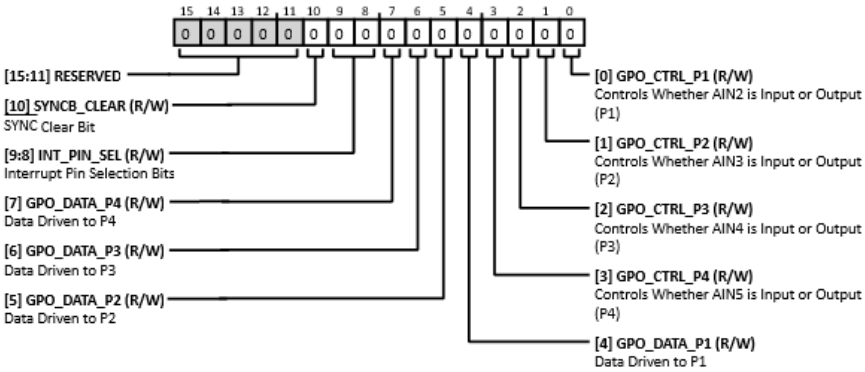


Figure 112.

AD4130-8 REGISTERS

Table 79. Bit Descriptions for IO_CONTROL Register

Bits	Bit Name	Settings	Description	Reset	Access
[15:11]	RESERVED		Reserved.	0x0	R
10	SYNCB_CLEAR		$\overline{\text{SYNC}}$ Clear Bit. This bit allows clearing the FIFO via the $\overline{\text{SYNC}}$ pin pulse.	0x0	R/W
		0	Disabled. Clearing of FIFO contents via $\overline{\text{SYNC}}$ is disabled.		
		1	Enabled. Clearing of FIFO contents via $\overline{\text{SYNC}}$ is enabled.		
[9:8]	INT_PIN_SEL		Data Ready/FIFO Interrupt Pin Selection Bits. These bits select what pin the Data ready/FIFO interrupt signal is sent to. When the FIFO is disabled, the data ready signal acts as the interrupt event. Otherwise, the FIFO interrupt event is determined by the configuration of the FIFO_CONTROL register.	0x0	R/W
		00	INT Pin (WLCSP) or DOUT/$\overline{\text{RDY}}$ Pin (LFCSP) for the Data Ready Signal. INT Pin (WLCSP)/ Unused (LFCSP) for the FIFO Interrupt signal.		
		01	CLK Pin. The data ready/FIFO interrupt signal is sent to the CLK pin. This setting takes priority on the CLK_SEL bit setting in the ADC_CONTROL register.		
		10	P2 (AIN3) Pin. The data ready/FIFO interrupt signal is sent to the P2 pin. This setting takes priority on the GPO_CTRL_P2 bit of the IO_CONTROL register.		
		11	DOUT Pin (WLCSP) or DOUT/$\overline{\text{RDY}}$ Pin (LFCSP). The data ready signal is sent to the DOUT pin (WLCSP) or DOUT/$\overline{\text{RDY}}$ pin (LFCSP). This option is unused for the FIFO interrupt signal.		
7	GPO_DATA_P4		Data Driven to P4. When the pin is configured as an output in GPO_CTRL_P4.	0x0	R/W
6	GPO_DATA_P3		Data Driven to P3. When the pin is configured as an output in GPO_CTRL_P3.	0x0	R/W
5	GPO_DATA_P2		Data Driven to P2. When the pin is configured as an output in GPO_CTRL_P2.	0x0	R/W
4	GPO_DATA_P1		Data Driven to P1. When the pin is configured as an output in GPO_CTRL_P1.	0x0	R/W
3	GPO_CTRL_P4		Controls Whether AIN5 is Input or Output (P4). Functions as standby pin (via the STBY_OUT_EN bit in the MISC register) and takes highest priority and overrides its other functions.	0x0	R/W
		0	GPIO Has Specific Input Function.		
		1	GPIO Functions as Output.		
2	GPO_CTRL_P3		Controls Whether AIN4 is Input or Output (P3).	0x0	R/W
		0	GPIO Has Specific Input Function.		
		1	GPIO Functions as Output.		
1	GPO_CTRL_P2		Controls Whether AIN3 is Input or Output (P2). Functions as an interrupt pin (via the INT_PIN_SEL bit of the IO_CONTROL Register) and takes highest priority and overrides its other functions.	0x0	R/W
		0	GPIO Has Specific Input Function.		
		1	GPIO Functions as Output.		
0	GPO_CTRL_P1		Controls Whether AIN2 is Input or Output (P1).	0x0	R/W
		0	GPIO Has Specific Input Function.		
		1	GPIO Functions as Output.		

AD4130-8 REGISTERS

VBIAS Control Register

Address: 0x04, Reset: 0x0000, Name: VBIAS_CONTROL

Select output VBIAS on the analog input pins.

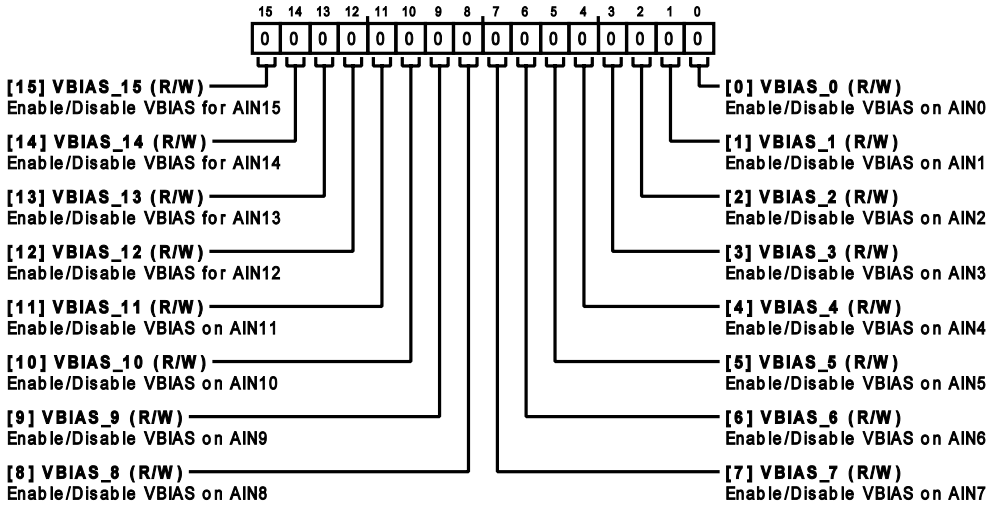


Figure 113.

Table 80. Bit Descriptions for VBIAS_CONTROL Register

Bits	Bit Name	Settings	Description	Reset	Access
15	VBIAS_15		Enable/Disable VBIAS for AIN15.	0x0	R/W
		0	VBIAS Disabled on This Pin.		
		1	VBIAS Enabled on This Pin.		
14	VBIAS_14		Enable/Disable VBIAS for AIN14.	0x0	R/W
		0	VBIAS Disabled on This Pin.		
		1	VBIAS Enabled on This Pin.		
13	VBIAS_13		Enable/Disable VBIAS for AIN13.	0x0	R/W
		0	VBIAS Disabled on This Pin.		
		1	VBIAS Enabled on This Pin.		
12	VBIAS_12		Enable/Disable VBIAS for AIN12.	0x0	R/W
		0	VBIAS Disabled on This Pin.		
		1	VBIAS Enabled on This Pin.		
11	VBIAS_11		Enable/Disable VBIAS on AIN11.	0x0	R/W
		0	VBIAS Disabled on This Pin.		
		1	VBIAS Enabled on This Pin.		
10	VBIAS_10		Enable/Disable VBIAS on AIN10.	0x0	R/W
		0	VBIAS Disabled on This Pin.		
		1	VBIAS Enabled on This Pin.		
9	VBIAS_9		Enable/Disable VBIAS on AIN9.	0x0	R/W
		0	VBIAS Disabled on This Pin.		
		1	VBIAS Enabled on This Pin.		
8	VBIAS_8		Enable/Disable VBIAS on AIN8.	0x0	R/W

AD4130-8 REGISTERS

Table 80. Bit Descriptions for VBIAS_CONTROL Register (Continued)

Bits	Bit Name	Settings	Description	Reset	Access
		0	VBIAS Disabled on This Pin.		
		1	VBIAS Enabled on This Pin.		
7	VBIAS_7		Enable/Disable VBIAS on AIN7.	0x0	R/W
		0	VBIAS Disabled on This Pin.		
		1	VBIAS Enabled on This Pin.		
6	VBIAS_6		Enable/Disable VBIAS on AIN6.	0x0	R/W
		0	VBIAS Disabled on This Pin.		
		1	VBIAS Enabled on This Pin.		
5	VBIAS_5		Enable/Disable VBIAS on AIN5.	0x0	R/W
		0	VBIAS Disabled on This Pin.		
		1	VBIAS Enabled on This Pin.		
4	VBIAS_4		Enable/Disable VBIAS on AIN4.	0x0	R/W
		0	VBIAS Disabled on This Pin.		
		1	VBIAS Enabled on This Pin.		
3	VBIAS_3		Enable/Disable VBIAS on AIN3.	0x0	R/W
		0	VBIAS Disabled on This Pin.		
		1	VBIAS Enabled on This Pin.		
2	VBIAS_2		Enable/Disable VBIAS on AIN2.	0x0	R/W
		0	VBIAS Disabled on This Pin.		
		1	VBIAS Enabled on This Pin.		
1	VBIAS_1		Enable/Disable VBIAS on AIN1.	0x0	R/W
		0	VBIAS Disabled on This Pin.		
		1	VBIAS Enabled on This Pin.		
0	VBIAS_0		Enable/Disable VBIAS on AIN0.	0x0	R/W
		0	VBIAS Disabled on This Pin.		
		1	VBIAS Enabled on This Pin.		

AD4130-8 REGISTERS

Identification Register

Address: 0x05, Reset: 0x0X, Name: ID

Returns an 8-bit ID of the device.

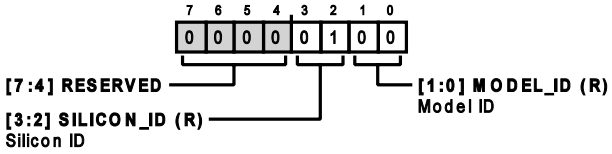


Figure 114.

Table 81. Bit Descriptions for ID Register

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	RESERVED		Reserved.	0x0	R
[3:2]	SILICON_ID		Silicon ID.	0x1	R
[1:0]	MODEL_ID		Model ID. These bits are set by default for each model and are read only.		R
		00	24-Bit WLCSP	0x0	
		01	24-Bit LFCSP	0x1	

Error Register

Address: 0x06, Reset: 0x0000, Name: ERROR

Each error bit in this register must be enabled in the ERROR_EN register to work as expected. All bits in this register are R/W1C.

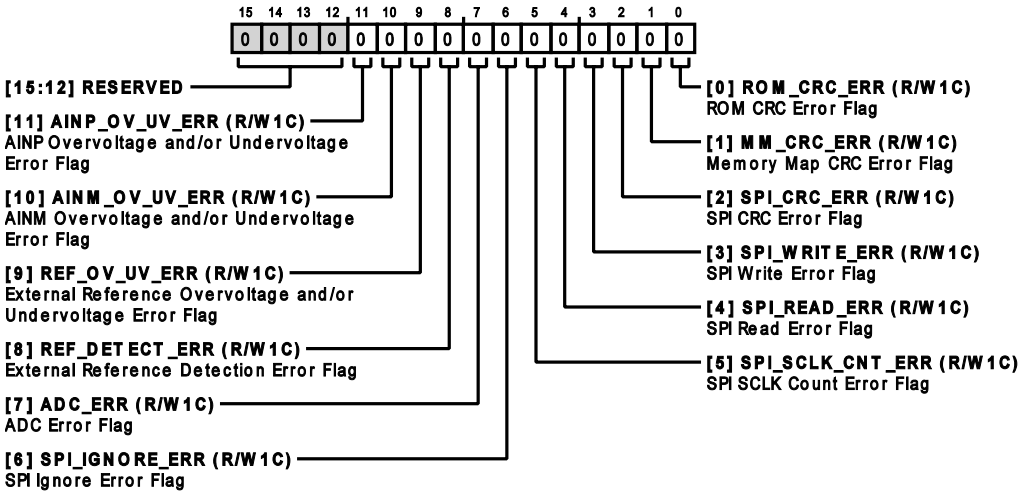


Figure 115.

Table 82. Bit Descriptions for ERROR Register

Bits	Bit Name	Settings	Description	Reset	Access
[15:12]	RESERVED		Reserved.	0x0	R
11	AINP_OV_UV_ERR		AINP Overvoltage and/or Undervoltage Error Flag. When set, this bit indicates that an overvoltage and/or undervoltage error on AINP is detected. Enable this error flag in the ERROR_EN register.	0x0	R/W1C

AD4130-8 REGISTERS

Table 82. Bit Descriptions for ERROR Register (Continued)

Bits	Bit Name	Settings	Description	Reset	Access
		0	No Error Detected.		
		1	AINP OV/UV Error Detected.		
10	AINM_OV_UV_ERR		AINM Overvoltage and/or Undervoltage Error Flag. When set, this bit indicates that an overvoltage and/or undervoltage error on AINM is detected. Enable this error flag in the ERROR_EN register.	0x0	R/W1C
		0	No Error Detected.		
		1	AINM OV/UV Error Detected.		
9	REF_OV_UV_ERR		External Reference Overvoltage and/or Undervoltage Error Flag. When set, this bit indicates that an overvoltage and/or undervoltage is detected on the external reference. Enable this error flag in the ERROR_EN register.	0x0	R/W1C
		0	No Error Detected.		
		1	REFIN OV/UV Error Detected.		
8	REF_DETECT_ERR		External Reference Detection Error Flag. When set, this bit indicates that the external reference voltage (REFINx(+) – REFINx(−)) is less than the threshold. Enable this error flag in the ERROR_EN register.	0x0	R/W1C
		0	No Error Detected.		
		1	REFIN Error Detected.		
7	ADC_ERR		ADC Error Flag. This error sets when one of the following ADC conversion/calibration errors is detected: ADC conversion result is clamped at positive full scale; ADC conversion result is clamped at negative full scale; ADC offset/gain calibration result outside specified range; modulator is in saturation. Enable this error flag in the ERROR_EN register.	0x0	R/W1C
		0	No Error Detected.		
		1	ADC Error Detected.		
6	SPI_IGNORE_ERR		SPI Ignore Error Flag. When set, this bit indicates that an SPI access is made at a time when it is ignored (such as while the ROM content is being downloaded). Enable this error flag in the ERROR_EN register.	0x0	R/W1C
		0	No Error Detected.		
		1	SPI Error Detected.		
5	SPI_SCLK_CNT_ERR		SPI SCLK Count Error Flag. When set, this bit indicates that the SCLKs on a given SPI frame are not multiples of eight. Enable this error flag in the ERROR_EN register.	0x0	R/W1C
		0	No Error Detected.		
		1	SCLK Count Error Detected.		
4	SPI_READ_ERR		SPI Read Error Flag. When set, this bit indicates that an SPI read is performed on an invalid address. Enable this error flag in the ERROR_EN register.	0x0	R/W1C
		0	No Error Detected.		
		1	SPI Read Error Detected.		
3	SPI_WRITE_ERR		SPI Write Error Flag. When set, this bit indicates that an SPI write is performed on an invalid address. Enable this error flag in the ERROR_EN register.	0x0	R/W1C
		0	No Error Detected.		
		1	SPI Write Error Detected.		
2	SPI_CRC_ERR		SPI CRC Error Flag. When set, this bit indicates that a CRC error on the SPI communication is detected. Enable this error flag in the ERROR_EN register.	0x0	R/W1C
		0	No Error Detected.		
		1	SPI CRC Error Detected.		
1	MM_CRC_ERR		Memory Map CRC Error Flag. When this error is enabled, periodic CRC checks on the memory map are performed. When set, this bit indicates that a change in the memory	0x0	R/W1C

AD4130-8 REGISTERS

Table 82. Bit Descriptions for ERROR Register (Continued)

Bits	Bit Name	Settings	Description	Reset	Access
			map contents (without actual writes) is detected. Enable this error flag in the ERROR_EN register.		
		0	No Error Detected.		
		1	Memory Map CRC Error Detected.		
0	ROM_CRC_ERR		ROM CRC Error Flag. A CRC calculation is performed on the ROM contents upon power-up. When set, this bit indicates that the ROM contents changed. Enable this error flag in the ERROR_EN register.	0x0	R/W1C
		0	No Error Detected.		
		1	ROM CRC Error Detected.		

Error Enable Register

Address: 0x07, Reset: 0x0040, Name: ERROR_EN

Each bit in this register enables a flag in the error register.

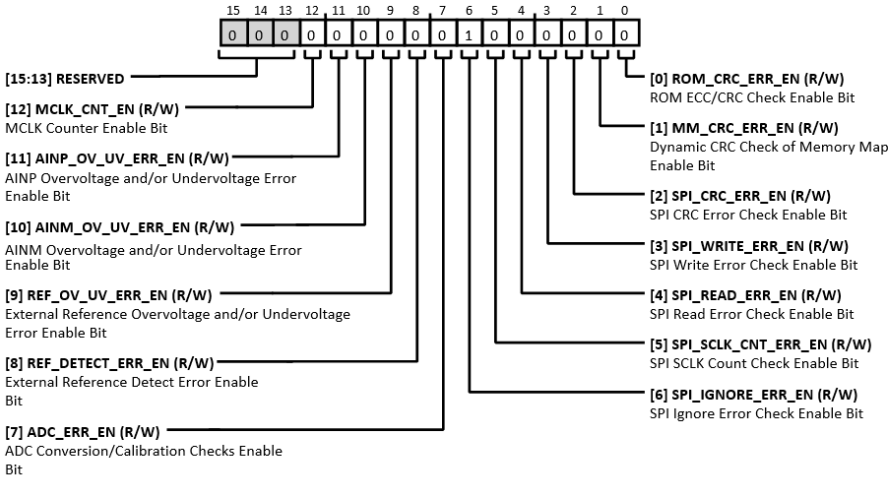


Figure 116.

Table 83. Bit Descriptions for ERROR_EN Register

Bits	Bit Name	Settings	Description	Reset	Access
[15:13]	RESERVED		Reserved.	0x0	R
12	MCLK_CNT_EN		MCLK Counter Enable Bit. The counter value is reported via the MCLK_COUNT register.	0x0	R/W
		0	MCLK Counter Disabled.		
		1	MCLK Counter Enabled.		
11	AINP_OV_UV_ERR_EN		AINP Overvoltage and/or Undervoltage Error Enable Bit. When set to 1, this bit enables the AINP overvoltage error seen in the error register.	0x0	R/W
		0	AINP OV/UV Error Disabled.		
		1	AINP OV/UV Error Enabled.		
10	AINM_OV_UV_ERR_EN		AINM Overvoltage and/or Undervoltage Error Enable Bit. When set to 1, this bit enables the AINM overvoltage/undervoltage error seen in the error register.	0x0	R/W
		0	AINM OV/UV Error Disabled.		

AD4130-8 REGISTERS

Table 83. Bit Descriptions for ERROR_EN Register (Continued)

Bits	Bit Name	Settings	Description	Reset	Access
		1	AINM OV/UV Error Enabled.		
9	REF_OV_UV_ERR_EN		External Reference Overvoltage and/or Undervoltage Error Enable Bit. When set to 1, this bit enables the external reference overvoltage/undervoltage error seen in the error register.	0x0	R/W
		0	REFIN OV/UV Error Disabled.		
		1	REFIN OV/UV Error Enabled.		
8	REF_DETECT_ERR_EN		External Reference Detect Error Enable Bit. When set to 1, this bit enables the external reference error seen in the error register.	0x0	R/W
		0	REFIN Error Disabled.		
		1	REFIN Error Enabled.		
7	ADC_ERR_EN		ADC Conversion/Calibration Checks Enable Bit. When set to 1, this bit enables ADC_ERR seen in the error register.	0x0	R/W
		0	ADC Error Disabled.		
		1	ADC Error Enabled.		
6	SPI_IGNORE_ERR_EN		SPI Ignore Error Check Enable Bit. Enabled by default. The error is reported via the SPI_IGNORE_ERR in the error register. An error is flagged if the user writes to the memory map during power-up while fuses are copied across, or if the user writes to the memory map while offset or gain calibration is performed.	0x1	R/W
		0	SPI Ignore Error Disabled.		
		1	SPI Ignore Error Enabled.		
5	SPI_SCLK_CNT_ERR_EN		SPI SCLK Count Check Enable Bit. To enable this function, CSB_EN must also be set to 1 in ADC_CONTROL. The SPI SCLK counter counts the number of SCLK pulses used in each read and write operation. $\overline{CS}$ must frame every read and write operation when this function is used. All read and write operations are multiples of eight SCLK pulses. If the SCLK counter counts the SCLK pulses and the result is not a multiple of eight, an error is flagged; the SPI_SCLK_CNT_ERR bit in the error register is set. If a write operation is performed, and the SCLK contains an insufficient number of SCLK pulses, the value is not written to the addressed register and the write operation is aborted.	0x0	R/W
		0	SPI SCLK Error Disabled.		
		1	SPI SCLK Error Enabled.		
4	SPI_READ_ERR_EN		SPI Read Error Check Enable Bit. To enable this function, CSB_EN must also be set to 1 in ADC_CONTROL. The error is reported via SPI_READ_ERR in the error register. The SPI_READ_ERR bit is flagged if the user attempts to read an invalid address.	0x0	R/W
		0	SPI Read Error Disabled.		
		1	SPI Read Error Enabled.		
3	SPI_WRITE_ERR_EN		SPI Write Error Check Enable Bit. To enable this function, CSB_EN must also be a 1 in ADC_CONTROL. The error is reported via SPI_WRITE_ERR in the error register. The SPI_WRITE_ERR bit is flagged if the user attempts to write to either an invalid or read-only address.	0x0	R/W
		0	SPI Write Error Disabled.		
		1	SPI Write Error Enabled.		
2	SPI_CRC_ERR_EN		SPI CRC Error Check Enable Bit. Using the checksum ensures that only valid data is written to a register and allows data read from a register to be validated. If an error occurs during a register write, the CRC_ERR bit is set in the error register. However, to ensure that the register write is successful, read back the register and verify the checksum.	0x0	R/W

AD4130-8 REGISTERS

Table 83. Bit Descriptions for ERROR_EN Register (Continued)

Bits	Bit Name	Settings	Description	Reset	Access
		0	SPI CRC Check is Disabled.		
		1	SPI CRC Check is Enabled.		
1	MM_CRC_ERR_EN		Dynamic CRC Check of Memory Map Enable Bit. The error is reported via MM_CRC_ERR in the error register. Memory map CRC is performed on all memory map contents except for read-only registers (for example, status, data, and MCLK_COUNT). The CRC is performed every 426.6 µs (2.4 kHz). Any future memory write to memory map recalculates CRC. This happens for following cases: user write; offset/gain calibration; when the MODE bits change from single sequence to idle at the end of single sequence mode conversions; when exiting continuous read mode, the CONT_READ bit changes to 0 in ADC_CONTROL.	0x0	R/W
		0	MM CRC Check Disabled.		
		1	MM CRC Check Enabled.		
0	ROM_CRC_ERR_EN		ROM ECC/CRC Check Enable Bit. ROM CRC is always performed on power-up and this bit enables reporting of error. The error is reported via ROM_CRC_ERR in the error register.	0x0	R/W
		0	ROM CRC/ECC Check Disabled.		
		1	ROM CRC/ECC Check Enabled.		

MCLK Counter Register

Address: 0x08, Reset: 0x00, Name: MCLK_COUNT

Returns the MCLK count value when functionality is enabled.

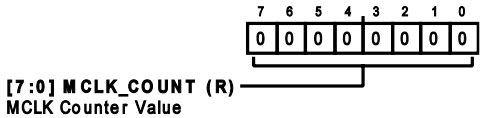


Figure 117.

Table 84. Bit Descriptions for MCLK_COUNT Register

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	MCLK_COUNT		MCLK Counter Value. This register allows the user to determine the frequency of the internal/external oscillator. Internally a clock counter increments every 131 pulses of the master clock (f_{MCLK} = 76.8 kHz), giving it an update rate of 586.26 Hz. The 8-bit counter wraps around on reaching its maximum value. Enable the MCLK counter functionality using the MCLK_CNT_EN bit in the ERROR_EN register.	0x00	R

AD4130-8 REGISTERS

Channel m Configuration Registers (m = 0 to 15)

Address: 0x09 to 0x18 (in Increments of 1), Reset: 0x800100 (CHANNEL_0), 0x000100 (All Other Channels), Name: CHANNEL_m (m = 0 to 15)

These registers allow the user to enable channels in the automated sequence, select plus and minus inputs, determine the availability of excitation currents on specific inputs, and enable thresholds for the FIFO. They also allow the user to select the ADC Setup n associated with each channel. An ADC setup is made up of configuration, filter, offset, and gain registers.

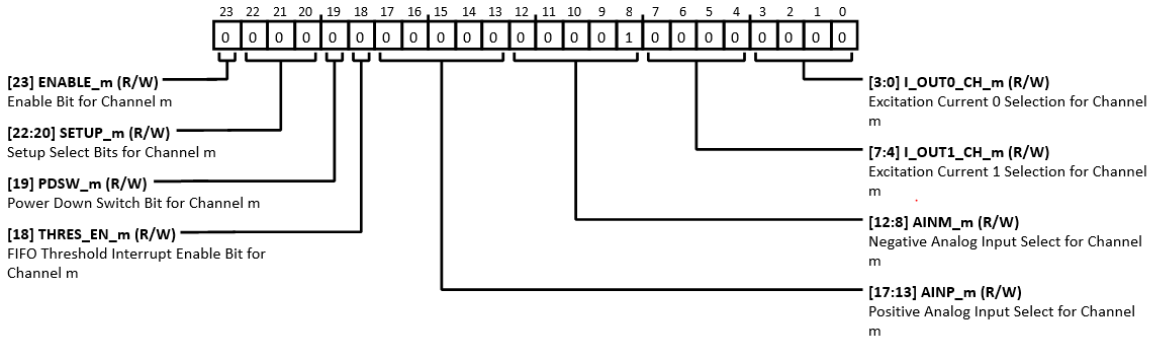


Figure 118.

Table 85. Bit Descriptions for CHANNEL_m Registers

Bits	Bit Name	Settings	Description	Reset	Access
23	ENABLE_m		Enable Bit for Channel m. This bit enables the relative channel to take part in the sequence. By default, only the ENABLE_0 bit for CHANNEL_0 is set to 1, and all the other ENABLE_m bits are set to 0. The order of conversions starts with the lowest enabled channel, then cycles through successively higher channel numbers, before wrapping around to the lowest channel again. When the ADC writes a result for a particular channel, the four LSBs of the status register are set to the channel number (range: 0 to 15). This allows the user to identify the channel that corresponds to the data being read.	0x1 (CHANNEL_0) 0x0 (CHANNEL_m)	R/W
		0	Channel Disabled.		
		1	Channel Enabled.		
[22:20]	SETUP_m		ADC Setup Select Bits for Channel m. An ADC setup comprises a set of four corresponding registers: (CONFIG_n, FILTER_n, OFFSET_n, and GAIN_n). For example, if a channel has a SETUP_m value of 0, its settings come from CONFIG_0, FILTER_0, OFFSET_0, and GAIN_0. All channels can use the same setup, in which case the same 3-bit value is written to these bits on all active channels, or up to eight channels can be configured differently.	0x0	R/W
		0	ADC Setup 0. CONFIG_0/FILTER_0/OFFSET_0/GAIN_0 configuration used to configure ADC for this channel.		
		1	ADC Setup 1. CONFIG_1/FILTER_1/OFFSET_1/GAIN_1 configuration used to configure ADC for this channel.		
		2	ADC Setup 2. CONFIG_2/FILTER_2/OFFSET_2/GAIN_2 configuration used to configure ADC for this channel.		
		3	ADC Setup 3. CONFIG_3/FILTER_3/OFFSET_3/GAIN_3 configuration used to configure ADC for this channel.		
		4	ADC Setup 4. CONFIG_4/FILTER_4/OFFSET_4/GAIN_4 configuration used to configure ADC for this channel.		
		5	ADC Setup 5. CONFIG_5/FILTER_5/OFFSET_5/GAIN_5 configuration used to configure ADC for this channel.		

AD4130-8 REGISTERS

Table 85. Bit Descriptions for CHANNEL_m Registers (Continued)

Bits	Bit Name	Settings	Description	Reset	Access
		6	ADC Setup 6. CONFIG_6/FILTER_6/OFFSET_6/GAIN_6 configuration used to configure ADC for this channel.		
		7	ADC Setup 7. CONFIG_7/FILTER_7/OFFSET_7/GAIN_7 configuration used to configure ADC for this channel.		
19	PDSW_m		Power-Down Switch Bit for Channel m. This bit enables the option to connect the PSW pin to AV_{SS} on a per-channel basis, except when the device is in power-down or standby mode. If this bit is 1, the power-down switch is enabled for this channel, and anything connected to the PSW pin is shorted to AV_{SS}. In power-down mode, the switch is opened automatically (that is, disabled). While the device is in standby mode, the functionality of this bit is disabled if the STBY_PDSW_EN bit in the MISC register is set to 0.	0x0	R/W
		0	Power-Down Switch Off. The power-down switch is always disabled for this channel.		
		1	Power-Down Switch On. This allows the PSW pin to sink current.		
18	THRES_EN_m		FIFO Threshold Interrupt Enable Bit for Channel m. When this bit is set to 1, the conversion data from this channel is monitored for threshold crossing per THRES_LOW_VAL and THRES_HIGH_VAL of the FIFO_THRESHOLD register. This bit has no effect when the FIFO is disabled.	0x0	R/W
[17:13]	AINP_m		Positive Analog Input Select for Channel m. These bits select which of the analog inputs is connected to the positive input for this channel.	0x0	R/W
		00000	AIN0.		
		00001	AIN1.		
		00010	AIN2.		
		00011	AIN3.		
		00100	AIN4.		
		00101	AIN5.		
		00110	AIN6.		
		00111	AIN7.		
		01000	AIN8.		
		01001	AIN9.		
		01010	AIN10.		
		01011	AIN11.		
		01100	AIN12.		
		01101	AIN13.		
		01110	AIN14.		
		01111	AIN15.		
		10000	Temperature Sensor.		
		10001	AV_{SS}.		
		10010	Internal Reference.		
		10011	DGND.		
		10100	$(AV_{DD} - AV_{SS})/6+$. Use in conjunction with $(AV_{DD} - AVSS)/6-$ to monitor supply $AV_{DD} - AV_{SS}$.		
		10101	$(AV_{DD} - AV_{SS})/6-$. Use in conjunction with $(AV_{DD} - AV_{SS})/6+$ to monitor supply $AV_{DD} - AV_{SS}$.		
		10110	$(IOV_{DD} - DGND)/6+$. Use in conjunction with $(IOV_{DD} - DGND)/6-$ to monitor $IOV_{DD} - DGND$.		
		10111	$(IOV_{DD} - DGND)/6-$. Use in conjunction with $(IOV_{DD} - DGND)/6+$ to monitor $IOV_{DD} - DGND$.		
		11000	$(ALDO - AV_{SS})/6+$. Use in conjunction with $(ALDO - AVSS)/6-$ to monitor the analog LDO.		
		11001	$(ALDO - AV_{SS})/6-$. Use in conjunction with $(ALDO - AVSS)/6+$ to monitor the analog LDO.		
		11010	(DLDO − DGND)/6+. Use in conjunction with (DLDO − DGND)/6− to monitor the digital LDO.		
		11011	(DLDO − DGND)/6−. Use in conjunction with (DLDO − DGND)/6+ to monitor the digital LDO.		

AD4130-8 REGISTERS

Table 85. Bit Descriptions for CHANNEL_m Registers (Continued)

Bits	Bit Name	Settings	Description	Reset	Access
		11100	V_MV_P. Use in conjunction with V_MV_M to apply a tens of mV_{P-P} signal to the ADC.		
		11101	V_MV_M. Use in conjunction with V_MV_P to apply a tens of mV_{P-P} signal to the ADC		
		11110	Reserved.		
		11111	Reserved.		
[12:8]	AINM_m		Negative Analog Input Select for Channel m. These bits select which of the analog inputs is connected to the negative input for this channel.	0x1	R/W
		00000	AIN0.		
		00001	AIN1.		
		00010	AIN2.		
		00011	AIN3.		
		00100	AIN4.		
		00101	AIN5.		
		00110	AIN6.		
		00111	AIN7.		
		01000	AIN8.		
		01001	AIN9.		
		01010	AIN10.		
		01011	AIN11.		
		01100	AIN12.		
		01101	AIN13.		
		01110	AIN14.		
		01111	AIN15.		
		10000	Temperature Sensor.		
		10001	AV_{SS}.		
		10010	Internal Reference.		
		10011	DGND.		
		10100	$(AV_{DD} - AV_{SS})/6+$. Use in conjunction with $(AV_{DD} - AV_{SS})/6-$ to monitor supply $AV_{DD} - AV_{SS}$.		
		10101	$(AV_{DD} - AV_{SS})/6-$. Use in conjunction with $(AV_{DD} - AV_{SS})/6+$ to monitor supply $AV_{DD} - AV_{SS}$.		
		10110	$(IOV_{DD} - DGND)/6+$. Use in conjunction with $(IOV_{DD} - DGND)/6-$ to monitor $IOV_{DD} - DGND$.		
		10111	$(IOV_{DD} - DGND)/6-$. Use in conjunction with $(IOV_{DD} - DGND)/6+$ to monitor $IOV_{DD} - DGND$.		
		11000	$(ALDO - AV_{SS})/6+$. Use in conjunction with $(ALDO - AV_{SS})/6-$ to monitor the analog LDO.		
		11001	$(ALDO - AV_{SS})/6-$. Use in conjunction with $(ALDO - AV_{SS})/6+$ to monitor the analog LDO.		
		11010	(DLDO − DGND)/6+. Use in conjunction with (DLDO − DGND)/6− to monitor the digital LDO.		
		11011	(DLDO − DGND)/6−. Use in conjunction with (DLDO − DGND)/6+ to monitor the digital LDO.		
		11100	V_MV_P. Use in conjunction with V_MV_M to apply a tens of mV_{P-P} signal to the ADC.		
		11101	V_MV_M. Use in conjunction with V_MV_P to apply a tens of mV_{P-P} signal to the ADC.		
		11110	Reserved.		
		11111	Reserved.		
[7:4]	I_OUT1_CH_m		Excitation Current 1 Selection for Channel m.	0x0	R/W
		0000	I_OUT1 is available on AIN0.		
		0001	I_OUT1 is available on AIN1.		
		0010	I_OUT1 is available on AIN2.		
		0011	I_OUT1 is available on AIN3.		
		0100	I_OUT1 is available on AIN4.		

AD4130-8 REGISTERS

Table 85. Bit Descriptions for CHANNEL_m Registers (Continued)

Bits	Bit Name	Settings	Description	Reset	Access
		0101	I_OUT1 is available on AIN5.		
		0110	I_OUT1 is available on AIN6.		
		0111	I_OUT1 is available on AIN7.		
		1000	I_OUT1 is available on AIN8.		
		1001	I_OUT1 is available on AIN9.		
		1010	I_OUT1 is available on AIN10.		
		1011	I_OUT1 is available on AIN11.		
		1100	I_OUT1 is available on AIN12.		
		1101	I_OUT1 is available on AIN13.		
		1110	I_OUT1 is available on AIN14.		
		1111	I_OUT1 is available on AIN15.		
[3:0]	I_OUT0_CH_m		Excitation Current 0 Selection for Channel m.	0x0	R/W
		0000	I_OUT0 is available on AIN0.		
		0001	I_OUT0 is available on AIN1.		
		0010	I_OUT0 is available on AIN2.		
		0011	I_OUT0 is available on AIN3.		
		0100	I_OUT0 is available on AIN4.		
		0101	I_OUT0 is available on AIN5.		
		0110	I_OUT0 is available on AIN6.		
		0111	I_OUT0 is available on AIN7.		
		1000	I_OUT0 is available on AIN8.		
		1001	I_OUT0 is available on AIN9.		
		1010	I_OUT0 is available on AIN10.		
		1011	I_OUT0 is available on AIN11.		
		1100	I_OUT0 is available on AIN12.		
		1101	I_OUT0 is available on AIN13.		
		1110	I_OUT0 is available on AIN14.		
		1111	I_OUT0 is available on AIN15.		

AD4130-8 REGISTERS

Configuration n Registers (n = 0 to 7)

Address: 0x19 to 0x20 (in Increments of 1), Reset: 0x0000, Name: CONFIG_n (n = 0 to 7)

These registers allow the user to configure excitation currents and burnout current values, reference mode and buffers, and the PGA mode for up to seven different ADC setups to be selected in the CHANNEL_m registers.

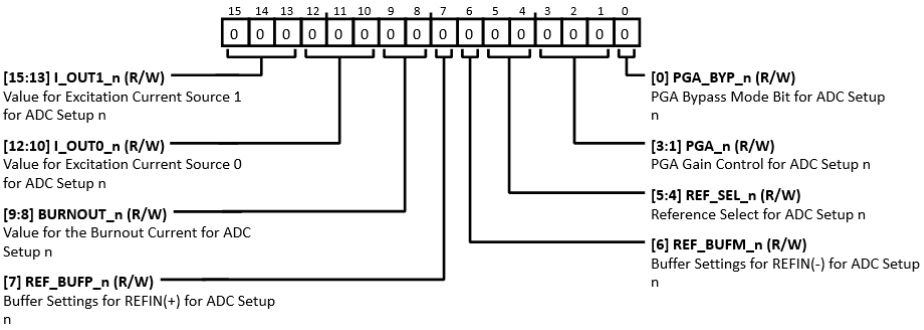


Figure 119.

Table 86. Bit Descriptions for CONFIG_n Registers

Bits	Bit Name	Settings	Description	Reset	Access
[15:13]	I_OUT1_n		Value for Excitation Current Source 1 for ADC Setup n.	0x0	R/W
		000	Off.		
		001	10 µA.		
		010	20 µA.		
		011	50 µA.		
		100	100 µA.		
		101	150 µA.		
		110	200 µA.		
		111	100 nA		
[12:10]	I_OUT0_n		Value for Excitation Current Source 0 for ADC Setup n.	0x0	R/W
		000	Off.		
		001	10 µA.		
		010	20 µA.		
		011	50 µA.		
		100	100 µA.		
		101	150 µA.		
		110	200 µA.		
		111	100 nA		
[9:8]	BURNOUT_n		Value for the Burnout Current for ADC Setup n.	0x0	R/W
		00	Burnout Current Off.		
		01	Burnout Current = 0.5 µA.		
		10	Burnout Current = 2 µA.		
		11	Burnout Current = 4 µA.		
7	REF_BUFP_n		Buffer Settings for REFIN(+) for ADC setup n.	0x0	R/W
		0	Buffer Bypass on REFIN(+).		
		1	Buffer ON for REFIN(+).		
6	REF_BUFM_n		Buffer Settings for REFIN(−) for ADC setup n.	0x0	R/W

AD4130-8 REGISTERS

Table 86. Bit Descriptions for CONFIG_n Registers (Continued)

Bits	Bit Name	Settings	Description	Reset	Access
		0	Buffer Bypass on REFIN(−).		
		1	Buffer ON for REFIN(−).		
[5:4]	REF_SEL_n		Reference Select for ADC setup n.	0x0	R/W
		00	REFIN1(+), REFIN1(−).		
		01	REFIN2(+), REFIN2(−)		
		10	REFOUT, AV_{SS}. Internal reference.		
		11	AV_{DD}, AV_{SS}.		
[3:1]	PGA_n		PGA Gain Control, for ADC setup n. Controls the gain of the PGA. If PGA_BYP_n of the same CONFIG_n register is set, the PGA_n bits are ignored, and the gain is fixed at 1.	0x0	R/W
		000	Gain = 1.		
		001	Gain = 2.		
		010	Gain = 4.		
		011	Gain = 8.		
		100	Gain = 16.		
		101	Gain = 32.		
		110	Gain = 64.		
		111	Gain = 128.		
0	PGA_BYP_n		PGA Bypass Mode Bit. When this bit is set, the PGA is on bypass mode and the settings in the PGA field of the same CONFIG_n register are ignored.	0x0	R/W
		0	PGA Bypass Disabled.		
		1	PGA Bypass Enabled.		

AD4130-8 REGISTERS

Filter n Registers (n = 0 to 7)

Address: 0x21 to 0x28 (in Increments of 1), Reset: 0x002030, Name: FILTER_n (n = 0 to 7)

These registers allow the user to configure up to seven different options for the digital filter to be selected in the CHANNEL_m registers by specifying the SETUP_m bitfields.

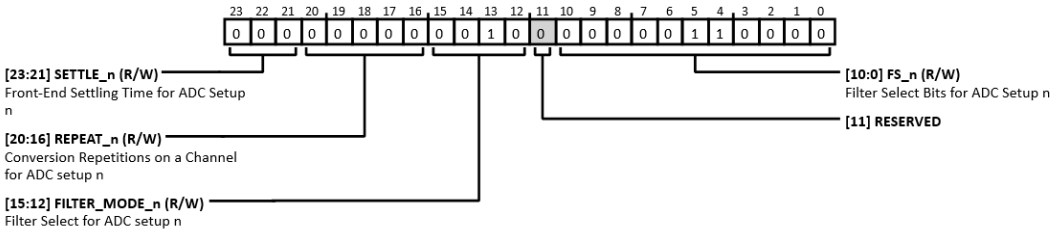


Figure 120.

Table 87. Bit Descriptions for FILTER_n Registers

Bits	Bit Name	Settings	Description	Reset	Access
[23:21]	SETTLE_n		Front-End Settling Time for ADC Setup n. To accommodate varying settling times of inputs, the user can configure the SETTLE_n bits so that the device waits for the appropriate time before the conversion on that channel starts. This is useful if there are excitation currents made available on an AINx input, or the PDSW is enabled for the channel being converted. This front-end settling time applies every time after a channel change. It does not apply for the subsequent repeated conversions determined by the REPEAT_n bits values.	0x0	R/W
		000	32 MCLK cycles (416.6 µs).		
		001	64 MCLK cycles (833.3 µs).		
		010	128 MCLK cycles (1.66 ms).		
		011	256 MCLK cycles (3.33 ms).		
		100	512 MCLK cycles (6.66 ms).		
		101	1024 MCLK cycles (13.33 ms).		
		110	2048 MCLK cycles (26.66 ms).		
		111	4096 MCLK cycles (53.33 ms).		
[20:16]	REPEAT_n		Conversion Repetitions on a Channel for ADC Setup n. Conversions for a given channel are repeated on the number indicated in the REPEAT_n bits. When REPEAT_n is 0, no repetition is done and the channel is converted only once. When REPEAT_n is at N, a channel is converted N+1 times before converting the next channel. These bits are not in use when duty cycling or any calibration mode is enabled.	0x0	R/W
[15:12]	FILTER_MODE_n		Filter Select for ADC Setup n.	0x2	R/W
		0000	$Sinc^4$. $Sinc^4$ standalone filter		
		0001	$Sinc^4$ + $sinc^1$. $Sinc^4$ averaging mode filter.		
		0010	$Sinc^3$. $Sinc^3$ standalone filter		
		0011	$Sinc^3$ + REJ60. This enables the generation of an additional notch at 6/5 of the main notch frequency. If the first main notch is set at 50 Hz (FS = 48), this mode enables simultaneous 50 Hz/60 Hz rejection at a 50 SPS update rate.		
		0100	$Sinc^3$ + $sinc^1$. $Sinc^3$ averaging mode filter.		
		0101	$Sinc^3$ + Post Filter 1. ODR (Hz) = 26.087 SPS.		
		0110	$Sinc^3$ + Post Filter 2. ODR (Hz) = 24 SPS.		
		0111	$Sinc^3$ + Post Filter 3. ODR (Hz) = 19.355 SPS.		
		1000	$Sinc^3$ + Post Filter 4. ODR (Hz) = 16.21 SPS.		

AD4130-8 REGISTERS

Table 87. Bit Descriptions for FILTER_n Registers (Continued)

Bits	Bit Name	Settings	Description	Reset	Access
		1001 to 1111	Reserved.		
11	RESERVED		Reserved.	0x0	R
[10:0]	FS_n		Filter Select Bits for ADC Setup n. These bits control the output data rate (ODR) of the ADC for ADC setup n. FS = 0 is treated as FS = 1.	0x30	R/W

Offset n Registers (n = 0 to 7)

Address: 0x29 to 0x30 (in Increments of 1), Reset: 0x800000, Name: OFFSET_n (n = 0 to 7)

These registers store the result of offset calibration for the corresponding ADC Setup n selected in the CHANNEL_m registers.

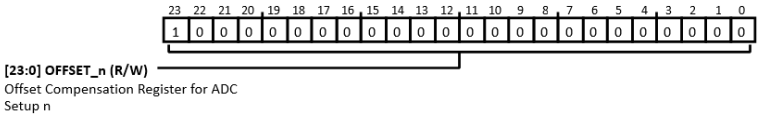


Figure 121.

Table 88. Bit Descriptions for OFFSET_n Registers

Bits	Bit Name	Settings	Description	Reset	Access
[23:0]	OFFSET_n		Offset Compensation Register for ADC Setup n. The results of an internal or system offset calibration gets written into the OFFSET_n register indicated by the SETUP_m bits in the CHANNEL_m register of the active channel. Only one channel can be active during a calibration. The default/reset value of the OFFSET_n registers is 0x800000.	0x800000	R/W

Gain n Registers (n = 0 to 7)

Address: 0x31 to 0x38 (in increments of 1), Reset: 0xXXXXXX, Name: GAIN_n (n = 0 to 7)

These registers store the result of gain calibration for the corresponding ADC Setup n selected in the CHANNEL_m registers.

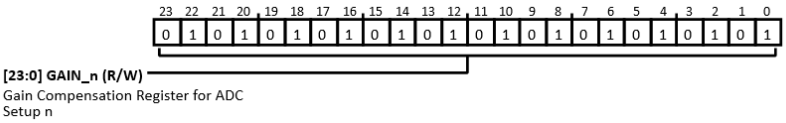


Figure 122.

Table 89. Bit Descriptions for GAIN_n Registers

Bits	Bit Name	Settings	Description	Reset	Access
[23:0]	GAIN_n		Gain Compensation Register for ADC Setup n. The results of an internal or system gain calibration get written into the GAIN_n register indicated by the Setup n bits in the CHANNEL_m register of the active channel. Only one channel can be active during a calibration. The nominal value of the GAIN_n registers is 0x555555. The device is factory calibrated at ambient temperature and with a gain of 1 and PGA_BYP_n = 0, and the resulting gain coefficient is loaded to the GAIN_n registers of the device as default/reset value.	0xXXXXXX	R/W

AD4130-8 REGISTERS

Miscellaneous Register

Address: 0x39, Reset: 0x0000, Name: MISC

Includes settings for oscillator, LDO, calibration and standby mode configuration.

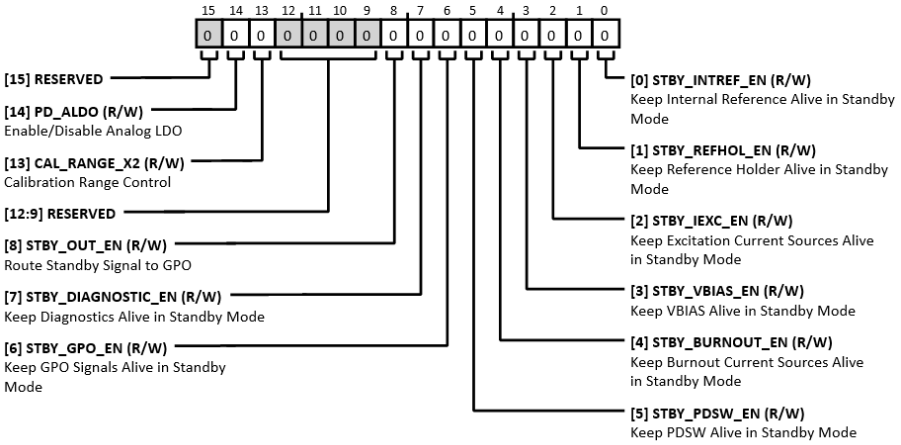


Figure 123.

Table 90. Bit Descriptions for MISC Register

Bits	Bit Name	Settings	Description	Reset	Access
15	RESERVED		Reserved. Always write 0 to this bit.	0x0	R/W
14	PD_ALDO		Enable/Disable Analog LDO.	0x0	R/W
		0	Analog LDO On.		
		1	Analog LDO Off.		
13	CAL_RANGE_X2		Calibration Range Control. This bit can be used for internal gain calibrations when the reference is higher than 2 V. When set to 1, this bit doubles the resistive string output voltage and improves the outcome of internal gain calibration.	0x0	R/W
		0	Disabled.		
		1	Enabled.		
[12:9]	RESERVED		Reserved.	0x0	R
8	STBY_OUT_EN		Route Standby Signal to GPO. When set to 1, values for GPO_CTRL_P4 and GPO_DATA_P4 are ignored, and the active low standby signal gets driven on the P4. When the device is in standby, the P4 pin is low. When the device is converting, the P4 pin is high. When STBY_OUT_EN is set to 1, GPO_CTRL_P4 and GPO_DATA_P4 determine if P4 is enabled and its value, respectively.	0x0	R/W
		0	No Signal to P4 (AIN5).		
		1	Standby Signal to P4 (AIN5).		
7	STBY_DIAGNOSTICS_EN		Keep Diagnostics Alive in Standby Mode. Diagnostics remain active in standby mode if enabled via the ERROR_EN register. Certain errors like the overvoltage/undervoltage detection errors (refer to the ERROR_EN register) require an oscillator to be running to function properly. When in standby mode, however, the internal oscillator can be turned off to save power if there is no enabled feature that makes use of it. Setting this bit compels the device to keep the internal oscillator alive, provided the appropriate errors are also enabled (for example, at least one overvoltage/undervoltage error), and that the user selected to operate with the internal oscillator per the CLK_SEL bits of the ADC_CONTROL register.	0x0	R/W

AD4130-8 REGISTERS

Table 90. Bit Descriptions for MISC Register (Continued)

Bits	Bit Name	Settings	Description	Reset	Access
		0	Diagnostics Disabled in Standby Mode.		
		1	Diagnostics Enabled in Standby Mode.		
6	STBY_GPO_EN		Keep GPO Signals Alive in Standby Mode. GPOs remain active in standby mode if enabled via the IO_CONTROL register	0x0	R/W
		0	GPO Disabled in Standby Mode.		
		1	GPO Enabled in Standby Mode.		
5	STBY_PDSW_EN		Keep PDSW Alive in Standby Mode.	0x0	R/W
		0	Power-Down Switch Disabled in Standby Mode.		
		1	Power-Down Switch Enabled in Standby Mode. The PDSW_m settings in the CHANNEL_m registers determine if the power-down switch closes or opens when the device is in standby for the channels using ADC Setup n.		
4	STBY_BURNOUT_EN		Keep Burnout Current Sources Alive in Standby Mode.	0x0	R/W
		0	Burnout Currents Disabled in Standby Mode.		
		1	Burnout Currents Enabled in Standby mode. The BURNOUT_n settings in the CONFIG_n register determines if the burnout current is enabled when device is in standby for the channels using ADC Setup n.		
3	STBY_VBIAS_EN		Keep VBIAS Alive in Standby Mode.	0x0	R/W
		0	VBIAS Disabled in Standby Mode.		
		1	VBIAS Enabled in Standby Mode. The VBIAS settings in the VBIAS register determine if VBIAS is enabled for the respective AINx pin.		
2	STBY_IEXC_EN		Keep Excitation Current Sources Alive in Standby Mode.	0x0	R/W
		0	Excitation Currents Disabled in Standby Mode.		
		1	Excitation Currents Enabled in Standby Mode. If set to 1, the I_OUT0_n or I_OUT1_n bits in the CONFIG_n register determines if the excitation current is enabled when device is in standby for the channels using Setup n. The excitation current value specified on the corresponding I_OUT0_n or I_OUT1_n field goes to the channels specified on the I_OUT0_CH_m and I_OUT1_CH_m fields of the CHANNEL_m register even in standby.		
1	STBY_REFHOL_EN		Keep Reference Holder Alive in Standby Mode.	0x0	R/W
		0	Reference Holder Disabled in Standby Mode.		
		1	Reference Holder Enabled in Standby Mode.		
0	STBY_INTREF_EN		Keep Reference Alive in Standby Mode.	0x0	R/W
		0	Internal Reference and REFOUT Buffer Disabled in Standby Mode.		
		1	Internal Reference and REFOUT Buffer Enabled in Standby Mode		

AD4130-8 REGISTERS

FIFO Control Register

Address: 0x3A, Reset: 0x040200, Name: FIFO_CONTROL

Control bits for operating the FIFO buffer.

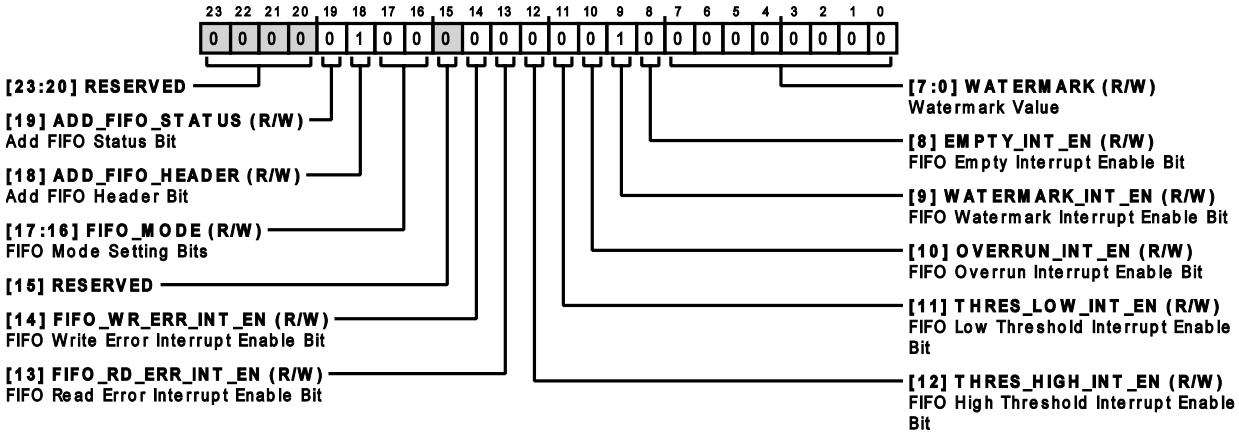


Figure 124.

Table 91. Bit Descriptions for FIFO_CONTROL Register

Bits	Bit Name	Settings	Description	Reset	Access
[23:20]	RESERVED		Reserved.	0x0	R
19	ADD_FIFO_STATUS		Add FIFO Status Bit. When this bit is set to 1, the FIFO_STATUS bits are appended once before the FIFO_DATA stream during a FIFO read command. If the ADD_FIFO_HEADER bit from this register is also set to 1, the FIFO_STATUS bits are added once to the FIFO_HEADER + FIFO_DATA readback stream. Each sample has its own header, but the status is only appended once.	0x0	R/W
		0	No FIFO Status.		
		1	Add FIFO Status.		
18	ADD_FIFO_HEADER		Add FIFO Header Bit. When this bit is set to 1, the FIFO_HEADER bits are appended before the FIFO_DATA bits during a FIFO read command. Each sample has its own header.	0x1	R/W
		0	No FIFO Header.		
		1	Add FIFO Header.		
[17:16]	FIFO_MODE		FIFO Mode Setting Bits. These bits control the mode of operation for the FIFO.	0x0	R/W
		00	Disabled. The FIFO is disabled by default, and the ADC data is read through data register.		
		01	Watermark Mode. This mode stores the first N conversions (N = watermark) in the FIFO. Newer conversions are discarded and only stored until after the FIFO contents up to the watermark are read entirely. Reading the data from the FIFO clears it. In this mode, OVERRUN_FLAG is set to 1 in FIFO_STATUS register if newer data was discarded because the FIFO was not read out in time.		
		10 to 11	Streaming Mode. This mode stores the newest conversions. When the FIFO depth is reached (irrespective of the watermark value), the older data is		

AD4130-8 REGISTERS

Table 91. Bit Descriptions for FIFO_CONTROL Register (Continued)

Bits	Bit Name	Settings	Description	Reset	Access
			automatically discarded to make way for the new one. In this mode, OVERRUN_FLAG is set to 1 in FIFO_STATUS register if older data was discarded because the FIFO was full.		
15	RESERVED		Reserved. Always write 0 to this bit.	0x0	R/W
14	FIFO_WRITE_ERR_INT_EN		FIFO Write Error Interrupt Enable Bit. When this bit is set to 1, FIFO_WRITE_ERR from the FIFO_STATUS register is allowed to trigger an interrupt event in the selected interrupt pin.	0x0	R/W
		0	FIFO Write Error Interrupt Disabled.		
		1	FIFO Write Error Interrupt Enabled.		
13	FIFO_READ_ERR_INT_EN		FIFO Read Error Interrupt Enable Bit. When this bit is set to 1, FIFO_READ_ERR from the FIFO_STATUS register is allowed to trigger an interrupt event in the selected interrupt pin.	0x0	R/W
		0	FIFO Read Error Interrupt Disabled.		
		1	FIFO Read Error Interrupt Enabled.		
12	THRES_HIGH_INT_EN		FIFO High Threshold Interrupt Enable Bit. When this bit is set to 1, THRES_HIGH_FLAG from the FIFO_STATUS register is allowed to trigger an interrupt event in the selected interrupt pin.	0x0	R/W
		0	FIFO High Threshold Interrupt Disabled.		
		1	FIFO High Threshold Interrupt Enabled.		
11	THRES_LOW_INT_EN		FIFO Low Threshold Interrupt Enable Bit. When this bit is set to 1, THRES_LOW_FLAG from the FIFO_STATUS register is allowed to trigger an interrupt event in the selected interrupt pin.	0x0	R/W
		0	FIFO Low Threshold Interrupt Disabled.		
		1	FIFO Low Threshold Interrupt Enabled.		
10	OVERRUN_INT_EN		FIFO Overrun Interrupt Enable Bit. When this bit is set to 1, OVERRUN_FLAG from the FIFO_STATUS register is allowed to trigger an interrupt event in the selected interrupt pin.	0x0	R/W
		0	FIFO Overrun Interrupt Disabled.		
		1	FIFO Overrun Interrupt Enabled.		
9	WATERMARK_INT_EN		FIFO Watermark Interrupt Enable Bit. When this bit is set to 1, WATERMARK_FLAG from the FIFO_STATUS register is allowed to trigger an interrupt event in the selected interrupt pin.	0x1	R/W
		0	FIFO Watermark Interrupt Disabled.		
		1	FIFO Watermark Interrupt Enabled.		
8	EMPTY_INT_EN		FIFO Empty Interrupt Enable Bit. When this bit is set to 1, EMPTY_FLAG bit from the FIFO_STATUS register is allowed to trigger an interrupt event in the selected interrupt pin. This interrupt triggers together with the EMPTY_FLAG bit.	0x0	R/W
		0	FIFO Empty Interrupt Disabled.		
		1	FIFO Empty Interrupt Enabled.		
[7:0]	WATERMARK		Watermark Value. These bits indicate the number of samples before the WATERMARK_FLAG is asserted in the FIFO_STATUS register. 0x00: 256 conversions (entire FIFO length). 0x01: 1 conversion (not recommended). ... 0xFF: 255 conversions.	0x0	R/W

AD4130-8 REGISTERS

FIFO Status Register

Address: 0x3B, Reset: 0x01, Name: FIFO_STATUS

Contains error flags for the FIFO, which are only triggered when the FIFO is either in watermark mode or streaming mode.

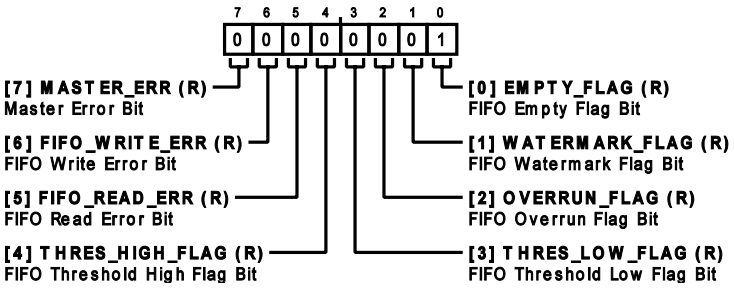


Figure 125.

Table 92. Bit Descriptions for FIFO_STATUS Register

Bits	Bit Name	Settings	Description	Reset	Access
7	MASTER_ERR		Master Error Bit. This bit is set to 1 when any of the errors in the error register are set. The MASTER_ERR bit of the status register is also set to 1 when this MASTER_ERR bit is set to 1.	0x0	R
		0	No Error Detected.		
		1	Master Error Detected.		
6	FIFO_WRITE_ERR		FIFO Write Error Bit. This bit is set to indicate that an ADC conversion was not written successfully in the FIFO. For watermark mode, the bit is set to 1 when an ADC conversion is not written due to an ongoing FIFO read request or an ADC conversion is not written as the watermark is reached, and the FIFO is not emptied out to make room for new conversions. That is, the FIFO is treated full when the watermark is reached and remains so until after the FIFO is emptied (see the FIFO MODE bits from the FIFO_CONTROL register for details). For this case, this bit behaves like the OVERRUN_FLAG error in the FIFO_STATUS register. For streaming mode, the bit is set to 1 when an ADC conversion is not written due to an ongoing FIFO read request. For both FIFO modes, this bit is set to 0 when the FIFO is emptied. The interrupt due to this error sets and clears together with the error flag.	0x0	R
		0	No Error Detected.		
		1	FIFO Write Error Detected.		
5	FIFO_READ_ERR		FIFO Read Error Bit. This bit is set to 1 when a read request on the FIFO fails due to an ADC conversion currently being written on the FIFO. This bit is set to 0 when a FIFO read request is granted or the FIFO is emptied. An interrupt associated with this error sets and clears together with the error bit.	0x0	R
		0	No Error Detected.		
		1	FIFO Read Error Detected.		
4	THRES_HIGH_FLAG		FIFO Threshold High Flag Bit. This flag indicates if a conversion is higher than or equal to the high threshold value set by the THRES_HIGH_VAL bits in the FIFO_THRESHOLD register. When THRES_EN_m of the CHANNEL_m register is set, this bit is set to 1 if the conversion data for CHANNEL_m stored in the FIFO is higher than or equal to the value in THRES_HIGH_VAL bits in the FIFO_THRESHOLD register. This bit is set to 0 when the FIFO is emptied. An interrupt associated with this flag sets and clears together with the bit.	0x0	R
		0	Flag Not Triggered.		
		1	FIFO High Threshold Flag Triggered.		
3	THRES_LOW_FLAG		FIFO Threshold Low Flag Bit. This flag indicates if a conversion is lower than or equal to the low threshold value set by the THRES_LOW_VAL bits in the FIFO_THRESHOLD register. When	0x0	R

AD4130-8 REGISTERS

Table 92. Bit Descriptions for FIFO_STATUS Register (Continued)

Bits	Bit Name	Settings	Description	Reset	Access
			THRES_EN_m of CHANNEL_m register is set, this bit is set to 1 if the conversion data for CHANNEL_m stored in the FIFO is lower than or equal to the value in THRES_LOW_VAL bits in the FIFO_THRESHOLD register. This bit is set to 0 when the FIFO is emptied. An interrupt associated with this flag sets and clears together with the bit.		
		0	Flag Not Triggered.		
		1	FIFO Low Threshold Flag Triggered.		
2	OVERRUN_FLAG		FIFO Overrun Error Bit. This bit sets depending on the FIFO mode. In watermark mode, OVERRUN_FLAG is set to 1 when new conversion data is discarded in the FIFO because the FIFO was not emptied out in time. In streaming mode, OVERRUN_FLAG is set to 1 when the older data in the FIFO is discarded to make way for new data as the FIFO is already full. This bit is set to 0 when the FIFO is emptied. An interrupt associated with this flag sets and clears together with the bit.	0x0	R
		0	Flag Not Triggered.		
		1	Overrun Flag Triggered.		
1	WATERMARK_FLAG		FIFO Watermark Flag Bit. This bit indicates that the FIFO stored the number of samples indicated by the watermark. This bit is set to 1 when the FIFO contains a number of samples greater than or equal to the indicated samples in the watermark field of the FIFO_CONTROL register. This bit is set to 0 when the samples in the FIFO are less than indicated in the watermark field. An interrupt associated with this flag sets and clears together with the bit.	0x0	R
		0	Flag Not Triggered.		
		1	Watermark Flag Triggered.		
0	EMPTY_FLAG		FIFO Empty Flag Bit. This bit is set to 1 when the FIFO becomes empty. The FIFO goes empty on the following conditions: when the FIFO is enabled and not yet initialized with data; as the last entry of the FIFO is being read; on a successful clear command on the FIFO; if the FIFO is disabled, this flag is set to 1 by default. This bit is set to 0 when there is at least one entry in the FIFO. An interrupt associated with this flag sets and clears together with the bit.	0x1	R
		0	Flag Not Triggered.		
		1	Empty Flag Triggered.		

FIFO Threshold Values Register

Address: 0x3C, Reset: 0xFFF000, Name: FIFO_THRESHOLD

Contains upper and lower FIFO threshold values.

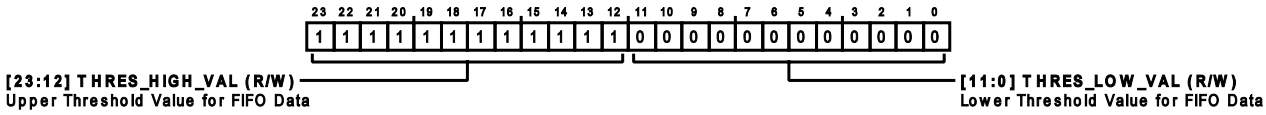


Figure 126.

Table 93. Bit Descriptions for FIFO_THRESHOLD Register

Bits	Bit Name	Settings	Description	Reset	Access
[23:12]	THRES_HIGH_VAL		Upper Threshold Value for FIFO Data. Provided the corresponding THRES_EN_m of CHANNEL_m is set, when a conversion result stored in the FIFO becomes higher than or equal to the value set in THRES_HIGH_VAL, the THRES_HIGH_FLAG bit from the FIFO_STATUS register is set to 1. Threshold values are assumed pseudo static. Thus, it is recommended to flush the FIFO and restart the ADC conversions after changing them to ensure that threshold comparisons are valid.	0xFFF	R/W

AD4130-8 REGISTERS

Table 93. Bit Descriptions for FIFO_THRESHOLD Register (Continued)

Bits	Bit Name	Settings	Description	Reset	Access
[11:0]	THRES_LOW_VAL		Lower Threshold Value for FIFO Data. Provided the corresponding THRES_EN_m of CHANNEL_m is set, when a conversion result stored in the FIFO becomes lower than or equal to the value set in THRES_LOW_VAL, the THRES_LOW_FLAG bit from the FIFO_STATUS register is set to 1. Threshold values are assumed pseudo static. Thus, it is recommended to flush the FIFO and restart the ADC conversions after changing them to ensure that threshold comparisons are valid.	0x0	R/W

FIFO Data Register

Address: 0x3D, Reset: 0x000000, Name: FIFO_DATA

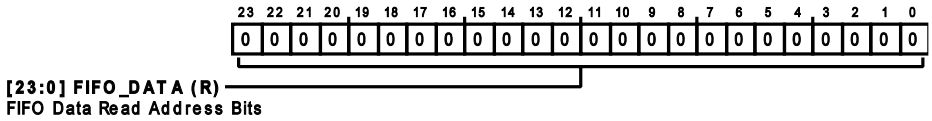


Figure 127.

Table 94. Bit Descriptions for FIFO_DATA Register

Bits	Bit Name	Settings	Description	Reset	Access
[23:0]	FIFO_DATA		FIFO Data Read Address Bits. Perform an SPI read command on this address to read the FIFO contents.	0x0	R

OUTLINE DIMENSIONS

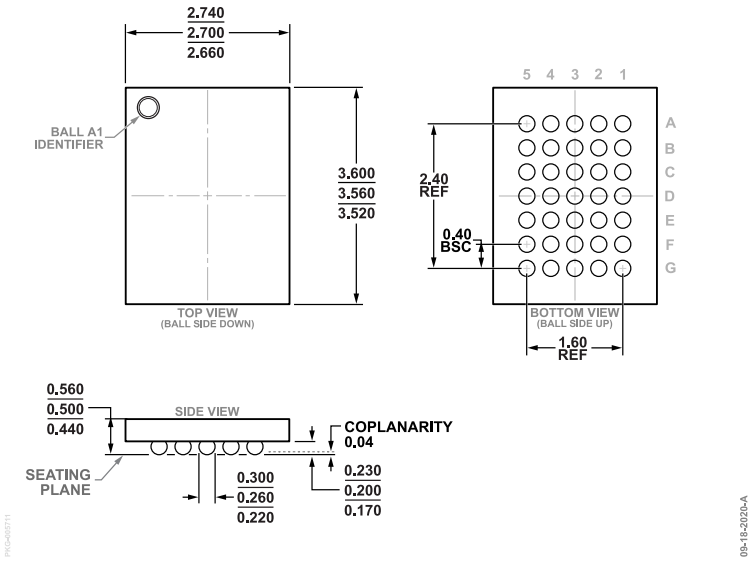


Figure 128. 35-Ball Wafer Level Chip Scale Package [WLCSP]
2.7 mm × 3.56 mm Body and 0.5 mm Package Height
(CB-35-3)
Dimensions shown in millimeters

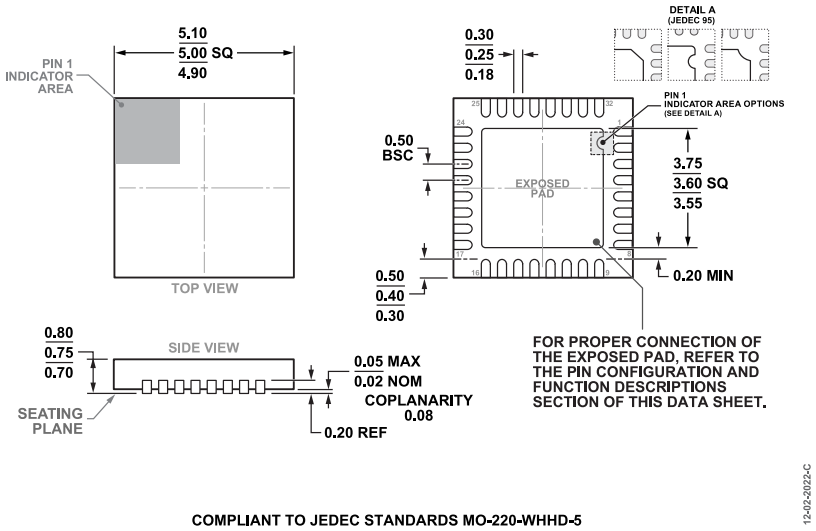


Figure 129. 32-Lead Lead Frame Chip Scale Package [LFCSP]
5 mm × 5 mm Body and 0.75 mm Package Height
(CP-32-12)
Dimensions shown in millimeters

OUTLINE DIMENSIONS

Updated: May 12, 2022

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
AD4130-8BCBZ-RL7	-40°C to +105°C	CHIPS W/SOLDER BUMPS/WLCSP	Reel, 1500	CB-35-3
AD4130-8BCPZ-RL7	-40°C to +125°C	32-Lead Lead Frame Chip Scale Package [LFCSP]	Reel, 1500	CP-32-12

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Model[1]	Description
EVAL-AD4130-8WARDZ	Evaluation Board for WLCSP
EVAL-AD4130-8ARDZ	Evaluation Board for LFCSP
EVAL-SDP-CK1Z	Evaluation Board

[1] Z = RoHS Compliant Part

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