

4A Integrated Switch, High Efficiency Synchronous Buck Regulator with Frequency Programmable up to 4 MHz

Features

- Input Voltage Range: 2.9V to 5.5V
- Output Voltage Adjustable Down to 0.7V
- Output Load Current Up to 4A
- Safe Start-Up into a Pre-Biased Output
- Full Sequencing and Tracking Capability
- Power Good Output
- Efficiency > 95% Across a Broad Load Range
- Programmable Frequency from 300 kHz to 4 MHz
- Ultra-Fast Transient Response
- Easy Ramp Control Compensation
- 100% Maximum Duty Cycle
- Fully Integrated MOSFET Switches
- Thermal Shutdown and Current-Limit Protection
- 20-Lead 3 mm x 4 mm VQFN
- -40°C to +125°C Junction Temperature Range

Applications

- High Power Density Point-of-Load Conversion
- Servers, Routers, and Base Stations
- DVD Recorders/Blu-Ray Players
- Computing Peripherals
- FPGAs, DSP, and Low Voltage ASIC Power

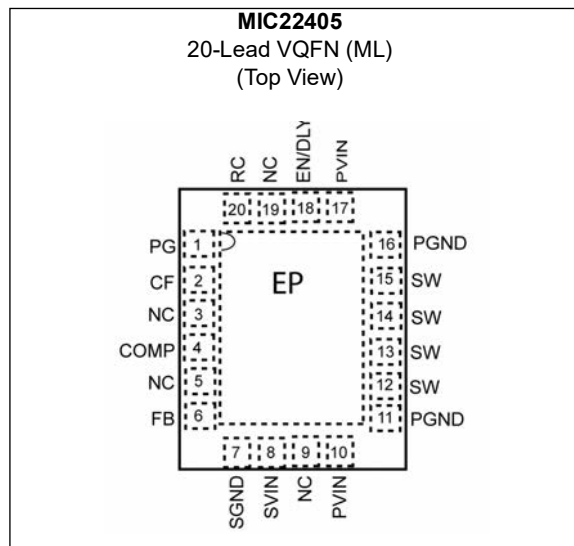
General Description

The MIC22405 is a high efficiency, 4A integrated switch synchronous buck (step-down) regulator. The MIC22405 is optimized for highest efficiency, achieving more than 95% efficiency while still switching at 1 MHz. The ultra-high speed control loop keeps the output voltage within regulation even under the extreme transient load swings commonly found in FPGAs and low-voltage ASICs. The output voltage is pre-bias safe and can be adjusted down to 0.7V to address all low-voltage power needs.

The MIC22405 offers a full range of sequencing and tracking options. The Enable/Delay (EN/DLY) pin, combined with the Power Good (PG) pin, allows multiple outputs to be sequenced in any way during turn-on and turn-off. The Ramp Control (RC) pin allows the device to be connected to another product in the MIC22xxx and/or MIC68xxx family to keep the output voltages within a certain ΔV on start-up.

The MIC22405 is available in a 20-lead 3 mm x 4 mm VQFN with a junction operating range from -40°C to +125°C.

Package Type



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

PV_{IN} to PGND	-0.3V to +6V
SV_{IN} to PGND	-0.3V to PV_{IN}
V_{SW} to PGND	-0.3V to PV_{IN}
$V_{EN/DLY}$ to PGND	-0.3V to PV_{IN}
V_{PG} to PGND	-0.3V to PV_{IN}
PGND to SGND	-0.3V to +0.3V
ESD Rating	(Note 1)

Operating Ratings ‡

Supply Voltage (PV_{IN}/SV_{IN})	+2.9V to +5.5V
Power Good Voltage (V_{PG})	0V to PV_{IN}
Enable Input Voltage ($V_{EN/DLY}$)	0V to PV_{IN}

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

‡ **Notice:** The device is not guaranteed to function outside its operating ratings.

Note 1: Device is ESD sensitive. Handling precautions are recommended.

ELECTRICAL CHARACTERISTICS

$SV_{IN} = PV_{IN} = V_{EN/DLY} = 3.3V$, $V_{OUT} = 1.8V$, $T_A = +25^{\circ}C$, unless noted. **Bold** values valid for $-40^{\circ}C \leq T_J \leq +125^{\circ}C$. (Note 1)

Parameter	Min.	Typ.	Max.	Units	Conditions
Power Supply Input					
Input Voltage Range (PV_{IN})	2.9	—	5.5	V	—
Undervoltage Lockout Trip Level	2.55	2.78	2.9	V	PV_{IN} Rising
UVLO Hysteresis	—	420	—	mV	—
Quiescent Supply Current	—	1.3	2	mV	$V_{FB} = 0.9V$ (not switching)
Shutdown Current	—	5	10	μA	$V_{EN/DLY} = 0V$
Reference					
Feedback Reference Voltage	0.686	0.7	0.714	V	—
Load Regulation	—	0.2	—	%	$I_{OUT} = 100\text{ mA to }4A$
Line Regulation	—	0.2	—	%	$V_{IN} = 2.9V\text{ to }5.5V$; $I_{OUT} = 100\text{ mA}$
FB Bias Current	—	1	—	nA	$V_{FB} = 0.5V$
Enable Control					
EN/DLY Threshold Voltage	1.14	1.24	1.34	V	—
EN Hysteresis	—	10	—	mV	—
EN/DLY Bias Current	0.6	1.0	1.8	μA	$V_{EN/DLY} = 0.5V$; $V_{IN} = 2.9V$ and $V_{IN} = 5.5V$
Ramp Control (RC)					
RC Pin Source Current	0.5	1.0	1.7	μA	$V_{RC} = 0.35V$
Oscillator					
Switching Frequency	0.8	1.0	1.2	MHz	—
Maximum Duty Cycle	100	—	—	%	$V_{FB} \leq 0.5V$
Short Current Protection					
Current Limit	4	7.8	14	A	$V_{FB} = 0.5V$

MIC22405

ELECTRICAL CHARACTERISTICS (CONTINUED)

$SV_{IN} = PV_{IN} = V_{EN/DLY} = 3.3V$, $V_{OUT} = 1.8V$, $T_A = +25^{\circ}C$, unless noted. **Bold** values valid for $-40^{\circ}C \leq T_J \leq +125^{\circ}C$. (Note 1)

Parameter	Min.	Typ.	Max.	Units	Conditions
Internal FETs					
Top MOSFET $R_{DS(ON)}$	—	60	—	mΩ	$V_{FB} = 0.5V$, $I_{SW} = 1A$
Bottom MOSFET $R_{DS(ON)}$	—	35	—	mΩ	$V_{FB} = 0.9V$, $I_{SW} = -1A$
Power Good (PG)					
PG Threshold	-7.5	-10	-12.5	%	Threshold % of V_{FB} from V_{REF}
Hysteresis	—	2.0	—	%	—
PG Output Low Voltage	—	135	—	mV	$I_{PG} = 5\text{ mA}$ (sinking), $V_{EN/DLY} = 0V$
PG Leakage Current	—	—	1.0	μA	$V_{PG} = 5.5V$; $V_{FB} = 0.9V$
	—	—	2.0		
Thermal Protection					
Overtemperature Shutdown	—	150	—	°C	T_J rising
Overtemperature Shutdown Hysteresis	—	10	—	°C	—

Note 1: Specification for packaged product only.

TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Junction Temperature Range	T_J	-40	—	+125	$^{\circ}C$	—
Maximum Junction Temperature	$T_{J(MAX)}$	—	—	+150	$^{\circ}C$	—
Storage Temperature Range	T_S	-65	—	+150	$^{\circ}C$	—
Lead Temperature	T_{LEAD}	—	—	+260	$^{\circ}C$	Soldering, 10 sec.
Package Thermal Resistances						
Thermal Resistance, VQFN 20-Ld	θ_{JC}	—	25	—	$^{\circ}C/W$	—
	θ_{JA}	—	55	—	$^{\circ}C/W$	—

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

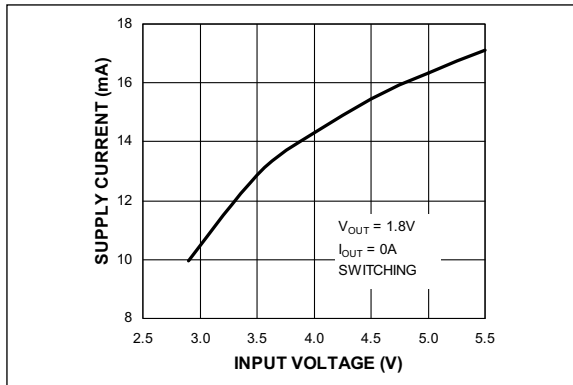


FIGURE 2-1: V_{IN} Operating Supply Current vs. Input Voltage.

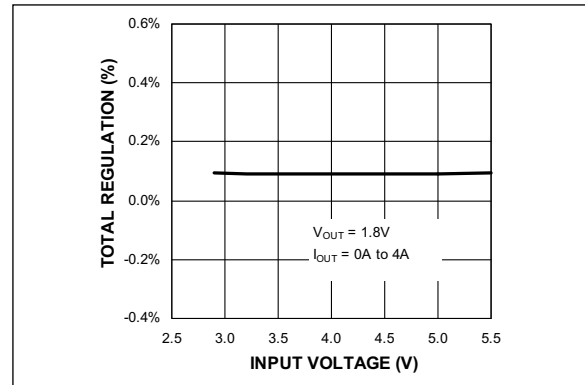


FIGURE 2-4: Load Regulation vs. Input Voltage.

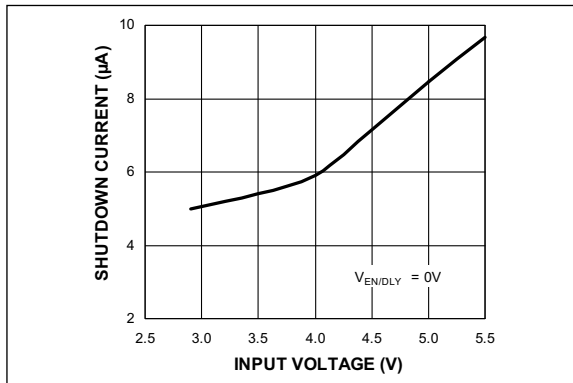


FIGURE 2-2: V_{IN} Shutdown Current vs. Input Voltage.

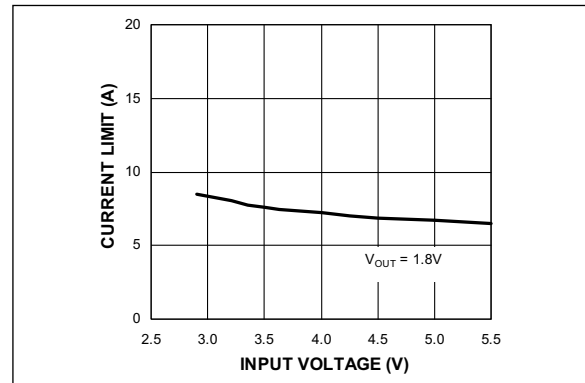


FIGURE 2-5: Current Limit vs. Input Voltage.

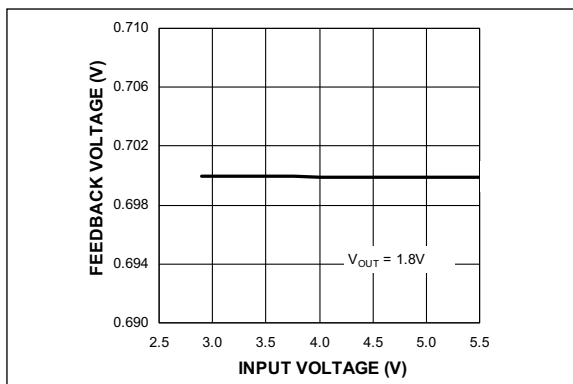


FIGURE 2-3: Feedback Voltage vs. Input Voltage.

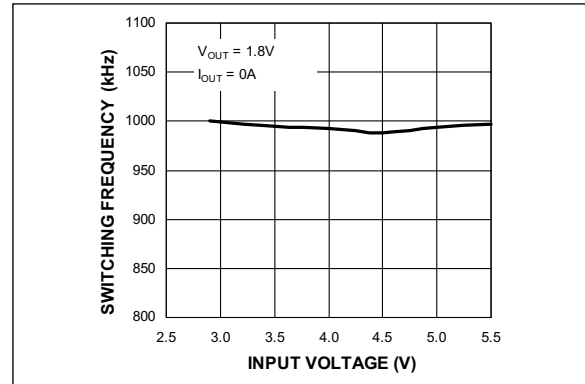


FIGURE 2-6: Switching Frequency vs. Input Voltage.

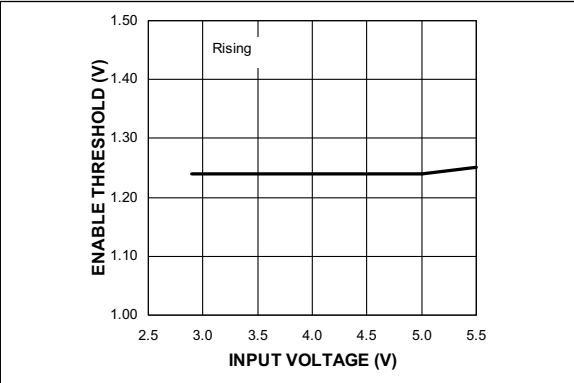


FIGURE 2-7: Enable Threshold vs. Input Voltage.

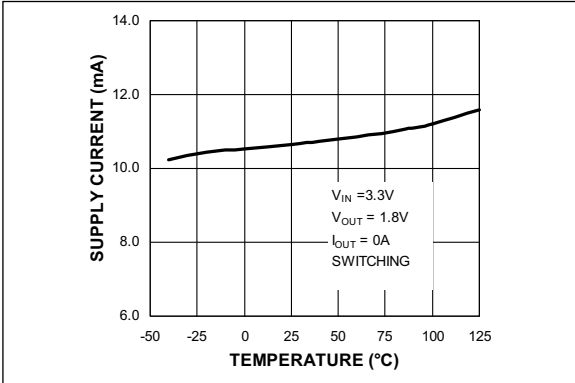


FIGURE 2-10: V_{IN} Operating Supply Current vs. Temperature.

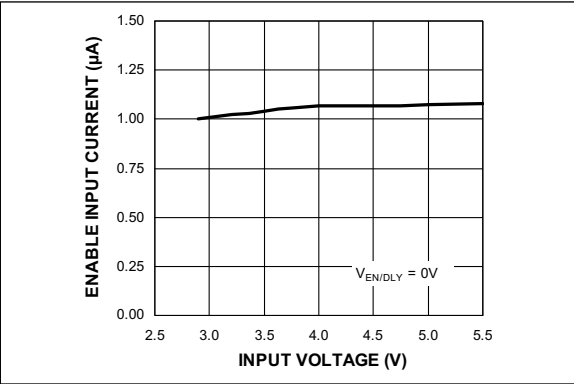


FIGURE 2-8: Enable Input Current vs. Input Voltage.

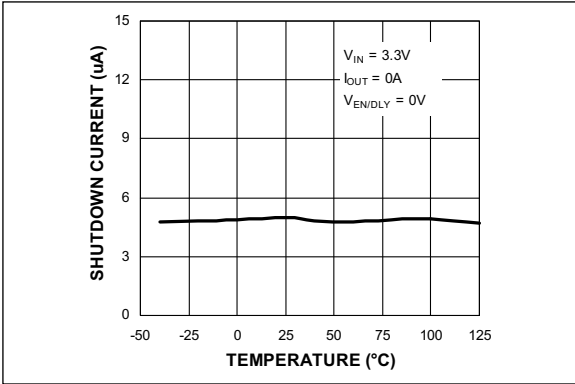


FIGURE 2-11: V_{IN} Shutdown Current vs. Temperature.

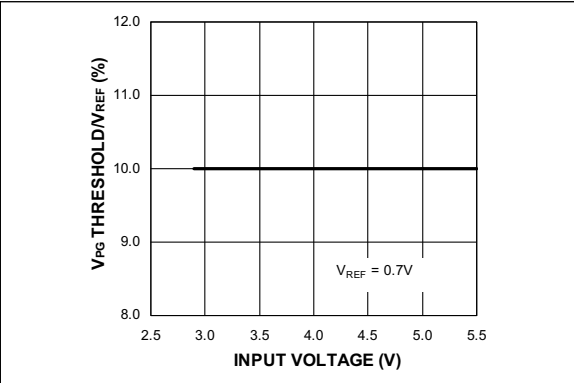


FIGURE 2-9: Power Good Threshold/ V_{REF} Ratio vs. Input Voltage.

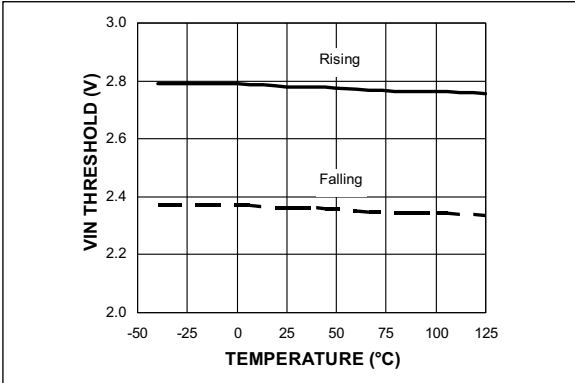


FIGURE 2-12: V_{IN} UVLO Threshold vs. Temperature.

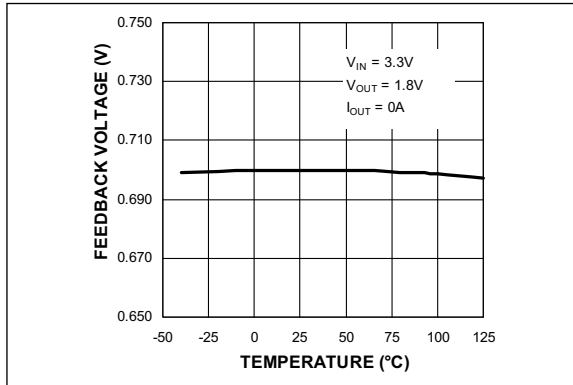


FIGURE 2-13: Feedback Voltage vs. Temperature.

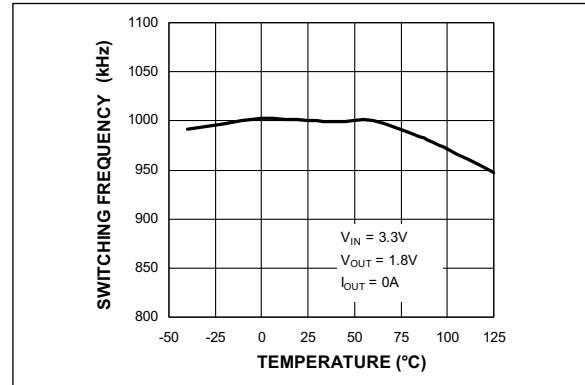


FIGURE 2-16: Switching Frequency vs. Temperature.

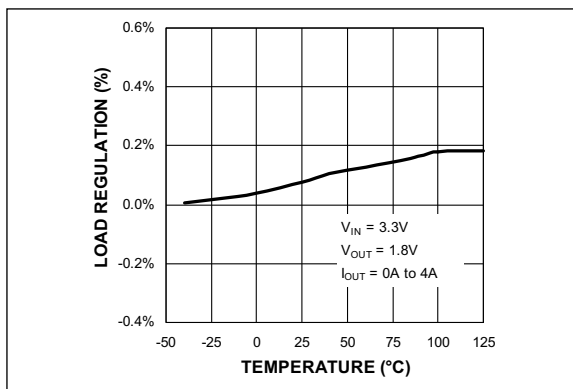


FIGURE 2-14: Load Regulation vs. Temperature.

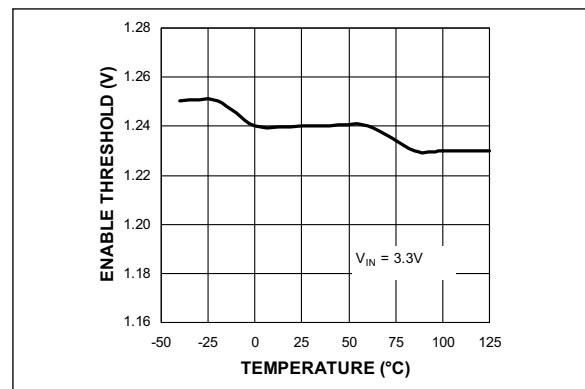


FIGURE 2-17: Enable Threshold vs. Temperature.

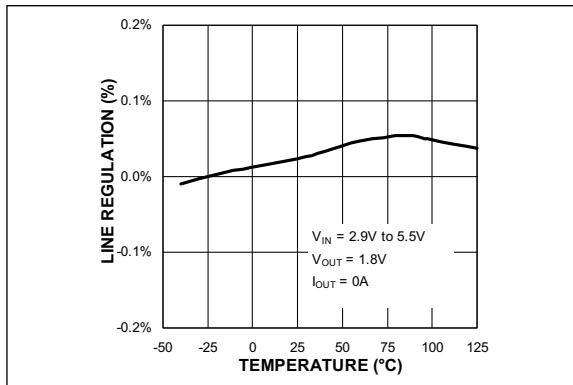


FIGURE 2-15: Line Regulation vs. Temperature.

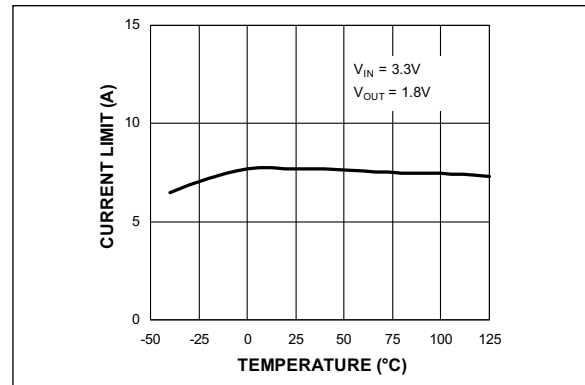


FIGURE 2-18: Current Limit vs. Temperature.

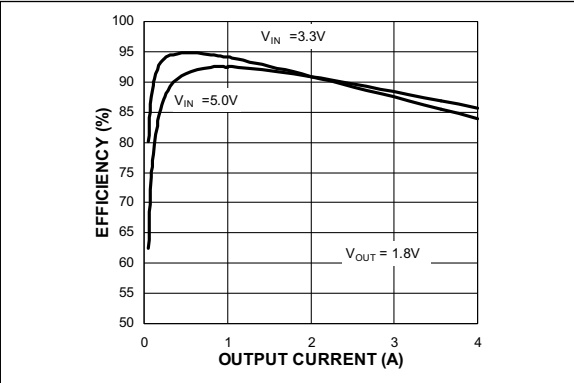


FIGURE 2-19: Efficiency vs. Output Current.

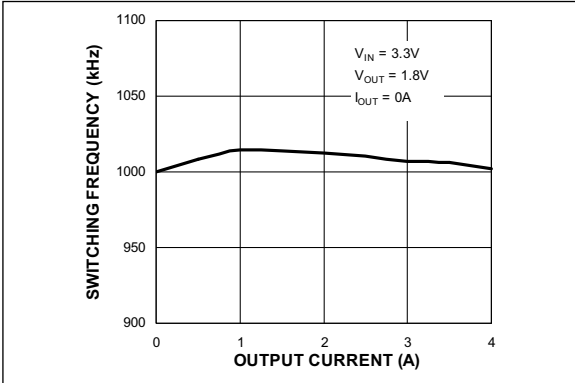


FIGURE 2-22: Switching Frequency vs. Output Current.

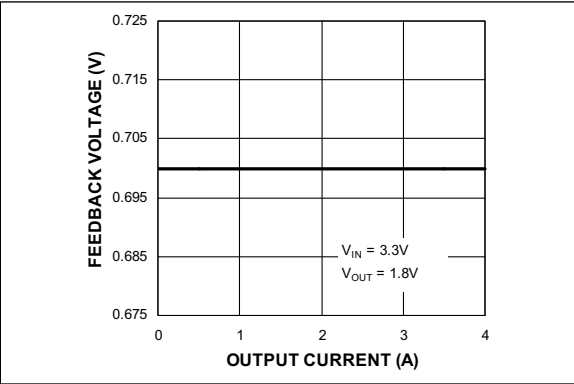


FIGURE 2-20: Feedback Voltage vs. Output Current.

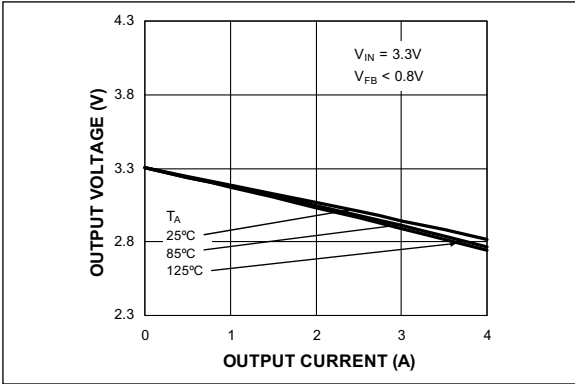


FIGURE 2-23: Output Voltage ($V_{IN} = 3.3V$) vs. Output Current.

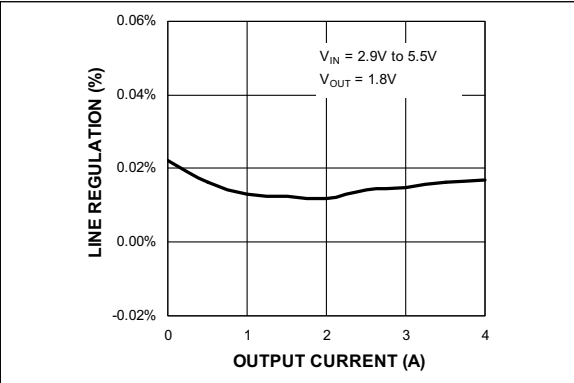


FIGURE 2-21: Line Regulation vs. Output Current.

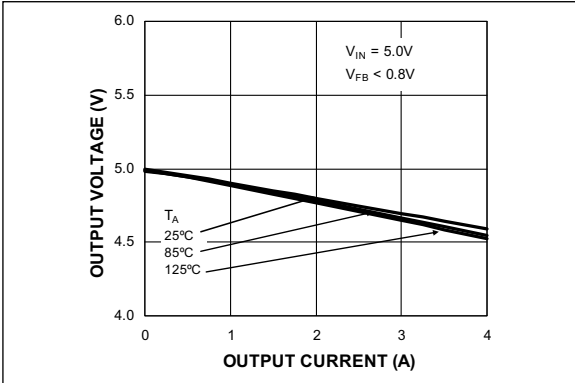


FIGURE 2-24: Output Voltage ($V_{IN} = 5.0V$) vs. Output Current.

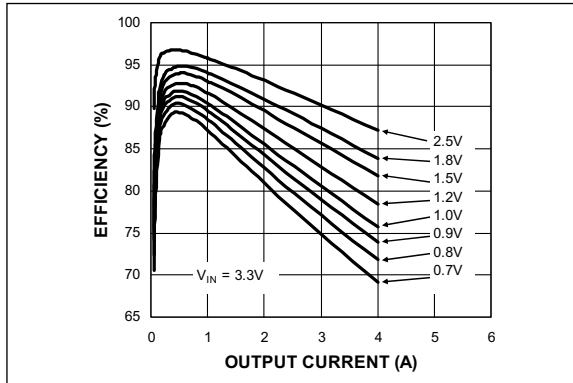


FIGURE 2-25: Efficiency ($V_{IN} = 3.3V$) vs. Output Current.

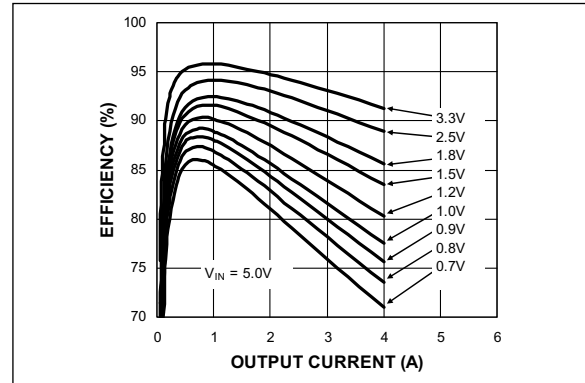


FIGURE 2-28: Efficiency ($V_{IN} = 5.0V$) vs. Output Current.

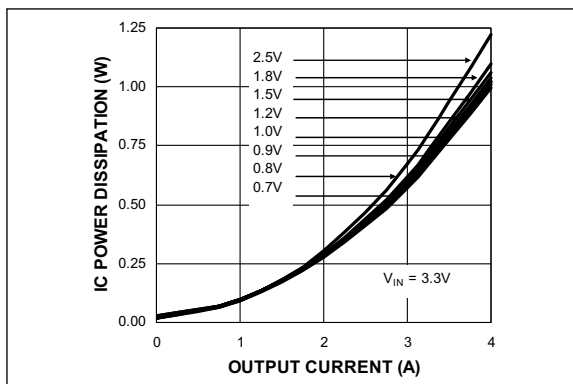


FIGURE 2-26: IC Power Dissipation ($V_{IN} = 3.3V$) vs. Output Current.

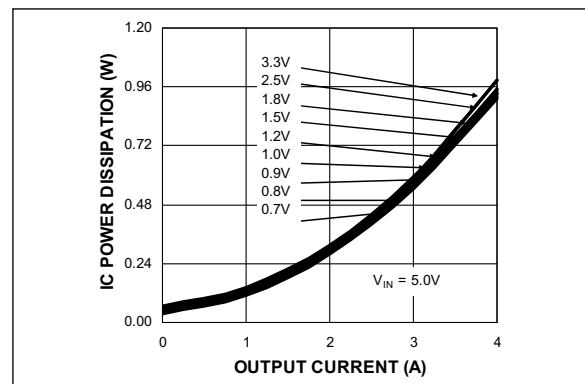


FIGURE 2-29: IC Power Dissipation ($V_{IN} = 5.0V$) vs. Output Current.

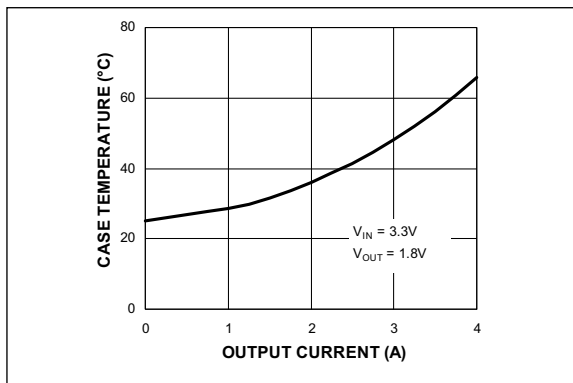


FIGURE 2-27: Case Temperature* ($V_{IN} = 3.3V$) vs. Output Current.

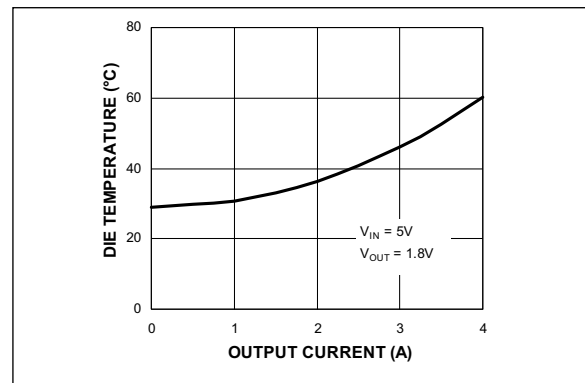


FIGURE 2-30: Case Temperature* ($V_{IN} = 5.0V$) vs. Output Current.

* **Case Temperature:** The temperature measurement was taken at the hottest point on the MIC22405 case and mounted on a five-square inch PCB (see the [Thermal Measurements](#) section). Actual results will depend upon the size of the PCB, ambient temperature, and proximity to other heat-emitting components.

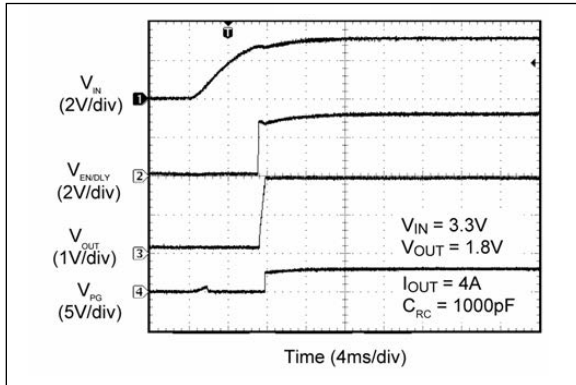


FIGURE 2-31: V_{IN} Turn-On.

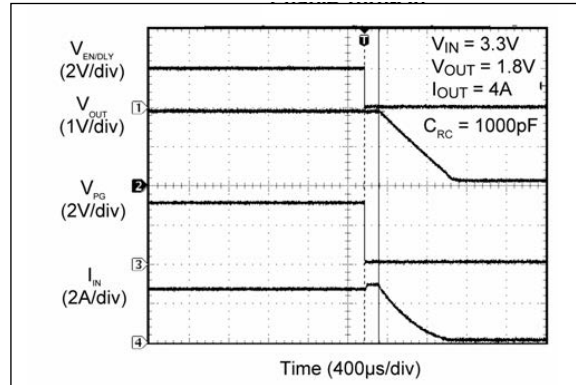


FIGURE 2-34: Enable Turn-Off.

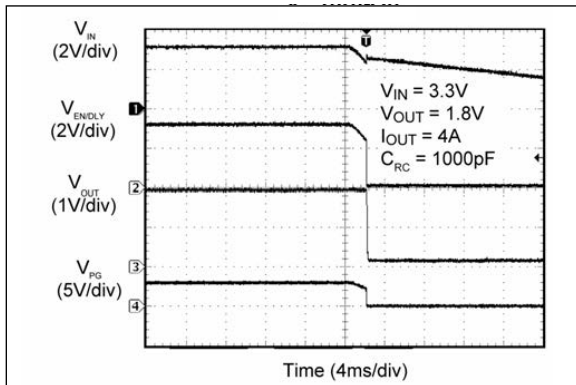


FIGURE 2-32: V_{IN} Turn-Off.

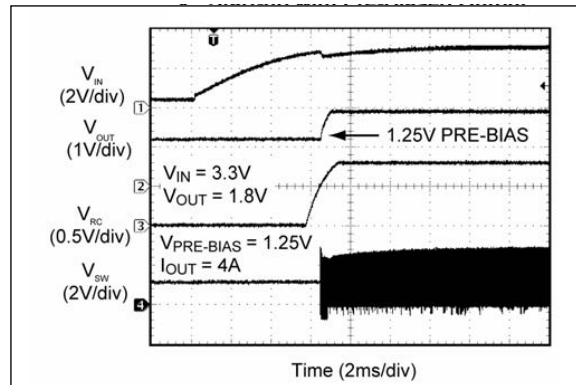


FIGURE 2-35: V_{IN} Start-Up with Pre-Biased Output.

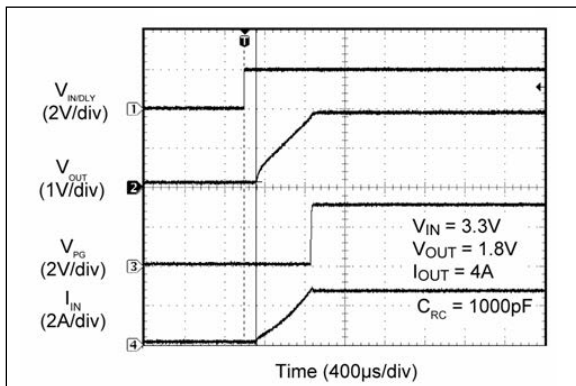


FIGURE 2-33: Enable Turn-On and Rise Time.

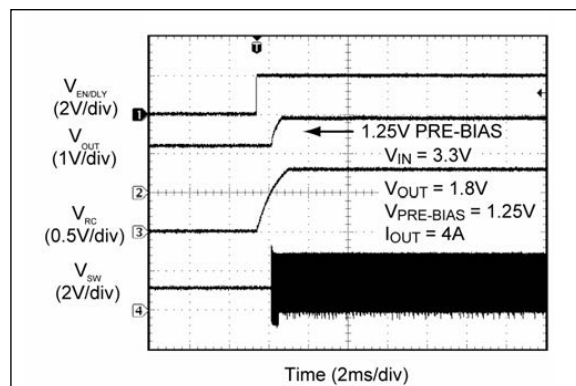


FIGURE 2-36: Enable Start-Up with Pre-Biased Output.

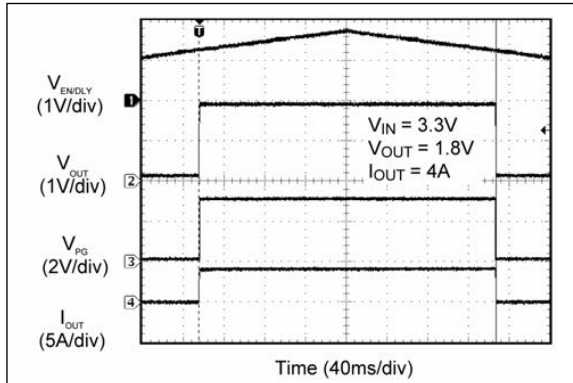


FIGURE 2-37: Enable Thresholds.

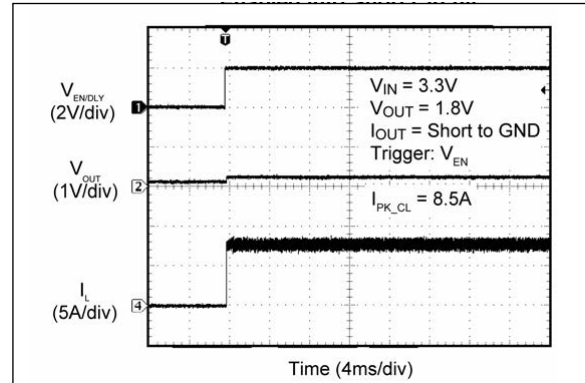


FIGURE 2-40: Enabled into Short-Circuit.

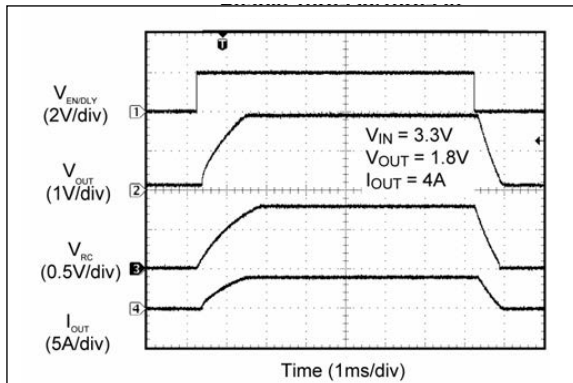


FIGURE 2-38: Enable Turn-On/Turn-Off.

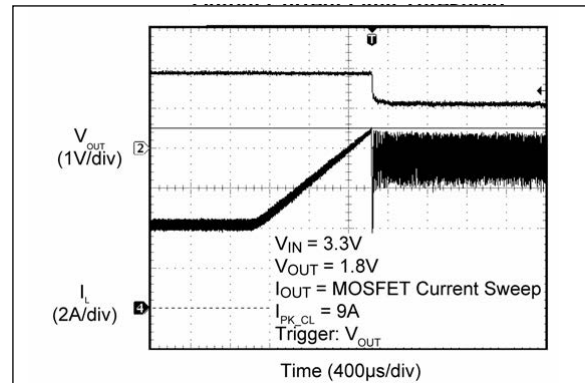


FIGURE 2-41: Output Current Limit Threshold.

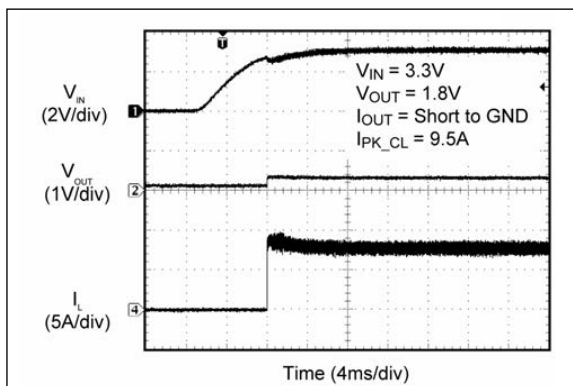


FIGURE 2-39: Power Up into Short-Circuit.

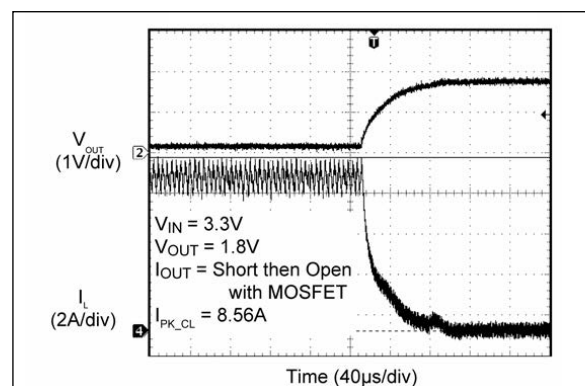


FIGURE 2-42: Output Recovery from Short-Circuit.

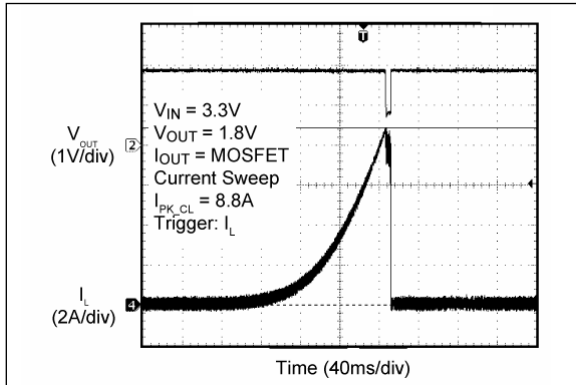


FIGURE 2-43: Peak Current Limit Threshold.

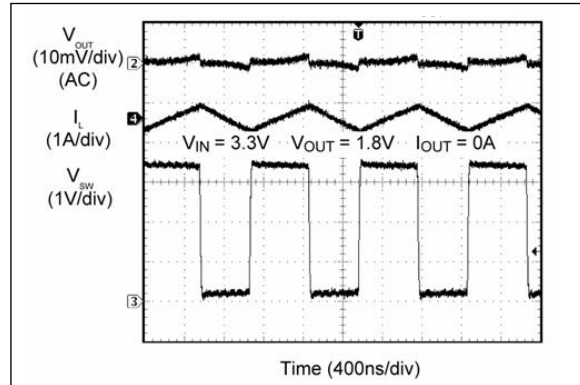


FIGURE 2-46: Switching Waveform;
 $I_{OUT} = 0A$.

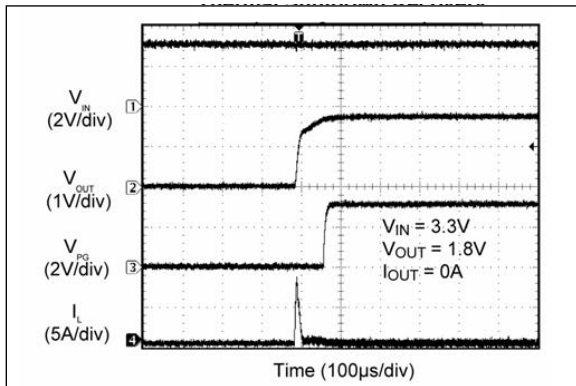


FIGURE 2-44: Thermal Shutdown Recovery.

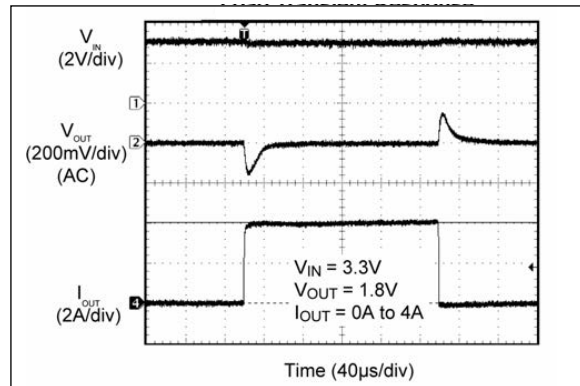


FIGURE 2-47: Load Transient Response.

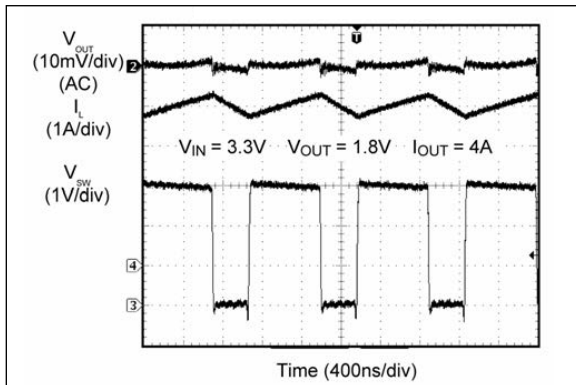


FIGURE 2-45: Switching Waveform;
 $I_{OUT} = 4A$.

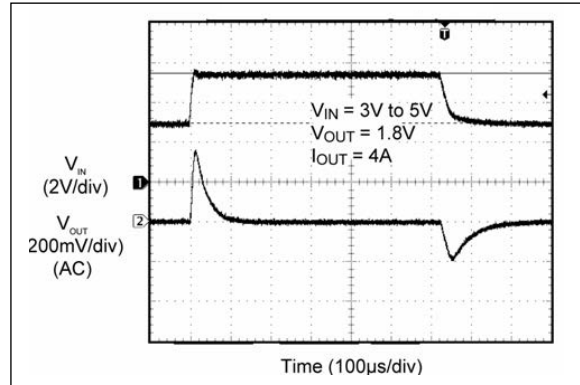


FIGURE 2-48: Line Transient Response.

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in [Table 3-1](#).

TABLE 3-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	PG	Power Good (Output): This is an open-drain output that indicates when the output voltage is below 90% of its nominal voltage. The PG flag is asserted without delay when the enable is set low or when the output goes below the 90% threshold.
2	CF	Adjustable frequency with external capacitor. Refer to Table 5-2 .
3	COMP	Compensation Pin (Input): The MIC22405 uses an internal compensation network containing a fixed-frequency zero (phase lead response) and pole (phase lag response) that allows the external compensation network to be much simplified for stability. The addition of a single capacitor and resistor to the COMP pin will add the necessary pole and zero for voltage mode loop stability using low-value, low-ESR ceramic capacitors.
6	FB	Feedback: Input to the error amplifier. The FB pin is regulated to 0.7V. A resistor divider connecting the feedback to the output is used to adjust the desired output voltage.
7	SGND	Signal Ground: Internal signal ground for all low power circuits.
8	SVIN	Signal Power Supply Voltage (Input): This pin is connected externally to the PVIN pin. A 2.2 μ F ceramic capacitor from the SVIN pin to SGND must be placed next to the IC.
10, 17	PVIN	Power Supply Voltage (Input): The PVIN pins are the input supply to the internal P-Channel Power MOSFET. A 22 μ F ceramic is recommended for bypassing at each PVIN pin. The SVIN pin must be connected to a PVIN pin.
11, 16	PGND	Power Ground: Internal ground connection to the source of the internal N-Channel MOSFETs.
12, 13, 14, 15	SW	Switch (Output): This is the connection to the drain of the internal P-Channel MOSFET and drain of the N-Channel MOSFET. This is a high-frequency, high-power connection; therefore, traces should be kept as short and as wide as practical.
18	EN/DLY	Enable/Delay (Input): This pin is internally fed with a 1 μ A current source from SVIN. A delayed turn on is implemented by adding a capacitor to this pin. The delay is proportional to the capacitor value. The internal circuits are held off until EN/DLY reaches the enable threshold of 1.24V. This pin is pulled low when the input voltage is lower than the UVLO threshold.
19	NC	No Connect: Leave this pin open. Do not connect to ground or route another signal through this.
20	RC	Ramp Control: A capacitor from the RC pin to ground determines the slew rate of output voltage during start-up. The RC pin is internally fed with a 1 μ A current source. The output voltage tracks the RC pin voltage. The slew rate is proportional by the internal 1 μ A source and RC pin capacitor. This feature can be used for tracking capability as well as soft-start.
EP	GND	Exposed Pad (Power): Must be connected to the GND plane for full output power to be realized.

4.0 APPLICATION INFORMATION

The MIC22405 is a 4A synchronous voltage mode PWM step-down regulator IC with a programmable frequency range from 300 kHz to 4 MHz. Other features include tracking and sequencing control for controlling multiple output power systems and power-on-reset (POR).

A regulated DC output voltage is achieved by controlling the ratio of the on-to-off time, or duty cycle. As load or supply voltage changes, so does the duty cycle to maintain a constant output voltage. In cases where the input supply runs into a dropout condition, the MIC22405 will run at 100% duty cycle.

The internal MOSFETs include a high-side P-channel MOSFET from the input supply to the switch pin and an N-channel MOSFET from the switch pin to ground. Because the low-side N-channel MOSFET provides the current during the off cycle, a very low amount of power is dissipated during the off period.

The PWM control technique also provides fixed-frequency operation. Predictable fundamental and harmonic frequencies are achieved by maintaining a constant switching frequency. Other methods of regulation, such as burst and skip modes, have frequency spectrums that change with load that can interfere with sensitive communication equipment.

5.0 COMPONENT SELECTION

5.1 Input Capacitor

A 22 μ F X5R or X7R dielectrics ceramic capacitor is recommended on each of the PVIN pins for bypassing. A Y5V dielectric capacitor should not be used. Aside from losing most of their capacitance over temperature, they also become resistive at high frequencies. This reduces their ability to filter out high-frequency noise.

5.2 Output Capacitor

The MIC22405 was designed specifically for use with ceramic output capacitors. The output capacitor can be increased from 100 μ F to a higher value to improve transient performance. Because the MIC22405 is in voltage mode, the control loop relies on the inductor and output capacitor for compensation. For this reason, do not use excessively large output capacitors. The output capacitor requires either an X7R or X5R dielectric. Y5V and Z5U dielectric capacitors, aside from the undesirable effect of their wide variation in capacitance over temperature, become resistive at high frequencies. Using Y5V or Z5U capacitors can cause instability in the MIC22405.

5.3 Inductor Selection

Inductor selection will be determined by the following (not necessarily in the order of importance):

- Inductance
- Rated current value
- Size requirements
- DC resistance (DCR)

The MIC22405 is designed for use with a 0.47 μ H to 4.7 μ H inductor.

Maximum current ratings of the inductor are generally given in two methods: permissible DC current and saturation current. Permissible DC current can be rated either for a 40°C temperature rise or a 10% loss in inductance. Ensure the inductor selected can handle the maximum operating current. When saturation current is specified, make sure that there is enough margin so that the peak current will not saturate the inductor. The ripple current can add as much as 1.2A to the output current level. The RMS rating should be chosen to be equal or greater than the current limit of the MIC22405 to prevent overheating in a fault condition. For best electrical performance, the inductor should be placed very close to the SW nodes of the IC. For this reason, the heat of the inductor is somewhat coupled to the IC, so it offers some level of protection if the inductor gets too hot (*in such cases, IC case temperature is not a true indication of IC dissipation*). It is important to test all operating limits before settling on the final inductor choice.

The size requirements refer to the area and height requirements that are necessary to fit a particular design. Please refer to the inductor dimensions on their data sheet.

DC resistance is also important. While DCR is inversely proportional to size, DCR increase can represent a significant efficiency loss. Refer to the next section for a more detailed description.

5.4 Efficiency Considerations

Efficiency is defined as the amount of useful output power divided by the amount of power consumed.

EQUATION 5-1:

$$\text{Efficiency [\%]} = \left(\frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN}} \right) \times 100$$

Maintaining high efficiency serves two purposes. First, it decreases power dissipation in the power supply, reducing the need for heat sinks and thermal design considerations and decreasing consumption of current for battery powered applications. Reduced current demand from a battery increases the devices operating time, which is critical in hand held devices.

There are mainly two loss terms in switching converters: static losses and switching losses. Static losses are simply the power losses due to V_I or I^2R . For example, power is dissipated in the high-side switch during the on cycle. Power loss is equal to the high-side MOSFET $R_{DS(ON)}$ multiplied by the RMS switch current squared (I_{SW}^2). During the off-cycle, the low-side N-channel MOSFET conducts, also dissipating power. Similarly, the inductor's DCR and capacitor's ESR also contribute to the I^2R losses. Device operating current also reduces efficiency by the product of the quiescent (operating) current and the supply voltage. The current required to drive the gates on and off at a constant 1 MHz frequency and the switching transitions make up the switching losses.

Figure 5-1 illustrates a typical efficiency curve. From 0A to 0.2A, efficiency losses are dominated by quiescent current losses, gate drive, transition, and core losses. In this case, lower supply voltages yield greater efficiency in that they require less current to drive the MOSFETs and have reduced input power consumption.

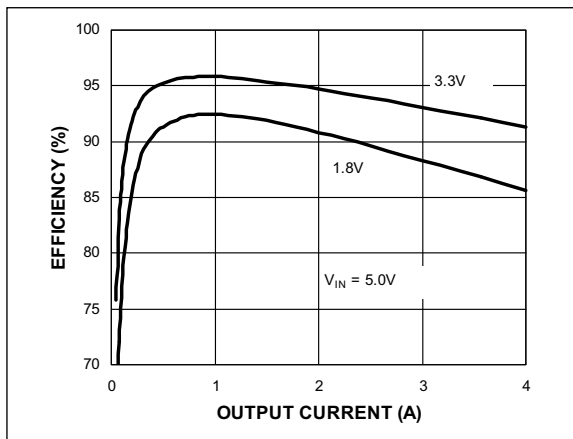


FIGURE 5-1: Efficiency Curve.

From 0.5A to 4A, efficiency loss is dominated by MOSFET $R_{DS(ON)}$ and inductor DC losses. Higher input supply voltages will increase the gate-to-source voltage on the internal MOSFETs, thereby reducing the internal $R_{DS(ON)}$. This improves efficiency by decreasing DC losses in the device. All but the inductor losses are inherent to the device. In which case, inductor selection becomes increasingly critical in efficiency calculations. As the inductors are reduced in size, the DC resistance (DCR) can become quite significant. The DCR losses can be calculated as follows:

EQUATION 5-2:

$$L_{PD} = I_{OUT}^2 \times DCR$$

From that, the loss in efficiency due to inductor resistance can be calculated as follows:

EQUATION 5-3:

$$\text{Efficiency Loss} = \left[1 - \left(\frac{V_{OUT} \times I_{OUT}}{V_{OUT} \times I_{OUT} + L_{PD}} \right) \right] \times 100$$

Efficiency loss due to DCR is minimal at light loads and gains significance as the load is increased. Inductor selection becomes a trade-off between efficiency and size in this case.

Alternatively, under lighter loads, the ripple current due to the inductance becomes a significant factor. When light load efficiencies become more critical, a larger inductor value may be desired. Larger inductances reduce the peak-to-peak inductor ripple current, which minimize losses.

5.5 Compensation

The MIC22405 has a combination of internal and external stability compensation to simplify the circuit for small, high efficiency designs. In such designs, voltage mode conversion is often the optimum solution. Voltage mode is achieved by creating an internal ramp signal and using the output of the error amplifier to modulate the pulse width of the switch node, thereby maintaining output voltage regulation. With a typical gain bandwidth of 100 kHz to 200 kHz, the MIC22405 is capable of extremely fast transient response.

The MIC22405 is designed to be stable with a typical application using a 1 μ H inductor and a 100 μ F ceramic (X5R) output capacitor. These values can be varied dependent upon the trade-off between size, cost and efficiency, keeping the LC natural frequency

EQUATION 5-4:

$$\frac{1}{2 \times \pi \times \sqrt{L \times C}}$$

ideally less than 26 kHz to ensure stability can be achieved. The minimum recommended inductor value is 0.47 μ H and minimum recommended output capacitor value is 22 μ F. The trade-off between changing these values is that with a larger inductor, there is a reduced peak-to-peak current which yields a greater efficiency at lighter loads. A larger output capacitor will improve transient response by providing a larger hold up reservoir of energy to the output.

The integration of one pole-zero pair within the control loop greatly simplifies compensation. The optimum values for C_{COMP} (in series with a 20 k Ω resistor) are shown in Table 5-1.

TABLE 5-1: COMPENSATION CAPACITOR SELECTION

$L \downarrow C \rightarrow$	22 μF to 47 μF	47 μF to 100 μF	100 μF to 470 μF
0.47 μH	0 pF to 10 pF (Note 1)	22 pF	33 pF
1 μH	0 pF to 15 pF (Note 2)	15 pF to 22 pF	33 pF
2.2 μH	15 pF to 33 pF	33 pF to 47 pF	100 pF to 220 pF

Note 1: $V_{\text{OUT}} > 1.2\text{V}$
 2: $V_{\text{OUT}} > 1.0\text{V}$
 3: Compensation values for various output voltages and inductor values are listed in Table 5-3.

5.6 Feedback

The MIC22405 provides a feedback pin to adjust the output voltage to the desired level. This pin connects internally to an error amplifier. The error amplifier then compares the voltage at the feedback to the internal 0.7V reference voltage and adjusts the output voltage to maintain regulation. The resistor divider network for a desired V_{OUT} is given by:

EQUATION 5-5:

$$R2 = \frac{R1}{\left(\frac{V_{\text{OUT}}}{V_{\text{REF}}} - 1\right)}$$

Where:

$V_{\text{REF}} = 0.7\text{V}$

$V_{\text{OUT}} =$ The desired output voltage.

A 10 k Ω or lower resistor value from the output to the feedback (R1) is recommended because large feedback resistor values increase the impedance at the feedback pin, making the feedback node more susceptible to noise pick-up. A small capacitor (50 pF to 100 pF) across the lower resistor can reduce noise pick-up by providing a low impedance path to ground.

5.7 Enable/Delay (EN/DLY) Pin

Enable/Delay (EN/DLY) sources 1 μA out of the IC to allow a start-up delay to be implemented. The delay time is simply the time it takes 1 μA to charge $C_{\text{EN/DLY}}$ to 1.25V. Therefore:

EQUATION 5-6:

$$t_{\text{EN/DLY}} = \frac{1.24 \times C_{\text{EN/DLY}}}{1 \times 10^{-6}}$$

5.8 CF Capacitor

Adding a capacitor to this pin can adjust the switching frequency from 800 kHz to 4 MHz. CF sources 400 μA out of the IC to charge the CF capacitor to set up the switching frequency. The switch period is simply the time it takes 400 μA to charge CF to 1.0V. Table 5-2 shows the frequencies achievable with different CF capacitor values.

TABLE 5-2: CF VS. FREQUENCY

CF Capacitor	Frequency
56 pF	4.4 MHz
68 pF	4 MHz
82 pF	3.4 MHz
100 pF	2.8 MHz
150 pF	2.1 MHz
180 pF	1.7 MHz
220 pF	1.4 MHz
270 pF	1.2 MHz
330 pF	1.1 MHz
390 pF	1.05 MHz
470 pF	1 MHz

It is necessary to connect the CF capacitor between the CF pin and signal ground.

5.9 300 kHz to 800 kHz Operation

The frequency range can be lowered by adding an additional resistor (R_{CF}) in parallel with the CF capacitor. This reduces the amount of current used to charge the capacitor, thus reducing the frequency. The following equation can be used for frequencies between 300 kHz and 800 kHz.

EQUATION 5-7:

$$-R_{\text{CF}} \times C_{\text{CF}} \times \ln\left(1 + \frac{1.0\text{V}}{400\mu\text{A} \times R_{\text{CF}}}\right) = t$$

$$R_{\text{CF}} > 2.9\text{k}\Omega$$

5.10 RC Pin (Soft-Start)

The RC pin provides a trimmed 1 μA current source/sink for accurate ramp-up (soft-start). This allows the MIC22405 to be used in systems that require voltage tracking or ratio-metric voltage tracking at start-up.

There are two ways of using the RC pin:

- Externally driven from a voltage source
- Externally attached capacitor sets output ramp-up/down rate

In the first case, driving RC with a voltage from 0V to V_{REF} will program the output voltage between 0% and 100% of the nominal set voltage as shown in Figure 5-2.

In the second case, the external capacitor sets the ramp-up and ramp-down time of the output voltage. The time is calculated by:

EQUATION 5-8:

$$t_{RAMP} = \frac{0.7 \times C_{RC}}{1 \times 10^{-6}}$$

Where:

t_{RAMP} = The time from 0% to 100% of the nominal output voltage.

During start-up, a light load condition ($I_{OUT} < 1.25A$) can lead to negative inductor current. Under these conditions, the maximum ramp-up time should not exceed the critical ramp-up time period to keep the regulator in continuous mode operation when V_{FB} reaches 90% of reference voltage.

Beyond the critical ramp-up time, the regulator is in discontinuous mode, which leads to prolonged N-channel MOSFET conduction, which, in turn, causes negative inductor current.

The maximum C_{RC} value is calculated as follows.

EQUATION 5-9:

$$C_{RC} < \frac{2.86 \times C_{OUT} \times L \times f_{SW} \times 10^{-6}}{1 - \frac{V_{OUT}}{V_{IN}}}$$

5.11 Pre-Bias Start-Up

The MIC22405 is designed for safe start-up into a pre-biased output. This prevents large negative inductor currents and excessive output voltage oscillations. The MIC22405 starts with the low-side MOSFET turned off, preventing reverse inductor current flow. The synchronous MOSFET stays off until Power Good (PG) goes high after the V_{FB} is above 90% of V_{REF} .

A pre-bias condition can occur if the input is turned off then immediately turned back on before the output capacitor is discharged to ground. It is also possible that the output of the MIC22405 could be pulled up or pre-biased through parasitic conduction paths from one supply rail to another in multiple voltage (V_{OUT}) level ICs such as a FPGA.

Figure 5-2 shows a normal start-up waveform. A 1 μA current source charges the soft-start capacitor C_{RC} . The C_{RC} capacitor forces the V_{RC} voltage to come up

slowly (V_{RC} trace), thereby providing a soft-start ramp. This ramp is used to control the internal reference (V_{REF}). The error amplifier forces the output voltage to follow the V_{REF} ramp from zero to the final value.

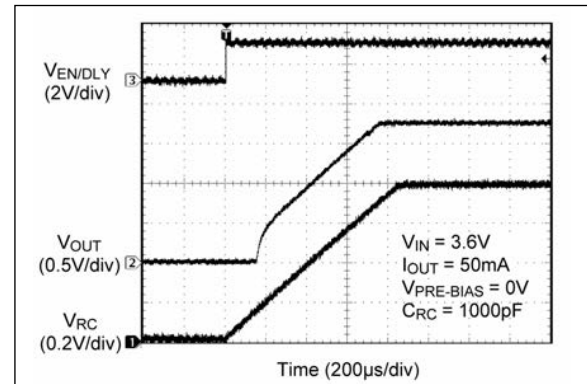


FIGURE 5-2: EN Turn-On Time: Normal Start-Up.

If the output is pre-biased to a voltage above the expected value, as shown in Figure 5-3, then neither MOSFET will turn on until the ramp control voltage (V_{RC}) is above the reference voltage (V_{REF}). Then, the high-side MOSFET starts switching, forcing the output to follow the V_{RC} ramp. Once the feedback voltage is above 90% of the reference voltage, the low-side MOSFET will begin switching.

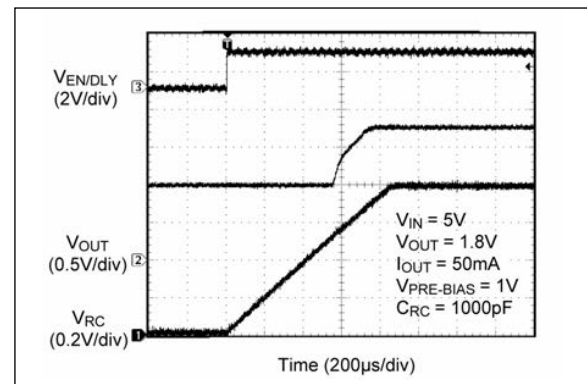


FIGURE 5-3: EN Turn-On at 1V Pre-Bias.

When the MIC22405 is turned off, the low-side MOSFET will be disabled and the output voltage will decay to zero. During this time, the ramp control voltage (V_{RC}) will still control the output voltage fall-time with the high-side MOSFET if the output voltage falls faster than the V_{RC} voltage. Figure 5-4 shows this operating condition. Here, a 4A load pulls the output down fast enough to force the high-side MOSFET on (V_{SW} trace).

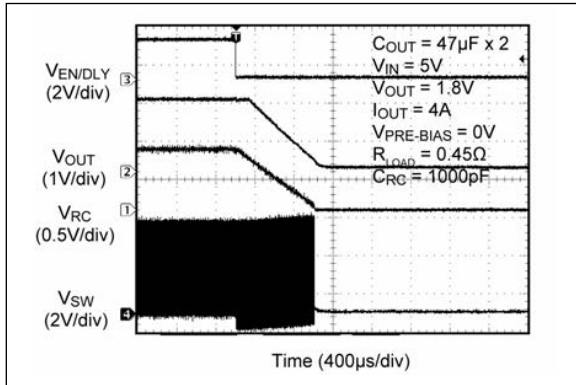


FIGURE 5-4: EN Turn-Off: 4A Load.

If the output voltage falls slower than the V_{RC} voltage, then the both MOSFETs will be off and the output will decay to zero as shown in the V_{OUT} trace in Figure 5-5. With both MOSFETs off, any resistive load connected to the output will help pull down the output voltage. This will occur at a rate determined by the resistance of the load and the output capacitance.

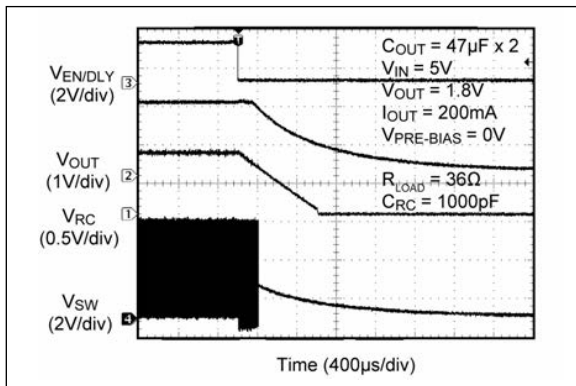


FIGURE 5-5: EN Turn-Off: 200 mA Load.

5.11.1 CURRENT LIMIT

The MIC22405 uses a two-stage technique to protect against overload. The first stage is to limit the current in the P-channel switch; the second is overtemperature shutdown.

Current is limited by measuring the current through the high-side MOSFET during its power stroke and immediately switching off the driver when the preset limit is exceeded.

The circuit in Figure 5-6 describes the operation of the current limit circuit. Because the actual $R_{DS(ON)}$ of the P-channel MOSFET varies from part to part, and with changes in temperature and with input voltage, simple IR voltage detection is not employed. Instead, a smaller copy of the Power MOSFET (Reference FET) is fed with a constant current that is directly proportional to the factory set current limit. This sets the current limit as a current ratio and, thus, is not dependent upon the $R_{DS(ON)}$ value. Current limit is set to nominal value.

Variations in the scale factor K between the power PFET and the reference PFET used to generate the limit threshold account for a relatively small inaccuracy.

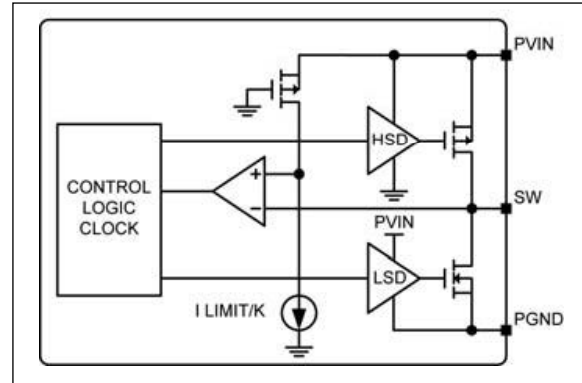


FIGURE 5-6: Current Limit Detail.

5.11.2 THERMAL CONSIDERATIONS

The MIC22405 is packaged in a 3 mm x 4 mm VQFN; a package that has excellent thermal performance equal to that of the larger TSSOP packages. This maximizes heat transfer from the junction to the exposed pad (ePAD) that connects to the ground plane. The size of the ground plane attached to the exposed pad determines the overall thermal resistance from the junction to the ambient air surrounding the printed circuit board. The junction temperature for a given ambient temperature can be calculated using:

EQUATION 5-10:

$$T_J = T_A + P_D \times R_{\theta JA}$$

Where:

P_D = The power dissipated within the VQFN package and is at 4A load.

$R_{\theta JA}$ = $R_{\theta JA}$ is a combination of junction-to-case thermal resistance ($R_{\theta JC}$) and case-to-ambient thermal resistance ($R_{\theta CA}$), because thermal resistance of the solder connection from the ePAD to the PCB is negligible; $R_{\theta CA}$ is the thermal resistance of the ground plane-to-ambient, so $R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$.

T_A = The operating ambient temperature.

Example:

The evaluation board has two copper planes contributing to an $R_{\theta JA}$ of approximately 55°C/W. The worst case $R_{\theta JC}$ of the 3 mm x 4 mm VQFN is 25°C/W.

EQUATION 5-11:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

$$R_{\theta JA} = 25 + 30 = 55^\circ\text{C/W}$$

To calculate the junction temperature for a 50°C ambient:

EQUATION 5-12:

$$T_J = T_A + P_D \times R\theta_{JA}$$

$$T_J = 50 + (0.89 \times 55) = 98.95^\circ\text{C}$$

This is below the maximum of 125°C.

5.12 Thermal Measurements

Measuring the IC's case temperature is recommended to ensure it is within its operating limits. Although this might seem like a very elementary task, it is easy to get erroneous results. The most common mistake is to use the standard thermal couple that comes with a thermal meter. This thermal couple wire gauge is large, typically 22 gauge, and behaves like a heat-sink, resulting in a lower case measurement.

Two better methods of temperature measurement are using a smaller thermal couple wire or an infrared thermometer. If a thermal couple wire is used, it must be constructed of 36 gauge wire or higher then (smaller wire size) to minimize the wire's heat-sinking effect. In addition, the thermal couple tip must be covered in either thermal grease or thermal glue to make sure that the thermal couple junction is making good contact with the case of the IC. Omega brand thermal couple (5SC-TT-K-36-36) is adequate for most applications.

Whenever possible, an infrared thermometer is recommended. The measurement spot size of most infrared thermometers is too large for an accurate reading on a small form factor ICs. However, an IR thermometer from Optris has a 1 mm spot size, which makes it a good choice for measuring the hottest point on the case. An optional stand makes it easy to hold the beam on the IC for long periods of time.

5.13 Sequencing and Tracking

There are four variations of sequencing and tracking that are easily implemented using the MIC22405. The two sequencing variations are Delayed and Windowed. The two tracking variants are Normal and Ratio Metric. The following diagrams illustrate methods for connecting two MIC22405's to achieve these requirements.

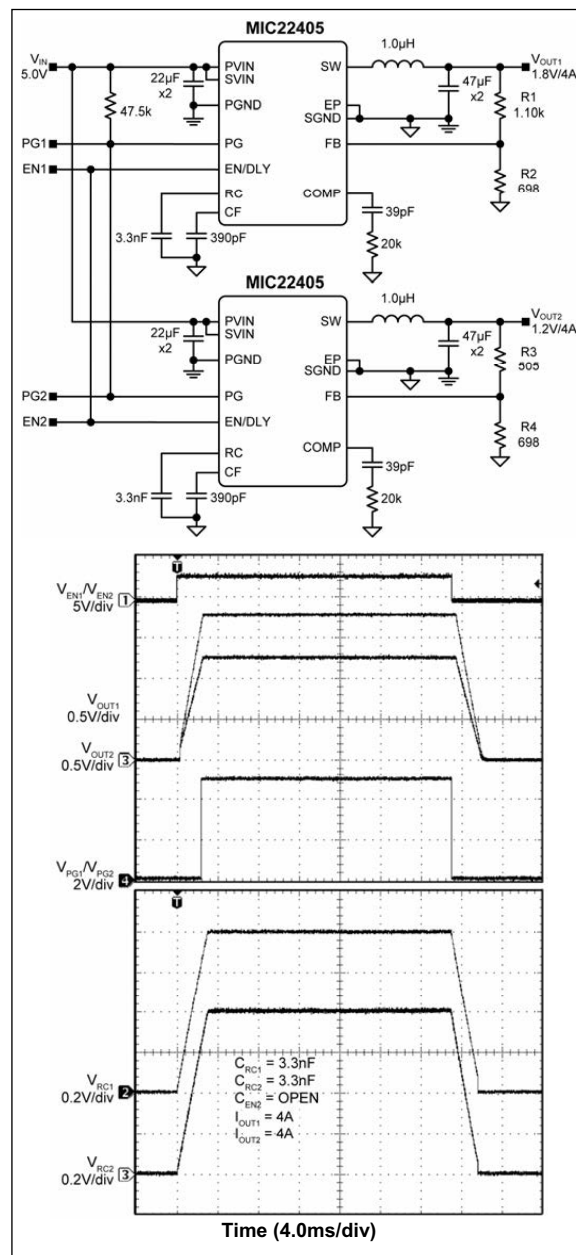


FIGURE 5-7: Windowed Sequencing.

MIC22405

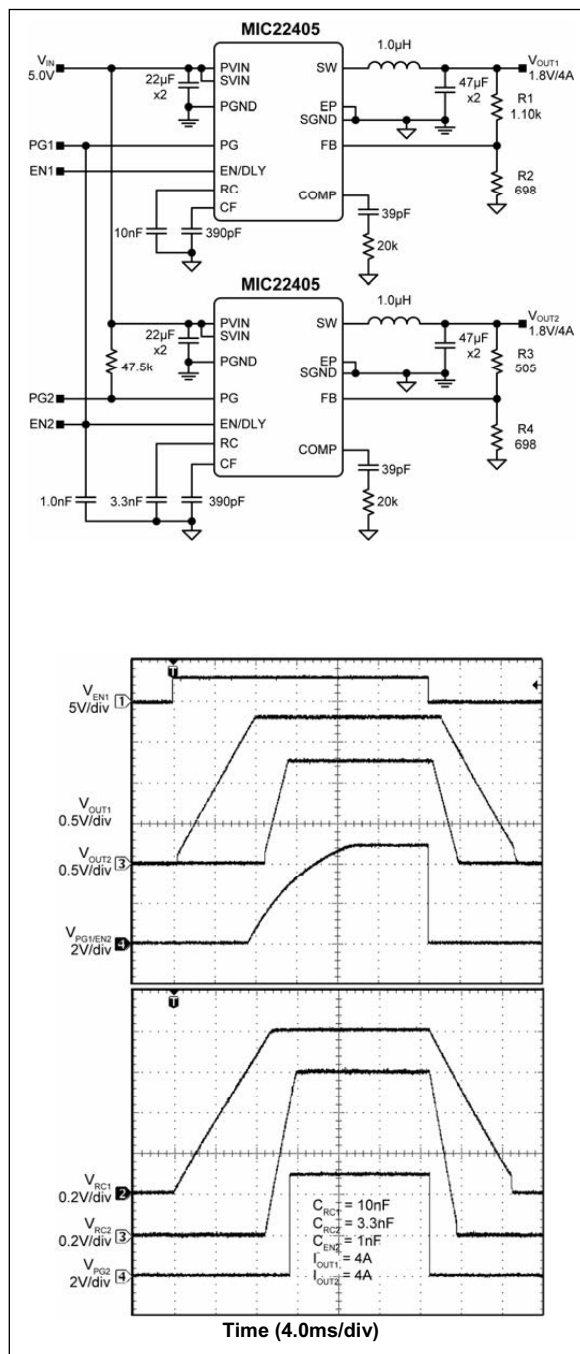


FIGURE 5-8: Delayed Sequencing.

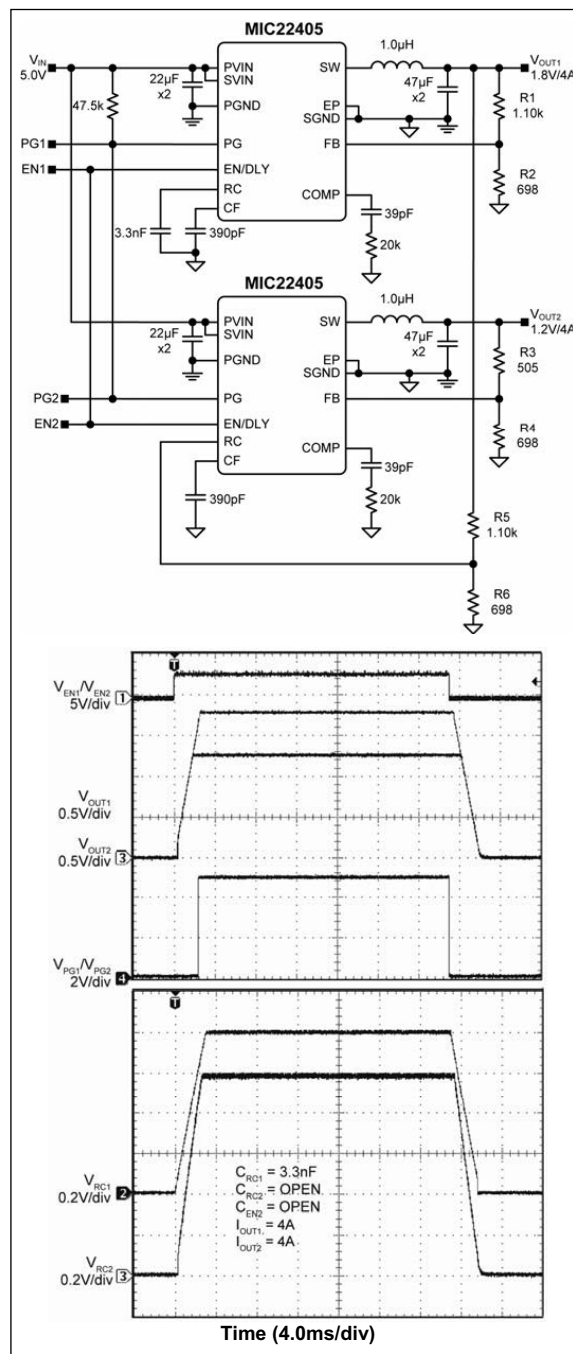


FIGURE 5-9: Normal Tracking.

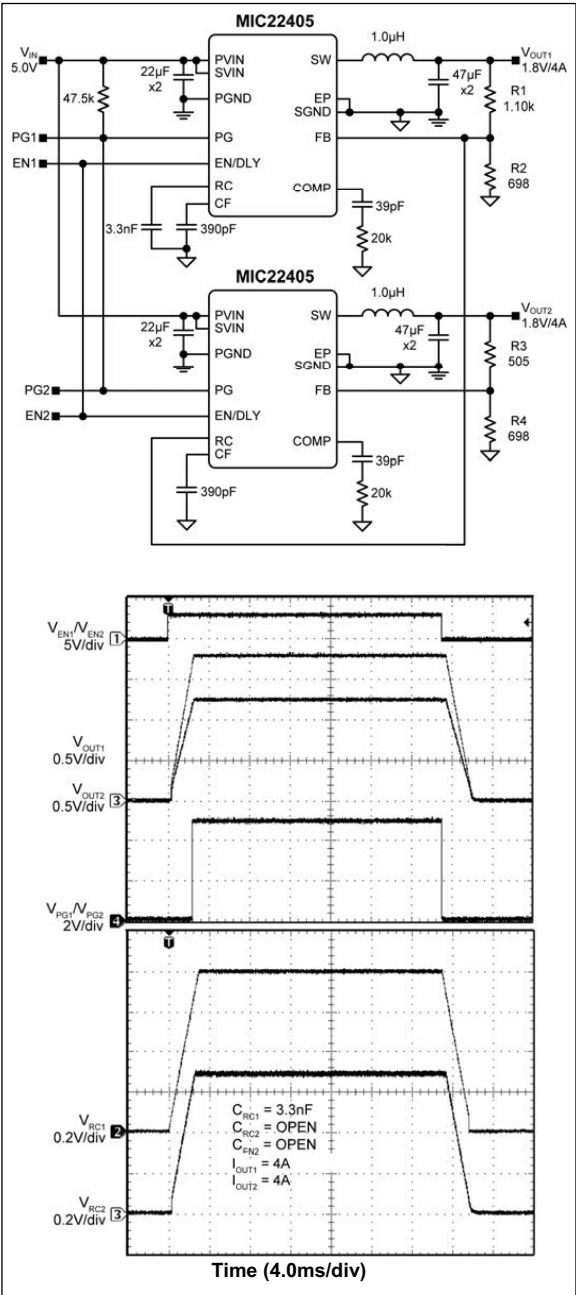


FIGURE 5-10: Ratio Metric Tracking.

TABLE 5-3: COMPENSATION SELECTION

$V_{IN} = 5V$								
V_{OUT}	L	C_{OUT}	C_{COMP}	R_{COMP}	C_{FF}	R_{FF}	C_{FB}	R_{FB}
4.2V	1.5 μH	2 x 47 μF	100 pF	20 k Ω	1 nF	4.7 k Ω	100 pF	953 Ω

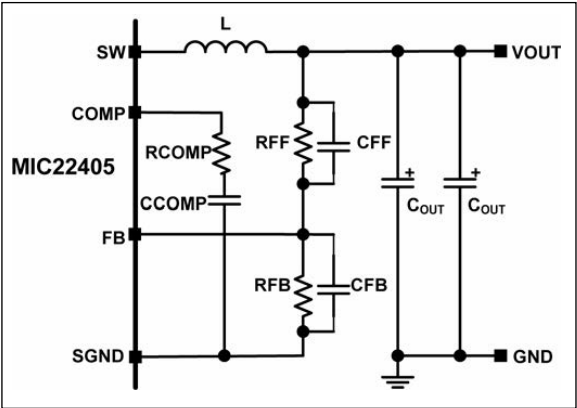


FIGURE 5-11: Schematic Reference.

6.0 PCB LAYOUT GUIDELINES

PCB layout is critical to achieve reliable, stable, and efficient performance. A ground plane is required to control EMI and minimize the inductance in power, signal and return paths.

To minimize EMI and output noise, the following guidelines should be followed to ensure proper operation of the MIC22405.

6.1 IC

- The 2.2 μ F ceramic capacitor, which is connected to the SVIN pin, must be located right at the IC. The SVIN pin is very noise sensitive and placement of the capacitor is very critical. Use wide traces to connect to the SVIN and SGND pins.
- The signal ground pin (SGND) must be connected directly to the ground planes. Do not route the SGND pin to the PGND Pad on the top layer.
- Place the IC close to the point-of-load (POL).
- Use wide traces to route the input and output power lines.
- Signal and power grounds should be kept separate and connected at only one location.

6.2 Input Capacitor

- A 22 μ F X5R or X7R dielectrics ceramic capacitor is recommended on each of the PVIN pins for bypassing.
- Place the input capacitors on the same side of the board and as close to the IC as possible.
- Keep both the PVIN pin and PGND connections short.
- Place several vias to the ground plane close to the input capacitor ground terminal.
- Use either X7R or X5R dielectric input capacitors. Do not use Y5V or Z5U type capacitors.
- Do not replace the ceramic input capacitor with any other type of capacitor. Any type of capacitor can be placed in parallel with the input capacitor.
- If a Tantalum input capacitor is placed in parallel with the input capacitor, it must be recommended for switching regulator applications and the operating voltage must be derated by 50%.
- In “Hot-Plug” applications, a Tantalum or Electrolytic bypass capacitor must be used to limit the over-voltage spike seen on the input supply with power is suddenly applied.

6.3 Inductor

- Keep the inductor connection to the switch node (SW) short.
- Do not route any digital lines underneath or close to the inductor.
- Keep the switch node (SW) away from the feedback (FB) pin.
- To minimize noise, place a ground plane underneath the inductor.
- The inductor can be placed on the opposite side of the PCB with respect to the IC. It does not matter whether the IC or inductor is on the top or bottom as long as there is enough air flow to keep the power components within their temperature limits. The input and output capacitors must be placed on the same side of the board as the IC.

6.4 Output Capacitor

- Use a wide trace to connect the output capacitor ground terminal to the input capacitor ground terminal.
- Phase margin will change as the output capacitor value and ESR changes. Contact the factory if the output capacitor is different from what is shown in the BOM.
- The feedback divider network must be placed close to the IC with the bottom of R2 connected to SGND.
- The feedback trace should be separate from the power trace and connected as close as possible to the output capacitor. Sensing a long high-current load trace can degrade the DC load regulation.

6.5 RC Snubber

- Place the RC snubber on either side of the board and as close to the SW pin as possible.

7.0 EVALUATION BOARD SCHEMATIC

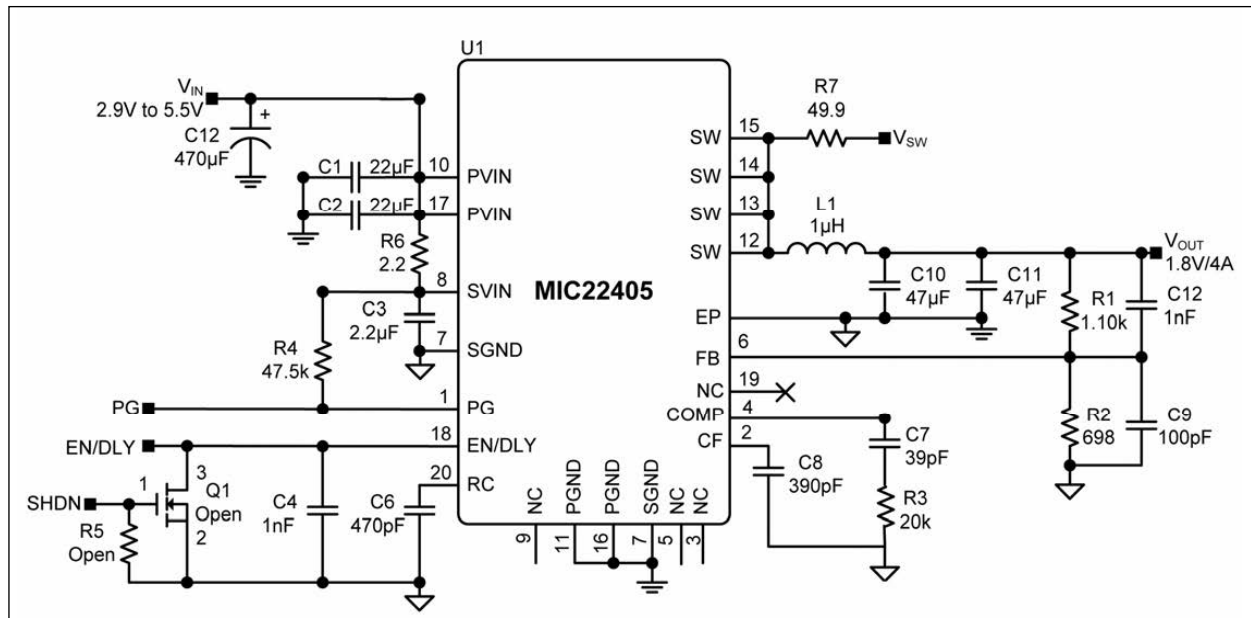


TABLE 7-1: BILL OF MATERIALS

Item	Part Number	Manufacturer	Description	Qty.
C1, C2	08056D226MAT	AVX	Capacitor, 22 μF, 6.3V, X5R, Size 0805	2
	C2012X5R0J226M	TDK		
	GRM21BR60J226ME39L	Murata		
C3	06036D225MAT2A	AVX	2.2 μF/6.3V, Ceramic Capacitor, X5R, Size 0603	1
	GRM188R60J225M	Murata		
	C1608X5R0J225M	TDK		
C4, C12	GRM188R71H102KA01D	Murata	Capacitor, 1 nF, 50V, X7R, Size 0603	2
	C1608C0G1H102J	TDK	Capacitor, 1 nF, 10V, COG, Size 0603	
	06035C102KAT2A	AVX		
C6	GRM188R71H471KA01D	Murata	Capacitor, 470 pF, 50V, X7R, Size 0603	1
	C1608X7R1H471K	TDK		
	06035C471KAT2A	AVX		
C7	C0603C390J5GACTU	Kemet	Capacitor, 39 pF, 50V, Size 0603	1
	C1608COG1H390J	TDK		
	06035A390JAT2A	AVX		
C8	GRM188R71H391KA01D	Murata	Capacitor, 390 pF, 50V, Size 0603	1
	1608COG1H391J	TDK		
	06035A391JAT2A	AVX		
C9	C0603X101J5GACAUTO	Kemet	Capacitor, 100 pF, 50V, Size 0603	1
	C1608COG1H101J	TDK		
	0603N101J500CT	Multicomp		
C10, C11	GRM31CR60J476ME19	Murata	Capacitor, 47 μF, 6.3V, X5R, Size 1206	2
	C3216X5R0J476M	TDK		
	12066D476MAT2A	AVX		

MIC22405

TABLE 7-1: BILL OF MATERIALS (CONTINUED)

Item	Part Number	Manufacturer	Description	Qty.
C _{IN}	ECA-1AM471	Panasonic	470 μ F, 10V, Electrolytic, 8x12.5-case	—
L	FP3-1R0-R (7.2x6.7x3mm)	Cooper	Inductor, 1 μ H, 6.26A	1
	CDRH8D28NP-1R0NC (8x6x3mm)	Sumida	Inductor, 1 μ H, 8A	
	SPM6530T-1R0M120 (7x6.5x3mm)	TDK	Inductor, 1 μ H, 12A	
R1	CRCW06031K10FKEA	Vishay	Resistor, 1.1 k Ω , 1%, Size 0603	1
R2	ERJP03F6980V	Panasonic	Resistor, 698 Ω , 1%, Size 0603	1
R3	ERJP03F2002V	Panasonic	Resistor, 20 k Ω , 1%, Size 0603	1
R4	CRCW060347K5FKEA	Vishay	Resistor, 47.5 k Ω , 1%, Size 0603	1
R5	(Open) CRCW0603100KFKEA	Vishay	Resistor, 100 k Ω , 1%, Size 0603	1
R6	CRCW06032R20FKEA	Vishay	Resistor, 2.2 Ω , 1%, Size 0603	1
R7	CRCW060349R9FKEA	Vishay	Resistor, 49.9 Ω , 1%, Size 0603	1
Q1	2N7002E	Vishay	Open	1
U1	MIC22405YML	Microchip	Integrated 4A Synchronous Buck Regulator	1

8.0 PCB LAYOUT RECOMMENDATIONS

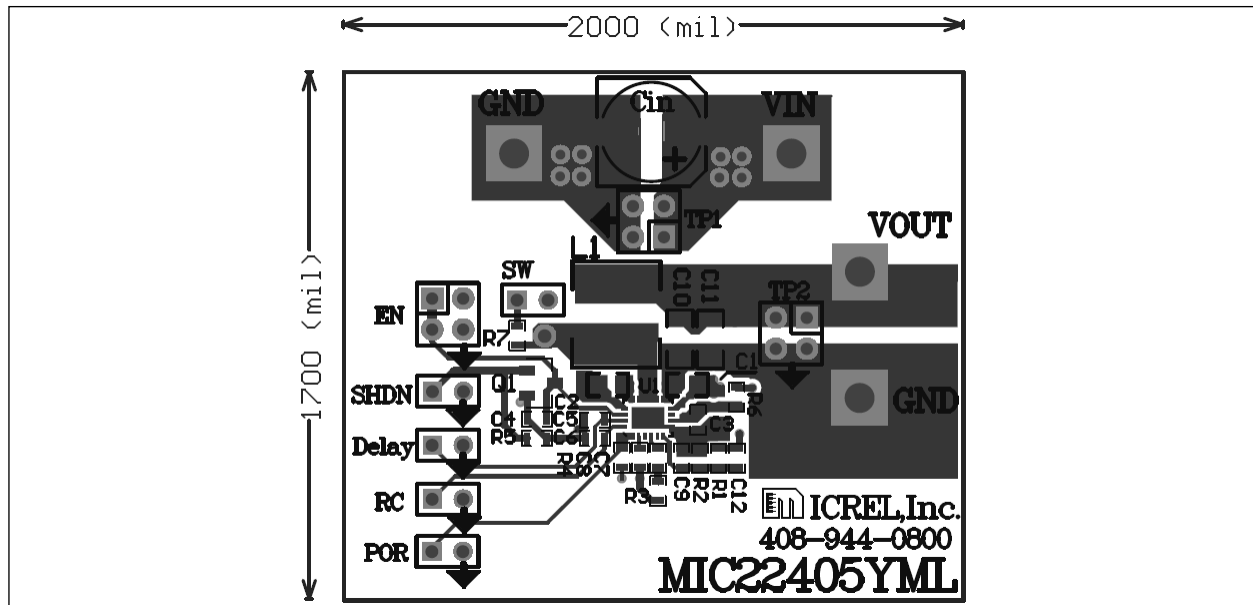


FIGURE 8-1: Evaluation Board Top Layer.

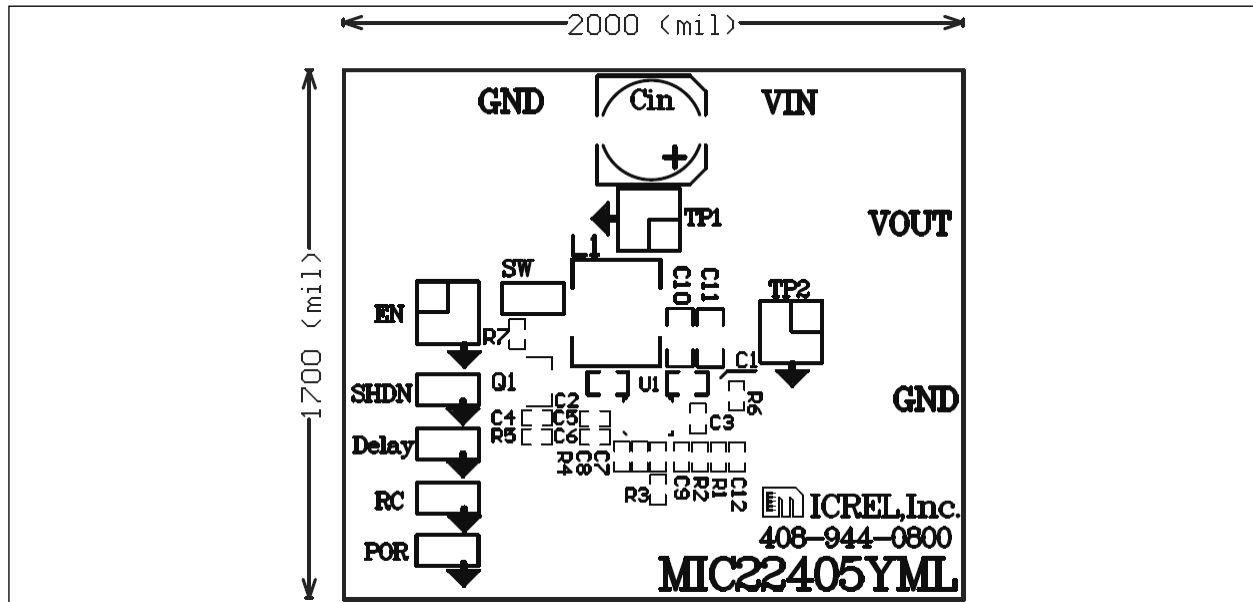


FIGURE 8-2: Evaluation Board Top Silk.

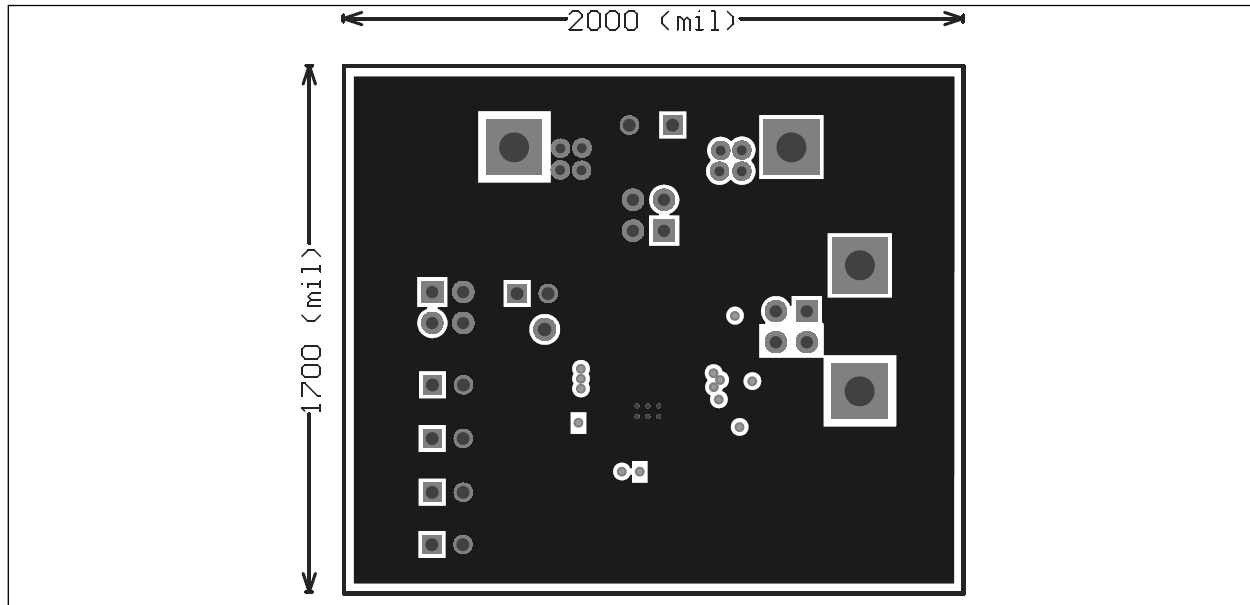


FIGURE 8-3: Evaluation Board Mid-Layer 1 (Ground Plane).

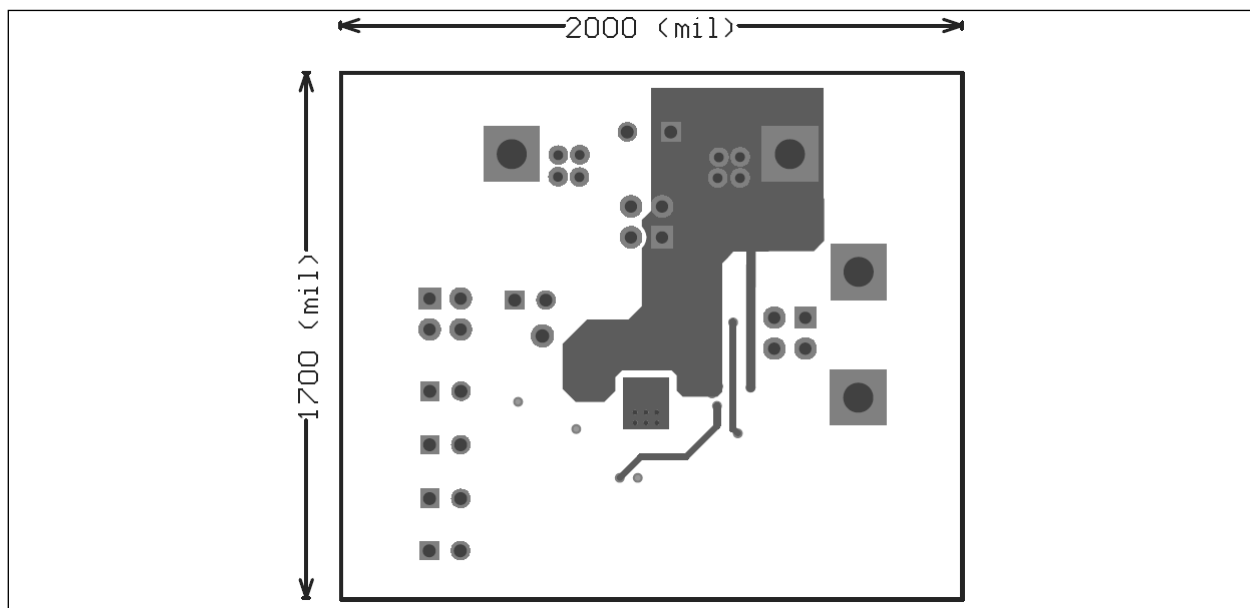


FIGURE 8-4: Evaluation Board Mid-Layer 2.

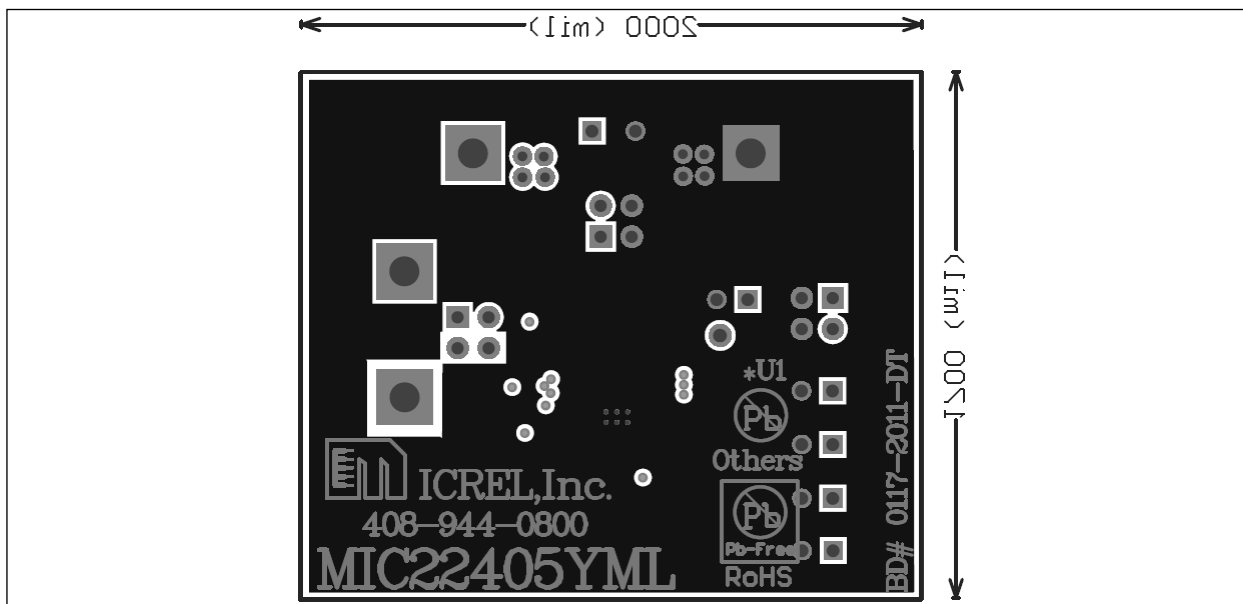


FIGURE 8-5: Evaluation Board Bottom Layer.

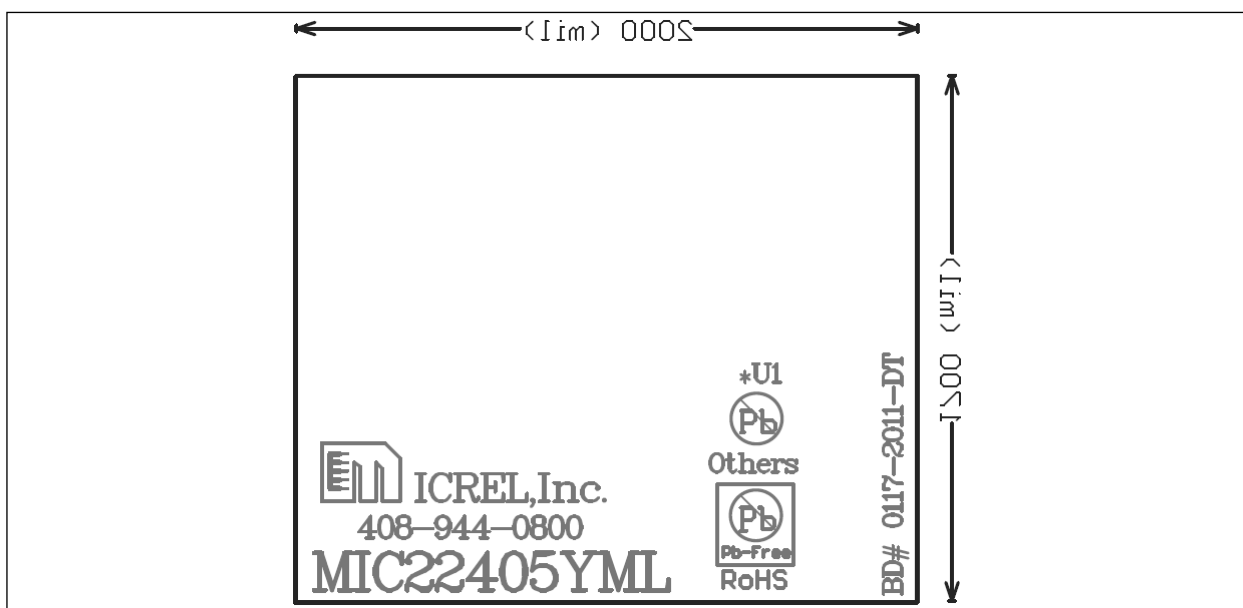
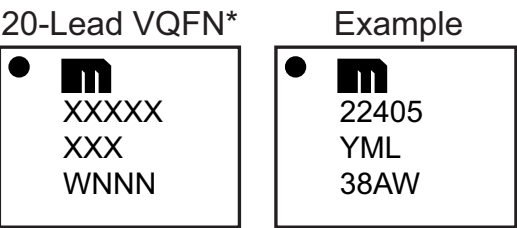


FIGURE 8-6: Evaluation Board Bottom Silk.

9.0 PACKAGING INFORMATION

9.1 Package Marking Information



Legend: XX...X Product code or customer-specific information
Y Year code (last digit of calendar year)
YY Year code (last 2 digits of calendar year)
WW Week code (week of January 1 is week '01')
NNN Alphanumeric traceability code
(e3) Pb-free JEDEC® designator for Matte Tin (Sn)
* This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

●, ▲, ▼ Pin one index is identified by a dot, delta up, or delta down (triangle mark).

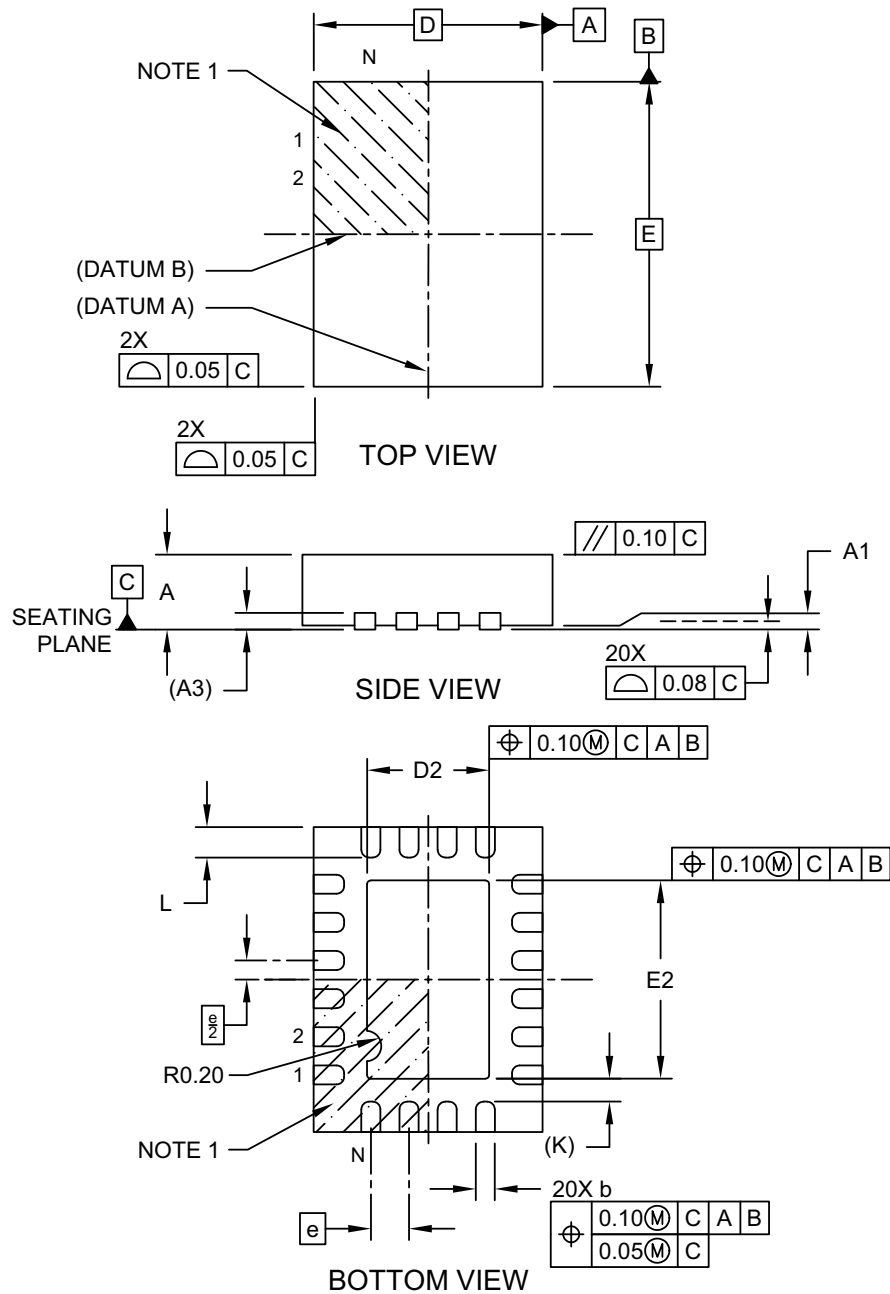
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

 Underbar (_) and/or Overbar (¯) symbol may not be to scale.

Note: If the full seven-character YYWWNNN code cannot fit on the package, the following truncated codes are used based on the available marking space:
6 Characters = YWWNNN; 5 Characters = WWNNN; 4 Characters = WNNN; 3 Characters = NNN;
2 Characters = NN; 1 Character = N

20-Lead Very Thin Plastic Quad Flat, No Lead Package (NQA) - 3x4 mm Body [VQFN] With 1.6x2.6 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

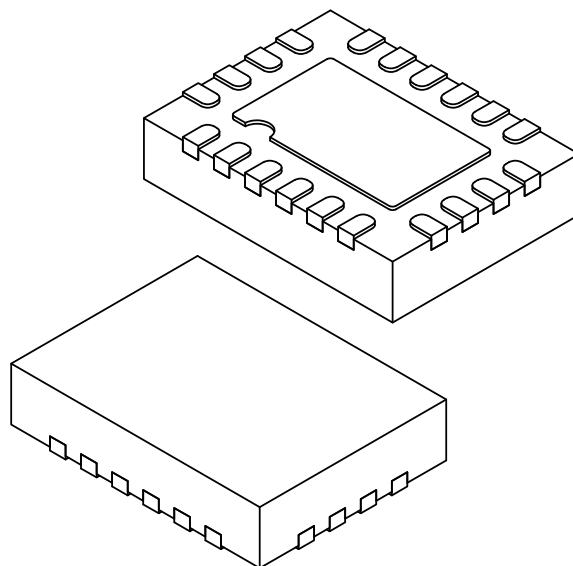


Microchip Technology Drawing C04-1106 Rev A Sheet 1 of 2

MIC22405

20-Lead Very Thin Plastic Quad Flat, No Lead Package (NQA) - 3x4 mm Body [VQFN] With 1.6x2.6 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N	20		
Pitch	e	0.50 BSC		
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3	0.203 REF		
Overall Length	D	4.00 BSC		
Exposed Pad Length	D2	2.55	2.60	2.65
Overall Width	E	3.00 BSC		
Exposed Pad Width	E2	1.55	1.60	1.65
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K	0.20 REF		

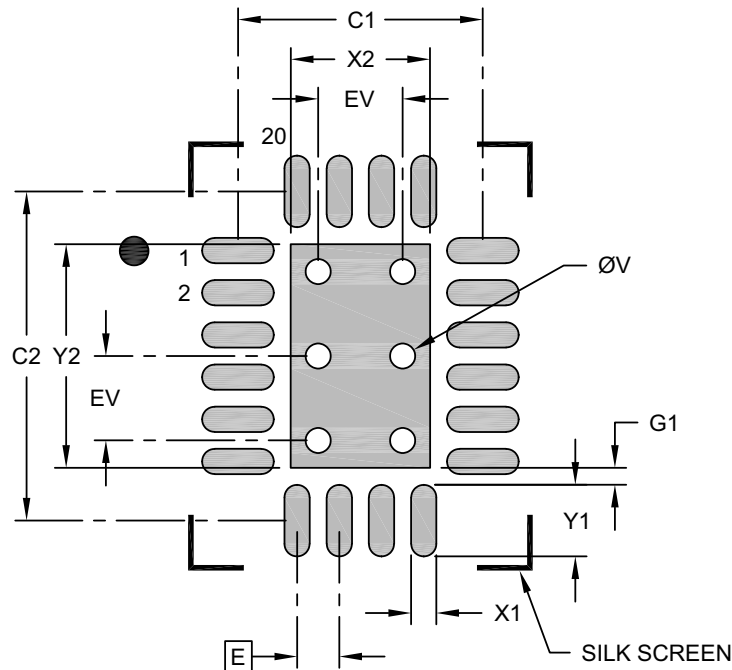
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1106 Rev A Sheet 2 of 2

20-Lead Very Thin Plastic Quad Flat, No Lead Package (NQA) - 3x4 mm Body [VQFN] With 1.6x2.6 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

		Units	MILLIMETERS		
Dimension		Limits	MIN	NOM	MAX
Contact Pitch	E		0.50 BSC		
Center Pad Width	X2				1.65
Center Pad Length	Y2				2.65
Contact Pad Spacing	C1			2.90	
Contact Pad Spacing	C2			3.90	
Contact Pad Width (X20)	X1				0.30
Contact Pad Length (X20)	Y1				0.85
Contact Pad to Center Pad (X20)	G1		0.20		
Contact Pad to Contact Pad (X20)	G2		0.20		
Thermal Via Diameter	V			0.30	
Thermal Via Pitch	EV			1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-3106 Rev A

MIC22405

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (September 2025)

- Converted Micrel document MIC22405 to Microchip data sheet DS20007042A.
- Minor text changes throughout.

MIC22405

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

<u>Part Number</u>	<u>X</u>	<u>X</u>	<u>-XX</u>	Examples:
Device	Temp. Range	Package	Media Type	
Device:	MIC22405:	4A Integrated Switch High-Efficiency Synchronous Buck Regulator with Frequency Programmable up to 4 MHz		a) MIC22405YML-TR: MIC22405, -40°C to +125°C Temp. Range, 20-Lead VQFN, 5,000/Reel Note: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.
Temperature Range:	Y	=	-40°C to +125°C	
Package:	ML	=	20-Lead 3 mm x 4 mm VQFN	
Media Type:	TR	=	5,000/Reel	

MIC22405

NOTES:

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