

ACOT™ Design Guide: Control-Loop Analysis and Performance Optimization

AN7166



Introduction

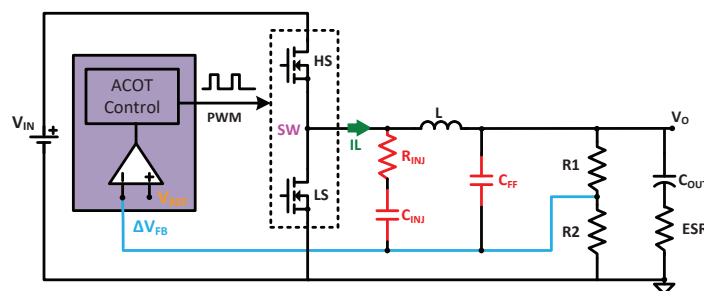
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This application note is a continuation of Part 1 (AN7167), titled “Introduction to Microchip’s Adaptive Constant-On-Time (ACOT™) Control and Ripple Injection Methods”, where the fundamental operating principles of ACOT control and various ripple injection techniques were introduced. ACOT control, also known as Microchip’s Hyper Speed Control® architecture, powers many of Microchip’s high-performance wide-input-voltage DC-DC converters, including devices such as the MIC2129, MIC24097, MIC28515, MIC28516, and other ACOT-based controller devices.

While multiple ripple injection methods are available, modern power supply designs increasingly demand very low output voltage ripple, particularly in applications such as POL converters, FPGAs, processors, and high-speed digital systems. Under these conditions, relying on output capacitor ESR to generate ripple (Type 1) or using moderate ripple through feed-forward techniques (Type 2), becomes impractical.

As a result, the Type 3 ripple injection scheme, in which ripple is derived from the switching node using an RC network along with a feed-forward capacitor has emerged as the most widely adopted approach in practical ACOT designs. This application note focuses on an in-depth analysis of the Type 3 ripple injection method (illustrated in Figure 1), with the objective of providing a comprehensive understanding of how ripple injection influences control loop behavior, stability and transient performance.

Figure 1. Type 3 Ripple Injection Scheme



ACOT control loop design can be approached from two complementary perspectives: a time-domain view and a frequency-domain view. Frequency-domain analysis provides deeper insight into why the system behaves the way it does. By representing the ACOT control loop using an S-domain model, the interactions between the ripple injection network, feedback network, and power stage can be understood in terms of loop gain, poles and zeros. This perspective reveals how ripple injection directly shapes bandwidth, phase margin and overall dynamic performance.

While ACOT converters can be designed successfully without performing a full frequency-domain analysis, understanding the control loop in this domain enables more precise and intentional design. In this application note, the frequency-domain foundation of ACOT control is first established to provide a clear understanding of loop behavior. This is then translated into practical design methodology, followed by real design examples and experimental validation. Through this approach, the document aims to connect theoretical analysis with practical implementation, enabling both intuitive and precise ACOT control loop design.

1. Control Loop Analysis

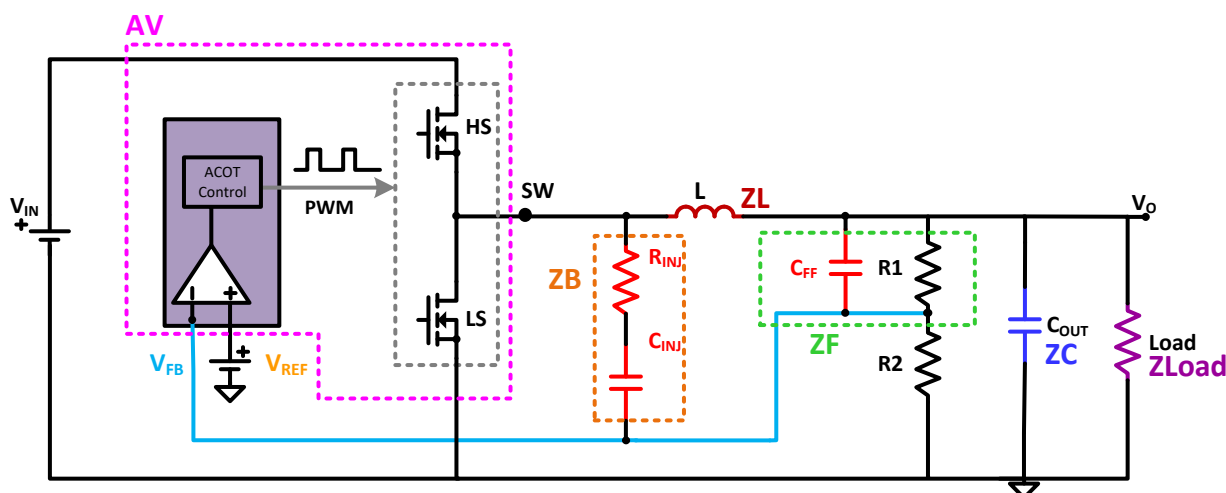
Frequency-domain analysis is important because it helps translate the time-domain switching behavior of any converter into a control-loop view that is easier to analyze, design and optimize. In the time domain, ACOT operation is understood through switching-node pulses, feedback ripple, inductor current and transient response.

However, for loop design, it is also necessary to understand how the ripple-injection network, feedback network and output LC filter shape the loop gain across frequency. S-domain analysis provides this framework by replacing resistors, inductors and capacitors with their corresponding impedances. This allows the ACOT loop to be represented using impedance ratios, making it possible to identify poles, zeros, crossover frequency and phase-margin-related behavior. In this way, S-domain analysis connects the physical ripple-injection components to the frequency-domain loop response and provides useful insight for stable and optimized ACOT design.

1.1. Loop Gain Modeling

Deeper analysis often necessitates circuit modeling, to provide greater insight. However, conventional modeling methods are typically designed for converters operating at fixed frequencies. This poses a challenge for ripple-based variable-frequency converters like those employing COT or ACOT control, which dynamically adjust their frequency in response to load and input voltage variations. However, for the modeling and analysis purpose, we make some practical assumptions to develop an ACOT and ripple-injection circuit model as illustrated in Figure 1-1 and the following derivations.

Figure 1-1. ACOT Control Loop Model



ZL = Impedance of Inductor	AV = Combined Gain of Modulator and MOSFET Power Stage
ZB = Impedance of R_{INJ} and C_{INJ}	V_{SW} = Voltage at SW (switching node), F_{SW} = Switching Frequency
ZF = Impedance of C_{FF} and R1	V_{FB} = Voltage at Feedback
ZC = Impedance of Output Capacitor	V_O = Output Voltage
ZLoad = Impedance of load	V_{REF} = Reference to the Error Comparator

We define AV as the combination of the modulator gain and MOSFET power stage gain for analysis purposes. The feedback circuit gain can be expressed as:

Equation 1-1.

$$G_{FB} = -\frac{V_{FB}}{V_O}$$

From [Figure 1-1](#), the LC filter stage gain can be expressed as:

Equation 1-2.

$$G_{LC} = \frac{V_O}{V_{SW}} = \frac{Z_C \parallel Z_{LOAD}}{Z_L + Z_C \parallel Z_{LOAD}}$$

From [Equation 1-1](#), [Equation 1-2](#) and [Figure 1-1](#), the Overall Loop Gain (G) can be expressed as:

Equation 1-3.

$$G = G_{FB} \cdot AV \cdot G_{LC}$$

Equation 1-3 can be rewritten as:

Equation 1-4.

$$G = -\frac{V_{FB}}{V_O} \cdot AV \cdot \frac{Z_C \parallel Z_{LOAD}}{Z_L + Z_C \parallel Z_{LOAD}}$$

Next, we aim to derive an expression for V_{FB}/V_O in relation to the impedances of the ripple injection circuit, allowing us to establish a correlation between the ripple injection components and loop gain. The detailed mathematical derivation for V_{FB}/V_O is provided in [Appendix 1: Derivation of ACOT Loop Gain](#). In summary, the Overall Loop Gain (G) can be expressed as:

Equation 1-5.

$$G \cong -\frac{Z_B}{Z_F} \cdot \frac{Z_C \parallel Z_{LOAD}}{Z_C \parallel Z_{LOAD} + Z_L}$$

As stated in [Figure 1-1](#), Z_B is the impedance of R_{INJ} and C_{INJ} , which can be expressed as:

Equation 1-6.

$$Z_B = R_{INJ} + \frac{1}{(2\pi \cdot F_{SW} \cdot C_{INJ})}$$

And Z_F is the impedance of $R1$ and C_{FF} , which can be expressed as:

Equation 1-7.

$$Z_F = \frac{R1}{1 + (2\pi \cdot F_{SW} \cdot R1 \cdot C_{FF})}$$

From [Equation 1-5](#), it is evident that the factor of Z_B/Z_F , that is, the ratio of the impedances of RC ripple injection and feed-forward circuits, plays a crucial role in enhancing the loop gain. From the basics of control theory, it is understood that the **higher loop gains improve overall regulation** (both DC set point accuracy and transient performance).

1.1.1. Key Insight

Equation 1-5 shows that the ACOT loop gain is directly influenced by the ratio Z_B/Z_F , which is determined by the ripple injection and feed-forward components. Therefore, R_{INJ} , C_{INJ} and C_{FF} are not only used to generate the required feedback ripple, but also play an important role in shaping the control loop response, including bandwidth, stability, and transient behavior.

1.2. Poles and Zeros

Understanding the poles and zeros of the ACOT control loop is essential for developing an effective control-loop design strategy. While the S-domain representation provides the mathematical framework for modeling the system, poles and zeros offer intuitive insight into how the loop gain behaves across frequency. Poles introduce phase lag and reduce gain slope, whereas zeros provide phase boost and help counteract the effects of dominant poles, particularly the double pole introduced by the output LC filter.

By appropriately placing these poles and zeros, the designer can shape the loop response to achieve a desired crossover frequency, sufficient phase margin, and stable operation. In ACOT control, where ripple injection replaces conventional compensation networks, the locations of poles and zeros are directly governed by the ripple injection and feedback components. Therefore, identifying and positioning these poles and zeros correctly is a critical step in ensuring both stability and optimal transient performance of the converter.

To quantitatively identify and locate these poles and zeros, the ACOT control loop must be expressed in terms of its S-domain impedance model. By representing each circuit element using its equivalent impedance, the ripple injection network, feedback network, and power stage can be combined into a unified loop-gain expression. This formulation allows the complex switching behavior of ACOT control to be translated into a continuous frequency-domain model, from which the dominant poles, zeros, and gain characteristics can be extracted.

Based on the S-domain equivalent circuit shown in [Figure 1-1](#), the following impedance relationships and loop-gain expressions are used to derive the standard pole-zero form of the ACOT control loop.

The basic S-domain impedance relationships used for this analysis are:

Equation 1-8.

$$\begin{aligned} Z_R(s) &= R \\ Z_L(s) &= sL \\ Z_C(s) &= \frac{1}{sC} \end{aligned}$$

For the ACOT control-loop model, the ripple-injection impedance is formed by R_{INJ} and C_{INJ} :

Equation 1-9.

$$Z_B(s) = R_{INJ} + \frac{1}{sC_{INJ}}$$

This can be rewritten as:

Equation 1-10.

$$Z_B(s) = \frac{1 + sR_{INJ}C_{INJ}}{sC_{INJ}}$$

The feed-forward feedback impedance is formed by $R1$ and C_{FF} :

Equation 1-11.

$$\begin{aligned} Z_F(s) &= R1 \parallel \frac{1}{sC_{FF}} \\ Z_F(s) &= \frac{R1}{1 + sR1C_{FF}} \end{aligned}$$

The output capacitor, inductor and load impedances are:

Equation 1-12.

$$\begin{aligned} ZC(s) &= \frac{1}{sC_{OUT}} \\ ZL(s) &= sL \\ Z_{LOAD}(s) &= R_{LOAD} \end{aligned}$$

Recalling Equation 1-5, ACOT loop gain can be expressed as:

Equation 1-13.

$$G(s) \cong -\frac{Z_B}{Z_F} \cdot \frac{Z_C \parallel Z_{LOAD}}{Z_C \parallel Z_{LOAD} + Z_L}$$

The transformation of $G(s)$ from this impedance-based expression into the final pole-zero form is provided in [Appendix 2: Step-by-Step Derivation of ACOT Loop Gain in S-Domain](#). This final form allows the dominant poles and zeros of the ACOT control loop to be identified and used for loop design.

Equation 1-14.

$$G(s) \cong \frac{\frac{1 + sR_{INJ}C_{INJ}}{sC_{INJ}}}{\frac{R1}{1 + sR1C_{FF}}} \cdot \frac{\frac{R_{LOAD}}{1 + sR_{LOAD}C_{OUT}}}{\frac{R_{LOAD}}{1 + sR_{LOAD}C_{OUT}} + sL}$$

This expression can be arranged into standard pole-zero form:

Equation 1-15.

$$G(s) = \frac{K \left(1 + \frac{s}{\omega_{Z1}}\right) \left(1 + \frac{s}{\omega_{Z2}}\right)}{s \left[1 + \frac{s}{Q\omega_p} + \left(\frac{s}{\omega_p}\right)^2\right]}$$

From this form, the gain constant, poles and zeros can be identified as follows:

Equation 1-16.

$$\begin{aligned} K &= \frac{1}{R1C_{INJ}} \\ \omega_p &= \frac{1}{2\pi\sqrt{LC_{OUT}}} \\ \omega_{Z1} &= \frac{1}{R_{INJ}C_{INJ}} \\ \omega_{Z2} &= \frac{1}{R1C_{FF}} \end{aligned}$$

1.2.1. Key Insight

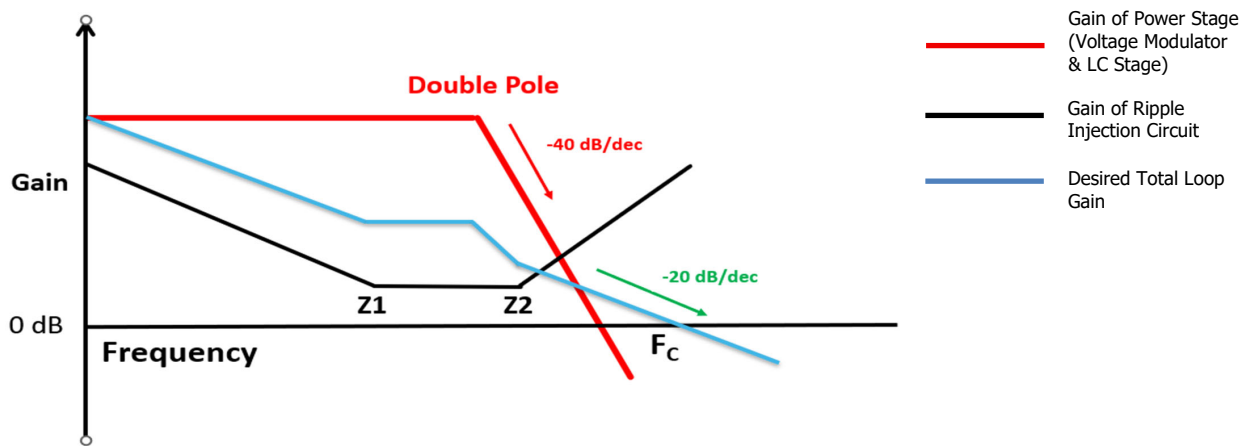
From above expressions, the ACOT loop contains one low-frequency pole from the $1/s$ term, a double pole from the output LC filter, and two zeros introduced by the ripple-injection and feed-forward networks. The first zero, ω_{Z1} , is mainly set by R_{INJ} and C_{INJ} , while the second zero, ω_{Z2} , is mainly set by $R1$ and C_{FF} . These zeros are important because they help compensate for the phase lag introduced by the output LC double pole and improve the phase margin near crossover frequency. Thus, proper placement of C_{INJ} , R_{INJ} and C_{FF} directly determines the stability and transient performance of the ACOT converter.

1.3. Control Loop Design Strategy

In any switching converter, control loop design fundamentally involves the strategic placement of poles and zeros to shape the loop gain response across frequency. Each pole and zero directly influences the gain slope and phase behavior of the system, thereby determining stability and dynamic performance. Poles tend to introduce phase lag and reduce stability margin, while zeros provide phase boost and help counteract the effects of dominant poles, such as the double pole introduced by the output LC filter. By carefully selecting the locations of these poles and zeros, the designer can control key parameters such as crossover frequency, phase margin, and transient response.

In ACOT control, this principle remains the same; however, instead of using a traditional error amplifier and compensation network, the placement of poles and zeros is primarily governed by the ripple injection and feedback components. As a result, ACOT control loop design can be effectively viewed as a structured process of shaping the frequency response through appropriate selection of R_{INJ} , C_{INJ} and C_{FF} to achieve the desired stability and performance.

Figure 1-2. Loop Gain Formation Using Pole-Zero Interaction



The control loop design strategy for ACOT control focuses on shaping the loop gain profile through proper placement of poles and zeros to ensure stability and optimal transient performance. As illustrated in Figure 1-2, the red curve represents the effect of the output LC filter, which introduces a double pole at $\omega_p = \frac{1}{\sqrt{LC_{OUT}}}$.

This results in a steep -40 dB/decade slope, causing significant phase lag. If left uncompensated, this would make the system unstable. To counteract this, zeros are introduced through the ripple injection and feedback networks. The first zero (Z1), visible as the flattening of the black curve in the mid-frequency region, is placed around $\frac{F_{LC}}{10}$ to $\frac{F_{LC}}{20}$ to reduce phase lag and improve mid-frequency response.

The second zero (Z2), which causes an upward trend in the black curve near crossover, is positioned closer to the crossover frequency to provide additional phase boost and ensure sufficient phase margin, typically at least 60°. The resulting overall loop gain (shown in blue) combines these effects, transitioning from the steep -40 dB/decade slope to a more manageable -20 dB/decade slope (green region) near the crossover frequency F_c , where the gain crosses 0 dB. This controlled shaping of the gain profile ensures stable operation while maintaining fast transient response.

It is important to note that, in this analysis, the output capacitor ESR zero is not explicitly considered. This is because the discussion is focused on the Type 3 ripple injection scheme, which is typically used in designs employing very low-ESR output capacitors, such as MLCCs. In such cases, the ESR zero occurs at a very high frequency, often well beyond the crossover frequency and the region of interest for control loop design.

As a result, it does not provide any meaningful phase boost in the operating bandwidth and can be safely neglected for the purpose of loop analysis. This assumption further reinforces the need for introducing zeros through the ripple injection and feed-forward networks, as they become the primary means of compensating the phase lag introduced by the output LC double pole.

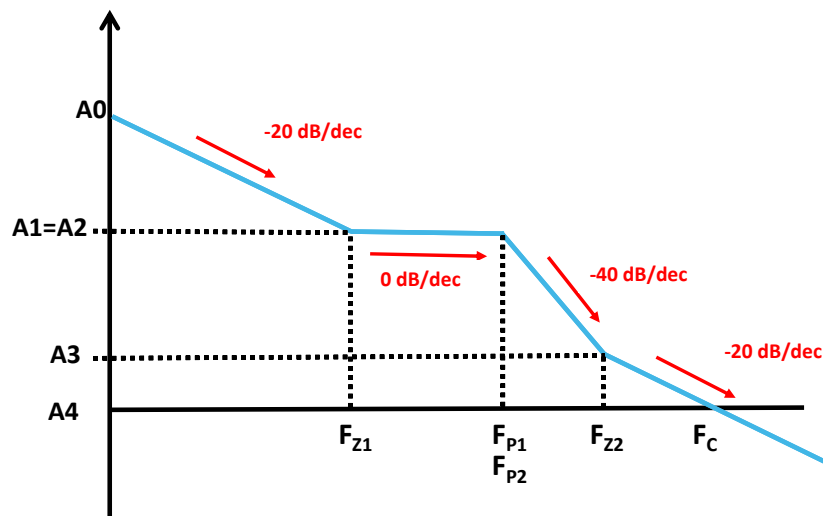
1.4. The Crossover Frequency

The crossover frequency (F_C) is one of the most critical parameters in control loop design, as it defines the effective bandwidth of the converter and directly determines the trade-off between transient response and stability. A higher crossover frequency generally enables faster transient response, while a lower crossover frequency improves stability margin. Therefore, accurate estimation and proper placement of F_C is essential in achieving an optimal balance between dynamic performance and robust operation in ACOT-controlled converters.

The determination of F_C can be understood from the loop gain profile shown in Figure 1-3. Starting from the low-frequency gain A_0 , the loop exhibits a **-20 dB/decade slope**, which is introduced by the dominant low-frequency pole associated with the ripple injection network. At the first zero frequency (F_{Z1}), this slope is canceled, resulting in a **flat gain region (0 dB/decade)** between F_{Z1} and the LC double pole frequency ($F_{P1} = F_{P2}$).

Beyond this point, the output LC filter introduces a **-40 dB/decade slope**, causing a rapid reduction in loop gain. The second zero (F_{Z2}), introduced by the feed-forward capacitor, provides phase boost and changes the slope to **-20 dB/decade**. The crossover frequency F_C is defined as the point where this overall gain curve intersects the 0 dB line. Thus, F_C is determined by the cumulative gain changes across these frequency regions.

Figure 1-3. ACOT Control Loop Gain Approximation



To derive F_C , the logarithmic gain relationship is used:

Equation 1-17.

$$\text{Gain}_2 = \text{Gain}_1 + (\text{Slope}) \cdot \log\left(\frac{F_2}{F_1}\right)$$

Applying this relationship step-by-step across the regions shown in [Figure 1-3](#):

- From A_0 to A_1 (slope = -20 dB/dec): $A_1 = A_0 - 20\log\left(\frac{F_{Z1}}{F_0}\right)$
- From A_1 to A_2 (flat region): $A_2 = A_1$
- From A_2 to A_3 (slope = -40 dB/dec): $A_3 = A_2 - 40\log\left(\frac{F_P}{F_{Z1}}\right)$
- From A_3 to crossover F_C (slope = -20 dB/dec): $A_4 = 0 = A_3 - 20\log\left(\frac{F_C}{F_{Z2}}\right)$

Substituting backward and simplifying these relationships leads to an expression for crossover frequency in terms of system parameters after rearranging and substituting the pole and zero locations:

Equation 1-18.

$$F_{Z1} = \frac{1}{2\pi R_{INJ} C_{INJ}}, \quad F_{Z2} = \frac{1}{2\pi R_1 C_{FF}}, \quad F_P = \frac{1}{2\pi \sqrt{L} C_{OUT}}$$

A detailed derivation, including application of logarithmic gain relationships and substitution of pole-zero locations, is provided in [Appendix 3: Derivation of Crossover Frequency](#). After performing these steps and simplifying the expressions, the crossover frequency can be expressed as:

Equation 1-19.

$$F_C = \frac{R_{INJ} \cdot C_{FF}}{2\pi L C_{OUT}}$$

Further, using the ripple injection relationship:

Equation 1-20.

$$\Delta V_{FB} = \frac{V_{IN} \cdot D \cdot (1 - D)}{R_{INJ} \cdot C_{FF} \cdot F_{SW}}$$

and rearranging and substituting into [Equation 1-19](#), the crossover frequency can be rewritten as:

Equation 1-21.

$$F_C = \frac{V_O \cdot (1 - D)}{2\pi L C_{OUT} \cdot \Delta V_{FB} \cdot F_{SW}}$$

1.4.1. Key Insight

This final expression provides key design insight, showing that the crossover frequency is directly controlled by the ripple injection network and operating conditions, and inversely proportional to the output LC filter. It highlights that in ACOT control, tuning the feedback ripple ΔV_{FB} effectively allows the designer to set the loop bandwidth and thereby optimize both transient response and stability.

2. Design Example (Using Frequency Domain Analysis)

The analytical framework developed in the previous sections provides a clear understanding of ACOT control loop behavior, including pole-zero placement and crossover frequency determination. The next step is to apply these concepts to a practical design scenario. This section introduces a real design example to demonstrate how the ripple injection network can be implemented to achieve the desired loop characteristics and performance targets.

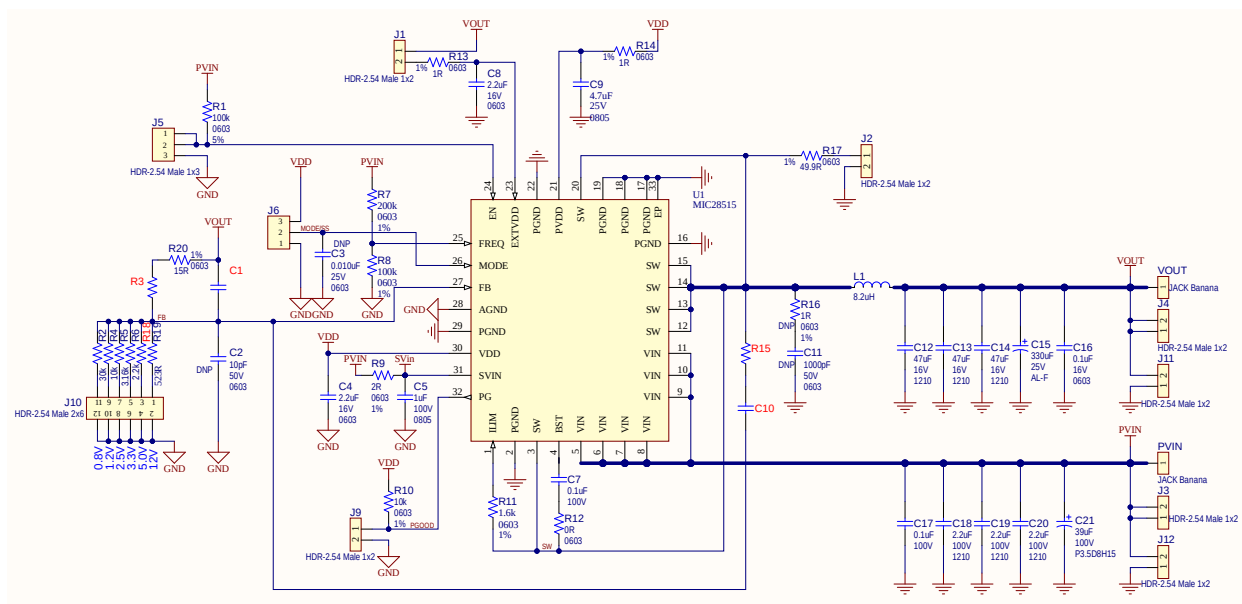
2.1. Control Loop Design of 48V to 5V Buck Converter Using MIC28515

The schematic shown in Figure 2-1 represents the MIC28515 evaluation board configured for this example and the Table 2-1 summarizes the design specifications. The design is based on an input voltage of 48V, an output voltage of 5V, and a maximum load current of 5A, with a switching frequency of 266 kHz. Additionally, a tight output voltage ripple requirement of 20 mV is specified, which necessitates the use of low-ESR output capacitors and, consequently, a Type 3 ripple injection scheme. The key components involved in the control loop design are highlighted in red, including the feedback divider (R3, R18) the feed-forward capacitor (C1) and the ripple injection network (R15, C10).

Table 2-1.

Parameter	Value
Input Voltage	48 V
Output Voltage	5 V
Maximum Output Current	5 A
Switching Frequency	266 kHz
Output Ripple Requirement	20 mV

Figure 2-1. MIC28515 EVB Schematic With Ripple Injection Components and Feedback Resistor Highlighted



The actual evaluation board uses specific reference designators (R3, R18, C1, R15 and C10). To simplify the control-loop design discussion and derivations throughout this document, generic component names are used. The table below maps the generic design variables used in the equations to their corresponding components in the evaluation board schematic.

Table 2-2.

Generic Name (Used in App Note)	EVb Schematic Reference	Function
R1	R3	Upper feedback resistor
R2	R18	Lower feedback resistor
C _{FF}	C1	Feed-forward capacitor
R _{INJ}	R15	Ripple injection resistor
C _{INJ}	C10	Ripple injection capacitor

The primary design objective in this example is to determine appropriate values for the ripple injection components such that the loop achieves the desired crossover frequency, maintains sufficient phase margin and delivers fast transient response while meeting the low output ripple specification.

This example will illustrate how the theoretical relationships derived earlier can be directly applied to select component values and validate the overall control loop performance.

2.2. Design Steps

1. **Select R2:** The lower feedback resistor R2 is selected in the kΩ range to limit the feedback divider bias current.
For this design example, R2 = 3 kΩ is selected, considering V_{REF} = 0.6V and approximately 200 μA bias current.
2. **Calculate R1:** Once R2 is selected, R1 is calculated based on the required output voltage using:

Equation 2-1.

$$R1 = R2 \cdot \left(\frac{V_{OUT}}{V_{REF}} - 1 \right)$$

For V_{OUT} = 5V, the calculated value is: R1 = 22 kΩ

3. **Choose F_C:** The crossover frequency is selected between F_{SW}/10 and F_{SW}/20. Since F_{SW} = 266 kHz, a crossover frequency of F_C = 20 kHz is chosen.
4. **Calculate ΔV_{FB}:** The feedback ripple must be within 40 mV to 200 mV, unless otherwise specified in the data sheet. It is estimated using:

Equation 2-2.

$$\Delta V_{FB} = \frac{V_O \cdot (1 - D)}{2\pi \cdot L \cdot C_{OUT} \cdot F_C \cdot F_{SW}}$$

For this design, the initial calculated feedback ripple is: ΔV_{FB} = 130 mV. This value must be recalculated after selecting C_{FF} and R_{INJ}.

5. **Calculate C_{FF}:** The feed-forward capacitor is selected to place the second zero slightly below F_C. In this example, F_{Z2} is placed at F_C/√3, providing sufficient phase boost at crossover. So, C_{FF} can be calculated using:

Equation 2-3.

$$C_{FF} = \frac{\sqrt{3}}{2\pi \cdot R1 \cdot F_C}$$

The calculated value is approximately: C_{FF} = 630 pF. For testing, the value selected is: C_{FF} = 560 pF.

6. **Calculate R_{INJ}:** The ripple injection resistor is calculated using rearranged Equation 1-20 as:

Equation 2-4.

$$R_{INJ} = \frac{V_O \cdot (1 - D)}{\Delta V_{FB} \cdot C_{FF} \cdot F_{SW}}$$

The calculated value is approximately: $R_{INJ} = 230 \text{ k}\Omega$. For practical implementation and testing, the standard value selected in this example is: $R_{INJ} = 200 \text{ k}\Omega$.

7. **Recalculate Feedback Ripple (ΔV_{FB}):** After selecting practical component values for C_{FF} and R_{INJ} , it is important to recalculate the resulting feedback ripple to account for deviations from the ideal calculated values.

For $C_{FF} = 560 \text{ pF}$ and $R_{INJ} = 200 \text{ k}\Omega$, the recalculated feedback ripple is: $\Delta V_{FB} = 150 \text{ mV}$.

It is essential to verify that this final value lies within the recommended operating range specified for the device. Ensuring that the feedback ripple remains within this range is critical for maintaining proper comparator operation, avoiding noise sensitivity or jitter, and achieving stable and predictable control loop performance.

8. **Calculate F_{LC} and C_{INJ} :** The LC resonant frequency is calculated first using [Equation 1-20](#). For this design: $F_{LC} = 5 \text{ kHz}$. The DC blocking capacitor C_{INJ} is then selected to place the first zero 1-2 decades below F_{LC} .

In this example, first zero is placed two decades below F_{LC} . So C_{INJ} can be calculated using:

Equation 2-5.

$$C_{INJ} = \frac{10^2}{2\pi \cdot R_{INJ} \cdot F_{LC}}$$

The calculated value is: $C_{INJ} = 15.9 \text{ nF}$. For testing, the selected value is: $C_{INJ} = 15 \text{ nF}$.

9. **Verify Stability Criteria:** The final step is to ensure we meet the required stability criteria. The impedance of C_{FF} at the switching frequency should be much smaller than the equivalent feedback resistance ($R1 \parallel R2$), so that the current through the feedback resistors can be neglected, allowing the feed-forward capacitor to effectively couple the switching ripple to the feedback node. This can be verified using:

Equation 2-6.

$$\frac{1}{2\pi \cdot C_{FF} \cdot F_{SW}} \ll R1 \parallel R2$$

For the selected values: $1.06 \text{ k}\Omega < 2.64 \text{ k}\Omega$. This confirms that the stability criterion is satisfied. Therefore, the ACOT control loop design is complete. However, final validation must always be performed on the bench to confirm feedback ripple, phase margin, and transient response.

2.3. Bench Test Results

While frequency-domain analysis and theoretical calculations provide a strong foundation for ACOT control loop design, it is essential to validate the design through bench measurements. Practical implementations are influenced by parasitic, component tolerances, layout effects, and non-idealities that are not fully captured in analytical models. Therefore, bench testing is critical to confirm that the designed loop achieves the intended crossover frequency, phase margin, and transient performance under real operating conditions. [Figure 2-2](#) shows the implemented test schematics along with the selected ripple injection component values and feedback resistors.

Figure 2-2. MIC28515 Schematic Used for Bench Testing After Populating the Component Values Obtained From the Design Example

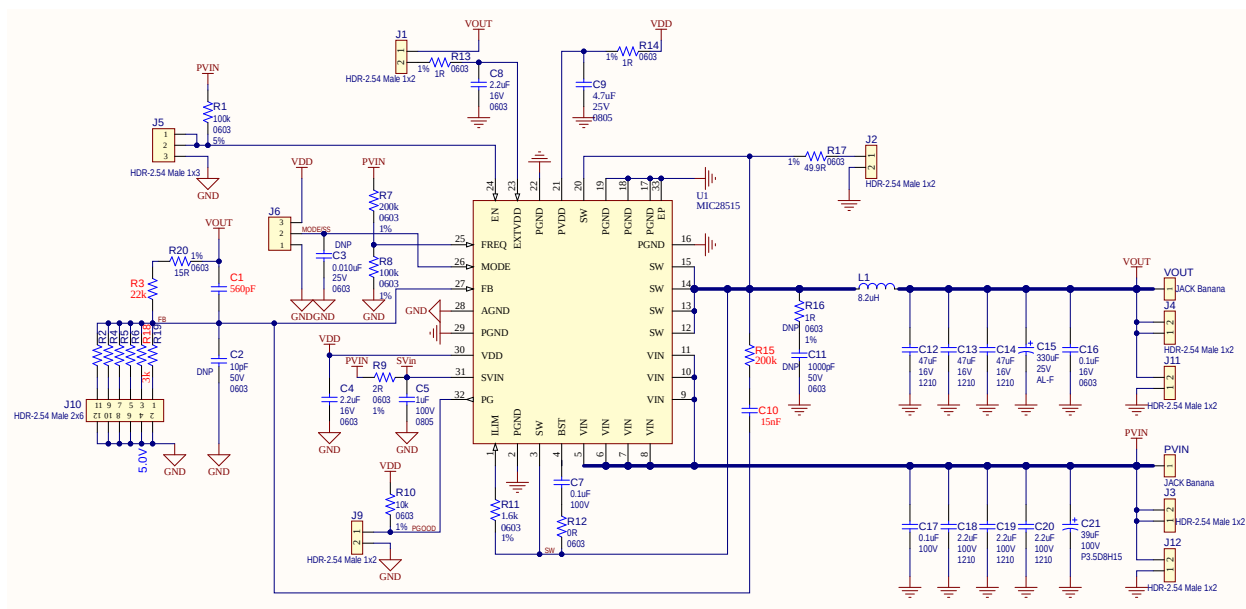
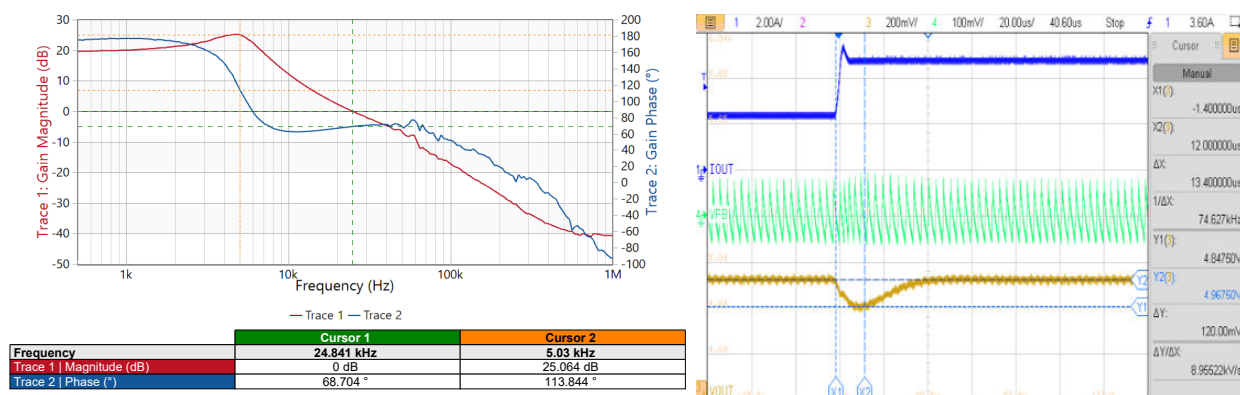


Figure 2-3. AC Analysis and Transient Response



Ripple Injection Components	ΔV_{FB}	F_C	Phase Margin	Undershoot	Response Time	Settling Time
$C_{INJ} = 15 \text{ nF}$, $R_{INJ} = 200 \text{ k}\Omega$, $C_{FF} = 560 \text{ pF}$	135 mV	24.8 kHz	68°	120 mV	13.4 μs	30 μs

The designed ACOT control loop is validated using frequency-domain measurements, as shown in the Bode plot. The gain crosses 0 dB at approximately 24.8 kHz, which closely matches the targeted crossover frequency selected during the design process. At this point, the measured phase margin is around 68°, indicating a stable control loop with sufficient margin for robust operation.

The second zero (F_{Z2}) is observed around 13 kHz, providing the intended phase boost prior to crossover. The gain and phase characteristics confirm that the placement of poles and zeros, along with the selected ripple injection components ($C_{INJ} = 15 \text{ nF}$, $R_{INJ} = 200 \text{ k}\Omega$, $C_{FF} = 560 \text{ pF}$), successfully shape the loop response as predicted by the analytical design. This validates the effectiveness of the frequency-domain design approach in achieving the desired loop stability.

The transient performance of the converter is evaluated using a load step from 2.5 A to 5 A with a fast transition time. The measured output voltage waveform shows an undershoot of approximately 120 mV, followed by a recovery within about 13.4 μs , and a settling time of approximately 30 μs .

The ripple waveform at the feedback node remains well-defined, confirming proper ripple injection and stable comparator operation during dynamic conditions. These results demonstrate that the designed control loop not only meets stability requirements but also delivers fast transient response, highlighting the trade-off achieved between crossover frequency, phase margin, and ripple amplitude. Overall, the measured performance aligns well with the design expectations, confirming the validity of the analytical and frequency-domain design methodology.

3. Design Example (Simplified Approach)

3.1. Design Steps

1. **Select C_{FF} :** In the simplified approach, the DC blocking capacitor C_{INJ} is first selected as a standard practical value that satisfies most operating conditions. For this design example: $C_{INJ} = 100 \text{ nF}$.
2. **Select C_{FF} :** Next, the feed-forward capacitor C_{FF} is selected in the typical range of 1 nF to 10 nF. This value generally provides adequate ripple integration and helps maintain proper loop behavior. For this example: $C_{FF} = 4.7 \text{ nF}$.
3. **Select ΔV_{FB} :** The feedback ripple amplitude is chosen within the recommended range of 40 mV to 200 mV, unless otherwise specified in the datasheet. Here, a practical target is selected: $\Delta V_{FB} = 100 \text{ mV}$.
4. **Calculate R_{INJ} :** Using the selected values of C_{FF} and ΔV_{FB} , the ripple injection resistor is calculated using:

Equation 3-1.

$$R_{INJ} = \frac{V_O \cdot (1 - D)}{\Delta V_{FB} \cdot C_{FF} \cdot F_{SW}}$$

For this design: $R_{INJ} = 36 \text{ k}\Omega$

5. **Calculate F_C :** The crossover frequency is then estimated using:

Equation 3-2.

$$F_C = \frac{V_O \cdot (1 - D)}{2\pi LC \Delta V_{FB} F_{SW}}$$

The calculated crossover frequency is: $F_C = 26 \text{ kHz}$.

6. **Select R_1 and Calculate R_2 :** R_1 is typically selected in the $\text{k}\Omega$ range to minimize the feedback divider current while maintaining good noise immunity. If R_1 is too large, it may allow noise to be introduced into the voltage feedback loop. If R_1 is too small, it will decrease the efficiency of the power supply, especially at light loads. Once R_1 is selected, R_2 can be calculated using equation . So, considering $R_1 = 10\text{k}$, the result is $R_2 = 1.36\text{k}$ for $V_{OUT} = 5\text{V}$.
7. **Verify Stability Criteria:** Finally, the selected components are checked against the required stability criteria. First, the impedance of C_{FF} at the switching frequency must be much lower than $R_1 \parallel R_2$:

$$\frac{1}{2\pi C_{FF} F_{SW}} < R_1 \parallel R_2$$

$$129\Omega \ll 1.15\text{k}\Omega$$

Next, the time-constant criterion must be satisfied. The ripple injection time constants should be significantly greater than the total switching period to ensure that the injected feedback ripple remains approximately linear over each switching cycle.

$$R_{INJ} C_{INJ} > R_1 C_{FF} > T_{SW}$$

$$3.6 \text{ ms} > 47 \mu\text{s} > 3.8 \mu\text{s}$$

Finally, the crossover frequency must remain below one-fifth of the switching frequency:

$$F_C < \frac{F_{SW}}{5}$$

$$26 \text{ kHz} < 53 \text{ kHz}$$

Since all three conditions are satisfied, the simplified ACOT control-loop design is complete. This approach provides a quick and practical method for selecting ripple injection components, while still ensuring that the loop meets the basic stability requirements.

3.2. Bench Test Results

Figure 2-2 shows the implemented test schematics along with the selected ripple injection component values and feedback resistors. The simplified design approach is validated through frequency-domain and transient measurements, as shown in Figure 2-3.

Figure 3-1. MIC28515 Schematic Used for Bench Testing After Populating the Component Values Obtained From the Design Example

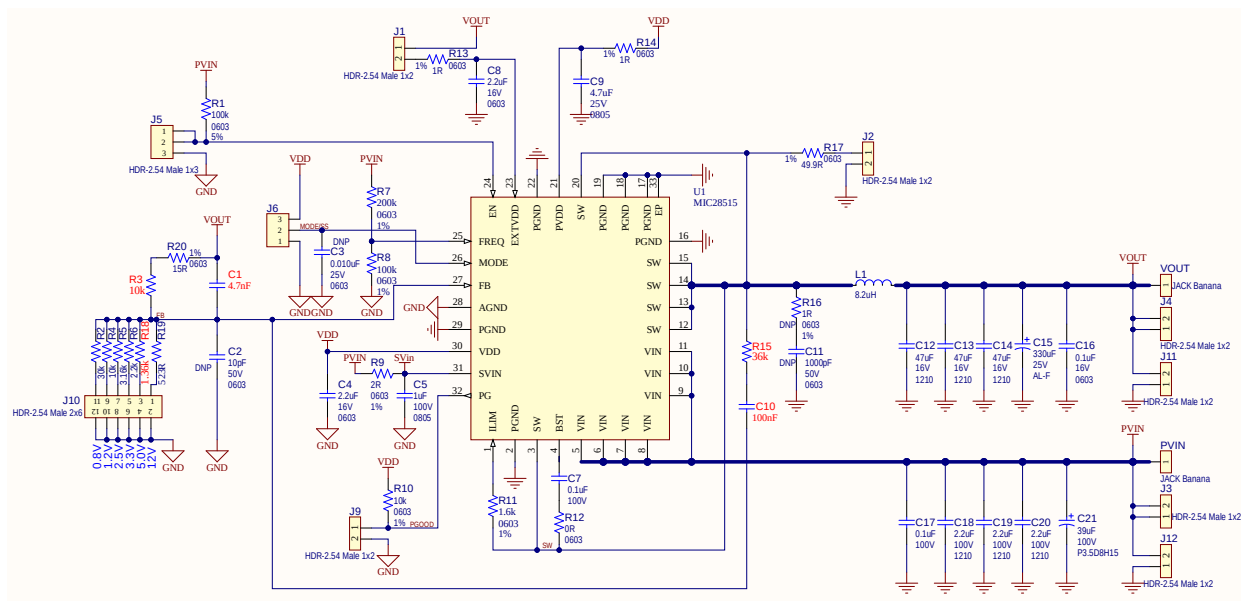
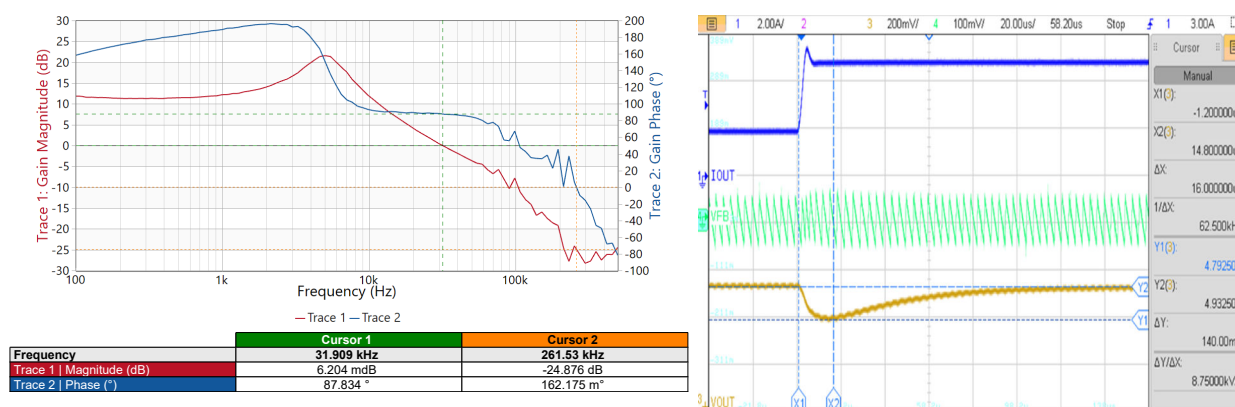


Figure 3-2. AC Analysis and Transient Response



Ripple Injection Components	ΔV_{FB}	F_C	Phase Margin	Undershoot	Response Time	Settling Time
$C_{INJ} = 100 \text{ nF}$, $R_{INJ} = 36 \text{ k}$, $C_{FF} = 4.7 \text{ nF}$	108 mV	31 kHz	87°	140 mV	16 us	80 us

The Bode plot indicates a crossover frequency of approximately 31 kHz, which is slightly higher than the earlier frequency-domain design, and a phase margin of about 87°, indicating a highly stable and well-damped control loop. The higher phase margin is a direct result of the larger C_{FF} value used in this approach, which shifts the second zero to a lower frequency and provides stronger

phase boost around the crossover region. The measured feedback ripple ΔV_{FB} is approximately 108 mV, which falls within the recommended design range and confirms proper ripple injection.

The transient response further validates the design, with a load step from 2.5A to 5A showing an undershoot of approximately 140 mV, a response time of around 16 μ s, and a settling time of about 80 μ s. Compared to the optimized frequency-domain design, the transient response is slightly slower, which is expected due to the higher phase margin. This demonstrates the inherent trade-off in control loop design: while the simplified approach provides robust stability and ease of implementation, it may result in reduced transient speed. Overall, the results confirm that the simplified method offers a practical and reliable starting point for ACOT control loop design, especially when rapid design iteration is required.

4. Comparison of Design Examples

Figure 4-1 and Table 4-1 present the ripple injection component values, pole-zero locations, and measured loop performance obtained using both the detailed frequency-domain analysis method and the simplified design approach. These examples demonstrate how each design methodology influences the resulting crossover frequency, phase margin, and overall control-loop behavior of the ACOT™ converter.

Figure 4-1. Ripple Injection Components Designed by AC Analysis Method and Simplified Approach Respectively

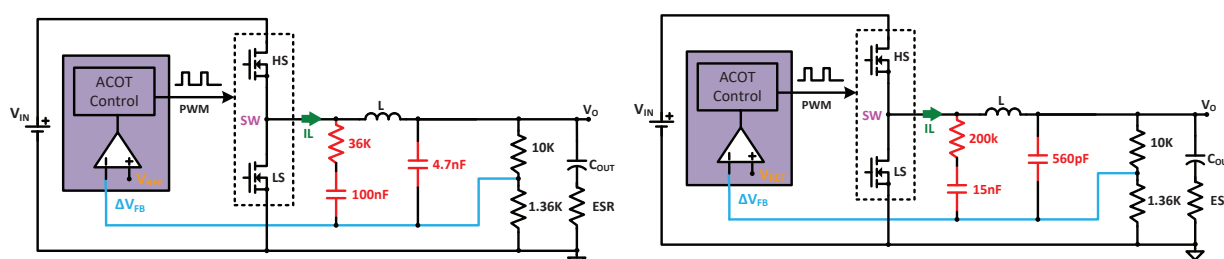


Table 4-1. Comparison of Design Examples Using Frequency Domain Analysis and Simplified Approach

Parameter	Frequency Domain Analysis	Simplified Approach
F_{Z1} (Zero by R_{INJ} and C_{INJ})	0.053 kHz	0.044 kHz
F_{LC}	5 kHz	5 kHz
F_{Z2} (Zero by R1 and C_{FF})	13 kHz	3.3 kHz
Crossover Frequency	25 kHz	31 kHz
Phase Margin	68°	80° or above
Stability Optimization	High control over stability and transient response	Naturally stable with high phase margin
Key Observation	Enables accurate tuning of crossover frequency and phase margin	Simplified method still satisfies most practical stability requirements

The comparison above highlights the difference between the detailed frequency-domain design approach and the simplified ripple-based design approach for ACOT™ control implementation. In the frequency-domain analysis method, the ripple injection network is intentionally designed by positioning the poles and zeros to achieve a targeted crossover frequency and a controlled phase margin. This provides better predictability and tighter optimization of transient response, stability, and loop bandwidth. In this example, the design achieves a crossover frequency of approximately 25 kHz with a well-controlled phase margin of 68°.

In contrast, the simplified approach selects the ripple injection components mainly based on practical ripple generation requirements and approximate design relationships, without performing a full AC loop analysis. Even though the resulting pole-zero locations and crossover frequency differ, the converter still achieves stable operation with a very high phase margin (> 80°). This demonstrates that the simplified approach is often sufficient for many practical applications and significantly reduces design complexity. However, when precise optimization of dynamic performance, bandwidth, or phase margin is required, the frequency-domain analysis approach provides much greater control and design accuracy.

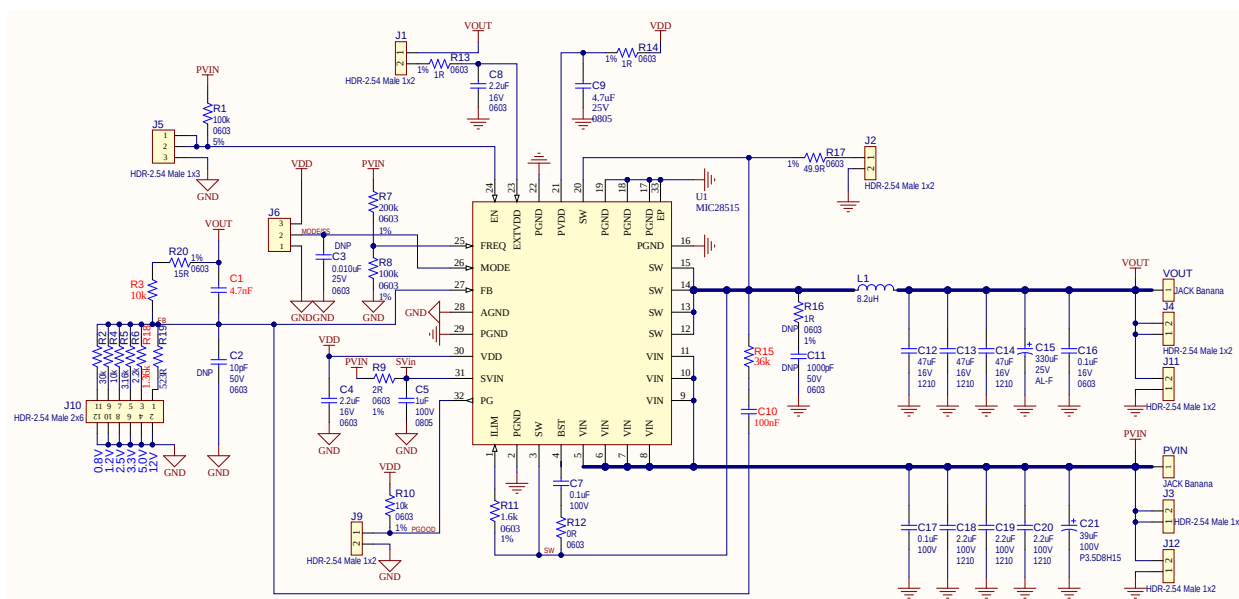
5. Feedback Ripple vs. Transient Response

Now, let us examine some design examples to validate the preceding analyses and explanations. This analysis aims to comprehend the transient response performance concerning variations in feedback ripple amplitude (ΔV_{FB}) so that we can optimize the ripple injection components for the desired transient performance.

Figure 5-1 illustrates the schematic diagram of an MIC28515 buck converter design with $V_{IN} = 48V$, $V_{OUT} = 5V$, $F_{SW} = 266$ kHz. Analysis will be performed with a transient load from 2.5A to 5A with a slew rate of 2.5A/3 μs . The details of the evaluation board used for testing can be found in the MIC28515 Evaluation Board user guide.

In the reference schematic (Figure 5-1), the ripple injection components employed are $R_{INJ} = 16.2k$, $C_{INJ} = 0.1$ μF and $C_{FF} = 4.7$ nF. Utilizing Equation 3-1, we can compute ΔV_{FB} . The calculated value is 220 mV, which closely aligns with the test result (slight variations in the duty cycle compensate for losses, leading to slight deviations in the calculated value). Figure 5-2 depicts the transient response performance associated with Figure 5-1 reference schematic, and Figure 5-3 through Figure 5-5 show the transient performance across different ΔV_{FB} amplitudes achieved by adjusting the ripple injection components.

Figure 5-1. MIC28515 Design Setup for Load Transient Test



ZB and ZF are calculated for the given switching frequency of 266 kHz, and their ratio is given in Table 5-1 to correlate its connection to the transient performance of converter. It is worth noting that the increase in impedance ratio reduces the feedback ripple which results in better transient response. However, Figure 5-6 illustrates that too high value of ZB/ZF results in too low value of ΔV_{FB} , which in turn can cause abnormal switching and lead to instability.

5.1. Feedback Ripple vs. Transient Response for Transient Step 2.5 to 5A (Slew Rate = 2.5A/3 μ s)

Figure 5-2. $R_{INJ} = 16.2k$, $C_{FF} = 4.7$ nF, $\Delta V_{FB} = 245$ mV, V_O Undershoot = 240 mV, Recovery Time = 70 μ s

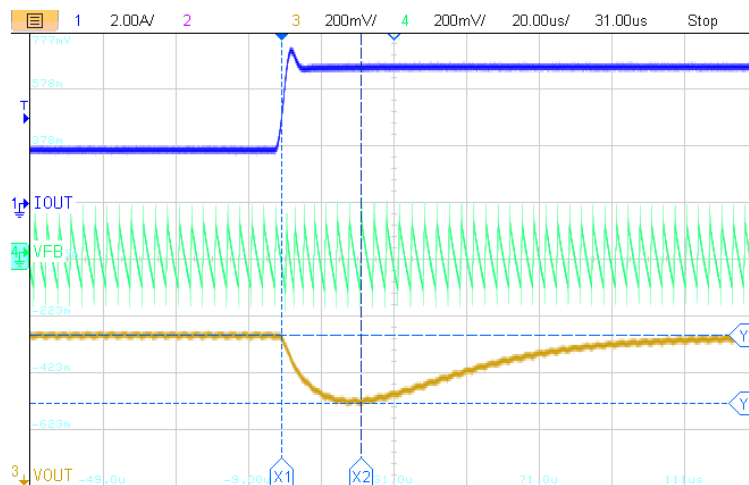


Figure 5-3. $R_{INJ} = 36k$, $C_{FF} = 4.7$ nF, $\Delta V_{FB} = 108$ mV, V_O Undershoot = 140 mV, Recovery Time = 40 μ s

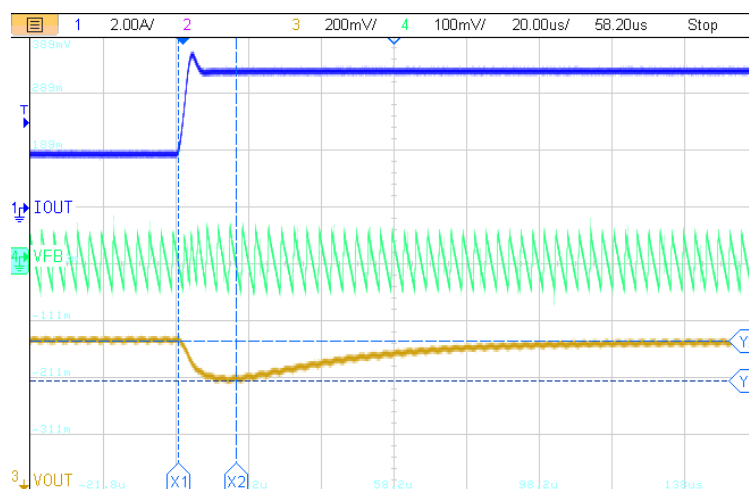


Figure 5-4. $R_{INJ} = 68k$, $C_{FF} = 4.7\text{ nF}$, $\Delta V_{FB} = 55\text{ mV}$, V_O Undershoot = 100 mV, Recovery Time = 25 μs

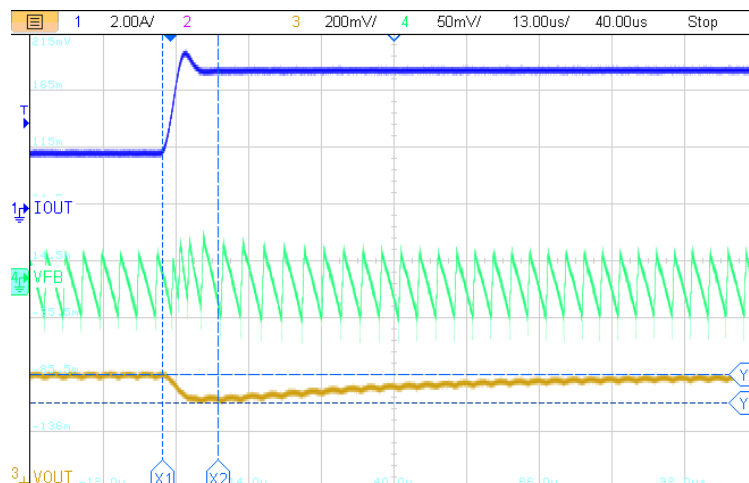


Figure 5-5. $R_{INJ} = 82k$, $C_{FF} = 4.7\text{ nF}$, $\Delta V_{FB} = 45\text{ mV}$, V_O Undershoot = 75 mV, Recovery Time = 20 μs

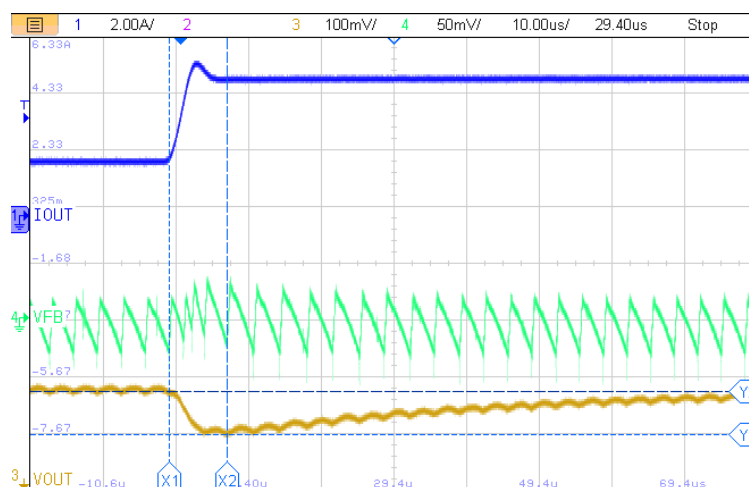


Figure 5-6. $R_{INJ} = 150k$, $C_{FF} = 4.7\text{ nF}$, $\Delta V_{FB} = 15\text{ mV}$, Abnormal Switching and Abnormal Feedback Waveform due to Very Low Ripple at Feedback

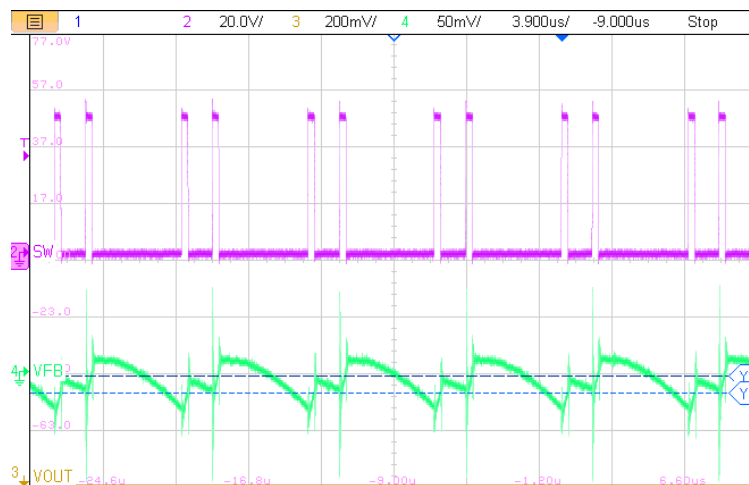


Table 5-1. Impact of Ripple Injection Optimization on Load Transient Performance

Figure #	Ripple Injection Components	ZB/ZF Ratio	ΔV_{FB} (mV)	V_{OUT} Undershoot (mV)	Recovery Time (μ s)
Figure 5-2	$R_{INJ} = 16.2k$, $C_{INJ} = 0.1 \mu F$, $C_{FF} = 4.7 nF$	129	245	240	70
Figure 5-3	$R_{INJ} = 36k$, $C_{INJ} = 0.1 \mu F$, $C_{FF} = 4.7 nF$	286	108	140	40
Figure 5-4	$R_{INJ} = 68k$, $C_{INJ} = 0.1 \mu F$, $C_{FF} = 4.7 nF$	541	55	100	25
Figure 5-5	$R_{INJ} = 82k$, $C_{INJ} = 0.1 \mu F$, $C_{FF} = 4.7 nF$	652	45	75	20

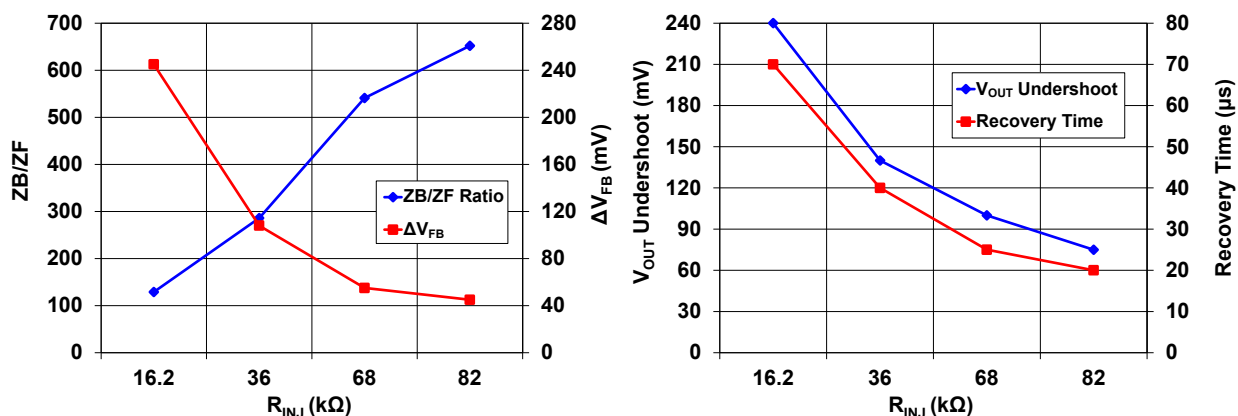
Figure 5-7. Graphical Representation of R_{INJ} vs. ΔV_{FB} and ΔV_{FB} vs. V_{OUT} Recovery Time During Transient

Table 5-1 and Figure 5-7 provide a comprehensive summary of how optimizing ripple injection can significantly impact transient performance in ACOT-based converters. Despite ACOT's renowned superiority in transient response compared to its counterparts, there is always room for further optimization and improvement.

As discussed earlier and derived in Equation 1-5, the loop gain of ACOT is heavily influenced by the injection RC impedance (ZB) and the impedance of the feed-forward network (ZF). Hence, the ratio of ZB/ZF plays a crucial role in designing the ripple injection circuit for achieving the best transient response. Because ACOT is a nonlinear ripple-based control method, Bode plot measurements must be interpreted carefully and should not be used as the only validation method. Frequency-domain measurements are useful for understanding loop bandwidth and phase behavior, but final stability validation should always include time-domain tests such as load transient response, feedback ripple observation, and switching behavior.

➔ Important: Design Warning: As illustrated in Figure 5-6, increasing R_{INJ} increases the ZB/ZF ratio and reduces the feedback ripple ΔV_{FB} , which can improve transient response. However, reducing ΔV_{FB} too much can make the FB comparator more sensitive to noise, jitter, and layout parasitics, potentially causing irregular switching or instability. Therefore, R_{INJ} should not be increased blindly; the selected value must maintain sufficient ΔV_{FB} according to the device data sheet and should be verified through bench testing.

6. Summary

In ACOT control, the control loop behavior is fundamentally governed by the ripple injection network rather than by a conventional compensation scheme. The loop gain can be effectively understood in the frequency domain by expressing it in terms of impedance ratios, which enables identification of dominant poles and zeros.

While a simplified design approach works effectively for most practical implementations, it relies on typical assumptions and empirical selection of component values. This approach is suitable for quick design and generally ensures stable operation. However, when precise control over performance parameters such as crossover frequency, phase margin, and transient response is required, a deeper understanding of frequency-domain analysis becomes essential. The frequency-domain approach enables designers to intentionally shape the loop response by accurately positioning poles and zeros, rather than relying on approximate starting points.

The simplified method is not a replacement for frequency-domain design when exact bandwidth or phase margin is required. However, because ACOT stability is strongly tied to proper feedback ripple generation, the simplified approach usually satisfies the major practical stability requirements and provides a fast starting point for bench optimization.

An important advantage of ACOT control is that ripple injection component selection based on time-domain considerations inherently satisfies most of the stability requirements observed in frequency-domain analysis. As a result, compared with conventional control schemes that require explicit compensation design, ACOT offers a more intuitive and simpler implementation, where stability can often be achieved with minimal iteration.

Ultimately, ACOT control loop design is a process of ripple engineering, where the selection of ripple injection components directly determines stability and dynamic performance. By understanding the relationships between ripple amplitude, pole-zero placement, and loop gain, designers can systematically achieve both robust stability and optimized transient performance.

7. Appendix 1: Derivation of ACOT Loop Gain

There are two components contributing to the overall feedback: V_{FB1} and V_{FB2} . V_{FB1} occurs when V_{SW} is high (almost equal to V_{IN}), while V_{FB2} contributes when V_{SW} is essentially grounded.

So,

Equation 7-1.

$$V_{FB} = V_{FB1} + V_{FB2}$$

Referring to [Figure 1-1](#), V_{FB1} and V_{FB2} can be expressed as:

Equation 7-2.

$$V_{FB1} = V_{SW} \cdot \frac{R2 \parallel ZF}{ZB + R2 \parallel ZF} = V_{SW} \cdot \frac{R2 \cdot ZF}{(ZB + ZF) \cdot R2 + (ZB \cdot ZF)}$$

Equation 7-3.

$$V_{FB2} = V_O \cdot \frac{R2 \parallel ZB}{ZF + R2 \parallel ZB} = V_O \cdot \frac{R2 \cdot ZB}{(ZB + ZF) \cdot R2 + (ZB \cdot ZF)}$$

And from [Figure 1-1](#), V_{SW} can be expressed as:

Equation 7-4.

$$V_{SW} = -AV \cdot V_{FB}$$

Using [Equation 7-2](#), [Equation 7-3](#) and [Equation 7-4](#), V_{FB} can be expressed as:

Equation 7-5.

$$V_{FB} = V_{FB1} + V_{FB2} = \left[(-AV \cdot V_{FB}) \cdot \frac{R2 \cdot ZF}{(ZB + ZF) \cdot R2 + (ZB \cdot ZF)} \right] + \left(V_O \cdot \frac{R2 \cdot ZB}{(ZB + ZF) \cdot R2 + (ZB \cdot ZF)} \right)$$

Rearranging [Equation 7-5](#), we can obtain V_{FB}/V_O as in below:

Equation 7-6.

$$\frac{V_{FB}}{V_O} = \frac{1}{1 + \frac{ZF}{R2} + \left(1 + AV\right) \cdot \frac{ZF}{ZB}}$$

Now placing [Equation 7-6](#) in loop gain expression ([Equation 1-4](#)), we obtain:

Equation 7-7.

$$G = \frac{-1}{\left(1 + \frac{ZF}{R2} + \frac{ZF}{ZB}\right) \cdot \frac{1}{AV} + \frac{ZF}{ZB}} \cdot \frac{ZC \parallel ZLOAD}{ZC \parallel ZLOAD + ZL}$$

By design and from test results, it is known that A_v acts as a high gain amplifier at low frequencies. With this practical assumption ($\frac{1}{A_v}$ is almost equal to zero), we could rewrite the expression for Loop Gain (G) as:

Equation 7-8.

$$G \cong -\frac{Z_B}{Z_F} \cdot \frac{Z_C \parallel Z_{LOAD}}{Z_C \parallel Z_{LOAD} + Z_L}$$

8. Appendix 2: Step-by-Step Derivation of ACOT Loop Gain in S-Domain

The small-signal loop gain of the ACOT control loop can be written as:

Equation 8-1.

$$G \cong -\frac{Z_B}{Z_F} \cdot \frac{Z_C \parallel Z_{LOAD}}{Z_C \parallel Z_{LOAD} + Z_L}$$

Where:

- Z_B = ripple injection path impedance
- Z_F = feedback path impedance
- Z_C = output capacitor impedance
- Z_{LOAD} = load impedance
- Z_L = output inductor impedance

The ripple injection path consists of R_{INJ} in series with C_{INJ} . Therefore:

Equation 8-2.

$$Z_B = R_{INJ} + \frac{1}{sC_{INJ}}$$

Rearranging:

Equation 8-3.

$$Z_B = \frac{1 + sR_{INJ}C_{INJ}}{sC_{INJ}}$$

The feedback path impedance is formed by $R1$ in parallel with C_{FF} . Therefore:

Equation 8-4.

$$Z_F = R1 \parallel \frac{1}{sC_{FF}}$$

$$Z_F = \frac{R1 \cdot \frac{1}{sC_{FF}}}{R1 + \frac{1}{sC_{FF}}}$$

Simplifying:

Equation 8-5.

$$Z_F = \frac{R1}{1 + sR1C_{FF}}$$

Substituting Z_B and Z_F :

Equation 8-6.

$$\frac{Z_B}{Z_F} = \frac{\frac{1 + sR_{INJ}C_{INJ}}{sC_{INJ}}}{\frac{R1}{1 + sR1C_{FF}}}$$

Therefore:

Equation 8-7.

$$\frac{Z_B}{Z_F} = \frac{(1 + sR_{INJ}C_{INJ})(1 + sR_1C_{FF})}{sC_{INJ}R_1}$$

The output capacitor impedance is:

Equation 8-8.

$$Z_C = \frac{1}{sC_{OUT}}$$

The load impedance is:

Equation 8-9.

$$Z_{LOAD} = R_{LOAD}$$

Therefore:

Equation 8-10.

$$Z_C \parallel Z_{LOAD} = \frac{\frac{1}{sC_{OUT}} \cdot R_{LOAD}}{\frac{1}{sC_{OUT}} + R_{LOAD}}$$

Simplifying:

Equation 8-11.

$$Z_C \parallel Z_{LOAD} = \frac{R_{LOAD}}{1 + sR_{LOAD}C_{OUT}}$$

The output inductor impedance is:

Equation 8-12.

$$Z_L = sL$$

The output stage gain is:

Equation 8-13.

$$\frac{Z_C \parallel Z_{LOAD}}{Z_C \parallel Z_{LOAD} + Z_L}$$

Substituting the impedance expressions:

Equation 8-14.

$$\frac{Z_C \parallel Z_{LOAD}}{Z_C \parallel Z_{LOAD} + Z_L} = \frac{\frac{R_{LOAD}}{1 + sR_{LOAD}C_{OUT}}}{\frac{R_{LOAD}}{1 + sR_{LOAD}C_{OUT}} + sL}$$

Multiplying numerator and denominator by $(1 + sR_{LOAD}C_{OUT})$:

Equation 8-15.

$$= \frac{R_{LOAD}}{R_{LOAD} + sL(1 + sR_{LOAD}C_{OUT})}$$

Expanding:

Equation 8-16.

$$= \frac{R_{LOAD}}{R_{LOAD} + sL + s^2LR_{LOAD}C_{OUT}}$$

Dividing numerator and denominator by R_{LOAD} :

Equation 8-17.

$$= \frac{1}{1 + \frac{sL}{R_{LOAD}} + s^2LC_{OUT}}$$

Starting from:

Equation 8-18.

$$G \cong -\frac{Z_B}{Z_F} \cdot \frac{Z_C \parallel Z_{LOAD}}{Z_C \parallel Z_{LOAD} + Z_L}$$

Substituting the derived expressions:

Equation 8-19.

$$G(s) \cong -\frac{(1 + sR_{INJ}C_{INJ})(1 + sR_1C_{FF})}{sC_{INJ}R_1} \cdot \frac{1}{1 + \frac{sL}{R_{LOAD}} + s^2LC_{OUT}}$$

Therefore, the ACOT loop gain is:

Equation 8-20.

$$G(s) = -\frac{(1 + sR_{INJ}C_{INJ})(1 + sR_1C_{FF})}{sC_{INJ}R_1\left(1 + \frac{sL}{R_{LOAD}} + s^2LC_{OUT}\right)}$$

The negative sign indicates the feedback polarity of the control loop. For gain magnitude analysis, the loop gain magnitude is commonly considered as:

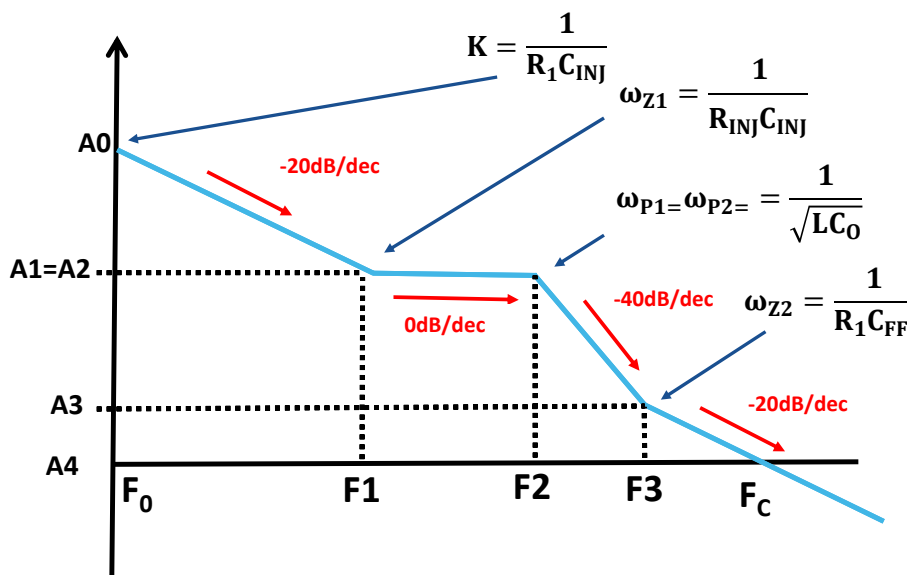
Equation 8-21.

$$|G(s)| = \frac{(1 + sR_{INJ}C_{INJ})(1 + sR_1C_{FF})}{sC_{INJ}R_1\left(1 + \frac{sL}{R_{LOAD}} + s^2LC_{OUT}\right)}$$

9. Appendix 3: Derivation of Crossover Frequency

In the [Poles and Zeros](#) section, we established the analytical expressions and locations of all dominant poles and zeros in the system—namely the injection zero, LC double pole, and high-frequency zero. Building on that understanding, we now move to derive the crossover frequency F_c using a logarithmic (Bode plot) approach, by tracking how the gain evolves across frequency.

Figure 9-1. Derivation of Crossover Frequency



We start from the low-frequency gain A_0 , which comes from the DC loop gain:

Equation 9-1.

$$A_0 = 20\log_{10}\left(\frac{1}{R_1C_{INJ}}\right)$$

From here, we move across frequency step-by-step, following the slopes introduced by poles and zeros:

From F_0 to F_1 :

A single pole dominates and the slope becomes -20 dB/dec

At F_1 , a zero is introduced:

Equation 9-2.

$$F_1 = \frac{1}{2\pi R_{INJ}C_{INJ}}:$$

A zero is introduced by the ripple injection network, cancelling the earlier pole and the slope becomes 0 dB/dec

At F_2 , LC double pole is introduced:

Equation 9-3.

$$F_2 = \frac{1}{2\pi\sqrt{LC_{OUT}}}$$

The LC double pole appears and the slope becomes -40 dB/dec

At F_3 , a zero is introduced:

Equation 9-4.

$$F_3 = \frac{1}{2\pi R1 C_{FF}}:$$

This high-frequency zero reduces slope to -20 dB/dec

Using the standard logarithmic gain relation:

Equation 9-5.

$$\text{Gain}_2 = \text{Gain}_1 + (\text{slope}) \cdot \log\left(\frac{F_2}{F_1}\right)$$

Now we translate the slope behavior into exact gain equations:

From A_0 to A_1 :

Equation 9-6.

$$A_1 = A_0 - 20\log_{10}\left(\frac{F_1}{F_0}\right) = 20\log_{10}\left(\frac{R_{INJ}}{R1^2 C_{INJ}}\right)$$

From A_1 to A_2 : Flat region (0 dB/dec), so:

Equation 9-7.

$$A_2 = A_1$$

From A_2 to A_3 :

Equation 9-8.

$$A_3 = A_2 - 40\log_{10}\left(\frac{F_3}{F_2}\right)$$

From A_3 to crossover F_C : At crossover, gain = 0 dB:

Equation 9-9.

$$0 = A_3 - 20\log_{10}\left(\frac{F_C}{F_3}\right)$$

This equation becomes the key to solving for F_C .

We now substitute all expressions back and solve them systematically:

Starting from:

Equation 9-10.

$$0 = 20\log_{10}\left(\frac{R_{INJ}}{R1^2 C_{INJ}}\right) - 40\log_{10}\left(\frac{F_3}{F_2}\right) - 20\log_{10}\left(\frac{F_C}{F_3}\right)$$

Rearranging:

Equation 9-11.

$$\log_{10}(F_C) = \log_{10}(F_3) + \log_{10}\left(\frac{R_{INJ}}{R1^2 C_{INJ}}\right) - 2\log_{10}\left(\frac{F_3}{F_2}\right)$$

Exponentiating:

Equation 9-12.

$$F_C = F_3 \cdot \left(\frac{R_{INJ}}{R1^2 C_{INJ}}\right) \cdot \left(\frac{F_2}{F_3}\right)^2$$

Substituting the known pole-zero frequencies:

Equation 9-13.

$$F_2 = \frac{1}{2\pi\sqrt{LC_{OUT}}}, \quad F_3 = \frac{1}{2\pi R1 C_{FF}}$$

After simplification, we arrive at the final compact expression:

Equation 9-14.

$$F_C = \frac{R_{INJ} \cdot C_{FF}}{2\pi LC_{OUT}}$$

10. References

Source	Document Title	Literature Number	Available/Authors
IEEE Transactions on Power Electronics	"Ripple-Based Control of Switching Regulators - An Overview", Dec. 2009.	—	R. Redl, J. Sun
IEEE Transactions on Power Electronics	"Characterization and Performance Comparison of Ripple-Based Control for Voltage Regulator Modules", Mar. 2006.	—	J. Sun
IEEE Transactions on Industrial Electronics	"Analysis of Pulse Bursting Phenomenon in Constant-On-Time-Controlled Buck Converter", Dec. 2011.	—	Jinping Wang, Jianping Xu, Bocheng Bao
Microchip Technology Inc.	MIC28515 - 75V/5A Hyper Speed Control® Synchronous DC/DC Buck Regulator with External Mode Control	DS20005762	MIC28515 Data Sheet
Microchip Technology Inc.	AN7167 - Introduction to Microchip's Adaptive Constant-On-Time (ACOT™) Control and Ripple Injection Methods	DS00007176	Muhsin Vilangappurath

11. Revision History

Revision	Date	Section	Description
A	07/2026	—	Initial release of this document.

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- Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip products are strictly prohibited and may violate the Digital Millennium Copyright Act.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is “unbreakable”. Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.