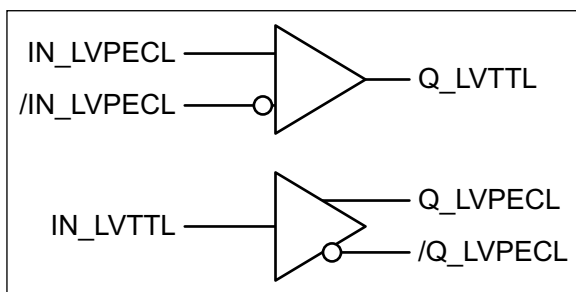


3.3V LVTTTL-to-Differential LVPECL and Differential LVPECL-to-LVTTTL Translator

Features

- 3.3V $\pm 10\%$ Power Supply
- Ensured AC Parameters over Temperature: $f_{MAX} > 275$ MHz (LVTTTL)
- < 2 ns LVPECL-to-LVTTTL Propagation Delay
- < 600 ps LVTTTL-to-LVPECL Propagation Delay
- Internal 75 k Ω Input Pull-Up and Pull-Down Resistors
- Industrial Temperature Range: -40°C to $+85^{\circ}\text{C}$
- Available in an Ultra-Small (2 mm x 2 mm) 8-Lead VDFN Package

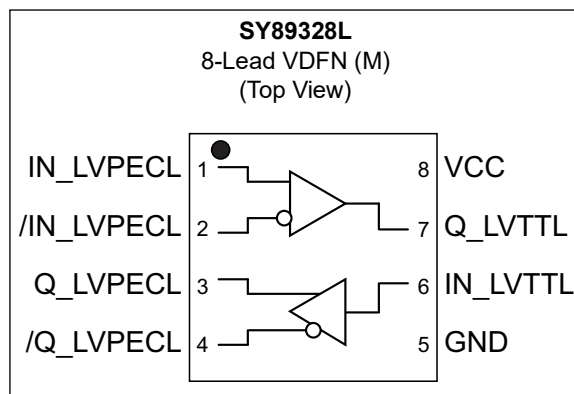
Block Diagram



General Description

The SY89328L is a differential LVPECL-to-LVTTTL translator and an LVTTTL-to-differential LVPECL translator in a single package. Because LVPECL (Positive ECL) levels are used, only +3.3V and ground are required. The SY89328L is functionally equivalent to the SY100EPT28L, but in an ultra-small 8-lead VDFN package that features a 70% smaller footprint. This ultra-small package and the dual translation design of the SY89328L make it ideal for applications that are sending and receiving signals across a backplane.

Package Type



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage (V_{CC})	–0.5V to +3.8V
Input Voltage (V_{IN})	–0.5V to V_{CC}
Source or Sink Current on IN, /IN	±50 mA
LVPECL Continuous Output Current (I_{OUT})	50 mA
LVPECL Surge Output Current (I_{OUT})	100 mA

Operating Ratings ‡

Supply Voltage (V_{CC})	+3.0V to +3.6V
-----------------------------	----------------

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

‡ **Notice:** The device is not guaranteed to function outside its operating ratings.

DC ELECTRICAL CHARACTERISTICS

Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Power Supply Voltage	V_{CC}	3.0	3.3	3.6	V	—
Power Supply Current	I_{CC}	—	22	40	mA	Maximum V_{CC} , no load

Note 1: The circuit is designed to meet the DC specifications shown in the table above after thermal equilibrium has been established.

LVPECL DC ELECTRICAL CHARACTERISTICS

$V_{CC} = +3.3V \pm 10\%$ and $V_{EE} = 0V$; $R_L = 50\Omega$ to $V_{CC} - 2V$; $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise noted. Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Output HIGH Voltage	V_{OH}	$V_{CC} - 1.145$	$V_{CC} - 1.020$	$V_{CC} - 0.895$	V	—
Output LOW Voltage	V_{OL}	$V_{CC} - 1.945$	$V_{CC} - 1.820$	$V_{CC} - 1.695$	V	—
Input HIGH Voltage	V_{IH}	$V_{CC} - 1.225$	—	$V_{CC} - 0.880$	V	—
Input LOW Voltage	V_{IL}	$V_{CC} - 1.945$	—	$V_{CC} - 1.625$	V	—
LVPECL Common Mode Range	V_{CMR}	1.2	—	V_{CC}	V	—
Input HIGH Current	I_{IH}	—	—	150	μA	$V_{IN} = 3.46V$
Input LOW Current	I_{IL}	0.5	—	—	μA	IN
		–300	—	—	μA	/IN

Note 1: The circuit is designed to meet the DC specifications shown in the table above after thermal equilibrium has been established.

LVTTTL DC ELECTRICAL CHARACTERISTICS

$V_{CC} = +3.3V \pm 10\%$; $C_L = 20 \text{ pF}$; $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, unless otherwise noted. [Note 1](#)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Output HIGH Voltage	V_{OH}	2.0	—	—	V	$I_{OH} = -3 \text{ mA}$
Output LOW Voltage	V_{OL}	—	—	0.5	V	$I_{OL} = 24 \text{ mA}$
Input HIGH Voltage	V_{IH}	2.0	—	—	V	—
Input LOW Voltage	V_{IL}	—	—	0.8	V	—
Input Clamp Voltage	V_{IK}	—	—	-1.2	V	$I_{IK} = -18 \text{ mA}$
Input HIGH Current	I_{IH}	—	—	20	μA	$V_{IN} = 2.7V$
		—	—	100	μA	$V_{IN} = V_{CC}$
Input LOW Current	I_{IL}	—	—	-0.2	μA	$V_{IN} = 0.5V$
LVTTTL Output Short-Circuit Current	$I_{OUT(SC)}$	-275	—	-80	mA	$V_{OUT} = 0V$

Note 1: The circuit is designed to meet the DC specifications shown in the table above after thermal equilibrium has been established.

AC ELECTRICAL CHARACTERISTICS

$V_{CC} = +3.3V \pm 10\%$; $C_L = 20 \text{ pF}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ unless otherwise noted.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Maximum Frequency	f_{MAX}	700	—	—	MHz	Note 2 , LVPECL
		275	300	—	MHz	Note 3 , LVTTTL
Propagation Delay	t_{PD}	1.5	—	2.5	ns	Note 3 , IN_LVPECL-to-Q_LVTTTL
		100	400	600	ps	Note 2 , IN_LVTTTL-to-Q_LVPECL
LVPECL Input Voltage Swing (Single-Ended)	V_{PP}	100	—	—	mV	Note 4
Duty Cycle	DC	45	50	55	%	—
Cycle-to-Cycle Jitter	t_{JITTER}	—	—	<1	ps_{RMS}	Note 5
Total Jitter		—	—	20	ps_{PP}	Note 6
LVPECL Output Rise/Fall Times (20% to 80%)	t_r/t_f	200	—	500	ps	At full output swing, Note 1
LVTTTL Output Rise/Fall Times (20% to 80%)		0.5	—	1.0	ns	At full output swing, Note 2

Note 1: The circuit is designed to meet the DC specifications shown in the table above after thermal equilibrium has been established.

2: $R_L = 50\Omega$ to $V_{CC} - 2V$.

3: $C_L = 20 \text{ pF}$.

4: $V_{PP(MIN)}$ is the minimum input swing for which AC parameters are ensured.

5: Cycle-to-cycle jitter definition: the variation of periods between adjacent cycles, $T_n - T_{n-1}$, where T is the time between rising edges of the output signal.

6: Total jitter definition: with an ideal clock input of frequency $\leq f_{MAX}$, no more than one output edge in 10^{12} output edge will deviate by more than the specified peak-to-peak jitter value.

TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Storage Temperature Range	T_S	-65	—	+150	°C	—
Lead Temperature	T_{LEAD}	—	—	+260	°C	Soldering, 20 sec.
Ambient Temperature Range	T_A	-40	—	+85	°C	—
Package Thermal Resistances (Note 1)						
Thermal Resistance, VDFN 8-Ld	θ_{JA}	—	93	—	°C/W	Still-Air
	θ_{JA}	—	87	—	°C/W	500 lfpm
	Ψ_{JB}	—	60	—	°C/W	Junction-to-board

Note 1: Package thermal resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential (GND) on the PCB.

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in [Table 2-1](#).

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Type	Description
1, 2	IN_LVPECL, /IN_LVPECL	100k ECL Input	Differential LVPECL Input: Includes internal 75 kΩ pull-down resistor or internal 75 kΩ pull-up and pull-down resistors on /IN. See the LVPECL Input Interface Applications section for single-ended inputs.
7	Q_LVTTL	LVTTL Output	Single-ended LVTTL Output: Translated from LVPECL input. Q_LVTTL output will default LOW with IN_LVPECL and /IN_LVPECL inputs left open.
6	IN_LVTTL	LVTTL Input	Single-ended LVTTL Input.
3, 4	Q_LVPECL, /Q_LVPECL	100k ECL Output	Differential LVPECL Output: Translated from LVTTL input. See the LVPECL Output Interface Applications section for recommendations on terminations.
8	VCC	VCC Power	Positive Power Supply: Bypass with 0.1 μF//0.01 μF low ESR capacitors.
5	GND, Exposed Pad	Ground	GND and exposed pad must be tied to ground plane.

LVPECL Input Interface Applications

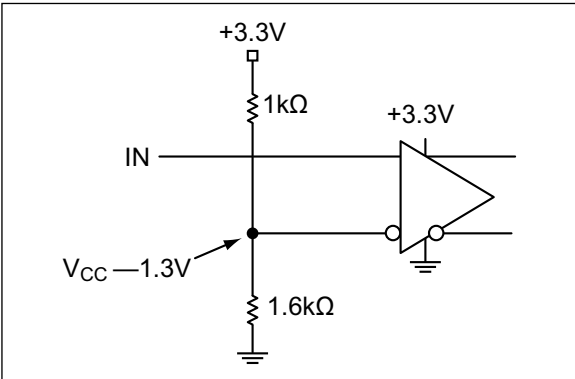


FIGURE 2-1: Single-Ended Input
(Terminating Unused Input).

LVPECL Output Interface Applications

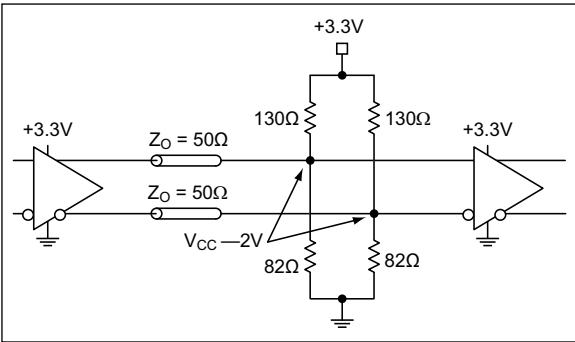


FIGURE 2-2: Parallel Thevenin-Equivalent Termination.

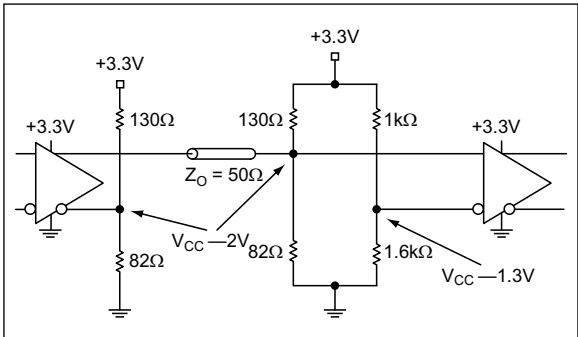


FIGURE 2-4: Terminating Unused I/O.

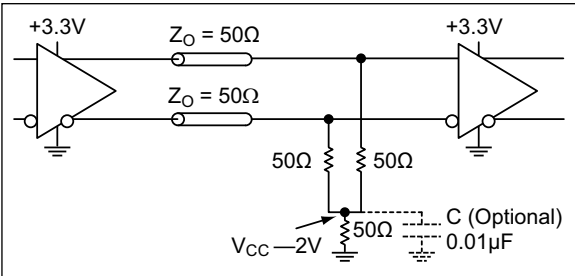
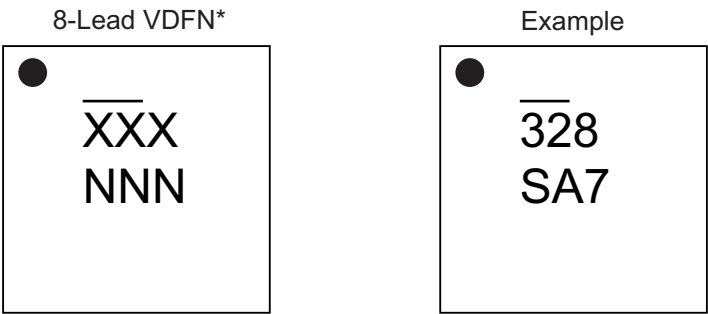


FIGURE 2-3: Three Resistor "Y-Termination".

3.0 PACKAGING INFORMATION

3.1 Package Marking Information



Legend:

XX...X

Y

YY

WW

NNN

(e3)

*

Product code or customer-specific information

Year code (last digit of calendar year)

Year code (last 2 digits of calendar year)

Week code (week of January 1 is week '01')

Alphanumeric traceability code

Pb-free JEDEC® designator for Matte Tin (Sn)

This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

•, ▲, ▼

Pin one index is identified by a dot, delta up, or delta down (triangle mark).

Note:

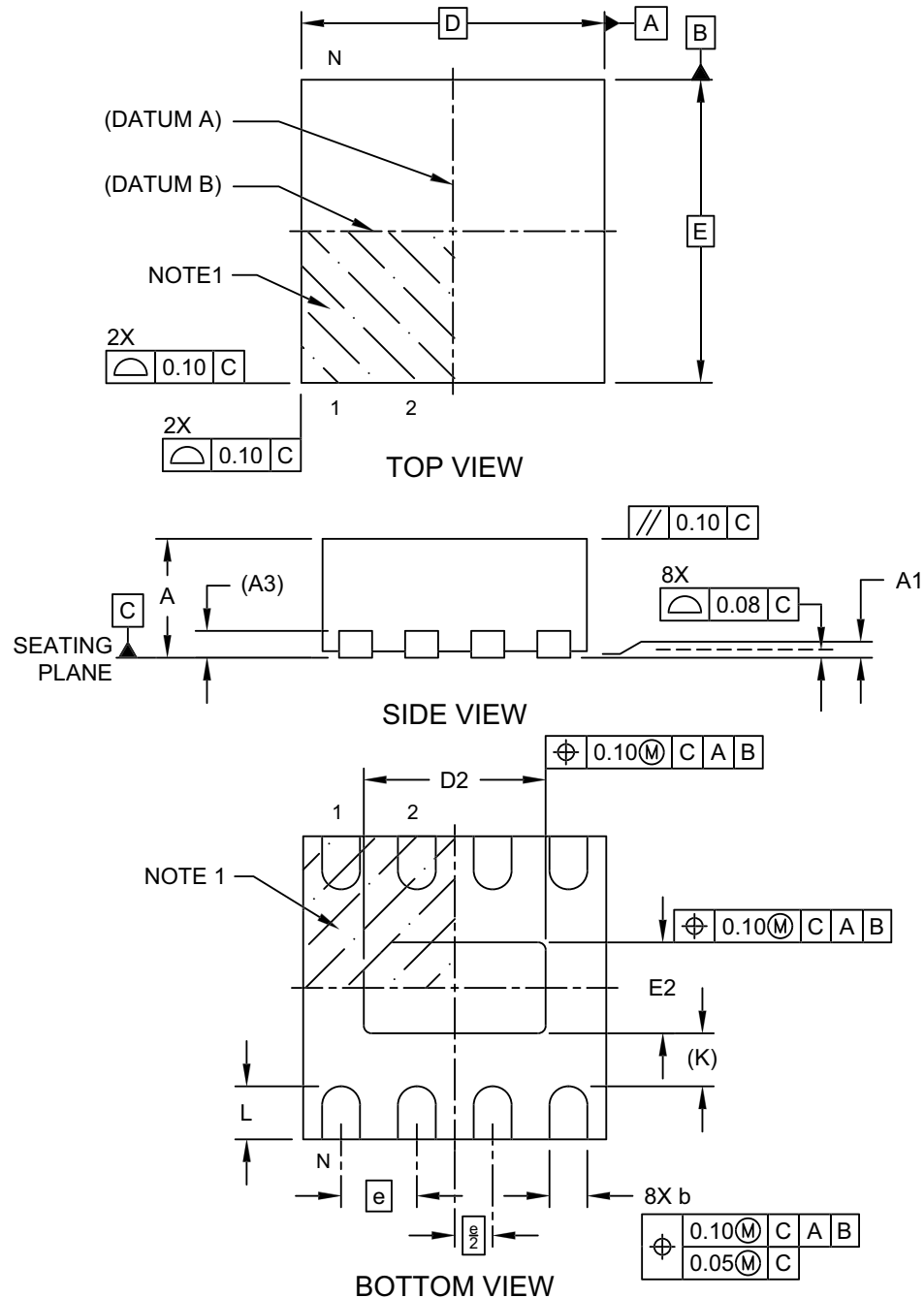
In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (¯) symbol may not be to scale.

Note: If the full seven-character YYWWNNN code cannot fit on the package, the following truncated codes are used based on the available marking space:
6 Characters = YYWWNNN; 5 Characters = WWNNN; 4 Characters = WNNN; 3 Characters = NNN;
2 Characters = NN; 1 Character = N

8-Lead Very Thin Plastic Dual Flat, No Lead Package (6XW) - 2x2x1.0 mm Body [VDFN] With 1.20x0.6 mm Exposed Pad

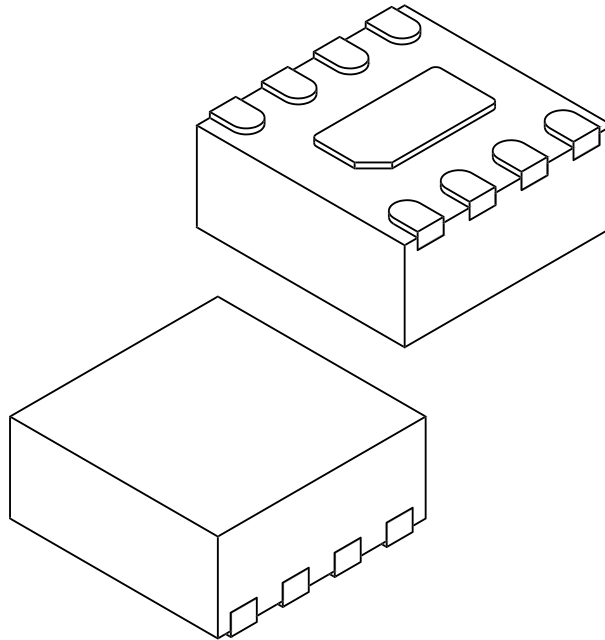
Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-00637 Rev B Sheet 1 of 2

**8-Lead Very Thin Plastic Dual Flat, No Lead Package (6XW) - 2x2x1.0 mm Body [VDFN]
With 1.20x0.6 mm Exposed Pad**

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N	8		
Pitch	e	0.50 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3	0.20 REF		
Overall Length	D	2.00 BSC		
Exposed Pad Length	D2	1.10	1.20	1.30
Overall Width	E	2.00 BSC		
Exposed Pad Width	E2	0.50	0.60	0.70
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.30	0.35	0.40
Terminal-to-Exposed-Pad	K	0.35 REF		

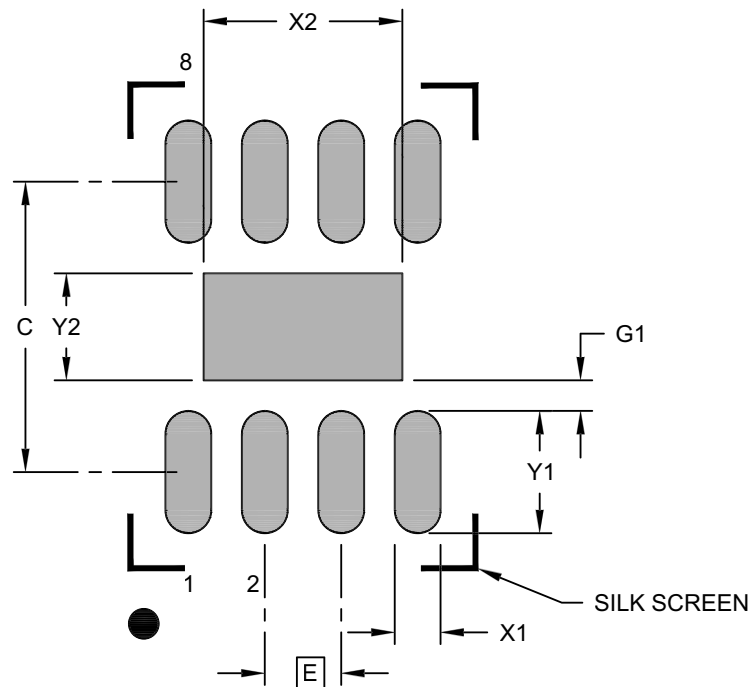
Notes:

- Pin 1 visual index feature may vary but must be located within the hatched area.
- Package is saw singulated.
- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-00637 Rev B Sheet 2 of 2

**8-Lead Very Thin Plastic Dual Flat, No Lead Package (6XW) - 2x2x1.0 mm Body
[VDFN] With 1.20x0.6 mm Exposed Pad**

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>


RECOMMENDED LAND PATTERN

Dimension	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Optional Center Pad Width	X2			1.30
Optional Center Pad Length	Y2			0.70
Contact Pad Spacing	C		1.90	
Contact Pad Width (X8)	X1			0.30
Contact Pad Length (X8)	Y1			0.80
Contact Pad to Center Pad (X8)	G1	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, please refer to current industry standard IPC-7093

Microchip Technology Drawing C04-02637 Rev. B

APPENDIX A: REVISION HISTORY

Revision A (April 2026)

- Converted Micrel document SY89328L to Microchip data sheet template DS20007038A.
- Minor text changes throughout.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

<u>Part No.</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>-XX</u>	Examples:
Device	Supply Voltage	Package	Temperature Range	Media Type	
Device:	SY89328:	3.3V Differential LVPECL/CML/LVDS-to-LVTTL Translator			a) SY89328LMG-TR: SY89328L, 3.3V Supply Voltage, 8-Lead VDFN, -40°C to +85°C Temperature Range, 1,000/Reel Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.
Supply Voltage:	L	=	3.3V		
Package:	M	=	8-Lead 2 mm x 2 mm VDFN		
Temperature Range:	G	=	-40°C to +85°C		
Media Type:	TR	=	1,000/Reel		

NOTES:

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ISBN: 979-8-3371-3123-8

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