

GENERAL DESCRIPTION

The 0912GN-1000V is an internally matched, COMMON SOURCE, class AB, GaN on SiC HEMT transistor capable of providing over 19.5 dB gain, 1000 Watts of pulsed RF output power at 128us, 10% duty cycle pulse format across the 960 to 1215 MHz band and can also transmit Mode-S ELM pulse format. The transistor has internal pre-match for optimal performance, and the wide bandwidth enables Tri-Band Avionics applications. It utilizes gold metallization and eutectic attach to provide highest reliability and superior ruggedness.

ABSOLUTE MAXIMUM RATINGS

Maximum Power Dissipation

Device Dissipation @ 25°C 2400W

Maximum Voltage and Current

Drain-Source Voltage (V_{DS}) 150 V

Gate-Source Voltage (V_{GS}) -8 to +0 V

Maximum Temperatures

Storage Temperature (T_{STG}) -55 to +125° C

Operating Junction Temperature +200° C

CASE OUTLINES

Common Source
55-Q03

HIGH RF POWER SOLUTION
FOR DME, TACAN, MIDS, SSR...



ELECTRICAL CHARACTERISTICS @ 25°C

Symbol	Characteristics	Test Conditions	Min	Typ	Max	Units
P_{IN}	Input Power	$P_{OUT}=1000W$, Freq=960,1215 MHz		12.5	16	W
G_P	Power Gain	$P_{in}=12.5W$	18.5	19.5		dB
η_D	Drain Efficiency	$P_{in}=12.5W$		63		%
Dr	Droop	$P_{in}=12.5W$			0.3	dB
VSWR-T	Load Mismatch Tolerance	$P_{OUT}=1000W$, Freq= 1090MHz			3:1	
Θ_{JC}	Thermal Resistance	128us, 10% duty cycle			0.28	°C/W

- Bias Condition : $V_{dd}=+50V$, $I_{dq}=150mA$ average current ($V_{gs}= -2.0 \sim -4.5V$ typical)

FUNCTIONAL CHARACTERISTICS @ 25°C

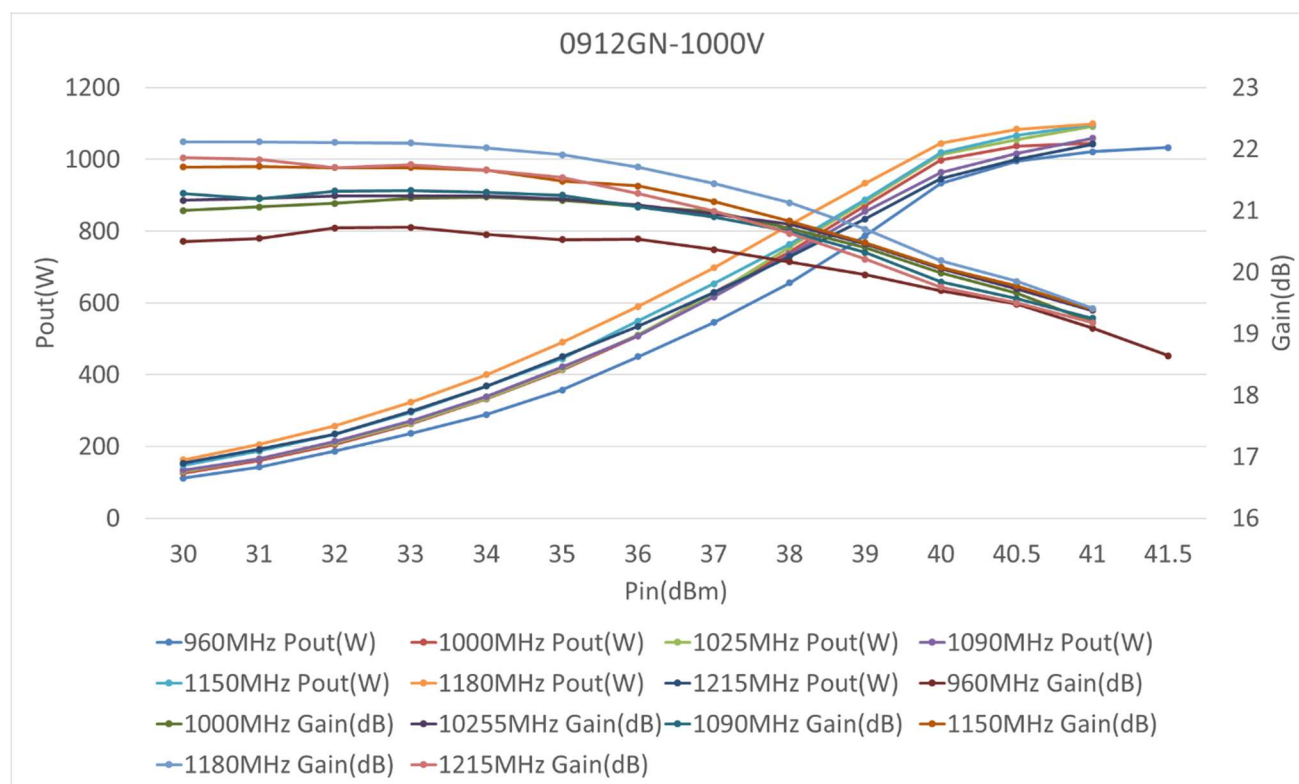
$I_{D(OFF)}$	Drain leakage current	$V_{GS} = -8V$, $V_D = 150V$			64	mA
$I_{G(OFF)}$	Gate leakage current	$V_{GS} = -8V$, $V_D = 0V$			20	mA

Export Classification: EAR 99

TYPICAL BROAD BAND PERFORMANCE DATA

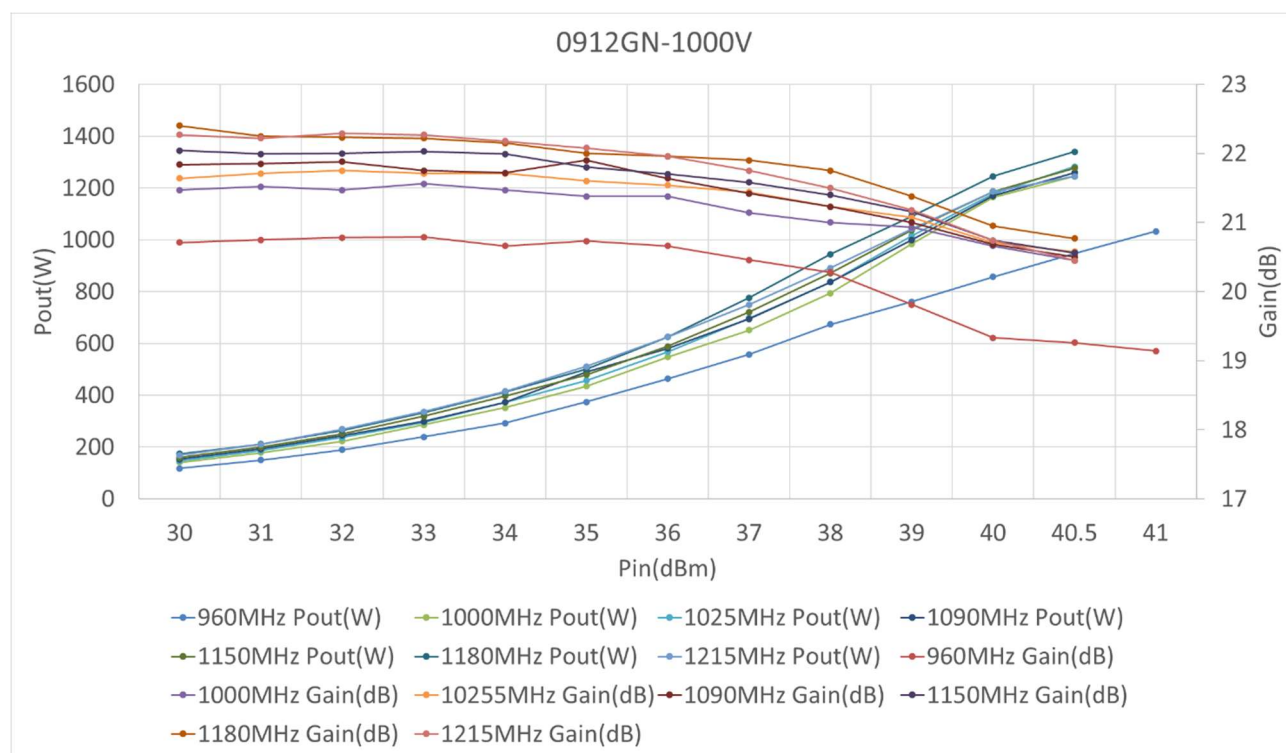
128uSec and 10% DF, Vds=50V

Frequency (GHz)	P _{IN} (W)	P _{OUT} (W)	IRL (dB)	Eff (%)	Gp (dB)	Droop
0.96	12.5	1021	-11.5	61	19.1	0.40
1.0	12.5	1045	-17	62	19.2	0.35
1.03	12.5	1091	-15	65	19.7	0.35
1.09	12.5	1059	-10	62	19.3	0.38
1.15	12.5	1096	-10	63	19.4	0.34
1.18	12.5	1099	-14	66	19.4	0.30
1.215	12.5	1042	-7	67	19.2	0.25



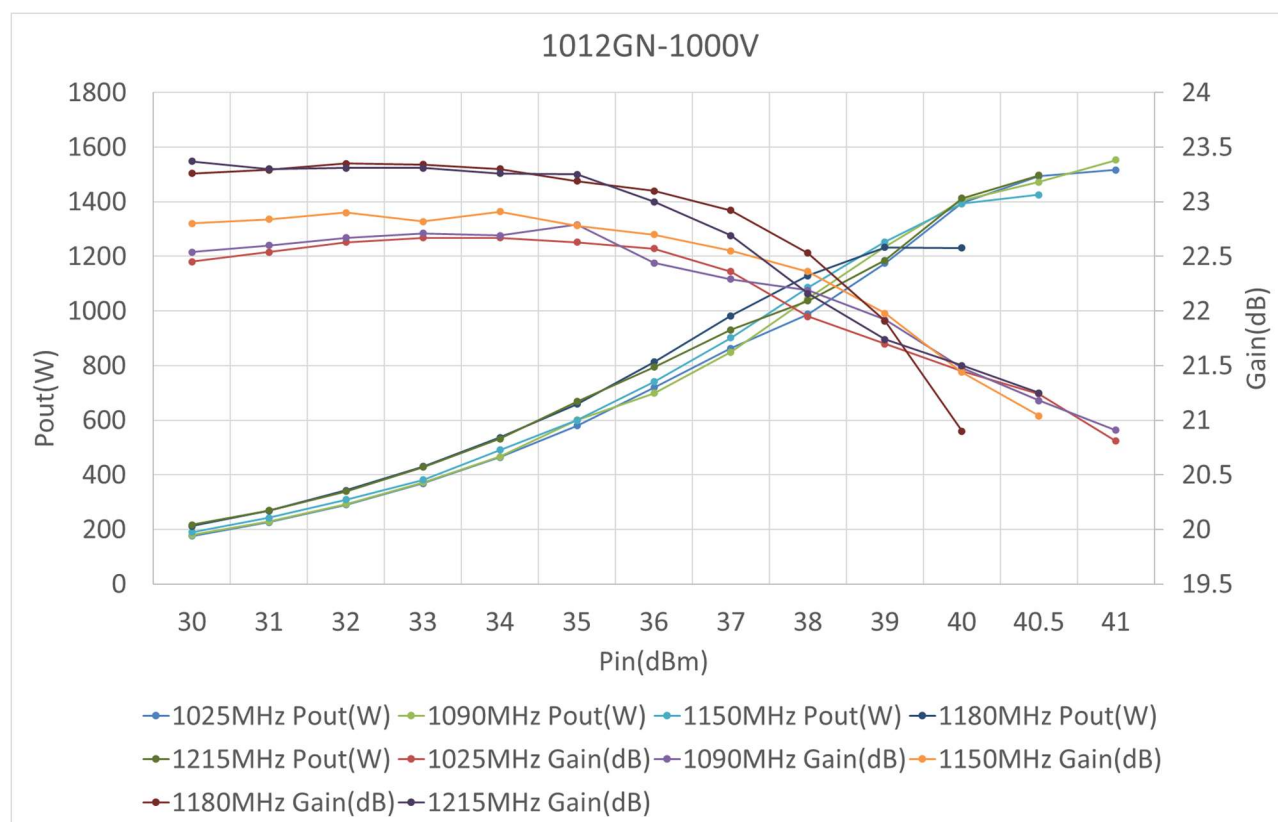
128uSec and 10% DF, Vds=60V

Frequency (GHz)	P _{IN} (W)	P _{OUT} (W)	IRL (dB)	Eff (%)	Gp (dB)	Droop
0.96	12.5	1033	-10	60	20.5	0.60
1.0	12.5	1245	-17	58	20.5	0.40
1.03	12.5	1282	-20	59	20.7	0.40
1.09	12.5	1259	-11	58	20.5	0.45
1.15	12.5	1276	-11	58	20.6	0.40
1.18	12.5	1340	-15	61	20.8	0.40
1.215	12.5	1245	-8	61	20.45	0.40

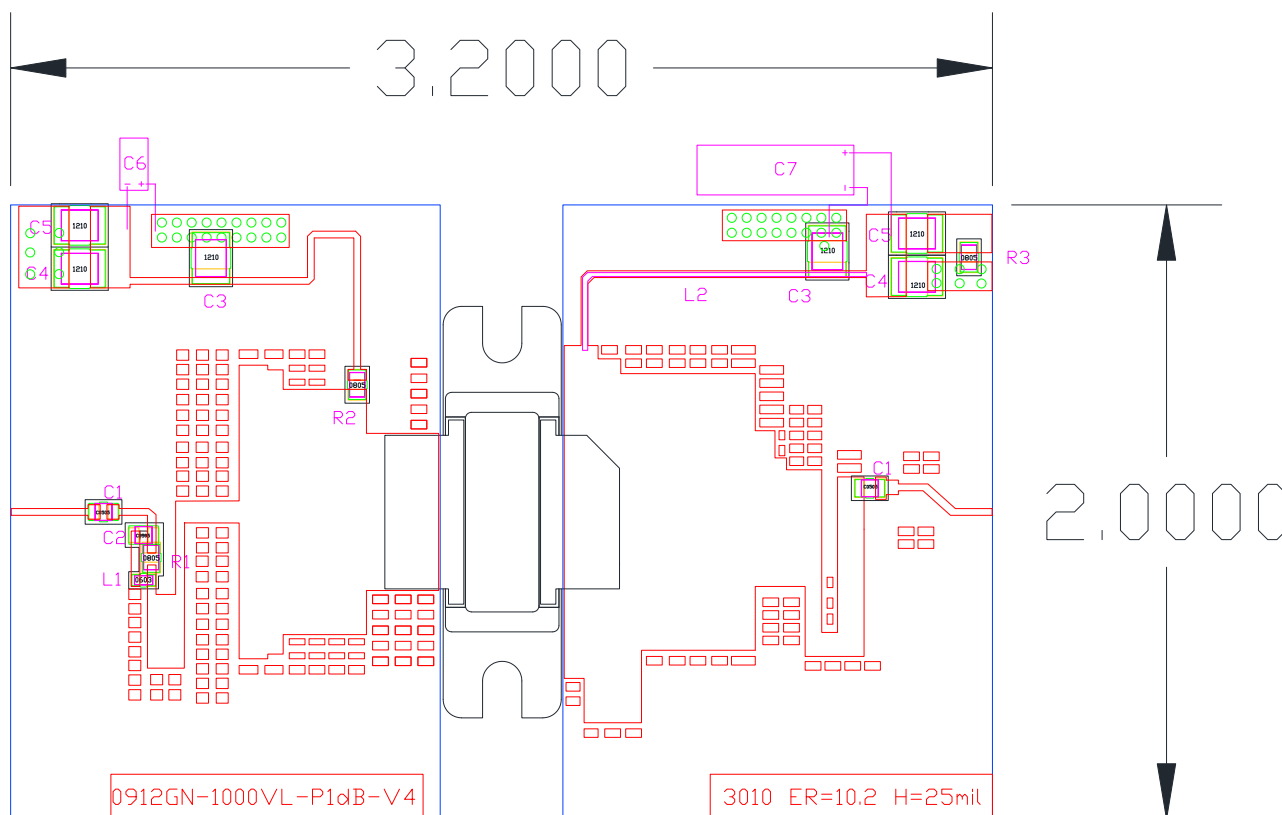


5uSec and 1% DF, Vds=60V

Frequency (GHz)	P _{IN} (W)	P _{OUT} (W)	IRL (dB)	Eff (%)	G _p (dB)
0.96	12.5	1517	-15	66	21.2
1.0	12.5	1045	-17	62	19.2
1.03	12.5	15.17	-15	68	20.8
1.09	12.5	1552	-10	67	20.9
1.15	12.5	1426	-10	64	21.0
1.18	12.5	1510	-14	67	20.8
1.215	12.5	1531	-8	70	20.7



TEST CIRCUIT (inches)

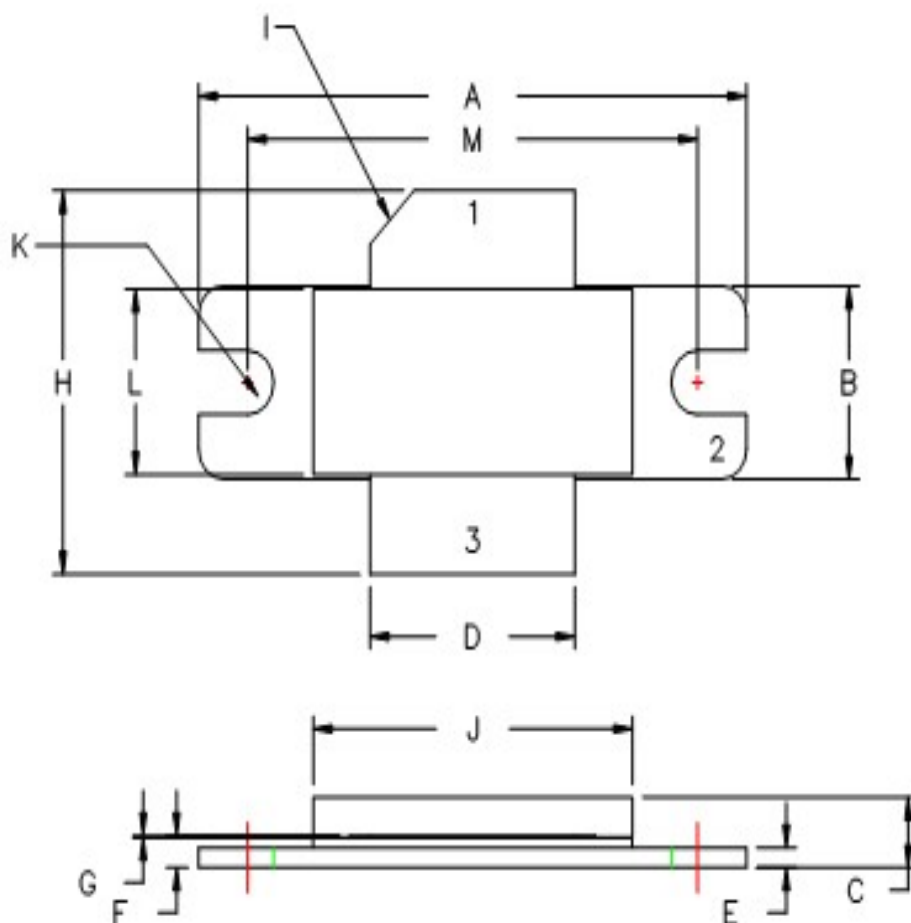


- Board Material: Roger Duroid 3010 @ H=25 mils, Er=10.2, 2oz Copper
- DXF file available upon request

BILL OF MATERIALS

Item	Description	Manufacturer	Manufacturer PN	Value	Quantity
C1	Ceramic Cap; 100pF; 250V; size 0505; $\pm 1\%$	Kyocera AVX	800A101FW250XT	100pF	2
C2	Ceramic Cap; 9.1pF; 150V; size 0505; $\pm 0.1\text{pF}$	Kyocera AVX	100A9R1BW150XT	9.1pF	1
C3	Ceramic Cap; 100pF; 500V; size 1111; $\pm 1\%$	Kyocera AVX	100B101FW500XT	100pF	2
C4	Ceramic Cap; 10,000pF; 100V; size 0805; $\pm 10\%$	KEMET	C0805C104K1RACAUTO	100,000pF	2
C5	Ceramic Cap; 1,000pF; 100V; size 0805; $\pm 10\%$	KEMET	C0805C102K1RAC7800	1000pF	2
C6	Alum Electrolytic Cap; 10uF; 250V; 20%; Radial; -55C to +105C	Nichicon	UVZ2E100MPD	10uF	1
C7	Alum Electrolytic Cap; CAP ALUM 6800UF 20% 80V SNAP	Nichicon	LGY1K682MELC45	6300uF	1
R1	Chip Resistor; 365 Ω ; 0.33W; size 0805; $1\pm\%$	TE Connectivity / Holsworthy	CRGH0805F365R	365ohms	1
R2	Chip Resistor; 20 Ω ; 0.5W; size 0805; $\pm 1\%$	Rohm Semiconductor	SDR10EZPF20R0	20ohms	1
R3	Chip Resistor; 5 Ω ; 0.5W; size 0805; $\pm 1\%$	Rohm Semiconductor	SDR10EZPF5R60	5ohms	1
L1	Chip Inductor, 1.2nH, size 0603, $\pm 0.3\text{nH}$	Verikel	LMC1608-1N2ST	1.2nH	1
L2	22 AWG COPPER WIRE FOR RF CHOKE	Any	Any	L=1400 Mils	1

0912GN-1000V 55-Q03 Package



DIM	MILLIMETER	TOL	INCHES	TOL
A	34.03	.25	1.340	.010
B	9.78	.25	.385	.010
C	3.55	.19	.140	.007
D	12.70	.13	.500	.005
E	1.02	.13	.040	.005
F	1.65	.13	.065	.005
G	0.13	.03	.005	.001
H	19.43	.76	.765	.030
I	45°	5°	45°	5°
J	19.81	.25	.780	.030
K	3.30 DIA	.13	.130 DIA	.005
L	9.40	.13	.370	.005
M	27.94	MAX	1.100	MAX

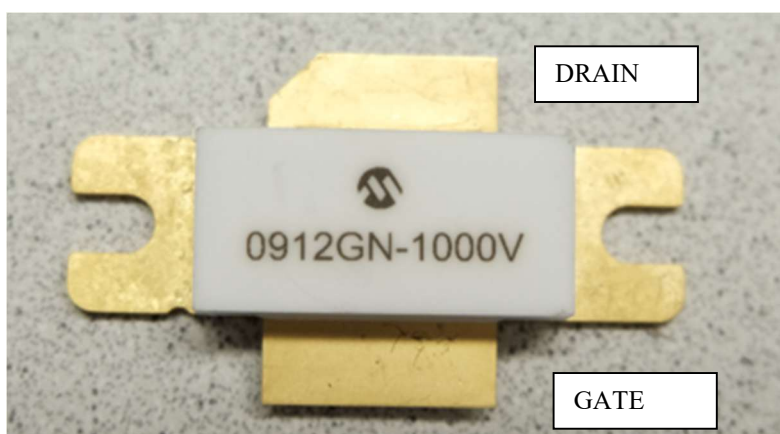
PIN 1 = DRAIN
PIN 2 = SOURCE
PIN 3 = GATE

0912GN-1000V Mounting Procedure and Tips

1. Background

The 0912GN-1000V model uses Q03 package. The package uses the package's two end "eared" sides to bolt down. It is possible that a less-than-ideal contact between flange bottom surface and heatsink slot surface can occur if careful attention is not made to the bolt down. Poor contact will cause transistor thermal and electrical ground defects and make the transistor easily prone to oscillation and low power output. Therefore, good flange and heatsink contact will be an important task during transistor mounting process.

2. Transistor Gate and source and drain photo



- Gate side has normal rectangular configuration.
- Drain side has chamfer at upper right side.
- The Source is the flange to heatsink bolt down slot to form both a thermal path and electrical ground surface.
- The flange bottom concave specification is 0mil -1 mil, therefore slot surface flatness required +/-0.5 mil flatness. The maximum gap between flange and slot is 1.5 mills.



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1000 Watts • 50 Volts • 128us, 10%
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3. Transistor mounting location should be in the middle of TF.
 - Transistor location should be in the middle of slot.
 - The unit should be pushed to drain side.
4. Slot surface flatness requirement is +/- 0.5 mil or less.
5. Apply thermal compound sparingly between flange bottom surface and heatsink slot surface. Make sure no visible particles are left on the flange bottom and slot surface to avoid voiding and poor contact.
6. The clamp post areas that contact ear'ed areas of package should be smooth and mechanically flat.
7. The 4-40 screws locking down the transistor unit should be screwed with symmetric force applied to either side.
8. Tips to identify the non-perfect contact between flange and slot surfaces:
 - a. At 1.15GHz, you can easily identify non-perfect contact: when you apply Pin=24dbm or below input power, you can observe over 23dB gain. Therefore 1.15GHz RF test should be started first.
 - b. Ensure the return loss level did not increase with increasing input power level.
 - c. Observe if the gain jumps significantly when input power level is increased.
9. Remount the device to get best contact when non-perfect contact is identified. Move the device up and down several times slightly in the slot and repeat action item 3 and 7 until close to the specification and any supplied RF test data at 1.15GHz. Maximum gain should be at about Pin=35dbm at room temperature.

Bias Instruction for Constant Gate Bias

Before connection to sample DUT, please check for Vgs and VDS solder contact damage. After Vgs and Vds power supply and RF in terminal and RF out terminal have been connected to DUT, please follow this procedure to turn on and off the device:

Turn ON procedure:

1. Set Vgs = -8V with current limit 200mA.
2. Use DMM to measure Vgs (input side of circuit) to make sure that Vgs = -8V
3. Slowly increase Vds (Drain voltage) from 0V to 50V & set limit current to 9.8A.
4. Slowly increase Vgs until Idq = 160mA (Vgs~-3.16V)
5. Apply RF input power & increase to spec (Pin=41dBm)

Turn OFF instruction:

1. Slowly decrease RF input power to minimum level and turn off.
2. Reduce Vgs to -8V.
3. Slowly decrease Vdd from 50V to 0V and turn off.
4. After large storage capacitor has been discharged fully and ensure Vdd (drain voltage) is completely turned off (0 Volts, no current).
5. Disconnect Vdd from DUT 6. Turn off Vgs.

Ordering Information

For additional ordering information, contact your Microchip sales representative.

Part Number	Package
0912GN-1000V	Flange Packaged Transistor
TF-0912GN-1000V	Test Fixture with Transistor Mounted



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Revision History

Revision Level / Date	Para. Affected	Description
12/12/2025	Typical Data	Initial Release



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