

16-Channel Serial-to-Parallel Converter with High-Voltage Backplane Driver and Push-Pull Outputs

Features

- +200V Maximum Output Voltage
- 500 kHz at $V_{DD} = 1.7V$ Shift Register Speed
- 16 High-Voltage Outputs
- High-Voltage Backplane Driver
- CMOS Input Levels

Applications

- Multiple Segment EL Display
- Piezoelectric Transducer Driver
- Braille Driver

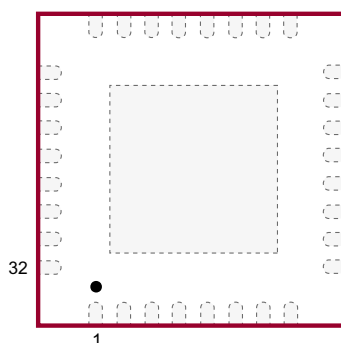
General Description

The HV528 is a 200V 16-channel serial-to-parallel converter with high-voltage outputs and backplane driver designed to source and sink ± 1 mA.

The high-voltage outputs are controlled by a 16-bit serial shift register, followed by a 16-bit latch. Data is shifted through the shift registers during the low-to-high clock transition. A data output buffer is provided for cascading multiple devices. Data is transferred to the 16-bit latch when a logic-level low is applied to the $\overline{LE}$ input. Data is stored in the latch when $\overline{LE}$ is high. Output states are controlled by the data in the latch and by the POL pin.

Package Type

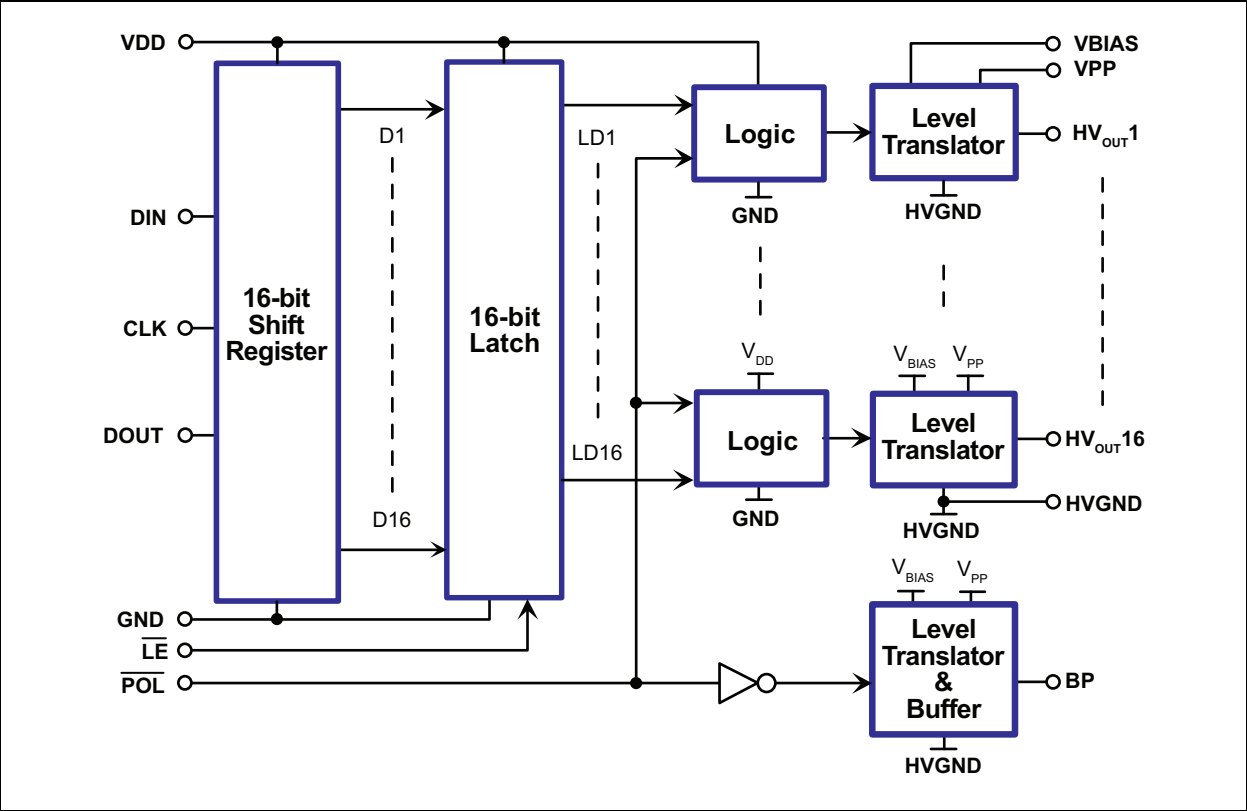
32-lead VQFN
(Top view)



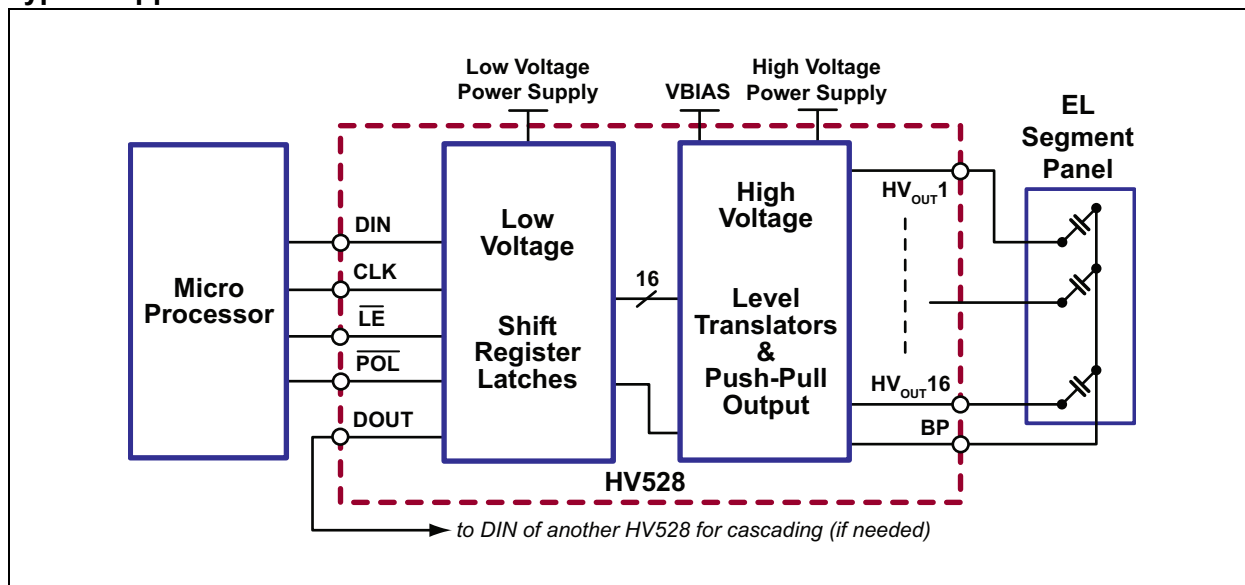
Pads are at the bottom of the package. Exposed heat slug is at V_{PP} potential. See [Table 2-1](#) for pin information.

HV528

Functional Block Diagram



Typical Application Circuit



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings^(†)

Logic Supply Voltage, V_{DD}	–0.5V to 7V
High-voltage Supply, V_{PP}	215V
Translator Supply Voltage, V_{BIAS}	–0.5V to 7V
Logic Input Levels	–0.5V to $V_{DD} + 0.5V$
Operating Junction Temperature, T_J	–40°C to +125°C
Storage Temperature, T_S	–65°C to +150°C

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Electrical Specifications: External ground noise reduction circuit will be provided by design upon characterization.						
Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Logic Supply Voltage	V_{DD}	1.7	3	5.5	V	
Level Translator Supply Voltage	V_{BIAS}	5.4	—	6.6	V	
Positive High-Voltage Supply	V_{PP}	50	—	200	V	
High-Level Input Voltage	V_{IH}	0.9 V_{DD}	—	V_{DD}	V	
Low-Level Input Voltage	V_{IL}	0	—	0.1 V_{DD}	V	
Operating Temperature	T_A	0	—	+70	°C	

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: Over operating supply voltages and temperature unless otherwise noted. $T_A = +25^\circ\text{C}$.						
Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
V_{DD} Supply Current	I_{DD}	—	—	1	mA	$f_{CLK} = 500\text{ kHz}$
Quiescent V_{DD} Supply Current	I_{DDQ}	—	—	10	μA	All logic inputs = V_{DD} or 0V
V_{BIAS} Supply Current	I_{BIAS}	—	—	100	μA	All HV_{OUTS} switching at 1 kHz. Peak $I_{BIAS} = 200\text{ mA}$ with all channels switching
Quiescent V_{BIAS} Current	I_{BIASQ}	—	—	10	μA	No HV_{OUT} switching
Quiescent V_{PP} Supply Current	I_{PPQ}	—	—	100	μA	$V_{PP} = 200V$, outputs are static
High-Level logic Input Current	I_{IH}	—	—	10	μA	$V_{IH} = V_{DD}$
Low-Level Logic Input Current	I_{IL}	—	—	–10	μA	$V_{IL} = 0V$
High-Level Output	HV_{OUT} & BP	V_{OH}	$V_{PP}-30V$	—	—	V $I_{HV_{OUT}} = -1\text{ mA}$, $50V \leq V_{PP} \leq 100V$
			$V_{PP}-16V$	—	—	V $I_{HV_{OUT}} = -1\text{ mA}$, $100V \leq V_{PP} \leq 200V$
	D_{OUT}		$V_{DD}-1V$	—	—	V $I_{D_{OUT}} = -1\text{ mA}$
Low-Level Output	HV_{OUT} & BP	V_{OL}	—	—	6	V $I_{HV_{OUT}} = 1\text{ mA}$
			—	—	1	V $I_{D_{OUT}} = 1\text{ mA}$
Logic Input Capacitance	C_{DIN}	—	—	10	pF	
Logic Output Capacitance	C_{DOUT}	—	—	10	pF	

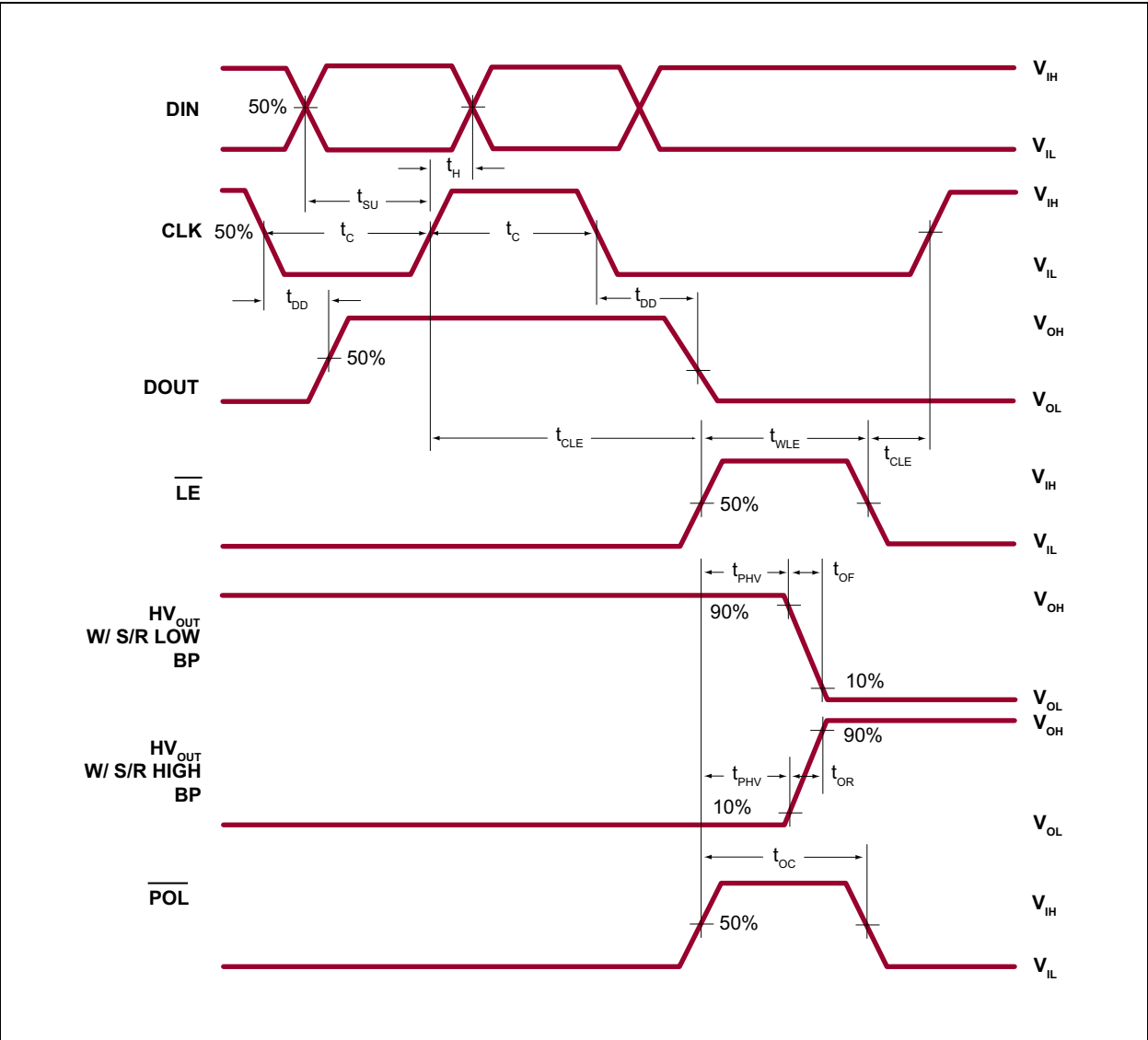
AC ELECTRICAL CHARACTERISTICS

Electrical Specifications: Over operating supply voltages and temperature unless otherwise noted. $T_A = +25\text{ }^{\circ}\text{C}$.						
Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Clock Frequency	f_{CLK}	0	—	500	kHz	
Clock High/Low Pulse Width	t_C	1	—	—	μs	
Data Setup Time before Clock Rises	t_{SU}	50	—	—	ns	
Data Hold Time after Clock Rises	t_H	50	—	—	ns	
$\overline{\text{LE}}$ from CLK Setup Time	t_{CLE}	15	—	—	ns	
$\overline{\text{LE}}$ Pulse Width	t_{WLE}	100	—	—	ns	
Clock Negative Edge to D_{OUT} Delay	t_{DD}	—	—	150	ns	$C_{\text{LDOUT}} = 50\text{ pF}$, (C_{LDOUT} includes C_{DIN} and C_{DOUT} .)
Delay Time from Inputs for $\text{HV}_{\text{OUT}}/\text{BP}$ to Start Rise/Fall	t_{PHV}	—	—	500	ns	$V_{\text{PP}} = 200\text{V}$, $V_{\text{BIAS}} = 5.4\text{V}$
$\text{HV}_{\text{OUTPUT}}/\text{BP}$ Rise Time	t_{OR}	—	—	300	μs	$C_L = 1500\text{ pF}$, $V_{\text{PP}} = 200\text{V}$
$\text{HV}_{\text{OUTPUT}}/\text{BP}$ Fall Time	t_{OF}	—	—	300	μs	$C_L = 1500\text{ pF}$, $V_{\text{BIAS}} = 5.4\text{V}$, $V_{\text{PP}} = 200\text{V}$
Width of POL Pulses	t_{OC}	$t_{\text{PHV}} + t_{\text{OR}}/t_{\text{OF}}$	—	—	μs	

TEMPERATURE SPECIFICATIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
TEMPERATURE RANGE						
Operating Junction Temperature	T_J	-40	—	+125	$^{\circ}\text{C}$	
Operating Ambient Temperature	T_A	0	—	+70	$^{\circ}\text{C}$	
Storage Temperature	T_S	-65	—	+150	$^{\circ}\text{C}$	
PACKAGE THERMAL RESISTANCE						
32-lead VQFN	θ_{JA}	—	22	—	$^{\circ}\text{C/W}$	

Timing Waveforms



2.0 PIN DESCRIPTION

The details on the pins of HV528 are listed in [Table 2-1](#).
Refer to [Package Type](#) for the location of pins.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	HVOUT12	High-voltage push-pull output
2	HVOUT11	High-voltage push-pull output
3	HVOUT10	High-voltage push-pull output
4	HVOUT9	High-voltage push-pull output
5	HVOUT8	High-voltage push-pull output
6	HVOUT7	High-voltage push-pull output
7	HVOUT6	High-voltage push-pull output
8	HVOUT5	High-voltage push-pull output
9	HVOUT4	High-voltage push-pull output
10	HVOUT3	High-voltage push-pull output
11	HVOUT2	High-voltage push-pull output
12	HVOUT1	High-voltage push-pull output
13	NC	No connect
14	VPP	High-voltage supply
15	GND	Logic ground
16	NC	No connect
17	DIN	Data in
18	NC	No connect
19	CLK	Clock input logic
20	VDD	Logic supply voltage
21	$\overline{\text{POL}}$	Polarity bar input logic
22	$\overline{\text{LE}}$	Latch enable bar input logic
23	NC	No connect
24	DOUT	Data out
25	NC	No connect
26	VBIAS	Level translator bias voltage
27	HVGND	High-voltage ground
28	BP	High-voltage backplane output
29	HVOUT16	High-voltage push-pull output
30	HVOUT15	High-voltage push-pull output
31	HVOUT14	High-voltage push-pull output
32	HVOUT13	High-voltage push-pull output
Center Pad		The center pad is at VPP potential. Leave floating or connect to VPP. Do not ground.

3.0 FUNCTIONAL DESCRIPTION

Follow the steps below to power up and power down the HV528.

TABLE 3-1: POWER-UP AND POWER-DOWN SEQUENCE

Power-up ⁽¹⁾		Power-down	
Step	Description	Step	Description
1	Connect ground.	1	Remove V_{PP} .
2	Apply V_{DD} .	2	Remove V_{BIAS} .
3	Set all inputs (D_{IN} , CLK , $\overline{LE}$, $\overline{POL}$) to a known state.	3	Set all inputs to low logic level.
4	Apply V_{BIAS} .	4	Remove V_{DD} .
5	Apply V_{PP} .	5	Disconnect ground.

Note 1: This power-up sequence requires an external high-voltage diode between V_{DD} and V_{PP} . Without the diode, power up V_{PP} to a V_{DD} level first to bias the silicon substrate. After all other signals are powered, finish raising the V_{PP} to its final level.

TABLE 3-2: TRUTH FUNCTION TABLE⁽¹⁾

Function	Inputs				Outputs					
					Shift Register Contents		HV Outputs		BP	D_{OUT}
	D_{IN}	CLK	$\overline{LE}$	$\overline{POL}$	1	2...16	1	2...16		
Load S/R	H or L	↑	H	X	H or L	Note 2	Note 2	Note 2	X	Note 2
Transfer Data in Latch	X	L	L	H	Note 3	Note 3	Note 3	Note 3	L	Note 2
	X	L	L	L	Note 3	Note 3	Note 3 (b)	Note 3 (b)	H	Note 2
Store Data in Latches	X	X	H	H	Note 2	Note 2	Note 2	Note 2	L	Note 2
	X	X	H	L	Note 2	Note 2	Note 2 (b)	Note 2 (b)	H	Note 2
Transparent Mode	L	↑	L	H	L	Note 2	L	Note 2	L	Note 2
	H	↑	L	H	H	Note 2	H	Note 2	L	Note 2
Invert Mode	X	X	H	L	Note 2	Note 2	Note 2 (b)	Note 2 (b)	H	X
	X	X	H	H	Note 2	Note 2	Note 2	Note 2	L	X

Note 1: H = High-logic level
 L = Low-logic level
 X = Irrelevant
 ↑ = Low-to-high transition
2: Dependent on previous stage's state before the last CLK or last LE low
3: Data at the last CLK ↑
4: **b** = bar over all symbols

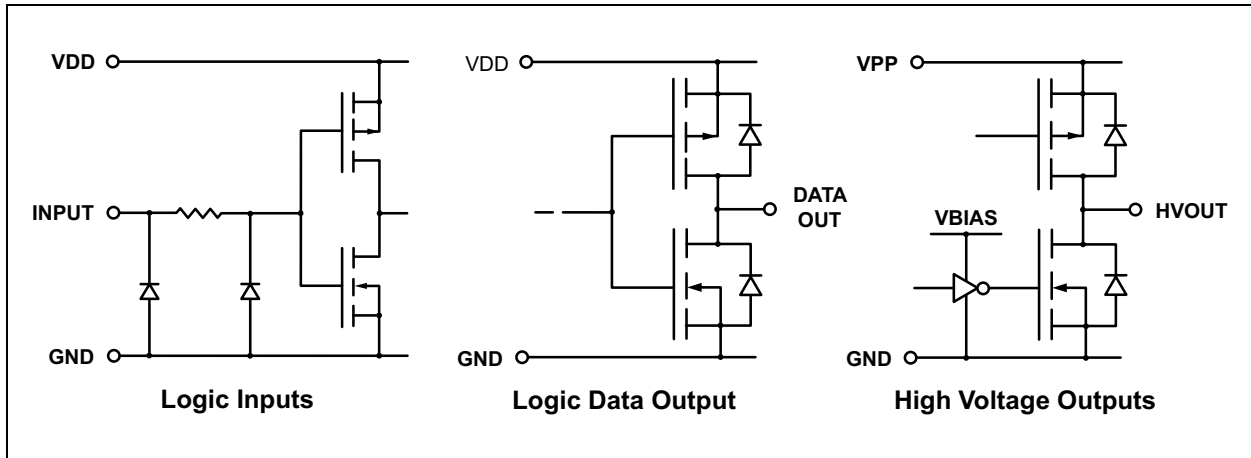


FIGURE 3-1: Input and Output Equivalent Circuits.

3.1 V_{BIAS} SUPPLY

The V_{BIAS} supply operates from 5.4V to 6.6V. It is the gate drive voltage for all of the output N-channel MOSFETs. This allows the output peak current sink to be set by varying the V_{BIAS} voltage. A higher V_{BIAS} voltage increases current sinking capability.

The operating V_{DD} range is from 1.7V to 5.5V. A plot showing the typical characteristics of I_{SINK} vs. V_{BIAS} is shown in [Figure 3-2](#).

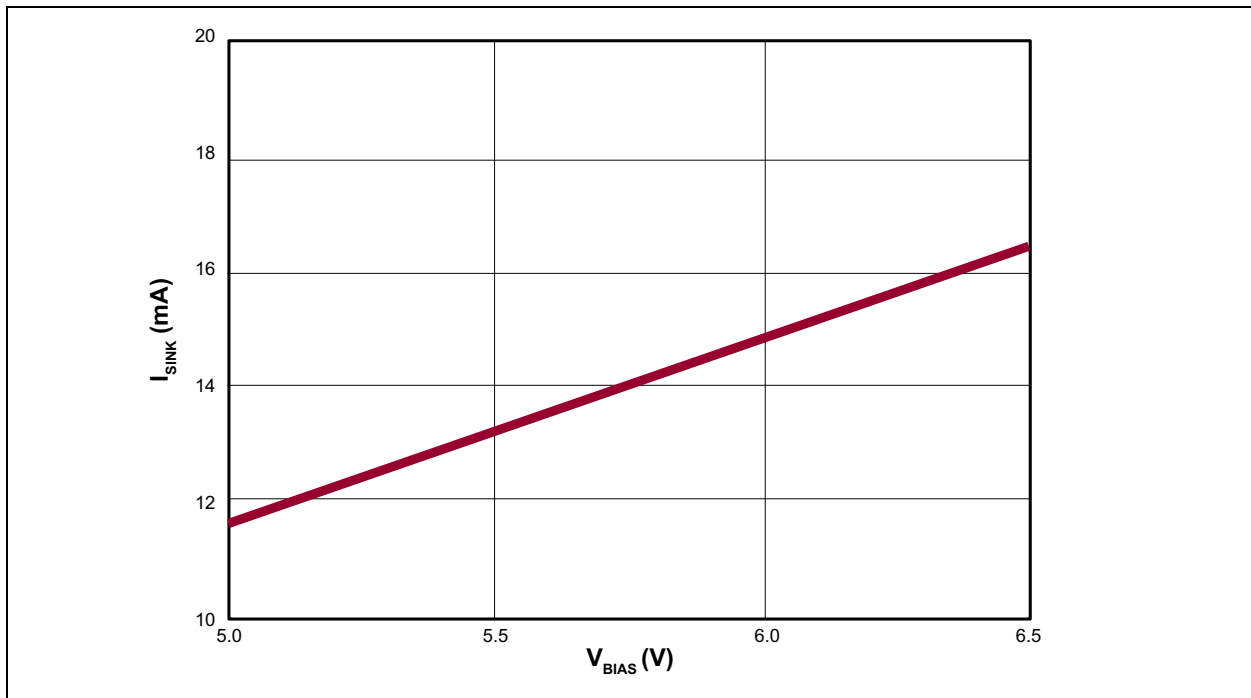
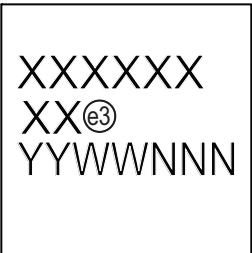


FIGURE 3-2: Typical H_{VOUT} I_{SINK} vs. V_{BIAS} ($V_{PP} = 200V$, $C_{LOAD} = 1\text{ nF}$).

4.0 PACKAGE MARKING INFORMATION

4.1 Packaging Information

32-lead VQFN



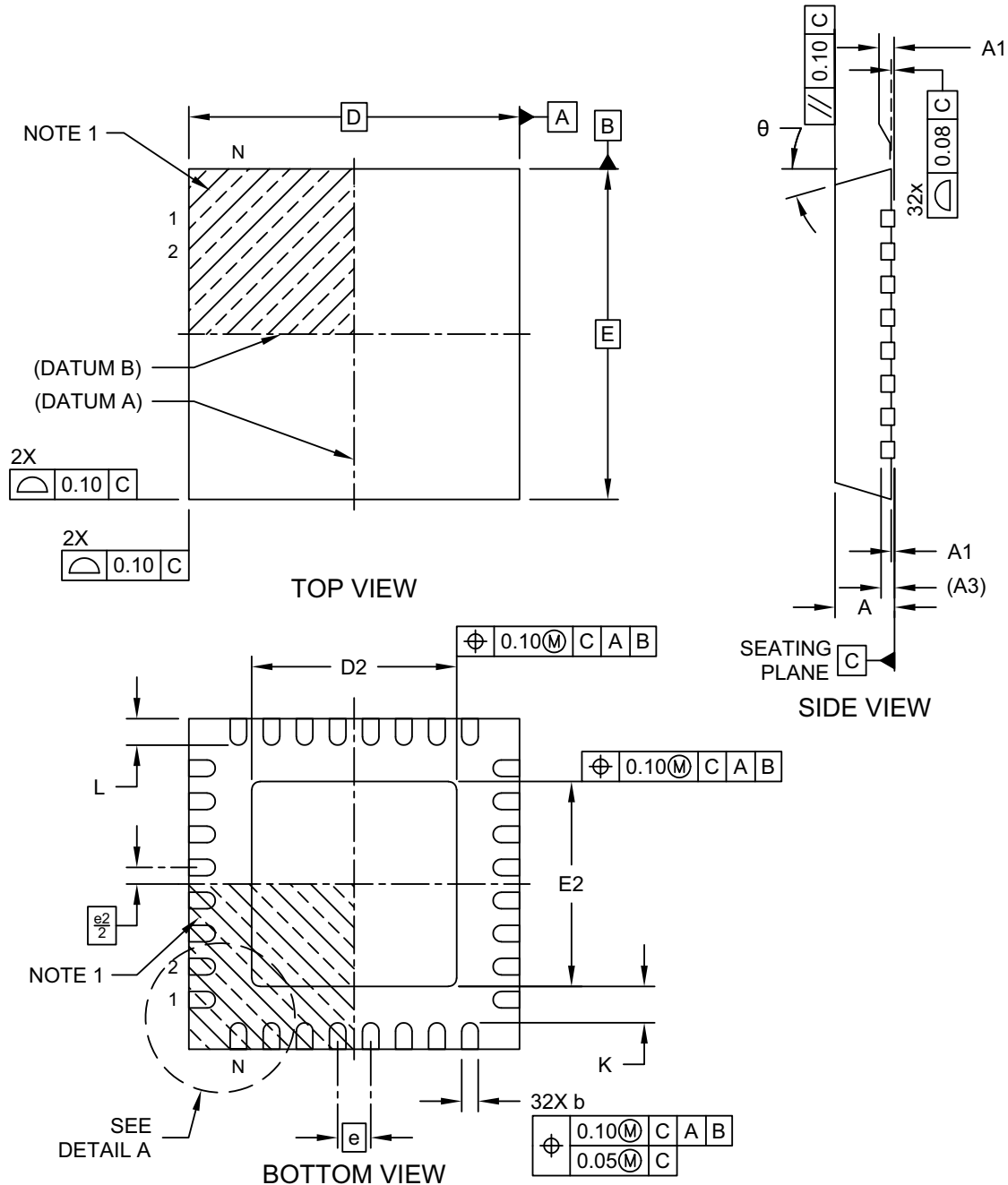
Example



Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC [®] designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.	

32-Lead Very Thin Plastic Quad Flat, No Lead Package (SHX) - 5x5x1.0 mm Body [VQFN] With Exposed Pad; Supertex Package Code K6

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

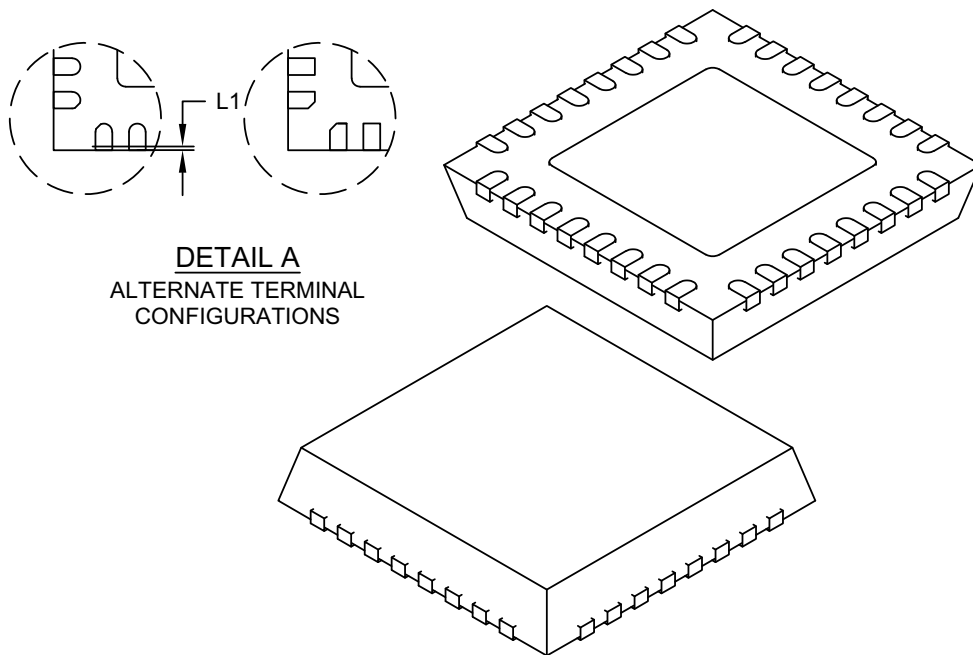


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32-Lead Very Thin Plastic Quad Flat, No Lead Package (SHX) - 5x5x1.0 mm Body [VQFN] With Exposed Pad; Supertex Package Code K6

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Terminals	N	32		
Pitch	e	0.50 BSC		
Overall Height	A	0.80	0.90	1.0
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3	0.20 REF		
Overall Length	D	5.00 BSC		
Exposed Pad Length	D2	1.05	—	3.55
Overall Width	E	5.00 BSC		
Exposed Pad Width	E2	1.05	—	3.55
Terminal Width	b	0.18	0.25	0.30
Terminal Length	L	0.30	0.40	0.50
Terminal-to-Exposed-Pad	K	0.20	—	—
Mold Draft Angle	θ	0°	—	14°
Pullback distance	L1	0	—	0.15

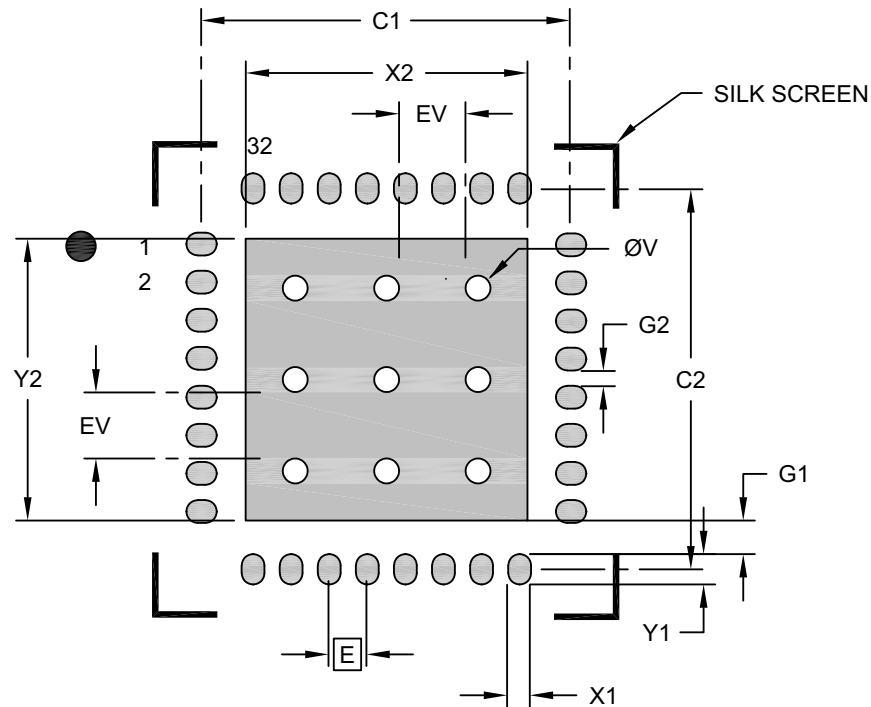
Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.
- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-00310-SHX Rev A Sheet 2 of 2

32-Lead Very Thin Plastic Quad Flat, No Lead Package (SHX) - 5x5x1.0 mm Body [VQFN] With Exposed Pad; Supertex Package Code K6

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Center Pad Width	X2			3.55
Center Pad Length	Y2			3.55
Contact Pad Spacing	C1		4.50	
Contact Pad Spacing	C2		4.50	
Contact Pad Width (Xnn)	X1			0.30
Contact Pad Length (Xnn)	Y1			0.40
Contact Pad to Center Pad (Xnn)	G1	0.44		
Contact Pad to Contact Pad (Xnn)	G2	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	
Thermal Via Pitch	EV		1.00	

Notes:

- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
- For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2310 Rev A

HV528

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (July 2023)

- Converted Supertex Doc# DSFP-HV528 to Microchip DS20005849A
- Removed reference to “HVC MOS[®] Technology”
- Changed the part marking format
- Removed the 32-lead VQFN K6 M932 media type to align packaging specifications with the actual BQM
- Updated package outline drawing
- Made minor text changes throughout the document

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<u>PART NO.</u>	<u>XX</u>	-	<u>X</u>	-	<u>X</u>
Device	Package Options		Environmental		Media Type
Device:	HV528	=	16-Channel Serial-to-Parallel Converter with High-Voltage Backplane Driver and Push-Pull Outputs		
Package:	K6	=	32-lead VQFN		
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package		
Media Types:	(blank)	=	490/Tray for a K6 Package		

Example:

a) HV528K6-G: 16-Channel Serial-to-Parallel Converter with High-Voltage Backplane Driver and Push-Pull Outputs, 32-lead VQFN, 490/Tray

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