

3A High-Efficiency Low Dropout Regulator

MIC38300



Description



Important: The MIC38300 is not recommended for new designs, as it is being replaced by the MIC38300A, which has a thicker package. More information about the MIC38300A part can be found on the Microchip website: www.microchip.com/en-us/product/mic38300a

The MIC38300 is a 3A peak, 2.2A continuous output current step down converter. This is the first device in a new generation of high-efficiency, low-dropout regulators that provide the benefits of an LDO in respect to ease of use, fast transient performance, high PSRR, and low noise while offering the efficiency of a switching regulator.

As output voltages move lower, the output noise and transient response of a switching regulator become an increasing challenge for designers. By combining a switcher whose output is slaved to the input of a high-performance LDO, high efficiency is achieved with a clean low noise output. The MIC38300 is designed to provide less than 5 mV of peak to peak noise and over 70 dB of PSRR at 1 kHz. Furthermore, the architecture of the MIC38300 is optimized for fast load transients that allow maintenance of less than 30 mV of output voltage deviation even during ultra-fast load steps, making the MIC38300 an ideal choice for low-voltage ASICs and other digital ICs.

The MIC38300 features a fully-integrated switching regulator and LDO combo, operates with input voltages from 3.0V to 5.5V input, and offers adjustable output voltages down to 1.0V.

The MIC38300 is offered in the small 28-pin 4 mm × 6 mm × 0.9 mm VQFN package and can operate from -40°C to +125°C.

Features

- 3.0A peak output current
- 2.2A continuous operating current
- Input voltage range: 3.0V to 5.5V
- Adjustable output voltage down to 1.0V
- Output noise less than 5 mV
- Ultra-fast transient performance
- Unique switcher plus LDO architecture
- Fully-integrated MOSFET switches
- Micro-power shutdown
- Easy upgrade from LDO as power dissipation becomes an issue
- Thermal shutdown and current-limit protection
- 28-pin 4 mm × 6 mm × 0.9 mm VQFN package

Applications

- Point-of-load applications
- Networking, server, industrial power
- Wireless base-stations
- Sensitive RF applications

Typical Application

Figure 1. Typical Application Circuit

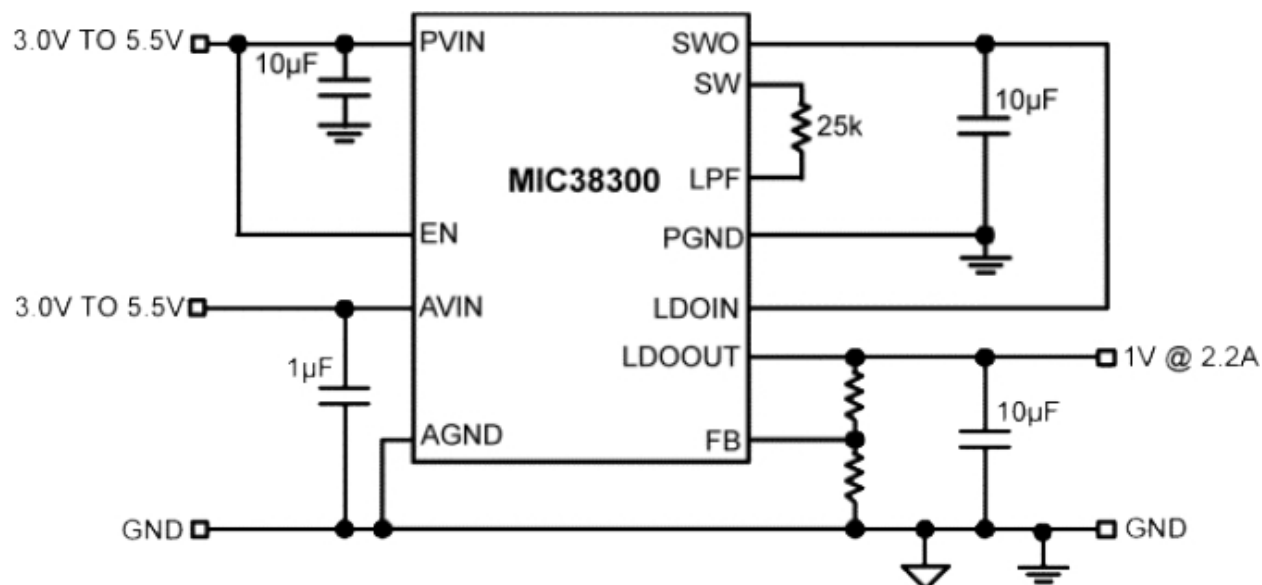
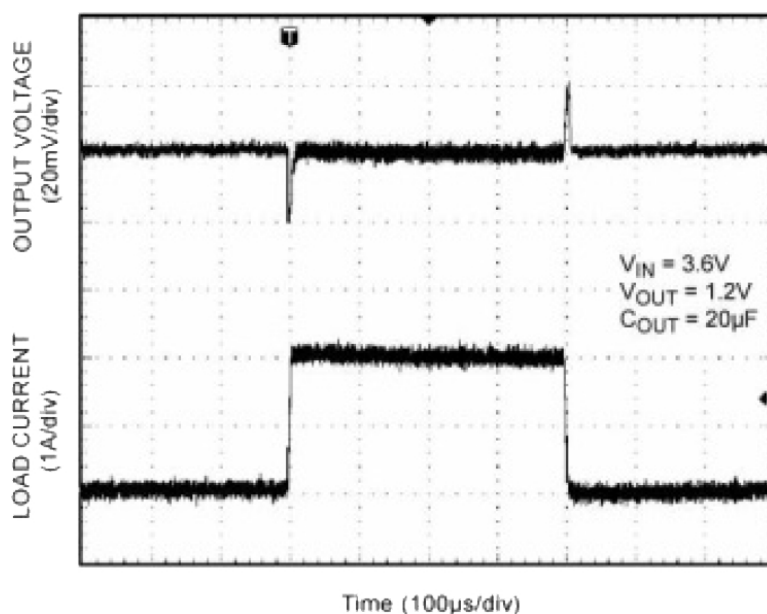


Figure 2. Load Transient 2A



Functional Block Diagram

Figure 3. Functional Block Diagram

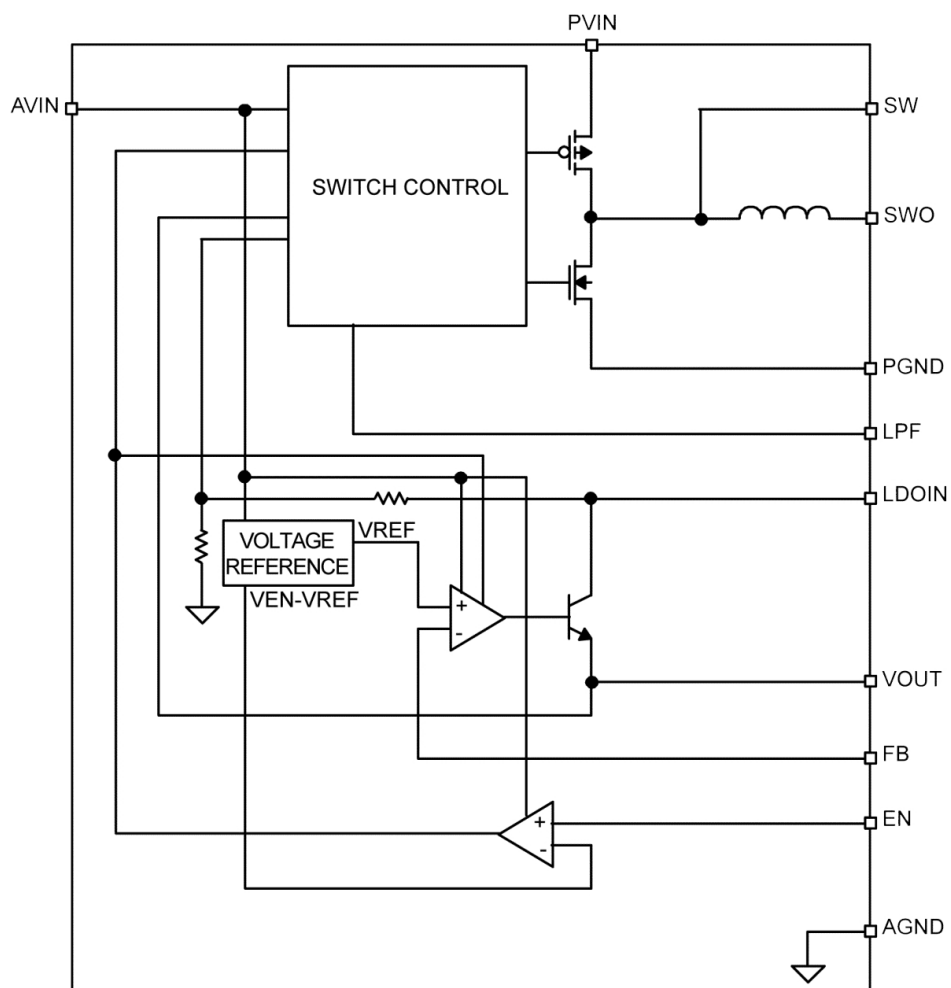


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1. Electrical Characteristics

1.1. Absolute Maximum Ratings

Supply Voltage (V_{IN})	6V
Output Switch Voltage (V_{SW})	6V
LDO Output Voltage (V_{OUT})	6V
Logic Input Voltage (V_{EN})	-0.3V to V_{IN}

Note: Exceeding the absolute maximum rating may damage the device.

1.2. Operating Ratings

Supply Voltage (V_{IN})	3.0V to 5.5V
Enable Input Voltage (V_{EN})	0V to V_{IN}

Note: The device is not guaranteed to function outside its operating rating.

1.3. Electrical Parameters and Values

$T_A = 25^\circ\text{C}$ with $V_{IN} = V_{EN} = 5\text{V}$; $I_{OUT} = 10\text{ mA}$, $V_{OUT} = 1.8\text{V}$. **Bold** values indicate $-40^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$, unless noted. See Note 1.

Table 1-1. Electrical Characteristics

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Supply Voltage Range	V_{IN}	3.0	—	5.5	V	AVIN, PVIN pins
Undervoltage Lockout Threshold	V_{UVLO_TH}	—	2.85	—	V	Turn-on
Undervoltage Lockout Hysteresis	V_{UVLO_HYS}	—	100	—	mV	—
Quiescent Current	I_Q	—	1	—	mA	$I_{OUT} = 0\text{A}$, not switching, open loop
Turn-on Time	t_{ON}	—	200	500	μs	V_{OUT} to 95% of nominal
Shutdown Current	I_{SD}	—	30	50	μA	$V_{EN} = 0\text{V}$
Feedback Voltage	V_{FB}	0.975	1	1.025	V	$\pm 2.5\%$
Feedback Current	I_{FB}	—	5	—	nA	—
Dropout Voltage	$V_{IN} - V_{OUT}$	—	0.85	1.2	V	$I_{LOAD} = 2.2\text{A}$; $V_{OUT} = 3\text{V}$
Current Limit	I_{LIM}	3	5	—	A	$V_{FB} = 0.9 \times V_{NOM}$
Output Voltage Load Regulation	$\Delta V_{OUT}/V_{OUT}$	—	0.3	1	%	$V_{OUT} = 1.8\text{V}$, 10 mA to 2.2A
Output Voltage Line Regulation	$\Delta V_{OUT} / (V_{OUT} \times \Delta V_{IN})$	—	0.35	0.5	%/V	$V_{OUT} = 1.8\text{V}$, V_{IN} from 3.0V to 5.5V
Output Ripple	ΔV_{OUT}	—	2	—	mV	$I_{LOAD} = 1.5\text{A}$, $C_{OUTLDO} = 20\text{ }\mu\text{F}$, $C_{OUTSW} = 20\text{ }\mu\text{F}$, LPF = 25 k Ω
Over-Temperature Shutdown	T_{SD}	—	150	—	$^\circ\text{C}$	—
Over-Temperature Shutdown Hysteresis	T_{SD_HYS}	—	15	—	$^\circ\text{C}$	—
Enable Input (see Note 2)						
Enable Input Threshold	$V_{IN(EN)}$	0.90	1	1.1	V	Regulator enable
Enable Hysteresis	HYS_{EN}	20	100	200	mV	—
Enable Input Current	I_{EN}	—	0.03	1	μA	—

Notes:

1. Specification for packaged product only.
2. Enable pin should not be left open.

1.4. Temperature Specifications

Note: Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5 kΩ in series with 100 pF.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Storage Temperature	T_S	-65	—	+150	°C	—
Junction Temperature	T_J	-40	—	+125	°C	—
Ambient Temperature	T_A	—	25	—	°C	—
Power Dissipation	P_D	—	—	$(T_{J(max)} - T_A) / \theta_{JA}$	°C/W	Internally limited. See Note 1 below.
Package Thermal Resistance, 28-pin VQFN	θ_{JA}	—	24	—	°C/W	—

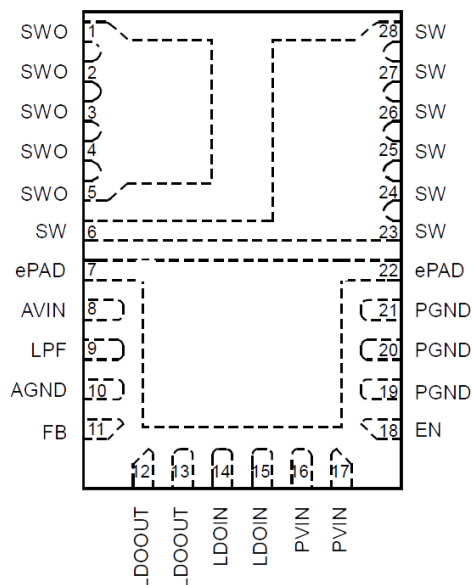
Note:

1. The maximum allowable power dissipation of any T_A (ambient temperature) is $P_{D(max)} = (T_{J(max)} - T_A) / \theta_{JA}$. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the regulator will go into thermal shutdown.

2. Pin Configuration

2.1. Package Type

Figure 2-1. Top View of the MIC38300 28-Pin 4mm × 6mm VQFN



2.2. Pin Descriptions

Table 2-1. MIC38300 Pin Descriptions

Pin Number	Pin Name	Description
1, 2, 3, 4, 5	SWO	Switch (Output): This is the output of the PFM Switcher.
6, 23, 24, 25, 26, 27, 28	SW	Switch Node: Attach external resistor from LPF to increase hysteric frequency.
7, 22	EPAD	Exposed Heat-sink Pad. Connect externally to PGND.
8	AVIN	Analog Supply Voltage: Supply for the analog control circuitry. Requires bypass capacitor to ground. Nominal bypass capacitor is 1 μ F.
9	LPF	Low Pass Filter: Attach external resistor from SW to increase hysteretic frequency.
10	AGND	Analog Ground.
11	FB	Feedback: Input to the error amplifier. Connect to the external resistor divider network to set the output voltage.
12, 13	LDOOUT	LDO Output: Output of voltage regulator. Place capacitor to ground to bypass the output voltage. Nominal bypass capacitor is 10 μ F.
14, 15	LDOIN	LDO Input: Connect to SW output. Requires a bypass capacitor to ground. Nominal bypass capacitor is 10 μ F.
16, 17	PVIN	Input Supply Voltage (Input): Requires bypass capacitor to GND. Nominal bypass capacitor is 10 μ F.
18	EN	Enable (Input): Logic low will shut down the device, reducing the quiescent current to less than 50 μ A. This pin can also be used as an undervoltage lockout function by connecting a resistor divider from EN/UVLO pin to VIN and GND. It should be not left open.
19, 20, 21	PGND	Power Ground.

3. Typical Characteristics

$V_{IN} = 3.3V$, $V_{OUT} = 1.8V$, $C_{OUT} = 10\ \mu F$, $R_{LPF} = 25\ k\Omega$, $I_{OUT} = 100\ mA$, unless noted.

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Figure 3-1. MIC38300 PSRR

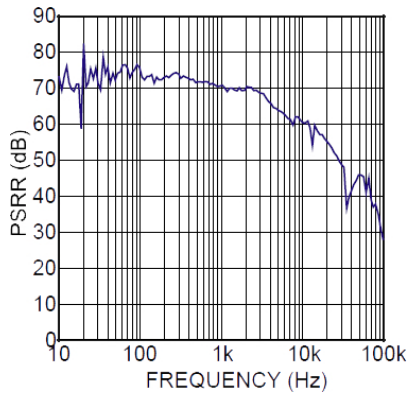


Figure 3-2. Load Regulation

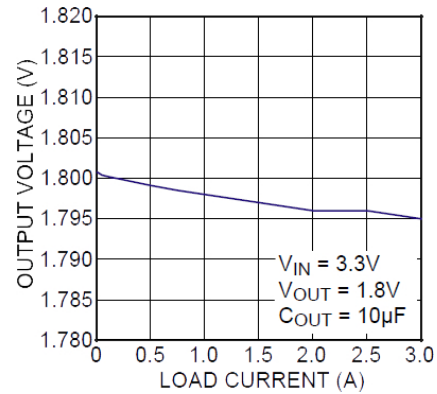


Figure 3-3. Output Voltage vs. Input Voltage

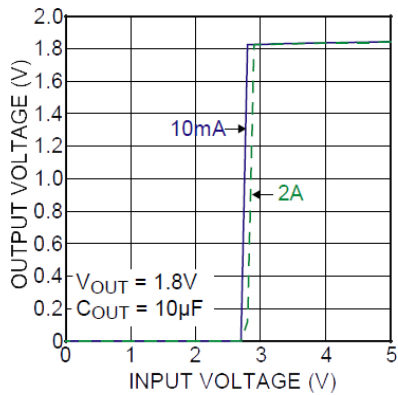


Figure 3-4. Output Voltage vs. Temperature

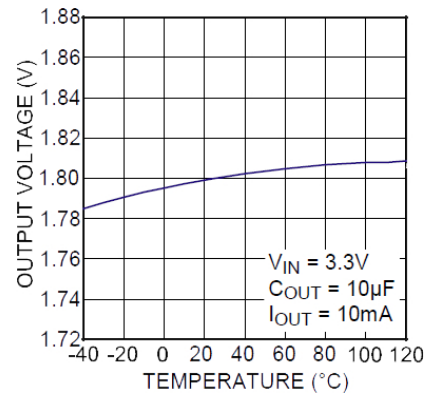


Figure 3-5. Thermal Shutdown

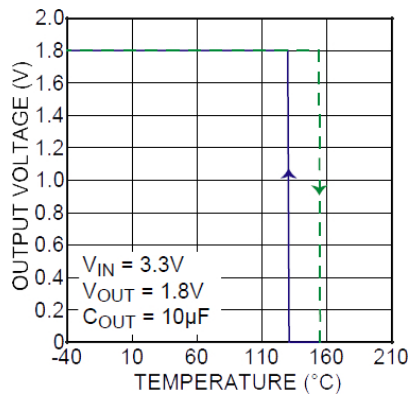


Figure 3-6. MIC38300 Efficiency

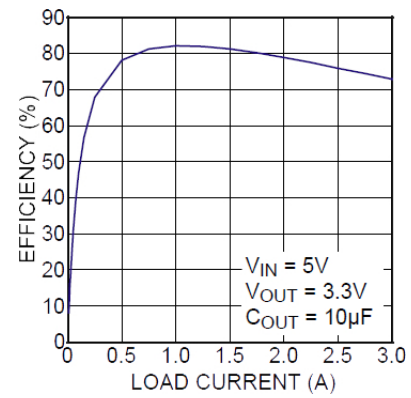


Figure 3-7. Dropout Voltage vs. Load Current

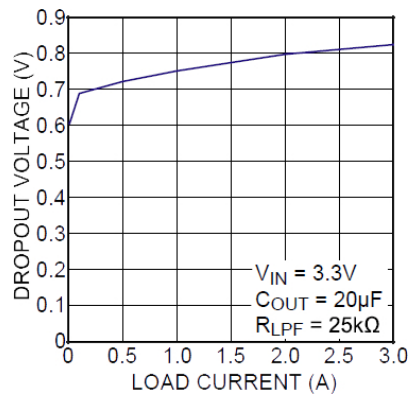


Figure 3-8. Dropout Voltage vs. Temperature

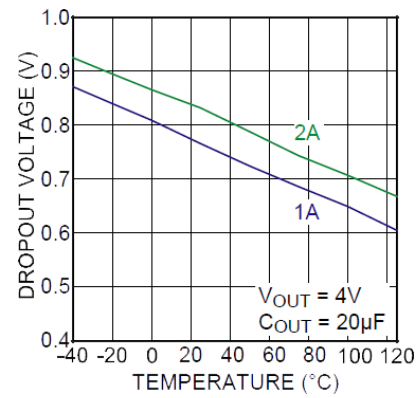


Figure 3-9. Current Limit vs. Input Voltage

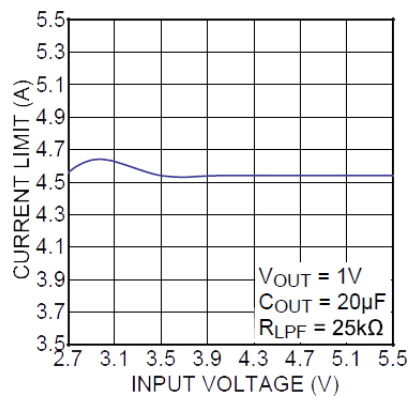


Figure 3-10. Enable Threshold

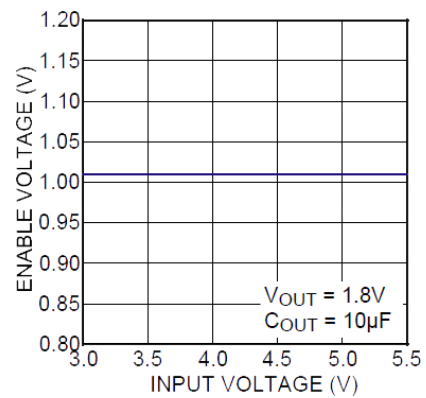


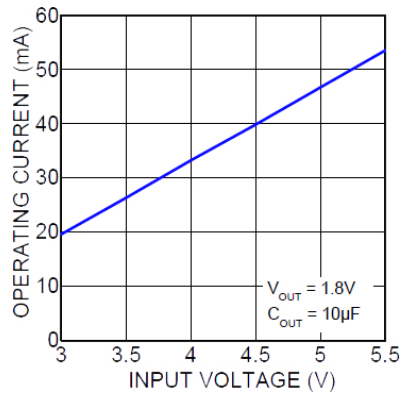
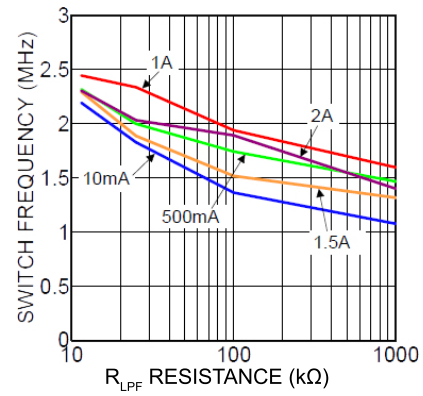
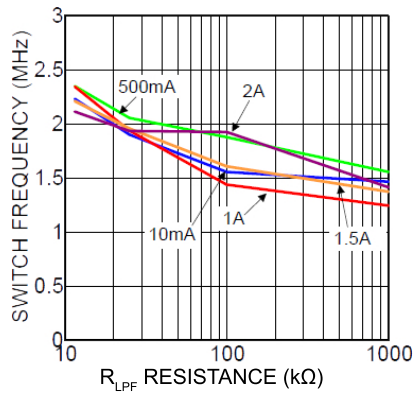
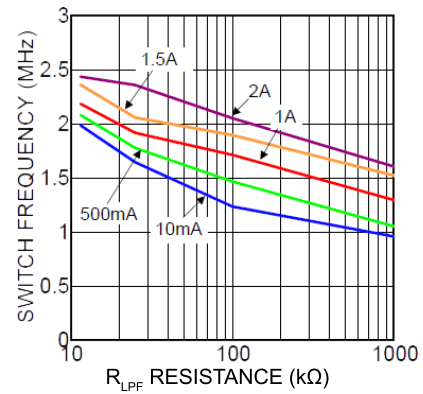
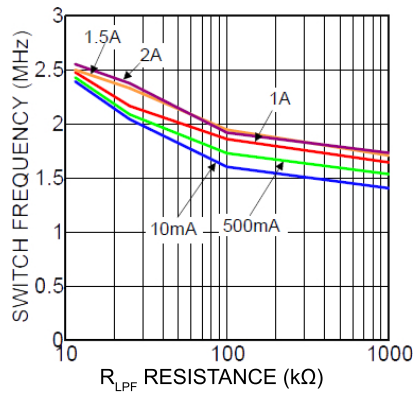
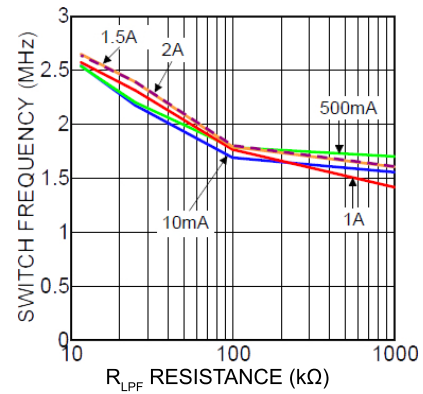
Figure 3-11. Operating Current vs. Input Voltage**Figure 3-12.** Switch Frequency vs. R_{LPF} Resistance ($V_{IN} = 3.3V$, $V_{OUT} = 1.0V$)**Figure 3-13.** Switch Frequency vs. R_{LPF} Resistance ($V_{IN} = 3.3V$, $V_{OUT} = 1.8V$)**Figure 3-14.** Switch Frequency vs. R_{LPF} Resistance ($V_{IN} = 5.0V$, $V_{OUT} = 1.0V$)**Figure 3-15.** Switch Frequency vs. R_{LPF} Resistance ($V_{IN} = 5.0V$, $V_{OUT} = 1.8V$)**Figure 3-16.** Switch Frequency vs. R_{LPF} Resistance ($V_{IN} = 5.0V$, $V_{OUT} = 2.5V$)

Figure 3-17. Max. Output Current @ 110°C Case Temp. (1.0V V_{OUT})

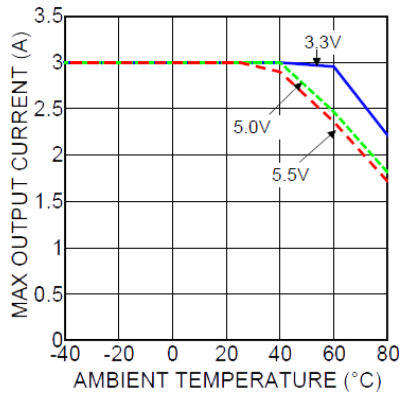


Figure 3-18. Max. Output Current @ 110°C Case Temp. (1.2V V_{OUT})

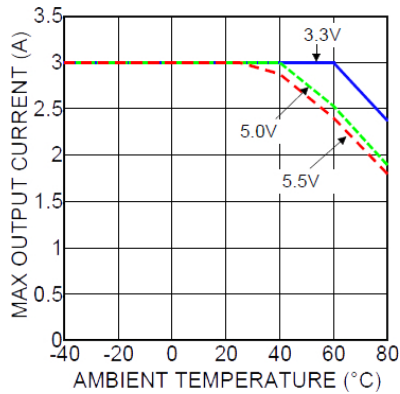


Figure 3-19. Max. Output Current @ 110°C Case Temp. (1.8V V_{OUT})

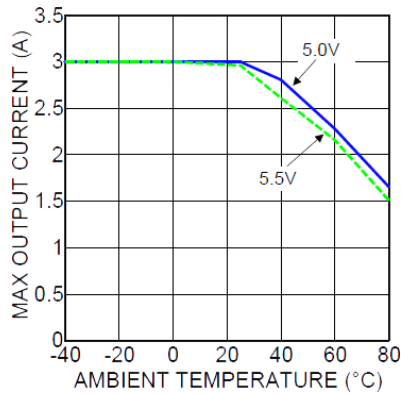
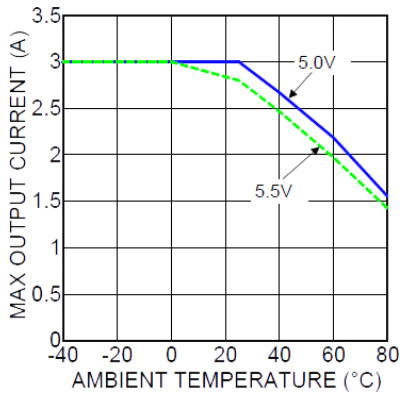


Figure 3-20. Max. Output Current @ 110°C Case Temp. (2.5V V_{OUT})



4. Functional Characteristics

$V_{IN} = 3.3V$, $V_{OUT} = 1.8V$, $C_{OUT} = 10\mu F$, Inductor = 470 nH; $R_{LPF} = 25\text{ k}\Omega$, $I_{OUT} = 100\text{ mA}$, unless noted.

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Figure 4-1. Enable Turn-On

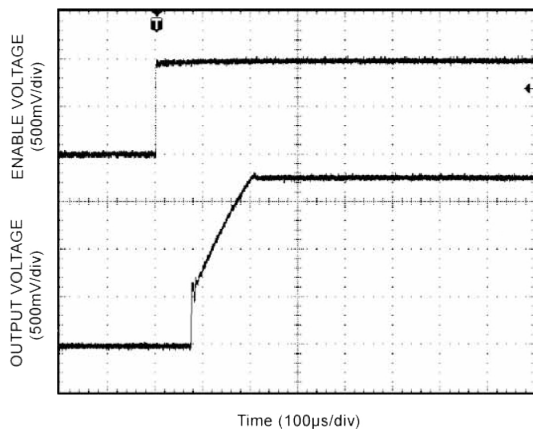


Figure 4-2. Line Transient

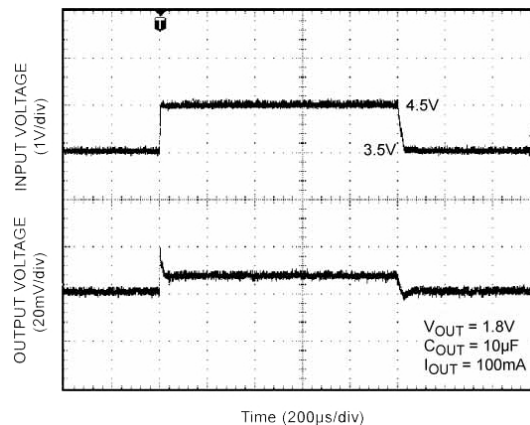


Figure 4-3. Load Transient 2A

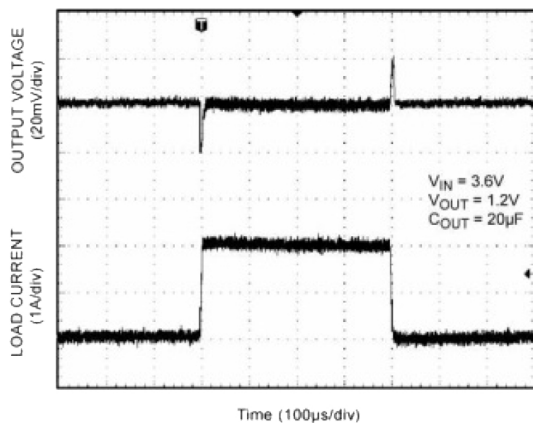


Figure 4-4. Load Transient 3A

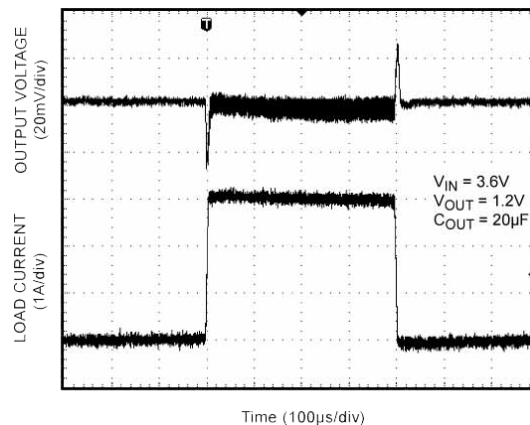
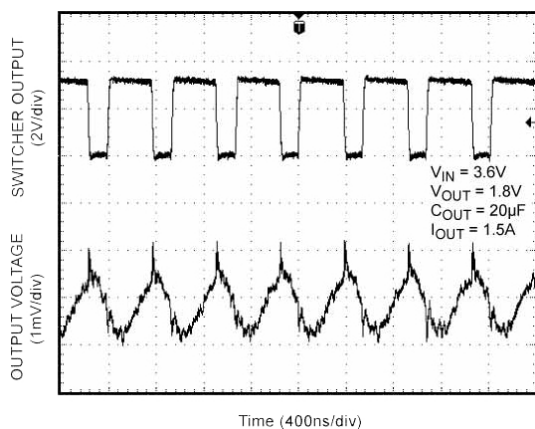


Figure 4-5. Output Noise

5. EMI Performance

$V_{OUT} = 1.8V$, $I_{OUT} = 1.2A$.

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Figure 5-1. EMI Test - Horizontal Front

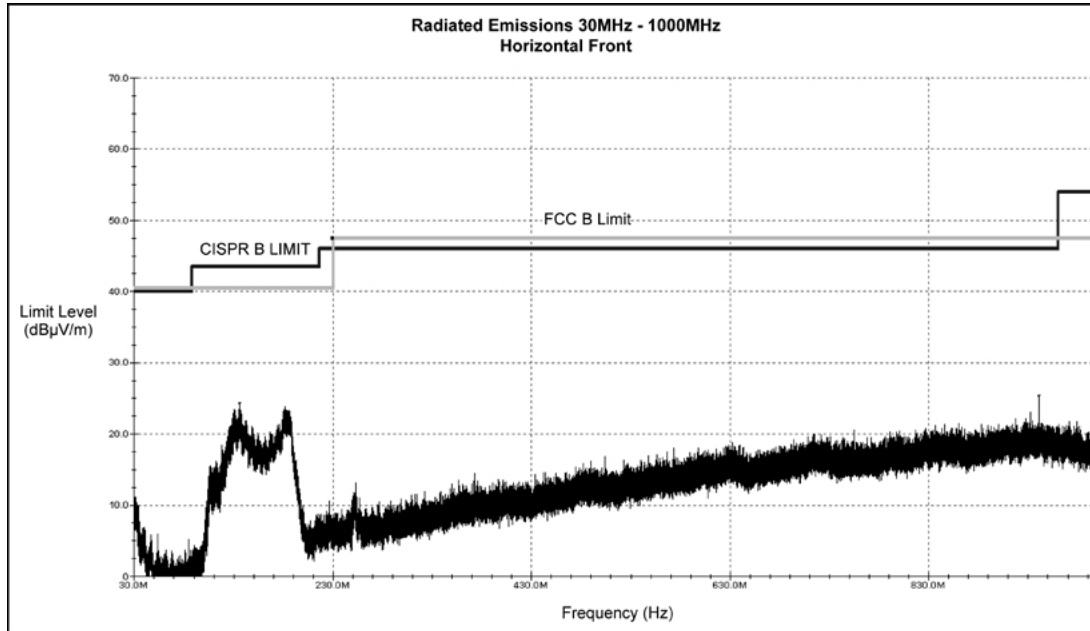
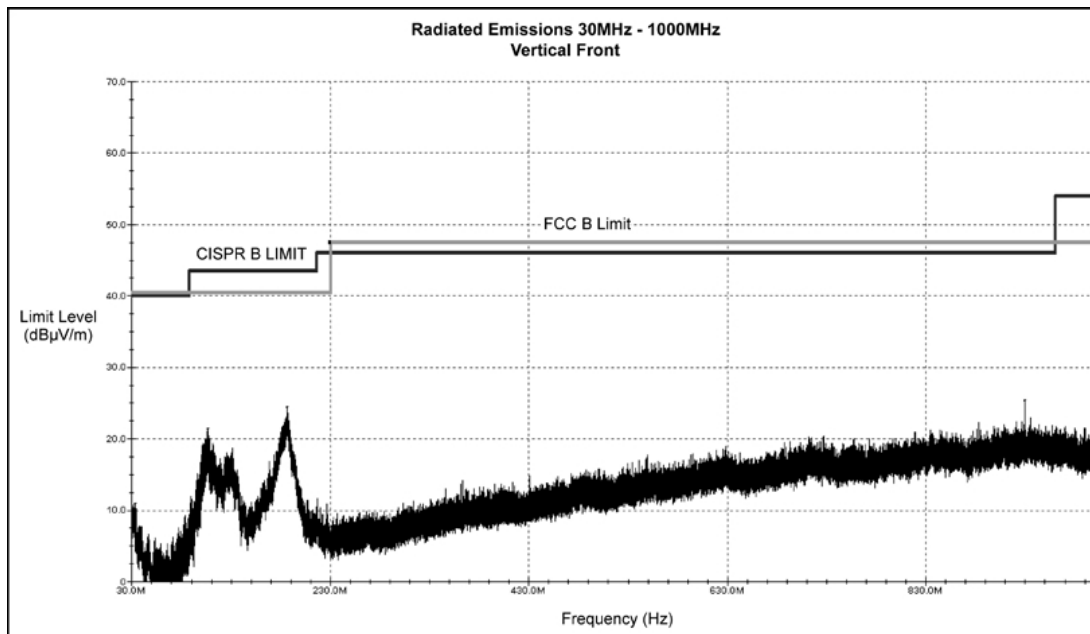


Figure 5-2. EMI Test - Vertical Front



6. Application Information

6.1. Enable Input

The MIC38300 features a TTL/CMOS compatible positive logic enable input for on/off control of the device. High enables the regulator while low disables the regulator. In shutdown the regulator consumes very little current (only a few microamperes/ μA of leakage). For simple applications the enable (EN) can be connected to V_{IN} (IN).

6.2. Input Capacitor

PVIN provides power to the MOSFETs for the switch mode regulator section and the gate drivers. Due to the high switching speeds, a 10 μF capacitor is recommended close to PVIN and the power ground (PGND) pin for bypassing.

Analog V_{IN} (AVIN) provides power to the analog supply circuitry. Careful layout should be considered to ensure high-frequency switching noise caused by PVIN is reduced before reaching AVIN. A 1 μF capacitor as close to AVIN as possible is recommended.

6.3. Output Capacitor

The MIC38300 requires an output capacitor for stable operation. As a μCap LDO, the MIC38300 can operate with ceramic output capacitors of 10 μF or greater. Values of greater than 10 μF improve transient response and noise reduction at high frequency. X7R/X5R dielectric-type ceramic capacitors are recommended because of their superior temperature performance. X7R-type capacitors change capacitance by 15% over their operating temperature range and are the most stable type of ceramic capacitors.

Larger output capacitances can be achieved by placing tantalum or aluminum electrolytics in parallel with the ceramic capacitor. For example, a 100 μF electrolytic in parallel with a 10 μF ceramic can provide the transient and high frequency noise performance of a 100 μF ceramic at a significantly lower cost. Specific undershoot/overshoot performance will depend on both the values and ESR/ESL of the capacitors.

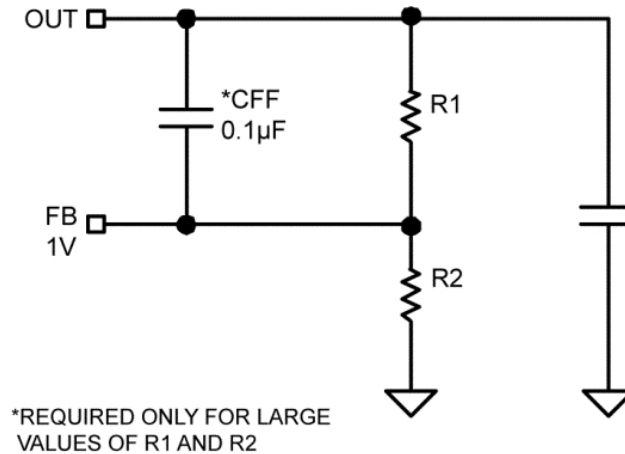
For less than 5 mV noise performance at higher current loads, 20 μF capacitors are recommended at LDOIN and LDOOUT.

6.4. Low Pass Filter Pin

The MIC38300 features a Low Pass Filter (LPF) pin for adjusting the switcher frequency. By tuning the frequency, the user can further improve output ripple without losing efficiency. Adjusting the frequency is accomplished by connecting a resistor between the LPF and SW pins. A small value resistor would increase the frequency while a larger value resistor decreases the frequency. Recommended R_{LPF} value is 25 k Ω . Please see Figure 3-12 to Figure 3-16 in the [Typical Characteristics](#) section for more details.

6.5. Adjustable Regulator Design

The adjustable MIC38300 output voltage can be programmed from 1V to 5.0V using a resistor divider from output to the FB pin. Resistors can be quite large, up to 100 k Ω because of the very high input impedance and low bias current of the sense amplifier. For large value resistors (>50 k Ω) R1 should be bypassed by a small capacitor ($C_{\text{FF}} = 0.1 \mu\text{F}$ bypass capacitor) to avoid instability due to phase lag at the ADJ/SNS input.

Figure 6-1. Adjustable Regulator with Resistors

The output resistor divider values are calculated by the equation below:

Equation 6-1. Calculating Output Resistor Divider Values

$$V_{OUT} = 1V \left(\frac{R1}{R2} + 1 \right)$$

6.6. Efficiency Considerations

Efficiency is defined as the amount of useful output power, divided by the amount of power supplied.

Equation 6-2. Calculating Efficiency

$$Efficiency_ \% = \left(\frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN}} \right) \times 100$$

Maintaining high efficiency serves two purposes. It reduces power dissipation in the power supply, reducing the need for heat sinks and thermal design considerations and it reduces consumption of current for battery-powered applications. Reduced current draw from a battery increases the devices operating time and is critical in handheld devices.

There are two types of losses in switching converters; DC losses and switching losses. DC losses are simply the power dissipation of I^2R . Power is dissipated in the high side switch during the on cycle. Power loss is equal to the high-side MOSFET $R_{DS(on)}$ multiplied by the switch current. During the off cycle, the low side N-channel MOSFET conducts, also dissipating power. Device operating current also reduces efficiency. The product of the quiescent (operating) current and the supply voltage is another DC loss.

Over 100 mA, efficiency loss is dominated by MOSFET $R_{DS(on)}$ and inductor losses. Higher input supply voltages will increase the gate-to-source threshold on the internal MOSFETs, reducing the internal $R_{DS(on)}$. This improves efficiency by reducing DC losses in the device. All but the inductor losses are inherent to the device. In which case, inductor selection becomes increasingly critical in efficiency calculations. As the inductors are reduced in size, the DC resistance (DCR) can become quite significant. The DCR losses can be calculated with the equation below:

Equation 6-3. Calculating DCR Losses

$$L_P_D = I_{OUT}^2 \times DCR$$

From that, the loss in efficiency due to inductor resistance can be calculated in the equation below:

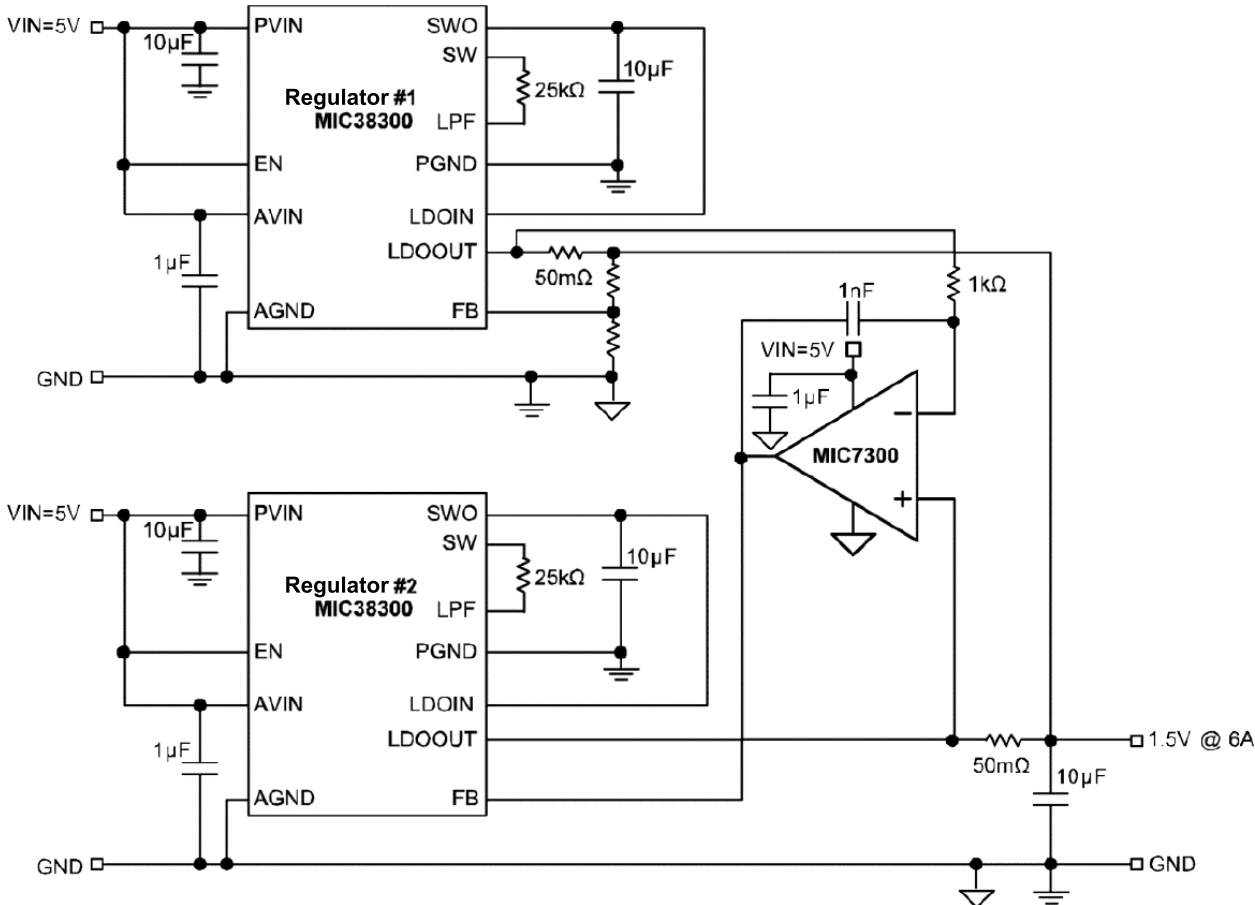
Equation 6-4. Calculating Efficiency Loss Due to Inductor Resistance

$$Efficiency_Loss = \left[1 - \left(\frac{V_{OUT} \times I_{OUT}}{V_{OUT} \times I_{OUT} + L \cdot P_D} \right) \right] \times 100$$

Efficiency loss due to DCR is minimal at light loads and gains significance as the load is increased. Inductor selection becomes a trade-off between efficiency and size in this case.

6.7. Current-Sharing Circuit

The figure below allows two MIC38300 regulators to share the load current equally.

Figure 6-2. Current-Sharing Circuit for 6A Output

Regulator #1 senses the output voltage at the load, on the other side of a current sense resistor. As the load changes, a voltage equal to the output voltage, plus the load current times the sense resistor, is developed at the V_{OUT} terminal of Regulator #1. The op-amp (MIC7300) inverting pin senses this voltage and compares it to the voltage on the V_{OUT} terminal of Regulator #2.

If the current through the current sense of Regulator #2 is less than the current through the current sense of Regulator #1, the inverting pin will be at a higher voltage than the non-inverting pin and the op-amp will drive the FB of Regulator #2 low. The low voltage sensed on Regulator #2 FB pin will drive the output up until the output voltage of Regulator #2 matches the output voltage of Regulator #1. Since V_{OUT} will remain constant and both regulator V_{OUT} terminals and sense resistances are matched, the output currents will be shared equally.

7. Package Information

7.1. Package Marking Drawings

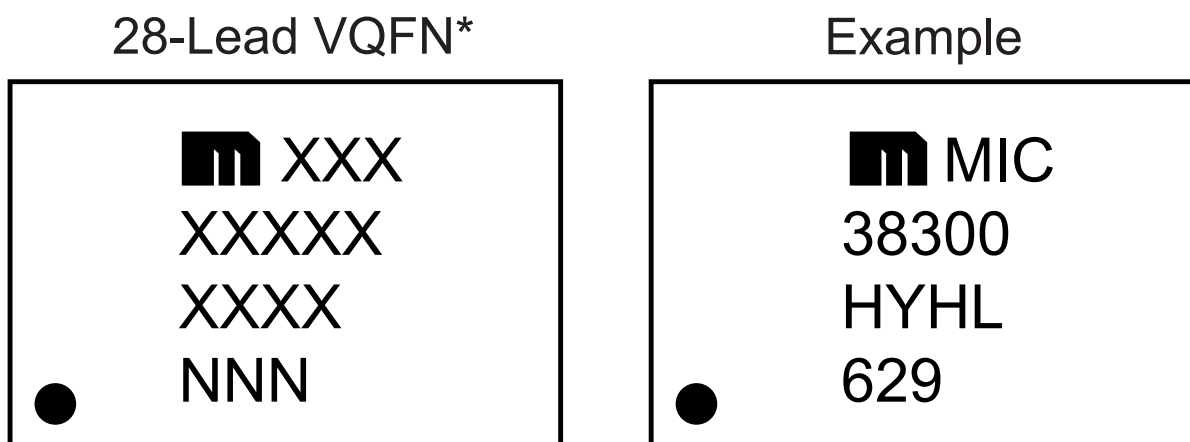


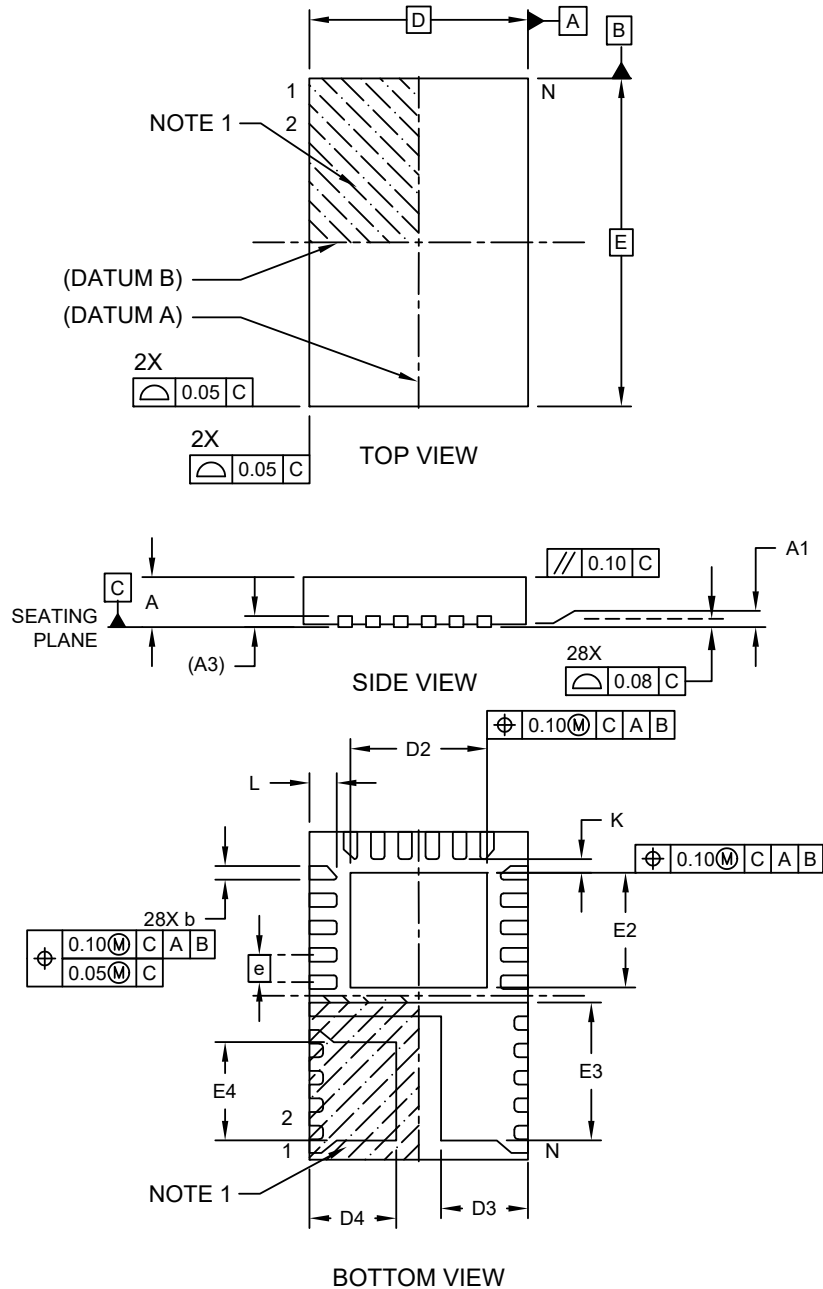
Figure 7-1. Package Marking Drawing Legend

Symbol	Definition
XX . . . X	Product code or customer-specific information. (Note 1, Note 2)
YYWW	Date code, where YY is the last 2 digits of calendar year and WW is the work week (i.e., week of January 1 is week 01). (Note 3)
M	Month of assembly (if applicable). January is represented by “A” and each month thereafter follows the order of the alphabet through “L” for December.
NNN	Alphanumeric traceability code. (Note 3, Note 4)
Ⓔ3	Pb-free JEDEC designator for Matte Tin (Sn).
*	Indicates this package is Pb-free. The Pb-free JEDEC designator (the symbol in the row above this one) can be found on the outer packaging for this package.
•, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note 1: If the full Microchip part number cannot fit on one line, it will be carried over to the next line, limiting the number of available characters for customer-specific information. The package may or may not include the corporate logo. 2: Any underbar (_) and/or overbar (¯) symbols shown in a package marking drawing may not be to scale. 3: If the full date code (YYWW) and the alphanumeric traceability code (NNN)—usually marked together on the last or only line of a package marking as the seven-character YYWWNNN—cannot fit on the package together, the codes will be truncated based on the number of available character spaces, as follows: 6 characters = YWWNNN; 5 characters = WWNNN; 4 characters = WNNN; 3 characters = NNN; 2 characters = NN; 1 character = N. 4: Some products might have a “Y” symbol at the end of the last or only line in a package marking, usually at the end of the alphanumeric traceability code (NNN or truncated versions), to indicate the product is Pb-free.	

7.2. Package Outline Drawings

28-Lead Very Thin Plastic Quad Flat, No Lead Package (P7A) - 4x6 mm Body [VQFN] With Multiple Fused Exposed Pads

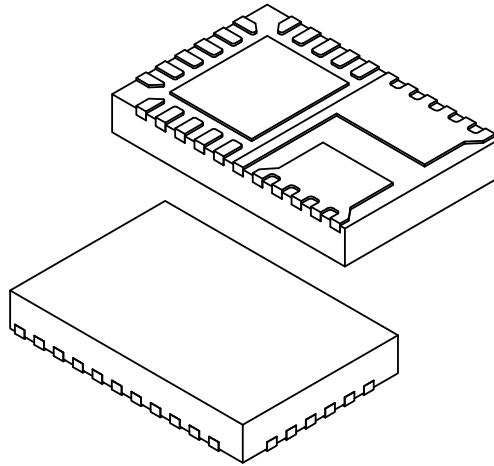
Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-1064 Rev A Sheet 1 of 2

28-Lead Very Thin Plastic Quad Flat, No Lead Package (P7A) - 4x6 mm Body [VQFN] With Multiple Fused Exposed Pads

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Terminals	N	28		
Pitch	e	0.50 BSC		
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3	0.20 REF		
Overall Length	D	4.00 BSC		
Exposed Pad Length	D2	2.45	2.50	2.55
Exposed Pad Length	D3	1.57	1.62	1.67
Exposed Pad Length	D4	1.57	1.62	1.67
Overall Width	E	6.00 BSC		
Exposed Pad Width	E2	2.05	2.10	2.15
Exposed Pad Width	E3	2.47	2.52	2.57
Exposed Pad Width	E4	1.75	1.80	1.85
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.45	0.50	0.55

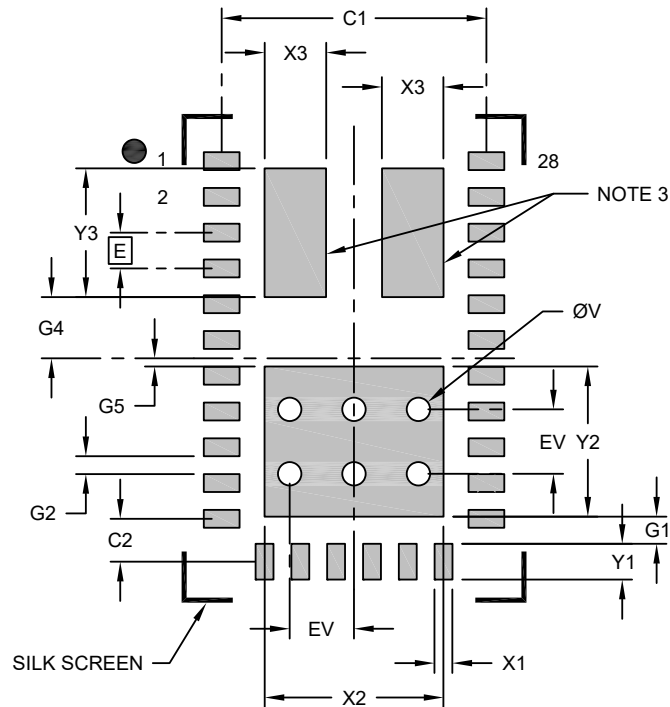
Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated
- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1064 Rev A Sheet 2 of 2

28-Lead Very Thin Plastic Quad Flat, No Lead Package (P7A) - 4x6 mm Body [VQFN] With Multiple Fused Exposed Pads

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Center Pad Width	X2			2.52
Center Pad Length	Y2			2.10
Center Pad Width	X3			0.86
Center Pad Length (X2)	Y3			1.80
Contact Pad Spacing	C1		3.70	
Contact Pad Spacing	C2		0.60	
Contact Pad Width (X28)	X1			0.27
Contact Pad Length (X28)	Y1			0.52
Contact Pad to Center Pad (X6)	G1	0.38		
Contact Pad to Contact Pad (X25)	G2	0.25		
Contact Pad to Contact Pad (X2)	G3	0.23		
Package Center to Center Pad (X2)	G4		0.86	
Package Center to Center Pad	G5		0.12	
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		0.90	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process
3. These center pads have different electrical potentials. DO NOT CONNECT TO GROUND.

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8. Product Identification System

To order or obtain information—such as on pricing or delivery—please refer to the factory or sales office.

Table 8-1. Product Number Format

XXXXXXXX	X	X	XX	-XX
Product	Output Current	Temperature Range	Package	Media Type

Table 8-2. Product Number Legend

Product:	MIC38300	High Efficiency Low Dropout Regulator
Output Current:	H	3A
Temperature Range:	Y	–40°C to 125°C
Package:	HL	28-Lead 4 mm × 6 mm VQFN
Media Type:	-TR	Tape and Reel (Base Qty. 1000)

Example: MIC38300HYHL-TR

Specs: MIC38300 - High Efficiency Low Dropout Regulator, 3A Output Current, –40°C to 125°C Temperature Range, 28-Lead 4 mm × 6 mm VQFN Package, Tape and Reel (Base Qty. 1000) Media Type

Note: Other specifications might be available upon request. Please contact your Microchip sales representative for more information.

9. Revision History

The revision history describes the changes that were implemented in the document.

Revision	Date	Section	Description
A	05/2026	—	Initial release of this document. (Note that this product is end-of-life.)

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