

6-Output SPI/I²C ePPS-Capable CMOS Fanout Buffer

Features

- **One CMOS Input**
 - Any input frequency up to 250 MHz
- **Six CMOS Outputs**
 - Output power supply pins support CMOS signal swing from 1.5V to 3.3V
 - Output enable/disable
 - Output polarity control
 - Output drive strength adjustment

General Features

- SPI or I²C processor interface
- Tiny 5 mm x 5 mm VQFN package

Applications

- CMOS signal fanout up to 250 MHz
- Supports clock, data, or ePPS signals
- Fanout and signal format conversion in a wide variety of equipment types

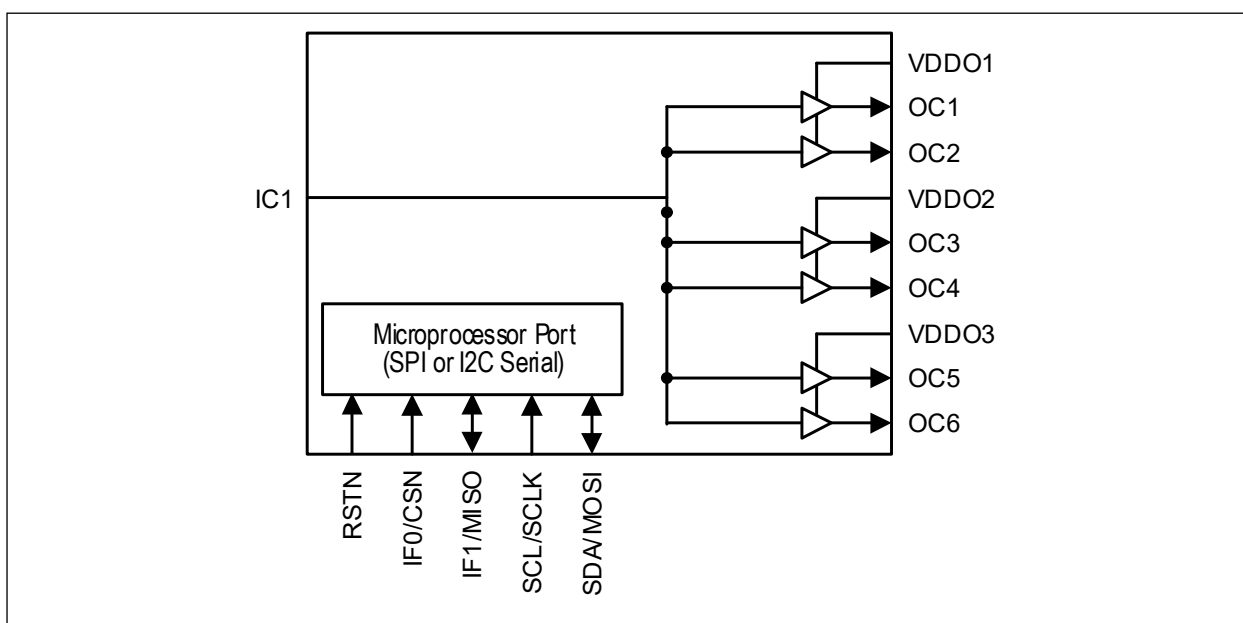


FIGURE 0-1: Functional Block Diagram.

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NOTES:

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1.0 PIN DIAGRAM

The ZL40255A is packaged in a 5 mm x 5 mm, 32-lead VQFN.

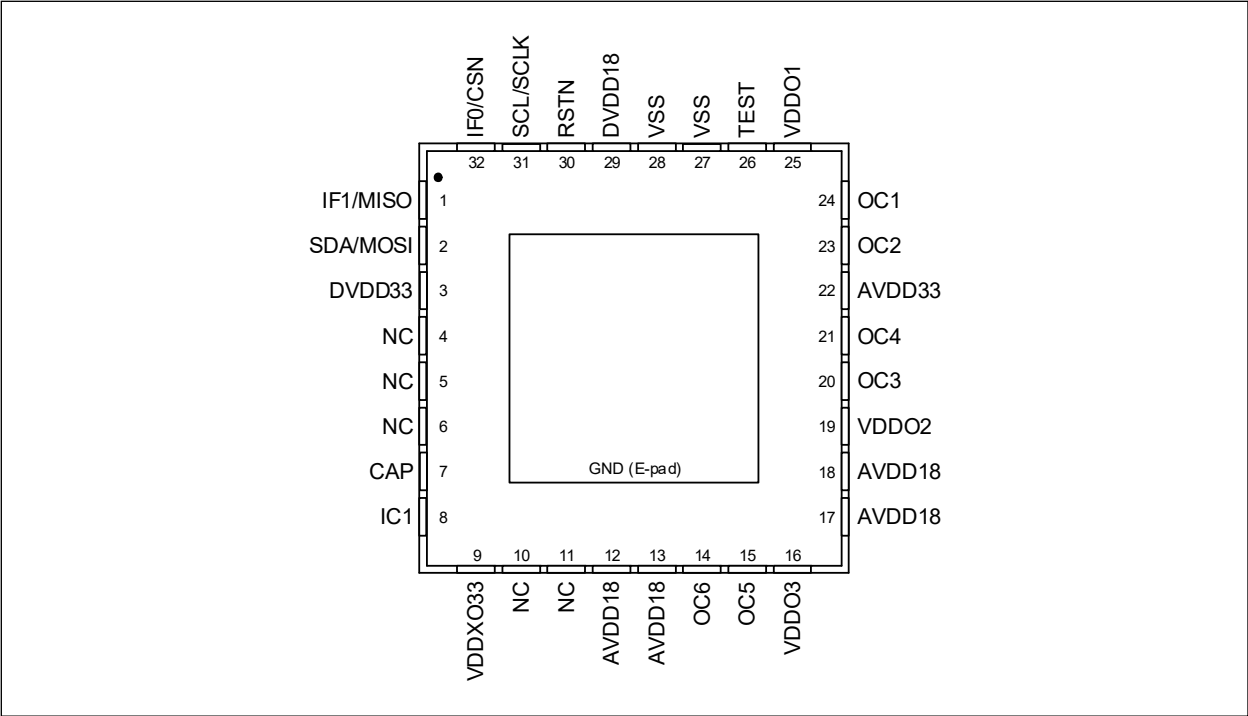


FIGURE 1-1: 32-Lead 5 mm x 5 mm VQFN

2.0 PIN DESCRIPTIONS

All device inputs and outputs are LVCMOS unless described otherwise. The Type column uses the following symbols: I – input, I_{PU} – input with 50 kΩ internal pull-up resistor, O – output, A – analog, P – power supply pin. All GPIO and SPI/I²C interface pins have Schmitt-trigger inputs and have output drivers that can be disabled (high impedance).

TABLE 2-1: PIN DESCRIPTION

Pin Number	Pin Name	Type	Description
8 7	IC1 CAP	I	Input Clock Pin, Capacitor Pin For input signal amplitude >2.5V, connect the signal directly to IC1. For input signal amplitude ≤2.5V, AC-coupling the signal to IC1 is recommended. Connect the CAP pin to a capacitor (0.1 μF or 0.01 μF) to VSS. The IC1 and CAP pins are internally biased to approximately 1.3V. Treat the CAP pin as a sensitive node; minimize stubs; do not connect to anything else. A differential signal can be connected to IC1 by AC-coupling the POS trace to IC1 and terminating the signal on the driver side of the coupling cap.
24 23 20 21 15 14	OC1 OC2 OC3 OC4 OC5 OC6	O	Output Clock Pins CMOS. Programmable drive strength. See Table 5-6 for electrical specifications for interfacing to CMOS inputs on neighboring devices.
30	RSTN	I _{PU}	Reset (Active Low) When this global asynchronous reset is pulled low, all internal circuitry is reset to default values. The device is held in reset as long as RSTN is low. See Section 3.5 .
26	TEST	I/O	Factory Test On the rising edge of RSTN, the pin behaves as TEST. Factory test mode is enabled when TEST is high. For normal operation TEST must be low on the rising edge of RSTN.
32	IF0/CSN	I/O	Interface Mode 0/SPI Chip Select (Active Low) <i>Interface Mode:</i> On the rising edge of RSTN, the pin behaves as IF0 and, together with IF1, specifies the interface mode for the device. See Section 3.1 . <i>SPI Chip Select:</i> After reset, this pin is CSN. When the device is configured as a SPI client, an external SPI host must assert (low) CSN to access device registers.
31	SCL/SCLK	I/O	I²C Clock/SPI Clock <i>I²C Clock:</i> When the device is configured as an I ² C client, an external I ² C host must provide the I ² C clock signal on the SCL pin. Note that I ² C requires an external pull-up resistor on this signal. See the I ² C specification for details. <i>SPI Clock:</i> When the device is configured as a SPI client, an external SPI host must provide the SPI clock signal on SCLK.
1	IF1/MISO	I/O	Interface Mode 1/SPI Host-In-Client-Out (MISO) <i>Interface Mode:</i> On the rising edge of RSTN, the pin behaves as IF1 and, together with IF0, specifies the interface mode for the device. See Section 3.1 . <i>SPI MISO:</i> After reset, this pin is MISO. When the device is configured as a SPI client, the device outputs data to an external SPI host on MISO during SPI read transactions.

TABLE 2-1: PIN DESCRIPTION (CONTINUED)

Pin Number	Pin Name	Type	Description
2	SDA/MOSI	I/O	I²C Data/SPI Host-Out-Client-In (MOSI) <i>I²C Data:</i> When the device is configured as an I ² C client, SDA is the bidirectional data line between the device and an external I ² C host. Note that I ² C requires an external pull-up resistor on this signal. See the I ² C specification for details. <i>SPI MOSI:</i> When the device is configured as a SPI client, an external SPI host sends commands, addresses, and data to the device on MOSI.
12 13 17 18	AVDD18	P	Analog Power Supply. 1.8V $\pm$ 5%.
22	AVDD33	P	Analog Power Supply. 3.3V $\pm$ 5%.
29	DVDD18	P	Digital Power Supply. 1.8V $\pm$ 5%.
3	DVDD33	P	Digital Power Supply. 3.3V $\pm$ 5%.
25	VDDO1	P	Output OC1 and OC2 Power Supply. 1.5V to 3.3V $\pm$ 5%.
19	VDDO2	P	Output OC3 and OC4 Power Supply. 1.5V to 3.3V $\pm$ 5%.
16	VDDO3	P	Output OC5 and OC6 Power Supply. 1.5V to 3.3V $\pm$ 5%.
9	VDDXO33	P	Analog Power Supply. 3.3V $\pm$ 5%.
27, 28	VSS	I/O	Ground. 0V.
ePad	VSS	P	Ground. 0V.
4, 5, 6, 10, 11	NC	--	No Connect. Do not connect anything to these pins.

3.0 FUNCTIONAL DESCRIPTION

3.1 Pin-Controlled Automatic Configuration at Reset

The device configuration is determined at reset (i.e. on the rising edge of RSTN) by the signal levels on three device pins: TEST, IF1/MISO, and IF0/CSN. For these pins, the first name (IF1, IF0) indicates their function when they are sampled by the rising edge of the RSTN pin. The second name, if any, refers to their function after reset. The values of these pins are latched into the [CFGSR](#) register when RSTN goes high. To ensure the device properly samples the reset values of these pins, the following guidelines should be followed:

1. Any pull-up or pull-down resistors used to set the value of these pins at reset should be 1 kΩ.
2. RSTN must be asserted at least as long as specified in [Section 3.5](#).

The IF[1:0] pins specify the processor interface mode and the I²C client address.

IF1	IF0	Processor Interface
0	0	I ² C, client address 10110 00
0	1	I ² C, client address 10110 01
1	0	I ² C, client address 10110 10
1	1	SPI client

3.2 Input Signal Enable/Disable

Input clock IC1 is enabled by setting the enable bit in the [ICEN](#) register. The power consumed by the IC1 receiver is shown in [Table 5-3](#). The electrical specifications are listed in [Table 5-5](#).

3.3 Output Clock Configuration

The device has six output clock pins arranged in three pairs: OC1 and OC2, OC3 and OC4, OC5 and OC6.

Using the [OCxCR2.OCSTF](#) register field, each output pair can be disabled or configured as one or two CMOS outputs. When an output is disabled, it is high impedance and the output driver is in a low-power state. In CMOS mode, the second output in the pair can be disabled, in phase, or inverted versus the first output in the pair. The clock to the output driver can be inverted by setting [OCxCR2.POL](#)=1. The output driver can be set to any of four drive strengths using [OCxCR2.DRIVE](#).

Each output pair has its own power supply pin to allow CMOS signal swing from 1.5V to 3.3V for glueless interfacing to neighboring components.

3.4 Microprocessor Interface

The device can communicate over a SPI interface or an I²C interface.

[Section 3.1](#) describes reset pin settings required to configure the device for these interfaces.

3.4.1 SPI CLIENT

The device can present a SPI client port on the CSN, SCLK, MOSI, and MISO pins. SPI is a widely used host/client bus protocol that allows a host and one or more clients to communicate over a serial bus. SPI hosts are typically microprocessors, ASICs, or FPGAs. Data transfers are always initiated by the host, which also generates the SCLK signal. The device receives serial data on the MOSI (Host Out Client In) pin and transmits serial data on the MISO (Host In Client Out) pin. MISO is high impedance except when the device is transmitting data to the bus host.

Bit Order. The register address and all data bytes are transmitted most significant bit first on both MOSI and MISO.

Clock Polarity and Phase. The device latches data on MOSI on the rising edge of SCLK and updates data on MISO on the falling edge of SCLK. SCLK does not have to toggle between accesses, i.e., when CSN is high.

Device Selection. Each SPI device has its own chip-select line. To select the device, the bus host drives its CSN pin low.

Command and Address. After driving CSN low, the bus host transmits an 8-bit command followed by a 16-bit register address. The available commands are shown below.

TABLE 3-1: SPI COMMANDS

Command	Hex	Bit Order, Left to Right
Write	0x02	0000 0010
Read	0x03	0000 0011

Read Transactions. After driving CSN low, the bus host transmits the read command followed by the 16-bit address. The device then responds with the requested data byte on MISO, increments its address counter, and prefetches the next data byte. If the bus host continues to demand data, the device continues to provide the data on MISO, increment its address counter, and prefetch the following byte. The read transaction is completed when the bus master drives CSN high. See [Figure 3-1](#).

Write Transactions. After driving CSN low, the bus host transmits the write command followed by the 16-bit register address followed by the first data byte to be written. The device receives the first data byte on MOSI, writes it to the specified register, increments its internal address register, and prepares to receive the next data byte. If the host continues to transmit, the device continues to write the data received and increment its address counter. The write transaction is completed when the bus host drives CSN high. See [Figure 3-2](#).

Early Termination of Bus Transactions. The bus host can terminate SPI bus transactions at any time by pulling CSN high. In response to early terminations, the device resets its SPI interface logic and waits for the start of the next transaction. If a write transaction is terminated prior to the SCLK edge that latches the least significant bit of a data byte, the data byte is not written.

Design Option: Wiring MOSI and MISO Together. Because communication between the bus host and the device is half-duplex, the MOSI and MISO pins can be wired together externally to reduce wire count. To support this option, the bus host must not drive the MOSI/MISO line when the device is transmitting.

AC Timing. See [Table 5-8](#) and [Figure 5-2](#) for AC timing specifications for the SPI interface.

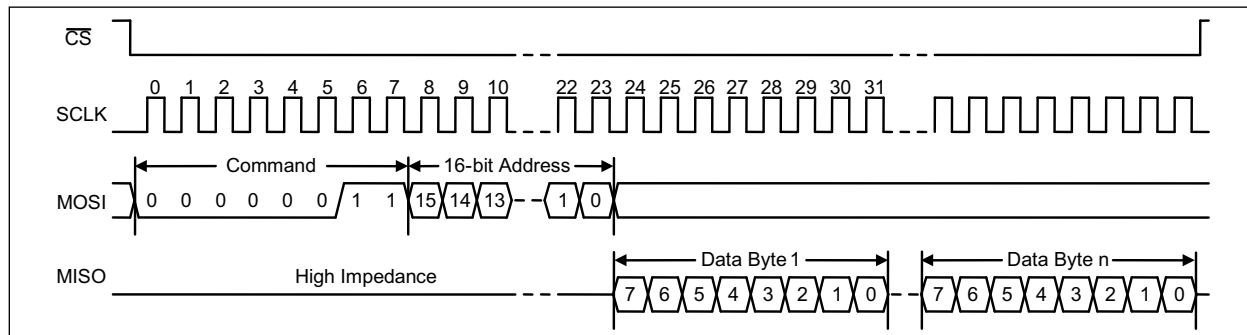


FIGURE 3-1: SPI Read Transaction Functional Timing.

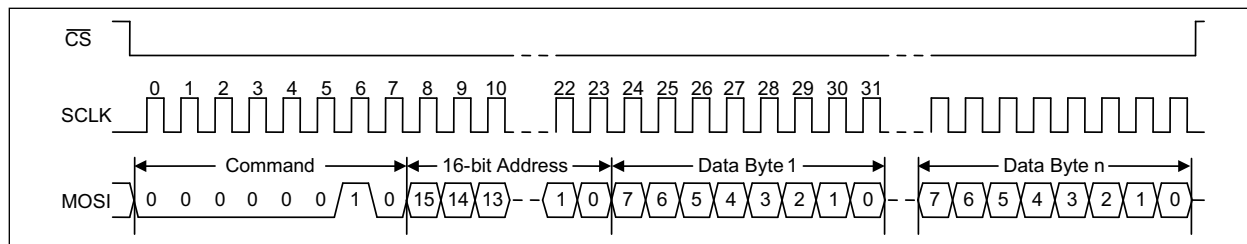


FIGURE 3-2: SPI Write Transaction Functional Timing.

3.4.2 I²C CLIENT

The device can present a fast-mode (400 kbit/s) I²C client port on the SCL and SDA pins. I²C is a widely used host/client bus protocol that allows one or more hosts and one or more clients to communicate over a two-wire serial bus. I²C hosts are typically microprocessors, ASICs, or FPGAs. Data transfers are always initiated by the host, which also generates the SCL signal. The device is compliant with version 2.1 of the I²C specification.

The I²C interface on the device is a protocol translator from external I²C transactions to internal SPI transactions. This explains the slightly increased protocol complexity described in the paragraphs that follow.

Read Transactions. The bus host first does an I²C write to the device. In this transaction, three bytes are written: the SPI Read command (see Table 3-1), the upper byte of the register address, and the lower byte of the register address. The bus host then does an I²C read. During each acknowledge (A) bit the device fetches data from the read address and then increments the read address. The device then transmits the data to the bus host during the next 8 SCL cycles. The bus host terminates the read with a not-acknowledge (NA) followed by a STOP condition (P). See Figure 3-3. Note: If the I²C write is separated in time from the I²C read by other I²C transactions, then the device only outputs the data value from the first address and repeats that same data value after each acknowledge (A) generated by the bus host.

Write Transactions. The bus host does an I²C write to the device. The first three bytes of this transaction are the SPI Write command (see Table 3-1), the upper byte of the register address, and the lower byte of the register address. Subsequent bytes are data bytes to be written. After each data byte is received, the device writes the byte to the write address and then increments the write address. The bus host terminates the write with a STOP condition (P). See Figure 3-4.

I²C Features Not Supported by the Device. The I²C specification has several optional features that are not supported by the device. These are: 3.4 Mbit/s high-speed mode (Hs-mode), 10-bit device addressing, general call address, software reset, and device ID. The device does not hold SCL low to force the host to wait.

I²C Client Address. The device's 7-bit client address can be pin-configured for any of three values as shown in the table in Section 3.1.

Bit Order. The I²C specification requires device address, register address, and all data bytes to be transmitted most significant bit first on the SDA signal.

Note: As required by the I²C specification, when power is removed from the device, the SDA and SCL pins are left floating so they don't obstruct the bus lines.

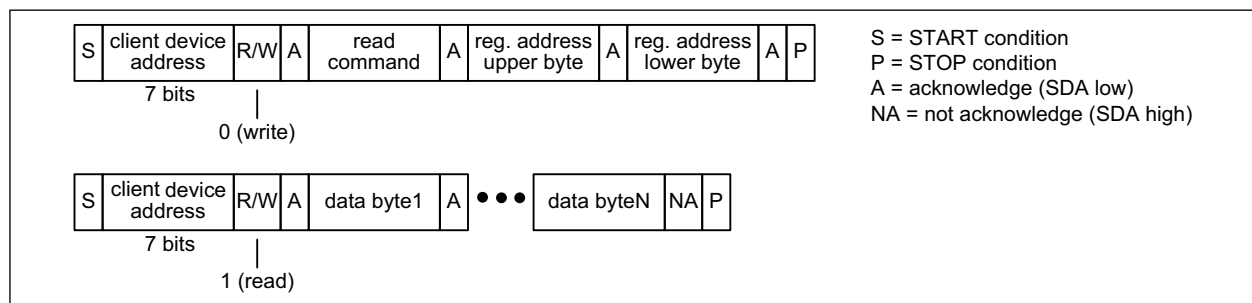


FIGURE 3-3: I²C Read Transaction Functional Timing.

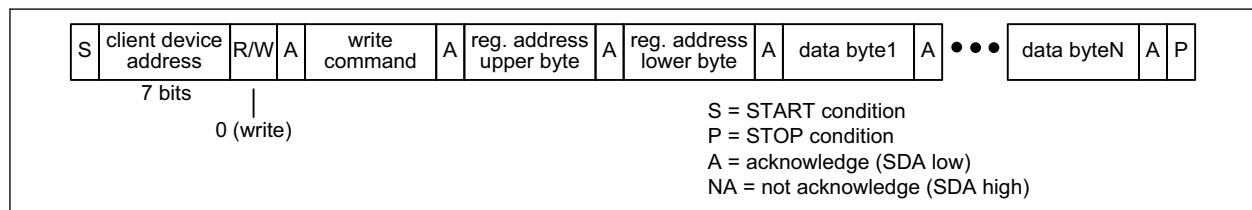


FIGURE 3-4: I²C Write Transaction Functional Timing.

Note: In Figure 3-3 and Figure 3-4, a STOP condition (P) immediately followed by a START condition (S) can be replaced by a repeated START condition (Sr) as described in the I²C specification.

3.5 Reset Logic

The device has two reset controls: the RSTN pin and the RST bit in MCR1. The RSTN pin asynchronously resets the entire device. When the RSTN pin is low, all internal registers are reset to their default values. The RSTN pin must be asserted once after power-up. At initial power-up, reset should be asserted for at least 1 μ s. During operation, the RSTN assertion time can be as short as 1 μ s with one important exception:

- Consider each of these pins: TEST, and IF1/MISO. If (1) the pin could be an output driving high when RSTN is asserted, and (2) an external pull-down resistor is used to set the at-reset value of the pin, then RSTN should be asserted for 100 milliseconds.

The [MCR1](#).RST bit resets the entire device (except for the microprocessor interface and the RST bit itself), but when the RST bit is active, the register fields with pin-programmed defaults do not latch their values from, or based on, the corresponding input pins. Instead these fields are reset to the default values that were latched when the RSTN pin was last active.

3.6 Power Supply Considerations

Due to the multi-power-supply nature of the device, some I/Os have parasitic diodes between a <3.3V supply and a 3.3V supply. When ramping power supplies up or down, care must be taken to avoid forward-biasing these diodes because it could cause latch-up. Two methods are available to prevent this. The first method is to place a Schottky diode external to the device between the <3.3V supply and the 3.3V supply to force the 3.3V supply to be within one parasitic diode drop of the <3.3V supply. The second method is to ramp up the 3.3V supply first and then ramp up the <3.3V supply. In some applications, VDDOx power supply pins can be at other voltages, such as 2.5V or 1.5V. In these applications, the general solution is to ramp up the supplies in order from highest nominal to lowest nominal voltage.

3.7 Power Supply Decoupling and Layout Recommendations

Application Note ZLAN-594 describes recommended power supply decoupling and layout practices.

4.0 REGISTER DESCRIPTIONS

The device has an overall address range from 000h to 6FFh. [Table 4-1](#) shows the register map. In each register, bit 7 is the MSb and bit 0 is the LSb. Register addresses not listed and bits marked “—” are reserved and must be written with 0. Writing other values to these registers may put the device in a factory test mode resulting in undefined operation. Bits labeled “0” or “1” must be written with that value for proper operation. Register fields with underlined names are read-only fields; writes to these fields have no effect. All other fields are read-write. Register fields are described in detail in the register descriptions that follow [Table 4-1](#).

4.1 Register Types

4.1.1 STATUS BITS

Status bits are read-only and indicate the state of a signal at the time it is read. Status bits marked “—” are reserved and must be ignored.

4.1.2 CONFIGURATION FIELDS

Configuration fields are read-write. During reset, each configuration field reverts to the default value shown in the register definition. Configuration register bits marked “—” are reserved and must be written with 0.

4.2 Register Map

TABLE 4-1: REGISTER MAP

ADDR	REGISTER	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
09	MCR1	RST	—	—	—	—	—	—	—
0C	ICEN	—	—	—	—	—	—	—	IC1EN
40	CFGSR	<u>TEST</u>	—	—	—	<u>IF[1:0]</u>		—	—
201	OC1CR2	—	POL	DRIVE[1:0]		—	OCSF[2:0]		
211	OC2CR2	—	POL	DRIVE[1:0]		—	OCSF[2:0]		
221	OC3CR2	—	POL	DRIVE[1:0]		—	OCSF[2:0]		

4.3 Register Definitions

Register Name: MCR1

Register Description: Master Configuration Register 1

Register Address: 09h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name:	RST	—	—	—	—	—	—	—
Default:	0	0	0	0	0	0	0	0

Bit 7: Device Reset (RST). When this bit is high, the entire device is held in reset and all register fields, except the RST bit itself, are reset to their default states. When RST is high, the register fields with pin-programmed defaults do not latch their values from the corresponding input pins. Instead these fields are reset to the default values that were latched from the pins when the RSTN pin was last active. See [Section 3.5](#).

0 = Normal operation

1 = Reset

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Register Name: ICEN
Register Description: Input Clock Enable Register
Register Address: 0Ch

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name:	—	—	—	—	—	—	—	IC1EN
Default:	0	0	0	0	0	0	0	0

Bit 0: Input Clock 1 Enable (IC1EN). This bit enables and disables the input clock 1 differential receiver and input dividers. See [Section 3.2](#).

0 = Disabled

1 = Enabled

Register Name: CFGSR
Register Description: Configuration Status Register
Register Address: 40h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name:	TEST	—	—	—	IF[1:0]		—	—
Default:	See Below	0	0	0	See Below		0	0

Bit 7: Test Mode (TEST). This read-only bit is the latched state of the TEST/GPIO2 pin when the RSTN pin transitions high. For proper operation it should be 0. See [Section 3.1](#).

Bits 3 to 2: Interface Mode (IF[1:0]). These read-only bits are the latched state of the IF1/MISO and IF0/CSN pins when the RSTN pin transitions high. See [Section 3.1](#).

Register Name: OCxCR2

Register Description: Output Clock x Configuration Register 2

Register Address: OC1 and OC2: 201h, OC3 and OC4: 211h, OC4 and OC6: 221h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name:	—	POL	DRIVE[1:0]		—	OCSF[2:0]		
Default:	0	0	0	0	0	0	0	0

Bit 6: Clock Path Polarity (POL). The clock path to the outputs is inverted when this bit set.

Bits 5 to 4: CMOS Output Drive Strength (DRIVE[1:0]). The CMOS output drivers have four equal sections that can be enabled or disabled to achieve four different drive strengths from 1x to 4x. When the output power supply VDDOx is 3.3V or 2.5V, the user should start with 1x and only increase drive strength if the output is highly loaded and signal transition time is unacceptable. When VDDOx is 1.8V or 1.5V the user should start with 4x and only decrease drive strength if the output signal has unacceptable overshoot.

00 = 1x

01 = 2x

10 = 3x

11 = 4x

Bits 2 to 0: Output Clock Signal Format (OCSF[2:0]).

000 = Disabled (high-impedance, low power mode)

100 = Two CMOS in phase

101 = One CMOS: first OCx of the pair high impedance, second OCx of the pair enabled

110 = One CMOS: first OCx of the pair enabled, second OCx of the pair high impedance

111 = Two CMOS: second OCx of the pair inverted vs. the first OCx of the pair

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NOTES:

5.0 ELECTRICAL CHARACTERISTICS

TABLE 5-1: ABSOLUTE MAXIMUM RATINGS

(Note 1, Note 2, Note 3, Note 4)				
Parameter	Symbol	Min.	Max.	Units
Supply voltage, nominal 1.8V	VDD18	−0.3	1.98	V
Supply voltage, nominal 3.3V	VDD33	−0.3	3.63	V
Supply voltage, VDDOx (x=1,2,3)	VDDOx	−0.3	3.63	V
Voltage on IC1, any OCx pin	VANAPIN	−0.3	3.63	V
Voltage on any digital I/O pin	VDIGPIN	−0.3	5.5	V
Storage Temperature Range	T _{ST}	−55	+125	°C

- Note 1:** Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.
- 2:** Voltages are with respect to ground (VSS) unless otherwise stated.
- 3:** The typical values listed in the tables of Section 5 are not production tested.
- 4:** Specifications to −40°C and +85°C are ensured by design or characterization and not production tested.

TABLE 5-2: RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Units
Supply voltage, nominal 1.8V	VDD18	1.71	1.8	1.89	V
Supply voltage, nominal 3.3V	VDD33	3.135	3.3	3.465	V
Supply voltage, VDDOx (x=1,2,3)	VDDOx	1.425	1.5	1.575	V
		1.71	1.8	1.89	
		2.375	2.5	2.625	
		3.135	3.3	3.465	
Operating Temperature	T _A	−40	—	+85	°C

TABLE 5-3: ELECTRICAL CHARACTERISTICS: SUPPLY CURRENTS

(Note 1)						
Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Total current, all 1.8V supply pins	I _{DD18}	—	110	—	mA	Note 2
Total current, all 3.3V supply pins	I _{DD33}	—	140	—	mA	Note 2
1.8V supply current change from enabling or disabling a pair of single-ended outputs	ΔI _{DD18CMOS}	—	2	—	mA	—
VDDOx supply current change from enabling or disabling a pair of single-ended outputs	ΔI _{DD33CMOS}	—	16	—	mA	Note 3

- Note 1:** Typical values measured at 1.80V and 3.30V supply voltages and 25°C ambient temperature.
- 2:** IC1 enabled with 100 MHz 3.3V CMOS input signal. All outputs enabled, VDDOx=3.3V. CMOS outputs terminated 1 MΩ to ground.
- 3:** V_{DDOx} = 3.3V, 1x drive strength, f_O = 250 MHz, 2 pF load.

TABLE 5-4: ELECTRICAL CHARACTERISTICS: NON-CLOCK CMOS PINS

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
Input high voltage, SCL and SDA	V_{IH}	$0.7 \times V_{DD33}$	—	—	V	—
Input low voltage, SCL and SDA	V_{IL}	—	—	$0.3 \times V_{DD33}$	V	—
Input high voltage, all other digital inputs	V_{IH}	2.0	—	—	V	—
Input low voltage, all other digital inputs	V_{IL}	—	—	0.8	V	—
Input leakage current, RSTN pin	I_{ILPU}	–85	—	10	μA	Note 1
Input leakage current, all other digital inputs	I_{IL}	–10	—	10	μA	Note 1
Input capacitance	C_{IN}	—	3	10	pF	—
Input capacitance, SCL/SCLK, SDA/MOSI	C_{IN}	—	3	11	pF	—
Input hysteresis, SCL and SDA in I ² C Bus Mode	—	$0.05 \times V_{DD33}$	—	—	mV	—
Output leakage (when high impedance)	I_{LO}	–10	—	10	μA	Note 1
Output high voltage (Note 2)	V_{OH}	2.4	—	—	V	$I_O = -3.0 \text{ mA}$
Output low voltage	V_{OL}	—	—	0.4	V	$I_O = 3.0 \text{ mA}$

Note 1: $0V < V_{IN} < V_{DD33}$ for all other digital inputs.

2: V_{OH} does not apply for SCL and SDA in I²C interface mode because they are open-drain.

TABLE 5-5: ELECTRICAL CHARACTERISTICS: CLOCK INPUT

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Input voltage tolerance	V_{TOL}	0	—	VDD33	V	Note 1
Input differential voltage	$ V_{ID} $	0.1	—		V	Note 2
Input DC bias voltage (internally biased)	V_{CMI}	—	1.3	—	V	—
Input frequency	f_{IN}	9.72	—	250	MHz	Note 3
Minimum input clock high, low time	t_H/t_L	—	smaller of 3 ns or $0.3 \times 1/f_{IN}$	—	ns	—
Input resistance, to VDD18	$R_{INVDD18}$	—	50	—	k Ω	—
Input resistance, to VSS	R_{INVSS}	—	80	—	k Ω	—

- Note 1:** The device can tolerate voltages as specified in V_{TOL} with respect to VSS on its IC1 pin without being damaged.
- 2:** $V_{ID} = V_{IC1} - V_{CMI}$.
- 3:** Single-ended signals can be connected to the IC1 pin. Signals with amplitude greater than 2.5V must be DC-coupled. For signals with amplitudes less than 2.5V, Microchip recommends AC-coupling, but DC-coupling can also be used.

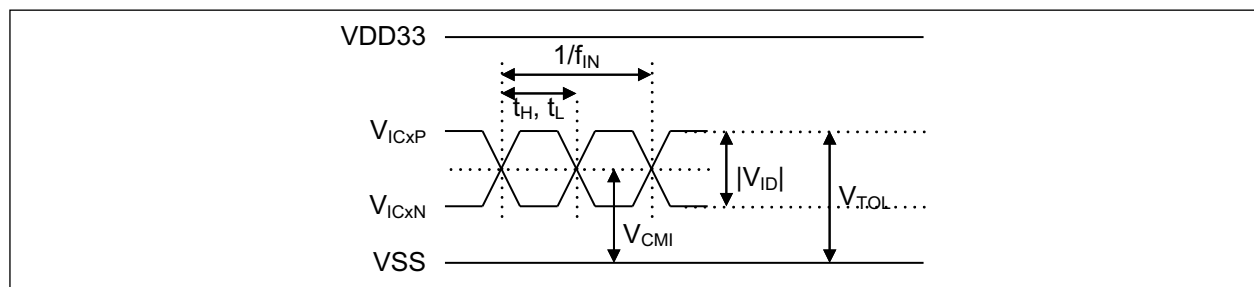


FIGURE 5-1: Electrical Characteristics: Clock Input.

TABLE 5-6: ELECTRICAL CHARACTERISTICS: CMOS CLOCK OUTPUTS

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Output frequency	f_{OCMOS}	$\ll 1$ Hz	—	250	MHz	Note 1
Output high voltage	V_{OH}	$V_{\text{DDOx}} - 0.4$	—	V_{DDOx}	V	Note 2
Output low voltage	V_{OL}	0	—	0.4	V	Note 2
Output rise/fall time, $V_{\text{DDOx}}=1.8\text{V}$, OCxCR2.DRIVE=4x	t_r/t_f	—	0.4	—	ns	2 pF load
Output rise/fall time, $V_{\text{DDOx}}=1.8\text{V}$, OCxCR2.DRIVE=4x		—	1.2	—	ns	15 pF load
Output rise/fall time, $V_{\text{DDOx}}=3.3\text{V}$, OCxCR2.DRIVE=1x		—	0.7	—	ns	2 pF load
Output rise/fall time, $V_{\text{DDOx}}=3.3\text{V}$, OCxCR2.DRIVE=1x		—	2.2	—	ns	15 pF load
Output current when output disabled	—	—	10	—	μA	OCxCR2.OCSF=0

- Note 1:** Minimum output frequency is a function of input frequency and device divider values and is ensured by design.
- 2:** For $V_{\text{DDOx}} = 3.3\text{V}$ and [OCxCR2.DRIVE=1x](#), $I_{\text{O}} = 4$ mA. For $V_{\text{DDOx}} = 1.5\text{V}$ and [OCxCR2.DRIVE=4x](#), $I_{\text{O}} = 8$ mA.

TABLE 5-7: ELECTRICAL CHARACTERISTICS: JITTER AND SKEW SPECIFICATIONS

Parameter	Min.	Typ.	Max.	Units	Notes
Additive Jitter, 100 MHz	—	400	—	f_{SRMS}	12 kHz to 20 MHz, Note 1 and Note 4
Input-to-Output Propagation Delay	—	3.9	—	ns	Note 3
Output-to-Output Skew	—	<75	—	ps	Note 2

- Note 1:** 3x output drive strength
- 2:** Only applies for outputs that have the same signal format, VDDO voltage, drive strength, and load/termination.
- 3:** Outputs unloaded
- 4:** Tested with input clock slew rate of 3V/ns.

TABLE 5-8: SPI CLIENT INTERFACE TIMING

Characteristics (Note 1, Note 2, Note 3)	Symbol	Min.	Typ.	Max.	Units
SCLK frequency	f_{BUS}	—	—	10	MHz
SCLK cycle time	t_{CYC}	100	—	—	ns
CSN setup to first SCLK edge	t_{SUC}	50	—	—	ns
CSN hold time after last SCLK edge	t_{HDC}	50	—	—	ns
CSN high time	t_{CSH}	50	—	—	ns
SCLK high time	t_{CLKH}	40	—	—	ns
SCLK low time	t_{CLKL}	40	—	—	ns
MOSI data setup time	t_{SUI}	10	—	—	ns
MOSI data hold time	t_{HDI}	10	—	—	ns
MISO enable time from SCLK edge	t_{EN}	0	—	—	ns
MISO disable time from CSN high	t_{DIS}	—	—	80	ns
MISO data valid time	t_{DV}	—	—	40	ns
MISO data hold time from SCLK edge	t_{HDO}	0	—	—	ns
CSN, MOSI input rise time, fall time	t_r/t_f	—	—	10	ns

Note 1: All timing is specified with 100 pF load on all SPI pins.

Note 2: All parameters in this table are ensured by design or characterization.

Note 3: See Figure 5-2.

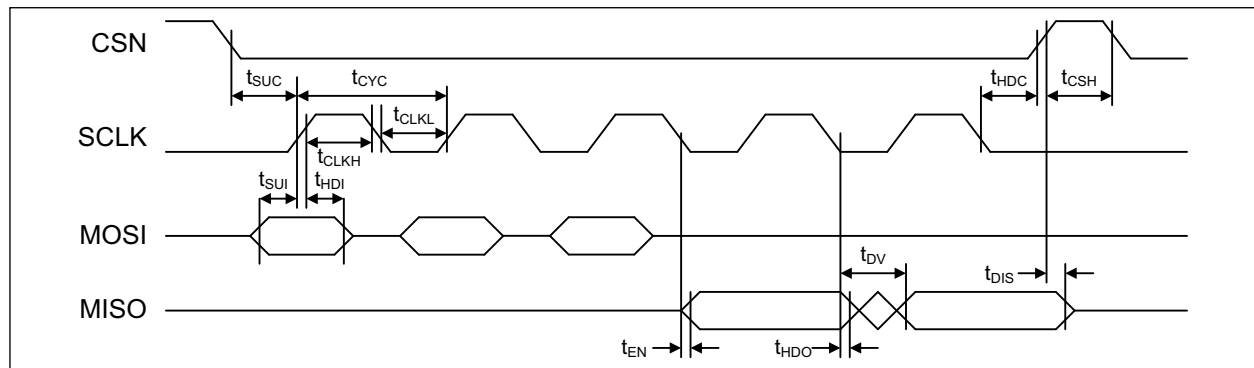


FIGURE 5-2: SPI Client Interface Timing.

TABLE 5-9: I²C CLIENT INTERFACE TIMING

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
SCL clock frequency	f_{SCL}	—	—	400	kHz	—
Hold time, START condition	$t_{HD:STA}$	0.6	—	—	μs	—
Low time, SCL	t_{LOW}	1.3	—	—	μs	—
High time, SCL	t_{HIGH}	0.6	—	—	μs	—
Setup time, START condition	$t_{SU:STA}$	0.6	—	—	μs	—
Data hold time	$t_{HD:DAT}$	0	—	0.9	μs	Note 2, Note 3
Data setup time	$t_{SU:DAT}$	100	—	—	ns	—
Rise time	t_R	—	—	—	ns	Note 4
Fall time	t_F	20 + 0.1C _b	—	300	ns	C _b is cap. of one bus line
Setup time, STOP condition	$t_{SU:STO}$	0.6	—	—	μs	—
Bus free time between STOP/START	t_{BUF}	1.3	—	—	μs	—
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	0	—	50	ns	—

Note 1: The timing parameters in this table are specifically for 400 kbps Fast Mode. Fast Mode devices are downward-compatible with 100 kbps Standard Mode I²C bus timing. All parameters in this table are ensured by design or characterization. All values referred to $V_{IH(MIN)}$ and $V_{IL(MAX)}$ levels (see Table 5-4).

- 2: The device internally provides a hold time of at least 300 ns for the SDA signal (referred to the $V_{IH(MIN)}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL. Other devices must provide this hold time as well per the I²C specification.
- 3: The I²C specification indicates that the maximum $t_{HD:DAT}$ spec only has to be met if the device does not stretch the low period (t_{LOW}) of the SCL signal. The device does not stretch the low period of the SCL signal.
- 4: Determined by choice of pull-up resistor.

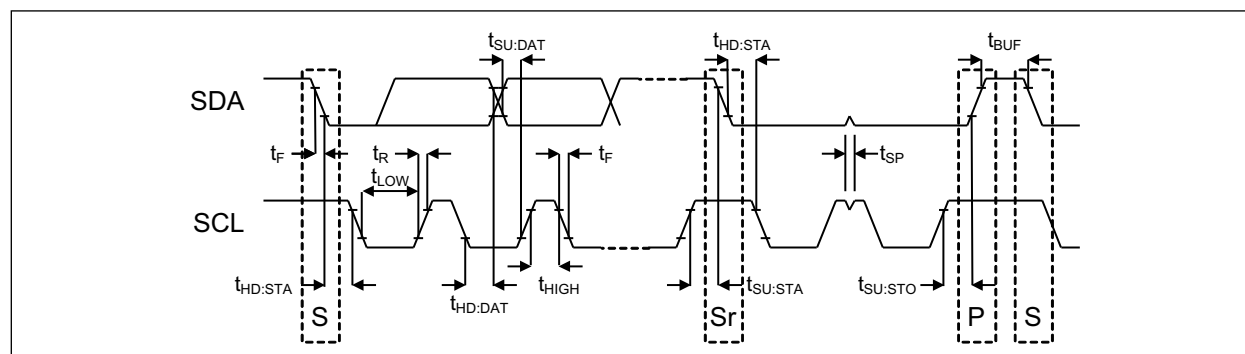
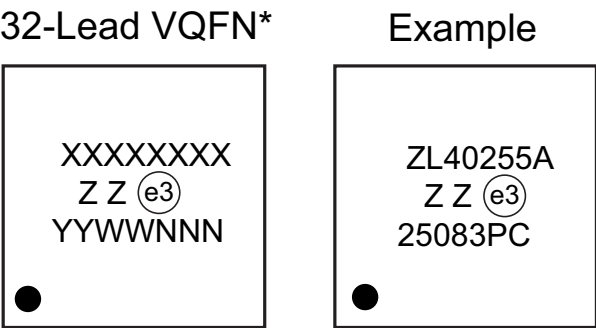


FIGURE 5-3: I²C Client Interface Timing.

6.0 PACKAGE AND THERMAL INFORMATION

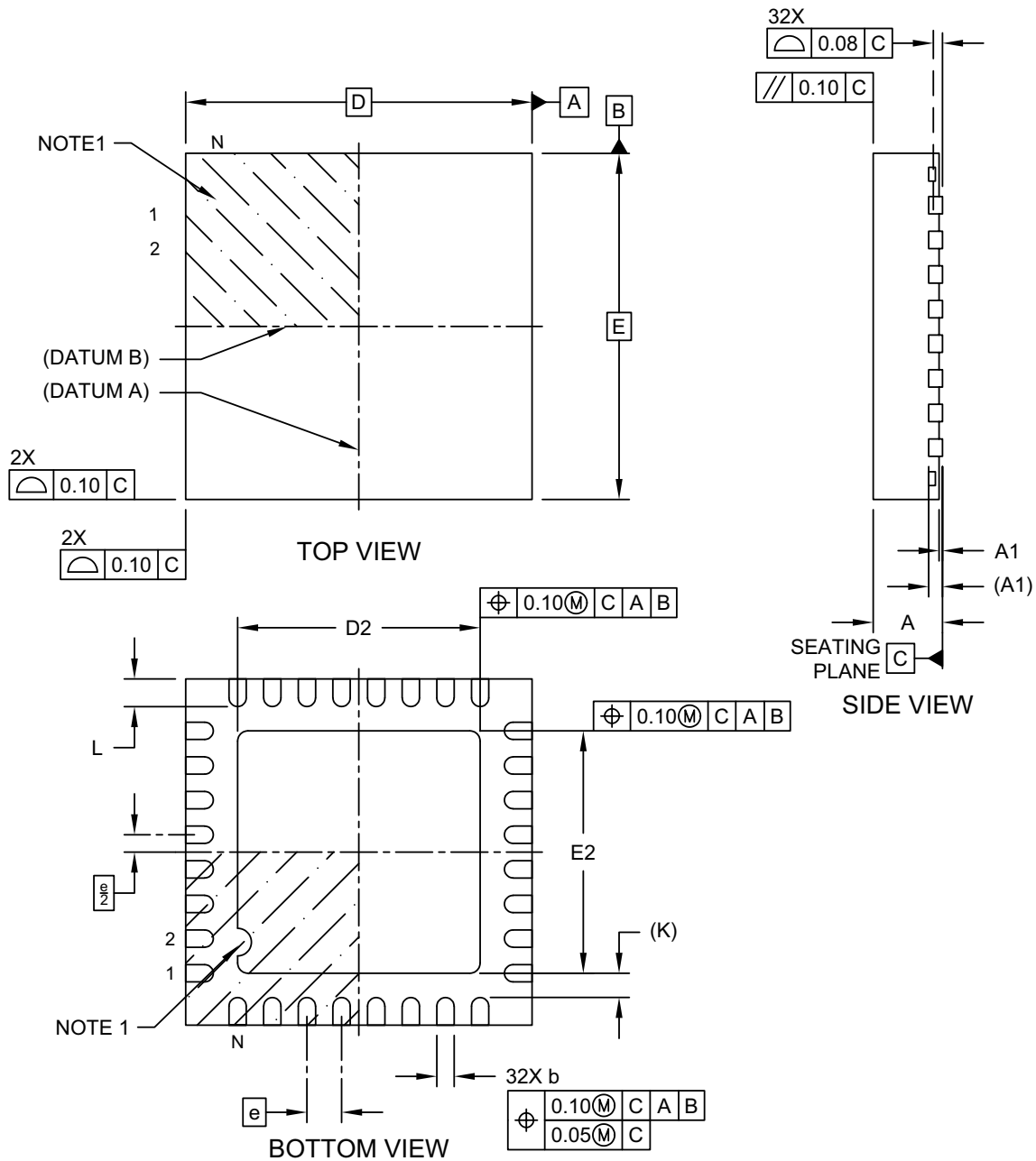
6.1 Package Marking Information



Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	•, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.	
	Underbar (_) and/or Overbar (¯) symbol may not be to scale.	

32-Lead Very Thin Plastic Quad Flat, No Lead Package (M4C) - 5x5x1 mm Body [VQFN] With 3.50 mm Exposed Pad; Microsemi Legacy Package

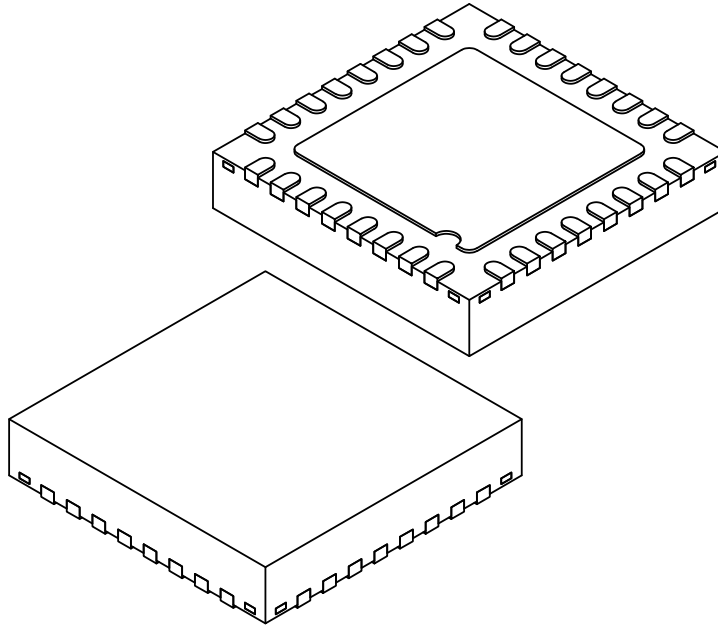
Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-25401 Rev A Sheet 1 of 2

32-Lead Very Thin Plastic Quad Flat, No Lead Package (M4C) - 5x5x1 mm Body [VQFN] With 3.50 mm Exposed Pad; Microsemi Legacy Package

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N	32		
Pitch	e	0.50 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3	0.20 REF		
Overall Length	D	5.00 BSC		
Exposed Pad Length	D2	3.40	3.50	3.60
Overall Width	E	5.00 BSC		
Exposed Pad Width	E2	3.40	3.50	3.60
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K	0.35 REF		

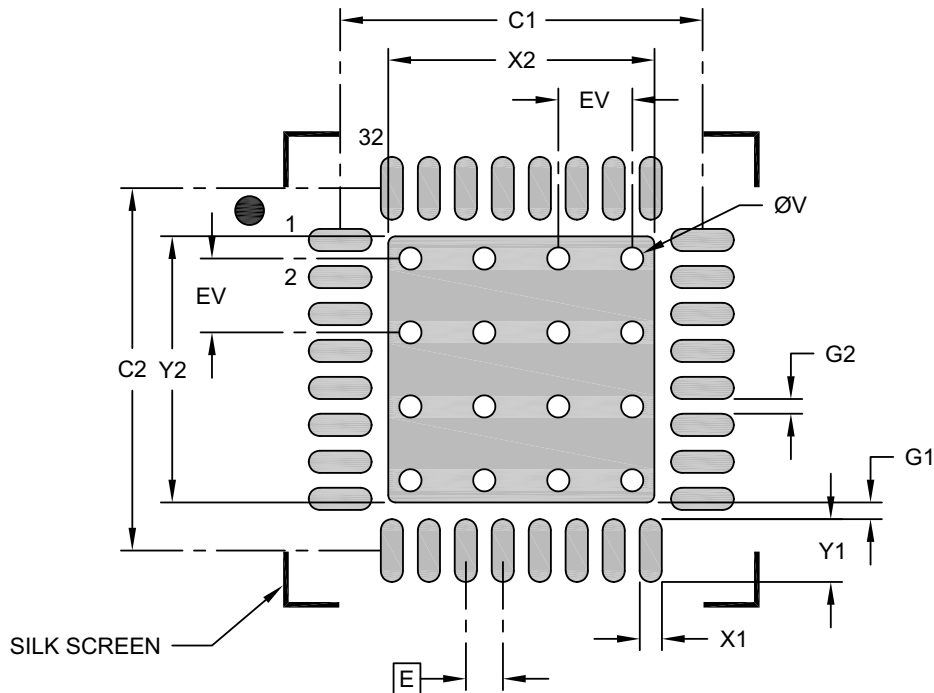
Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated
- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-25401 Rev A Sheet 2 of 2

32-Lead Very Thin Plastic Quad Flat, No Lead Package (M4C) - 5x5x1 mm Body [VQFN] With 3.50 mm Exposed Pad; Microsemi Legacy Package

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Optional Center Pad Width	X2			3.60
Optional Center Pad Length	Y2			3.60
Contact Pad Spacing	C1		4.90	
Contact Pad Spacing	C2		4.90	
Contact Pad Width (X32)	X1			0.30
Contact Pad Length (X32)	Y1			0.85
Contact Pad to Center Pad (X32)	G1	0.23		
Contact Pad to Contact Pad (X28)	G2	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
- For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-27401 Rev A

6.2 Thermal Specifications

TABLE 6-1: 5 MM X 5 MM VQFN THERMAL PROPERTIES

Parameter	Symbol	Value	Conditions
Maximum Ambient Temperature	$T_{A(MAX)}$	85°C	—
Maximum Junction Temperature	$T_{J(MAX)}$	125°C	—
Junction to Ambient Thermal Resistance (Note 1)	θ_{JA}	29.6°C/W	Still air
		23.3°C/W	1 m/s airflow
		20.6°C/W	2.5 m/s airflow
Junction to Board Thermal Resistance	θ_{JB}	9.8°C/W	—
Junction to Case Thermal Resistance	θ_{JC}	17.5°C/W	—
Junction to Pad Thermal Resistance (Note 2)	θ_{JP}	3.4°C/W	Still air
Junction to Top-Center Thermal Characterization Parameter	Ψ_{JT}	0.2°C/W	Still air

- Note 1:** Theta-JA (θ_{JA}) is the thermal resistance from junction to ambient when the package is mounted on a 4-layer JEDEC standard test board and dissipating maximum power.
- 2:** Theta-JP (θ_{JP}) is the thermal resistance from junction to the center exposed pad on the bottom of the package).
- 3:** For all numbers in the table, the exposed pad is connected to the ground plane with a 5x5 array of thermal vias; via diameter 0.33 mm; via pitch 0.76 mm.

APPENDIX A: DATA SHEET REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision	Section/Figure/Entry	Correction
DS20007046A (09-03-25)	—	Initial release of ZL40255A as Microchip data sheet DS20007046A.
DS20007046B (01-14-26)	Table 5-6	Remove output duty cycle information in Table 5-6 as it is governed by minimum input clock spec in Table 5-5.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>X</u>
Device	Chip Carrier Type	Package	Media Type	Finish
Device: ZL40255A: 6-Output SPI/I²C ePPS-Capable CMOS Fanout Buffer Chip Carrier Type: L = Leadless Chip Carrier Package: D = 32-Lead 5 mm x 5 mm VQFN Package Media Type: G = 490/Tray F = 4,000/Reel Finish: 1 = Pb Free with Matte Sn Lead Finish Equating to RoHS e3				
Examples: a) ZL40255ALDG1: ZL40255A, Leadless Chip Carrier, 32-Lead VQFN Package, 490/Tray, Pb Free with Matte Sn Lead Finish Equating to RoHS e3 b) ZL40255ALDF1: ZL40255A, Leadless Chip Carrier, 32-Lead VQFN Package, 4,000/Reel, Pb Free with Matte Sn Lead Finish Equating to RoHS e3 Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.				

ZL40255A

NOTES:

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