

24 Channel Data Acquisition System with Synchronized Motor Control Interface

Description

The [LX4580](#) is an analog front end for motor-actuator control systems working under stringent standards such as DO-160.

The LX4580 interfaces with MCUs or FPGAs to execute digital control system algorithms in real time. Dual high speed SPI or UART interfaces offer simultaneous dual-port register access for redundant COM/MON system architectures. The interfaces use ECC encoding to provide 1 bit error correction and 2 bit error detection in every 16 bit data transaction. Sequential logic is implemented with Triple Mode Redundancy (TMR) to protect against Single-Event Upsets (SEUs). Analog inputs, LVDT drivers, and logic I/Os can be cold spared, allowing two LX4580s to operate in a redundant configuration with one powered on while the other is off or in reset. System configuration, calibration, and interface setup data is stored in internal OTP memory and automatically loaded at power-up.

For motor control, there are 8 independent PWM outputs to drive upper and lower MOSFET gate drivers in half-bridge or other configurations. The LX4580 includes 5 sigma-delta ADCs operating up to 2MHz sample rate to measure motor phase currents and supply current (or other inputs) synchronously.

The LX4580 includes primary drivers, secondary interfaces and fault detection for 2 independent LVDT/resolver sensors. Full bridge primary drivers drive a PWM modulated sine wave or other desired waveform from independent internal lookup tables. Each of the 4 secondary circuits has a dedicated sigma-delta ADC operating up to 2MHz sample rate, and secondary RMS voltage calculation is available in addition to the instantaneous ADC sample data streams.

5 resistive temperature sensors, the LVDT drive waveform, and three 4-20mA (typically pressure) sensors interface dedicated instrumentation amplifiers with differential inputs and are multiplexed with 2 additional single-ended inputs into dual SAR ADCs. Each 4-20mA input has a power off switch, and each temperature input has a configurable current source for Pt100 or Pt1000 RTDs. All inputs include short/open testing.

Nine GPIOs are programmable as I/O, fault outputs, PWM and LVDT timing synchronization, or Hall Effect sensor inputs.

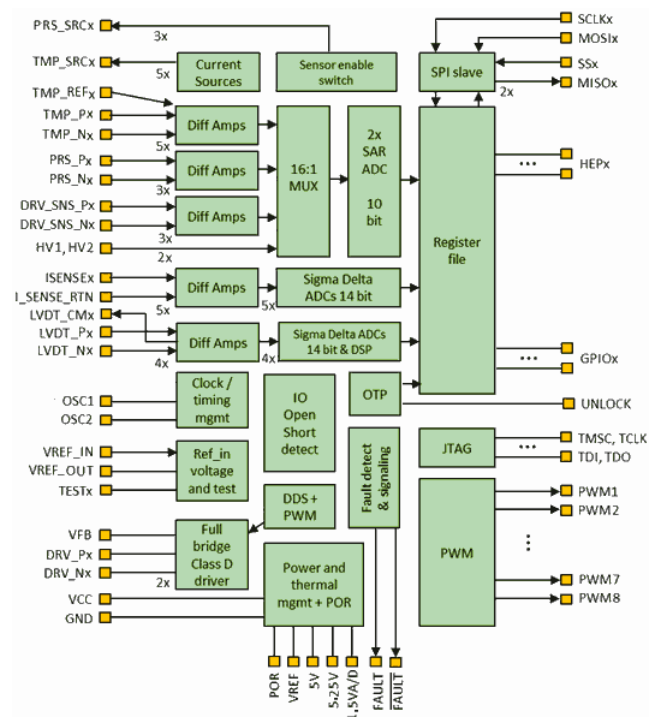
The LX4580 is packaged in a 144-pin lead-free non-hermetic plastic quad flat pack and operates over a -55°C to 110°C temperature range. Enquire for higher temperature operation.

Features

- Dual 30MHz SPI or dual 1MHz UART serial interfaces with single bit error correction
- 8 PWM outputs for 4 motor half-bridges
- 5 current sense interfaces via 5 dedicated Σ - Δ ADCs
- 2 independent LVDT/resolver primary drivers
- 4 dedicated Σ - Δ ADCs with differential inputs providing instantaneous and RMS outputs from 4 LVDT/resolver secondary windings
- Dual 10 bit SAR ADCs acquire analog input signals:
 - 5 Pt100/Pt1000 temperature sensor interfaces
 - 3 pressure sensor (or other 4-20mA) interfaces
 - 2 additional general purpose analog inputs
 - LVDT/resolver drive waveform monitoring
- 3 Hall Effect proximity sensor inputs
- Integrated regulators for internal circuits and sensors
- 9 register programmable GPIO and status I/Os
- Advanced fault detection and signaling
- JTAG scan and test interface
- Small 144 pin LQFP plastic package

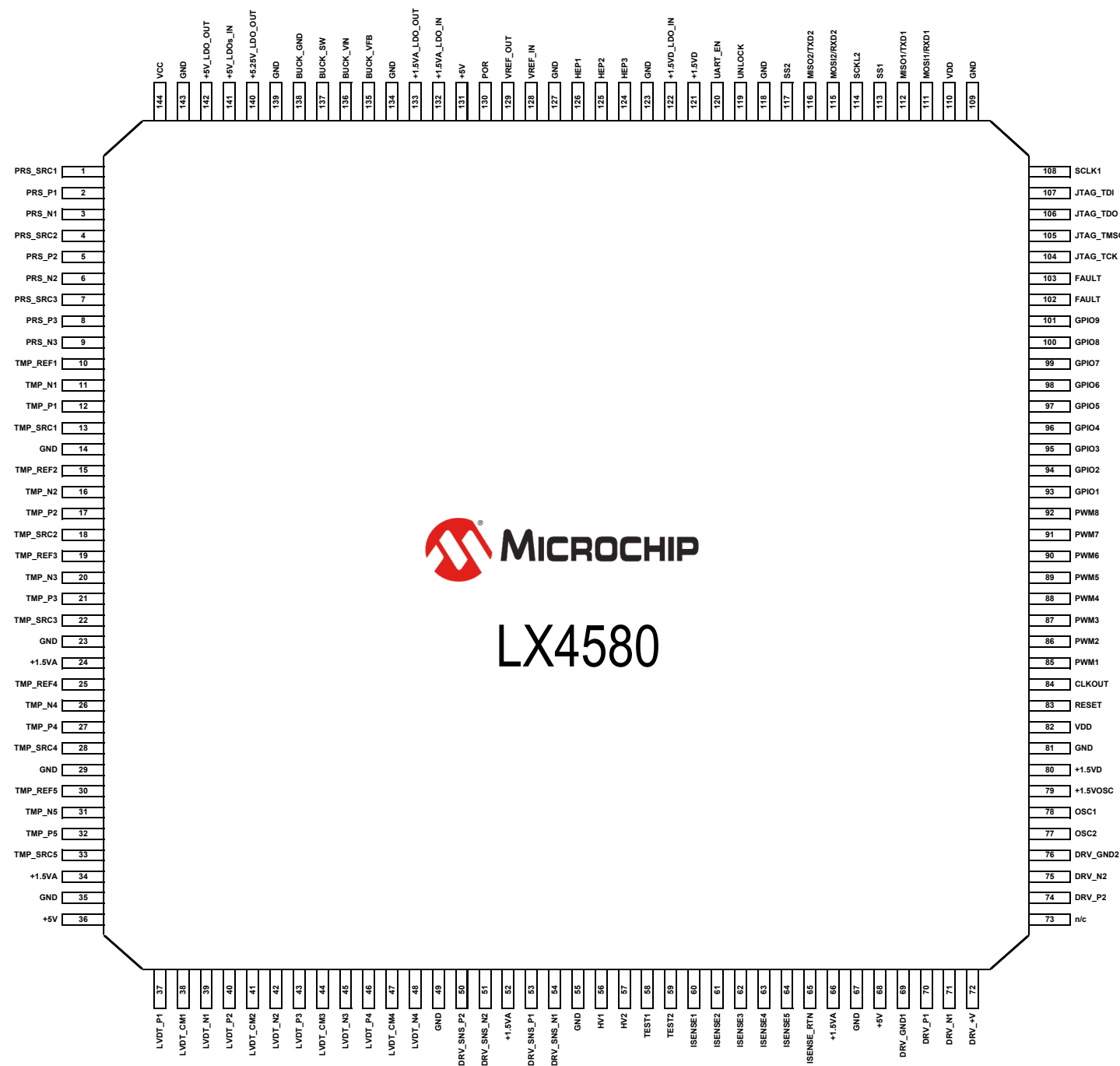
Applications

- Aviation, industrial and guidance servo actuators



Top-Level Block Diagram

1 LQFP-144 Pin Configuration and Pinout



- Note 1. Pin 73 marked n/c on the pinout is not bonded internally
- Note 2. Connect the exposed pad to the GND ground pins
- Note 3. The exposed pad is recommended as the main heat conducting path using the circuit board to dissipate heat

2 Ordering Information

Operating Temperature	Package Type	Package	Part Number	Flow	Shipping Type
-55°C to 110°C	Plastic Quad Flat Pack	LQFP-144	LX4580SLF	JEDEC	Tray
			MECH-SAMPLE-LQFP144	Empty Package Sample	

3 Pin Numbering and Pin Descriptions

Pin	Name	Pin Type	Pin Function	Description
1	PRS_SRC1	Power Output	Pressure Sensor 1 Voltage Source	Protected, register-enabled VCC power to 4-20mA sensor 1. Leave pin open if unused.
2	PRS_P1	Analog Input	Pressure Sensor 1 Amplifier +ve Input	Non-inverting input for 4-20mA sensor 1 differential amplifier. Tie PRS_P1 to GND if unused
3	PRS_N1	Analog Input	Pressure Sensor 1 Amplifier -ve Input	Inverting input for 4-20mA sensor 1 differential amplifier. Tie PRS_N1 to GND if unused
4	PRS_SRC2	Power Output	Pressure Sensor 2 Voltage Source	Protected, register-enabled VCC power to 4-20mA sensor 2. Leave pin open if unused.
5	PRS_P2	Analog Input	Pressure Sensor 2 Amplifier +ve Input	Non-inverting input for 4-20mA sensor 2 differential amplifier. Tie PRS_P2 to GND if unused
6	PRS_N2	Analog Input	Pressure Sensor 2 Amplifier -ve Input	Inverting input for 4-20mA sensor 2 differential amplifier. Tie PRS_N2 to GND if unused
7	PRS_SRC3	Power Output	Pressure Sensor 3 Voltage Source	Protected, register-enabled VCC power to 4-20mA sensor 3. Leave pin open if unused.
8	PRS_P3	Analog Input	Pressure Sensor 3 Amplifier +ve Input	Non-inverting input for 4-20mA sensor 3 differential amplifier. Tie PRS_P3 to GND if unused
9	PRS_N3	Analog Input	Pressure Sensor 3 Amplifier -ve Input	Inverting input for 4-20mA sensor 3 differential amplifier. Tie PRS_N3 to GND if unused
10	TMP_REF1	Analog Input	Temperature Sensor 1 external reference resistor	Connect a precision reference resistor from TMP_REF1 to GND pin 14 to develop the positive measurement voltage for temperature sensor 1. The current set by the I_TEMP1_SRC current DAC passes from the TMP_SRC1 pin through the remote resistive temperature sensor and back through the resistor at TMP_REF1 to GND
11	TMP_N1	Analog Input	Temp Sensor 1 Amplifier -ve Input	Inverting input for temperature sensor 1 differential amplifier. Connect to one end of the remote resistive temperature sensor and to TMP_REF1 either locally or at the temperature sensor for 2-wire or 4-wire measurement respectively
12	TMP_P1	Analog Input	Temp Sensor 1 Amplifier +ve Input	Non-inverting input for temperature sensor 1 differential amplifier. Connect to one end of the remote resistive temperature sensor and to TMP_SRC1 either locally or at the temperature sensor for 2-wire or 4-wire measurement respectively
13	TMP_SRC1	Analog Output	Temperature Sensor 1 Source	Programmable current source for temperature sensor 1 set by the I_TEMP1_SRC current DAC
14	GND	Power	Temperature Sensor 1 & 2 GND	Connect to ground and TMP_REF4 use as star point for the reference resistors at TMP_REF1 and TMP_REF2
15	TMP_REF2	Analog Input	Temperature Sensor 2 external reference resistor	Connect a precision reference resistor from TMP_REF2 to GND pin 24 to develop the positive measurement voltage for temperature sensor 2. The current set by the I_TEMP2_SRC current DAC passes from the TMP_SRC2 pin through the remote resistive temperature sensor and back through the resistor at TMP_REF2 to GND
16	TMP_N2	Analog Input	Temp Sensor 2 Amplifier -ve Input	Inverting input for temperature sensor 2 differential amplifier. Connect to one end of the remote resistive temperature sensor and to TMP_REF2 either locally or at the temperature sensor for 2-wire or 4-wire measurement respectively
17	TMP_P2	Analog Input	Temp Sensor 2 Amplifier +ve Input	Non-inverting input for temperature sensor 2 differential amplifier. Connect to one end of the remote resistive temperature sensor and to TMP_SRC2 either locally or at the temperature sensor for 2-wire or 4-wire measurement respectively
18	TMP_SRC2	Analog Output	Temperature Sensor 2 Source	Programmable current source for temperature sensor 2 set by the I_TEMP2_SRC current DAC
19	TMP_REF3	Analog Input	Temperature Sensor 3 external reference resistor	Connect a precision reference resistor from TMP_REF3 to GND pin 34 to develop the positive measurement voltage for temperature sensor 3. The current set by the I_TEMP3_SRC current DAC passes from the TMP_SRC3 pin through the remote resistive temperature sensor and back through the resistor at TMP_REF3 to GND
20	TMP_N3	Analog Input	Temp Sensor 3 Amplifier -ve Input	Inverting input for temperature sensor 3 differential amplifier. Connect to one end of the remote resistive temperature sensor and to

Pin	Name	Pin Type	Pin Function	Description
				TMP_REF3 either locally or at the temperature sensor for 2-wire or 4-wire measurement respectively
21	TMP_P3	Analog Input	Temp Sensor 3 Amplifier +ve Input	Non-inverting input for temperature sensor 3 differential amplifier. Connect to one end of the remote resistive temperature sensor and to TMP_SRC3 either locally or at the temperature sensor for 2-wire or 4-wire measurement respectively
22	TMP_SRC3	Analog Output	Temperature Sensor 3 Source	Programmable current source for temperature sensor 3 set by the I_TEMP3_SRC current DAC
23	GND	Power	Temperature Sensor 3 & 4 GND	Connect to ground and optionally use as star point for the reference resistors at TMP_REF3 and TMP_REF4
24	+1.5VA	Power	+1.5VA Analog Supply	+1.5VA power rail for analog core. Connect this pin and pins 34, 52, 66, and 79 to the output of the internal +1.5V linear regulator at +1.5VA_LDO_OUT pin 133. Bypass close to the pin with a 100nF capacitor to GND pin 23
25	TMP_REF4	Analog Input	Temperature Sensor 4 external reference resistor	Connect a precision reference resistor from TMP_REF4 to GND pin 44 to develop the positive measurement voltage for temperature sensor 4. The current set by the I_TEMP4_SRC current DAC passes from the TMP_SRC4 pin through the remote resistive temperature sensor and back through the resistor at TMP_REF4 to GND
26	TMP_N4	Analog Input	Temp Sensor 4 Amplifier -ve Input	Inverting input for temperature sensor 4 differential amplifier. Connect to one end of the remote resistive temperature sensor and to TMP_REF4 either locally or at the temperature sensor for 2-wire or 4-wire measurement respectively
27	TMP_P4	Analog Input	Temp Sensor 4 Amplifier +ve Input	Non-inverting input for temperature sensor 4 differential amplifier. Connect to one end of the remote resistive temperature sensor and to TMP_SRC4 either locally or at the temperature sensor for 2-wire or 4-wire measurement respectively
28	TMP_SRC4	Analog Output	Temperature Sensor 4 Source	Programmable current source for temperature sensor 4 set by the I_TEMP4_SRC current DAC
29	GND	Power	Temperature Sensor 5 GND	Connect to ground and optionally use as star point for the reference resistor at TMP_REF5
30	TMP_REF5	Analog Input	Temperature Sensor 5 external reference resistor	Connect a precision reference resistor from TMP_REF5 to GND pin 54 to develop the positive measurement voltage for temperature sensor 5. The current set by the I_TEMP5_SRC current DAC passes from the TMP_SRC5 pin through the remote resistive temperature sensor and back through the resistor at TMP_REF5 to GND
31	TMP_N5	Analog Input	Temp Sensor 5 Amplifier -ve Input	Inverting input for temperature sensor 5 differential amplifier. Connect to one end of the remote resistive temperature sensor and to TMP_REF5 either locally or at the temperature sensor for 2-wire or 4-wire measurement respectively
32	TMP_P5	Analog Input	Temp Sensor 5 Amplifier +ve Input	Non-inverting input for temperature sensor 5 differential amplifier. Connect to one end of the remote resistive temperature sensor and to TMP_SRC5 either locally or at the temperature sensor for 2-wire or 4-wire measurement respectively
33	TMP_SRC5	Analog Output	Temperature Sensor 5 Source	Programmable current source for temperature sensor 5 set by the I_TEMP5_SRC current DAC
34	+1.5VA	Power	+1.5VA Analog Supply	+1.5VA power rail for analog core. Connect this pin and pins 24, 52, 66, and 79 to the output of the internal +1.5V linear regulator at +1.5VA_LDO_OUT pin 133. Bypass close to the pin with a 100nF capacitor to GND pin 35
35	GND	Power	Analog GND	Ground. All GND pins must be used and connected together
36	+5V	Power	+5V Signal Supply	Connect this pin, pin 68, and pin 131 to the output of the internal +5V linear regulator at +5V_LDO_OUT pin 142. Bypass close to the pin with a 100nF capacitor to GND pin 67
37	LVDT_P1	Analog Input	LVDT 1 +ve Input	Non-inverting input for LVDT secondary 1 differential amplifier
38	LVDT_CM1	Analog Input	LVDT 1 CM input	Common mode input for LVDT secondary 1 differential amplifier and output of internal 750mV common mode biasing
39	LVDT_N1	Analog Input	LVDT 1 -ve Input	Inverting input for LVDT secondary 1 differential amplifier

Pin	Name	Pin Type	Pin Function	Description
40	LVDT_P2	Analog Input	LVDT 2 +ve Input	Non-inverting input for LVDT secondary 2 differential amplifier
41	LVDT_CM2	Analog Input	LVDT 2 CM input	Common mode input for LVDT secondary 2 differential amplifier. Connect to LVDT_CM1 pin 38
42	LVDT_N2	Analog Input	LVDT 2 -ve Input	Inverting input for LVDT secondary 2 differential amplifier
43	LVDT_P3	Analog Input	LVDT 3 +ve Input	Non-inverting input for LVDT secondary 3 differential amplifier
44	LVDT_CM3	Analog Input	LVDT 3 CM input	Common mode input for LVDT secondary 3 differential amplifier and output of internal 750mV common mode biasing
45	LVDT_N3	Analog Input	LVDT 3 -ve Input	Inverting input for LVDT secondary 3 differential amplifier
46	LVDT_P4	Analog Input	LVDT 4 +ve Input	Non-inverting input for LVDT secondary 4 differential amplifier
47	LVDT_CM4	Analog Input	LVDT 4 CM input	Common mode input for LVDT secondary 4 differential amplifier. Connect to LVDT_CM3 pin 44
48	LVDT_N4	Analog Input	LVDT 4 -ve Input	Inverting input for LVDT secondary 4 differential amplifier
49	GND	Power	Analog GND	Ground. All GND pins must be used and connected together
50	DRV_SNS_P2	Analog Input	LVDT 2 drive +ve Input	Non-inverting input for differential amplifier typically used for measuring the LC filtered LVDT 2's driver output
51	DRV_SNS_N2	Analog Input	LVDT 2 drive -ve Input	Inverting input for differential amplifier typically used for measuring the LC filtered LVDT 2's driver output
52	+1.5VA	Power	+1.5VA Analog Supply	+1.5VA power rail for analog core. Connect this pin and pins 24, 34, 66, and 79 to the output of the internal +1.5V linear regulator at +1.5VA_LDO_OUT pin 133. Bypass close to the pin with a 100nF capacitor to GND
53	DRV_SNS_P1	Analog Input	LVDT 1 drive +ve Input	Non-inverting input for differential amplifier typically used for measuring the LC filtered LVDT 1's driver output
54	DRV_SNS_N1	Analog Input	LVDT 1 drive -ve Input	Inverting input for differential amplifier typically used for measuring the LC filtered LVDT 1's driver output
55	GND	Power	Analog GND	Analog Ground. All GND and GND pins must be used and connected together
56	HV1	Analog Input	SAR ADC Input	1 of 2 single ended analog voltage inputs with nominal 1.3V FSD that can be multiplexed into one of the two 10 bit SAR ADCs
57	HV2	Analog Input	SAR ADC Input	2 of 2 single ended analog voltage inputs with nominal 1.3V FSD that can be multiplexed into one of the two 10 bit SAR ADCs
58	TEST1	Logic I/O	Test pin 1	Leave open
59	TEST2	Logic I/O	Test pin 2	Leave open
60	ISENSE1	Analog Input	Current Sense Input 1	Output of external isolated current sensor typically for motor phase current
61	ISENSE2	Analog Input	Current Sense Input 2	Output of external isolated current sensor typically for motor phase current
62	ISENSE3	Analog Input	Current Sense Input 3	Output of external isolated current sensor typically for motor phase current
63	ISENSE4	Analog Input	Current Sense Input 4	Output of external isolated current sensor typically for motor phase current
64	ISENSE5	Analog Input	Current Sense Input 5	Output of external isolated current sensor typically for motor phase current
65	ISENSE_RTN	Analog Input	Current Sense GND Reference	GND reference for all current sense inputs
66	+1.5VA	Power	+1.5VA Analog Supply	+1.5VA power rail for analog core. Connect this pin and pins 24, 34, 52, and 79 to the output of the internal +1.5V linear regulator at +1.5VA_LDO_OUT pin 133. Bypass close to the pin with a 100nF capacitor to GND pin 67
67	GND	Power	Analog GND	Ground. All GND pins must be used and connected together
68	+5V	Power	+5V Signal Supply	Connect this pin, pin 36, and pin 131 to the output of the internal +5V linear regulator at +5V_LDO_OUT pin 142. Bypass close to the pin with a 100nF capacitor to GND pin 67
69	GND_DRV1	Power	LVDT 1 GND	Connect to analog ground and use as star point for any LC filter used between the DRV_P1 and DRV_N1 LVDT drive outputs and LVDT 1's

Pin	Name	Pin Type	Pin Function	Description
				primary
70	DRV_P1	Analog Output	LVDT 1 Half bridge driver P	Output of one of the two complementary half bridge drivers working together to provide a full-bridge drive to LVDT 1's primary
71	DRV_N1	Analog Output	LVDT 1 Half bridge driver P	Output of one of the two complementary half bridge drivers working together to provide a full-bridge drive to LVDT 1's primary
72	VFB	Power	LVDT Drivers Supply	Connect to the LVDT bridge drivers power supply (10V to 30V). Bypass close to the pin with a 2.2μF capacitor to GND
73	n/c	-		Pin is not connected
74	DRV_P2	Analog Output	LVDT 2 Half bridge driver P	Output of one of the two complementary half bridge drivers working together to provide a full-bridge drive to LVDT 2's primary
75	DRV_N2	Analog Output	LVDT 2 Half bridge driver P	Output of one of the two complementary half bridge drivers working together to provide a full-bridge drive to LVDT 2's primary
76	GND_DRV2	Power	LVDT 2 GND	Connect to analog ground and use as star point for any LC filter used between the DRV_P2 and DRV_N2 LVDT drive outputs and LVDT 2's primary
77	OSC2	Analog Output	Crystal Oscillator	Connect to a crystal/capacitor network to set the system clock frequency in the range 20MHz to 30MHz, or drive OSC1 with external 1.5V CMOS clock and leave OSC2 open
78	OSC1	Analog Input	Crystal Oscillator	
79	+1.5VOSC	Power	+1.5VA Analog Supply	+1.5V power rail for the crystal oscillator. Connect this pin and pins 24, 34, 52, and 66 to the output of the internal +1.5V linear regulator at +1.5VA_LDO_OUT pin 133. Bypass close to the pin with a 100nF capacitor to GND
80	+1.5VD	Power	+1.5VD Digital Supply, Internally Generated	+1.5VD power rail for digital core, generated by an internal +1.5V linear regulator. Connect this pin to pin 121. Bypass close to the pin with a 100nF capacitor to GND pin 81
81	GND	Power	Digital GND	Ground. All GND pins must be used and connected together
82	VDD	Power	I/O Supply	Connect this pin and pin 110 to the system I/O power supply (2.25V to 5.5V) to set the I/O logic level for all logic I/Os. Bypass close to the pin with a 1μF capacitor to GND
83	RESET	Logic Input (50kΩ to VDD)	Reset Input	Active high input resets the internal settings to a known state
84	CLKOUT	Logic Output	Clock Output	Buffered clock output of frequency defined at the OSC1 and OSC2 pins
85	PWM1	Logic Output	PWM Output 1	Pulse width modulated output 1 intended for a motor phase or solenoid driver
86	PWM2	Logic Output	PWM Output 2	Pulse width modulated output 2 intended for a motor phase or solenoid driver
87	PWM3	Logic Output	PWM Output 3	Pulse width modulated output 3 intended for a motor phase or solenoid driver
88	PWM4	Logic Output	PWM Output 4	Pulse width modulated output 4 intended for a motor phase or solenoid driver
89	PWM5	Logic Output	PWM Output 5	Pulse width modulated output 5 intended for a motor phase or solenoid driver
90	PWM6	Logic Output	PWM Output 6	Pulse width modulated output 6 intended for a motor phase or solenoid driver
91	PWM7	Logic Output	PWM Output 7	Pulse width modulated output 7 intended for a motor phase or solenoid driver
92	PWM8	Logic Output	PWM Output 8	Pulse width modulated output 8 intended for a motor phase or solenoid driver
93	GPIO1	Logic I/O	GPIO 1	General purpose logic I/O port 1 with programmable 50kΩ pulldown
94	GPIO2	Logic I/O	GPIO 2	General purpose logic I/O port 2 with programmable 50kΩ pulldown
95	GPIO3	Logic I/O	GPIO 3	General purpose logic I/O port 3 with programmable 50kΩ pulldown
96	GPIO4	Logic I/O	GPIO 4	General purpose logic I/O port 4 with programmable 50kΩ pulldown
97	GPIO5	Logic I/O	GPIO 5	General purpose logic I/O port 5 with programmable 50kΩ pulldown
98	GPIO6	Logic I/O	GPIO 6	General purpose logic I/O port 6 with programmable 50kΩ pulldown

Pin	Name	Pin Type	Pin Function	Description
99	GPIO7	Logic I/O	GPIO 7	General purpose logic I/O port 7 with programmable 50kΩ pulldown
100	GPIO8	Logic I/O	GPIO 8	General purpose logic I/O port 8 with programmable 50kΩ pulldown
101	GPIO9	Logic I/O	GPIO 9	General purpose logic I/O port 9 with programmable 50kΩ pulldown
102	FAULT	Logic Output	Fault Alert	Active low fault alert
103	FAULT	Logic Output	Fault Alert	Active high fault alert
104	JTAG_TCK	Logic Input (320kΩ to GND)	JTAG Clock	JTAG Clock
105	JTAG_TMSC	Logic Input (320kΩ to GND)	JTAG Mode Select	JTAG Mode Select
106	JTAG_TDO	Logic Output	JTAG Data Output	JTAG Data Output
107	JTAG_TDI	Logic Input (320kΩ to GND)	JTAG Data Input	JTAG Data Input
108	SCLK1	Logic Input	SPI Clock 1	Clock input for SPI channel 1 interface
109	GND	Power	Digital GND	Ground. All GND pins must be used and connected together
110	VDD	Power	I/O Supply	Connect this pin and pin 82 to the system I/O power supply (2.25V to 5.5V) to set the I/O logic level for all logic I/Os. Bypass close to the pin with a 1μF capacitor to GND
111	MOSI1/RXD1	Logic Input	SPI MOSI 1, or UART RXD 1	Data input for SPI channel 1 or UART channel 1 interface
112	MISO1/TXD1	Logic Output	SPI MISO 1, or UART TXD 2	Data output for SPI channel 1 or UART channel 1 interface
113	SS1	Logic Input	SPI Select 1	Active low SPI select for SPI channel 1 interface. Set CONTROL_REG2 bit 9 to change the polarity of both SS1 and SS2 to be active high SS1 and SS2 instead
114	SCKL2	Logic Input	SPI Clock 2	Clock input for SPI channel 2 interface
115	MOSI2/RXD2	Logic Input	SPI MOSI 2, or UART RXD 2	Data input for SPI channel 2 or UART channel 2 interface
116	MISO2/TXD2	Logic Output	SPI MISO 2, or UART TXD 2	Data output for SPI channel 2 or UART channel 2 interface
117	SS2	Logic Input	SPI Select 2	Active low SPI select for SPI channel 2 interface. Set CONTROL_REG2 bit 9 to change the polarity of both SS1 and SS2 to be active high SS1 and SS2 instead
118	GND	Power	Digital GND	Ground. All GND pins must be used and connected together
119	UNLOCK	Logic Input (50kΩ to GND)	OTP Programming Enable	Connect to logic high to enable enable OTP programming. Connect to GND for normal operation
120	UART_EN	Logic Input (50kΩ to GND)	UART/SPI Mode	Connect to VDD or logic high to enable dual UART serial interfaces. Connect to GND to enable dual SPI serial interfaces
121	+1.5VD	Power	+1.5VD Digital Supply, Internally Generated	+1.5VD power rail for digital core, generated by an internal +1.5V linear regulator. Connect this pin to pin 80. Bypass close to the pin with a 1μF capacitor to GND pin 123
122	+1.5VD_LDO_IN	Power	+1.5VD Regulator Input	+1.5VD linear regulator input for digital core. Connect this pin to a 1.85V to 5.5V supply. Bypass close to the pin with a 2.2μF capacitor to GND pin 123
123	GND	Power	Digital GND	Connect to ground and use as star point for the +1.5VD regulator bypass capacitors
124	HEP3	Logic Input (320kΩ to GND)	Hall Effect Input 3	Hall Effect or other sensor comparator input. 5V logic input with 2V hysteresis
125	HEP2	Logic Input (320kΩ to GND)	Hall Effect Input 2	Hall Effect or other sensor comparator input. 5V logic input with 2V hysteresis
126	HEP1	Logic Input (320kΩ to GND)	Hall Effect Input 1	Hall Effect or other sensor comparator input. 5V logic input with 2V hysteresis
127	GND	Power	VREF GND	Connect to ground and use as star point for the bypass capacitor(s) at VREF_OUT and also VREF_IN if an external reference is used

Pin	Name	Pin Type	Pin Function	Description
128	VREF_IN	Analog Input	External VREF Input	To use the internal +1.235V reference voltage, connect VREF_IN to VREF_OUT pin 129. To use an external reference voltage, connect the reference to VREF_IN and bypass with a 100nF capacitor from VREF_IN to GND pin 127
129	VREF_OUT	Analog Output	Internal VREF Output	+1.235V internal reference voltage. Bypass with a 100nF capacitor from VREF_OUT to GND pin 127, even if an external reference voltage is used at VREF_IN
130	POR	Logic Input	POR Delay	Fit a 10nF capacitor from POR to GND to set the power on reset delay
131	+5V	Power	+5V Signal Supply	Connect this pin, pin 36, and pin 68 to the output of the internal +5V linear regulator at +5V_LDO_OUT pin 142. Bypass close to the pin with a 100nF capacitor to GND pin 67
132	+1.5VA_LDO_IN	Power	+1.5VA Regulator Input	+1.5VA analog linear regulator input. Connect this pin to a 1.85V to 5.5V supply. Bypass close to the pin with a 2.2μF capacitor to GND pin 134
133	+1.5VA_LDO_OUT	Power	+1.5VA Regulator Output	+1.5VA analog linear regulator output. Connect this pin to the +1.5VA supply pins 24, 34, 52, 66, and 79. Bypass close to the pin with a 1μF capacitor to GND pin 134
134	GND	Power	+1.5VA GND	Connect to ground and use as star point for the +1.5VA regulator bypass capacitors
135	BUCK_VFB	Analog Input	Buck voltage sense	The buck converter regulates its output to maintain the voltage at this pin to the voltage at VREF_IN pin 128 (1.235V typ)
136	BUCK_VIN	Power	Buck supply	Buck converter supply input, normally connected to VCC.
137	BUCK_SW	Analog Output	Buck SW output	Buck converter switching node. Connect to external inductor and Schottky diode
138	BUCK_GND	Power	Buck GND	Buck converter GND pin. Connect to GND pin 139
139	GND	Power	Analog GND	Ground. All GND pins must be used and connected together
140	+5.25V_LDO_OUT	Power	+5.25V Regulator Output	+5.25V linear regulator output. This supply is available for external system loads up to 25mA. Bypass close to the pin with a 1μF capacitor to GND
141	+5V_LDOs_IN	Power	+5.25 and +5V Regulators Input	+5.25 and +5V linear regulators input. Connect this pin a 6.2V to 16V supply. Bypass close to the pin with a 1μF capacitor to GND
142	+5V_LDO_OUT	Power	+5V Regulator Output	+5V linear regulator output. Connect this pin to the +5V supply pins 36, 68, and 131. Bypass close to the pin with a 1μF capacitor to GND
143	GND	Power	Analog GND	Ground. All GND pins must be used and connected together
144	VCC	Power	Input Supply	Connect to the main power supply (10V to 30V). Bypass close to the pin with a 2.2μF capacitor to GND pin 143
EP	Exposed Pad			Connect the exposed pad to GND

4 Absolute Maximum Ratings

Stresses above those listed in ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Parameter	Min	Max	Units
Main Power Supply (VCC) to GND	-0.5	40	V
Resolver/LVDT Driver Power Supply (VFB) to GND	-0.5	40	V
PS_SRC# Voltage to GND	-0.5	40	V
Buck Regulator Power Supply (BUCK_VIN) to GND	-0.5	VCC + 0.5	V
5V Linear Regulators Power Supply (+5V_LDOs_IN) to GND	-0.5	17.5	V
1.5VA Linear Regulator Power Supply (+1.5VA_LDO_IN) to GND	-0.5	5.75	V
1.5VD Linear Regulator Power Supply (+1.5VD_LDO_IN) to GND	-0.5	5.75	V
Digital I/O Power Supply (VDD) to GND	-0.5	5.75	V
All Other 5V Domain Pins to GND	-0.5	5.75	V
1.5V Domains (Analog And Digital Core) I/O to GND	-0.5	1.7	V
HV1 and HV2 inputs to GND	0	1.7	V
Operating Junction Temperature	-55	155	°C
Storage Junction Temperature	-65	165	°C
Peak Lead Solder Temperature (10 seconds)		260	°C

5 Electrostatic Discharge Ratings

JEDEC JEP155 and JEP157 state that 500V HBM and 250V CDM respectively allows safe manufacturing with a standard ESD controlled process. ESD ratings apply to all pins.

ESD Test	Minimum Capability
HBM: Human Body Model, per MIL-STD-883 TM3015	±2kV
CDM: Charged Device Model, per ANSI/ESDA/JEDEC JS-002	±400V

6 Operating Ratings

Performance is generally guaranteed over this range as further detailed below under Electrical Characteristics.

Parameter	Min	Max	Units
Main Power Supply (VCC) to GND	10	30	V
Resolver/LVDT Driver Power Supply (VFB) to GND	10	30	V
PS_SRC# Voltage (internal connection)	0	VCC	V
Buck Regulator Power Supply (BUCK_VIN) to GND	4	VCC	V
Digital I/O Power Supply (VDD) to GND	2.25	5.5	V
5.25V and 5V Linear Regulators Power Supply (+5V_LDOs_IN) to GND	6.2	16.5	V
5.25V Linear Regulator Output (+5.25V_LDO_OUT) to GND	5.15	5.35	V
5V Linear Regulator Output (+5V_LDO_OUT) to GND	4.9	5.1	V
5V domains (analog core associated with Pins 36, 68, and 131)	4.5	5.5	V
VREF_IN	1.229	1.237	V
1.5VA Linear Regulator Power Supply (+1.5VA_LDO_IN) to GND	1.85	5.5	V
1.5VD Linear Regulator Power Supply (+1.5VD_LDO_IN) to GND	1.85	5.5	V
1.5VA analog Core Supply (+1.5VA_LDO_OUT) to GND	1.505	1.545	V
1.5VD digital Core Supply (+1.5VD_LDO_OUT) and OSC1 to GND	1.45	1.55	V
HV1 and HV2 inputs to GND	0	1.6	V
DRV_P, DRV_N voltage	0	VFB	V
DRV_P, DRV_N current	-25	25	mA
All other pins to GND	0	5.5	V

7 Electrical Characteristics

The following specifications apply over the operating ambient temperature of $-55^{\circ}\text{C} \leq T_A \leq 110^{\circ}\text{C}$ except where otherwise noted with the following test conditions: $V_{CC} = V_{FB} = 15\text{V}$, $V_{DD} = 3.3\text{V}$; $V_{REF_IN} = 1.235\text{V}$; Crystal frequency = 22.5MHz. Typical parameters refer to $T_J = 25^{\circ}\text{C}$. Positive currents flow into pins.

Symbol	Parameter	Test Conditions/Comments	Min	Typ	Max	Units
Operating Current						
I_{VCC}	VCC Current	Maximum loading on pressure sensor supplies before current limit			100	mA
I_{VDD}	VDD Current	Ready Mode		6	8	mA
I_{VFB}	VFB Current	With 10k Ω between DRV_P and DRV_N			10	mA
I_{REF_IN}	REF_IN Current	$V_{REF} = 1.235\text{V}$			0.1	mA
I_{VCC_R}	VCC ready current	After reset done and $\overline{\text{FAULT}} = 1$		2	3	mA
I_{VCC_O}	VCC operating current	Using "use case 1" activity pattern			4	mA
$I_{VFB_IN_R}$	VFB ready current	After reset done and $\overline{\text{FAULT}} = 1$		0.4	1	mA
$I_{VFB_IN_O}$	VFB operating current	Using "use case 1" activity pattern			4	mA
$I_{+5V_LDOs_IN_R}$	+5V_LDOs_IN ready current	After reset done and $\overline{\text{FAULT}} = 1$		0.6	1	mA
$I_{+5V_LDOs_IN_O}$	+5V_LDOs_IN operating current	Using "use case 1" activity pattern			6	mA
$I_{+1.5VD_LDO_IN_R}$	+1.5VD_LDO_IN ready current	After reset done and $\overline{\text{FAULT}} = 1$		19	25	mA
$I_{+1.5VD_LDO_IN_O}$	+1.5VD_LDO_IN operating current	Using "use case 1" activity pattern			35	mA
$I_{+1.5VA_LDO_IN_R}$	+1.5VA_LDO_IN ready current	After reset done and $\overline{\text{FAULT}} = 1$		4.5	6	mA
$I_{+1.5VA_LDO_IN_O}$	+1.5VA_LDO_IN operating current	Using "use case 1" activity pattern			21.5	mA
Input Supplies Under-Voltage (UV) and Over-Voltage (OV) Detection						
$OV_{VCC/VFB}$	VCC & VFB over-voltage	VCC and VFB power supplies. $V_{REF} = 1.235\text{V}$	36.25		37.75	V
OV_{VCC/VFB_hyst}	VCC & VFB over-voltage hysteresis	VCC and VFB power supplies. $V_{REF} = 1.235\text{V}$	0.6		1.6	V
$UV_{VCC/VFB}$	VCC & VFB under-voltage	VCC and VFB power supplies. $V_{REF} = 1.235\text{V}$	9.6		10.2	V
UV_{VCC/VFB_HYST}	VCC & VFB under-voltage hysteresis	VCC and VFB power supplies. $V_{REF} = 1.235\text{V}$	0.15	0.30	0.45	V
OV_{VDD}	VDD over-voltage	$V_{REF} = 1.235\text{V}$	5.75		5.95	V
OV_{VDD_HYST}	VDD over-voltage hysteresis	$V_{REF} = 1.235\text{V}$	0.08	0.17	0.25	V
UV_{VDD}	VDD under-voltage	$V_{REF} = 1.235\text{V}$	1.85		2.05	V
UV_{VDD_HYST}	VDD under-voltage hysteresis	$V_{REF} = 1.235\text{V}$	0.02	0.06	0.09	V
$OV_{+5V_LDOs_IN}$	+5V_LDOs_IN over-voltage	$V_{REF} = 1.235\text{V}$	17.65		18.25	V
$OV_{+5V_LDOs_IN_HYST}$	+5V_LDOs_IN over-voltage hysteresis	$V_{REF} = 1.235\text{V}$	0.08	0.17	0.25	V
$UV_{+5V_LDOs_IN}$	+5V_LDOs_IN under-voltage	$V_{REF} = 1.235\text{V}$	5.9		6.08	V
$UV_{+5V_LDOs_IN_HYST}$	+5V_LDOs_IN under-voltage hysteresis	$V_{REF} = 1.235\text{V}$	0.02	0.05	0.09	V
$OV_{+1.5V_LDOs_IN}$	+1.5V_LDOs_IN over-voltage	Applies to both +1.5VA_LDO_IN and +1.5VD_LDO_IN. $V_{REF} = 1.235\text{V}$	5.75		5.95	V
$OV_{+1.5V_LDOs_IN_HYST}$	+1.5V_LDOs_IN over-voltage hysteresis	Applies to both +1.5VA_LDO_IN and +1.5VD_LDO_IN. $V_{REF} = 1.235\text{V}$	0.08	0.17	0.25	V
$UV_{+1.5V_LDOs_IN}$	+1.5V_LDOs_IN under-voltage	Applies to both +1.5VA_LDO_IN and +1.5VD_LDO_IN. $V_{REF} = 1.235\text{V}$	1.7		1.8	V
$UV_{+1.5V_LDOs_IN_HYST}$	+1.5V_LDOs_IN under-voltage hysteresis	Applies to both +1.5VA_LDO_IN and +1.5VD_LDO_IN. $V_{REF} = 1.235\text{V}$	0.02	0.05	0.09	V

Symbol	Parameter	Test Conditions/Comments	Min	Typ	Max	Units
Internally Regulated Voltages and Currents						
V _{+5.25V_LDO_OUT}	5.25V regulator	External load of 25mA	5.15	5.25	5.35	V
V _{+5V_LDO_OUT}	5V regulator	For internal circuits	4.9	5.0	5.1	V
V _{+1.5VA_LDO_OUT}	1.5V regulator for analog	For internal circuits	1.505	1.525	1.545	V
V _{+1.5VD_LDO_OUT}	1.5V regulator for digital	For internal circuits, up to 2mA external load	1.45	1.5	1.55	V
V _{VREF}	VREF reference	Connected to REF_IN	1.229	1.235	1.237	V
I _{+5.25V_LDO_OUT_SC}	5.25V regulator	Short circuit current	55		170	mA
I _{+5.25V_LDO_OUT}	5.25V regulator	Maximum current for linear region operation, +5V_LDOs_IN = 6V, Output = 5V			50	mA
I _{+5V_LDO_OUT_SC}	5V regulator	Short circuit current	145		220	mA
I _{+5V_LDO_OUT}	5V regulator	Maximum current for linear region operation, +5V_LDOs_IN = 5.8V, Output = 4.8V			40	mA
I _{1.5VA/D_SC}	1.5V regulator	Short circuit current. Applies to both +1.5VA_LDO_OUT and +1.5VD_LDO_OUT	40		125	mA
I _{1.5VA}	1.5V regulator	Maximum current for linear region operation. +1.5VA_LDO_IN = 1.8V and +1.5VA_LDO_OUT = 1.48V			25	mA
I _{1.5VA/D}	1.5V regulator	Maximum current for linear region operation. +1.5VD_LDO_IN = 1.8V and +1.5VD_LDO_OUT = 1.4V			15	mA
I _{VREF}	VREF reference	Short circuit current	1.25	2	2.75	mA
I _{+5.25V_LDO_OUT_OPEN}	5.25V regulator low current detection	Light load	0.2		3.6	mA
Regulated Outputs Under-Voltage (UV) and Over-Voltage (OV) Detection						
OV _{+5.25V_LDO_OUT}		VREF = 1.235V	5.65		5.9	V
OV _{+5.25V_LDO_OUT_HYST}		VREF = 1.235V	-0.25	-0.175	-0.08	V
UV _{+5.25V_LDO_OUT}		VREF = 1.235V	4.60		4.85	V
UV _{+5.25V_LDO_OUT_HYST}		VREF = 1.235V	0.07	0.14	0.2	V
OV _{+5V_LDO_OUT}		VREF = 1.235V	5.30		5.75	V
OV _{+5V_LDO_OUT_HYST}		VREF = 1.235V	-0.25	-0.17	-0.08	V
UV _{+5V_LDO_OUT}		VREF = 1.235V	4.35		4.65	V
UV _{+5V_LDO_OUT_HYST}		VREF = 1.235V	0.07	0.14	0.2	V
OV _{+5V}	+5V supply input pins	VREF = 1.235V	5.45		5.7	V
OV _{+5V_HYST}	+5V supply input pins	VREF = 1.235V	-0.09	-0.05	-0.02	V
UV _{+5V}	+5V supply input pins	VREF = 1.235V	4.45		4.7	V
UV _{+5V_HYST}	+5V supply input pins	VREF = 1.235V	0.01	0.045	0.08	V
OV _{+1.5VA_LDO_OUT}		VREF = 1.235V	1.57		1.625	V
OV _{+1.5VA_LDO_OUT_HYST}		VREF = 1.235V	-0.075	-0.05	-0.025	V
UV _{+1.5VA_LDO_OUT}		VREF = 1.235V	1.445		1.487	V
UV _{+1.5VA_LDO_OUT_HYST}		VREF = 1.235V	0.002	0.01	0.019	V
OV _{+1.5VA}	+1.5VA supply input pins	VREF = 1.235V	1.575		1.625	V
OV _{+1.5VA_HYST}	+1.5VA supply input pins	VREF = 1.235V	-0.025	-0.015	-0.005	V
UV _{+1.5VA}	+1.5VA supply input pins	VREF = 1.235V	1.43		1.48	V
UV _{+1.5VA_HYST}	+1.5VA supply input pins	VREF = 1.235V	0.002	0.013	0.025	V
OV _{+1.5VD_LDO_OUT}		VREF = 1.235V	1.6		1.675	V
OV _{+1.5VD_LDO_OUT_HYST}		VREF = 1.235V	-0.075	-0.05	-0.025	V
UV _{+1.5VD_LDO_OUT}		VREF = 1.235V	1.30		1.39	V
UV _{+1.5VD_LDO_OUT_HYST}		VREF = 1.235V	0.015	0.04	0.065	V
OVC _{+1.5VD_LDO_OUT}	Critical over-voltage	VREF = 1.235V	2.4	2.47	2.56	V
T _{LDOs_OT}		+1.5VA, +1.5VD, +5.25V and +5V LDOs over-temperature shutdown threshold (note 1)	140		170	°C
T _{LDOs_OT_HYST}		+1.5VA, +1.5VD, +5.25V and +5V LDOs over-temperature shutdown hysteresis (note 1)		12		°C

Symbol	Parameter	Test Conditions/Comments	Min	Typ	Max	Units
SAR ADCs Reference						
VREF_H	SARs upper reference	REF_IN = 1.235V	1.296	1.3	1.304	V
VREF_HL	SARs references difference	REF_IN = 1.235V. VREF_L = VREF_H - VREF_HL = 0.2V typical	1.094	1.1	1.105	V
ResSAR#	Resolution	As ratio of digital full scale			1/2 ¹⁰	FS
Redundant Bandgap Reference Voltage						
VBG_redundant			1.18	1.2	1.22	V
TMP (Pt100 and Pt1000 Temperature Sensor) Inputs						
ITMP_SRC#_Pt100	Current source output	After calibration, Pt100 mode selected	0.965	1	1.035	mA
ITMP_SRC#_Pt1000		After calibration, Pt1000 mode selected	0.4825	0.5	0.5175	mA
ITMP_SRC#_ACC	Current source accuracy	Over temperature, Pt100 and Pt1000	-3.5		3.5	%
GainPt100	Analog front end gain	Pt100 mode selected		18/3.5		V/V
GainPt1000		Pt1000 mode selected		18/17		V/V
VFSD_Pt100	Differential input voltage	Full scale output, Pt100 mode selected	203.9	213.9	233.9	mV
VZERO_Pt100		Zero output, Pt100 mode selected	-10	0	20	mV
VFSD_Pt1000	Differential input voltage	Full scale output, Pt1000 mode selected	1.019	1.039	1.064	V
VZERO_Pt1000		Zero output, Pt1000 mode selected	-10	0	20	mV
VFULL_Pt	Input voltage range	Relative to GND	0		1.5	V
VCMR_Pt	Common mode rejection	Pt100 common mode = 0.135V to 0.335V Pt1000 common mode = 0.675V to 1.075V	57			dB
IPt_MID	Pin Leakage Current TMP_N#, TMP_P#, TMP_REF#	Interface on and 0V < VPt < 1.5V	-1		4	µA
IPt_FULL		Interface off and 0V < VPt < 1.5V	-0.2		0.2	
LinPt	Relative to full scale	Analog front end gain error from straight line (Pt100)	-1.4		1.4	LSB
SNRPt	Signal to noise ratio (SNR)	Analog front end. Input 0.96Vpk-pk (PT100), 0.196Vpkp-pk (PT1000), bandwidth = 200Hz	60			dB FS
CNP_Pt	Differential input capacitance	TMP_N# to TMP_P#		10		pF
RNP_Pt100	Differential input resistance	TMP_N# to TMP_P#, Pt100 mode selected		200		kΩ
RNP_Pt1000		TMP_N# to TMP_P#, Pt1000 mode selected		1000		kΩ
IWPU_TEMP	Weak pull up current	Floating input detection on TMP_## pins	9	15	23	µA
PRS_SRC# Sources for Pressure or other 4mA - 20mA Sensors						
VPRS_SRC	Voltage drop between VCC and PRS_SRC#	20mA load			0.45	V
MonGainPRS_SRC	Analog front end gain	PRS_SRC# voltage drop monitor amplifier		2.03		V/V
MonAccPRS_SRC	Analog front end Accuracy	At VPRS_SRC = 0.45V, error from nominal 10-bit SAR reading of d'719'	-2.5		2.5	% FS
PRS_P# and PRS_N# (Pressure or other 4mA - 20mA Sensor) Inputs						
VPRS_##	Differential input voltage	Full scale output	1.08	1.10	1.12	V
		Zero output	-0.02	0	0.02	V
	Input voltage range	Relative to GND	0.2		1	
CMRRPRS_##	Common mode rejection		57			dB
IPRS_MID	Input leakage current	Interface on and 0.1V < VPRS_## < 1.4V	-5		8.6	µA
Interface off and 0V < VPRS_P < 1.5V		-0.25		6.25		
		Interface off and 0V < VPRS_N < 1.5V		-0.25		
GainPRS_##	Analog front end gain			1		V/V
LINPRS_##	Linearity rel. to full scale	Gain error from straight line	-1.5		1.5	LSB
SNRPRS_##	Signal to noise ratio (SNR)	Input 1.06Vpk-pk, bandwidth = 200Hz	65			dB
RIN_PRS_##	Input resistance	PRS_P# to GND	200	325	500	kΩ
VCC Monitor SAR ADC Analog Front End						
GainVCC_MON	Divider gain			0.0405		V/V
AccVCC_MON	Divider accuracy	VCC = 10V to 30V. Error from nominal value: SAR Reading = (VCC-4.9)*0.0405*1024/1.1V	-2.5		2.5	%FS

Symbol	Parameter	Test Conditions/Comments	Min	Typ	Max	Units
ISENSE# and ISENSE_RTN Differential Inputs (With Sinc³ Filter set for OSR = 512)						
V _{ISENSE+}	Differential Input voltage corrected with OTP offset values (see ISENSE correction section)	Extrapolated positive full scale	1.082	1.1	1.118	V
V _{ISENSE_OFF}		Offset	-0.008	0	0.008	
V _{ISENSE-}		Extrapolated negative full scale	-1.118	-1.1	-1.082	
V _{ISENSE_RTN}	ISENSE_RTN allowed voltage range		1.2		3.8	V
V _{ISENSE_RTN_CMR}	Common mode rejection	DC	55			dB
I _{ISENSE_RTN_MID}	RTN pin leakage current	Interface on and 0.1V < V _{ISENSE#} < 1.4V	-20		20	μA
I _{ISENSE_RTN_FULL}		Interface off and 0V < V _{ISENSE#} < 1.5V	-1		50	
I _{ISENSE_MID}	Pin leakage current	Interface on and 0.1V < V _{ISENSE#} < 1.4V	-4		4	μA
I _{ISENSE_FULL}		Interface off and 0V < V _{ISENSE#} < 1.5V	-0.2		10	
Gain _{ISENSE#}	Analog front end gain			1		V/V
Lin _{ISENSE#}	Relative to full scale	Gain error from straight line (-1V to +1V)	-175		175	PPM
CH-CH _{ISENSE#}	Matching CH to CH	ISENSE1 to ISENSE2, ISENSE3 to ISENSE4	-0.2		0.2	%
Res _{ISENSE}	Resolution	As ratio of digital full scale (OSR = 256)			1/214	FS
SNR _{ISENSE}	Signal to noise ratio (SNR)	At 5.5 ksps output rate (OSR = 512) in 1 kHz bandwidth	71			dB FS
		At 87.9 ksps output rate (OSR = 32) in 8 kHz bandwidth	70			
C _{IN_ISENSE}	Differential input capacitance	ISENSE# to ISENSE_RTN		10		pF
R _{IN_ISENSE}	Differential input resistance	ISENSE# to ISENSE_RTN		200		kΩ
I _{PU_HV}	Pullup current	Floating input detection on ISENSE# and ISENSE_RTN pins	0.8	1	1.5	mA
Internal Junction Temperature Sensing Analog Front End						
V _{TJ-60°C}	SAR output code at cold	-55°C, external reference	583	603	623	-
V _{TJ+25°C}	SAR output code at 25°C	25°C, external reference	455	475	495	-
V _{TJ+115°C}	SAR output code at hot	110°C	310	340	350	-
HV1 and HV2 Single-Ended SAR ADC Inputs						
V _{HV}	Input voltage	Full scale output	1.28	1.3	1.32	V
		Zero output	-0.006	0	+0.006	
		Range relative to GND	0		1.3	
I _{HV_MID}	Input leakage current	Interface on and 0.1V < V _{HV} < 1.4V	-400		800	nA
I _{HV_FULL}		Interface off and 0V < V _{HV} < 1.5V	-200		200	
Lin _{HV}	Relative to full scale	Gain error from straight line	-1		1	LSB
SNR _{HV}	Signal to noise ratio (SNR)	Input 1.25Vpk-pk, bandwidth = 1kHz	60			dB FS
I _{WPU_HV}	Weak pullup current	Floating input detection on HV# pins	3	5	7	μA
I _{SPU_HV}	Strong pullup current	Short detection on HV# pins	300	400	500	μA
DRV_SNS_## Differential Analog Front End						
V _{DRV_SNS_FULL}	Differential Input voltage	Full scale output	1.065	1.1	1.13	V
V _{DRV_SNS_HALF}		Half scale output	-0.025	0	0.025	
V _{DRV_SNS_ZERO}		Zero output	-1.13	-1.1	-1.065	
V _{FULL_DRV_SNS}	Input voltage range	Relative to GND	0		1.5	V
SNR _{DRV_SNS_DIFF}	Signal to noise ratio (SNR)	DRV_SNS_P# to DRV_SNS_N#, input 1.06Vpk-pk, bandwidth = 1kHz	60			dB FS
THD _{DRV_SNS_DIFF}	Total Harmonic Distortion (THD)	DRV_SNS_P# to DRV_SNS_N#			-53	dB
C _{IN_DRV_SNS}	Diff input capacitance			10		pF
R _{IN_DRV_SNS}	Diff input resistance		2000			kΩ
I _{WPU_DRV_SNS}	Weak pullup current	Floating input detection on DRV_SNS_## pins	3	5	7	μA
I _{SPU_DRV_SNS}	Strong pullup current	Short detection on DRV_SNS_## pins	300	425	600	μA

Symbol	Parameter	Test Conditions/Comments	Min	Typ	Max	Units
LVDT DRV#_# Half Bridge Drivers						
V _{DRV}	High level output voltage	Relative to VFB, sourcing 160mA	-650	-400		mV
	Low level output voltage	Sinking 160mA		400	650	
I _{DRV}	Hi-Z state leakage	Output disabled or powered off, VFB = 0 to 15V	-10		15	μA
t _{PHL}	Propagation delay H to L	PWM edge to DRV#_# edge	130	220	330	ns
t _{PLH}	Propagation delay L to H	PWM edge to DRV#_# edge	130	220	330	ns
t _{PHL,PLH}	Propagation delay	Matching between DRV#_P and DRV#_#N	-60		60	ns
OC _{DRV#_#}	Over-current detection			330		mA
LVDT_P#, LVDT_N# Differential Inputs and LVDT_CM# Outputs (With Sinc³ Filter set for OSR = 256)						
V _{LVDT#_CM}	Regulated V _{CM} for secondary windings		0.73	0.75	0.77	V
I _{LVDT#_CM}	Load current range	For a common mode error of 20mV	-1		1	mA
V _{LVDT#+}	Differential Input voltage	Extrapolated positive full scale	1.07	1.1	1.13	V
V _{LVDT#_OFFSET}		Offset	-0.025	0	0.025	
V _{LVDT#-}		Extrapolated negative full scale	-1.13	-1.1	-1.07	
V _{LVDT_CMR}	Common mode rejection	DC	40			dB
I _{LVDT_MID}	Pin leakage current	Interface on and 0.1V < V _{ISENSE#} < 1.4V	-1		1	μA
I _{LVDT_FULL}		Interface off and 0V < V _{ISENSE#} < 1.5V	-0.4	0	0.4	
I _{inLVDT#}	Relative to full scale	Gain error from straight line (-1V to +1V)	-120		120	PPM
CH-CH _{LVDT#}	Matching CH to CH	CH1 to CH2, CH3 to CH4	-0.07		0.07	%
Res _{LVDT}	Resolution	As ratio of digital full scale (OSR = 256)			1/2 ¹⁴	FS
SNR _{LVDT}	Signal to noise ratio (SNR)	At 11ksps output rate (OSR = 256) in 1 kHz bandwidth	70			dB FS
		At 87.9ksps output rate (OSR = 32) in 8 kHz bandwidth	70			dB FS
C _{in_LVDT}	Differential input capacitance				5	pF
R _{in_LVDT}	Differential input resistance		1000			kΩ
I _{WPU_LVDT}	Weak pullup current	Floating input detection on LVDT_### pins	3	5	7	μA
HEP# Hall Effect Inputs						
V _{LOG_IN_HALL}	Input Logic Threshold	V _{IH}			4	V
		V _{IL}	1			
		Hysteresis	1.9	2.2		
I _{LOG_IN_HALL}	Input current	0V	-1	0	1	μA
		5V	9	15	22	
T _D	Input to logic output delay	Output GPIO loaded with ≤ 100pF			0.2	μs
Buck Regulator						
V _{BUCK_VFB_L}	Feedback target	BUCK_VFB pin	1.11	1.135	1.16	V
V _{BUCK_VFB_H}	Feedback target threshold voltage high	BUCK_VFB pin	1.13	1.155	1.18	V
V _{BUCK_VFB_HYST}	Feedback Hysteresis		10	17	25	mV
OV _{BUCK_VFB}	Over-voltage detection	BUCK_VFB pin	1.40	1.435	1.48	V
UV _{BUCK_VFB}	Undervoltage detection	BUCK_VFB pin	1.01	1.04	1.07	V
Load_Reg _{BUCK}	Load regulation	L _{BUCK} = 100μH, C _{OUT} = 10μF, load step = 30mA		10		%
Line_Reg _{BUCK}	Line regulation	L _{BUCK} = 100μH, C _{OUT} = 10μF, line step = 1V		10		%
I _{LIM}	Output current limit			500		mA
T _{START}	Output ramp-up time			1		ms
T _{OFF}	Switch off time			4		μs
T _{BUCK_OT}		Over-temp shutdown threshold (note 1)	140		170	°C
T _{BUCK_OT_HYST}		Over-temp shutdown hysteresis (note 1)		12		°C

Symbol	Parameter	Test Conditions/Comments	Min	Typ	Max	Units
Power-On-Reset (POR)						
t _{POR}	Power on reset delay	With C _{POR} = 1nF from POR pin 130 to GND	0.7	1.3	2.0	ms
Clocks						
F _{OSC}	Oscillator frequency	System clock at OSC1 and OSC2 pins	20	22.5	30	MHz
OV _{+1.5VOSC}	Crystal supply +1.5VOSC		1.61		1.67	V
OV _{+1.5VOSC HYST}	Crystal supply +1.5VOSC		-0.030	-0.015	-0.005	V
UV _{+1.5VOSC}	Crystal supply +1.5VOSC	Disables crystal oscillator	1.300		1.39	V
UV _{+1.5VOSC HYST}	Crystal supply +1.5VOSC		0.002	0.015	0.025	V
V _{OSC1_TH}	OSC1 Input Threshold	OSC2 = 0.75V	0.4	0.6	0.8	V
V _{OSC2_1.5V}	OSC2 Output Level	High level (0.2mA source)	1.3	1.45		V
		Low level (0.2mA sink)		0.02	0.1	
	Oscillator Transconductance	For OSC1 voltage 0.2V to 1V	3	6	12	mA/V
F _{PWM}	PWM frequency		5	10	20	kHz
F _{LVDT_PWM}	PWM for LVDT sinewave driver		100	200	300	kHz
F _{SAMPLE}	Σ-Δ modulator sample clock	As a multiple of F _{OSC} frequency		1/12		-
F _{PLL}	Internal PLL	Equals 4 x F _{OSC}	80	90	120	MHz
T _{Lock}	PLL Lock time	Supplies stable, time from clock restart to PLL Lock = 1;			0.5	ms
F _{WD}	Internal watchdog frequency		400	450	520	kHz
GPIO, SPI, PWM, Other Digital Interface Pins (VDD domain)						
V _{LOG_IN}	Input Logic Threshold	V _{IH} ; VDD = 2.25,3.3V			66	%VDD
		V _{IL} VDD = 2.25,3.3V	22			
		Hysteresis VDD = 2.25	7.9	18	30	
		Hysteresis VDD = 3.3V	10	20	35	
V _{LOG_IN}	Input Logic Threshold	V _{IH} ; VDD = 5.5V			66	%VDD
		V _{IL} VDD = 5.5V	20			
		Hysteresis VDD ≤ 3.3V	15	20	40	
V _{LOG_OUT}	Logic Output Levels	High logic level (1mA source)	VDD - 0.25	VDD - 0.05	VDD	V
		Low logic level (1mA sink)	0	0.05	0.25	
I _{LOG_OUT_FAULT}	GPIO output short circuit current	High logic level short to 0V (VDD = 3.3V)	-31	-23	-15	mA
		Low logic level short to VDD (VDD = 3.3V)	15	23	31	
I _{LOG_IN_RESET}	Input current	RESET = 0V, VDD = 5.5V	-30	-18	-10	μA
		RESET = VDD = 5.5V	-1	0	1	
I _{LOG_IN}	Input current	V _{LOG_IN} = 0V	-1	0	1	μA
I _{GPIO_IN}	Input current	V _{GPIO_IN} = 5.5V (GPIO pulldown disabled)	-1	0	1	μA
R _{PD_IO}	I/O pulldown resistor	All digital inputs, GPIO when enabled via GPIO_REG4 (VDD = 5.5V)	200	325	450	kΩ
F _{UART}	UART baud rate	Tested to 115,200 bps			1	Mbps
f _{SCLK}	SCLKx Clock Frequency	Loading on MISOx ≤ 10pF			30	MHz
t _{CH}	SCLKx Pulse Width High		10			ns
t _{CL}	SCLKx Pulse Width Low		10			ns
t _{CSS}	SSx Fall to SCLKx Rise Setup Time	F _{OSC} = 25MHz, PLL mode	15			ns
		F _{OSC} = 25MHz, PLL bypass mode				
t _{CSW}	Minimum SSx Pulse High		4 / F _{OSC}			ns
t _{CSH}	SCLKx Fall to SSx Rise Hold Time	Guaranteed by design, not tested	0			ns
t _{DS}	MOSIx Setup Time		4			ns
t _{DH}	MOSIx Hold Time		1.5			ns
t _{SSDO}	SSx Fall to MISOx Output Propagation Delay				190	ns

Symbol	Parameter	Test Conditions/Comments	Min	Typ	Max	Units
t_{DO}	MISOx Output Propagation Delay from SCLK	Loading on MISOx $\leq 10\text{pF}$ (note 1)			21	ns
t_{FT}	MISOx Output Rise and Fall Times	Loading on MISOx $\leq 10\text{pF}$ (note 1)	1		6	ns

¹ Guaranteed by design and characterisation, but not production tested

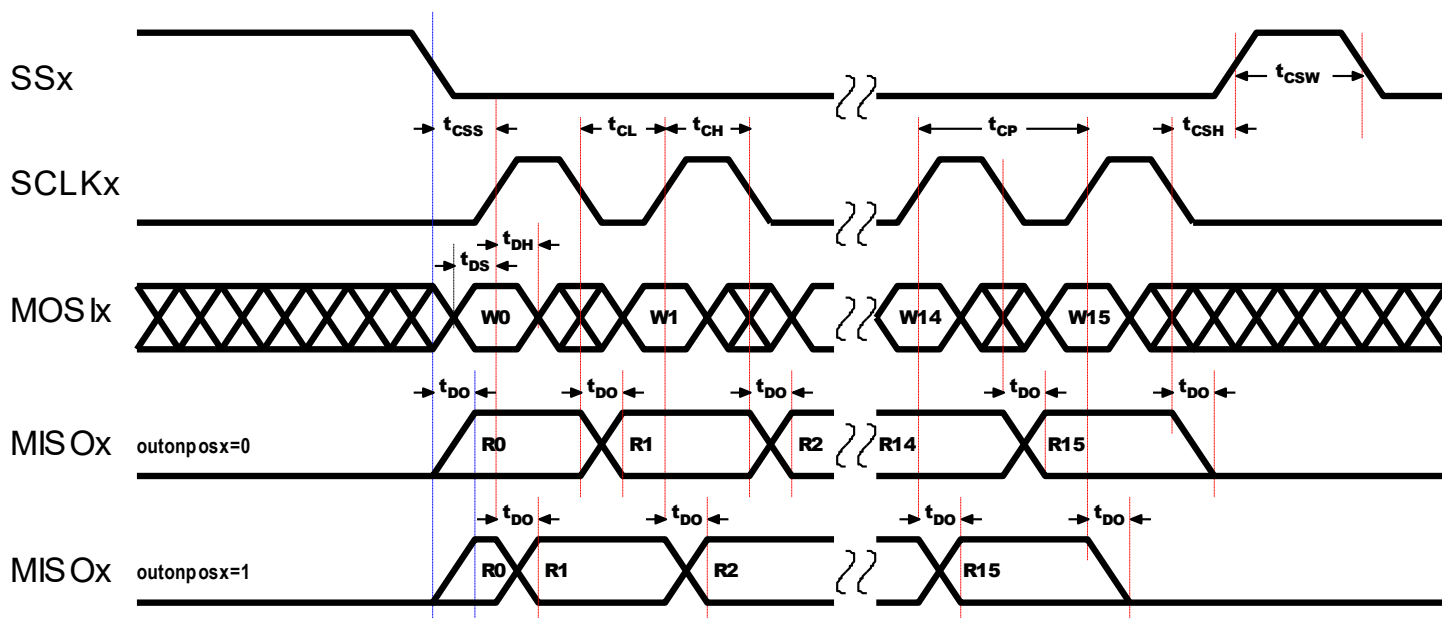


Figure 1. SPI Timing

8 Thermal Properties

Thermal resistance, θ_{JB} , is provided from die to the back surface of the package. Junction temperature T_J is calculated using $T_J = T_B + (PD \times \theta_{JB})$, where T_B is the temperature maintained on the back surface of the package.

Package	Thermal Resistance	Typ	Units
LQFP-144	θ_{JB}	5	$^{\circ}\text{C/W}$

9 Functional Block Diagram

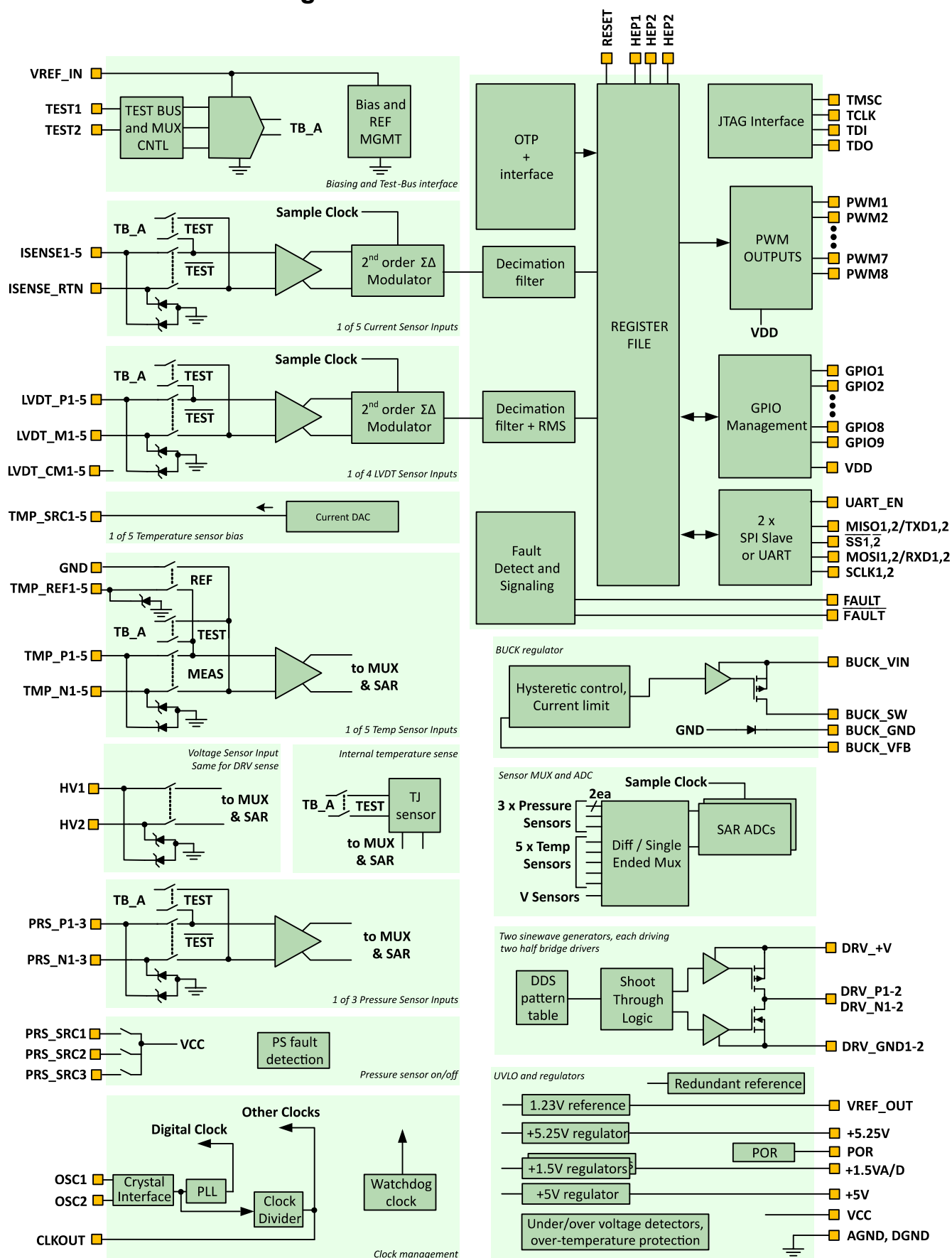


Figure 2. Functional Block Diagram

10 Typical Applications

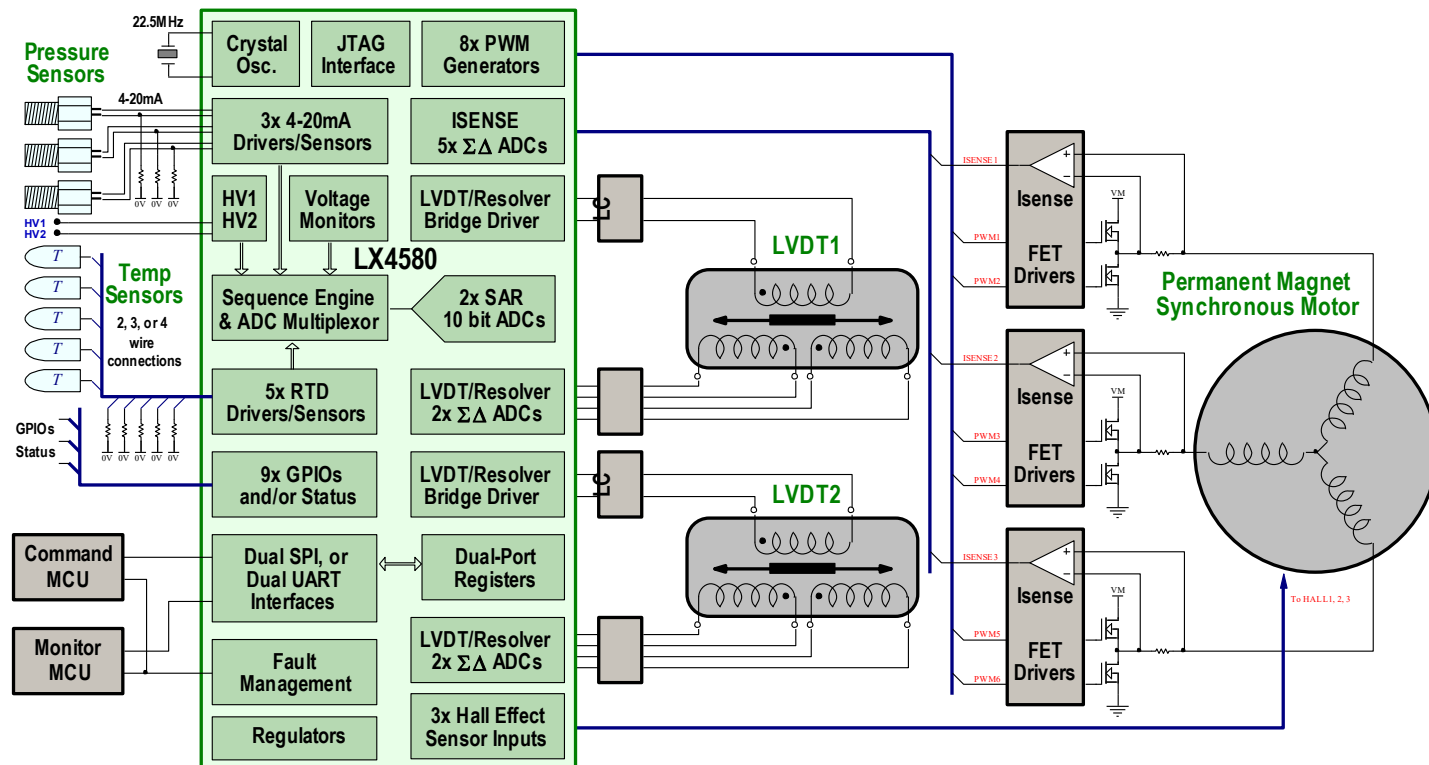


Figure 3. Typical Application for PMSM with In-Phase Current Sensing and Two LVDTs

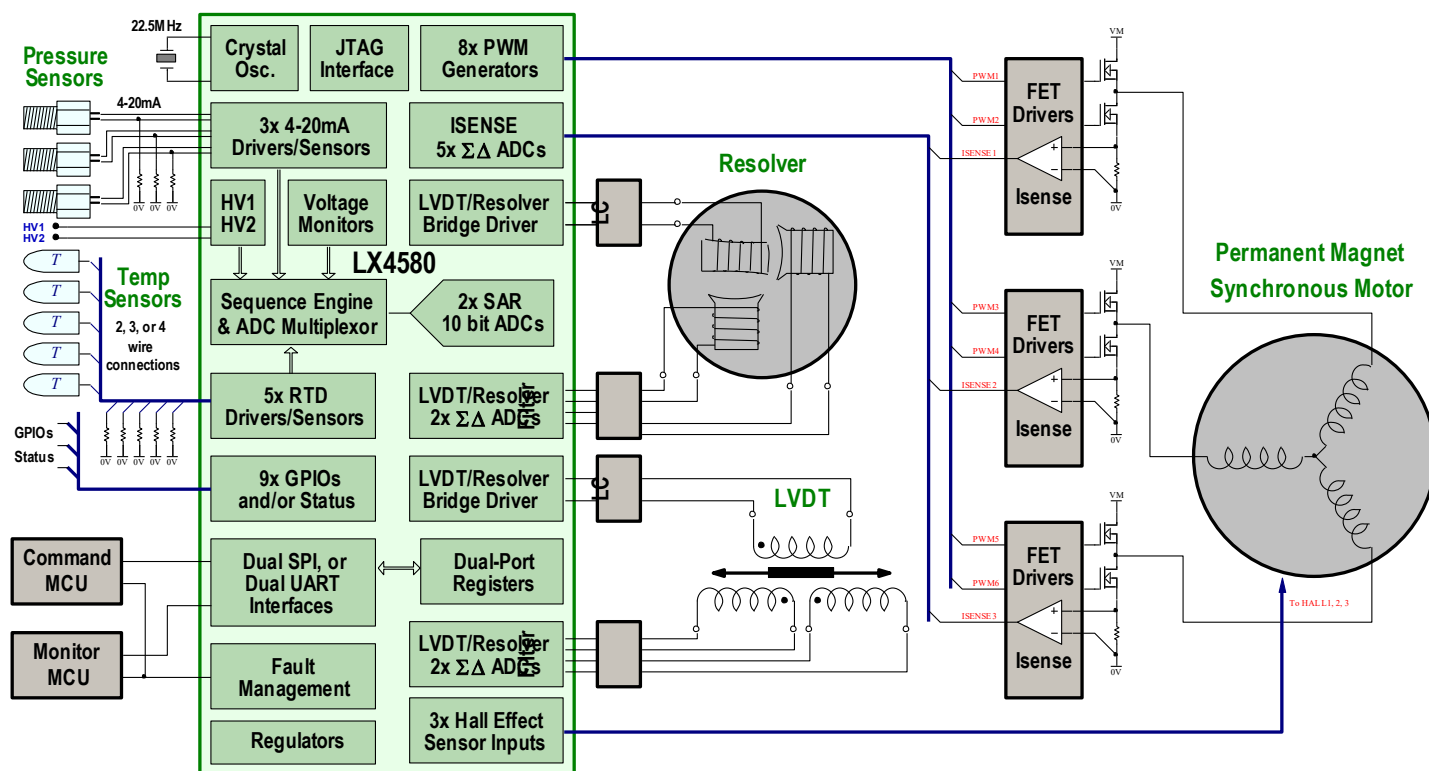


Figure 4. Typical Application for PMSM with Ground-Side Current Sensing, a Resolver and an LVDT

11 LX4580 System Blocks

The sections covering LX4580 main system blocks are listed below to assist navigation:

Section 11.1: LX4580 Supplies
 Section 11.2: LX4580 Supply Rail Fault Management
 Section 11.4: Voltage Reference (VREF_OUT and VREF_IN Pins)
 Section 11.3: Hysteretic Buck Converter
 Section 11.5: Clock Generator (OSC1 and OSC2 pins)
 Section 11.6: RESET Input
 Section 11.7: UNLOCK Input
 Section 11.8: FAULT and FAULT Outputs
 Section 11.10: GPIO Pins
 Section 11.11: UART_EN Input
 Section 11.9: JTAG Interface
 Section 11.12: SPI and UART Interfaces
 Section 11.13: Pulse Width Modulated (PWM) Outputs
 Section 11.14: 10-Bit SAR Analog-to-Digital Converters
 Section 11.15: Σ - Δ Analog-to-Digital Converters
 Section 11.16: 4-20mA Current Loop (Pressure Sensor) Interfaces
 Section 11.17: Hall Effect Comparator Inputs
 Section 11.18: Temperature Sensor Interfaces
 Section 11.19: HV1 and HV2 General Purpose ADC Inputs
 Section 11.20: ISENSE Current Sensing Interfaces
 Section 11.21: LVDT/RVDT/Resolver Interface

Section 12 on page 42 discusses LX4580 operating modes: Startup Mode, Functional Mode, and Safe Mode.
 Section 13 on page 43 provides details of registers.

11.1 LX4580 Supplies

The LX4580 requires several external supply rails, and generates several supply rails with internal low-drop-out (LDO) linear regulators, as shown in Table 1 below.

Table 1. Input Supply Rails

Rail	Pins	Supply Range	Description
VCC	144	10V to 30V	Analog high voltage supply, typically 15V
BUCK_VIN	136	0V to VCC	Optional buck regulator input supply, typically VCC. See section 11.3 on page 23
VFB	72	10V to 30V	Resolver/LVDT primary drive supply, typically 15V
VDD	82, 110	2.25V to 5.5V	Logic I/O supply, typically a nominal 2.5V, 3.3V, or 5V
+5V_LDOs_IN to +5V_LDO_OUT, +5.25V_LDO_OUT	141	6.2V to 17.5V	Input to LX4580's internal 5V analog LDO, output at +5V_LDO_OUT pin 142
			Input to LX4580's internal 5.25V auxiliary LDO, output at +5.25V_LDO_OUT pin 140
+1.5VA_LDO_IN to +1.5VA_LDO_OUT	132	1.85V to 5.5V	Input to LX4580's internal 1.5VA analog core supply LDO, output at +1.5VA_LDO_OUT pin 133. +1.5VA_LDO_IN is normally connected to +5V_LDO_OUT pin 142
+1.5VD_LDO_IN to +1.5VD	122	1.85V to 5.5V	Input to LX4580's internal 1.5VD digital core supply LDO, output at +1.5VD pins 80 and 121. +1.5VD_LDO_IN is normally connected to +5.25V_LDO_OUT pin 140

The 5V and 5.25V LDOs are supplied at a common input pin, +5V_LDOs_IN. Each LDO has an internal reverse-biased diode from its output to the common input, so on power-down the 5V and 5.25V outputs will fall together regardless of the relative loadings. The LX4580 includes a buck regulator block (section 11.3 on page 23), intended to be used to pre-regulate VCC to a low voltage, such as 7V, as input to these two LDOs to reduce dissipation. This isn't mandatory, however, and the buck regulator block can be allocated to a different purpose or not used at all.

The 5V analog supply at pins 36, 68, and 131 are normally connected to the output of the internal +5V LDO at +5V_LDO_OUT pin 142. The 5.25V LDO output is not used internally, but is provided to supply up to 25mA for external circuits such as Hall Effect sensors.

Figure 5 below shows a typical power supply setup, with decoupling.

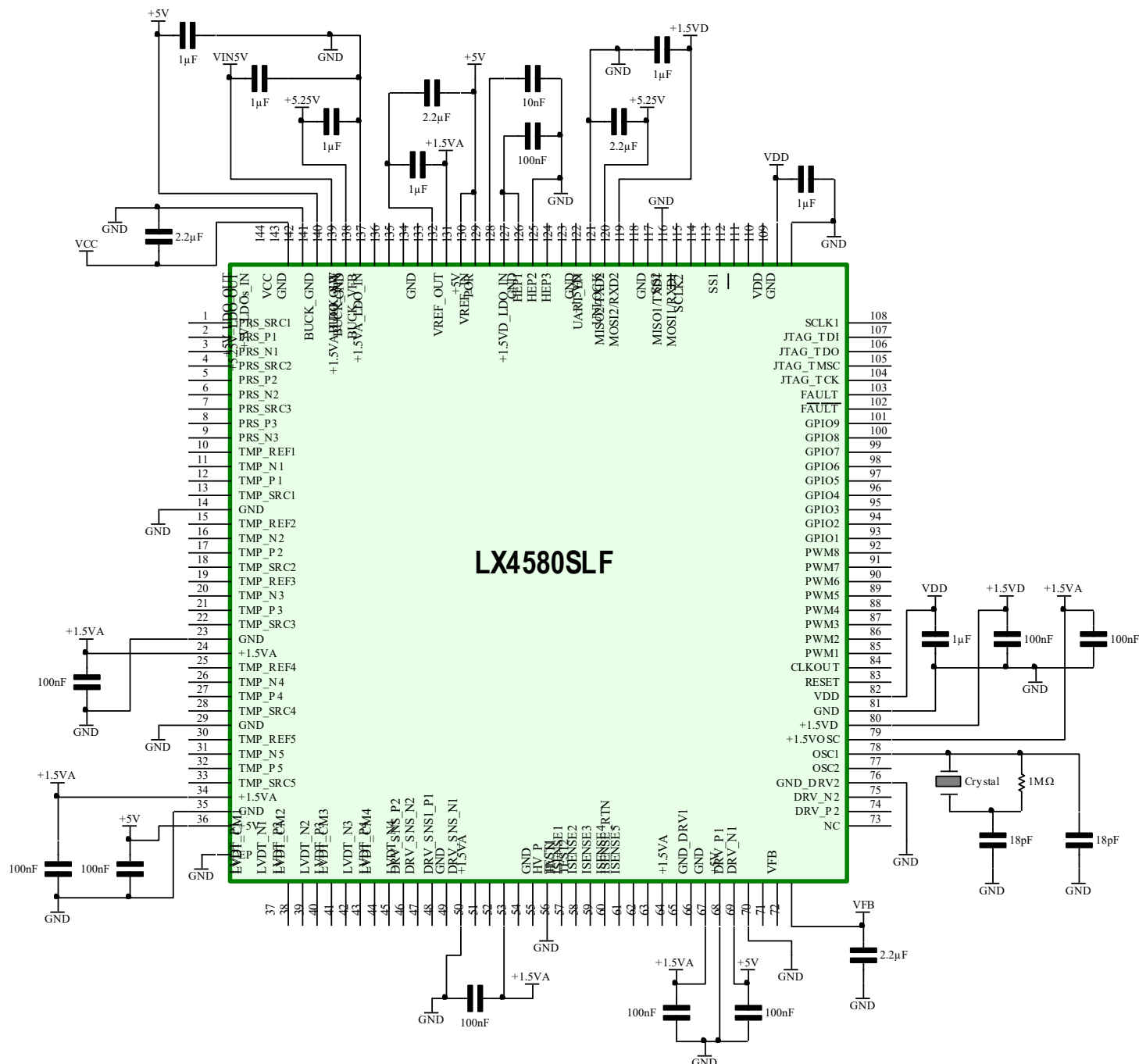


Figure 5. Typical Power Supply and Reference Decoupling and Crystal Oscillator

The VIN5V supply at the top left to +5V_LDOs_IN pin 141 can be supplied by the buck regulator generating a nominal 7V, as shown in the example circuit Figure 7 on page 24. The pre-regulator architecture is optional, but is recommended to reduce LDO dissipation. This setup is shown below in block diagram form in Figure 6 on page 21, with the buck regulator providing 7V for the 5V and 5.25V LDOs.

The 1.5VA analog and 1.5VD digital LDOs are intended to be operated from the 5V and 5.25V LDO outputs respectively. The reverse protection diodes around the 5V and 5.25V regulators make these two LDO outputs follow each other down on power-off, and consequently the 1.5VA and 1.5VD LDO outputs will also follow each other down. For power-off, the two 1.5V rails need to remain up until the 5V supply has dropped to 2V or lower. This supply rail sequencing happens automatically with the series-LDO topology. There is no other supply rail sequencing requirement.

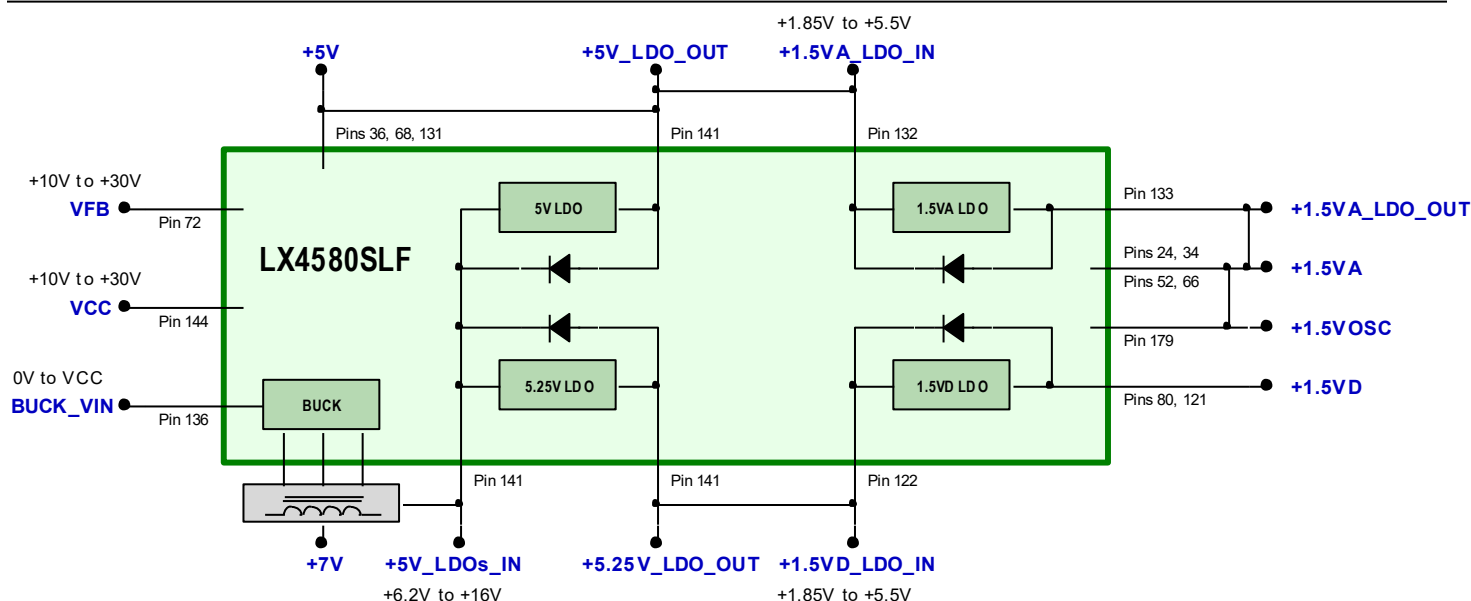


Figure 6. Typical Power Supply Interconnections

11.2 LX4580 Supply Rail Fault Management

The LX4580 includes under- and over-voltage (UV/OV) detectors on power rails to detect out-of-specification conditions, plus over-temperature (OT) detection for the internal regulators. Table 2 below summarizes the registers that provide power rail status.

Table 2. Supply Rail Fault Management

Rail	UV/OV Status Register	UV/OV Fault Register	OT Status Register	OT Fault Register		
VDD	STATUS_REG0 (page 46)	CRITICAL_STATUS (page 65)	Not applicable (external supplies)			
VCC						
VFB	STATUS_REG1 (page 47)	FAULT_STATUS1 (page 59) VFB UV/OV is latched in FAULT_STATUS1 after a delay count in GLITCH_REG10 (page 55)	STATUS_REG4 (page 48)	Delay count in GLITCH_REGF (page 55) before latching in FAULT_STATUS3 (page 63)		
Buck Regulator						
+5V_LDOs_IN						
+5V_LDO_OUT						
+5.25V_LDO_OUT						
+1.5VOSC	STATUS_REG5 (page 49)	VCC UV is latched in FAULT_STATUS3 (page 63) both before and after a delay count in GLITCH_REGB (page 53)	STATUS_REG4 (page 48)	Delay count in GLITCH_REGF (page 55) before latching in FAULT_STATUS3 (page 63)		
+5V						
+1.5VA						
+1.5VA_LDO_IN						
+1.5VD_LDO_IN						
+1.5VA_LDO_OUT	STATUS_REG0 (page 46)	VCC UV is latched in FAULT_STATUS3 (page 63) both before and after a delay count in GLITCH_REGB (page 53)	STATUS_REG4 (page 48)	Delay count in GLITCH_REGF (page 55) before latching in FAULT_STATUS3 (page 63)		
+5V startup supply						
+1.5VD	POR_REG1 (page 45)				CRITICAL_STATUS (page 65)	

A general overview of supply rail fault management is as follows:

- Real-time fault status is available in Status registers (section 13.3 on page 46)
- The first occurrence of a fault is latched in a Fault register (section 0 on page 56)
 - A fault latched in a FAULT_STATUS register is cleared by writing the corresponding FAULT_CLEAR register
 - Some faults have to persist for a short time before latching a fault, managed by Glitch filters
 - The 5V and 5.25V supplies share a latched fault bit, as do the 1.5VA and 1.5VD supplies
 - Noisy supplies may trip random under- or over-voltage faults which don't persist long enough for the host system to identify the issue(s) when Status registers are examined.
 - Faults can be masked as to whether they cause the LX4580 to initiate Safe Mode. Operating modes, including Safe Mode, are discussed in section 12 on page 42
- Linear regulator over-temperature fault status can be routed to GPIOs (sections 11.10 on page 25, 13.11 on page 83)

- Failure of either the VDD external logic supply, the 1.5VD internal logic supply, or the clock source at OSC1 are deemed critical faults latched into the CRITICAL_STATUS register (section 11.2.1 below). Any one of these faults causes the LX4580 to shut down and restart in an attempt to clear the unsafe condition
- The LX4580 also reports a light load on the +5.25V supply (under a threshold in the 200µA to 2mA tolerance range) in the STATUS_REG5 register (section 13.3.6 on page 49)

11.2.1 CRITICAL SUPPLY FAULTS - 1.5VD AND VDD UNDER- AND OVER-VOLTAGE FAULTS

Two supply under- or over-voltage conditions are deemed critical faults, and will cause the LX4580 to shut down and restart in an attempt to clear the unsafe condition:

- The VDD external logic supply, with status indicated in the STATUS_REG0 register (section 13.3.1 on page 46), or
- The 1.5VD internal logic supply, with status indicated in the POR_REG1 register (section 13.2.1 on page 45)

Critical faults are alerted in the CRITICAL_STATUS register (section 13.5.13 on page 65). All registers except CRITICAL_STATUS lose their data, and both the FAULT pin 103 and the $\overline{\text{FAULT}}$ pin 102 go low to signal a critical fault. The serial busses are also disabled during critical fault, and the external system must determine and correct the fault(s) before the LX4580 can be accessed. The LX4580 will indicate recovery by taking the FAULT pin high. The CRITICAL_STATUS register can then be read to check which critical faults were latched.

11.2.2 +5V AND +5.25V REGULATOR UNDER- AND OVER-VOLTAGE FAULTS

The Fault_+5V bit in the FAULT_STATUS1 register (section 13.5.4 on page 59) is latched when one or more of the following supply faults is detected, even if transiently:

- The shared input supply to the 5V and 5.25V regulators had an under- or over-voltage condition
 - Bits +5V_LDOs_IN_UV and +5V_LDOs_IN_OV in the STATUS_REG1 register (section 13.3.2 on page 47) provide real-time status
- The 5.25V regulator output had an under- or over-voltage condition
 - Bits +5.25V_UV and +5.25V_OV in the STATUS_REG1 register provide real-time status
- The 5V regulator output had an under- or over-voltage condition
 - Bits +5V_UV and +5V_OV in the STATUS_REG1 register provide real-time status
- The 5V internal startup supply had an under- or over-voltage condition
 - Bits VC5_UV and VC5_OV in the STATUS_REG0 register (section 13.3.1 on page 46) provide real-time status

11.2.3 +1.5VA AND +1.5VD REGULATOR AND +1.5VOSC SUPPLY UNDER- AND OVER-VOLTAGE FAULTS

The Fault_+1.5V bit in the FAULT_STATUS1 register (section 13.5.4 on page 59) is latched when one or more of the following supply faults is detected, even if transiently:

- The 1.5VA regulator input had an under- or over-voltage condition
 - Bits +1.5VA_LDO_IN_UV and +1.5VA_LDO_IN_OV in the STATUS_REG0 register (section 13.3.1 on page 46) provide real-time status
- The 1.5VA regulator output had an under- or over-voltage condition
 - +1.5VA_LDO_OUT_UV in the STATUS_REG0 register and +1.5VA_LDO_OUT_OV in the STATUS_REG1 register (section 13.3.2 on page 47) provide real-time status
- The 1.5VD regulator input had an under- or over-voltage condition
 - Bits +1.5VD_LDO_IN_UV and +1.5VD_LDO_IN_OV in the STATUS_REG0 register (section 13.3.1 on page 46) provide real-time status

An under- or over-voltage condition on the 1.5VD regulator output is deemed a critical fault, as discussed in section 11.2.1 above.

The Fault_+1.5VOSC bit in the FAULT_STATUS1 register (section 13.5.4 on page 59) is latched when the +1.5VOSC supply has an over-voltage condition. The +1.5VOSC_OV bit in the STATUS_REG1 register (section 13.3.2 on page 47) provides real-time detector status.

11.2.4 VCC UNDER- AND OVER-VOLTAGE FAULTS

The Fault_VCC_OV bit in the FAULT_STATUS1 register (section 13.5.4 on page 59) is latched when an over-voltage condition is detected on VCC, even if transiently. The Spike_VCC_UV bit in the FAULT_STATUS3 register (section 13.5.10 on page 63) is latched when an under-voltage condition is detected on VCC, even if transiently. The GLITCH_REGB register (section 13.4.11 on page 53) reports the number of counts of the $F_{\text{osc}} / 1024$ debounce clock

that have accumulated since an under-voltage was detected. If the count reaches a value of $31 \times 1024 / F_{osc}$ (1.24ms for $F_{osc} = 25.6\text{MHz}$), then a further fault is latched in the Fault_VCC_UV bit in FAULT_STATUS3.

Bits VCC_UV and VCC_OV in the STATUS_REG0 register (section 13.3.1 on page 46) provide real-time VCC under- and over-voltage status.

11.2.5 VFB UNDER- AND OVER-VOLTAGE FAULTS

The Fault_VFB in the FAULT_STATUS1 register (section 13.5.4 on page 59) is latched when an under- or over-voltage condition has detected on VFB for longer than a debounce delay. The GLITCH_REG10 register (section 13.4.16 on page 55) reports the number of counts of the $F_{osc} / 1024$ debounce clock that have accumulated since an under- or over-voltage was detected. If the count reaches a value of $31 \times 1024 / F_{osc}$ (1.24ms for $F_{osc} = 25.6\text{MHz}$), then the Fault_VFB fault is latched.

Bits VFB_UV and VFB_OV in the STATUS_REG1 register (section 13.3.2 on page 47) provide real-time VFB under- and over-voltage status.

11.2.6 BUCK REGULATOR UNDER- AND OVER-VOLTAGE FAULTS

The Fault_BUCK bit in the FAULT_STATUS1 register (section 13.5.4 on page 59) is latched when an under- or over-voltage condition is detected on the feedback pin of the buck converter, BUCK_VFB pin 135. The thresholds are typically 1.04V and 1.44V. To put the thresholds into perspective, the buck converter regulates keeping BUCK_VFB at around 1.147V. Taking the example circuit Figure 7 on page 24 which regulates 7V, the under- or over-voltage trip points would

be typically $7V \times \frac{1.04V}{1.147V} = 6.35V$ and $7V \times \frac{1.44V}{1.147V} = 8.79V$ respectively.

11.2.7 INTERNAL REGULATOR OVER-TEMPERATURE FAULTS

The Fault_OT bit in the FAULT_STATUS3 register (section 13.5.10 on page 63) is latched when an over-temperature fault is detected on one or more of the four internal linear regulators (+5.25V, +5V, +1.5VD, +1.5VA) or the buck pass transistor for longer than a debounce delay. The GLITCH_REGF register (section 0 on page 55) reports the number of counts of the $F_{osc} / 8$ debounce clock that have accumulated since an over-temperature was detected. If the count reaches a value of $31 \times 8 / F_{osc}$ (9.7μs for $F_{osc} = 25.6\text{MHz}$), then the Fault_OT fault is latched. Regulators cut off when over-temperature is detected, and restart automatically when the temperature drops to a safe level. The STATUS_REG4 register (section 13.3.5 on page 48) identifies regulators in over-temperature shutdown:

- The +5V_+5.25_OT bit provides joint real-time over-temperature status for the +5V and +5.25V LDO regulators
 - Fault status can be routed to GPIO2 (section 13.11 on page 83)
- The +1.5VD_LDO_OT bit provides real-time over-temperature status for the +1.5VD LDO regulator
 - Fault status can be routed to GPIO7
- The +1.5VA_LDO_OT bit provides real-time over-temperature status for the +1.5VA LDO regulator
 - Fault status can be routed to GPIO4
- The BUCK_OT bit provides real-time over-temperature status for the buck regulator
 - Fault status can be routed to GPIO6

11.3 Hysteretic Buck Converter

The LX4580 includes a general purpose hysteretic buck converter, generally intended to operate as a typically 7V pre-regulator for the 5V and 5.25V LDO regulators from the typically 15V analog supply. Figure 7 below shows a typical circuit generating 7V for this purpose, as used on the LX4580 evaluation board. This circuit, using a 10mm x 10mm x 4.5mm size inductor with 2.8Ω ESR, provides a flat efficiency of about 83% over the load range up to 120mA and about 85mV p-p output ripple voltage.

A hysteretic buck does not operate a closed loop for output voltage regulation, but simply performs power cycles when out of regulation. Out of regulation is detected here when the voltage at the BUCK_VFB pin is less than the VBUCK_VFB_L threshold, typically 1.135V. In-regulation is detected when the voltage at the BUCK_VFB pin is higher than the VBUCK_VFB_H threshold, which is 10mV to 25mV higher. This hysteresis means that in normal operation the buck's

output voltage ripple will be at least $\Delta V = \frac{10\text{mV}}{1.135V} = 0.88\%$ and can be as high as $\Delta V = \frac{25\text{mV}}{1.135V} = 2.2\%$. This

architecture targets pre-regulator applications rather than precisely regulated voltages.

A buck power cycle starts by turning on the internal high-side power switch which connects the BUCK_VIN pin to the BUCK_SW pin. Current will ramp up through the series inductor from the V_{BK} supply to the output capacitor and load until either output voltage reaches regulation or the internal nominal 500mA current limit is reached. When one of these conditions occurs, the high-side power switch is turned off, and the inductor current will ramp down into the output capacitor and load through the external commutation diode.

If the power cycle stopped because the output voltage reached regulation, meaning that the voltage at the BUCK_VFB pin reached {1.135V + hysteresis}, then power cycles are stopped until out of regulation is detected again (BUCK_VFB at 1.135V). If the power cycle stopped because the 500mA current limit was reached, then after a typically 40μs off-time, another power cycle is initiated. The power cycles repeat until in-regulation is detected. Operating frequency for Figure 7 typically varies from 250Hz at no load to 14kHz at high load.

Set the output voltage with the equation $V_{OUT} = 1.147 \times \frac{R1 + R2}{R2} V$ where R1 and R2 are the feedback resistors as

shown in Figure 7. In the Figure 7 example, the output voltage is set to $V_{OUT} = 1.147 \times \frac{51k + 10k}{10k} = 7V$.

If the buck regulator is unused, leave the BUCK_VIN pin 136 and BUCK_SW pin 137 open, and tie BUCK_VFB pin 135 to GND together with the associated GND pins 138 and 139.

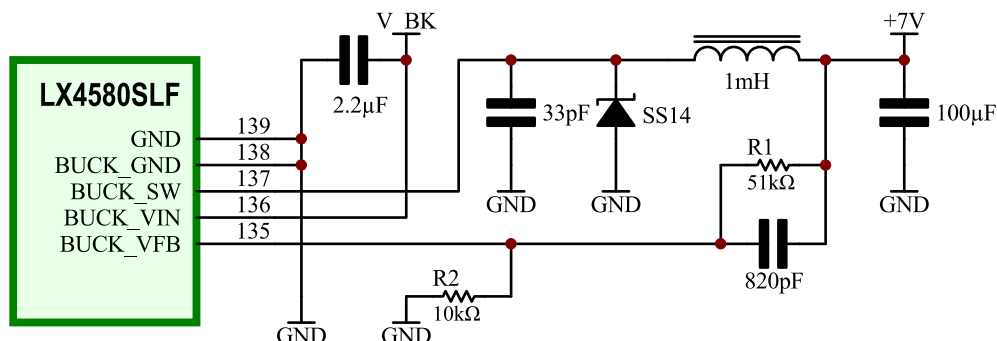


Figure 7. Typical Buck Application Generating 7V to Power the 5V and 5.25V LDOs

11.4 Voltage Reference (VREF_OUT and VREF_IN Pins)

The LX4580 includes a 1.235V internal voltage reference at the VREF_OUT pin 129. To use the internal voltage reference, connect VREF_IN pin 128 to VREF_OUT. To use an external reference voltage, connect the reference to VREF_IN. VREF_OUT must be bypassed with a 100nF capacitor from VREF_OUT to GND pin 127 even if it is not connected to VREF_IN because the internal reference is used for internal rail under- and over-voltage detection.

An additional internal bandgap, V_{BG_redundant} provides a 1.2V ±20mV backup reference voltage that can be switched in to VREF_IN via the CONTROL_REG2 register (section 13.6.3 on page 67) to provide redundancy. V_{BG_redundant} can also be measured via one of the 10-bit SAR ADCs for monitoring.

11.5 Clock Generator (OSC1 and OSC2 pins)

The LX4580 contains a crystal oscillator amplifier between OSC1 and OSC2 to generate the internal clocks. Alternatively, the input OSC1 can be driven by a 1.5V CMOS external clock. The allowed frequency range is 20MHz to 30MHz using either a crystal or an external clock source. The CLKOUT pin provides a buffered copy of the clock by default, unless disabled by the CLKOUT_Disable bit in the CONTROL_REG2 register (section 13.6.3 on page 67). Clock failure is a critical fault, causing the LX4580 to shut down and restart to try to clear the condition (section 13.6.13 on page 60).

The PWM logic can be clocked at 4x the OSC1 frequency to increase PWM resolution using an internal PLL. Enable the PLL in CLKGEN_REG0 (section 13.7.1 on page 68) as part of the initial post power-up register configuration. The PLL lock status is available in the PLL_LOCK bit in the STATUS_REG0 register (section 13.3.1 on page 46), and can be optionally routed to GPIO2 if a logic status output is needed (sections 11.10 on page 25, 13.11 on page 83). The PLL going out of lock is latched as the PLL_Unlocked bit in the FAULT_STATUS3 register (section 13.5.10 on page 63).

11.6 RESET Input

The LX4580's RESET input pin 83 has a 50k Ω internal pullup that ensures that the part is in reset mode if the pin is open. The LX4580 is designed for redundant operation. Analog inputs can be cold spared. Resolver/LVDT drivers, PWM outputs, serial bus outputs, and GPIOs are also high-Z when either VDD is off or the RESET input is high.

The GLITCH_REG3 register (section 13.4.4 on page 51) sets a debounce delay before a logic high input on the RESET input is accepted and the LX4580 is reset. The GLITCH_REG4 register (section 13.4.4 on page 51) provides the current debounce count between the RESET input being taken high and a reset event being triggered.

11.7 UNLOCK Input

The LX4580's UNLOCK input pin 119 has a 50k Ω internal pulldown to default lock mode if the pin is open. Certain critical functions such as programming the internal OTP are enabled when UNLOCK is high. A logic transition from low to high on UNLOCK is also latched in the UNLOCK_High bit in the FAULT_STATUS2 register (section 13.5.7 on page 61).

11.8 FAULT and $\overline{\text{FAULT}}$ Outputs

The LX4580 offers comprehensive fault detection not only for internal operation but also whether external signal inputs and outputs are open or shorted. Most faults cause the FAULT pin 103 to go high and the $\overline{\text{FAULT}}$ pin 102 to go low to signal the fault. Both FAULT and $\overline{\text{FAULT}}$ are low during power-up or reset until the LX4580 has passed self-tests.

Fault management and reporting is controlled by the Fault registers (section 0 on page 56). The read-back status of the FAULT and $\overline{\text{FAULT}}$ outputs is also available in the STATUS_REG0 register (section 13.3.1 on page 46).

By default, all faults initiate Safe Mode. The four fault mask registers FAULT_MASK0 to FAULT_MASK3 all the system configure specific faults to not cause the LX4580 to initiate Safe Mode. Operating modes, including Safe Mode, are discussed in section 12 on page 42.

The FAULT_STATUS0 register (section 13.5.1 on page 57) reports if the FAULT outputs or $\overline{\text{FAULT}}$ output appears to be shorted. A short fault is detected when the output is driven to one logic level by the LX4580, but reads back as the opposite logic level. The GLITCH_REG0 register (section 13.4.1 on page 50) sets the delay before a short fault on either the FAULT output or the $\overline{\text{FAULT}}$ output is reported in the FAULT_STATUS0 register. The GLITCH_REG1 register (section 13.4.2 on page 50) and the GLITCH_REG2 register (section 13.4.3 on page 51) provide the current short fault debounce counts for the FAULT and $\overline{\text{FAULT}}$ outputs respectively.

11.9 JTAG Interface

A JTAG interface is available at pins 104 to 107 for optional scan testing and debug.

11.10 GPIO Pins

Overloaded GPIO outputs cause a fault alert in the FAULT_STATUS0 register (section 13.5.1 on page 57). A short fault is detected when the output is driven to one logic level by the LX4580, but reads back as the opposite logic level. GPIO pins are programmed through the GPIO registers (section 13.11 on page 83) to be either:

- Logic inputs with programmable 50k Ω pulldown resistors
- Logic outputs with programmable output enables
- Logic outputs for the HEP1, HEP2, and HEP3 analog comparator inputs (section 11.17 on page 31)
- Over-temperature fault status for the internal linear regulators (section 11.2 on page 21), buck switch (section 11.3 on page 23), 4-20mA current loop driver (section 11.16 on page 30), and LVDT driver (section 11.21.1 on page 37)
- Internal PLL lock status

11.11 UART_EN Input

The UART_EN pin 120 selects between either two client SPI serial interfaces operating up to 30MHz, or two client UART serial interfaces operating up to 1MHz. It is not possible to select the combination of one SPI serial interface and one UART serial interface. The status of the UART_EN pin is available in the STATUS_REG0 register (section 13.3.1 on page 46). The UART_EN input has a 50k Ω internal pulldown that defaults the interface selection to SPI mode if the pin is open.

11.12 SPI and UART Interfaces

Each serial interface has simultaneous and asynchronous dual-port read/write access to the register set. If both interfaces execute a simultaneous write to the same register, then the write by interface 1 will execute first, to be then overwritten by the write by interface 2.

A single command from a serial interface host comprises four 16-bit SPI packets. For the UART interface, each 16-bit packet is split into two 8-bit chunks (plus start, parity, and stop bits). Each 16-bit packet comprises 11 payload bits and 5 parity bits as a Hamming 16-11 Error Correction Code (ECC) implementation. This Hamming code is Single-Error Correcting and Double-Error Detecting (SECDED) due to the inclusion of the 5th parity bit.

The fundamental 4-packet structure (for a single-register write) is shown in Table 3 below. For each 16-bit packet, the appropriate SPI select $\overline{SS1}$ or $\overline{SS2}$ goes low before packet transmission, and returns high between packets and after the final packet. The first bit of every packet is 0, indicating that the packet is from the host. The next two bits are the Packet ID bits, which identify which of the four types of packet it is. The next 8 bits are the packet's payload, which include Command, 12-bit register address, and 16-bit register data. The final 5 bits are parity.

Table 3. A 4-Packet Serial Interface Transmission from a Bus Host to Client LX4580 on MOSI1 or MOSI2

Packet	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
	0	Packet ID										Parity				
First Command {C0:C3} Address {A0:A3}	0	0	0	C0	C1	C2	C3	A0	A1	A2	A3	P0	P1	P2	P3	P4
2nd Address {A4:A11}	0	1	0	A4	A5	A6	A7	A8	A9	A10	A11	P0	P1	P2	P3	P4
3rd Data {D0:D7}	0	0	1	D0	D1	D2	D3	D4	D5	D6	D7	P0	P1	P2	P3	P4
Last Data {D8:D15}	0	1	1	D8	D9	D10	D11	D12	D13	D14	D15	P0	P1	P2	P3	P4

If the 4 Command bits {C0:C3} = 1st packet bits {D3:D6} are for a register read, then the 3rd and 4th packet transmissions will include data sent by the LX4580 as shown in Table 4 below. This first bit is the Data Ready bit, and is 1 to indicate a valid transmission. The Data Ready bit will be 0 for null packets, which happen when the Command only asks for a high or low data byte, but not both. Each packet contains 10 data bits as opposed to just a byte, which allows the results of the 10-bit SARs, for example, to be read in one packet. Note that the least significant word is packed as D8, D9, {D0-D7} while the most significant word is packed as {D6:D15}.

Table 4. A 2-Packet Serial Interface Transmission from a Client LX4580 to a Bus Host on MISO1 or MISO2

Packet	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
	Data Ready											Parity				
3rd Data D8-D9,{D0:D7}	1	D8	D9	D0	D1	D2	D3	D4	D5	D6	D7	P0	P1	P2	P3	P4
Last Data {D6:D15}	1	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	P0	P1	P2	P3	P4

The 5 parity bits {P0:P4} = packet bits {D11:D15} are calculated from the preceding 11 packet bits {D0:D10} as follows, where the $\oplus$ symbol is the XOR operator:

$$P0 = D0 \oplus D1 \oplus D3 \oplus D4 \oplus D6 \oplus D8 \oplus D10$$

$$P1 = D0 \oplus D2 \oplus D3 \oplus D5 \oplus D6 \oplus D9 \oplus D10$$

$$P2 = D1 \oplus D2 \oplus D3 \oplus D7 \oplus D8 \oplus D9 \oplus D10$$

$$P3 = D4 \oplus D5 \oplus D6 \oplus D7 \oplus D8 \oplus D9 \oplus D10$$

$$P4 = D0 \oplus D1 \oplus D2 \oplus D3 \oplus D4 \oplus D5 \oplus D6 \oplus D7 \oplus D8 \oplus D9 \oplus D10 \oplus P0 \oplus P1 \oplus P2 \oplus P3$$

Transmission related faults are latched into the FAULT_STATUS1 register (section 13.5.4 on page 59). Faults are incorrect packet order as determined by the packet ID, internal state machine integrity failure, and double bit error detection. In all fault cases the packet is rejected. Additionally, an alert is given should single bit error correction occur. Although the packet will have been executed successfully, the alert provides warning of possible interference or other issues on the interface. Any combination of faults can be routed to the FAULT and FAULT output pins (section 11.8 on page 25).

The Command nibble is the key to optimizing efficient use of the serial interface, reducing register addressing overhead and unnecessary data transfers to a minimum (Table 7 on page 28). The 4 bits select the combinations of:

- C0: $\overline{\text{Rd}}/\text{Wr}$ Set for the host to write register(s), clear to read register(s)
- C1: AutoInc Set for the read or write transaction to affect sequential registers in one sequence
- C2: LoData Set for the read or write transaction to affect the lower 8 bits of a register
- C3: HiData Set for the read or write transaction to affect the upper 8 bits of a register

The register access options are:

- Read or write just the lower byte of a register in a 3-packet transaction
- Read or write just the upper byte of a register in a 3-packet transaction
- Read or write both the lower byte and the upper byte of a register (in that order) in a 4-packet transaction
- Read or write just the lower byte of sequential registers in a 3-packet transaction for the first register, plus a single packet for subsequent registers (address incrementing)
- Read or write just the upper byte of sequential registers in a 3-packet transaction for the first register, plus a single packet for subsequent registers (address incrementing)
- Read or write both the lower byte and the upper byte of a register (in that order) in a 4-packet transaction for the first register, plus two packets for subsequent registers (address incrementing)

These communication sequences are detailed in Table 7 on page 28.

Between active commands, extra 00 command packets before a 10 address packet are ignored. The final 00 command packet received is used to define the new active command associated with the 10 address packet just received. Table 5 below shows the allowed packet sequences sent by a bus host to an LX4580. Table 6 shows unallowed packet sequences that will set the Fault_Command_Ch# bit in the FAULT_STATUS1 register (section 13.5.4 on page 59).

Table 5. Allowed Host Transmitted Packet Sequences on MOSI

Packet Label	Packet Label	Packet Label	Packet Label	Packet Label	Packet Label	Packet Label	Communication Sequence
00	00	00	00	00	00	10	Extra 00 command packets before the 10 address packet are ignored. The final 00 command packet received is used
00	10	00	00	00	00	00	Read operation: Host sends 00 command packet and 10 address packet, then sends repeated 00 command packets while reading the requested register(s) on MISO
00	10	01	00	00	00	00	Write a single register lower byte operation
00	10	11	00	00	00	00	Write a single register upper byte operation
00	10	01	11	00	00	00	Write a single complete register word operation

Table 6. Unallowed Host Transmitted Packet Sequences on MOSI

Packet Label	Packet Label	Packet Label	Packet Label	Communication Sequence
00	01			00 command packets must not be followed by an 01 or a 11 data packet
00	11			
00	10	10		Read operation: 10 address packet must be followed by a 00 command packet
00	10	01		
00	10	11		
00	10	00		Write operation to the lower byte only of a register word: 10 address packet must be followed by an 01 lower byte packet
00	10	10		
00	10	11		
00	10	00		Write operation to the upper byte only of a register word: 10 address packet must be followed by an 11 upper byte packet
00	10	10		
00	10	01		
00	10	01	00	Write operation to a complete register word: 10 address packet must be followed by an 01 lower byte packet and then by an 11 upper byte packet in that order
00	10	01	10	
00	10	01	01	
00	10	00		
00	10	10		
00	10	11		

Table 7. Communication Sequences as Defined by the Command Bits {C0:C3}

C0 Rd/Wr	C1 AutoInc	C2 LoData	C3 HiData	Packet Label Sequence	Command	Action at Address {A11:A0} Selected by Packet 1 and Packet 2
0	x	0	0	00 10 00	Null (dummy read)	Value 0x0000 returned by LX4580 (Data Ready = 0)
0	0	1	0	00 10 00	Read low byte only	Low byte returned by LX4580 during 3rd packet
0	0	0	1	00 10 00	Read high byte only	High byte returned by LX4580 during 3rd packet
0	0	1	1	00 10 00 00	Read {low, high} bytes	Low byte returned by LX4580 during 3rd packet High byte returned by LX4580 during 4th packet
0	1	0	1	00 10 00 .. 00	Auto-incremented read of high bytes only	High byte for address {A11:A0} returned by LX4580 during 3rd packet High byte for address 1 + {A11:A0} returned by LX4580 during 4th packet Auto-incrementing reads continue until an 01 packet is received.
0	1	1	0	00 10 00 .. 00	Auto-incremented read of low bytes only	Low byte for address {A11:A0} returned by LX4580 during 3rd packet Low byte for address 1 + {A11:A0} returned by LX4580 during 4th packet Auto-incrementing reads continue until an 01 packet is received.
0	1	1	1	00 10 00 00 .. 00 00	Auto-incremented read of {low, high} bytes	Low byte for address {A11:A0} returned by LX4580 during 3rd packet High byte for address {A11:A0} returned by LX4580 during 4th packet Low byte for address 1 + {A11:A0} returned by LX4580 during 5th packet High byte for address 1 + {A11:A0} returned by LX4580 during 6th packet Auto-incrementing reads continue until an 01 packet is received.
1	x	0	0	00 10 00	Null (dummy write)	Writes to neither byte
1	0	1	0	00 10 01 00	Write low byte only	Low byte written to LX4580 after receiving 3rd packet
1	0	0	1	00 10 11 00	Write high byte only	High byte written to LX4580 after receiving 3rd packet
1	0	1	1	00 10 01 11 00	Write {low, high} bytes	High byte written to LX4580 after receiving 3rd packet Low byte written to LX4580 after receiving 4th packet
1	1	1	0	00 10 01 01 .. 01 00	Auto-incremented write of low bytes only	Low byte for address {A11:A0} written to LX4580 after receiving 3rd packet Low byte for address 1 + {A11:A0} written to LX4580 after receiving 4th packet Auto-incrementing writes continue until an 00 packet is received.
1	1	0	1	00 10 11 11 .. 11 00	Auto-incremented write of high bytes only	High byte for address {A11:A0} written to LX4580 after receiving 3rd packet High byte for address 1 + {A11:A0} written to LX4580 after receiving 4th packet Auto-incrementing writes continue until an 00 packet is received.
1	1	1	1	00 10 01 11 01 11 .. 01 11 00	Auto-incremented write of {low, high} bytes	Low byte for address {A11:A0} written to LX4580 after receiving 3rd packet High byte for address {A11:A0} written to LX4580 after receiving 4th packet Low byte for address 1 + {A11:A0} written to LX4580 after receiving 5th packet High byte for address 1 + {A11:A0} written to LX4580 after receiving 6th packet Auto-incrementing writes continue until an 00 packet is received.

11.12.1 SPI SLAVE SELECT LOGIC POLARITY

The active low SPI selects $\overline{SS1}$ and $\overline{SS2}$ can be switched to active high using the SPI_Polarity bit in the CONTROL_REG2 register (section 13.6.3 on page 67).

11.13 Pulse Width Modulated (PWM) Outputs

The LX4580 provides 8 PWM outputs that are register programmable for frequency, duty cycle and initial phase. These PWM outputs control the 4 half bridge circuits for driving typically a three-phase motor and controlling a park, anti-extension solenoid. 2-phase bipolar stepper motors are suitable also.

The motor control PWMs, LVDT primary drive PWM sinewave synthesis, and ADC sampling are programmable in a harmonic ratio such that an integer number of motor control switching cycles corresponds to any of the other timings, and also an integer number of ADC samples are taken during any of the two LVDT driver independent sinewaves.

The CLKGEN registers (section 13.7 on page 68) set the timing for the LVDT and current sense Σ - Δ ADCs, and for the PWM period as a direct function of these timings.

In a typical application, the top-level clock is 22.5MHz, the two LVDT sinewave frequencies are 1.4kHz and 2.0kHz, motor control PWM frequency is 11kHz, and the LVDT sense sigma delta modulator clocks are 1.4MHz and 1.9MHz.

11.14 10-Bit SAR Analog-to-Digital Converters

The LX4580 include dual 10-bit SAR ADCs which are operated by a state machine synchronized to the motor control PWM. The SAR registers (section 13.9 on page 71) set up acquisition timing and select which analog input signals are acquired and their order, including repetition.

The 1.245V nominal reference voltage, VREF, is internally scaled by 1300/1245 to provide a 1.3V upper reference voltage VREF_H, and a lower reference voltage VREF_L at 1.1V below it, so VREF_L is nominally 0.2V. Most ADC inputs use this 0.2V to 1.3V input range too allow 200mV headroom for input amplifier stages operating from the 1.5VA supply. Bipolar analog inputs use an internal 0.75V bias point as the midpoint. The HV1 and HV2 analog inputs are unamplified and offer the full 0V to 1.3V input range. The correct ADC reference range is selected automatically with the analog input.

The analog signals that can be multiplexed into either SAR ADC are:

- Outputs from the five Pt100/Pt1000 temperature sensor interfaces (section 11.18 on page 41)
 - Any of the five interfaces can be used instead to provide a single-ended ADC input and a differential ADC input, both inputs having the same selectable 213.9mV or 1.039V full scales
- The 3 pressure sensor (or other 4-20mA) interface differential amplifier outputs and source driver headroom voltage (section 11.16 on page 30)
 - Any of the three interfaces can be used instead to provide a single-ended ADC input with 1.1V full scale
- Two general purpose single-ended ADC inputs, HV1 and HV2, with 1.3V full scale (section 11.19 on page 34)
- Two LVDT/resolver primary drive waveform monitoring interfaces (section 11.21.3 on page 39)
 - Either of the two interfaces can be used instead to provide a differential bipolar ADC input with ± 1.1 V full scale
- Die temperature
 - ADC output value varies from typically 603 at -60°C to 340 at +115°C, a slope of nominally -1.5 LSB/°C
- VCC voltage, which has an operating range of 10V to 30V
- Redundant nominally 1.2V bandgap reference voltage, VBG_redundant

11.15 Σ - Δ Analog-to-Digital Converters

The LX4580 include nine sigma delta (Σ - Δ) ADCs operating simultaneously with independent 2nd order Σ - Δ modulators and sinc³ filters. The Σ - Δ modulators can be clocked at or below 2MHz. The resolution of the ADC is a function of the oversampling ratio and can vary from 8 bits to 16 bits. The Filter registers (section 13.10 on page 76) configure the Σ - Δ processing parameters. Outputs are stored in 16 bit registers and are updated at the decimation rate.

- Five ADCs are assigned to current sense interfaces (section 11.20 on page 35)
- Four ADCs are assigned to LVDT secondary interfaces (section 11.21.4 on page 40)

11.16 4-20mA Current Loop (Pressure Sensor) Interfaces

The LX4580 includes three independent 4-20mA current loop interfaces for typically pressure sensors for acquisition by the 10-bit SAR ADCs. Each interface comprises a differential analog input between the PRS_P# and PRS_N# pins and a current limited VCC power switch at the PRS_SRC# pin for sensor excitation (Figure 8 below). Each power switch has a maximum voltage drop of 0.45V at 20mA, and current limits to typically 30mA for safety.

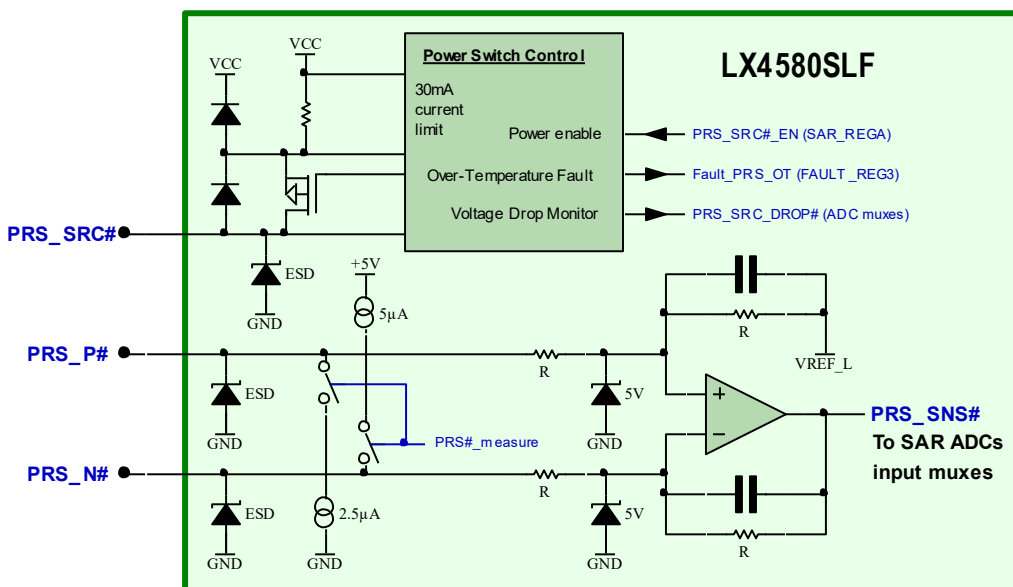


Figure 8. 4-20mA Current Loop Analog Front End (One of Three)

SAR_REGA (section 13.9.10 on page 73) provides independent enables for the three current loop power switches, PRS_SRC1 (pin 1), PRS_SRC2 (pin 4), and PRS_SRC3 (pin 7). Disabling a power switch also disables the associated front-end amplifier and a subsequent 10-bit SAR ADC conversion would return an undefined value.

The GLITCH_REGC register reports the number of counts of the F_{OSC} debounce clock that have accumulated since an over-temperature fault detected in one or more of the three 4-20mA power sources, PRS_SRC#. If the count reaches a value of $31 / F_{OSC}$ ($1.21\mu s$ for $F_{OSC} = 25.6MHz$), then a fault is latched in the Fault_PRS_SRC_OT bit in the FAULT_STATUS3 register (section 13.5.10 on page 63).

The STATUS_REG2 register (section 13.3.3 on page 47) identifies the over-temperature 4-20mA power source(s).

Figure 9 below shows the shows the wiring diagram for a 4-20mA loop sensor and also how to use an interface as a single-ended general purpose ADC input. In both cases, the full scale input voltage is 1.1V, with 1 LSB corresponding to 1.074mV. Using a 50Ω current sense resistor, the measurement range is 200mV to 1V for a 4-20mA loop current range.



Figure 9. 4-20mA Sensor Connection or General Purpose ADC Connection

Fault detection operates as follows:

- Excessive power switch dissipation will trigger an over-temperature fault indicated in STATUS_REG2 (section 13.3.3 on page 48)
 - There is a settling time of $31 \times 1024 / F_{OSC}$ ($1.24ms$ for $F_{OSC} = 25.6MHz$) between fault detection and the fault being latched in the Fault_PRS_SRC_OT bit in the FAULT_STATUS3 register (section 13.5.10 on page 63)
 - The FAULT_CLEAR3 register (section 13.5.11 on page 64) clears faults flagged in FAULT_STATUS3.
 - The fault is maskable as to whether it initiates Safe Mode (section 12.4 on page 42)

- The GLITCH_REGC register (section 0 on page 54) reports the number of counts of the $F_{osc} / 1024$ debounce clock that have accumulated since fault detection
- The PRS_SRC1_OT status in STATUS_REG2 can be output to GPIO6 if desired (section 13.11.13 on page 86)
- The PRS_SRC2_OT status in STATUS_REG2 can be output to GPIO1 if desired (section 13.11.8 on page 85)
- The PRS_SRC3_OT status in STATUS_REG2 can be output to GPIO5 if desired (section 13.11.12 on page 86)
- The voltage drop across each power switch can be monitored by the SAR2 10-bit ADC to check that the driver isn't running out of voltage headroom. The voltage drop monitor circuit has a gain of 2.03, so with the 1.3V SAR ADC input range a power switch voltage drop of greater than typically 640mV will show as full scale 1023 (0x3FF). The monitor is calibrated for a SAR value of $719 \pm 2.5\%$ with a power switch voltage drop of 0.45V, so a SAR value in the range 738 to 1023 guarantees power switch correct operation
- Faulty connections to PRS_P# and PRS_N# are detected by a weak pullup current (5 μ A) on PRS_N# and a weak pulldown current (2.5 μ A) on PRS_P# that are both enabled at the start of every ADC conversion. The 2.5 μ A injected into PRS_P# raises the current sense voltage by 75 μ V, corresponding to about 1/14th LSB
 - If either the loop itself or the connection to PRS_P# is broken, the weak pulldown on PRS_P# will cause an ADC value below the 200mV minimum for a working sensor
 - If the connection to PRS_N# is broken, the weak pullup on PRS_N# will again cause an ADC value below the 200mV minimum for a working sensor

11.17 Hall Effect Comparator Inputs

There are three general purpose comparator inputs, HEP1, HEP2, and HEP3 intended for Hall Effect sensors but also suitable for digitizing other slow moving analog inputs (Figure 10 below). The inputs have large hysteresis of typically 2.2V, and guarantee to produce a logic 0 for inputs below 1V, and a logic 1 for inputs above 4V. Outputs are available in STATUS_REG2 (section 13.3.3 on page 47).

Each comparator output can be also be routed to GPIO outputs (section 11.10 on page 25, section 13.11 on page 83):

- The PRS_SRC1_OT status in STATUS_REG2 can be output to GPIO6 if desired (section 13.11.13 on page 86)
- The PRS_SRC2_OT status in STATUS_REG2 can be output to GPIO1 if desired (section 13.11.8 on page 85)
- The PRS_SRC3_OT status in STATUS_REG2 can be output to GPIO5 if desired (section 13.11.12 on page 86)

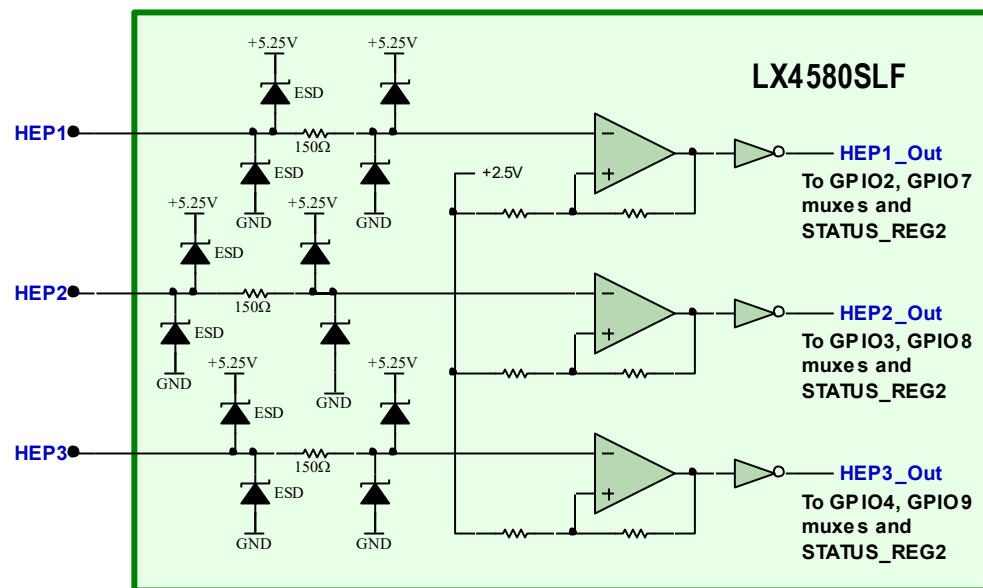


Figure 10. Hall Effect Comparator Inputs

11.18 Temperature Sensor Interfaces

The LX4580 includes five independent temperature sensor interfaces for acquisition by the 10-bit SAR ADCs. An interface can be used instead to provide two general purpose ADC inputs.

Each interface comprises a differential analog input between the TMP_P# and TMP_N# pins, a single-ended analog input between the TMP_REF# and GND pins, and a current source at the TMP_SRC# pin for sensor excitation (Figure 11 below). The current source is only gated on prior to and during an ADC acquisition to minimize sensor self-heating and power consumption.

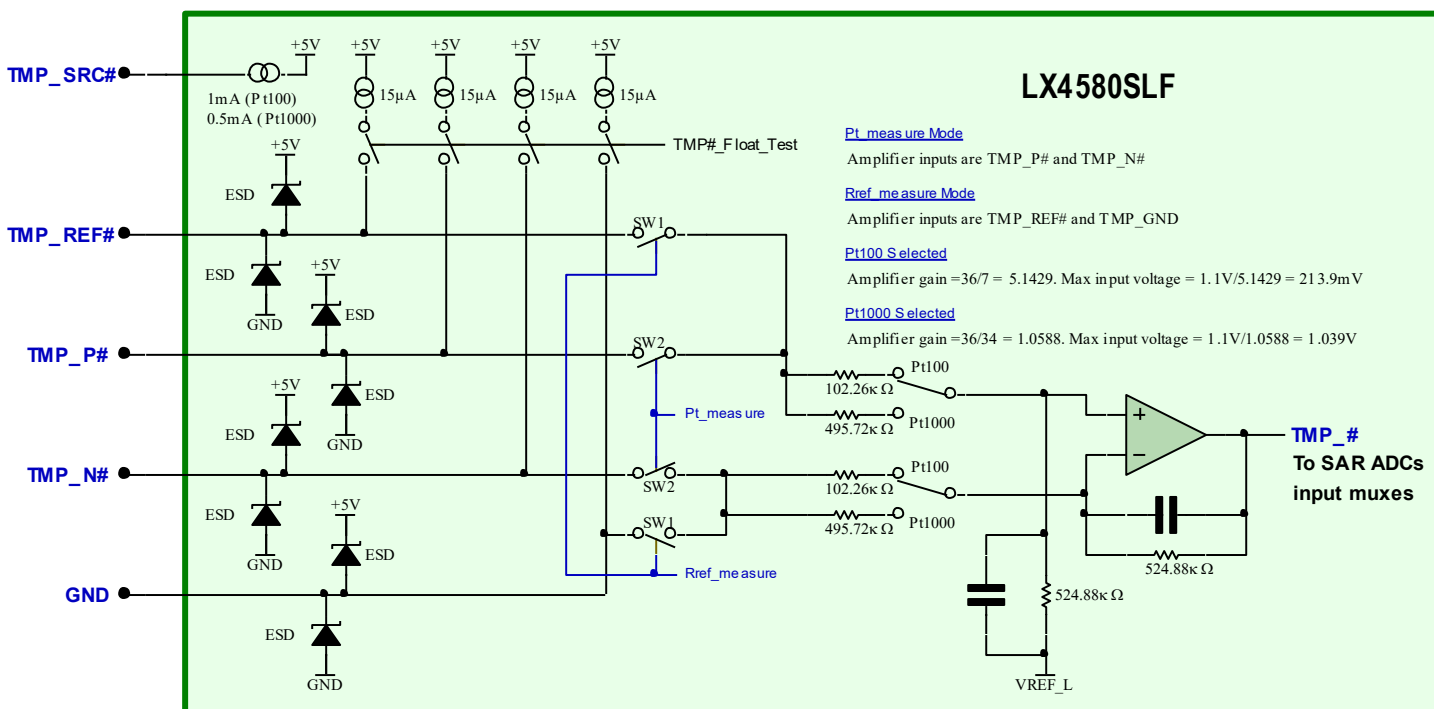


Figure 11. Pt100 and Pt1000 Temperature Sensor Analog Front End (One of Five)

The five bits TMP#_Pt_Type in CONTROL_REG0 (section 13.6.1 on page 66) configure the five temperature sensing analog front ends individually to suit either Pt100 or Pt1000 type temperature sensors. Any combination of Pt100 and Pt1000 sensors can be programmed. Selecting Pt100 sets the drive current to 1mA and the ADC full scale input voltage to 213.9mV. Selecting Pt1000 sets the temperature sensor drive current at TMP_SRC# to 0.5mA and the ADC full scale input voltage to 1.039V. The sensor drive currents are controlled by individual DACs, which can be adjusted through the Trim registers (section 13.12 on page 88).

When an ADC channel is due to read a TMP input, the TMP_SRC# is enabled and the two SW1 switches route the TMP_P# and TMP_N# signals to the amplifier as a differential input. When an ADC channel is due to read a REF input, the TMP_SRC# is enabled and the two SW2 switches route the TMP_REF# and GND signals to the amplifier effectively as a single-ended input.

The five pins associated with each interface allow either 2, 3, or 4 wire temperature sensor connections to suit remote and local sensor locations. In all cases:

- The TMP_SRC# pin connects to the TMP_P# pin and one side of the temperature sensor
- The TMP_REF# pin connects to the TMP_N# pin and the other side of the temperature sensor
- An external precision reference resistor, R_{REF} is fitted between the TMP_REF# pin and a close by GND pin. The stability of R_{REF} with temperature and aging directly affects measurement accuracy

Figure 12 on page 33 shows the wiring diagrams for 2, 3, and 4 wire sensors.

A 4-wire connection uses a pair of wires for the temperature sensor excitation current, and a separate pair of wires for the sensor voltage measurement. The parasitic resistance of two excitation wires does not affect accuracy. The differential input resistance between TMP_P# and TMP_N# is typically 204kΩ or 991kΩ in Pt100 or Pt1000 modes respectively, so sensor voltage measurement wiring resistance has negligible effect on accuracy.

A 3-wire connection uses a dedicated wire for the temperature sensor excitation current, and a separate pair of wires for the sensor voltage measurement. This architecture is as accurate as a 4-wire network if the parasitic resistance of the excitation wire is identical to the parasitic resistance of the ground wire.

A 2-wire connection is accurate if the wiring resistances are negligible. This architecture is suitable to local temperature sensors, and also remote temperature sensors where highest accuracy isn't required.

In all cases, the standard ratiometric measurement technique is used which relies on a precision reference resistance, R_{REF} . Since the same current passes through both the temperature sensor and the reference resistance, the sensor resistance can be calculated by the equation $I_{TMP_SRC\#} = \frac{V_{Pt}}{R_{Pt}} = \frac{V_{REF}}{R_{REF}}$ or $R_{Pt} = \frac{V_{Pt} \times R_{REF}}{V_{REF}}$. The system host programs ADC conversions of a REF input followed by the TMP input, and performs the calculation. Since the temperature coefficient of a Pt sensor is non-linear, curvature correction by polynomial or lookup table typically follows.

The maximum resistance that can be measured for a Pt100 sensor is typically $R_{Pt100(max)} = \frac{213.9mV}{1mA} = 214\Omega$.

The maximum resistance that can be measured for a Pt1000 sensor is typically $R_{Pt1000(max)} = \frac{1.039V}{0.5mA} = 2.08k\Omega$.

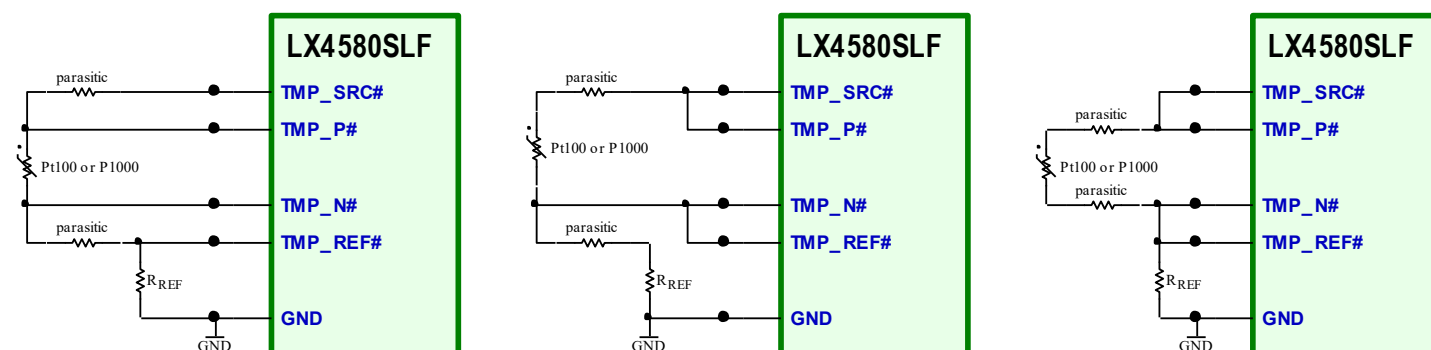


Figure 12. 4-Wire, 3-Wire, and 2-Wire Temperature Sensor Connections

Figure 13 below shows how to use a temperature sensor interface to provide two general purpose ADC inputs, one differential and one single-ended, with the same full scale input voltage. The TMP_SRC# current source output will still be enabled during conversions, so leave it open to save power. Use the TMP#_Pt_Type bit in the CONTROL_REG0 register to select the desired input voltage range.

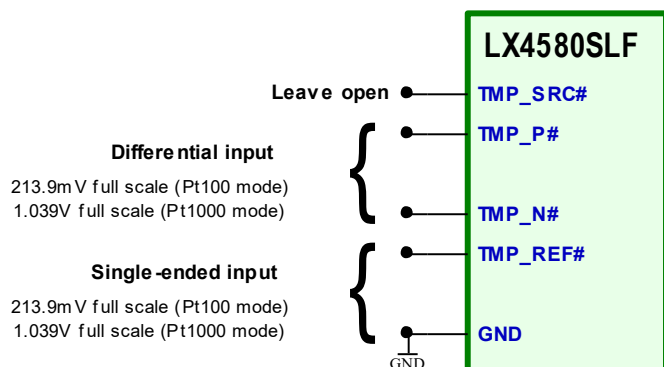


Figure 13. Using a Temperature Sensor Interface for General Purpose ADC Inputs

Fault detection operates as follows:

- When a sensor interface is idle between ADC conversions, weak ($15\mu A$) current sources are switched to each of the input pins to check for open connections, detected by internal comparators
- There is a settling time of $31 / F_{OSC}$ ($1.21\mu s$ for $F_{OSC} = 25.6MHz$) between fault detection and the fault being latched in the Fault_TMP_float bit in the FAULT_STATUS3 register (section 13.5.10 on page 63)
- The FAULT_CLEAR3 register (section 13.5.11 on page 64) clears faults flagged in FAULT_STATUS3

- The fault is maskable as to whether it initiates Safe Mode (section 12.4 on page 42)
- The GLITCH_REGD register (section 13.4.8 on page 52) reports the number of counts of the F_{OSC} debounce clock that have accumulated since fault detection
- The five TMP_#_Fault bits in the STATUS_REG4 register (section 13.3.5 on page 48) identify the faulty channel(s)
- Other faults in either a Pt sensor or a reference resistor are detected by out of bounds ADC acquisition results

11.19 HV1 and HV2 General Purpose ADC Inputs

The LX4580 includes two single ended inputs, HV1 and HV2 with 0V to 1.3V input range, multiplexed to the two 10-bit SAR ADCs (section 13.9 on page 71).

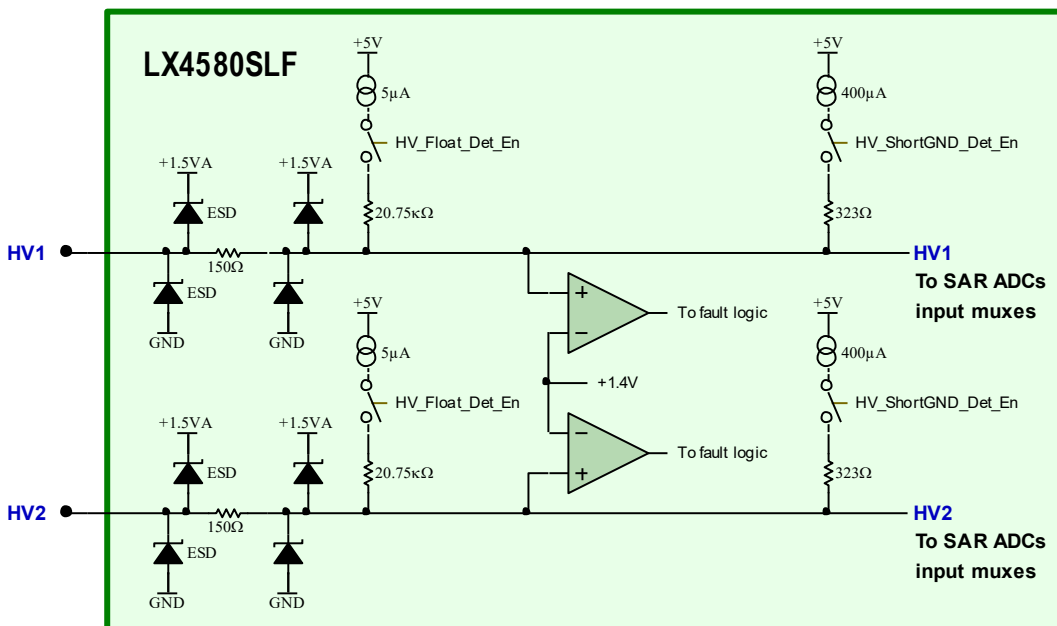


Figure 14. HV1 and HV2 General Purpose ADC Inputs Analog Front End

Each input includes fault testing for inputs either floating, shorted to GND, or over-voltage. Each of the 3 fault conditions is tested individually when required by setting the appropriate bit in the CONTROL_REG1 register (section 13.6.2 on page 67). Tests must be selected one at a time, and operate on both HV1 and HV2 at the same time.

Fault detection operates as follows:

- Setting the HV_Float_Det_En bit in CONTROL_REG1 enables 5μA current sources on both the HV1 and HV2 inputs to test for floating inputs
 - An input is detected as floating if it can be pulled higher than 1.4V by 5μA, corresponding to a source resistance greater than 280kΩ
- Setting the HV_ShortGND_Det_En bit in CONTROL_REG1 enables 400μA current sources on both the HV1 and HV2 inputs to test for inputs shorted to GND
 - An input is detected as shorted to GND if it cannot be pulled higher than 1.4V by 400μA, corresponding to a source resistance lower than 3.5kΩ
- Setting the HV_OV_Det_En bit in CONTROL_REG1 detects inputs that are higher than 1.4V
- There is a settling time of $31 \times 1024 / F_{OSC}$ (1.24ms for $F_{OSC} = 25.6\text{MHz}$) between fault detection and the fault being latched in the Fault_HV bit in the FAULT_STATUS3 register (section 13.5.10 on page 63)
- The FAULT_CLEAR3 register (section 13.5.11 on page 64) clears faults flagged in FAULT_STATUS3
- The fault is maskable as to whether it initiates Safe Mode (section 12.4 on page 42)
- The GLITCH_REG8 register (section 13.4.8 on page 52) reports the number of counts of the $F_{OSC} / 1024$ debounce clock that have accumulated since fault detection
- The HV1_Fault and HV2_Fault bits in the STATUS_REG4 register (section 13.3.5 on page 48) further indicate whether a fault was detected in the HV1 input, the HV2 input, or both

11.20 ISENSE Current Sensing Interfaces

There are five current sensing differential inputs which have dedicated Σ - Δ ADCs. The differential input architecture simplifies interfacing to current transformers or isolated current sense amplifiers that have a common reference voltage (ISENSE_RTN) for all channels. The differential full scale input voltage range is $\pm 1.1\text{V}$ with reference to ISENSE_RTN which has an working range of 1.2V to 2.8V. Each ISENSE# input is enabled individually by an ISENSE#_EN bit in the CLKGEN_REG0 register (section 13.7.1 on page 68).

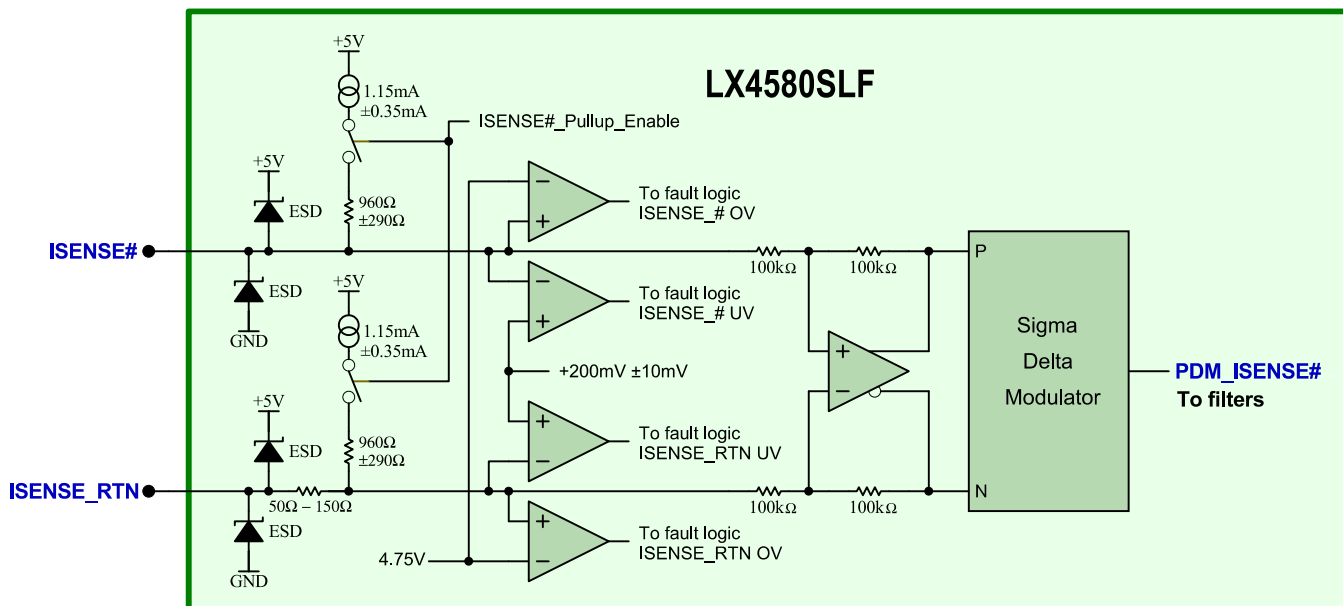


Figure 15. Current Sensing Analog Front End (One of Five)

The LX4580 includes fault detection for open or shorted to GND current sensing inputs. The fault detection technique presumes that the external sensor's output resistance is within a certain range. The required resistance can be obtained by adding a series resistor to the sensor output. When fault detection is enabled, the LX4580 forces a nominal 1.15mA current out of both the target ISENSE# pin and the ISENSE_RTN pin, and uses window comparators to check that both pin voltages are within an expected range. The voltage will be too low if the sensor line is shorted to GND, or too high if the sensor wiring is open.

Fault testing is normally initiated when no current is flowing through the current sensor. In this case, the ISENSE# and ISENSE_RTN inputs will be at the DC voltage that ISENSE_RTN is biased to, in the range 1.2V to 2.8V. The minimum sensor resistance is that which under worst-case conditions won't be detected as a short. A short can be detected if the minimum pullup current (0.8mA) can't pull the input higher than 210mV, so the minimum sensor resistance is therefore 262.5Ω.

The maximum sensor output resistance is that which won't be detected as an open. An open is detected if there is less than 0.25V across the current source. The maximum current that the input has to sink at this threshold is $0.25\text{V} / (960\Omega - 290\Omega) = 373\mu\text{A}$. With no current flowing through the sensor, ISENSE# will be at the same voltage as the bias applied to ISENSE_RTN, V_{RTN} . The maximum sensor output resistance is therefore $(4.75\text{V} - V_{\text{RTN}}) / 373\mu\text{A}$. This resolves to 9.5kΩ with $V_{\text{RTN}} = 1.2\text{V}$ (lower limit) and 5.2kΩ with $V_{\text{RTN}} = 2.8\text{V}$ (upper limit).

In summary, a sensor source resistance between 262.5Ω and 5.2kΩ covers all design variants. A value such as 500Ω to 1kΩ would be a good choice for ISENSE# inputs, and also ISENSE_RTN if this voltage is buffered by an opamp. If ISENSE_RTN is provided by a 2-resistor divider from a supply rail, ensure that the effective source resistance of the divider (the two resistances in parallel) is low enough to avoid being detected as an open. Lower ISENSE_RTN bias voltages allow a higher source resistance.

Figure 16 below shows an example 3-phase ground-referred current sense implementation using amplifiers from the AEC-Q100 qualified [MCP6V91 op amp family](#) operating from the LX4580's 5.25V supply for auxiliary circuits.

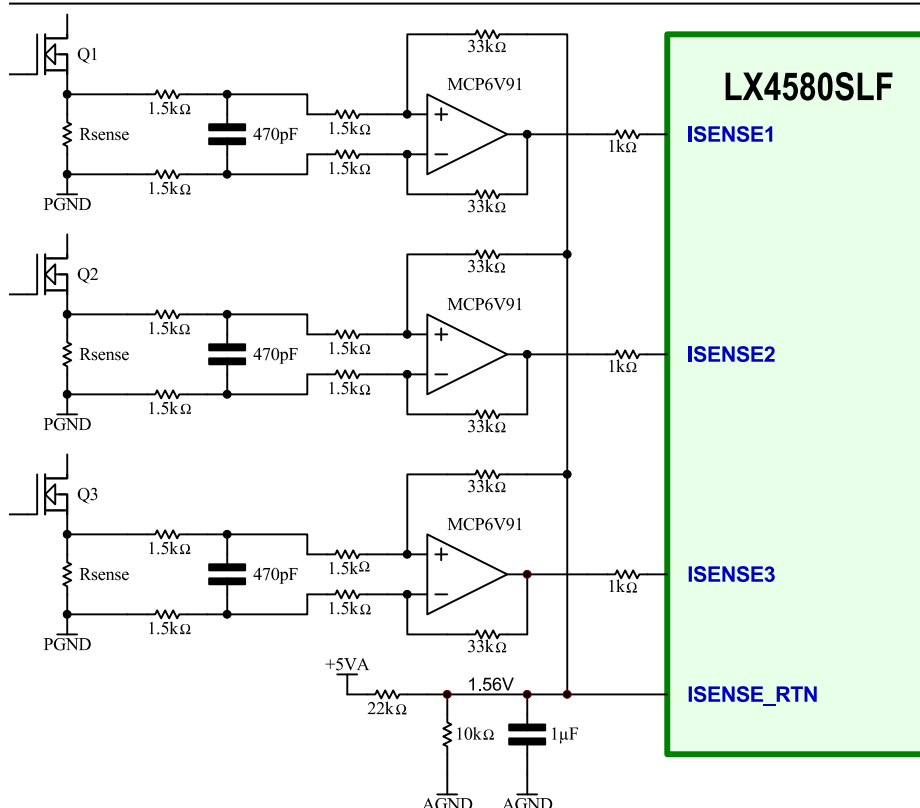


Figure 16. Ground-Referred Current Sensing Example Circuit

The example in Figure 16 is designed for a $\pm 100\text{mV}$ drop across the current sense resistors, and so requires an amplifier gain of 11 to meet the LX4580's $\pm 1.1\text{V}$ ISENSE input range. The input resistors to the x11 gain stages are split to allow capacitors to be added to make a low pass filter (LPF) for common mode noise filtering. The LPF's corner frequency,

$$f_{3\text{dB}} = \frac{1}{2 \times \pi \times (2 \times 1.5\text{k}\Omega \times 470\text{pF})} = 113\text{kHz},$$

is a tradeoff between filter effectiveness and latency in current measurement. ISENSE_RTN and the differential amplifiers are biased to 1.56V using a 2-resistor divider from the +5VA analog supply. This sets the amplifier outputs at a nominal $1.56\text{V} \pm 1.1\text{V}$ full scale for positive and negative currents. The divider's 22k Ω and 10k Ω resistors offer a 6.9k Ω source resistance, which is under the 8.5k Ω upper limit for this bias voltage to avoid falsely detecting an open circuit on ISENSE_RTN.

Fault detection for the current sensing differential inputs is managed by registers as follows:

- Setting the appropriate ISENSE#_Pullup_Enable bit in CONTROL_REG0 register (section 13.6.1 on page 66) enables individual 1mA current sources on the selected ISENSE input(s) and also the ISENSE_RTN input
 - Any combination of ISENSE# inputs can be enabled for testing at the same time
- There is a settling time of $31 / F_{\text{OSC}}$ ($1.21\mu\text{s}$ for $F_{\text{OSC}} = 25.6\text{MHz}$) between fault detection and the fault being latched in the Fault_ISENSE_Range bit in the FAULT_STATUS3 register (section 13.5.10 on page 63)
- The FAULT_CLEAR3 register (section 13.5.11 on page 64) clears faults flagged in FAULT_STATUS3
- The fault is maskable in the FAULT_MASK3 register (section 13.5.12 on page 64) as to whether it initiates Safe Mode (section 12.4 on page 42)
- The GLITCH_REGE register (section 13.4.14 on page 54) reports the number of counts of the F_{OSC} debounce clock that have accumulated since fault detection
- The ISENSE#_Range_Fault bits in the STATUS_REG3 register (section 13.3.4 on page 48) identifies the faulty ISENSE interface(s)

11.21 LVDT/RVDT/Resolver Interface

There are two independent (apart from primary driver supply voltage) LVDT interfaces, which can also be used with RVDT or resolver instruments. Each LVDT interface comprises 3 sections:

- A full bridge primary driver with 160mA sink/source capability operating from the 10V to 30V VFB supply. The driver is operated by a state machine reading from an internal host-configured PWM lookup table for autonomous operation
- A differential amplifier for the primary drive waveform (after external filtering) to be monitored via a 10-bit SAR ADC
- A differential input plus dedicated Σ - Δ ADC for each of the two secondaries

Figure 17 below shows the networks used by the LX4580 evaluation board for primary drive filtering, drive sense voltage attenuation and filtering, plus secondary bias, attenuation, and filtering. The component values suit the Solartron Metrology ± 15 mm stroke 930982 [S series LVDT](#) and the [AMCI R11X-A10/7](#) resolver.

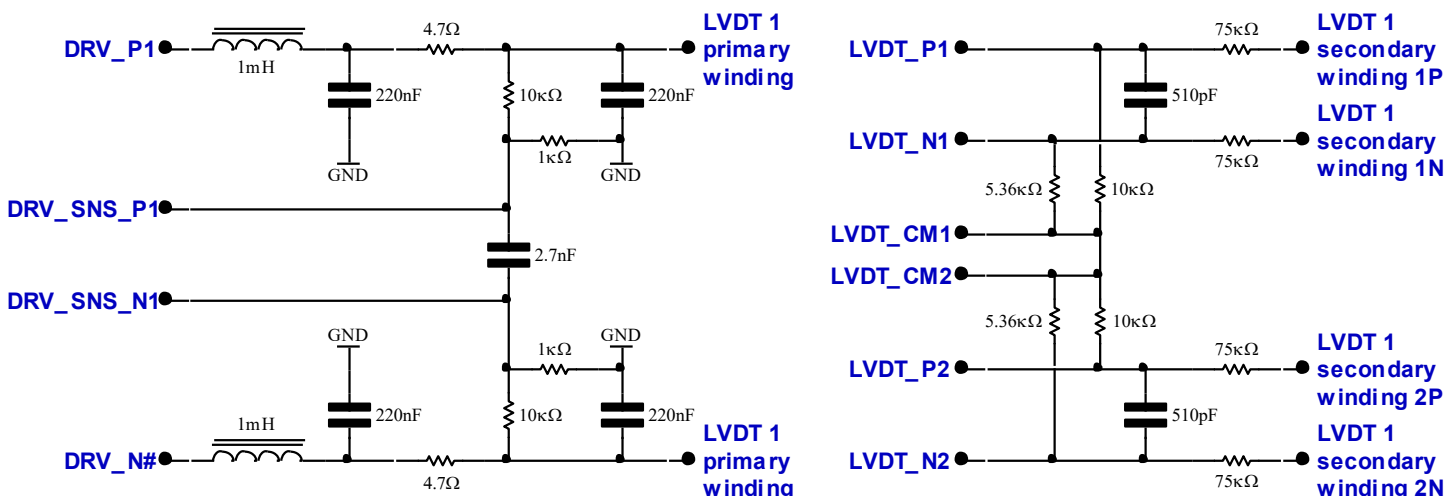


Figure 17. Example LVDT Primary Drive, Primary Waveform Monitoring, and Secondary Filter Networks

11.21.1 LVDT PRIMARY FULL BRIDGE DRIVERS (DRV_P# AND DRV_N# PINS)

The 10V to 30V VFB supply is used only for the two LVDT primary drivers, so it can be optimised independently of the main analog supply, VCC (section 11.1 on page 19).

The primary drive architecture uses direct digital synthesis (DDS) of a complete primary drive waveform period, based around a 128 element, 10 bit PWM look-up table, LVDT#_Duty0 to LVDT#_Duty7F. The LVDT1_Drive registers (section 13.8 on page 70) manage the DRV_P1 and DRV_N1 PWM drive waveform for LVDT1's primary. The matching LVDT2_Drive registers configure the DRV_P2 and DRV_N3 PWM drive waveform for LVDT2's primary.

Each DDS table holds the amplitude samples for a complete (typically sine) waveform period for its LVDT, and allows for the waveform to be tuned to compensate for the response of the external LC filter between the DRV_P# and DRV_N# half-bridge outputs and the LVDT primary. The DDS state machine uses the PLL clock ($F_{PLL} = 4 \times F_{OSC}$) to achieve high PWM granularity, so it is recommended that the PLL should be enabled using the CLKGEN_REG0 register (section 13.7.1 on page 68) early in the LX4580's post power-up initialization routine. If the PLL is disabled, then DDS PWM resolution will reduce by 2 bits.

The number of samples making up a complete primary drive waveform period is set to between 8 and 128 (128 being the capacity limit of the look-up table) by the LVDT#_Frame register. The LVDT#_F_Count register identifies which frame is currently being used to set PWM duty during operation. Its value will vary from 0 to {LVDT#_Frame - 1}.

For an LVDT waveform frequency of F_{LVDT} , the primary drive waveform period equation is:

$$LVDT_Period \times LVDT_Frame = \frac{F_{OSC}}{F_{LVDT}}$$

The LVDT#_Offset register sets the number of F_{OSC} clocks where the DRV_P# and DRV_N# outputs are both low for commutation at PWM duty transitions. The selection range varies from 50ns to 800ns (50ns resolution) with $F_{OSC} = 20$ MHz to 75ns to 1200ns with $F_{OSC} = 30$ MHz (75ns resolution).

Soft-start and soft-stop are configured by two registers that set the slope of duty ramp-up, and ramp-down when the state of the DRV_#_EN bit in CLKGEN_REG1 (section 13.7.2 on page 68) is changed from 0 to 1, and 1 to 0 respectively.

The duty ramp rate register LVDT#_Ramp sets the rate = $2 * 2^{LVDT\#_Ramp}$ at which the duty limit rises or falls.

The duty limit register LVDT#_Limit reads 0 when DRV_#_EN = 0, and increments every frame by $2^{LVDT\#_Ramp}$ after DRV_#_EN has gone high (ramp-up), and decrements every frame by $2^{LVDT\#_Ramp}$ after DRV_#_EN has gone low (ramp-down).

An LVDT is enabled, after configuring these registers, by setting the DRV_#_EN bit in CLKGEN_REG1 (section 13.7.2 on page 68).

LVDT driver fault detection operates as follows:

- Excessive power switch dissipation in a half-bridge output (DRV_P1, DRV_N1, DRV_P2, or DRV_N2) will trigger an over-temperature fault indicated in the appropriate one of the four DRV_##_OT bits in the STATUS_REG2 register (section 13.3.3 on page 48)
 - The DRV_P1_OT status in STATUS_REG2 can be output to GPIO8 if desired (section 13.11.15 on page 87)
 - The DRV_N1_OT status in STATUS_REG2 can be output to GPIO6 if desired (section 13.11.13 on page 86)
 - The DRV_P2_OT status in STATUS_REG2 can be output to GPIO4 if desired (section 13.11.11 on page 86)
 - The DRV_N2_OT status in STATUS_REG2 can be output to GPIO2 if desired (section 13.11.9 on page 85)
 - The Fault_DRV1_OT bit is latched in the FAULT_STATUS3 register (section 13.5.10 on page 63) if either or both of the DRV_P1 and DRV_N1 half-bridge outputs has an over-temperature fault
 - The Fault_DRV2_OT bit is latched in the FAULT_STATUS3 register if either or both of the DRV_P2 and DRV_N2 half-bridge outputs has an over-temperature fault
 - The fault is maskable as to whether it initiates Safe Mode (section 12.4 on page 42)
 - The FAULT_CLEAR3 register (section 13.5.11 on page 64) clears faults flagged in FAULT_STATUS3
- Excessive current in either the DRV_P1 or the DRV_N1 half-bridge output will trigger an over-current fault indicated in the appropriate one of the two DRV_#1_OC bits in the STATUS_REG2 register (section 13.3.3 on page 48)
 - There is a settling time of $31 \times 1024 / F_{OSC}$ (1.24ms for $F_{OSC} = 25.6\text{MHz}$) between fault detection and the fault being latched in the Fault_DRV1_OC bit in the FAULT_STATUS3 register (section 13.5.10 on page 63)
 - The GLITCH_REG6 register (section 13.4.6 on page 52) reports the number of counts of the $F_{OSC} / 1024$ debounce clock that have accumulated since fault detection
 - The fault is maskable as to whether it initiates Safe Mode (section 12.4 on page 42)
 - The FAULT_CLEAR3 register (section 13.5.11 on page 64) clears faults flagged in FAULT_STATUS3
- Excessive current in either the DRV_P2 or the DRV_N2 half-bridge output will trigger an over-current fault indicated in the appropriate one of the two DRV_#2_OC bits in the STATUS_REG2 register (section 13.3.3 on page 48)
 - There is a settling time of $31 \times 1024 / F_{OSC}$ (1.24ms for $F_{OSC} = 25.6\text{MHz}$) between fault detection and the fault being latched in the Fault_DRV2_OC bit in the FAULT_STATUS3 register (section 13.5.10 on page 63)
 - The GLITCH_REG7 register (section 13.4.7 on page 52) reports the number of counts of the $F_{OSC} / 1024$ debounce clock that have accumulated since fault detection
 - The fault is maskable as to whether it initiates Safe Mode (section 12.4 on page 42)
 - The FAULT_CLEAR3 register (section 13.5.11 on page 64) clears faults flagged in FAULT_STATUS3

11.21.2 PRIMARY WAVEFORM SYNTHESIS DESIGN EXAMPLE

Having a 22.5MHz crystal, a 3kHz primary sinewave drive is desired. This leads to the following parameters:

- $22.5 \times 10^6 / 3000 = 7500 F_{OSC}$ clocks (= 30k F_{PLL} clocks) per sine period
- This could be arranged as LVDT1_Period = 150 x F_{OSC} clocks per PWM period, and LVDT1_Frame = 50
- The PWM resolution is $4 \times LVDT1_Period = 600 F_{PLL}$ clocks, out of the 1024 clock maximum, since the look-up table provides 10 bits depth per PWM sample
- 50 look-up table samples describe the full LVDT waveform period, stored from LVDT1_Duty0 to LVDT1_Duty31
- Zero crossings are at the 1st and the 26th sample
- The minimum (or negative peak) of the waveform will have a duty cycle value of 0%, so 0
- The maximum (or positive peak) of the waveform will have a duty cycle value of 100%, so 600
- There are 601 PWM values, so the ideal zero crossing value is 300½, which must be approximated to 300 or 301

11.21.3 LVDT PRIMARY DRIVE VOLTAGE SENSING (DRV_SNS_P# AND DRV_SNS_N# PINS)

Each LVDT section includes a differential amplifier to both monitor the primary drive waveform for automatic acquisition by one of the LX4580's two 10-bit SAR ADCs (section 13.9 on page 71), and also facilitate open/short fault testing of the LVDT primary circuit (Figure 18 below).

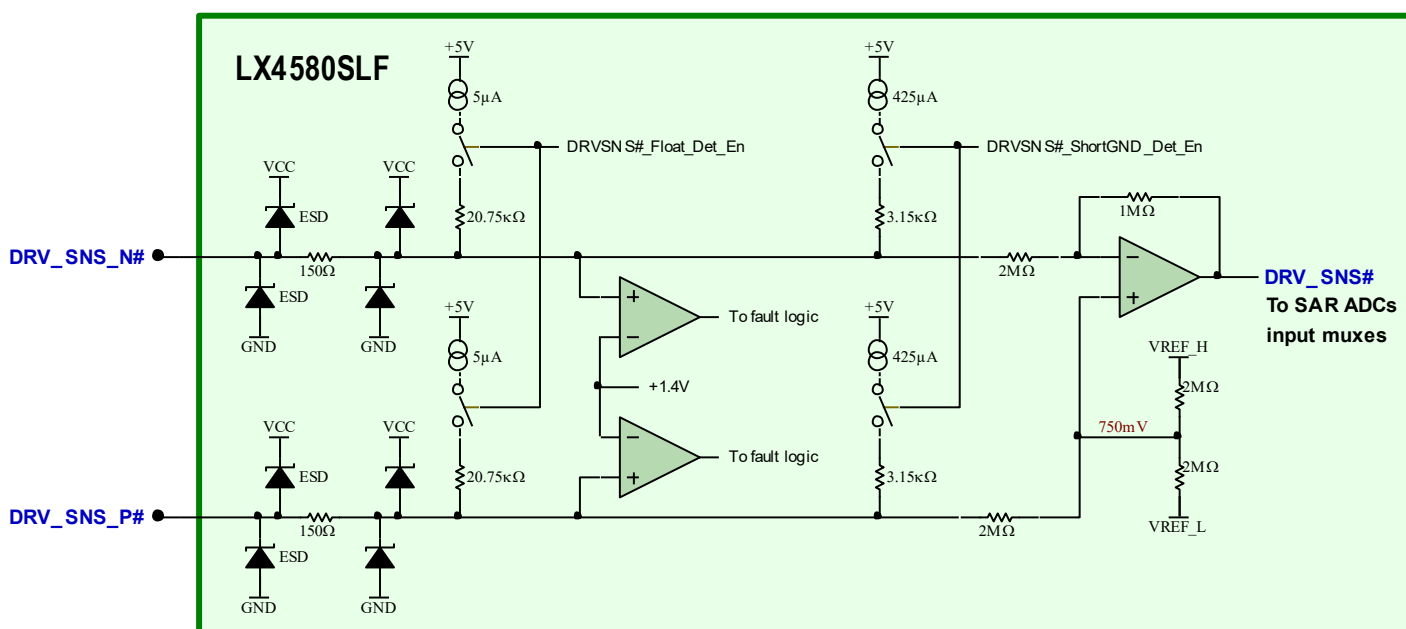


Figure 18. LVDT Primary Drive Waveform Sensing Analog Front End (One of Two)

LVDT primary waveform monitoring is not obligatory for satisfactory LVDT operation, but offers the following benefits:

- The DDS PWM values can be scaled to maintain a specific waveform amplitude at the LVDT primary after the LC filter, compensating for component tolerances and value shifts with temperature
- The DDS PWM values can be tuned to pre-distort the waveform to compensate for LC filter characteristics
- Calibration of the primary waveform allows an LVDT to be used with only one secondary operational, by characterizing the amplitude:position relationship for each secondary
- The DRV_SNS circuit includes current source for fault testing primary winding continuity

The differential amplifier level shifts a $\pm 1.1V$ maximum input signal to the 200mV to 1.3V SAR ADC input range, by attenuating the differential input signal by a factor of 2, and adding a 750mV offset following the equation:

$$DRV_SNS\# = \frac{DRV_SNS_P\# - DRV_SNS_N\#}{2} + \frac{V_{REF_H} + V_{REF_L}}{2} \approx \frac{DRV_SNS_P\# - DRV_SNS_N\#}{2} + 750mV$$

Each input includes fault testing for inputs either floating, shorted to GND, or over-voltage. Each of the 3 fault conditions is tested individually when required by setting the appropriate bit in the CONTROL_REG1 register (section 13.6.2 on page 67). Tests must be selected one at a time for each LVDT driver, but the testing for the two LVDT drivers is independent and can be initiated at the same time or separately as desired.

Fault detection operates as follows:

- Setting the DRV_SNS1_Float_Det_En bit in CONTROL_REG1 enables 5μA current sources on both the DRV_SNS_P1 and DRV_SNS_N1 inputs for the 1st LVDT driver to test for floating DRV_SNS_#1 inputs. Similarly, setting the DRV_SNS2_Float_Det_En bit in CONTROL_REG2 enables 5μA current sources on both the DRV_SNS_P2 and DRV_SNS_N2 inputs for the 2nd LVDT driver to test for floating DRV_SNS_#2 inputs
 - An input is detected as floating if it can be pulled higher than 1.4V by 5μA, corresponding to a source resistance greater than 280kΩ
- Setting the DRV_SNS1_ShortGND_Det_En bit in CONTROL_REG1 enables 400μA current sources on both the DRV_SNS_P1 and DRV_SNS_N1 inputs for the 1st LVDT to test for inputs shorted to GND. Similarly, setting the DRV_SNS2_ShortGND_Det_En bit in CONTROL_REG1 enables 400μA current sources on both the DRV_SNS_P2 and DRV_SNS_N2 inputs for the 2nd LVDT driver to test for inputs shorted to GND

- An input is detected as shorted to GND if it cannot be pulled higher than 1.4V by 400μA, corresponding to a source resistance lower than 3.5kΩ
- Setting the DRV_SNS1_OV_Det_En bit in CONTROL_REG1 detects DRV_SNS_P1 and DRV_SNS_N1 inputs for the 1st LVDT that are higher than 1.4V. Similarly, setting the DRV_SNS2_OV_Det_En bit in CONTROL_REG1 detects DRV_SNS_P2 and DRV_SNS_N2 inputs for the 2nd LVDT driver that are higher than 1.4V.

There is a settling time of $31 \times 1024 / F_{OSC}$ (1.24ms for $F_{OSC} = 25.6\text{MHz}$) between fault detection and the fault being latched in either the Fault_DRV_SNS_#1 bit or the Fault_DRV_SNS_#2 bit in the FAULT_STATUS3 register (section 13.5.10 on page 63). FAULT_CLEAR3 register (section 13.5.11 on page 64) clears faults flagged in FAULT_STATUS3. The faults are independently maskable as to whether they initiate Safe Mode (section 12.4 on page 42).

The GLITCH_REG9 register (section 0 on page 53) reports the number of counts of the $F_{OSC} / 1024$ debounce clock that have accumulated since fault detection on DRV_SNS1. The DRV_SNS_P1_Fault bit and DRV_SNS_N1_Fault bit in the STATUS_REG4 register (section 13.3.5 on page 48) further indicate whether a fault was detected in the DRV_SNS_P1_Fault input, the DRV_SNS_N1_Fault input, or both.

The GLITCH_REGA register (section 13.4.10 on page 53) reports the number of counts of the $F_{OSC} / 1024$ debounce clock that have accumulated since fault detection on DRV_SNS2. The DRV_SNS_P1_Fault bit and DRV_SNS_N1_Fault bit in the STATUS_REG4 register (section 13.3.5 on page 48) further indicate whether a fault was detected in the DRV_SNS_P2_Fault input, the DRV_SNS_N2_Fault input, or both.

11.21.4 LVDT SECONDARY SIGNAL ACQUISITION (LVDT_P#, LVDT_N#, AND LVDT_CM#, PINS)

These differential input pairs are designed to interface to an otherwise floating transformer secondary that is referenced to VREF. The LVDT speed and angle algorithm is executed by the user application. Alternatively, the user can read the on-chip logic that calculates the RMS value per channel over one period useful for position calculation at the external application level. This is provided at a rate of one or two samples per exciter input period.

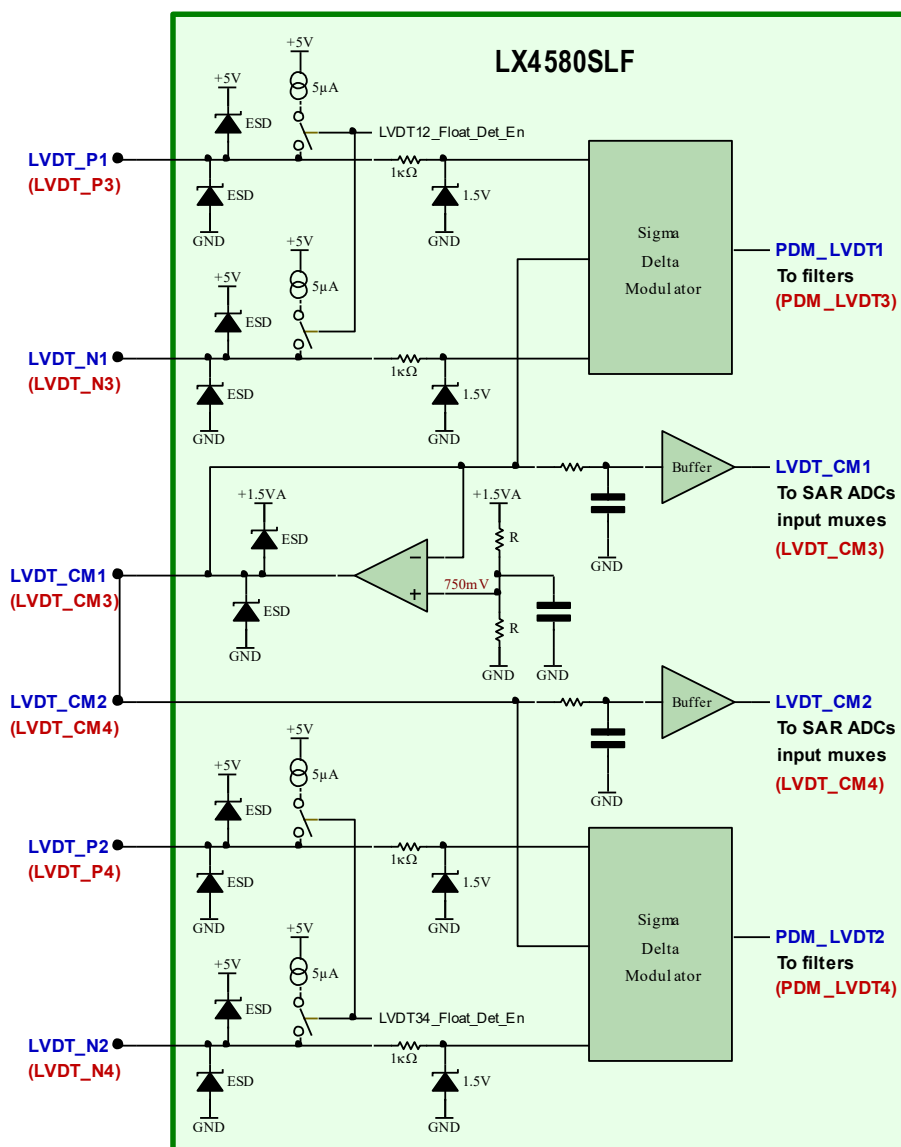


Figure 19. One of Two LVDT Secondaries Analog Front End (2nd block's names in parentheses)

12 Operating modes

12.1 Startup Mode

Startup Mode sets the LX4580 in a known initial state based on the OTP configuration memory contents and then verifies its functional integrity. Before all internal power supplies reach compliance levels, all registers are held in reset, the FAULT and FAULT outputs are asserted low, while all I/Os and other outputs are high impedance. After all power supplies reach compliance levels, the LX4580 waits for the crystal oscillator (if present) to stabilize and then enters self-test. If all the tests pass, the FAULT output is asserted low and FAULT is asserted high and LX4580 enters Functional Mode.

12.2 Manual Reset

The host processor can reset the LX4580 to power-up condition (Startup Mode) by pulsing the RESET input pin high then returning low. While the RESET input is high, all registers are held in reset and all I/Os and outputs are high impedance.

12.3 Functional Mode

In Functional Mode, the host processor can run extended tests on the LX4580 if desired prior to operation, change configuration data loaded from OTP memory (registers can be tested for stuck-at faults, digital filters can be tested with a known pattern, analog input sense pins can be tested for short or open condition, internal references, bias currents, ADCs can be checked for consistency and calibration can be verified, internal voltage regulators can be checked for consistency using the ADCs) and also to provide synchronized filtered ADC data, to allow the host processor to control the 8 PWM drivers and two LVDT driver channels and to signal internally detected fault conditions as they occur. Additionally, during functional mode, the external processing can override configuration data.

During this mode both SPI/UART client interfaces operate concurrently to read or write LX4580 registers allowing the external processing to do the following operations:

- Set divider for PWM1-PWM8 timing resolution
- Set sigma-delta modulator groups divider to clock input
- Set divider determining PWM1-PWM8 cycle period
- Set individual delay for each PWM1-PWM8 with respect to the reference PWM period
- Set individual duty cycle for PWM1-PWM8
- Set divider determining the two LVDT driver switching cycles
- Set pattern length for each of the two LVDT drivers
- Set pattern data for each of the two LVDT drivers
- Set individual sinc³ oversampling ratio for each delta-sigma modulator
- Set RMS calculation window and post RMS oversampling ratio for the two groups of two LVDT sense channels
- Set Critical fault mask register
- Set various digital fault limits for under / over currents and voltages measured
- Enable self-calibration configurations
- Set GPIO configuration including support for host processor interrupts for PWM and LVDT synchronization
- Re-initialize (reset) timing origin for PWM reference cycle and for LVDT drivers pattern address pointer.
- Read SAR ADC output data for any input (or group of inputs) acquisition channel(s)
- Read delta sigma modulators output after decimation
- Read RMS data for the four LVDT input channels
- Read FAULT register status (that is driven by analog or digital comparators and internal checkers including ECC)

If a fault is identified (ADC value, supply voltage, pin voltage range is out of set bounds, uncorrected error occurs in communications or in the internal logic) the corresponding bit is set high in a FAULT register (section 0 on page 56). If any fault bit is set, then the FAULT output is set high and the FAULT output is set low. Also, if a FAULT_MASK register (section 13.5.3 on page 58) has the corresponding bit low, then the LX4580 transitions into Safe Mode.

12.4 Safe Mode

The purpose of the Safe Mode is to set the outputs of LX4580 into a state that makes the system safe under fault conditions. In this mode, all functional inputs and outputs are either high impedance or in another safe condition. However, the SPI or UART serial interfaces still operate in order to allow the host processor to diagnose the fault. All fault register file updates are frozen. Exit from this mode is via manual reset or power cycling. Safe mode can also be asserted by writing 0xC3 to the SAFE_FORCE register (section 13.5.14 on page 65). Read the SAFE_STATUS register (section 13.5.15 on page 65) to check safe mode status.

13 Registers

13.1 Register Map

Address	Register	Section
0x004	POR_REG1	13.2
0x201	WATCHDOG_REG1	13.15
0x202	WATCHDOG_REG2	
0x203	WATCHDOG_REG3	
0x204	WATCHDOG_REG4	
0x206	WATCHDOG_REG6	
0x207	WATCHDOG_REG7	
0x208	WATCHDOG_REG8	
0x210	CLKGEN_REG0	13.7
0x211	CLKGEN_REG1	
0x212	CLKGEN_REG2	
0x213	CLKGEN_REG3	
0x214	CLKGEN_REG4	
0x220	GLITCH_REG0	13.4
0x221	GLITCH_REG1	
0x222	GLITCH_REG2	
0x223	GLITCH_REG3	
0x224	GLITCH_REG4	
0x225	GLITCH_REG5	
0x226	GLITCH_REG6	
0x227	GLITCH_REG7	
0x228	GLITCH_REG8	
0x229	GLITCH_REG9	
0x22A	GLITCH_REGA	
0x22B	GLITCH_REGB	
0x22C	GLITCH_REGC	
0x22D	GLITCH_REGD	
0x22E	GLITCH_REGE	
0x22F	GLITCH_REGF	
0x230	GLITCH_REG10	
0x100	FAULT_STATUS0	0
0x101	FAULT_STATUS1	
0x102	FAULT_STATUS2	
0x103	FAULT_STATUS3	
0x104	FAULT_CLEAR0	
0x105	FAULT_CLEAR1	
0x106	FAULT_CLEAR2	
0x107	FAULT_CLEAR3	
0x108	FAULT_MASK0	
0x109	FAULT_MASK1	
0x10A	FAULT_MASK2	
0x10B	FAULT_MASK3	
0x10C	CRITICAL_STATUS	
0x10D	CRITICAL_CLEAR	
0x10E	SAFE_FORCE	
0x10F	SAFE_STATUS	

Address	Register	Section
0X300	FILTER_CH12_CFG	13.10
0X301	FILTER_CH12_CFG2	
0X302	FILTER_CH12_COR	
0X308	FILTER_CH34_CFG	
0X309	FILTER_CH34_CFG2	
0X30A	FILTER_CH34_COR	
0X310	FILTER_CH1_SINC	
0X311	FILTER_CH2_SINC	
0X312	FILTER_CH3_SINC	
0X313	FILTER_CH4_SINC	
0X314	FILTER_CH1_IIR	
0X315	FILTER_CH2_IIR	
0X316	FILTER_CH3_IIR	
0X317	FILTER_CH4_IIR	
0X318	FILTER_CH1_RMS	
0X319	FILTER_CH2_RMS	
0X31A	FILTER_CH3_RMS	
0X31B	FILTER_CH4_RMS	
0X31C	FILTER_CH1_OUT	
0X31D	FILTER_CH2_OUT	
0X31E	FILTER_CH3_OUT	
0X31F	FILTER_CH4_OUT	
0X321	FILTER_IS1_CFG	
0X322	FILTER_IS2_CFG	
0X323	FILTER_IS3_CFG	
0X324	FILTER_IS4_CFG	
0X325	FILTER_IS5_CFG	
0X331	FILTER_IS1_SINC	0
0X332	FILTER_IS2_SINC	
0X333	FILTER_IS3_SINC	
0X334	FILTER_IS4_SINC	
0X335	FILTER_IS5_SINC	
0X336	FILTER_IS1_IIR	
0X337	FILTER_IS2_IIR	0
0X338	FILTER_IS3_IIR	
0X339	FILTER_IS4_IIR	
0X33A	FILTER_IS5_IIR	
0x400	CONTROL_REG0	
0x401	CONTROL_REG1	
0x402	CONTROL_REG2	
0x403	CONTROL_REG3	
0x404	CONTROL_REG4	
0x500	STATUS_REG0	0
0x501	STATUS_REG1	
0x502	STATUS_REG2	
0x503	STATUS_REG3	
0x504	STATUS_REG4	
0x505	STATUS_REG5	
0x506	STATUS_REG6	

Address	Register	Section
0x600	TRIM_REG0	0
0x601	TRIM_REG1	
0x602	TRIM_REG2	
0x603	TRIM_REG3	
0x604	TRIM_REG4	
0x605	TRIM_REG5	
0x606	TRIM_REG6	
0x607	TRIM_REG7	
0x608	TRIM_REG8	13.13
0x700	OTP_REG0	
0x701	OTP_REG1	
0x702	OTP_REG2	
0x703	OTP_REG3	
0x704	OTP_REG4	
0x705	OTP_REG5	
0x706	OTP_REG6	
0x707	OTP_REG7	
0x801	SAR_REG1	13.9
0x802	SAR_REG2	
0x803	SAR_REG3	
0x804	SAR_REG4	
0x805	SAR_REG5	
0x806	SAR_REG6	
0x807	SAR_REG7	
0x808	SAR_REG8	
0x809	SAR_REG9	
0x80A	SAR_REGA	
0x80B	SAR_REGB	
0x80C	SAR_REGC	
0x80D	SAR_REGD	
0x80E	SAR_REGE	
0x80F	SAR_REGF	
0x810	SAR_REG10	
0x811	SAR_REG11	
0x812	SAR_REG12	
0x813	SAR_REG13	

Address	Register	Section
0x814	SAR_REG14	13.9
0x815	SAR_REG15	
0x816	SAR_REG16	
0x817	SAR_REG17	
0x818	SAR_REG18	
0x819	SAR_REG19	
0x81A	SAR_REG1A	
0x81B	SAR_REG1B	
0x81C	SAR_REG1C	
0x81D	SAR_REG1D	
0x81E	SAR_REG1E	
0x81F	SAR_REG1F	
0x820	SAR_REG20	
0x830	SAR_REG30	
0x838	SAR_REG38	
0x840	SAR_REG40	
0x850	SAR_REG50	13.11
0x858	SAR_REG58	
0x860	SAR_REG60	
0x870	SAR_REG70	
0x880	SAR_REG80	
0x8A0	SAR_REGA0	
0xA00	GPIO_REG0	
0xA01	GPIO_REG1	13.8
0xA02	GPIO_REG2	
0xA03	GPIO_REG3	
0xA04	GPIO_REG4	
0xA05	GPIO_REG5	
0xA06	GPIO_REG6	
0xBxx	LVDT1_Drive	13.8
0xCxx	LVDT2_Drive	
0xD00	UART_U1_WARN	13.16
0xD01	UART_U1_WARN_RST	
0xD02	UART_U2_WARN	
0xD03	UART_U2_WARN_RST	

13.2 POR Status Register

The over- and under-voltage status of the +1.5VD supply rail is available in POR_REG1.

Address	Name	R/W	Register Contents															
			D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0x004	POR_REG1	R	-	-	-	-	-	-	-	-	-	-	1.5VD over/under-voltage status					

13.2.1 POR_REG1 REGISTER 0x004 (+1.5VD SUPPLY UNDER- AND OVER-VOLTAGE DETECTION)

The LX4580 implements triple comparators for both under- and over-voltage detection on the critical digital core supply voltage +1.5VD (pins 80 and 121). Voltage detection follows triple modular redundant voting, being the state of at least two comparators. If an over- or under-voltage fault is detected for longer than longer than $255 / F_{OSC}$ ($10\mu s$ for $F_{OSC} = 25.6MHz$), then the POR_Fault bit is latched high in the FAULT_STAUS0 register (section 13.5.1 on page 57).

See the supply rail fault management section 11.2 on page 21 for details on how over- and under-voltage status of the other rails is managed.

Bit	Name	Description
0	+1.5VD_UV1	Triple comparators for +1.5VD under-voltage detection. High if +1.5VD is below the $UV_{+1.5VD_LDO_OUT}$ threshold (1.35V typ)
1	+1.5VD_UV2	
2	+1.5VD_UV3	
3	+1.5VD_OV1	Triple comparators for +1.5VD over-voltage detection. High if +1.5VD is above the $OV_{+1.5VD_LDO_OUT}$ threshold (2.47V typ)
4	+1.5VD_OV2	
5	+1.5VD_OV3	
6 - 15	-	Unimplemented bits which read back as 0

13.3 Status Registers

Status registers show real-time conditions. Detected faults are latched and stored in separate Fault registers as shown. Status bits that can be optionally routed to a GPIO pin are indicated in the GPIO columns. See section 11.10 on page 25 and section 13.11 on page 83 for details on GPIO.

Address	Name	R/W	Register Contents															
			D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0x500	STATUS_REG0	R	FAULT outputs, UNLOCK input, UART_EN input, PLL lock, supply over/under-voltage status															
0x501	STATUS_REG1	R	-	-	-	RESET input, supply over-/under-voltage statuses												
0x502	STATUS_REG2	R	-	-	Hall inputs, 4-20mA and LVDT over-temperature, LVDT over-current													
0x503	STATUS_REG3	R	-	-	LVDT and current sense input faults													
0x504	STATUS_REG4	R	-	LVDT voltage sense input, HV, temperature inputs, and regulator over-temperature faults														
0x505	STATUS_REG5	R	Reserve status bits used for supply over-/under-voltage statuses															
0x506	STATUS_REG6	R/W	Enable/disable for reserve status bits in STATUS_REG5 latching a fault															

13.3.1 STATUS_REG0 REGISTER 0x500

Bits	Name	Description	Fault Register	GPIO
0	FAULT_IN	Logic level read back from the FAULT output pin 103. If this logic level is not what the FAULT output is expected to be, then after a delay set by the GLITCH_REG0 register (section 13.4.1 on page 50) a short fault is detected on this pin	FAULT_STATUS0 See section 13.3.1 on page 46	
1	$\overline{\text{FAULT_IN}}$	Logic level read back from the FAULT output pin 102. If this logic level is not what the FAULT output is expected to be, then after a delay set by the GLITCH_REG0 register (section 13.4.1 on page 50) a short fault is detected on this pin		
2	UNLOCK	Logic level at the UNLOCK input pin 119. Since the unlocked state enables actions that are normally blocked, taking UNLOCK high latches a fault which can be used or ignored	FAULT_STATUS2 See section 13.5.7 on page 61	
3	UART_EN	Logic level at the UART_EN input pin 120	Not fault status	
4	PLL_LOCK	High if the PLL is in lock. The PLL going out of lock is latched as the PLL_Unlocked bit in the FAULT_STATUS3 (section 13.5.10 on page 63)	FAULT_STATUS3 See section 13.5.10 on page 63	GPIO2
5	VCC_UV	High if the VCC supply pin 144 is below the $UV_{VCC/VFB}$ threshold (9.6V typ). This status is also latched in the Spike_VCC_UV bit in the FAULT_STATUS3 register. The GLITCH_REGB register (section 13.4.11 on page 53) reports the number of counts of the $F_{OSC} / 1024$ debounce clock that have accumulated since an under-voltage was detected. If the count reaches a value of $31 \times 1024 / F_{OSC}$ (1.24ms for $F_{OSC} = 25.6\text{MHz}$), then a further fault is latched in the Fault_VCC_UV bit in FAULT_STATUS3		
6	VCC_OV	High if the VCC supply pin 144 is above the $OV_{VCC/VFB}$ threshold (37V typ)	FAULT_STATUS1 See section 13.5.4 on page 59	
7	VC5_UV	High if the internal 5V startup supply is below its working range		
8	VC5_OV	High if the internal 5V startup supply is above its working range		
9	VDD_UV	High if the VDD supply pins 82 & 110 is below the UV_{VDD} threshold (1.95V typ)	CRITICAL_STATUS See section 13.5.13 on page 59	
10	VDD_OV	High if the VDD supply pins 82 & 110 is above the OV_{VDD} threshold (5.85V typ)		
11	+1.5VD_LDO_IN_UV	High if +1.5VD_LDO_IN pin 122 is below the $UV_{+1.5V_LDO_IN}$ threshold (1.75V typ)	FAULT_STATUS1 See section 13.5.4 on page 59	
12	+1.5VD_LDO_IN_OV	High if +1.5VD_LDO_IN pin 122 is above the $OV_{+1.5V_LDO_IN}$ threshold (5.85V typ)		
13	+1.5VA_LDO_IN_UV	High if +1.5VA_LDO_IN pin 132 is below the $UV_{+1.5V_LDO_IN}$ threshold (1.75V typ)		
14	+1.5VA_LDO_IN_OV	High if +1.5VA_LDO_IN pin 132 is above the $OV_{+1.5V_LDO_IN}$ threshold (5.85V typ)		
15	+1.5VA_LDO_OUT_UV	High if +1.5VA_LDO_OUT pin 133 is below the $UV_{+1.5V_LDO_OUT}$ threshold (1.47V typ)		

13.3.2 STATUS_REG1 REGISTER 0x501

Bits	Name	Description	Fault Register
0	+1.5VA_LDO_OUT_OV	High if +1.5VA_LDO_OUT pin 133 is above the OV _{+1.5VA_LDO_OUT} threshold (1.6V typ)	FAULT_STATUS1 See section 13.5.4 on page 59
1	+5V_LDOs_IN_UV	High if +5V_LDOs_IN pin 141 is below the UV _{+5V_LDOs_IN} threshold (5.99V typ)	
2	+5V_LDOs_IN_OV	High if +5V_LDOs_IN pin 141 is above the OV _{+5V_LDOs_IN} threshold (17.95V typ)	
3	+5V_LDO_OUT_UV	High if +5V_LDO_OUT pin 142 is below the UV _{+5V_LDO_OUT} threshold (4.5V typ)	
4	+5V_LDO_OUT_OV	High if +5V_LDO_OUT pin 142 is above the OV _{+5V_LDO_OUT} threshold (5.48V typ)	
5	+5.25V_LDO_OUT_UV	High if +5.25V_LDO_OUT pin 140 is below the UV _{+5.25V_LDO_OUT} threshold (4.73V typ)	
6	+5.25V_LDO_OUT_OV	High if +5.25V_LDO_OUT pin 140 is above the OV _{+5.25V_LDO_OUT} threshold (5.8V typ)	
7	BUCK_VFB_UV	High if the BUCK_VFB pin 135 voltage is below the UV _{BUCK_VFB} threshold (1.04V typ)	
8	BUCK_VFB_OV	High if the BUCK_VFB pin 135 voltage is above the OV _{BUCK_VFB} threshold (1.44V typ)	
9	VFB_UV	High if the VFB supply pin 72 is below the UV _{VCC/VFB} threshold (9V typ)	
10	VFB_OV	High if the VFB supply pin 72 is above the OV _{VCC/VFB} threshold (37V typ)	
11	+1.5VOSC_OV	High if the +1.5VOSC supply pin 79 is above the OV _{+1.5VOSC} threshold (1.64V typ)	
12	RESET	Logic level at the RESET input pin 83	
13 - 15	-	Unimplemented bits which read back as 0	

13.3.3 STATUS_REG2 REGISTER 0x502

Bits	Name	Description	Fault Register	GPIO
0	HEP1_Out	Output of the Hall Effect or other sensor at comparator input HEP1 pin 126	Not fault status	GPIO2 GPIO7
1	HEP2_Out	Output of the Hall Effect or other sensor at comparator input HEP2 pin 125		GPIO3 GPIO8
2	HEP3_Out	Output of the Hall Effect or other sensor at comparator input HEP3 pin 124		GPIO4 GPIO9
3	PRS_SRC1_OT	High if over-temperature fault detected in the 4-20mA power switch PRS_SRC1 pin 1	FAULT_STATUS3 See section 13.5.10 on page 63	GPIO6
4	PRS_SRC2_OT	High if over-temperature fault detected in the 4-20mA power switch PRS_SRC2 pin 4		GPIO1
5	PRS_SRC3_OT	High if over-temperature fault detected in the 4-20mA power switch PRS_SRC3 pin 7		GPIO5
6	DRV_P1_OT	High if over-temperature fault detected in the LVDT/resolver driver DRV_P1 pin 70		GPIO8
7	DRV_N1_OT	High if over-temperature fault detected in the LVDT/resolver driver DRV_N1 pin 71		GPIO6
8	DRV_P2_OT	High if over-temperature fault detected in the LVDT/resolver driver DRV_P2 pin 74		GPIO4
9	DRV_N2_OT	High if over-temperature fault detected in the LVDT/resolver driver DRV_N2 pin 75		GPIO2
10	DRV_P1_OC	High if the LVDT/resolver half-bridge driver DRV_P1 pin 70 output current exceeds the OC _{DRV#_#} over-current threshold in Electrical Characteristics		
11	DRV_N1_OC	High if the LVDT/resolver half-bridge driver DRV_N1 pin 71 output current exceeds the OC _{DRV#_#} over-current threshold in Electrical Characteristics		
12	DRV_P2_OC	High if the LVDT/resolver half-bridge driver DRV_P2 pin 74 output current exceeds the OC _{DRV#_#} over-current threshold in Electrical Characteristics		
13	DRV_N2_OC	High if the LVDT/resolver half-bridge driver DRV_N2 pin 75 output current exceeds the OC _{DRV#_#} over-current threshold in Electrical Characteristics		
14 - 15	-	Unimplemented bits which read back as 0		

13.3.4 STATUS_REG3 REGISTER 0x503

Bits	Name	Description	Fault Register
0	LVDT_P1_Fault	High if LVDT/resolver secondary input LVDT_P1 pin 37 appears to be floating	FAULT_STATUS3 See section 13.5.10 on page 63
1	LVDT_N1_Fault	High if LVDT/resolver secondary input LVDT_N1 pin 39 appears to be floating	
2	LVDT_P2_Fault	High if LVDT/resolver secondary input LVDT_P2 pin 40 appears to be floating	
3	LVDT_N2_Fault	High if LVDT/resolver secondary input LVDT_N2 pin 42 appears to be floating	
4	LVDT_P3_Fault	High if LVDT/resolver secondary input LVDT_P3 pin 43 appears to be floating	
5	LVDT_N3_Fault	High if LVDT/resolver secondary input LVDT_N3 pin 45 appears to be floating	
6	LVDT_P4_Fault	High if LVDT/resolver secondary input LVDT_P4 pin 46 appears to be floating	
7	LVDT_N4_Fault	High if LVDT/resolver secondary input LVDT_N4 pin 48 appears to be floating	
8	ISENSE1_Range_Fault	High if range fault detected in the current sense input ISENSE1 pin 60	
9	ISENSE2_Range_Fault	High if range fault detected in the current sense input ISENSE2 pin 61	
10	ISENSE3_Range_Fault	High if range fault detected in the current sense input ISENSE3 pin 62	
11	ISENSE4_Range_Fault	High if range fault detected in the current sense input ISENSE4 pin 63	
12	ISENSE5_Range_Fault	High if range fault detected in the current sense input ISENSE5 pin 64	
13	ISENSE_RTN_Range_Fault	High if range fault detected in the current sense ground reference ISENSE_RTN pin 65	
14 - 15	-	Unimplemented bits which read back as 0	

13.3.5 STATUS_REG4 REGISTER 0x504

Bits	Name	Description	Fault Register	GPIO
0	DRV_SNS_P1_Fault	High if an input fault was detected on the LVDT primary monitoring ADC input DRV_SNS_P1 pin 53. The fault type depends on the fault test selected in the CONTROL_REG1 register (section 13.6.2 on page 67)	FAULT_STATUS3 See section 13.5.10 on page 63	
1	DRV_SNS_N1_Fault	High if an input fault was detected on the LVDT primary monitoring ADC input DRV_SNS_N1 pin 54. The fault type depends on the fault test selected in the CONTROL_REG1 register (section 13.6.2 on page 67)		
2	DRV_SNS_P2_Fault	High if an input fault was detected on the LVDT primary monitoring ADC input DRV_SNS_P2 pin 50. The fault type depends on the fault test selected in the CONTROL_REG1 register (section 13.6.2 on page 67)		
3	DRV_SNS_N2_Fault	High if an input fault was detected on the LVDT primary monitoring ADC input DRV_SNS_N2 pin 51. The fault type depends on the fault test selected in the CONTROL_REG1 register (section 13.6.2 on page 67)		
4	HV1_Fault	High if an input fault was detected on the general purpose ADC input HV1 pin 56. The fault type depends on the fault test selected in the CONTROL_REG1 register (section 13.6.2 on page 67)		
5	HV2_Fault	High if an input fault was detected on the general purpose ADC input HV2 pin 57. The fault type depends on the fault test selected in the CONTROL_REG1 register (section 13.6.2 on page 67)		
6	TMP_1_Fault	High if one or more of the temperature measurement inputs TMP_REF1, TMP_P1, and TMP_N1 appears to be floating		
7	TMP_2_Fault	High if one or more of the temperature measurement inputs TMP_REF2, TMP_P2, and TMP_N2 appears to be floating		
8	TMP_3_Fault	High if one or more of the temperature measurement inputs TMP_REF3, TMP_P3, and TMP_N3 appears to be floating		
9	TMP_4_Fault	High if one or more of the temperature measurement inputs TMP_REF4, TMP_P4, and TMP_N4 appears to be floating		
10	TMP_5_Fault	High if one or more of the temperature measurement inputs TMP_REF5, TMP_P5, and TMP_N5 appears to be floating		
11	+5V_+5.25_OT	High if over-temperature fault detected in either the +5V or +5.25V LDO		GPIO2
12	+1.5VD_LDO_OT	High if over-temperature fault detected in the +1.5VD digital supply LDO		GPIO7
13	+1.5VA_LDO_OT	High if over-temperature fault detected in the +1.5VA analog supply LDO		GPIO4
14	BUCK_OT	High if over-temperature fault detected in the buck regulator		GPIO6
15	-	Unimplemented bit which reads back as 0		

13.3.6 STATUS_REG5 REGISTER 0x505

Any of these faults are maskable by the same bit position in STATUS_REG6 as to whether or not they latch the Fault_+5V_+1.5V fault bit in FAULT_STATUS0 (section 13.3.1 on page 46).

Bits	Name	Description	Fault Register
0	+5.25V_OPEN	High if a light load on the +5.25V supply (under a threshold in the 200µA to 2mA tolerance range) is detected	FAULT_STATUS0 See section 13.3.1 on page 46
1 - 7	-	Unimplemented bits which read back as 0	
8	+1.5VA_OV	High if the +1.5VA supply at pins 24, 34, 52, 66, & 79 is above the OV ^{+1.5VA} threshold (1.6V typ)	
9	+1.5VA_UV	High if the +1.5VA supply at pins 24, 34, 52, 66, & 79 is above the UV ^{+1.5VA} threshold (1.46V typ)	
10	+5V_OV	High if the +5V supply at pins 36, 68, & 131 is above the OV ^{+5V} threshold (5.56V typ)	
11	+5V_UV	High if the +5V supply at pins 36, 68, & 131 is below the UV ^{+5V} threshold (4.56V typ)	
12 - 15	-	Unimplemented bits which read back as 0	

13.3.7 STATUS_REG6 REGISTER 0x506

The operation of STATUS_REG6 is different to the other STATUS registers. It is a 16-bit read-write register with bits that default to 0 on power-up and after a reset. 5 bits are used to mask whether active-high status alerts in the same bit position in STATUS_REG5 latch the Fault_+5V_+1.5V fault bit in FAULT_STATUS0 (section 13.3.1 on page 46). Unless STATUS_REG6 is written setting at least one of these 5 bits high, the Fault_+5V_+1.5V fault bit in FAULT_STATUS0 will never latch a fault.

The remaining 11 bits (1 to 7, 12 to 15) can be used as general purpose read-write bits by the system. Since this register is cleared on power-up and reset, setting an unused bit to 1 can serve as a flag to test whether an unexpected power or reset event occurred.

Bits	Name	Description	Fault Register
0	+5.25V_OPEN_Fault_En	High to allow a +5.25V_OPEN fault in STATUS_REG5 to latch the Fault_+5V_+1.5V fault bit in FAULT_STATUS0	FAULT_STATUS0 See section 13.3.1 on page 46
1 - 7	-	Implemented bits which are unused internally	
8	+1.5VA_OV_Fault_En	High to allow a +1.5VA_OV fault in STATUS_REG5 to latch the Fault_+5V_+1.5V fault bit in FAULT_STATUS0	
9	+1.5VA_UV_Fault_En	High to allow a +1.5VA_UV fault in STATUS_REG5 to latch the Fault_+5V_+1.5V fault bit in FAULT_STATUS0	
10	+5V_OV_Fault_En	High to allow a +5V_OV fault in STATUS_REG5 to latch the Fault_+5V_+1.5V fault bit in FAULT_STATUS0	
11	+5V_UV_Fault_En	High to allow a +5V_UV fault in STATUS_REG5 to latch the Fault_+5V_+1.5V fault bit in FAULT_STATUS0	
12 - 15	-	Implemented bits which are unused internally	

13.4 Glitch (Fault Debounce) Registers

The glitch registers set up debounce times for fault and status signals to allow transient alerts to be ignored and not latched as faults. The debounce clock is $F_{OSC} / 1024$. The granularity of each debounce time setting is therefore $1024 / F_{OSC}$, which is $40\mu s$ for $F_{OSC} = 25.6MHz$ for example.

Address	Name	R/W	Register Contents															
			D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0x220	GLITCH_REG0	R/W	-	-	-	-	-	-	-	-	Fault_I/O_Filter							
0x221	GLITCH_REG1	R	-	-	-	-	-	-	-	Fault_I/O_Counter								
0x222	GLITCH_REG2	R	-	-	-	-	-	-	-	Fault_I/O_Counter								
0x223	GLITCH_REG3	R/W	-	-	-	-	-	Reset_Filter_Size										
0x224	GLITCH_REG4	R	-	-	-	-	Reset_Filter_Counter											
0x225	GLITCH_REG5	R/W	-	-	-	-	-	-	-	-	DRV1/2_Over-Current_Max							
0x226	GLITCH_REG6	R	-	-	-	-	-	-	-	DRV1_OC_Fault_Counter								
0x227	GLITCH_REG7	R	-	-	-	-	-	-	-	DRV2_OC_Fault_Counter								
0x228	GLITCH_REG8	R	-	-	-	-	-	-	-	-	-	-	-	HV_Fault_Counter				
0x229	GLITCH_REG9	R	-	-	-	-	-	-	-	-	-	-	-	DRV_SNS1_Fault_Counter				
0x22A	GLITCH_REGA	R	-	-	-	-	-	-	-	-	-	-	-	DRV_SNS2_Fault_Counter				
0x22B	GLITCH_REGB	R	-	-	-	-	-	-	-	-	-	-	-	VCC_UV_Counter				
0x22C	GLITCH_REGC	R	-	-	-	-	-	-	-	-	-	-	-	PRS_SRC_OT_Counter				
0x22D	GLITCH_REGD	R	-	-	-	-	-	-	-	-	-	-	-	TMP_Fault_Counter				
0x22E	GLITCH_REGE	R	-	-	-	-	-	-	-	-	-	-	-	ISENSE_Fault_Counter				
0x22F	GLITCH_REGF	R	-	-	-	-	-	-	-	-	-	-	-	Reg_Over_Temp_Counter				
0x230	GLITCH_REG10	R	-	-	-	-	-	-	-	-	-	-	-	VFB UV/OV_Counter				

13.4.1 GLITCH_REG0 REGISTER 0x220 (FAULT AND $\overline{\text{FAULT}}$ DEBOUNCE DELAY)

The GLITCH_REG0 register sets the delay before a short fault on either the FAULT output pin pin 103 or the $\overline{\text{FAULT}}$ output pin 102 is reported in the FAULT_STATUS0 register (section 13.5.1 on page 57). The delay is a programmable number of $F_{OSC} / 1024$ debounce clock periods. A short fault is detected when the output is driven to one logic level by the LX4580, but reads back internally as the opposite logic level. The logic level read back from the FAULT and $\overline{\text{FAULT}}$ outputs is available in the STATUS_REG0 register bits 0 and 1 (section 13.3.1 on page 46).

Set GLITCH_REG0 to 7 to configure the minimum delay of $8 \times 1024 / F_{OSC}$. This is $320\mu s$ for $F_{OSC} = 25.6MHz$. Set GLITCH_REG0 to 255 (0xFF) to configure the maximum delay of $256 \times 1024 / F_{OSC}$. This is $10.24ms$ for $F_{OSC} = 25.6MHz$. The default safe value 0x20 configures a delay of $32 \times 1024 / F_{OSC}$. This is $1.28ms$ for $F_{OSC} = 25.6MHz$.

Bits	Name	Safe Value	Description
0 - 7	Fault_I/O_Filter	0x20	Divides the 20 - 30MHz F_{OSC} clock by 1024, and then divides by a further 8 to 256 for values 7 to 255. Do not program values in the range 0 to 6
8 - 15		-	Unimplemented bits which read back as 0

13.4.2 GLITCH_REG1 REGISTER 0x221 (FAULT DEBOUNCE COUNT)

The GLITCH_REG1 register reports the number of counts of the $F_{OSC} / 1024$ debounce clock that have accumulated since a short fault on the FAULT output was detected. If the count reaches the value configured in the GLITCH_REG0 register, then a fault is latched in bit 14 of the FAULT_STATUS0 register (section 13.5.1 on page 57).

The logic level read back from the FAULT output is available in the STATUS_REG0 register (section 13.3.1 on page 46).

Bits	Name	Description
0 - 8	Fault_I/O_Counter	$F_{OSC} / 1024$ counts accumulated since a short fault on the FAULT output was detected
9 - 15	-	Unimplemented bits which read back as 0

13.4.3 GLITCH_REG2 REGISTER 0x222 (FAULT DEBOUNCE COUNT)

The GLITCH_REG2 register reports the number of counts of the $F_{OSC} / 1024$ debounce clock that have accumulated since a short fault on the $\overline{FAULT}$ output was detected. If the count reaches the value configured in the GLITCH_REG0 register, then a fault is latched in bit 13 of the FAULT_STATUS0 register (section 13.5.1 on page 57).

The logic level read back from the $\overline{FAULT}$ output is available in the STATUS_REG0 register (section 13.3.1 on page 46).

Bits	Name	Description
0 - 8	Fault_I/O_Counter	$F_{OSC} / 1024$ counts accumulated since a short fault on the $\overline{FAULT}$ output was detected
9 - 15	-	Unimplemented bits which read back as 0

13.4.4 GLITCH_REG3 REGISTER 0x223 (RESET INPUT DEBOUNCE DELAY)

The GLITCH_REG3 register sets the delay before a logic high input on the RESET input is accepted and the LX4580 is reset. The delay is a programmable number of $F_{OSC} / 1024$ debounce clock periods.

Set GLITCH_REG3 to 0 to configure minimal delay of $1 \times 1024 / F_{OSC}$. This is $40\mu s$ for $F_{OSC} = 25.6MHz$. This would be appropriate if RESET is a signal from a controller. Setting GLITCH_REG3 to 2047 (0x7F) configures the maximum delay of $2048 \times 1024 / F_{OSC}$. This is 81.92ms for $F_{OSC} = 25.6MHz$. This may be appropriate if RESET is a signal from a mechanical switch. The default safe value 0x20 configures a delay of $32 \times 1024 / F_{OSC}$. This is 1.28ms for $F_{OSC} = 25.6MHz$.

Bits	Name	Safe Value	Description
0 - 10	Reset_Filter_Size	0x20	Divides the 20 - 30MHz F_{OSC} clock by 1024, and then divides by a further 1 to 2048 for values 0 to 2047
11 - 15	-	-	Unimplemented bits which read back as 0

13.4.5 GLITCH_REG4 REGISTER 0x224 (RESET INPUT DEBOUNCE COUNT)

The GLITCH_REG4 register reports the number of counts of the $F_{OSC} / 1024$ debounce clock that have accumulated since a logic high input on the RESET input was detected. If the count reaches the value configured in the GLITCH_REG3 register, then the RESET input is accepted and the LX4580 is reset.

Bits	Name	Description
0 - 11	Reset_Filter_Counter	$F_{OSC} / 1024$ counts accumulated since the RESET input toggled from low to high
12 - 15	-	Unimplemented bits which read back as 0

GLITCH_REG5 REGISTER 0x225 (LVDT DRIVER MAX OVER-CURRENT TIME)

The GLITCH_REG5 register sets the soft-start delay before an over-current fault on one of the LVDT full-bridge driver outputs (DRV_P1, DRV_N1, DRV_P2, or DRV_N2) is recognized. The delay is a programmable number of $F_{OSC} / 1024$ debounce clock periods.

Set GLITCH_REG5 to 0 to configure the minimum delay of $1 \times 1024 / F_{OSC}$. This is $40\mu s$ for $F_{OSC} = 25.6MHz$. Set GLITCH_REG5 to 255 (0xFF) to configure the maximum delay of $256 \times 1024 / F_{OSC}$. This is 10.24ms for $F_{OSC} = 25.6MHz$. The default safe value 0x20 configures a delay of $32 \times 1024 / F_{OSC}$. This is 1.28ms for $F_{OSC} = 25.6MHz$.

Bits	Name	Safe Value	Description
0 - 7	DRV1/2_Over-Current_Max	0x20	Divides the 20 - 30MHz F_{OSC} clock by 1024, and then divides by a further 1 to 256 for values 0 to 255.
8 - 15	-	-	Unimplemented bits which read back as 0

13.4.6 GLITCH_REG6 REGISTER 0x226 (LVDT DRIVER DRV_P1 & DRV_N1 OVER-CURRENT COUNT)

The GLITCH_REG6 register reports the number of counts of the $F_{OSC} / 1024$ debounce clock that have accumulated since an over-current fault was detected on one or both of the LVDT full-bridge driver outputs DRV_P1 and DRV_N1.

If DRV1_OC_Fault_Counter reaches the value DRV1/2_Over-Current_Max configured in the GLITCH_REG5 register, then a fault is latched in the Fault_DRV1_OC bit in the FAULT_STATUS3 register (section 13.5.10 on page 63).

The DRV_P1_OC and DRV_N1_OC bits in the STATUS_REG2 register (section 13.3.3 on page 47) indicate whether the over-current fault was detected in the DRV_P1 driver output, the DRV_N1 driver output, or both.

Bits	Name	Description
0 - 8	DRV1_OC_Fault_Counter	$F_{OSC} / 1024$ counts accumulated since an over-current fault was detected on one or both of the LVDT full-bridge driver outputs DRV_P1 and DRV_N1
9 - 15	-	Unimplemented bits which read back as 0

13.4.7 GLITCH_REG7 REGISTER 0x227 (LVDT DRIVER DRV_P2 & DRV_N2 OVER-CURRENT COUNT)

The GLITCH_REG7 register reports the number of counts of the $F_{OSC} / 1024$ debounce clock that have accumulated since an over-current fault was detected on one or both of the LVDT full-bridge driver outputs DRV_P2 and DRV_N2.

If DRV2_OC_Fault_Counter reaches the value DRV1/2_Over-Current_Max configured in the GLITCH_REG5 register, then a fault is latched in the Fault_DRV2_OC bit in the FAULT_STATUS3 register (section 13.5.10 on page 63).

The DRV_P2_OC and DRV_N2_OC bits in the STATUS_REG2 register (section 13.3.3 on page 47) indicate whether the over-current fault was detected in the DRV_P2 driver output, the DRV_N2 driver output, or both.

Bits	Name	Description
0 - 8	DRV2_OC_Fault_Counter	$F_{OSC} / 1024$ counts accumulated since an over-current fault was detected on one or both of the LVDT full-bridge driver outputs DRV_P2 and DRV_N2
9 - 15	-	Unimplemented bits which read back as 0

13.4.8 GLITCH_REG8 REGISTER 0x228 (HV1 AND HV2 ANALOG INPUTS FAULT COUNT)

The GLITCH_REG8 register reports the number of counts of the $F_{OSC} / 1024$ debounce clock that have accumulated since an open, short, or over-voltage fault was detected on one or both of the HV1 and HV2 general purpose ADC inputs (section 11.19 on page 34).

If HV_Fault_Counter reaches a value of $31 \times 1024 / F_{OSC}$ (1.24ms for $F_{OSC} = 25.6\text{MHz}$), then a fault is latched in the Fault_HV bit in the FAULT_STATUS3 register (section 13.5.10 on page 63).

The HV1_Fault and HV2_Fault bits in the STATUS_REG4 register (section 13.3.5 on page 48) indicate whether the fault was detected in the HV1 input, the HV2 input, or both.

Bits	Name	Description
0 - 4	HV_Fault_Counter	$F_{OSC} / 1024$ counts accumulated since an open, short, or over-voltage fault was detected on one or both of the HV1 and HV2 general purpose ADC inputs
5 - 15	-	Unimplemented bits which read back as 0

13.4.9 GLITCH_REG9 REGISTER 0x229 (LVDT DRV_SNS_P1 AND DRV_SNS_N1 FAULT COUNT)

The GLITCH_REG9 register reports the number of counts of the $F_{OSC} / 1024$ debounce clock that have accumulated since an open, short, or over-voltage fault was detected on one or both of the DRV_SNS_P1 and DRV_SNS_N1 primary drive waveform monitoring ADC inputs (section 11.19 on page 34).

If DRV_SNS1_Fault_Counter reaches a value of $31 \times 1024 / F_{OSC}$ (1.24ms for $F_{OSC} = 25.6\text{MHz}$), then a fault is latched in the Fault_DRV_SNS1 bit in the FAULT_STATUS3 register (section 13.5.10 on page 63).

The DRV_SNS_P1_Fault and DRV_SNS_N1_Fault bits in the STATUS_REG4 register (section 13.3.5 on page 48) indicate whether the fault was detected in the DRV_SNS_P1 input, the DRV_SNS_N1 input, or both.

Bits	Name	Description
0 - 4	DRV_SNS1_Fault_Counter	$F_{OSC} / 1024$ counts accumulated since an open, short, or over-voltage fault was detected on one or both of the LVDT primary drive waveform monitoring ADC inputs DRV_SNS_P1 and DRV_SNS_N1
5 - 15	-	Unimplemented bits which read back as 0

13.4.10 GLITCH_REGA REGISTER 0x22A (LVDT DRV_SNS_P2 AND DRV_SNS_N2 FAULT COUNT)

The GLITCH_REGA register reports the number of counts of the $F_{OSC} / 1024$ debounce clock that have accumulated since an open, short, or over-voltage fault was detected on one or both of the DRV_SNS_P2 and DRV_SNS_N2 primary drive waveform monitoring ADC inputs (section 11.19 on page 34).

If DRV_SNS2_Fault_Counter reaches a value of $31 \times 1024 / F_{OSC}$ (1.24ms for $F_{OSC} = 25.6\text{MHz}$), then a fault is latched in the Fault_DRV_SNS2 bit in the FAULT_STATUS3 register (section 13.5.10 on page 63).

The DRV_SNS_P2_Fault and DRV_SNS_N2_Fault bits in the STATUS_REG4 register (section 13.3.5 on page 48) indicate whether the fault was detected in the DRV_SNS_P2 input, the DRV_SNS_N2 input, or both.

Bits	Name	Description
0 - 4	DRV_SNS2_Fault_Counter	$F_{OSC} / 1024$ counts accumulated since an open, short, or over-voltage fault was detected on one or both of the LVDT primary drive waveform monitoring ADC inputs DRV_SNS_P2 and DRV_SNS_N2
5 - 15	-	Unimplemented bits which read back as 0

13.4.11 GLITCH_REGB REGISTER 0x22B (VCC UNDER-VOLTAGE FAULT COUNT)

The GLITCH_REGB register reports the number of counts of the $F_{OSC} / 1024$ debounce clock that have accumulated since an under-voltage was detected on the VCC supply.

An under-voltage on VCC is indicated by the VCC_UV bit in both the STATUS_REG0 register (section 13.3.1 on page 46) and also latched in the Spike_VCC_UV bit in the FAULT_STATUS3 register (section 13.5.10 on page 63).

If the VCC supply remains under-voltage until VCC_UV_Counter reaches a value of $31 \times 1024 / F_{OSC}$ (1.24ms for $F_{OSC} = 25.6\text{MHz}$), then a further fault is latched in the Fault_VCC_UV bit in the FAULT_STATUS3 register.

Bits	Name	Description
0 - 4	VCC_UV_Counter	$F_{OSC} / 1024$ counts accumulated since an under-voltage was detected the VCC supply
5 - 15	-	Unimplemented bits which read back as 0

13.4.12 GLITCH_REGC REGISTER 0x22C (4-20mA DRIVER OVER-TEMPERATURE FAULT COUNT)

The GLITCH_REGC register reports the number of counts of the F_{OSC} debounce clock that have accumulated since an over-temperature fault detected in one or more of the three 4-20mA power sources, PRS_SRC#.

If PRS_SRC_OT_Counter reaches a value of $31 / F_{OSC}$ ($1.21\mu s$ for $F_{OSC} = 25.6MHz$), then a fault is latched in the Fault_PRS_SRC_OT bit in the FAULT_STATUS3 register (section 13.5.10 on page 63).

The three PRS_SRC1_OT, PRS_SRC2_OT, and PRS_SRC3_OT bits in the STATUS_REG2 register (section 13.3.3 on page 47) identify the over-temperature 4-20mA power source(s).

Bits	Name	Description
0 - 4	PRS_SRC_OT_Counter	F_{OSC} counts accumulated since an over-temperature fault was detected on one or more of the three 4-20mA power sources, PRS_SRC#
5 - 15	-	Unimplemented bits which read back as 0

13.4.13 GLITCH_REGD REGISTER 0x22D (TEMP SENSOR OPEN FAULT COUNT)

The GLITCH_REGD register reports the number of counts of the F_{OSC} clock that have accumulated since an open fault was detected on one or more of the five temperature sensor interfaces (section 11.18 on page 32).

If TMP_Fault_Counter reaches a value of $31 / F_{OSC}$ ($1.21\mu s$ for $F_{OSC} = 25.6MHz$), then a fault is latched in the Fault_TMP_float bit in the FAULT_STATUS3 register (section 13.5.10 on page 63).

The TMP_1_Fault, TMP_2_Fault, TMP_3_Fault, TMP_4_Fault, and TMP_5_Fault bits in the STATUS_REG4 register (section 13.3.5 on page 48) identify the faulty temperature sensor interface(s).

Bits	Name	Description
0 - 4	TMP_Fault_Counter	F_{OSC} counts accumulated since an open fault was detected on one or more of the five temperature sensor interfaces
5 - 15	-	Unimplemented bits which read back as 0

13.4.14 GLITCH_REGE REGISTER 0x22E (ISENSE ADC INPUT RANGE FAULT COUNT)

The GLITCH_REGE register reports the number of counts of the F_{OSC} clock that have accumulated since an over-range fault was detected on one or more of the five current sensor interfaces (section 11.20 on page 35).

If ISENSE_Fault_Counter reaches a value of $31 / F_{OSC}$ ($1.21\mu s$ for $F_{OSC} = 25.6MHz$), then a fault is latched in the Fault_ISENSE_Range bit in the FAULT_STATUS3 register (section 13.5.10 on page 63).

The ISENSE1_Range_Fault, ISENSE2_Range_Fault, ISENSE3_Range_Fault, ISENSE4_Range_Fault, ISENSE5_Range_Fault, and ISENSE_RTN_Range_Fault bits in the STATUS_REG3 register (section 13.3.4 on page 48) identify the faulty ISENSE interface(s).

Bits	Name	Description
0 - 4	ISENSE_Fault_Counter	F_{OSC} counts accumulated since an over-range fault was detected on one or more of the five current sensor interfaces
5 - 15	-	Unimplemented bits which read back as 0

13.4.15 GLITCH_REGF REGISTER 0x22F (REGULATOR OVER-TEMPERATURE FAULT COUNT)

The GLITCH_REGF register reports the number of counts of the $F_{OSC} / 8$ debounce clock that have accumulated since an over-temperature fault was detected on one or more of the four internal linear regulators (+5.25V, +5V, +1.5VD, +1.5VA) or the buck pass transistor.

If Reg_Over_Temp_Counter reaches a value of $31 \times 8 / F_{OSC}$ ($9.7\mu s$ for $F_{OSC} = 25.6MHz$), then a fault is latched in the Fault_OT bit in the FAULT_STATUS3 register (section 13.5.10 on page 63).

The +5V_+5.25_OT, +1.5VD_LDO_OT, +1.5VA_LDO_OT, and BUCK_OT bits in the STATUS_REG4 register (section 13.3.5 on page 48) identify regulators in over-temperature shutdown. See section 11.2.7 on page 23.

Bits	Name	Description
0 - 4	Reg_Over_Temp_Counter	$F_{OSC} / 8$ counts accumulated since one or more regulator over-temperature was detected
5 - 15	-	Unimplemented bits which read back as 0

13.4.16 GLITCH_REG10 REGISTER 0x230 (VFB UNDER-/OVER-VOLTAGE FAULT COUNT)

The GLITCH_REG10 register reports the number of counts of the $F_{OSC} / 1024$ debounce clock that have accumulated since an under- or over-voltage was detected on the VFB supply.

If the VFB supply remains under- or over-voltage until VFB_UV/OV_Counter reaches a value of $31 \times 1024 / F_{OSC}$ (1.24ms for $F_{OSC} = 25.6MHz$), then a fault is latched in the Fault_VFB bit in the FAULT_STATUS1 register (section 13.5.4 on page 59).

The VFB_UV, and VFB_OV bits in the STATUS_REG1 register (section 13.3.2 on page 47) provide VFB supply under- and over-voltage status.

Bits	Name	Description
0 - 4	VFB_UV/OV_Counter	$F_{OSC} / 1024$ counts accumulated since an under- or over-voltage was detected the VFB supply
5 - 15	-	Unimplemented bits which read back as 0

13.5 Fault Registers

There are 2 types of fault which are detected and acted on by the LX4580:

- 64 non-critical faults which cause the FAULT pin 103 to go high and the $\overline{\text{FAULT}}$ pin 102 to go low to signal the fault
 - Faults are latched and reported in the 4 registers FAULT_STATUS0 to FAULT_STATUS3
 - Faults can be cleared in the 4 matching registers FAULT_CLEAR0 to FAULT_CLEAR3
 - Faults can be set to also initiate Safe Mode in the 4 matching registers FAULT_MASK0 to FAULT_MASK3
 - For some faults, the FAULT_MASK# register doesn't just select Safe Mode, but also disables the FAULT and $\overline{\text{FAULT}}$ functionality for those faults if Safe Mode is disabled. This prevents faults being unnecessarily alerted for situations which occur because the functionality is unused in the application:
 - Fault_VFB alerting that the LVDT rail is open, when the LVDT drivers are not used
 - Fault_BUCK alerting that the buck is out of regulation, when the buck regulator is not used
 - Fault_ISENSE_float alerting that one of the current sense amplifier inputs appears to be floating
 - Fault_LVDT1_float alerting that one of the LVDT_#1 or LVDT_#2 amplifier inputs appears to be floating
 - Fault_LVDT2_float alerting that one of the LVDT_#3 or LVDT_#4 amplifier inputs appears to be floating
 - Fault_DRV1_float alerting that one of the LVDT DRV_SNS_#1 amplifier inputs appears to be floating
 - Fault_DRV2_float alerting that one of the LVDT DRV_SNS_#2 amplifier inputs appears to be floating
 - Fault_HV alerting that one of the HV1 or HV2 general purpose 10-bit ADC inputs appears to be floating, shorted to GND, or over-voltage
 - Fault_TMP_float alerting that one of the TMP_## amplifier inputs appears to be floating
- 3 critical faults (section 13.5.13 on page 65) which cause the LX4580 to shut down and restart into Startup Mode (section 12.1 on page 42) to attempt to clear the unsafe condition
 - Critical faults are clock failure or an out of range supply voltage on either the VDD or the 1.5VD logic supplies
 - Both FAULT and $\overline{\text{FAULT}}$ go low to signal a critical fault, and remain low until the LX4580 restarts safely
 - All registers except CRITICAL_STATUS are cleared as part of the restart procedure
 - If any critical fault(s) still exist, the LX4580 will remain in reset and serial bus access will be unavailable
 - If no critical faults exist, the LX4580 will indicate recovery by taking the FAULT pin high
 - The fault status register CRITICAL_STATUS can then be read to check which critical faults were latched

Writing 0xC3 to the SAFE_FORCE register forces the LX4580 into safe mode, tri-stating all outputs except the serial and JTAG interfaces. Writing another value to the SAFE_FORCE register or taking the RESET pin high clears the register to exit forced safe mode. The read-only SAFE_STATUS register provides safe mode status.

Address	Name	R/W	Register Contents															
			D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0x100	FAULT_STATUS0	R	A high bit in a FAULT_STATUS register indicates a fault															
0x101	FAULT_STATUS1	R																
0x102	FAULT_STATUS2	R																
0x103	FAULT_STATUS3	R																
0x104	FAULT_CLEAR0	W	Setting a bit high in a FAULT_CLEAR register clears the corresponding bit in the FAULT_STATUS register															
0x105	FAULT_CLEAR1	W																
0x106	FAULT_CLEAR2	W																
0x107	FAULT_CLEAR3	W																
0x108	FAULT_MASK0	R/W	For most faults, a clear bit in its FAULT_MASK register sets whether or not that fault causes the LX4580 to enter Safe Mode. FAULT and $\overline{\text{FAULT}}$ always activate on these faults. For some faults, a clear bit in its FAULT_MASK register sets both whether or not that fault causes the LX4580 to enter Safe Mode, and also whether FAULT and $\overline{\text{FAULT}}$ activate															
0x109	FAULT_MASK1	R/W																
0x10A	FAULT_MASK2	R/W																
0x10B	FAULT_MASK3	R/W																
0x10C	CRITICAL_STATUS	R	High bits indicate which fault(s) caused the LX4580 to shut down and restart															
0x10D	CRITICAL_CLEAR	W	Setting a bit high in a CRITICAL_CLEAR register clears the corresponding bit in the CRITICAL_STATUS register															
0x10E	SAFE_FORCE	R/W	-	-	-	-	-	-	-	-	Force safe mode							
0x10F	SAFE_STATUS	R	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	SM

13.5.1 FAULT_STATUS0 REGISTER 0x100

Faults alerted in fault status register FAULT_STATUS0 can be cleared by clearing the same bit position in fault reset register FAULT_CLEAR0, after the fault has been fixed. Any of these faults are maskable by the same bit position in fault mask FAULT_MASK0 as to whether they cause the LX4580 to initiate Safe Mode if the fault occurs.

High if uncorrectable double bit error on SPI1 bus. Bus transaction is invalid and was rejected

High if single bit error corrected on SPI2 bus. Bus transaction completed successfully

Bit	Name	Description
0	GPIO_Fault	High if overload detected in one or more GPIO outputs (section 13.11 on page 83). Compare GPIO output logic levels in GPIO_REG6 with readback values in GPIO_REG5 to identify faulty output(s). Fault conditions can be removed by setting overloaded outputs to inputs in register GPIO_REG3
1	-	Implemented bit with reserved function
2	CLKGEN_Fault	Fault in clock generation block. sources: #1,2 only are checked when ISENSE_EN is high (CLKGEN_REG1, one or more of bits 4-0 high) 1) write to CLKGEN_REG0/2/3/4. 2) ISENSE_SINC_DIV < 2 (in CLKGEN_REG2) 3) LVDT12_DE_DIV < 7 or LVDT12_SINC_DIV < 7. 3) LVDT34_DE_DIV < 7 or LVDT34_SINC_DIV < 7 disable ISENSE (write CLKGEN_REG1, bits 4-0 = 0). read CLKGEN_REG2/3/4, identify bad configuration If none are mis-configured, it was a bad write command
3	POR_Fault	High if +1.5VD under-voltage or over-voltage fault detected for longer than longer than 255 / FOSC (10µs for FOSC = 25.6MHz). The +1.5VD_UV# and +1.5VD_OV# bits in the POR_REG1 register (section 13.2.1 on page 45) provide real-time status of these voltage detectors
4	WD_Clock_Fault	Either the internal watchdog clock is stuck, or the watchdog clock and system clock are not running at the expected relative frequency. See section 13.15 on page 93
5	Fault_+5V_+1.5V	High if +1.5VA and/or +5V under- or over-voltage fault detected or the +5.25V output is underloaded. Faults only latch here if enabled in STATUS_REG6. See section 11.2.2 on page 22
6	OTP_Corrected_Fault	High if a single bit error was detected and corrected when reading OTP. At power-up, means a single bit error in the trim and coms section was detected during the power-up load of OTP state After power-up, means that the prior operation had a correctable bit error No action is required (it was corrected), but to understand failure, put OTP in raw mode (OTP_REG5) and read out data. Check SECDED encoding vs data read.
7	OTP_Fault	A write to a register occurred at an illegal time or an attempt to program an OTP bit in a locked sector Write was blocked and did not happen, or check what OTP commands just occurred, or a program command to a locked bit, or write when the OPT controller is not in the idle state, or a program command when the unlock pin is low, or a write to OTP_REG0 (OTP memory address) with bena[0] low or address chosen > 127, or a write to OTP_REG6 (shadow reload) that's not 16bit write or not the keyword data, or a write to a trim register while shadow load is ongoing
8	OTP_Error_Fault	Bad load of trim bits from OTP memory Indicates ECC error (>=2 bit) or CRC error or a stuck bit in the trim registers. Read trim registers, read OTP memory and compare contents. If that looks good, check ECC and CRC encoding (will need to read in "raw" mode to see ECC encoding)
9	Trim_Fault	High if a write was attempted to registers TRIM_REG0 to TRIM_REG3 when the UNLOCK input is low. The write transaction was blocked and did not happen
10	Status_Fault	Factory reserved
11	Control_Fault	Factory reserved
12	SAR_Fault	1) Fault in PWMs (configuration or synchronization), 2) Attempt to start new burst before last burst finishes, 3) Bad SAR configuration, write to SAR_REG0/1/3/6/7/8/9/10-17 when ISENSE_EN 4) Die temperature too high For #3 or configuration issue in #1, they will fire when ISENSE_EN is turned on (CLKGEN_REG1[4:0]). If PWM period is too short for one SAR read to finish before next SAR burst starts or ISENSE_EN is not turned off for an entire burst #2 may occur. To Check #4, check die temperature SAR target stored values vs SAR_REGB. If none of those, check synchronization issue between filters and PWMs for a transient glitch.
13	FAULT_I/O_Fault	High if the FAULT output appears to be shorted. A short fault is detected when the output is driven to one logic level by the LX4580, but reads back as the opposite logic level. The FAULT_IN bit in

		STATUS_REG0 (section 13.3.1 on page 46) provides real-time status of this read-back
14	FAULT_I/O_Fault	High if the FAULT output appears to be shorted. A short fault is detected when the output is driven to one logic level by the LX4580, but reads back as the opposite logic level. The FAULT_IN bit in STATUS_REG0 (section 13.3.1 on page 46) provides real-time status of this read-back
15	-	Implemented bit with reserved function

13.5.2 FAULT_CLEAR0 REGISTER 0x104

Faults alerted in fault status register FAULT_STATUS0 can be cleared by clearing the same bit position in fault reset register FAULT_CLEAR0, after the fault has been cleared. Any of these faults cause the FAULT pin 103 to go high and the FAULT pin 102 to go low to signal the fault.

Bit	Name	Description
0	GPIO_Fault	Set this bit to clear the GPIO_Fault bit in the FAULT_STATUS0 register
1	-	Implemented bit with reserved function
2	CLKGEN_Fault	Set this bit to clear the CLKGEN_Fault bit in the FAULT_STATUS0 register
3	POR_Fault	Set this bit to clear the POR_Fault bit in the FAULT_STATUS0 register
4	WD_Clock_Fault	Set this bit to clear the WD_Clock_Fault bit in the FAULT_STATUS0 register
5	Fault_+5V_+1.5V	Set this bit to clear the Fault_+5V_+1.5V bit in the FAULT_STATUS0 register
6	OTP_Corrected_Fault	Set this bit to clear the OTP_Corrected_Fault bit in the FAULT_STATUS0 register
7	OTP_Fault	Set this bit to clear the OTP_Fault bit in the FAULT_STATUS0 register
8	OTP_Error_Fault	Set this bit to clear the OTP_Error_Fault bit in the FAULT_STATUS0 register
9	Trim_Fault	Set this bit to clear the Trim_Fault bit in the FAULT_STATUS0 register
10	Status_Fault	Factory reserved. Write either a 0 or a 1 to this bit
11	Control_Fault	Factory reserved. Write either a 0 or a 1 to this bit
12	SAR_Fault	Set this bit to clear the SAR_Fault bit in the FAULT_STATUS0 register
13	FAULT_I/O_Fault	Set this bit to clear the FAULT_I/O_Fault bit in the FAULT_STATUS0 register
14	FAULT_I/O_Fault	Set this bit to clear the FAULT_I/O_Fault bit in the FAULT_STATUS0 register
15	-	

13.5.3 FAULT_MASK0 REGISTER 0x108

Faults alerted in fault status register FAULT_STATUS0 (section 13.5.1 on page 57) are maskable by the same bit position in fault mask register FAULT_MASK0 as to whether they cause the LX4580 to initiate Safe Mode if the fault occurs. Faults are always indicated by a bit set in the FAULT_STATUS0 register regardless of the FAULT_MASK0 setting.

Bit	Name	Safe Value	Description
0	GPIO_Fault	0	Bit = 0: On fault, FAULT → high, $\overline{\text{FAULT}}$ → low, LX4580 enters Safe Mode Bit = 1: On fault, FAULT → high, $\overline{\text{FAULT}}$ → low, LX4580 does not enter Safe Mode
1	-	-	Implemented bit with reserved function
2	CLKGEN_Fault	0	Bit = 0: On fault, FAULT → high, $\overline{\text{FAULT}}$ → low, LX4580 enters Safe Mode Bit = 1: On fault, FAULT → high, $\overline{\text{FAULT}}$ → low, LX4580 does not enter Safe Mode
3	POR_Fault	0	
4	WD_Clock_Fault	0	
5	Fault_+5V_+1.5V	0	
6	OTP_Corrected_Fault	0	
7	OTP_Fault	0	
8	OTP_Error_Fault	0	
9	Trim_Fault	0	
10	Status_Fault	0	Factory reserved. Write a 0 to this bit
11	Control_Fault	0	Factory reserved. Write a 0 to this bit
12	SAR_Fault	0	Bit = 0: On fault, FAULT → high, $\overline{\text{FAULT}}$ → low, LX4580 enters Safe Mode Bit = 1: On fault, FAULT → high, $\overline{\text{FAULT}}$ → low, LX4580 does not enter Safe Mode
13	FAULT_I/O_Fault	0	
14	FAULT_I/O_Fault	0	
15	-	-	Implemented bit with reserved function

13.5.4 FAULT_STATUS1 REGISTER 0x101

Faults alerted in fault status register FAULT_STATUS1 can be cleared by clearing the same bit position in fault reset register FAULT_CLEAR1, after the fault has been fixed. Any of these faults are maskable by the same bit position in fault mask FAULT_MASK1 as to whether they cause the LX4580 to initiate Safe Mode if the fault occurs.

Bit	Name	Description
0	Fault_Command_Ch2	High if incorrect packet order received on SPI2 bus. Bus transaction is invalid and was rejected
1	Fault_Command_Ch1	High if incorrect packet order received on SPI1 bus. Bus transaction is invalid and was rejected
2	Fault_Arbiter_Ch2	High if invalid state machine condition detected for SPI2 bus. Bus transaction was rejected
3	Fault_Arbiter_Ch1	High if invalid state machine condition detected for SPI1 bus. Bus transaction was rejected
4	Fault_DED_Ch2	High if uncorrectable double bit error on SPI2 bus. Bus transaction is invalid and was rejected
5	Fault_DED_Ch1	High if uncorrectable double bit error on SPI1 bus. Bus transaction is invalid and was rejected
6	Alert_SEC_Ch2	High if single bit error corrected on SPI2 bus. Bus transaction completed successfully
7	Alert_SEC_Ch1	High if single bit error corrected on SPI1 bus. Bus transaction completed successfully
8	Fault_+1.5VOSC	High if +1.5VOSC pin 79 over-voltage fault detected. The +1.5VOSC_OV bit in the STATUS_REG1 register (section 13.3.2 on page 47) provides real-time status of this voltage detector
9	Fault_VFB	High if VFB supply pin 72 under-voltage or over-voltage fault detected. The VFB_UV and VFB_OV bits in the STATUS_REG1 register (section 13.3.2 on page 47) provide real-time status of these voltage detectors
10	Fault_BUCK	High if BUCK_VFB feedback input pin 135 under-voltage or over-voltage fault detected. The BUCK_VFB_UV and BUCK_VFB_OV bits in the STATUS_REG1 register (section 13.3.2 on page 47) provide real-time status of these voltage detectors
11	Fault_VCC_OV	High if VCC supply pin 144 over-voltage fault detected. The VCC_OV bit in the STATUS_REG0 register (section 13.3.1 on page 46) provides real-time status of this voltage detector
12	Fault_+1.5V	High if +1.5VD_LDO_IN pin 122 and/or +1.5VA_LDO_IN pin 132 and/or +1.5VA_LDO_OUT pin 133 under-voltage or over-voltage fault detected. The +1.5VD_LDO_IN_UV, +1.5VD_LDO_IN_OV, +1.5VA_LDO_IN_UV, +1.5VA_LDO_IN_OV, and +1.5VA_LDO_OUT_UV bits in the STATUS_REG0 register (section 13.3.1 on page 46) and the +1.5VA_LDO_OUT_OV bit in the STATUS_REG1 register (section 13.3.2 on page 47) provide real-time status of these voltage detectors
13	Fault_+5V	High if +5V_LDOs_IN pin 141 and/or +5V_LDO_OUT pin 142 and/or +5.25V_LDO_OUT pin 140 and/or internal 5V startup supply under-voltage or over-voltage fault detected. The VC5_UV and VC5_OV bits in the STATUS_REG0 register (section 13.3.1 on page 46) and the +5V_LDOs_IN_UV, +5V_LDOs_IN_OV, +5V_LDO_OUT_UV, +5V_LDO_OUT_OV, +5.25V_LDO_OUT_UV, and +5.25V_LDO_OUT_OV bits in the STATUS_REG1 register (section 13.3.2 on page 47) provide real-time status of these voltage detectors
14	Fault_UART1	High if UART1 transaction had one or more of these faults: incorrect packet order, parity error, bad stop bit, uncorrectable double bit error. Bus transaction is invalid and was rejected
15	Fault_UART2	High if UART2 transaction had one or more of these faults: incorrect packet order, parity error, bad stop bit, uncorrectable double bit error. Bus transaction is invalid and was rejected

13.5.5 FAULT_CLEAR1 REGISTER 0x105

Faults alerted in fault status register FAULT_STATUS1 can be cleared by clearing the same bit position in fault reset register FAULT_CLEAR1, after the fault has been fixed. Any of these faults are maskable by the same bit position in fault mask FAULT_MASK1 as to whether they cause the LX4580 to initiate Safe Mode if the fault occurs.

Bit	Name	Description
0	Fault_Command_Ch2	Set this bit to clear the Fault_Command_Ch2 bit in the FAULT_STATUS1 register
1	Fault_Command_Ch1	Set this bit to clear the Fault_Command_Ch1 bit in the FAULT_STATUS1 register
2	Fault_Arbiter_Ch2	Set this bit to clear the Fault_Arbiter_Ch2 bit in the FAULT_STATUS1 register
3	Fault_Arbiter_Ch1	Set this bit to clear the Fault_Arbiter_Ch1 bit in the FAULT_STATUS1 register
4	Fault_DED_Ch2	Set this bit to clear the Fault_DED_Ch2 bit in the FAULT_STATUS1 register
5	Fault_DED_Ch1	Set this bit to clear the Fault_DED_Ch1 bit in the FAULT_STATUS1 register
6	Alert_SEC_Ch2	Set this bit to clear the Alert_SEC_Ch2 bit in the FAULT_STATUS1 register
7	Alert_SEC_Ch1	Set this bit to clear the Alert_SEC_Ch1 bit in the FAULT_STATUS1 register
8	Fault_+1.5VOSC	Set this bit to clear the Fault_+1.5VOSC bit in the FAULT_STATUS1 register
9	Fault_VFB	Set this bit to clear the Fault_VFB bit in the FAULT_STATUS1 register
10	Fault_BUCK	Set this bit to clear the Fault_BUCK bit in the FAULT_STATUS1 register
11	Fault_VCC_OV	Set this bit to clear the Fault_VCC_OV bit in the FAULT_STATUS1 register
12	Fault_+1.5V	Set this bit to clear the Fault_+1.5V bit in the FAULT_STATUS1 register
13	Fault_+5V	Set this bit to clear the Fault_+5V bit in the FAULT_STATUS1 register
14	Fault_UART1	Set this bit to clear the Fault_UART1 bit in the FAULT_STATUS1 register
15	Fault_UART2	Set this bit to clear the Fault_UART2 bit in the FAULT_STATUS1 register

13.5.6 FAULT_MASK1 REGISTER 0x109

Faults alerted in fault status register FAULT_STATUS1 are maskable by the same bit position in fault mask register FAULT_MASK1 as to whether they cause the LX4580 to initiate Safe Mode if the fault occurs. Faults are always indicated by a bit set in the FAULT_STATUS1 register regardless of the FAULT_MASK1 setting.

Bit	Name	Safe Value	Description
0	Fault_Command_Ch2	0	Bit = 0: On fault, FAULT → high, $\overline{\text{FAULT}}$ → low, LX4580 enters Safe Mode Bit = 1: On fault, FAULT → high, $\overline{\text{FAULT}}$ → low, LX4580 does not enter Safe Mode
1	Fault_Command_Ch1	0	
2	Fault_Arbiter_Ch2	0	
3	Fault_Arbiter_Ch1	0	
4	Fault_DED_Ch2	0	
5	Fault_DED_Ch1	0	
6	Alert_SEC_Ch2	0	
7	Alert_SEC_Ch1	0	
8	Fault_+1.5VOSC	0	Bit = 0: On fault, FAULT → high, $\overline{\text{FAULT}}$ → low, LX4580 enters Safe Mode Bit = 1: On fault, FAULT and $\overline{\text{FAULT}}$ are unchanged, LX4580 does not enter Safe Mode
9	Fault_VFB	0	
10	Fault_BUCK	0	Bit = 0: On fault, FAULT → high, $\overline{\text{FAULT}}$ → low, LX4580 enters Safe Mode Bit = 1: On fault, FAULT → high, $\overline{\text{FAULT}}$ → low, LX4580 does not enter Safe Mode
11	Fault_VCC_OV	0	
12	Fault_+1.5V	0	
13	Fault_+5V	0	
14	Fault_UART1	0	
15	Fault_UART2	0	

13.5.7 FAULT_STATUS2 REGISTER 0x102

Faults alerted in fault status register FAULT_STATUS2 can be cleared by clearing the same bit position in fault reset register FAULT_CLEAR2, after the fault has been fixed. Any of these faults are maskable by the same bit position in fault mask FAULT_MASK2 as to whether they cause the LX4580 to initiate Safe Mode if the fault occurs.

Note: The LVDT#_Period and LVDT#_Frame registers must be configured when all of the 5 ISENSE current sense inputs are disabled, by clearing the 5 ISENSE#_EN bits in the CLKGEN_REG1 register (section 13.7.2 on page 68). If any of these bits is set when either of the LVDT#_Period or LVDT#_Frame registers is written, then the appropriate LVDT#_Fault will be asserted in the FAULT_STATUS2 register (section 0 on page 61).

Bit	Name	Description
0	-	Implemented bit with reserved function
1	-	Implemented bit with reserved function
2	Filter_Fault0	LVDT Ch1 RMS overflow. The MSB of the signal is outside of the range observed. So the signal will likely look like noise.
3	Filter_Fault1	LVDT Ch2 RMS overflow. The MSB of the signal is outside of the range observed. So the signal will likely look like noise.
4	Filter_Fault2	LVDT Ch3 RMS overflow. The MSB of the signal is outside of the range observed. So the signal will likely look like noise.
5	Filter_Fault3	LVDT Ch4 RMS overflow. The MSB of the signal is outside of the range observed. So the signal will likely look like noise.
6	Filter_Fault4	ISENSE1 signal range overflow. The MSB of the signal is outside of the range observed. So the signal will likely look like noise.
7	Filter_Fault5	ISENSE2 signal range overflow. The MSB of the signal is outside of the range observed. So the signal will likely look like noise.
8	Filter_Fault6	ISENSE3 signal range overflow. The MSB of the signal is outside of the range observed. So the signal will likely look like noise.
9	Filter_Fault7	ISENSE4 signal range overflow. The MSB of the signal is outside of the range observed. So the signal will likely look like noise.
10	Filter_Fault8	ISENSE5 signal range overflow. The MSB of the signal is outside of the range observed. So the signal will likely look like noise.
11	LVDT2_Fault	Any of: - A write to either of the LVDT2_Period and LVDT2_Frame registers when any of the 5 ISENSE#_EN is enabled in the CLKGEN_REG1 register (section 13.7.2 on page 68) - Invalid LVDT1_Period and LVDT1_Frame register data combinations - The LVDT2 driver is out of sync with the LVDT filter settings (section 13.10 on page 76)
12	LVDT1_Fault	Any of: - A write to either of the LVDT1_Period and LVDT1_Frame registers when any of the 5 ISENSE#_EN is enabled in the CLKGEN_REG1 register (section 13.7.2 on page 68) - Invalid LVDT1_Period and LVDT1_Frame register data combinations - The LVDT1 driver is out of sync with the LVDT filter settings (section 13.10 on page 76)
13	UNLOCK_High	High if UNLOCK input pin is high. Since the unlocked state enables actions that are normally blocked, taking UNLOCK high latches this fault which can be used or ignored. The UNLOCK bit in the STATUS_REG0 register (section 13.3.1 on page 46) provides real-time UNLOCK input pin status
14	UART1_Noise_Fault	Noise on receiver (data recovered). Caused by inconsistent bit sample or single bit correction
15	UART2_Noise_Fault	Noise on receiver (data recovered). Caused by inconsistent bit sample or single bit correction

13.5.8 FAULT_CLEAR2 REGISTER 0x106

Faults alerted in fault status register FAULT_STATUS2 can be cleared by clearing the same bit position in fault reset register FAULT_CLEAR2, after the fault has been cleared.

Any of these faults cause the FAULT pin 103 to go high and the $\overline{\text{FAULT}}$ pin 102 to go low to signal the fault.

Bit	Name	Description
0	-	Implemented bit with reserved function
1	-	Implemented bit with reserved function
2	Filter_Fault0	Set this bit to clear the Filter0_Fault0 bit in the FAULT_STATUS2 register
3	Filter_Fault1	Set this bit to clear the Filter1_Fault0 bit in the FAULT_STATUS2 register
4	Filter_Fault2	Set this bit to clear the Filter2_Fault0 bit in the FAULT_STATUS2 register
5	Filter_Fault3	Set this bit to clear the Filter3_Fault0 bit in the FAULT_STATUS2 register
6	Filter_Fault4	Set this bit to clear the Filter4_Fault0 bit in the FAULT_STATUS2 register
7	Filter_Fault5	Set this bit to clear the Filter5_Fault0 bit in the FAULT_STATUS2 register
8	Filter_Fault6	Set this bit to clear the Filter6_Fault0 bit in the FAULT_STATUS2 register
9	Filter_Fault7	Set this bit to clear the Filter7_Fault0 bit in the FAULT_STATUS2 register
10	Filter_Fault8	Set this bit to clear the Filter8_Fault0 bit in the FAULT_STATUS2 register
11	LVDT2_Fault	Set this bit to clear the LVDT2_Fault bit in the FAULT_STATUS2 register
12	LVDT1_Fault	Set this bit to clear the LVDT1_Fault bit in the FAULT_STATUS2 register
13	UNLOCK_High	Set this bit to clear the UNLOCK_High bit in the FAULT_STATUS2 register
14	UART1_Noise_Fault	Set this bit to clear the UART1_Noise_Fault bit in the FAULT_STATUS2 register
15	UART2_Noise_Fault	Set this bit to clear the UART2_Noise_Fault bit in the FAULT_STATUS2 register

13.5.9 FAULT_MASK2 REGISTER 0x10A

Faults alerted in fault status register FAULT_STATUS2 are maskable by the same bit position in fault mask register FAULT_MASK2 as to whether they cause the LX4580 to initiate Safe Mode if the fault occurs. Faults are always indicated by a bit set in the FAULT_STATUS2 register regardless of the FAULT_MASK2 setting.

Bit	Name	Safe Value	Description
0	-	-	Implemented bit with reserved function
1	-	-	Implemented bit with reserved function
2	Filter_Fault0	0	Bit = 0: On fault, FAULT → high, $\overline{\text{FAULT}}$ → low, LX4580 enters Safe Mode Bit = 1: On fault, FAULT → high, $\overline{\text{FAULT}}$ → low, LX4580 does not enter Safe Mode
3	Filter_Fault1	0	
4	Filter_Fault2	0	
5	Filter_Fault3	0	
6	Filter_Fault4	0	
7	Filter_Fault5	0	
8	Filter_Fault6	0	
9	Filter_Fault7	0	
10	Filter_Fault8	0	
11	LVDT2_Fault	0	
12	LVDT1_Fault	0	
13	UNLOCK_High	0	
14	UART1_Noise_Fault	0	
15	UART2_Noise_Fault	0	

13.5.10 FAULT_STATUS3 REGISTER 0x103

Faults alerted in fault status register FAULT_STATUS3 can be cleared by clearing the same bit position in fault reset register FAULT_CLEAR3, after the fault has been fixed. Any of these faults are maskable by the same bit position in fault mask FAULT_MASK3 as to whether they cause the LX4580 to initiate Safe Mode if the fault occurs.

Bit	Name	Description
0	Fault_ISENSE_Range	High if range fault detected in one or more of the five ISENSE current sensing interfaces. There is a settling time of $31 / F_{OSC}$ ($1.21\mu s$ for $F_{OSC} = 25.6MHz$) between fault detection and the fault being latched here, with the GLITCH_REGE register (section 13.4.14 on page 54) reporting the debounce count. The ISENSE#_Range_Fault and ISENSE_RTN_Range_Fault bits in the STATUS_REG4 register (section 13.3.4 on page 48) provide real-time status of these inputs
1	Fault_LVDT2_Float	LVDT3/4 p/n appear to be floating. Check SAR readings
2	Fault_LVDT1_Float	LVDT1/2 p/n appear to be floating. Check SAR readings
3	Fault_DRV_SNS_#2	High if open, short, or over-voltage fault detected in one or both of the DRV_SNS_P2 and DRV_SNS_N2 analog SAR ADC inputs. The DRV_SNS_P2_Fault and DRV_SNS_N2_Fault bits in the STATUS_REG4 register (section 13.3.5 on page 48) provide real-time status of these inputs
4	Fault_DRV_SNS_#1	High if open, short, or over-voltage fault detected in one or both of the DRV_SNS_P1 and DRV_SNS_N1 analog SAR ADC inputs. The DRV_SNS_P1_Fault and DRV_SNS_N1_Fault bits in the STATUS_REG4 register (section 13.3.5 on page 48) provide real-time status of these inputs
5	Fault_HV	High if open, short, or over-voltage fault detected in one or both of the HV1 and HV2 analog SAR ADC inputs. The HV1_Fault and HV2_Fault bits in the STATUS_REG4 register (section 13.3.5 on page 48) provide real-time status of these inputs
6	Fault_PRS_SRC_OT	High if over-temperature fault detected in one or more of the three 4-20mA power switches, PRS_SRC#. STATUS_REG2 (section 13.3.3 on page 47) provide real-time status of these outputs
7	Fault_TMP_Float	High if open fault detected in one or more of the five temperature sensor interfaces. There is a settling time of $31 / F_{OSC}$ ($1.21\mu s$ for $F_{OSC} = 25.6MHz$) between fault detection and the fault being latched here, with the GLITCH_REGD register (section 13.4.13 on page 54) reporting the debounce count. The TMP_#_Fault bits in the STATUS_REG4 register (section 13.3.5 on page 48) provide real-time status of these inputs
8	Fault_DRV2_OT	High if excessive power switch dissipation detected in the DRV_P2 and/or DRV_N2 LVDT half-bridge output. The DRV_P2_OT and DRV_N2_OT bits in the STATUS_REG2 register (section 13.3.3 on page 48) provide real-time status of these over-temperature detectors
9	Fault_DRV1_OT	High if excessive power switch dissipation detected in the DRV_P1 and/or DRV_N1 LVDT half-bridge output. The DRV_P1_OT and DRV_N1_OT bits in the STATUS_REG2 register (section 13.3.3 on page 48) provide real-time status of these over-temperature detectors
10	Fault_DRV2_OC	High if excessive output current detected in the DRV_P2 and/or DRV_N2 LVDT half-bridge output. There is a settling time of $31 \times 1024 / F_{OSC}$ ($1.24ms$ for $F_{OSC} = 25.6MHz$) between fault detection and the fault being latched here, with the GLITCH_REG7 register (section 13.4.7 on page 52) reporting the debounce count. The DRV_P2_OC and DRV_N2_OC bits in the STATUS_REG2 register (section 13.3.3 on page 48) provide real-time status of these over-current detectors
11	Fault_DRV1_OC	High if excessive output current detected in the DRV_P1 and/or DRV_N1 LVDT half-bridge output. There is a settling time of $31 \times 1024 / F_{OSC}$ ($1.24ms$ for $F_{OSC} = 25.6MHz$) between fault detection and the fault being latched here, with the GLITCH_REG6 register (section 13.4.6 on page 52) reporting the debounce count. The DRV_P1_OC and DRV_N1_OC bits in the STATUS_REG2 register (section 13.3.3 on page 48) provide real-time status of these over-current detectors
12	PLL_Unlocked	High if the PLL has gone out of lock since this bit was last cleared. The PLL_LOCK bit in the STATUS_REG0 register (section 13.3.1 on page 46) provides real-time PLL lock status
13	Fault_VCC_UV	The Spike_VCC_UV bit is latched high when a transient under-voltage fault detected on the VCC supply pin 144. If the VCC under-voltage fault remains longer than a settling time of $31 \times 1024 / F_{OSC}$ ($1.24ms$ for $F_{OSC} = 25.6MHz$), then the Fault_VCC_UV is latched high also. The VCC_UV bit in the STATUS_REG0 register (section 13.3.1 on page 46) provides real-time status of this voltage detector
14	Spike_VCC_UV	
15	Fault_OT	High if over-temperature fault detected in one or more of the four internal linear regulators (+5.25V, +5V, +1.5VD, +1.5VA) or the buck pass transistor. There is a settling time of $31 \times 8 / F_{OSC}$ ($9.7\mu s$ for $F_{OSC} = 25.6MHz$) between fault detection and the fault being latched here, with the GLITCH_REGF register (section 0 on page 55) reporting the debounce count. The +5V_+5.25_OT, +1.5VD_LDO_OT, +1.5VA_LDO_OT, and BUCK_OT bits in the STATUS_REG4 register (section 13.3.5 on page 48) provide real-time status of these over-temperature detectors. Regulators cut off when over-temperature is detected, and restart when the temperature has dropped to a safe level

13.5.11 FAULT_CLEAR3 REGISTER 0x107

Faults alerted in fault status register FAULT_STATUS3 can be cleared by clearing the same bit position in fault reset register FAULT_CLEAR3, after the fault has been cleared.

Most of these faults cause the FAULT pin 103 to go high and the $\overline{\text{FAULT}}$ pin 102 to go low to signal the fault. Some faults only affect the FAULT and $\overline{\text{FAULT}}$ pins if their fault mask register bits in FAULT_MASK3 are clear to select Safe Mode on fault. These faults are identified by a Yes in the "FAULT masked?" column below. For these faults, if the corresponding bit in fault mask FAULT_MASK3 is set, then this fault will not cause the FAULT pin to go high and the $\overline{\text{FAULT}}$ pin to go low to signal the fault, as well as not initiate Safe Mode

Bit	Name	Description
0	Fault_ISENSE_Range	Set this bit to clear the Fault_ISENSE_Range bit in the FAULT_STATUS3 register
1	Fault_LVDT2_Float	Set this bit to clear the Fault_LVDT2_Float bit in the FAULT_STATUS3 register
2	Fault_LVDT1_Float	Set this bit to clear the Fault_LVDT1_Float bit in the FAULT_STATUS3 register
3	Fault_DRV_SNS_#2	Set this bit to clear the Fault_DRV_SNS_#2 bit in the FAULT_STATUS3 register
4	Fault_DRV_SNS_#1	Set this bit to clear the Fault_DRV_SNS_#1 bit in the FAULT_STATUS3 register
5	Fault_HV	Set this bit to clear the Fault_HV bit in the FAULT_STATUS3 register
6	Fault_PRS_SRC_OT	Set this bit to clear the Fault_PRS_SRC_OT bit in the FAULT_STATUS3 register
7	Fault_TMP_Float	Set this bit to clear the Fault_TMP_Float bit in the FAULT_STATUS3 register
8	Fault_DRV2_OT	Set this bit to clear the Fault_DRV2_OT bit in the FAULT_STATUS3 register
9	Fault_DRV1_OT	Set this bit to clear the Fault_DRV1_OT bit in the FAULT_STATUS3 register
10	Fault_DRV2_OC	Set this bit to clear the Fault_DRV2_OC bit in the FAULT_STATUS3 register
11	Fault_DRV1_OC	Set this bit to clear the Fault_DRV1_OC bit in the FAULT_STATUS3 register
12	PLL_Unlocked	Set this bit to clear the PLL_Unlocked bit in the FAULT_STATUS3 register
13	Fault_VCC_UV	Set this bit to clear the Fault_VCC_UV bit in the FAULT_STATUS3 register
14	Spike_VCC_UV	Set this bit to clear the Spike_VCC_UV bit in the FAULT_STATUS3 register
15	Fault_OT	Set this bit to clear the Fault_OT bit in the FAULT_STATUS3 register

13.5.12 FAULT_MASK3 REGISTER 0x10B

Faults alerted in fault status register FAULT_STATUS3 are maskable by the same bit position in fault mask register FAULT_MASK3 as to whether they cause the LX4580 to initiate Safe Mode if the fault occurs. Faults are always indicated by a bit set in the FAULT_STATUS3 register regardless of the FAULT_MASK3 setting.

Bit	Name	Safe Value	Description
0	Fault_ISENSE_Range	0	Bit = 0: On fault, FAULT → high, $\overline{\text{FAULT}}$ → low, LX4580 enters Safe Mode Bit = 1: On fault, FAULT and $\overline{\text{FAULT}}$ are unchanged, LX4580 does not enter Safe Mode
1	Fault_LVDT2_Float	0	
2	Fault_LVDT1_Float	0	
3	Fault_DRV_SNS_#2	0	
4	Fault_DRV_SNS_#1	0	
5	Fault_HV	0	Bit = 0: On fault, FAULT → high, $\overline{\text{FAULT}}$ → low, LX4580 enters Safe Mode Bit = 1: On fault, FAULT → high, $\overline{\text{FAULT}}$ → low, LX4580 does not enter Safe Mode
6	Fault_PRS_SRC_OT	0	
7	Fault_TMP_Float	0	Bit = 0: On fault, FAULT → high, $\overline{\text{FAULT}}$ → low, LX4580 enters Safe Mode Bit = 1: On fault, FAULT and $\overline{\text{FAULT}}$ are unchanged, LX4580 does not enter Safe Mode
8	Fault_DRV2_OT	0	
9	Fault_DRV1_OT	0	Bit = 0: On fault, FAULT → high, $\overline{\text{FAULT}}$ → low, LX4580 enters Safe Mode Bit = 1: On fault, FAULT → high, $\overline{\text{FAULT}}$ → low, LX4580 does not enter Safe Mode
10	Fault_DRV2_OC	0	
11	Fault_DRV1_OC	0	
12	PLL_Unlocked	0	
13	Fault_VCC_UV	0	
14	Spike_VCC_UV	0	
15	Fault_OT	0	

13.5.13 CRITICAL_STATUS REGISTER 0x10B AND CRITICAL_CLEAR REGISTER 0x10C

Faults alerted in the CRITICAL_STATUS register are deemed critical faults, and cause the LX4580 to shut down and restart, in an attempt to clear the unsafe condition. All registers except CRITICAL_STATUS lose their data, and both the FAULT pin 103 and the FAULT pin 102 go low to signal a critical fault.

The serial busses are also disabled during critical fault, and the external system must determine and correct the fault(s) before the LX4580 can be accessed. The LX4580 will indicate recovery by taking the FAULT pin high. The CRITICAL_STATUS register can then be read to check which critical faults were latched.

Faults alerted in the CRITICAL_STATUS register are reset by clearing the same bit position in the write-only CRITICAL_CLEAR register.

Bit	Name	Description
0	vdd_OV	VDD I/O supply voltage is high
1	vdd_UV	VDD I/O supply voltage is too low
2	-	
3	Fosc_Fault	Watchdog has detected that the 20MHz to 30MHz clock input is either too slow or stuck
4	+1.5VD_OV_Fault	1.5VD digital core supply voltage is too high
5	+1.5VD_UV_Fault	1.5VD digital core supply voltage is too low
6 - 15	-	Unimplemented bits which read back as 0

13.5.14 SAFE_FORCE REGISTER 0x10E

Writing 0xC3 to the SAFE_FORCE register forces the LX4580 into safe mode (section 12.4 on page 42), tri-stating all outputs except the serial and JTAG interfaces. Writing another value to SAFE_FORCE or taking the RESET input pin high clears the register to exit forced safe mode.

Address	Action	R/W	Register Contents															
			D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0x10E	Safe_Force	R/W	-	-	-	-	-	-	-	-	1	1	0	0	0	0	1	1
	Normal operation		-	-	-	-	-	-	-	-	Any value but 0xC3							

13.5.15 SAFE_STATUS REGISTER 0x10F

The read-only SAFE_STATUS register provides safe mode status.

Bit	Name	Description
0	Safe_Mode	High indicates that the LX4580 is in safe mode
1 - 15	-	Unimplemented bits which read back as 0

13.6 Control Registers

Address	Name	R/W	Register Contents															
			D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0x400	CONTROL_REG0	R/W	-	-	-	-	-	-	TMP#_Pt_Type				ISENSE#_Pullup_Enable					
0x401	CONTROL_REG1	R/W	-	-	-	LVDT, HV1, HV2, and ISENSE test enables												
0x402	CONTROL_REG2	R/W	CLKOUT_Disable and SPI_Polarity															
0x403	CONTROL_REG3	R/W	Factory test															
0x404	CONTROL_REG4	R/W	Factory test															

13.6.1 CONTROL_REG0 REGISTER 0x400

The five ISENSE#_Pullup_Enable bits enable test currents to check whether the selected current sense input has a low impedance connection or is floating. An additional 1mA current source is also enabled on the ISENSE_RTN input whenever any of the ISENSE#_Pullup_Enable bits is set high, since the ISENSEx inputs are differential with respect to ISENSE_RTN. ISENSE faults are indicated in STATUS_REG3 register (section 13.3.4 on page 48).

The five TMP#_Pt_Type bits configure the five temperature sensing analog front ends individually to suit either Pt100 or Pt1000 type temperature sensors, as discussed in section 11.18 on page 41.

Bits	Name	Safe Value	Description
0	ISENSE1_Pullup_Enable	0	High enables a 1mA current source to test whether the ISENSE1 input has a low impedance connection or is floating
1	ISENSE2_Pullup_Enable	0	High enables a 1mA current source to test whether the ISENSE2 input has a low impedance connection or is floating
2	ISENSE3_Pullup_Enable	0	High enables a 1mA current source to test whether the ISENSE3 input has a low impedance connection or is floating
3	ISENSE4_Pullup_Enable	0	High enables a 1mA current source to test whether the ISENSE4 input has a low impedance connection or is floating
4	ISENSE5_Pullup_Enable	0	High enables a 1mA current source to test whether the ISENSE5 input has a low impedance connection or is floating
5	TMP1_Pt_Type	0	Low selects Pt100 temperature sensor type for TMP1 temperature input High selects Pt1000 temperature sensor type for TMP1 temperature input
6	TMP2_Pt_Type	0	Low selects Pt100 temperature sensor type for TMP2 temperature input High selects Pt1000 temperature sensor type for TMP2 temperature input
7	TMP3_Pt_Type	0	Low selects Pt100 temperature sensor type for TMP3 temperature input High selects Pt1000 temperature sensor type for TMP3 temperature input
8	TMP4_Pt_Type	0	Low selects Pt100 temperature sensor type for TMP4 temperature input High selects Pt1000 temperature sensor type for TMP4 temperature input
9	TMP5_Pt_Type	0	Low selects Pt100 temperature sensor type for TMP5 temperature input High selects Pt1000 temperature sensor type for TMP5 temperature input
10 - 15	-		Unimplemented bits which read back as 0

13.6.2 CONTROL_REG1 REGISTER 0x401 (LVDT, HV1, HV2, AND ISENSE TEST ENABLES)

Only enable one of the three HV1 and HV2 input fault tests HV_Float_Det_En, HV_ShortGND_Det_En, and HV_OV_Det_En at a time.

Bits	Name	Safe Value	Description
0	LVDT12_Float_Det_En	0	High enables a 5µA current source to each of the LVDT_P1, LVDT_N1, LVDT_P2, and LVDT_N2 inputs to test whether an input is floating
1	LVDT34_Float_Det_En	0	High enables a 5µA current source to each of the LVDT_P3, LVDT_N3, LVDT_P4, and LVDT_N4 inputs to test whether an input is floating
2	DRV_SNS1_Float_Det_En	0	High enables a 5µA current source to each of the DRV_SNS_P1 and DRV_SNS_N1 inputs to test for floating inputs
3	DRV_SNS2_Float_Det_En	0	High enables a 5µA current source to each of the DRV_SNS_P2 and DRV_SNS_N2 inputs to test for floating inputs
4	DRV_SNS1_ShortGND_Det_En	0	High enables a 425µA current source to each of the DRV_SNS_P1 and DRV_SNS_N1 inputs to test whether the inputs are shorted to GND
5	DRV_SNS2_ShortGND_Det_En	0	High enables a 425µA current source to each of the DRV_SNS_P2 and DRV_SNS_N2 inputs to test whether the inputs are shorted to GND
6	HV_Float_Det_En	0	High enables 5µA current sources to each of the HV1 and HV2 inputs to test whether the inputs are floating
7	HV_ShortGND_Det_En	0	High enables 400µA current sources to each of the HV1 and HV2 inputs to test whether the inputs are shorted to GND
8	DRV_SNS1_OV_Det_En	0	High tests whether either of the DRV_SNS_P1 and DRV_SNS_N1 inputs is over-range by detecting inputs greater than 1.4V
9	DRV_SNS2_OV_Det_En	0	High tests whether either of the DRV_SNS_P2 and DRV_SNS_N2 inputs is over-range by detecting inputs greater than 1.4V
10	HV_OV_Det_En	0	High tests whether either of the HV1 and HV2 inputs is over-range by detecting inputs greater than 1.4V
11	LVDT_Mods_BIST_En	0	Factory test mode. Always write 0 to this bit
12	ISENSE_Mods_BIST_En	0	Factory test mode. Always write 0 to this bit
13 - 15	-	-	Unimplemented bits which read back as 0

13.6.3 CONTROL_REG2 REGISTER 0x402

The operation of CONTROL_REG2 is different to the other CONTROL_REG registers. It is a 16-bit read-write register with bits that default to 0 on power-up and after a reset. Only bits 2 and bit 9 serve user functions. Only write 0 to bits 0, 1, 3, 14, and 15. The remaining 9 bits (4 to 8, 10 to 13) can be used as general purpose read-write bits by the system.

Bits	Name	Safe Value	Description
0 - 1		0	Factory test bits. Do not write anything but 0 to these two bits
2	CLKOUT_Disable	0	Low enables CLKOUT pin 84 High disables CLKOUT pin 84
3		0	Factory test bit. Do not write anything but 0 to this bit
4 - 8	-	-	Implemented bits which are unused internally
9	SPI_Polarity	0	Low selects active low SS1 and SS2 device select inputs in SPI mode High selects active high SS1 and SS2 device select inputs in SPI mode
10 - 13	-	-	Implemented bits which are unused internally
14 - 15		0	Factory test bits. Do not write anything but 0 to these two bits

13.6.4 CONTROL_REG3 REGISTER 0x403

This register is used for factory test purposes. Do not write anything but 0x0000 to this register.

13.6.5 CONTROL_REG4 REGISTER 0x404

This register is used for factory test purposes. Do not write anything but 0x0000 to this register.

13.7 Clock Generator Registers

The CLKGEN_REG0, CLKGEN_REG2, CLKGEN_REG3 and CLKGEN_REG4 registers are normally configured as part of the post power-up register configuration, before any of the ISENSEx analog inputs are enabled using the CLKGEN_REG1 register. A fault will be issued if one of these 4 registers is modified while any of the ISENSEx analog inputs are enabled, or if the ISENSEx analog inputs have just been disabled but an ongoing ISENSEx acquisition sequence hasn't completed.

Address	Name	R/W	Register Contents															
			D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0x210	CLKGEN_REG0	R/W	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	PLL_EN
0x211	CLKGEN_REG1	R/W	-	-	-	-	-	-	-	-	LVDT and ISENSE Enables							
0x212	CLKGEN_REG2	R/W	-	-	-	-	-	-	-	-	ISENSE_CLK_CFG							
0x213	CLKGEN_REG3	R/W	-	-	LVDT12_CLK_CFG													
0x214	CLKGEN_REG4	R/W	-	-	LVDT34_CLK_CFG													

13.7.1 CLKGEN_REG0 REGISTER 0x210 (PLL ENABLE)

Bits	Name	Safe Value	Description
0	PLL_EN	0	When low, uses the frequency F_{OSC} at the OSC1 and OSC2 pins as the PWM clock. When high, uses the output of the internal PLL, F_{PLL} , as the PWM clock. $F_{PLL} = 4 \times F_{OSC}$ when the PLL is in lock
1 - 15	-	-	Unimplemented bits which read back as 0 which read back as 0

13.7.2 CLKGEN_REG1 REGISTER 0x211 (ISENSE AND LVDT DRIVERS ENABLE)

Configure the CLKGEN_REG0, CLKGEN_REG2, CLKGEN_REG3 and CLKGEN_REG4 registers before enabling any of the ISENSEx analog inputs.

Bits	Name	Safe Value	Description
0	ISENSE1_EN	0	When high, enables the ISENSE1 analog input at pin 60
1	ISENSE2_EN	0	When high, enables the ISENSE2 analog input at pin 61
2	ISENSE3_EN	0	When high, enables the ISENSE3 analog input at pin 62
3	ISENSE4_EN	0	When high, enables the ISENSE4 analog input at pin 63
4	ISENSE5_EN	0	When high, enables the ISENSE5 analog input at pin 64
5	DRV_1_EN	0	When high, enables the LVDT DRV_P1 and DRV_N1 outputs at pins 70 and 71 and initiates LVDT 1's drive waveform synthesis configured by the LVDT_Drive registers in section 13.8 on page 70 with soft start (ramp-up). When low, ramps down LVDT 1's drive waveform and then disables the driver
6	DRV_2_EN	0	When high, enables the LVDT DRV_P2 and DRV_N2 outputs at pins 74 and 75 and initiates LVDT 2's drive waveform synthesis configured by the LVDT_Drive registers in section 13.8 on page 70 with soft start (ramp-up). When low, ramps down LVDT 2's drive waveform and then disables the driver
7	CLK_AZ_ISENS_EN	0	When high, enables the auto-zero clock for the ISENSEx analog inputs
8 - 15	-	-	Unimplemented bits which read back as 0

13.7.3 CLKGEN_REG2 REGISTER 0x212 (ISENSE CLOCKS AND PWM PERIOD)

Ensure that $(4 * 2^{\text{ISENSE_SINC_DIV}}) * (8 * \text{ISENSE_DE_DIV}) * (\text{SAR_PWM_MULT} + 1) < 2^{14}$ (16384) otherwise the PWM counters in the SAR ADC will overflow and issue a fault.

Bits	Name	Safe Value	Description
0 - 1	ISENSE_DE_DIV	0	Divides the 20 - 30MHz F _{osc} clock by 8, 16, 24, or 32 for values 0 to 3
2 - 4	ISENSE_SINC_DIV	0	Divides the ISENSE_DE_DIV output by $4 * 2^2$, $4 * 2^3$, $4 * 2^4$, $4 * 2^5$, $4 * 2^6$, or $4 * 2^7$ for values 2 to 7
5 - 7	SAR_PWM_MULT	0	PWM period = ISENSE decimation period * (SAR_PWM_MULT + 1)
8 - 15	-	-	Unimplemented bits which read back as 0

13.7.4 CLKGEN_REG3 REGISTER 0x213 (LVDT1 CLOCKS)

Bits	Name	Safe Value	Description
0 - 4	LVDT12_DE_DIV	0	Divides the 20 - 30MHz F _{osc} clock by 8 to 32 for values 7 to 31. A fault will be issued when any of the ISENSE _{Ex} analog inputs are enabled (CLKGEN_REG1) if the value here is in the range 0 to 7 at the time
5 - 12	LVDT12_SINC_DIV	0	Divides the LVDT12_DE_DIV output by 8 to 256 for values 7 to 255. A fault will be issued when any of the ISENSE _{Ex} analog inputs are enabled (CLKGEN_REG1) if the value here is in the range 0 to 7 at the time
13	LVDT12_OSR_DIV	0	When low, divides the LVDT12_SINC_DIV output by 4 When high, divides the LVDT12_SINC_DIV output by 8
14 - 15	-	-	Unimplemented bits which read back as 0

13.7.5 CLKGEN_REG4 REGISTER 0x214 (LVDT2 CLOCKS)

Bits	Name	Safe Value	Description
0 - 4	LVDT34_DE_DIV	0	Divides the 20 - 30MHz F _{osc} clock by 8 to 32 for values 7 to 31. A fault will be issued when any of the ISENSE _{Ex} analog inputs are enabled (CLKGEN_REG1) if the value here is in the range 0 to 7 at the time
5 - 12	LVDT34_SINC_DIV	0	Divides the LVDT34_DE_DIV output by 8 to 256 for values 7 to 255. A fault will be issued when any of the ISENSE _{Ex} analog inputs are enabled (CLKGEN_REG1) if the value here is in the range 0 to 7 at the time
13	LVDT34_OSR_DIV	0	When low, divides the LVDT34_SINC_DIV output by 4 When high, divides the LVDT34_SINC_DIV output by 8
14 - 15	-	-	Unimplemented bits which read back as 0

13.8 LVDT_Drive Registers

The 0xBxx registers manage the DRV_P1 and DRV_N1 PWM drive waveform for LVDT1's primary. The 0xCxx registers configure the DRV_P2 and DRV_N3 PWM drive waveform for LVDT2's primary. Zero duty corresponds to waveform minimum, 50% duty to the zero crossing, and 100% duty to maximum in the duty cycle look-up tables.

The LVDT#_Period and LVDT#_Frame registers must be configured when all of the 5 ISENSE current sense inputs are disabled, by clearing the 5 ISENSE#_EN bits in the CLKGEN_REG1 register (section 13.7.2 on page 68). If any of these bits is set when either of the LVDT#_Period or LVDT#_Frame registers is written, then the appropriate LVDT#_Fault will be asserted in the FAULT_STATUS2 register (section 13.5.7 on page 61).

An LVDT is enabled, after configuring these registers, by setting the DRV_#_EN bit in the CLKGEN_REG1 register (section 13.7.2 on page 68). No further system interaction is needed for the primary waveform management. The LVDT architecture is discussed in section 11.21 on page 37.

Address	Name	R/W	Register Contents															
			D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0xB00	LVDT1_Duty0	R/W	-	-	-	-	-	-	Duty cycle look-up table (number of F _{PLL} = 4 x F _{OSC} clocks for the on-time for one frame)									
to		R/W	-	-	-	-	-	-										
0xB7F	LVDT1_Duty7F	R/W	-	-	-	-	-	-										
0xB80	LVDT1_Period	R/W	-	-	-	-	-	-	-	PWM Period (32 to 256 F _{OSC} clocks)								
0xB81	LVDT1_Frame	R/W	-	-	-	-	-	-	-	Frame Size (8 to 128 duty look-up table values)								
0xB82	LVDT1_Offset	R/W	-	-	-	-	-	-	-					Offset				
0xB83	LVDT1_F_Count	R	-	-	-	-	-	-	-		Frame Counter							
0xB84	LVDT1_Ramp	R/W	-	-	-	-	-	-	-						Duty ramp rate			
0xB85	LVDT1_Limit	R	-	-	-	-	-	-	Duty limit (0 to {PWM period} x 4)									

Address	Name	R/W	Register Contents															
			D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0xC00	LVDT2_Duty0	R/W	-	-	-	-	-	-	Duty cycle look-up table (number of $F_{PLL} = 4 \times F_{OSC}$ clocks for the on-time for one frame)									
to		R/W	-	-	-	-	-	-										
0xC7F	LVDT2_Duty7F	R/W	-	-	-	-	-	-										
0xC80	LVDT2_Period	R/W	-	-	-	-	-	-	-	PWM Period (32 to 256 F_{OSC} clocks)								
0xC81	LVDT2_Frame	R/W	-	-	-	-	-	-	-		Frame Size (8 to 128 duty look-up table values)							
0xC82	LVDT2_Offset	R/W	-	-	-	-	-	-	-					Offset				
0xC83	LVDT2_F_Count	R	-	-	-	-	-	-	-		Frame counter							
0xC84	LVDT2_Ramp	R/W	-	-	-	-	-	-	-					Duty ramp rate				
0xC85	LVDT2_Limit	R	-	-	-	-	-	-	Duty limit (0 to {PWM period} x 4)									

13.9 Configuration of SAR Registers

Address	Name	R/W	Register Contents																
			D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
0x801	SAR_REG1	R/W	-	-	0	0	0	0					PWM_Per_Loop				PWM_CFGS		
0x802	SAR_REG2	R/W	-	-	-	-	-	-	-	-	PWM_OE1 to PWM_OE8								
0x803	SAR_REG3	R/W	-	-	-	-	-	-	-	-	-	-	-	-	-	CLKDIV			
0x804	SAR_REG4	R/W	SNS1																
0x805	SAR_REG5	R/W	SNS2																
0x806	SAR_REG6	R/W	-	-	-	-	-	-	-	-	PWM_CENTERED								
0x807	SAR_REG7	R/W	-	-	-	-	-	-	-	-	PWM_HI								
0x808	SAR_REG8	R	0	0	0	0	STATUS1												
0x809	SAR_REG9	R	0	0	0	0	0	0	STATUS2										
0x80A	SAR_REGA	R/W	-	-	-	-	-	-	-	-	-	-	-	-	-	PRS#_SNS_EN			
0x80B	SAR_REGB	R/W	-	-	-	-	-	-	DIE_TEMP_REG										
0x810	SAR_REG10	R/W	PWM_X_DELAY																
...	to																		
0x817	SAR_REG17																		
0x818	SAR_REG18	R/W	PWM_X_DUTY																
...	to																		
0x81F	SAR_REG1F																		
0x820	SAR_REG20	R/W	SAR1_TARGETS																
...	to																		
0x837	SAR_REG37																		
0x840	SAR_REG40	R/W	SAR2_TARGETS																
...	to																		
0x857	SAR_REG57																		
0x860	SAR_REG60	R	0	0	0	0	0	0	SAR1_RESULTS alternating with SAR2_RESULTS										
...	to		0	0	0	0	0	0											
0x89F	SAR_REG9F		0	0	0	0	0	0											

13.9.1 SAR_REG1 REGISTER 0x801

Configures SAR periods

Note: fault condition if changed while SAR engine is running (ISENSE1-5 on (CLKGEN_REG1[4:0]) or not burst_finish (SAR_REG9[0]))

A fault will be issued if one of these 4 registers is modified while any of the ISENSEx analog inputs are enabled, or if the ISENSEx analog inputs have just been disabled but an ongoing ISENSEx acquisition sequence hasn't completed.

Bits	Name	Safe Value	Description
0 - 2	PWM_CFGS	0	Number of different PWM configurations for the SAR (PWM_CFGS) - 1. Valid logical values are 2,3,4, and 8. Set the register to 1,2,3,7 to get these logical values
3 - 6	PWM_Per_Loop	0	Number of PWM before SAR engine loops (Pwm_Per_Loop) - 1. Valid values are 2-16, (set Reg to 1-15), but Reg must >= PWM_CFGS
7	Burst_Frequency	0	== 1, 4 burst per PWM. == 0, 2 burst per PWM
9 - 8	Burst_Number	0	Set to # of SAR reads per burst -2, valid settings are 2-5 reads per burst, set this REG to 0-3
10 - 13	reserved		Changes sense timing, for debug only
14 - 15	-	-	Unimplemented bits which read back as 0

13.9.2 SAR_REG2 REGISTER 0x802

SAR_REG2 provides independent output enables for the 8 PWM logic outputs PWM1 (pin 85) to PWM8 (pin 92). Set the appropriate PWM_OE bit high to enable a PWM output. Clear the appropriate PWM_OE bit low to tri-state a PWM output.

When the LX4580 is in safe mode, SAR_REG2 is cleared thus tri-stating all PWM outputs. Safe mode is entered automatically when a critical fault is detected (section 0 on page 65), but can also be asserted by writing 0xC3 to SAFE_FORCE (section 13.5.14 on page 65).

Bits	Name	Safe Value	Description
0	PWM_OE1	0	Set bit to enable PWM1 output (pin 85). Clear bit to tri-state PWM1 output
1	PWM_OE2	0	Set bit to enable PWM2 output (pin 86). Clear bit to tri-state PWM2 output
2	PWM_OE3	0	Set bit to enable PWM3 output (pin 87). Clear bit to tri-state PWM3 output
3	PWM_OE4	0	Set bit to enable PWM4 output (pin 88). Clear bit to tri-state PWM4 output
4	PWM_OE5	0	Set bit to enable PWM5 output (pin 89). Clear bit to tri-state PWM5 output
5	PWM_OE6	0	Set bit to enable PWM6 output (pin 90). Clear bit to tri-state PWM6 output
6	PWM_OE7	0	Set bit to enable PWM7 output (pin 91). Clear bit to tri-state PWM7 output
7	PWM_OE8	0	Set bit to enable PWM8 output (pin 92). Clear bit to tri-state PWM8 output
8 - 15	-	-	Unimplemented bits which read back as 0

13.9.3 SAR_REG3 REGISTER 0x803

Defines SAR CLKDIV period as function of system clock cycles.

Period of CLK_SAR = $1/\{1'b1, CLKDIV\} + 1$

Valid values for clock division are 9-16 (set CLKDIV Reg to 0-7), works with 20-30MHz clock to give 2 MHz or slower clock.

Note: fault condition if changed while SAR engine is running (ISENSE1-5 on (CLKGEN_REG1[4:0]) or not Burst_Finish (SAR_REG9[0])).

Bits	Name	Safe Value	Description
0 - 2	CLKDIV	0	
3 - 15	-	-	Unimplemented bits which read back as 0

13.9.4 SAR_REG4 REGISTER 0x804

Chooses SAR1 target for first read of each burst

Bits	Name	Safe Value	Description
0 - 15	SNS1	0	

13.9.5 SAR_REG5 REGISTER 0x805

Chooses SAR2 target for first read of each burst

Bits	Name	Safe Value	Description
0 - 15	SNS2	0	

13.9.6 SAR_REG6 REGISTER 0x806

Sets whether PWM format is centered or not for PWM 8:1

Note: fault condition if changed while SAR engine is running (ISENSE1-5 on (CLKGEN_REG1[4:0]) or not Burst_Finish (SAR_REG9[0]))

Bits	Name	Safe Value	Description
0 - 7	PWM_Centered	0	
8 - 15	-	-	Unimplemented bits which read back as 0

13.9.7 SAR_REG7 REGISTER 0x807

Sets whether PWM format is high first for PWM 8:1

Note: fault condition if changed while SAR engine is running (ISENSE1-5 on (CLKGEN_REG1[4:0]) or not Burst_Finish (SAR_REG9[0]))

Bits	Name	Safe Value	Description
0 - 7	PWM_Hi	0	
8 - 15	-	-	Unimplemented bits which read back as 0

13.9.8 SAR_REG8 REGISTER 0x808

Status of SAR

Bits	Name	Description
0 - 2	PWM_CFG	Configures state of PWM burst. Valid values are 0-7
3 - 6	PWM_Count	Indicates which PWM frame read target the SAR is engine in. Reflection of PWM_CFGS
7 - 8	PWM_Index	Shows which burst of the PWM frame the engine is in. Reflection of Burst_Frequency
9 - 11	Burst_Index	Shows current burst of the group
12 - 15	-	Unimplemented bits which read back as 0

13.9.9 SAR_REG9 REGISTER 0x809

Detailed status of SAR

Bits	Name	Description
0	Burst_Finish	Checks if SAR is done with the reads and ready for next burst
1	Burst_Start	Start of a new burst (high for one cycle)
2 - 5	CLKDIV_Counter	Counts CLKDIV divider, counts 0-9 up to 0-15, based on CLKDIV register
6 - 9	SAR_Cycle	Counter for SAR clock generation
10 - 15	-	Unimplemented bits which read back as 0

13.9.10 SAR_REGA REGISTER 0x80A

SAR_REGA provides independent enables for the three 4-20mA current loop (pressure sensor) interfaces' power switches, PRS_SRC1 (pin 1), PRS_SRC2 (pin 4), and PRS_SRC3 (pin 3). Disabling a power switch also disables the associated front-end amplifier and so a subsequent 10-bit SAR ADC conversion would return an undefined value.

Bits	Name	Safe Value	Description
0	PRS_SRC1_EN	0	Set bit to enable 4-20mA current loop PRS_SRC1 power switch and AFE
1	PRS_SRC2_EN	0	Set bit to enable 4-20mA current loop PRS_SRC2 power switch and AFE
2	PRS_SRC3_EN	0	Set bit to enable 4-20mA current loop PRS_SRC3 power switch and AFE
3 - 15	-	-	Unimplemented bits which read back as 0

13.9.11 SAR_REGB REGISTER 0x80B

Sets trip point for die temperature fault detection when SAR reads die temperature and results is greater than this register.

Bits	Name	Safe Value	Description
0 - 9	Die_Temp_Reg	0x3FF	
10 - 15	-	-	Unimplemented bits which read back as 0

13.9.12 SAR_REG10 TO SAR_REG17 REGISTERS 0x810 TO 0x817

Delay register for PWM, sets # of cycles to delay PWM format. This count uses 4x the system clock rate

Note: fault condition if changed while SAR engine is running (ISENSE1-5 on (CLKGEN_REG1[4:0]) or not Burst_Finish (SAR_REG9[0]))

Bits	Name	Safe Value	Description
0 - 15	PWM_X_Delay	0	

13.9.13 SAR_REG18 TO SAR_REG1F REGISTERS 0x818 TO 0x81F

Duty (# of cycles) for PWM 8-1. This count uses 4x the system clock rate

Bits	Name	Safe Value	Description
0 - 15	PWM_X_Duty	0	

13.9.14 SAR_REG20 TO SAR_REG37 REGISTERS 0x820 TO 0x837

Chooses analog inputs for 10-bit ADC SAR1 for 2-5th targets of each burst. These are 5 bit registers. Bit 4 of the register is the "Ref" column and bits [3:0] of the register is the mux value.

SAR1 ADC Analog Input	Mux	Ref	SAR1_VREFL_SEL
CM_LVDT1	1	x	1
CM_LVDT2	9	x	1
CM_LVDT3	0	x	1
CM_LVDT4	8	x	1
DIE_TEMP	3	x	1
DRV_SNS_1	7	x	1
DRV_SNS_2	6	x	1
HV_1_SNS	10	x	0
HV_2_SNS	5	x	0
TEMP5_SNS_REF	11	1	1
TEMP5_SNS_Pt	11	0	1
TEMP4_SNS_REF	12	1	1
TEMP4_SNS_Pt	12	0	1
TEMP3_SNS_REF	13	1	1
TEMP3_SNS_Pt	13	0	1
TEMP2_SNS_REF	14	1	1
TEMP2_SNS_Pt	14	0	1
TEMP1_SNS_REF	15	1	1
TEMP1_SNS_Pt	15	0	1
VBG_RED	2	x	1
VCC	4	x	1

13.9.15 SAR_REG40 TO SAR_REG57 REGISTERS 0x840 TO 0x857

Chooses SAR2 targets for 2-5th targets of each burst. These are 5 bit registers. Bit 4 of the register is the “Ref” column and bits [3:0] of the register is the mux value.

SAR2 ADC Analog Input	Mux	Ref	SAR2_VREFL_SEL
LVDT4_CM	0	x	1
LVDT2_CM	1	x	1
PRS_SRC_DROP3	2	x	0
PRS_SRC_DROP2	3	x	0
PRS_SRC_DROP1	4	x	0
HV_2_SNS	5	x	0
DRV_SNS_2	6	x	1
DRV_SNS_1	7	x	1
PRS_SNS3	8	x	1
PRS_SNS2	9	x	1
PRS_SNS1	10	x	1
VBG_RED	11	x	1
VCC	12	x	1
DIE_TEMP	13	x	1
HV_1_SNS	14	x	0
TEMP1_SNS_REF	15	1	1
TEMP1_SNS_PT	15	0	1

13.9.16 SAR_REG60 TO SAR_REG9F REGISTERS 0x860 TO 0x89F

Holds results of SAR1 reads as SAR1_Results and results of SAR2 reads as SAR2_Results in alternating sequence of registers.

SAR1_Results and SAR2_Results are loaded sequentially, in order.

The first SAR1_Result is in SAR_REG60, the first SAR2_Result is in SAR_REG61, the second SAR1_Result is in SAR_REG62, the second SAR2_Result is in SAR_REG63, and so on.

This continues until there are 32 results in registers for SAR1 and SAR2, ending at SAR_REG9F

Note: registers are cleared back to 0 when the ISENSE are disabled (CLKGEN_REG1[4:0] == 0)

13.10 LVDT and ISENSE Σ - Δ ADC Filter Registers

The filter registers configure the processing parameters for both the four Σ - Δ ADC channels dedicated to the two LVDTs' dual secondary winding outputs, and the five Σ - Δ ADC channels dedicated to current sensing.

The two ADC channels dedicated to LVDT1 process the signals at the differential inputs {LVDT_P1, LVDT_N1} and {LVDT_P2, LVDT_N2}. The two ADC channels dedicated to LVDT2 process the signals at the differential inputs {LVDT_P3, LVDT_N3} and {LVDT_P4, LVDT_N4}.

Processing is configured independently (with identical options) for the two LVDTs, allowing:

- Two different instrument types (or an LVDT plus a resolver) to be optimized
- Two identical LVDTs to be operated at different primary drive frequencies, amplitude, or phase to minimize the effects of signal coupling between instruments
- One LVDT to be wired to both drivers and both sets of ADC channels for redundancy
- Both sets of ADC channels synchronized or phased to obtain twice the ADC sampling rate on a single LVDT

The ADC signal processing includes more than the decimation and sinc³ filters associated with Σ - Δ converters to reduce the processing burden on the host system. After an initial sinc³ filter, each bipolar secondary signal (normally with a sine wave envelope) is rectified by conversion from a signed to an unsigned value. Signal path processing options are then:

- Choice of RMS computation, simple average computation, or no computation before the second sinc³ filter
- Choice of IIR filter or static register value for signal DC offset correction

The density of the pulses (proportion of 1s) within each PDM stream corresponds to the analog signal's amplitude. All 7 ADC inputs are bipolar, so continuous 0s indicates negative full scale (or lower), and continuous 1s indicates positive full scale (or higher). A matching density of 0s and 1s indicates zero input.

Decimation factors, table length and clock frequency should be chosen to yield 1 or 2 samples per LVDT driver period.

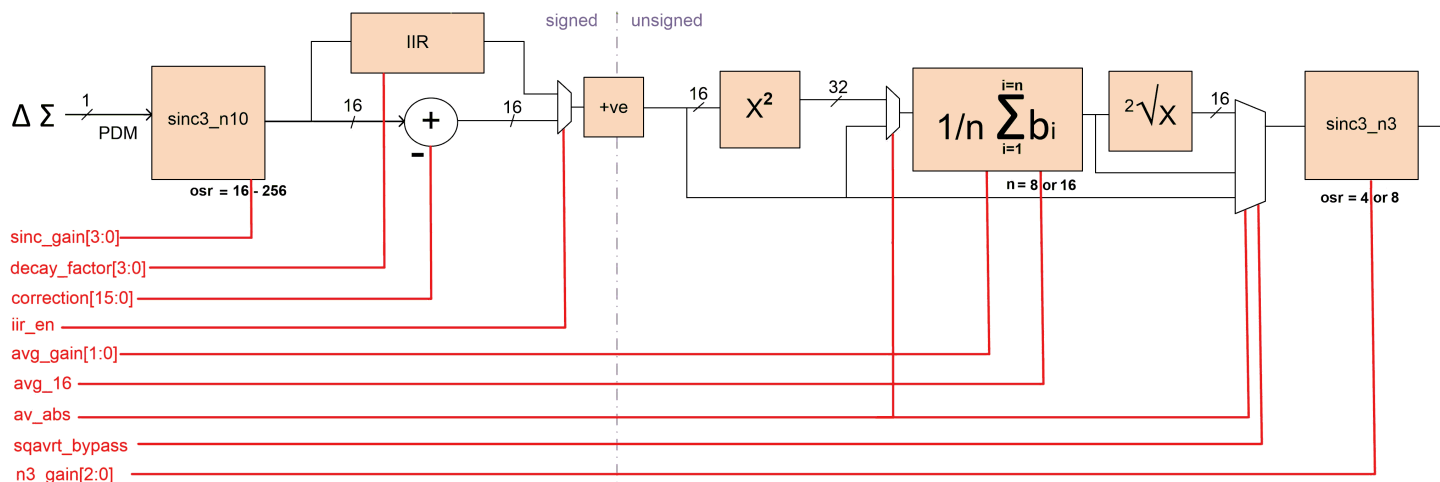


Figure 20. LVDT Secondary Signal Processing Chain

Address	Name	R/W	Register Contents															
			D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0x300	CH12_CFG1	R/W	-	-	-	PW M12 _EN	IIR1 2_E N	AVG 12 _ABS	AVG12_G ain		Sinc12_Gain				Decay12			
0x301	CH12_CFG2	R/W	-	-	-	-	-	-	x	x	x	x	x	AVG 12_ 16	RM S12 _By pass	N312_Gain		
0x302	CH12_COR	R/W	Correction12															
0x308	CH34_CFG1	R/W	-	-	-	PW	IIR3	QV	AVG34_G		Sinc34_Gain				Decay34			

						M_E N	4_E N	G34 _AB S	ain							
0x309	CH34_CFG2	R/W	-	-	-	-	-	-	x	x	x	x	x	AVG 34_ 16	RM S34 _By pass	N334_Gain
0x30A	CH34_COR	R/W	Correction34													
0x310	CH1_SINC	R	CH1_Sinc													
0x311	CH2_SINC	R	CH2_Sinc													
0x312	CH3_SINC	R	CH3_Sinc													
0x313	CH4_SINC	R	CH4_Sinc													
0x314	CH1_IIR	R	CH1_IIR													
0x315	CH2_IIR	R	CH2_IIR													
0x316	CH3_IIR	R	CH3_IIR													
0x317	CH4_IIR	R	CH4_IIR													
0x318	CH1_RMS	R	CH1_RMS													
0x319	CH2_RMS	R	CH2_RMS													
0x31A	CH3_RMS	R	CH3_RMS													
0x31B	CH4_RMS	R	CH4_RMS													
0x31C	CH1_OUT	R	CH1_Out													
0x31D	CH2_OUT	R	CH2_Out													
0x31E	CH3_OUT	R	CH3_Out													
0x31F	CH4_OUT	R	CH4_Out													
0x321	IS1_CFG	R/W	-	-	-	-	-	-	-	ISE NSE 1_P WM _EN	ISENSE1_Sinc_Gain				ISENSE1_Decay	
0x322	IS2_CFG	R/W	-	-	-	-	-	-	-	ISE NSE 2_P WM _EN	ISENSE2_Sinc_Gain				ISENSE2_Decay	
0x323	IS3_CFG	R/W	-	-	-	-	-	-	-	ISE NSE 3_P WM _EN	ISENSE3_Sinc_Gain				ISENSE3_Decay	
0x324	IS4_CFG	R/W	-	-	-	-	-	-	-	ISE NSE 4_P WM _EN	ISENSE4_Sinc_Gain				ISENSE4_Decay	
0x325	IS5_CFG	R/W	-	-	-	-	-	-	-	ISE NSE 5_P WM _EN	ISENSE5_Sinc_Gain				ISENSE5_Decay	
0x331	IS1_SINC	R	ISENSE1_Sinc_Out													
0x332	IS2_SINC	R	ISENSE2_Sinc_Out													
0x333	IS3_SINC	R	ISENSE3_Sinc_Out													
0x334	IS4_SINC	R	ISENSE4_Sinc_Out													
0x335	IS5_SINC	R	ISENSE5_Sinc_Out													
0x336	IS1_IIR	R	ISENSE1_IIR_Out													
0x337	IS2_IIR	R	ISENSE2_IIR_Out													
0x338	IS3_IIR	R	ISENSE3_IIR_Out													
0x339	IS4_IIR	R	ISENSE4_IIR_Out													
0x33A	IS5_IIR	R	ISENSE5_IIR_Out													

13.10.1 FILTER_CH12_CFG1 REGISTER 0x300

Bits	Name	Safe Value	Description
0 - 3	Decay12	10	IIR decay factor (for removing DC offset)
4 - 7	Sinc12_Gain	4	Gain of the Sinc filter OSR = 16 to 256 with steps of 16
8 - 9	AVG12_Gain	2	For high frequency signals this gain can give more definition
10	AVG12_ABS	0	Use absolute value instead of RMS for average function
11	IIR12_En	1	Enable the IIR filter
12	PWM12_En	0	Input to CH1 & CH2 filters are feedback from PWM1 and PWM2 instead of Σ - Δ channels
13 - 15	-	-	Unimplemented bits which read back as 0

13.10.2 FILTER_CH12_CFG2 REGISTER 0x301

Bits	Name	Safe Value	Description
0 - 2	N312_Gain	0	Gain of the sinc ³ filter
3	RMS12_Bypass	0	Use the rectified only signal as input to last sinc filter
4	AVG12_16	1	0: average last 8 samples; 1: averages last 16 samples
5 - 9	unused		Implemented bits which are not used
10 - 15	-	-	Unimplemented bits which read back as 0

13.10.3 FILTER_CH12_COR REGISTER 0x302

Bits	Name	Safe Value	Description
0 - 15	Correction12	0	DC offset correction factor

13.10.4 FILTER_CH1_SINC REGISTER 0x310

Bits	Name	Description
0 - 15	CH1_Sinc	Output from Sinc_N8 stage

13.10.5 FILTER_CH1_IIR REGISTER 0x314

Bits	Name	Description
0 - 15	CH1_IIR	Output from IIR stage

13.10.6 FILTER_CH1_RMS REGISTER 0x318

Bits	Name	Description
0 - 15	CH1_RMS	Output from RMS stage

13.10.7 FILTER_CH1_OUT REGISTER 0x31C

Bits	Name	Description
0 - 15	CH1_Out	Output from stage

13.10.8 FILTER_IS1_CFG REGISTER 0x321

Bits	Name	Safe Value	Description
0 - 3	ISENSE1_Ddecay	0xA	IIR decay factor (for removing DC offset)
4 - 7	ISENSE1_Sinc_Gain	7	Gain of the Sinc_N11 filter
8	ISENSE1_PWM_EN	0	Input to ISENSE is feedback from PWM5 instead of the Σ - Δ channel
9 - 15	-	-	Unimplemented bits which read back as 0

13.10.9 FILTER_IS1_SINC REGISTER 0x331

Bits	Name	Description
0 - 15	ISENSE1_Sinc_Out	Output from Sinc_N11 stage

13.10.10 FILTER_IS1_IIR REGISTER 0x336

Bits	Name	Description
0 - 15	ISENSE1_IIR_Out	Output from IIR stage

13.10.11 FILTER_CH2_SINC REGISTER 0x311

Bits	Name	Description
0 - 15	CH2_Sinc	Output from Sinc_N8 stage

13.10.12 FILTER_CH2_IIR REGISTER 0x315

Bits	Name	Description
0 - 15	CH2_IIR	Output from IIR stage

13.10.13 FILTER_CH2_RMS REGISTER 0x319

Bits	Name	Description
0 - 15	CH2_RMS	Output from RMS stage

13.10.14 FILTER_CH2_OUT REGISTER 0x31D

Bits	Name	Description
0 - 15	CH2_Out	Output from Sinc_N3 stage

13.10.15 FILTER_IS2_CFG REGISTER 0x332

Bits	Name	Safe Value	Description
0 - 3	ISENSE2_Ddecay	0xA	IIR decay factor (for removing DC offset)
4 - 7	ISENSE2_Sinc_Gain	7	Gain of the Sinc_N11 filter
8	ISENSE2_PWM_EN	0	Input to ISENSE is feedback from PWM6 instead of the Σ - Δ channel
9 - 15	-	-	Unimplemented bits which read back as 0

13.10.16 FILTER_IS2_SINC REGISTER 0x332

Bits	Name	Description
0 - 15	ISENSE2_Sinc_Out	Output from Sinc_N11 stage

13.10.17 FILTER_IS2_IIR REGISTER 0x337

Bits	Name	Description
0 - 15	ISENSE2_IIR_Out	Output from IIR stage

13.10.18 FILTER_CH34_CFG1 REGISTER 0x308

Bits	Name	Safe Value	Description
0 - 3	Decay34	10	IIR decay factor (for removing DC offset)
4 - 7	Sinc34_Gain	4	Gain of the sinc ³ filter
8 - 9	AVG34_Gain	2	For high frequency signals this gain can give more definition
10	AVG34_ABS	0	Use absolute value instead of RMS for average function
11	IIR34_EN	1	Enable the IIR filter
12	PWM34_EN	0	Input to CH3 and CH4 filters are feedback from PWM3 and PWM4 instead of the Σ - Δ channels
13 - 15	-	-	Unimplemented bits which read back as 0

13.10.19 FILTER_CH34_CFG2 REGISTER 0x309

Bits	Name	Safe Value	Description
0 - 2	N34_Gain	0	Gain of the sinc ³ Filter
3	RMS34_Bypass	0	Use the rectified only signal as input to last sinc filter
4	AVG34_16	1	0: average last 8 samples; 1: averages last 16 samples
5 - 9	unused		Implemented bits which are not used
10 - 15	-	-	Unimplemented bits which read back as 0

13.10.20 FILTER_CH34_COR REGISTER 0x30A

Bits	Name	Safe Value	Description
0 - 15	Correction34	0	DC offset correction factor

13.10.21 FILTER_CH3_SINC REGISTER 0x312

Bits	Name	Description
0 - 15	CH3_Sinc	Output from Sinc N8 stage

13.10.22 FILTER_CH3_IIR REGISTER 0x316

Bits	Name	Description
0 - 15	CH3_IIR	Output from IIR stage

13.10.23 FILTER_CH3_RMS REGISTER 0x31A

Bits	Name	Description
0 - 15	CH3_RMS	Output from RMS stage

13.10.24 FILTER_CH3_OUT REGISTER 0x31E

Bits	Name	Description
0 - 15	CH3_Out	Output from Sinc_N3 stage

13.10.25 FILTER_IS3_CFG REGISTER 0x323

Bits	Name	Safe Value	Description
0 - 3	ISENSE3_Ddecay	0xA	IIR decay factor (for removing DC offset)
4 - 7	ISENSE3_Sinc_Gain	7	Gain of the Sinc N11 filter
8	ISENSE3_PWM_EN	0	Input to ISENSE is feedback from PWM7 instead of the Σ - Δ channel
9 - 15	-	-	Unimplemented bits which read back as 0

13.10.26 FILTER_IS3_SINC REGISTER 0x333

Bits	Name	Description
0 - 15	ISENSE3_Sinc_Out	Output from Sinc_N11 stage

13.10.27 FILTER_IS3_IIR REGISTER 0x338

Bits	Name	Description
0 - 15	ISENSE3_IIR_Out	Output from IIR stage

13.10.28 FILTER_CH4_SINC REGISTER 0x313

Bits	Name	Description
0 - 15	CH4_Sinc	Output from Sinc_N8 stage

13.10.29 FILTER_CH4_IIR REGISTER 0x317

Bits	Name	Description
0 - 15	CH4_IIR	Output from IIR stage

13.10.30 FILTER_CH4_RMS REGISTER 0x31B

Bits	Name	Description
0 - 15	CH4_RMS	Output from RMS stage

13.10.31 FILTER_CH4_OUT REGISTER 0x31F

Bits	Name	Description
0 - 15	CH4_Out	Output from Sinc_N3 stage

13.10.32 FILTER_IS4_CFG REGISTER 0x324

Bits	Name	Safe Value	Description
0 - 3	ISENSE4_Ddecay	0xA	IIR decay factor (for removing DC offset)
4 - 7	ISENSE4_Sinc_Gain	7	Gain of the Sinc N11 filter
8	ISENSE4_PWM_EN	0	Input to ISENSE is feedback from PWM8 (same option as ISENSE5) instead of the Σ - Δ channel
9 - 15	-	-	Unimplemented bits which read back as 0

13.10.33 FILTER_IS4_SINC REGISTER 0x334

Bits	Name	Description
0 - 15	ISENSE4_Sinc_Out	Output from Sinc_N11 stage

13.10.34 FILTER_IS4_IIR REGISTER 0x339

Bits	Name	Description
0 - 15	ISENSE4_IIR_Out	Output from IIR stage

13.10.35 FILTER_IS5_CFG REGISTER 0x325

Bits	Name	Safe Value	Description
0 - 3	ISENSE5_Ddecay	0xA	IIR decay factor (for removing DC offset)
4 - 7	ISENSE5_Sinc_Gain	7	Gain of the Sinc N11 filter
8	ISENSE5_PWM_EN	0	Input to ISENSE is feedback from PWM8 (same option as ISENSE4) instead of the Σ - Δ channel
9 - 15	-	-	Unimplemented bits which read back as 0

13.10.36 FILTER_IS5_SINC REGISTER 0x335

Bits	Name	Description
0 - 15	ISENSE5_Sinc_Out	Output from Sinc_N11 stage

13.10.37 FILTER_IS5_IIR REGISTER 0x33A

Bits	Name	Description
0 - 15	ISENSE5_IIR_Out	Output from IIR stage

13.11 GPIO Registers

The 9 GPIOs on pins 93 to 101 are configurable as logic inputs, static logic outputs, or as logic outputs for various internal signals (section 11.10 on page 25). To use a GPIO as a logic input, clear the appropriate bit in GPIO_REG3 to tristate the output, and optionally enable its internal 50kΩ pulldown resistor by clearing the appropriate bit in GPIO_REG4. GPIO inputs are read from GPIO_REG5.

To use a GPIO as a logic output, first select the desired output signal from the tables starting in section 13.11.8 on page 85, which provide a 5 bit selection number from b'00000' to b'11111'. Update the 5 bits in the appropriate one of GPIO_REG0 to GPIO_REG2 to make the output selection for that GPIO. Then set the appropriate bit in GPIO_REG3 to enable the GPIO as an output.

The internal signal options are:

- Logic outputs for the HEP1, HEP2, and HEP3 analog comparator inputs (section 11.17 on page 31)
- Over-temperature fault status for the internal linear regulators (section 11.2 on page 21), buck switch (section 11.3 on page 23), 4-20mA current loop driver (section 11.16 on page 30), and LVDT driver (section 11.21.1 on page 37)
- Internal PLL lock status

Shorted (or overloaded) GPIO outputs latch a fault alert in FAULT_STATUS0 (section 13.5.1 on page 57). A short fault is detected when the output is driven to one logic level by the LX4580, but reads back as the opposite logic level.

Address	Name	R/W	Register Contents															
			D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0xA00	GPIO_REG0	R/W	-	GPIO_Mux_Control123														
0xA01	GPIO_REG1	R/W	-	GPIO_Mux_Control456														
0xA02	GPIO_REG2	R/W	-	GPIO_Mux_Control789														
0xA03	GPIO_REG3	R/W	-	-	-	-	-	-	-	GPIO_OE								
0xA04	GPIO_REG4	R/W	-	-	-	-	-	-	-	GPIO_Pulldown								
0xA05	GPIO_REG5	R/W	-	-	-	-	-	-	-	GPIO_Input								
0xA06	GPIO_REG6	R/W	-	-	-	-	-	-	-	GPIO_Output								

13.11.1 GPIO_REG0 REGISTER 0xA00

Bits	Name	Safe Value	Description
0 - 4	GPIO_Mux_Control1	0x00	Selects one of several possible outputs on GPIO1, GPIO2, and GPIO3 when output is enabled. The options are shown in section 13.11.8 on page 85
5 - 9	GPIO_Mux_Control2	0x00	Selects one of 32 possible outputs on GPIO4, GPIO5, and GPIO6 when output is enabled. The options are shown in section 13.11.11 on page 86
10 - 14	GPIO_Mux_Control3	0x00	Selects one of 32 possible outputs on GPIO7, GPIO8, and GPIO9 when output is enabled. The options are shown in section 13.11.14 on page 86
15	-	-	Unimplemented bits which read back as 0

13.11.2 GPIO_REG1 REGISTER 0xA01

Bits	Name	Safe Value	Description
0 - 4	GPIO_Mux_Control4	0x00	Selects one of 32 possible outputs on GPIO4 when output is enabled. The options are shown in section 13.11.11 on page 86
5 - 9	GPIO_Mux_Control5	0x00	Selects one of 32 possible outputs on GPIO5 when output is enabled. The options are shown in section 13.11.12 on page 86
10 - 14	GPIO_Mux_Control6	0x00	Selects one of 32 possible outputs on GPIO6 when output is enabled. The options are shown in section 13.11.13 on page 86
15	-	-	Unimplemented bits which read back as 0

13.11.3 GPIO_REG2 REGISTER 0xA02

Bits	Name	Safe Value	Description
0 - 4	GPIO_Mux_Control7	0x00	Selects one of 32 possible outputs on GPIO7 when output is enabled. The options are shown in section 13.11.14 on page 86
5 - 9	GPIO_Mux_Control8	0x00	Selects one of 32 possible outputs on GPIO8 when output is enabled. The options are shown in section 13.11.15 on page 87
10 - 14	GPIO_Mux_Control9	0x00	Selects one of 32 possible outputs on GPIO9 when output is enabled. The options are shown in section 13.11.16 on page 87
15	-	-	Unimplemented bits which read back as 0

13.11.4 GPIO_REG3 REGISTER 0xA03

All output enables are disabled in safe mode, making all GPIO ports inputs, but GPIO_REG3 values are not changed.

Bits	Name	Safe Value	Description
0	GPIO_OE1	0	Set to 0 to tristate GPIO1 output. GPIO1 can now be used as an input port Set to 1 to enable GPIO1 output when GPIO1 is an output port
1	GPIO_OE2	0	Set to 0 to tristate GPIO2 output. GPIO2 can now be used as an input port Set to 1 to enable GPIO2 output when GPIO2 is an output port
2	GPIO_OE3	0	Set to 0 to tristate GPIO3 output. GPIO3 can now be used as an input port Set to 1 to enable GPIO3 output when GPIO3 is an output port
3	GPIO_OE4	0	Set to 0 to tristate GPIO4 output. GPIO4 can now be used as an input port Set to 1 to enable GPIO4 output when GPIO4 is an output port
4	GPIO_OE5	0	Set to 0 to tristate GPIO5 output. GPIO5 can now be used as an input port Set to 1 to enable GPIO5 output when GPIO5 is an output port
5	GPIO_OE6	0	Set to 0 to tristate GPIO6 output. GPIO6 can now be used as an input port Set to 1 to enable GPIO6 output when GPIO6 is an output port
6	GPIO_OE7	0	Set to 0 to tristate GPIO7 output. GPIO7 can now be used as an input port Set to 1 to enable GPIO7 output when GPIO7 is an output port
7	GPIO_OE8	0	Set to 0 to tristate GPIO8 output. GPIO8 can now be used as an input port Set to 1 to enable GPIO8 output when GPIO8 is an output port
8	GPIO_OE9	0	Set to 0 to tristate GPIO9 output. GPIO9 can now be used as an input port Set to 1 to enable GPIO9 output when GPIO9 is an output port
9 - 15	-	-	Unimplemented bits which read back as 0

13.11.5 GPIO_REG4 REGISTER 0xA04

All pulldown resistors are enabled in safe mode, but GPIO_REG4 values are not changed.

Bits	Name	Safe Value	Description
0	GPIO_Pulldown1	0	Clear to 0 to enable GPIO1 50kΩ pulldown resistor
1	GPIO_Pulldown2	0	Clear to 0 to enable GPIO2 50kΩ pulldown resistor
2	GPIO_Pulldown3	0	Clear to 0 to enable GPIO3 50kΩ pulldown resistor
3	GPIO_Pulldown4	0	Clear to 0 to enable GPIO4 50kΩ pulldown resistor
4	GPIO_Pulldown5	0	Clear to 0 to enable GPIO5 50kΩ pulldown resistor
5	GPIO_Pulldown6	0	Clear to 0 to enable GPIO6 50kΩ pulldown resistor
6	GPIO_Pulldown7	0	Clear to 0 to enable GPIO7 50kΩ pulldown resistor
7	GPIO_Pulldown8	0	Clear to 0 to enable GPIO8 50kΩ pulldown resistor
8	GPIO_Pulldown9	0	Clear to 0 to enable GPIO9 50kΩ pulldown resistor
9 - 15	-	-	Unimplemented bits which read back as 0

13.11.6 GPIO_REG5 REGISTER 0xA05

Bits	Name	Description
0	GPIO_Input1	Read logic input level at GPIO1 pin 93
1	GPIO_Input2	Read logic input level at GPIO2 pin 94
2	GPIO_Input3	Read logic input level at GPIO3 pin 95
3	GPIO_Input4	Read logic input level at GPIO4 pin 96
4	GPIO_Input5	Read logic input level at GPIO5 pin 97
5	GPIO_Input6	Read logic input level at GPIO6 pin 98
6	GPIO_Input7	Read logic input level at GPIO7 pin 99
7	GPIO_Input8	Read logic input level at GPIO8 pin 100
8	GPIO_Input9	Read logic input level at GPIO9 pin 101
9 - 15	-	Unimplemented bits which read back as 0

13.11.7 GPIO_REG6 REGISTER 0xA06

Bits	Name	Description
0	GPIO_Output1	Read back output logic level at GPIO1 pin 93
1	GPIO_Output2	Read back output logic level at GPIO2 pin 94
2	GPIO_Output3	Read back output logic level at GPIO3 pin 95
3	GPIO_Output4	Read back output logic level at GPIO4 pin 96
4	GPIO_Output5	Read back output logic level at GPIO5 pin 97
5	GPIO_Output6	Read back output logic level at GPIO6 pin 98
6	GPIO_Output7	Read back output logic level at GPIO7 pin 99
7	GPIO_Output8	Read back output logic level at GPIO8 pin 100
8	GPIO_Output9	Read back output logic level at GPIO9 pin 101
9 - 15	-	Unimplemented bits which read back as 0

13.11.8 GPIO1 PORT FUNCTION SELECTION

GPIO_REG0 Bits					GPIO1 Function	Description	Register With Same Signal	Page
4	3	2	1	0				
0	1	1	1	1	Logic low output	Static logic low (0) output		
1	0	0	0	0	PRS_SRC2_OT	High if over-temperature fault detected in the 4-20mA power switch PRS_SRC2 pin 4	STATUS_REG2	47
1	1	1	1	1	Logic high output	Static logic high (1) output		

13.11.9 GPIO2 PORT FUNCTION SELECTION

GPIO_REG0 Bits					GPIO2 Function	Description	Register With Same Signal	Page
9	8	7	6	5				
0	0	1	1	0	DRV_N2_OT	High if over-temperature fault detected in the LVDT/resolver half-bridge driver DRV_N2 pin 75	STATUS_REG2	47
0	0	1	1	1	HEP1_Out	Output of the Hall Effect or other sensor at comparator input HEP1 pin 126	STATUS_REG2	47
0	1	1	0	1	Logic low output	Static logic low (0) output		
0	1	1	1	1	PLL_LOCK	High if the PLL is in lock	STATUS_REG0	46
1	1	0	1	1	+5V_+5.25_OT	High if either the +5V LDO or the +5.25V LDO exceeds the T _{LDOs_OT} over-temperature threshold (180°C typ)	STATUS_REG4	48
1	1	1	1	1	Logic high output	Static logic high (1) output		

13.11.10 GPIO3 PORT FUNCTION SELECTION

GPIO_REG0 Bits					GPIO3 Function	Description	Register With Same Signal	Page
E	D	C	B	A				
0	0	1	1	1	HEP2_Out	Output of the Hall Effect or other sensor at comparator input HEP2 pin 125	STATUS_REG2	47
0	1	1	1	1	Logic low output	Static logic low (0) output		
1	1	1	1	1	Logic high output	Static logic high (1) output		

13.11.11 GPIO4 PORT FUNCTION SELECTION

GPIO_REG1 Bits					GPIO4 Function	Description	Register With Same Signal	Page
4	3	2	1	0				
0	0	1	1	0	DRV_P2_OT	High if over-temperature fault detected in the LVDT/resolver half-bridge driver DRV_P2 pin 74	STATUS_REG2	47
0	0	1	1	1	HEP3_Out	Output of the Hall Effect or other sensor at comparator input HEP3 pin 124	STATUS_REG2	47
0	1	1	0	1	Logic low output	Static logic low (0) output		
1	1	0	1	0	+1.5VA_LDO_OT	High if the 1.5VA LDO exceeds the T _{LDOs_OT} over-temperature threshold (180°C typ)	STATUS_REG4	48
1	1	1	1	1	Logic high output	Static logic high (1) output		

13.11.12 GPIO5 PORT FUNCTION SELECTION

GPIO_REG1 Bits					GPIO5 Function	Description	Register With Same Signal	Page
9	8	7	6	5				
0	1	1	0	1	Logic low output	Static logic low (0) output		
1	0	0	0	0	PRS_SRC3_OT	High if over-temperature fault detected in the 4-20mA power switch PRS_SRC3 pin 7	STATUS_REG2	47
1	1	1	1	1	Logic high output	Static logic high (1) output		

13.11.13 GPIO6 PORT FUNCTION SELECTION

GPIO_REG1 Bits					GPIO6 Function	Description	Register With Same Signal	Page
E	D	C	B	A				
0	0	0	1	0	BUCK_OT	High if over-temperature fault detected in the buck regulator	STATUS_REG4	48
0	0	1	0	1	DRV_N1_OT	High if over-temperature fault detected in the LVDT/resolver half-bridge driver DRV_N1 pin 71	STATUS_REG2	47
0	1	1	1	1	PRS_SRC1_OT	High if over-temperature fault detected in the 4-20mA power switch PRS_SRC1 pin 1	STATUS_REG2	47
1	1	1	0	1	Logic low output	Static logic low (0) output		
1	1	1	1	1	Logic high output	Static logic high (1) output		

13.11.14 GPIO7 PORT FUNCTION SELECTION

GPIO_REG2 Bits					GPIO7 Function	Description	Register With Same Signal	Page
4	3	2	1	0				
1	1	0	1	0	+1.5VD_LDO_OT	High if the 1.5VD LDO exceeds the T _{LDOs_OT} over-temperature threshold (180°C typ)	STATUS_REG4	48
1	1	1	0	1	Logic low output	Static logic low (0) output		
1	1	1	1	0	HEP1_Out	Output of the Hall Effect or other sensor at comparator input HEP1 pin 126	STATUS_REG2	47
1	1	1	1	1	Logic high output	Static logic high (1) output		

13.11.15 GPIO8 PORT FUNCTION SELECTION

GPIO_REG2 Bits					GPIO8 Function	Description	Register With Same Signal	Page
9	8	7	6	5				
0	0	1	0	1	DRV_P1_OT	High if over-temperature fault detected in the LVDT/resolver half-bridge driver DRV_P1 pin 70	STATUS_REG2	47
1	1	1	0	1	Logic low output	Static logic low (0) output		
1	1	1	1	0	HEP2_Out	Output of the Hall Effect or other sensor at comparator input HEP2 pin 125	STATUS_REG2	47
1	1	1	1	1	Logic high output	Static logic high (1) output		

13.11.16 GPIO9 PORT FUNCTION SELECTION

GPIO_REG2 Bits					GPIO9 Function	Description	Register With Same Signal	Page
E	D	C	B	A				
1	1	1	0	1	Logic low output	Static logic low (0) output		
1	1	1	1	0	HEP3_Out	Output of the Hall Effect or other sensor at comparator input HEP3 pin 124	STATUS_REG2	47
1	1	1	1	1	Logic high output	Static logic high (1) output		

13.12 Trim Registers

The trim registers are shadow registers which are written with factory trim values stored in OTP on reset and power-up. Registers TRIM_REG0 to TRIM_REG3 can only be written when the UNLOCK input pin 119 is high. The Trim_Fault bit is set in the FAULT_STATUS0 register (section 13.5.1 on page 57) if a write is attempted to registers TRIM_REG0 to TRIM_REG3 when the UNLOCK input is low, and the write transaction is blocked.

Trim values are 2's complement, so all 0s is mid range, all 100...0 is full negative trim, and 011...1 is full positive trim.

Address	Name	R/W	Register Contents															
			D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0x600	TRIM_REG0	R/W	-	-	-	Trim_+1.5VD			Trim_+1.5VA				Trim_+5V					
0x601	TRIM_REG1	R/W	-	Trim_VREF					Trim_VREF_TC				Trim_VBG_Redundant					
0x602	TRIM_REG2	R/W	-	-	-	Trim_VREFH				Trim_VREFHL				Trim_VTOI				
0x603	TRIM_REG3	R/W	-	-	Trim_REFPN_LVDT34					Trim_REFPN_LVDT12				Trim_WD				
0x604	TRIM_REG4	R/W	Trim_Reserve															
0x605	TRIM_REG5	R/W	-	Trim_TEMP3_SRC					Trim_TEMP2_SRC				Trim_TEMP1_SRC					
0x606	TRIM_REG6	R/W	-	Trim_REFPN_ISENSE12					Trim_TEMP5_SRC				Trim_TEMP4_SRC					
0x607	TRIM_REG7	R/W	-	Trim_5.25V					Trim_REFPN_ISENSE5				Trim_REFPN_ISENSE34					
0x608	TRIM_REG8	R/W	COM_CFG0 (UART baud rate tuning)							COM_CFG0 (SPI/UART timeout)								

13.12.1 TRIM_REG0 REGISTER 0x600

This register adjusts, in real time, the outputs of the +5V, +1.5VA, and +1.5VD internal voltage regulators. Default values are written during power-up and reset with factory trim values stored in OTP. This register can only be written when the UNLOCK input pin 119 is high.

Bits	Name	Description
0 - 4	Trim_+5V	0 is mid trim position The 7 values from b'00001' to b'01111' increase the +5V regulator's output voltage by 66mV to 495mV, in steps of 66mV The 8 values from b'11111' to b'10000' decrease the +5V regulator's output voltage by -66mV to -561mV, in steps of -66mV
5 - 9	Trim_+1.5VA	0 is mid trim position The 7 values from b'00001' to b'01111' increase the +1.5VA regulator's output voltage by 3mV to 21mV, in steps of 3mV The 8 values from b'11111' to b'10000' decrease the +1.5VA regulator's output voltage by -3mV to -24mV, in steps of -3mV
10 - 12	Trim_+1.5VD	0 is mid trim position The 3 values from b'0001' to b'0111' increase the +1.5VD regulator's output voltage by 7.2mV to 21.6mV, in steps of 7.2mV The 4 values from b'1111' to b'1000' decrease the +1.5V Dregulator's output voltage by -7.2mV to -28.8mV, in steps of -7.2mV
13 - 15	-	Unimplemented bits which read back as 0

13.12.2 TRIM_REG1 REGISTER 0x601

This register adjusts, in real time, the VREF and redundant bandgap voltage references, and the VREF temperature trim. This register can only be written when the UNLOCK input pin 119 is high.

Bits	Name	Description
0 - 4	Trim_VBG_Redundant	0 is mid trim position The 7 values from b'00001' to b'01111' increase the redundant bandgap's voltage by 4.4mV to 30.8mV, in steps of 4.4mV The 8 values from b'11111' to b'10000' decrease the redundant bandgap's voltage by -4.4mV to -35.2mV, in steps of -4.4mV
5 - 8	Trim_VREF_TC	0 is mid trim position The 7 values from b'00001' to b'01111' increasingly reduce VREF's temperature coefficient The 8 values from b'11111' to b'10000' increasingly raise VREF's temperature coefficient
9 - 14	Trim_VREF	0 is mid trim position The 15 values from b'00001' to b'01111' increase the VREF voltage by 1.25mV to 18.75mV, in steps of 1.25mV The 16 values from b'11111' to b'10000' decrease the VREF voltage by -1.25mV to -20mV, in steps of -1.25mV
15	-	Unimplemented bit which reads back as 0

13.12.3 TRIM_REG2 REGISTER 0x602

VREFH trims the ADC high reference (1.3V). VREFHL trims the ADC low reference to make VREFH - VREFL = 1.1V. This register can only be written when the UNLOCK input pin 119 is high.

Bits	Name	Description
0 - 3	Trim_VTOI	0 is mid trim position The 3 values from b'0001' to b'0111' increase VTOI by 1μA to 3μA, in steps of 1μA The 4 values from b'1111' to b'1000' decrease VTOI by -1μA to -4μA, in steps of -1μA
4 - 8	Trim_VREFHL	0 is mid trim position The 7 values from b'00001' to b'01111' increase VREFHL by 1mV to 7mV, in steps of 1mV The 8 values from b'11111' to b'10000' decrease VREFHL by -1mV to -8mV, in steps of -1mV
9 - 12	Trim_VREFH	0 is mid trim position The 3 values from b'0001' to b'0111' increase VREFH by 0.7mV to 2.1mV, in steps of 0.7mV The 4 values from b'1111' to b'1000' decrease VREFH by -0.7mV to -2.8mV, in steps of -0.7mV
13 - 15	-	Unimplemented bits which read back as 0

13.12.4 TRIM_REG3 REGISTER 0x603

This register can only be written when the UNLOCK input pin 119 is high.

Bits	Name	Description
0 - 3	Trim_WD	0 is mid trim position The 3 values from b'0001' to b'0111' increase the watchdog frequency by 10kHz to 30kHz, in steps of 10kHz The 4 values from b'1111' to b'1000' decrease the watchdog frequency by -10kHz to -40kHz, in steps of -10kHz
4 - 8	Trim_REFPN_LVDT12	0 is mid trim position The 7 values from b'00001' to b'01111' increase REFPN_LVDT12 by 55LSB/V to 385LSB/V, in steps of 55LSB/V The 8 values from b'11111' to b'10000' decrease REFPN_LVDT12 by -55LSB/V to -440LSB/V, in steps of -55LSB/V
9 - 13	Trim_REFPN_LVDT34	0 is mid trim position The 7 values from b'00001' to b'01111' increase REFPN_LVDT34 by 55LSB/V to 385LSB/V, in steps of 55LSB/V The 8 values from b'11111' to b'10000' decrease REFPN_LVDT34 by -55LSB/V to -440LSB/V, in steps of -55LSB/V

		in steps of -55LSB/V
14 - 15	-	Unimplemented bits which read back as 0

13.12.5 TRIM_REG5 REGISTER 0x605

Bits	Name	Description
0 - 4	Trim_TEMP1_SRC	0 is mid trim position The 7 values from b'00001' to b'01111' increase the TEMP1_SRC current in 1mA mode by 22µA to 154µA, in steps of 22µA The 8 values from b'11111' to b'10000' decrease the TEMP1_SRC current in 1mA mode by -22µA to -176mV, in steps of -22µA
5 - 9	Trim_TEMP2_SRC	0 is mid trim position The 7 values from b'00001' to b'01111' increase the TEMP2_SRC current in 1mA mode by 22µA to 154µA, in steps of 22µA The 8 values from b'11111' to b'10000' decrease the TEMP2_SRC current in 1mA mode by -22µA to -176mV, in steps of -22µA
10 - 14	Trim_TEMP3_SRC	0 is mid trim position The 7 values from b'00001' to b'01111' increase the TEMP3_SRC current in 1mA mode by 22µA to 154µA, in steps of 22µA The 8 values from b'11111' to b'10000' decrease the TEMP3_SRC current in 1mA mode by -22µA to -176mV, in steps of -22µA
15	-	Unimplemented bit which reads back as 0

13.12.6 TRIM_REG6 REGISTER 0x606

Bits	Name	Description
0 - 4	Trim_TEMP4_SRC	0 is mid trim position The 7 values from b'00001' to b'01111' increase the TEMP4_SRC current in 1mA mode by 22µA to 154µA, in steps of 22µA The 8 values from b'11111' to b'10000' decrease the TEMP4_SRC current in 1mA mode by -22µA to -176mV, in steps of -22µA
5 - 9	Trim_TEMP5_SRC	0 is mid trim position The 7 values from b'00001' to b'01111' increase the TEMP5_SRC current in 1mA mode by 22µA to 154µA, in steps of 22µA The 8 values from b'11111' to b'10000' decrease the TEMP5_SRC current in 1mA mode by -22µA to -176mV, in steps of -22µA
10 - 14	Trim_REFPN_ISENSE12	0 is mid trim position The 7 values from b'00001' to b'01111' increase the trim voltage by mV to mV, in steps of mV The 8 values from b'11111' to b'10000' decrease the trim voltage by -mV to -mV, in steps of -mV
15	-	Unimplemented bit which reads back as 0

13.12.7 TRIM_REG7 REGISTER 0x607

Bits	Name	Description
0 - 4	Trim_REFPN_ISENSE34	0 is mid trim position The 7 values from b'00001' to b'01111' increase REFPN_ISENSE34 by by 55LSB/V to 385LSB/V, in steps of 55LSB/V The 8 values from b'11111' to b'10000' decrease REFPN_ISENSE34 by by -55LSB/V to -440LSB/V, in steps of -55LSB/V
5 - 9	Trim_REFPN_ISENSE5	0 is mid trim position The 7 values from b'00001' to b'01111' increase REFPN_ISENSE5 by by 55LSB/V to 385LSB/V, in steps of 55LSB/V The 8 values from b'11111' to b'10000' decrease REFPN_ISENSE5 by by -55LSB/V to -440LSB/V, in steps of -55LSB/V
10 - 14	Trim_5.25V	0 is mid trim position The 7 values from b'00001' to b'01111' increase the +5.25V regulator's output voltage by 41.4mV to 289.8mV, in steps of 41.4mV The 8 values from b'11111' to b'10000' decrease the +5.25V regulator's output voltage by -41.4mV to -331.2mV, in steps of -41.4mV

15	-	Unimplemented bit which reads back as 0
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13.12.8 TRIM_REG8 REGISTER 0x608

Bits	Name	Description
0 - 7	COM_CFG0	SPI/UART timeout
8 - 15		UART baud rate tuning

13.13 OTP Registers

OTP memory can only be programmed when the UNLOCK input pin 119 is high.

Address	Name	R/W	Register Contents																
			D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
0x700	OTP_REG0	R/W	-	-	-	-	-	-	-	-	-	OTP_Address							
0x701	OTP_REG1	R/W	-	-	-	-	-	-	-	-	-	-	-	-	-	OTP_Program			
0x702	OTP_REG2	R/W	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-		
0x703	OTP_REG3	R	-	-	-	-	-	-	-	OTP_Read_Data									
0x704	OTP_REG4	R	-	-	-	OTP_State													
0x705	OTP_REG5	R/W	-	-	-	-	-	-	-	-	-	-	-	-	-	-	OTP_Config		
0x706	OTP_REG6	W	OTP_Shadow_Load																
0x707	OTP_REG7	R/W	-	-	-	-	-	-	-	OTP_Write_Duration									

13.13.1 OTP_REG0 REGISTER 0x701

Bits	Name	Safe Value	Description
0 - 6	OTP_Address[6:0]	0x00	Target address for OTP read and write. These are bits 9:3 of the OTP. In SECDED mode (below), LSB is a don't care
7 - 15	-	-	Unimplemented bits which read back as 0

13.13.2 OTP_REG1 REGISTER 0x702

Bits	Name	Safe Value	Description
0 - 2	OTP_Program[2:0]	0x0	Target bit for OTP program. Write to this address after choosing the address in OTP_REG0. A write to this location will initiate a programming event if unlock is high
3 - 15	-	-	Unimplemented bits which read back as 0

13.13.3 OTP_REG3 REGISTER 0x703

Bits	Name	Description
0 - 8	OTP_Read_Data[8:0]	8 LSB are the 8 bit read, MSB is a valid bit. Only valid when read completes (~6 cycles after write to OTP_REG0). Invalidated once another OTP command occurs (read/program/shadow_load)
9 - 15	-	Unimplemented bits which read back as 0

13.13.4 OTP_REG4 REGISTER 0x704

Bits	Name	Description
0 - 2	OTP_State[2:0]	OTP state
3 - 7	OTP_State[7:3]	Command processor state
8 - 11	OTP_State[11:8]	SECDED state
12	OTP_State[12]	Unlock bit

13 - 15	-	Unimplemented bits which read back as 0
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13.13.5 OTP_REG5 REGISTER 0x705

Bits	Name	Safe Value	Description
0	OTP_Config[0]	0	Bit 0 controls "raw (uncorrected)" or SECDED read access. When 0 (or in shadow load mode), LSB of OTP addr is ignored and two bytes are read. The two bytes go into a 16-bit SECDED decoder and the 8 LSB of the SECDED output are read into OTP_REG3. If a fault occurs, if correctable, OTP_correctable_Fault fires. If uncorrectable, OTP_uncorrectable_Fault fires. SECDED read: read OTP ADDR bbbbbbb1 and bbbbbbb0, where bbbbbbbX is written into OTP_REG0, treat the 16 bits as input to SECDED decoder, returns 11 bits, use 8 LSBs, drop 3 MSBs When 1, then LSB of address is used, 8 bits from that OTP location are transferred to OTP_REG3. Raw read: read OTP ADDR bbbbbbb where bbbbbbb is written into OTP_REG0, the 8 bits from that OTP location go into OTP_REG3
1	OTP_Config[1]	0	Disables power to the OTP memory. In that scenario, no reads or writes will occur. Any operation to the OTP with this bit low is a fault
2 - 15	-	-	Unimplemented bits which read back as 0

13.13.6 OTP_REG6 REGISTER 0x706

Bits	Name	Safe Value	Description
0 - 15	OTP_Shadow_Load	-	A write to this location of 0x524C will initiate a full refresh of all shadowed registers with the OTP values (see section 13.14 OTP Memory Map)

13.13.7 OTP_REG7 REGISTER 0x707

Bits	Name	Safe Value	Description
0 - 8	OTP_Write_Duration[8:0]	0xC0	Number of system clocks for write pulse (set to ~8us/clock period). Default meets the 6us to 10us spec limit for 20-30Mhz system clock, but this can be tuned for better margin to spec
9 - 15	-	-	Unimplemented bits which read back as 0

13.14 OTP Memory Map

Some OTP uses the same SECDED protection as the serial interfaces (section 11.12 on page 26). For the 32-bit trim words Trim0 to Trim7, the 16 bit trim values are {Byte 2, Byte 0}, with Byte 1 protecting Byte 0, Byte 3 protecting Byte 2.

OTP Sector	OTP Address	Byte 3	Byte 2	Byte 1	Byte 0	Description
0	0, 4, 8, 12	Trim0, Trim1, Trim2, Trim3				Factory trim
1	16, 20, 24, 28	Trim4, Trim5, Trim6, Trim7				Factory trim
2	32	CRC				CRC16 ccitt, polynomial 1021, seed FFFF, shift in MSB first for each 16bit word
2	36, 40, 44	free				
3	48-63	free				
4	64-79	free				
5	80-95	free				
6	96-111	free				
7	112	SECDED protection for Byte 2	COM_CFG[15:14], stop2, parity, Baud_Rate [11:8]	SECDED protection for Byte 0	Baud_Rate [7:0]	COM_CFG[15:0] is mapped to: COM_CFG[15:14] (used to select UART_Mode), Stop2 (two stop bits needed for each UART byte), parity (even byte), Baud_Rate [11:0] (bit[1] used in SPI2 for out on positive edge, bit[0] used in SPI1 for out on positive edge).
7	116, 120	free				

7	124	Lock7,7,6,6, 5,5,4,4	Lock3,3,2,2, 1,1,0,0	free	free	
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13.15 Watchdog Registers

The internal watchdog operates from an independent internal 440kHz ± 30 kHz clock, and operates after power-up or a reset to check that the 20MHz to 30MHz system clock, F_{OSC} , is operating within reasonable bounds. The serial interfaces remain inoperative until the watchdog test is complete. The system clock is always F_{OSC} and not $4 \times F_{OSC}$ when the watchdog check is running because the system is in Startup Mode with the PLL disabled.

There are two fault outputs: the WD_Clock_Fault bit in the FAULT_STATUS0 register (section 13.5.1 on page 57) and the Fosc_Fault bit in the CRITICAL_STATUS register (section 13.5.13 on page 65). A fault means that either the respective clock is stuck, or that the watchdog clock and system clock are not running at the expected relative frequency. The watchdog cannot distinguish which clock (or even both) is at the wrong frequency, just that the relative frequency is outside the bounds set by the window settings.

A WD_Clock_Fault is a maskable fault, because by itself it does not create any functional issue, but indicates that part of the on-chip diagnostics are not functioning properly.

A Fosc_Fault indicates that there is something wrong with the 20MHz to 30MHz system clock and so is treated as a critical fault. Since this may indicate that the system clock F_{OSC} is frozen, preventing the chip from entering a valid state, this fault will hold the chip in reset.

Address	Name	R/W	Register Contents																	
			D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0		
0x201	WATCHDOG_REG1	R/W	-	-	-	-	-	WD_Window_Hi[10:0]												
0x202	WATCHDOG_REG2	R/W	-	-	-	-	-	WD_Window_Lo[10:0]												
0x203	WATCHDOG_REG3	R/W	WD_Sample_Size[15:0]																	
0x204	WATCHDOG_REG4	R/W	WD_Min_Count[15:0]																	
0x206	WATCHDOG_REG6	R	-	-	-	-	-	WD_Clock_Counter[10:0]												
0x207	WATCHDOG_REG7	R	Fosc_Counter[15:0]																	
0x208	WATCHDOG_REG8	R	-	-	-	-	-	-	-	-	-	-	WD_Count[2:0]		Fosc_Count[2:0]					

The watchdog configures two up-counters, the 16 bit Fosc_Counter and the 11 bit WD_Clock_Counter, to check the relative frequency between the watchdog clock and the system clock. Window registers set the acceptable tolerance between the two clocks. Two up/down-counters, Fosc_Counter and WD_Clock_Counter, count successive tests from the perspective of each clock. The up/down-counters both start at the value 2, and are incremented for each successful test, and decremented for a failure. If either counter reaches 0, the watchdog terminates with a fault. If WD_Clock_Counter reaches 4, the watchdog exits successfully.

The watchdog state machine operates as follows:

- The good system clock restart counter Fosc_Count and the good system clock restart counter WD_Count are set to 0x2
- The two up-counters Fosc_Counter and WD_Clock_Counter are cleared and start counting from system clock and watchdog clock respectively
- When the Fosc_Counter up-counter reaches the value WD_Sample_Size (default: 10000) set in the WATCHDOG_REG3 register:
 - The value of WD_Clock_Counter shadowed in the WATCHDOG_REG7 register is checked to be between the lower limit WD_Window_Lo (default: 50) set in the WATCHDOG_REG2 register and the upper limit WD_Window_Hi (default: 1000) set in the WATCHDOG_REG1 register
 - If shadow WD_Clock_Counter is within the window, then Fosc_Count is incremented
 - If shadow WD_Clock_Counter is not within the window, then Fosc_Count is decremented
 - The value of WD_Clock_Counter itself is also checked to be between WD_Window_Lo and WD_Window_Hi
 - If WD_Clock_Counter is within the window, then WD_Count is incremented
 - If WD_Clock_Counter is not within the window, then WD_Count is decremented
- If the Fosc_Count counter has reached 0, this is treated as a watchdog fault, and the watchdog exits with a WD_Clock_Fault

- If the WD_Count counter has reached 0, this is treated as a system clock fault, and the watchdog exits with a Fosc_Fault
- If the WD_Count counter has reached 2, the watchdog exits successfully. Otherwise, the two up-counters Fosc_Counter and WD_Clock_Counter are cleared again and another test performed

There are two other checks that catch unusual fault scenarios:

- When the Fosc_Counter reaches a low count value, WD_Min_Count (default:500) set in the WATCHDOG_REG4 register, the watchdog counter is checked that it is not already past the lower limit WD_Window_Lo. This detects the case where watchdog clock is stuck and the watchdog counter is frozen in the range between WD_Window_Lo and WD_Window_Hi
- If the watchdog counter goes above the upper limit WD_Window_Hi during the tests, the system clock is either stopped or running very slowly. The watchdog exits with a Fosc_Fault

13.15.1 WATCHDOG_REG1 REGISTER 0x201 (WATCHDOG HIGH WINDOW)

Bits	Name	Safe Value	Description
10 - 0	WD_Window_Hi[10:0]	1000	High window for watchdog
11 - 15	-	-	Unimplemented bits which read back as 0

13.15.2 WATCHDOG_REG2 REGISTER 0x202 (WATCHDOG LOW WINDOW)

Bits	Name	Safe Value	Description
10 - 0	WD_Window_Lo[10:0]	50	Low window for watchdog
11 - 15	-	-	Unimplemented bits which read back as 0

13.15.3 WATCHDOG_REG3 REGISTER 0x203 (WATCHDOG SAMPLE FREQUENCY)

The safe value of 10000 counts reduces the 20MHz - 30MHz system clock F_{osc} to 2 - 3kHz, providing a watchdog window check every 333 - 500 μ s.

Bits	Name	Safe Value	Description
15 - 0	WD_Sample_Size[15:0]	10000	Number of system clocks before checking watchdog window

13.15.4 WATCHDOG_REG4 REGISTER 0x204 (WATCHDOG STUCK TEST)

Bits	Name	Safe Value	Description
15 - 0	WD_Min_CLK[15:0]	500	Early sample to make sure watchdog clock is not stuck in the good window range

13.15.5 WATCHDOG_REG6 REGISTER 0x206 (WATCHDOG CLOCK COUNT)

Bits	Name	Description
10 - 0	WD_Clock_Counter[10:0]	Shadow of the watchdog clock counter value, synchronized to the system clock F_{osc}
11 - 15	-	Unimplemented bits which read back as 0

13.15.6 WATCHDOG_REG7 REGISTER 0x207 (SYSTEM CLOCK COUNT)

Bits	Name	Description
15 - 0	Fosc_Counter[15:0]	Shadow of the system clock counter value, synchronized to the system clock F_{osc}

13.15.7 WATCHDOG_REG8 REGISTER 0x208 (WATCHDOG AND SYSTEM RESTARTS)

Bits	Name	Description
0 - 2	Fosc_Count[2:0]	Good system clock restart count

3 - 5	WD_Count[2:0]	Good watchdog clock restart count
6 - 15	-	Unimplemented bits which read back as 0

13.16 UART Registers

The 0xD00 and 0xD01 registers manage UART channel 1, and the 0xD02 and 0xD03 registers manage UART channel 2.

The two counters U1_Warn_Baud_Counter and U2_Warn_Baud_Counter log up to 255 events of the respective UART bit sampling timing being out of spec, allowing timing shifts in the serial interface to be monitored.

Either both UART are active or both SPI are active.

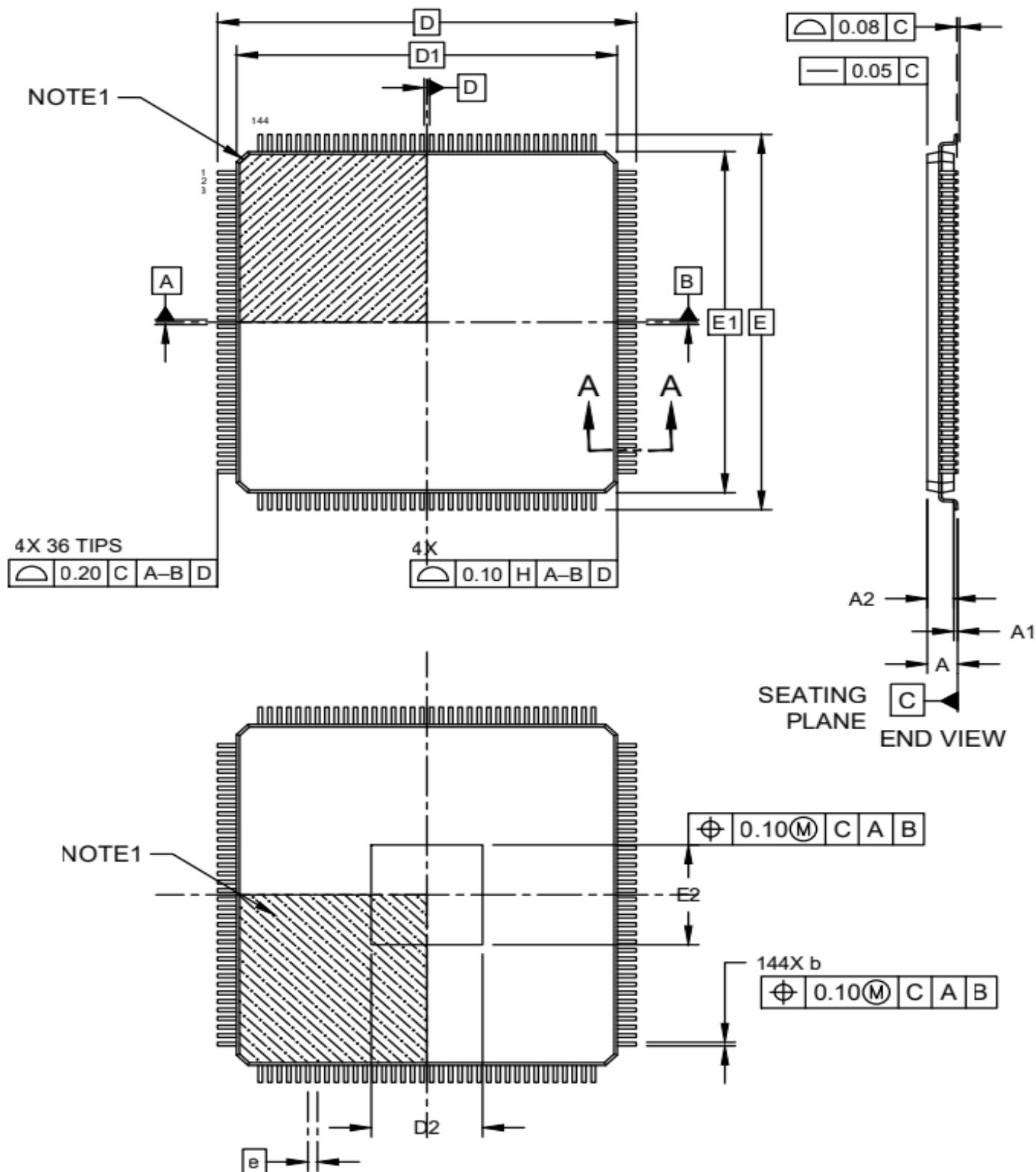
UART is active when 2 OTP bits are set in the COM CONFIG word (bits 15&14). This is the permanent set condition. UART_EN and UNLOCK are raised. This is the temporary UART mode. UNLOCK ensures that there is not a single point of failure that would kill the SPI ports (if UART_EN was shorted high or the input buffer failed)

Address	Name	R/W	Register Contents															
			D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0xD00	UART_U1_WARN	R	-	-	-	-	-	-										U1_Warn_Baud_Counter
0xD01	UART_U1_WARN_RST	W	Writing any value to this register resets U1_Warn_Baud_Counter															
0xD02	UART_U2_WARN	R	-	-	-	-	-	-	-									U2_Warn_Baud_Counter
0xD03	UART_U2_WARN_RST	W	Writing any value to this register resets U2_Warn_Baud_Counter															

14 LQFP-144 Dimensions

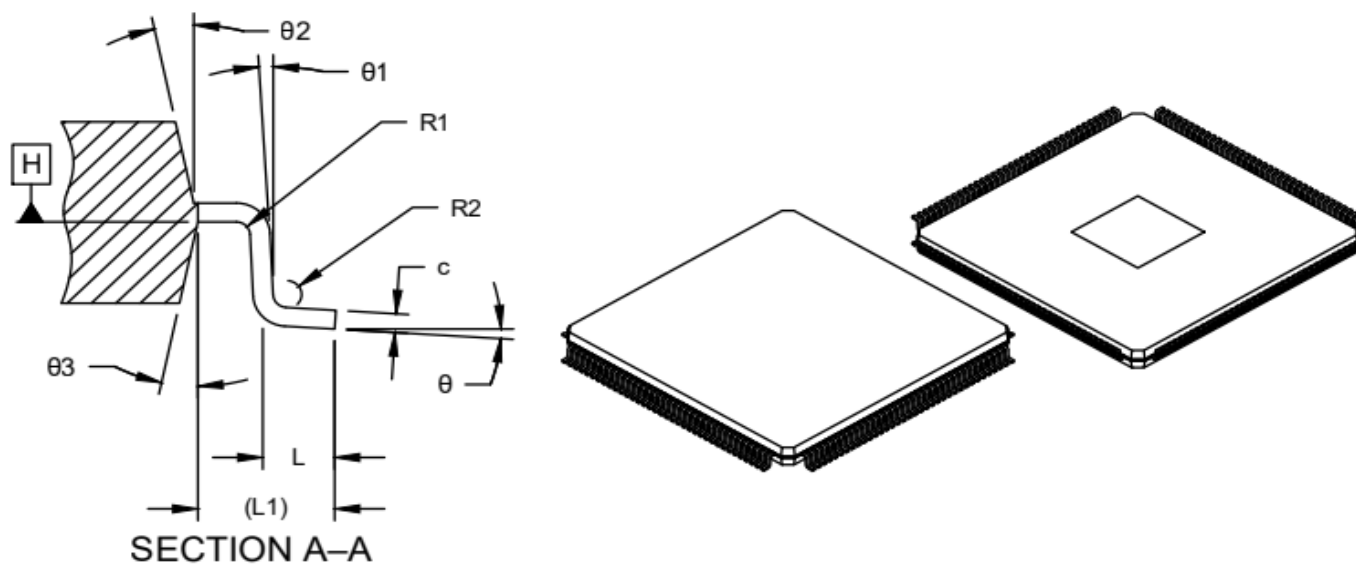
144-Lead Low-profile Plastic Quad Flat Pack (L7C) 20x20x1.4mm Body [LQFP] With Exposed Pad 5.85x5.85mm

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



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Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		144	
Lead Pitch	e		0.50 BSC	
Overall Height	A	-	-	1.60
Molded Package Height	A2	1.35	1.40	1.45
Standoff	A1	0.05	-	0.15
Overall Length	D		22.00 BSC	
Overall Width	E		22.00 BSC	
Molded Body Length	D1		20.00 BSC	
Molded Body Width	E1		20.00 BSC	
Exposed Pad Length	D2	5.75	5.85	5.95
Exposed Pad Width	E2	5.75	5.85	5.95
Lead Thickness	c	0.09	-	0.20
Lead Width	b	0.17	0.22	0.27
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 (REF)	
Lead Bend Radius	R1	0.08	-	-
Lead Bend Radius	R2	0.08	-	0.20
Terminal Foot Angle	θ	0°	3.5°	7°
Lead Angle	θ1	0°	-	-
Mold Draft Angle Top	θ2	11°	12°	13°
Mold Draft Angle Bottom	θ3	11°	12°	13°

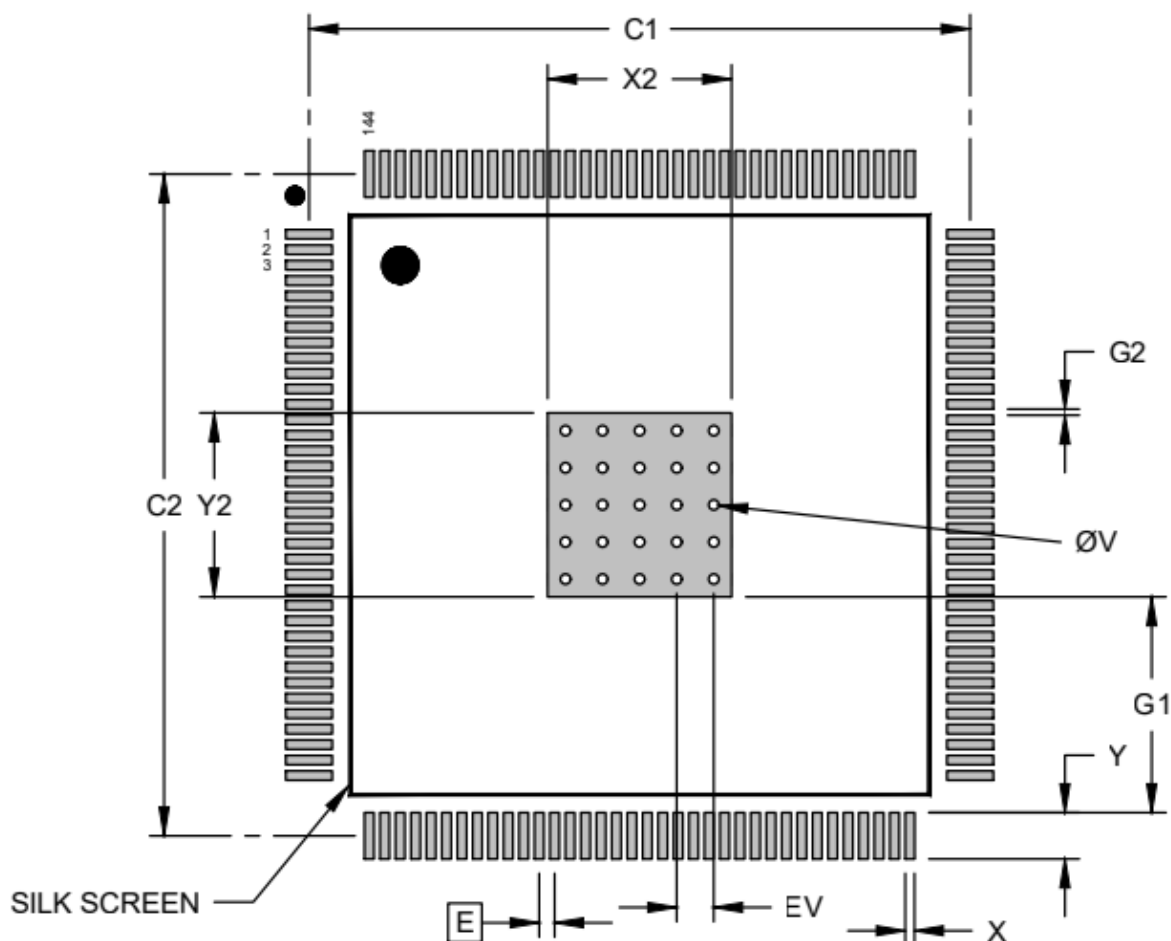
Figure 21. 144-Lead LQFP Package Dimensions

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area
2. Dimensioning and tolerancing per ASME Y14.5M
 - a. BSC: Basic Dimension. Theoretically exact value shown without tolerances
 - b. REF: Reference Dimension, usually without tolerance, for information purposes only.

144-Lead Low-profile Plastic Quad Flat Pack (L7C) 20x20x1.4mm Body [LQFP] With Exposed Pad 5.85x5.85mm

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Center Pad Width	X2			5.95
Center Pad Length	Y2			5.95
Contact Pad Spacing	C1		21.40	
Contact Pad Spacing	C2		21.40	
Contact Pad Width (X144)	X1			0.30
Contact Pad Length (X144)	Y1			1.50
Contact Pad to Center Pad (X144)	G1	6.98		
Contact Pad to Contact Pad (X140)	G2	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Figure 22. 144-Lead LQFP typical footprint

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
 - a. BSC: Basic Dimension. Theoretically exact value shown without tolerances.

15 Revision History

15.1 Revision 0.73 - November 2025

Pre-release. Changes not logged.

15.2 Revision 1.0 - January 2026

First release.

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