

32-Channel LCD Driver with Separate Backplane Output

Features

- 32-Channel High-Voltage Push-Pull Outputs
- Up to 60V Output Voltage
- Low-Power Level Shifting
- 5 MHz Shift Register Speed
- Latched Data Outputs
- Bidirectional Shift Register (DIR)
- Backplane Output

Applications

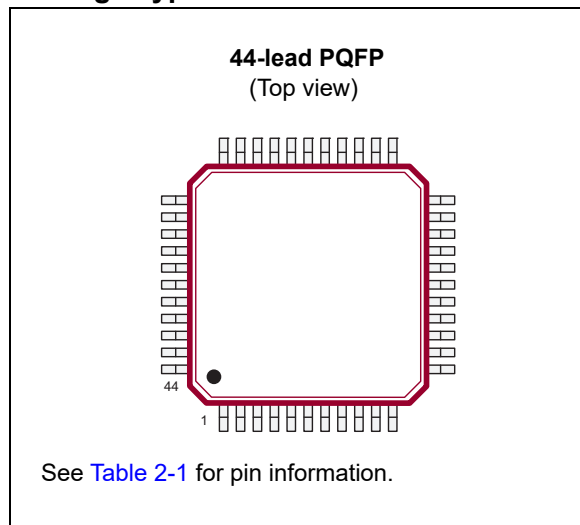
- LCD Drivers
- Display Drivers
- Inkjet Drivers
- 3D Printer Drivers
- Microelectromechanical Systems Applications

General Description

The HV66 is a low-voltage to high-voltage serial-to-parallel converter with push-pull outputs. This device is designed as a driver circuit for LCD displays. It can also be used in any application requiring multiple-output high-voltage current sourcing-and-sinking capabilities. The inputs are fully CMOS compatible.

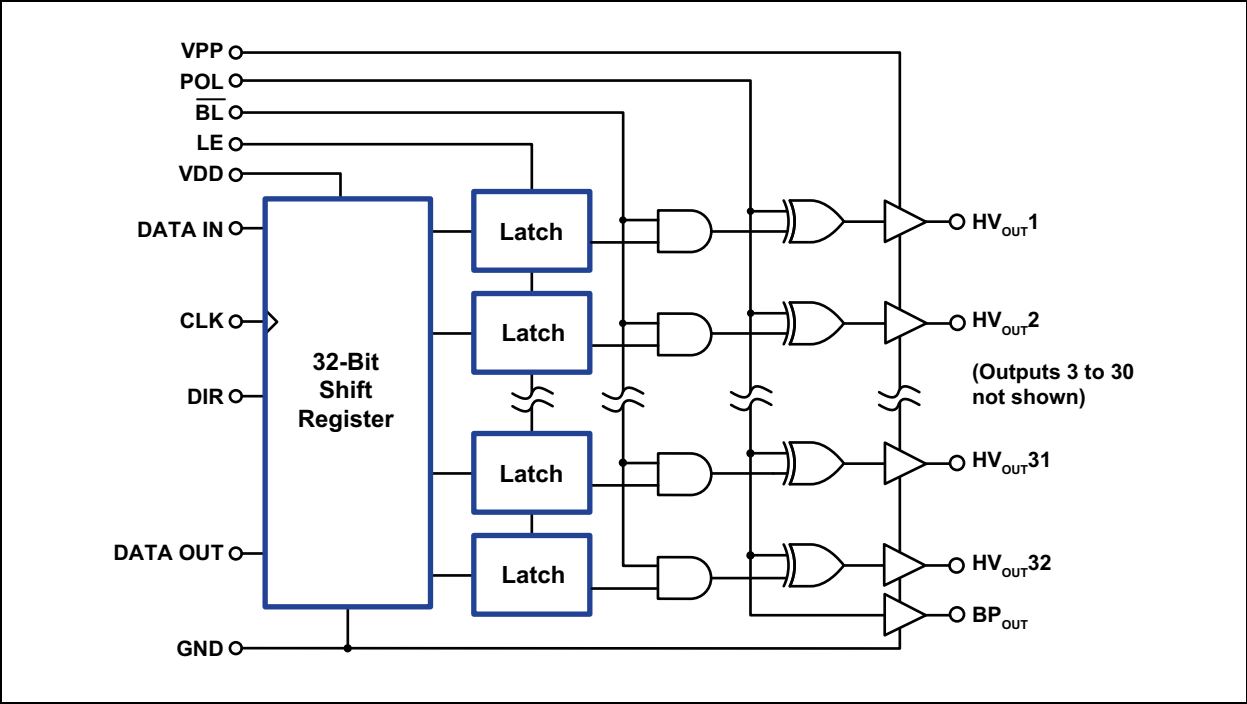
The device consists of a 32-bit Shift register, 32 latches, and control logic to perform blanking and polarity control of the outputs. The HV_{OUT1} is connected to the first stage of the Shift register. Data is shifted through the Shift register on the logic rising transition of the clock. A DIR pin causes data shifting to move in a clockwise direction when grounded. When connected to V_{DD}, the pin causes data shifting to move in a counter clockwise direction. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the Shift register. The operation of the Shift register is not affected by the latch enable (LE), blanking (BL) and the polarity (POL) inputs. Transfer of data from the Shift register to the latch occurs when the latch enable (LE) input is high. The data in the latch is stored after LE transitions from high to low.

Package Type

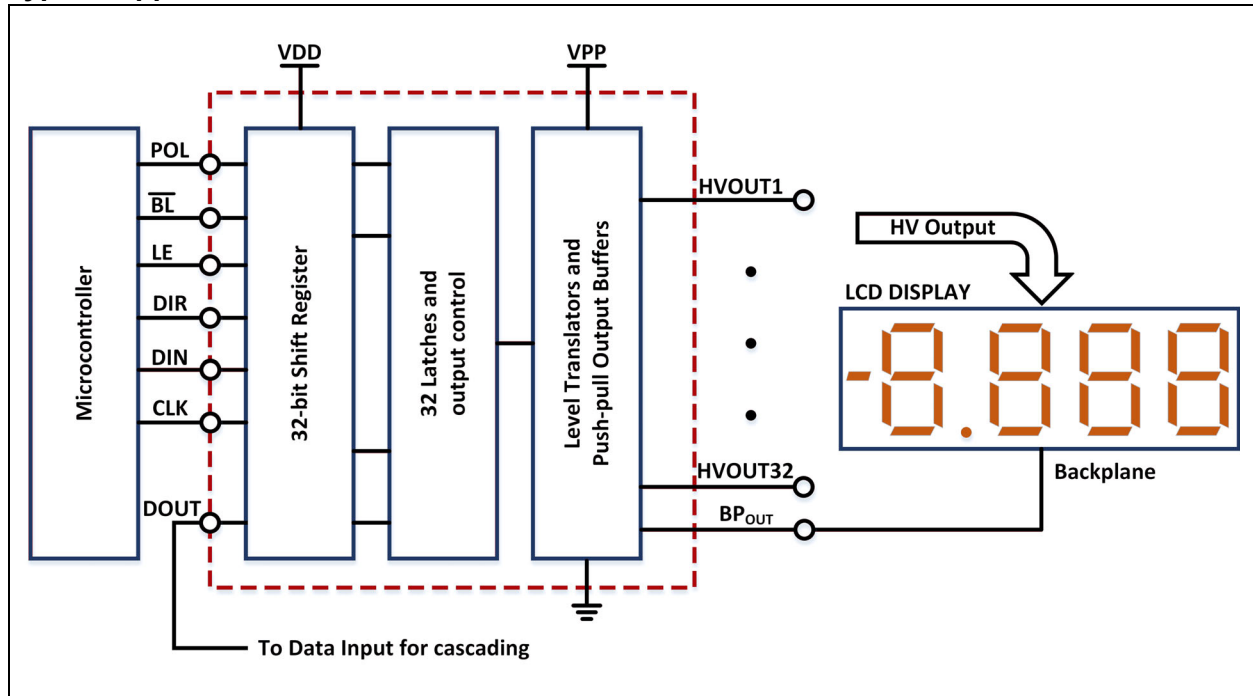


HV66

Functional Block Diagram



Typical Application Circuit



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Logic Supply Voltage, V_{DD} (Note 1)	–0.5V to +7V
High-Voltage Supply Voltage, V_{PP} (Note 1)	–0.5V to +70V
Logic Input Levels	–0.5V to $V_{DD}+0.5V$
Ground Current (Note 2)	1.5A
Maximum Junction Temperature, $T_{J(MAX)}$	+125°C
Storage Temperature, T_S	–65°C to +125°C
Continuous Total Power Dissipation:	
44-lead PQFP (Note 3)	1200 mW

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: All voltages are referenced to GND.

2: Duty cycle is limited by the total power dissipated in the package.

3: For operations above 25°C ambient, derate linearly to 85°C at 20 mW/°C.

RECOMMENDED OPERATING CONDITIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Logic Supply Voltage	V_{DD}	4.5	—	5.5	V	
High-Voltage Supply Voltage	V_{PP}	12	—	60	V	
High-Level Input Voltage	V_{IH}	2.4	—	V_{DD}	V	
Low-Level Input Voltage	V_{IL}	0	—	0.8	V	
Clock Frequency	f_{CLK}	0	—	5	MHz	
Operating Ambient Temperature	T_A	–40	—	+85	°C	
Allowable Current through Output Diodes	I_{OD}	—	—	200	mA	

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: Over recommended operating conditions unless otherwise stated. V _{DD} = 5V, V _{PP} = 60V.							
Parameter		Sym.	Min.	Typ.	Max.	Unit	Conditions
V _{DD} Supply Current		I _{DD}	—	—	15	mA	f _{CLK} = 5 MHz, V _{DD} = 5.5V
Quiescent V _{PP} Supply Current		I _{PPQ}	—	—	0.5	mA	
Quiescent V _{DD} Supply Current		I _{DDQ}	—	—	0.5	mA	All V _{IN} = GND or V _{DD}
High-Level Logic Input Current		I _{IH}	—	—	1	μA	V _{IH} = V _{DD}
Low-Level Logic Input Current		I _{IL}	—	—	−1	μA	V _{IL} = 0V
High-Level Output Data Out	HV _{OUT}	V _{OH}	50	—	—	V	I _O = −5 mA, V _{PP} = 60V
	Data Out		4.6	—	—	V	I _O = −100 μA
Low-Level Output Voltage	HV _{OUT}	V _{OL}	—	—	8	V	I _O = 5 mA, V _{PP} = 60V
	Data Out		—	—	0.4	V	I _O = 100 μA
Low-Level Output Voltage, Backplane		V _{OLBP}	—	—	3	V	I _O = 10 mA
High-Level Output Voltage, Backplane		V _{OHBP}	57	—	—	V	I _O = −10 mA

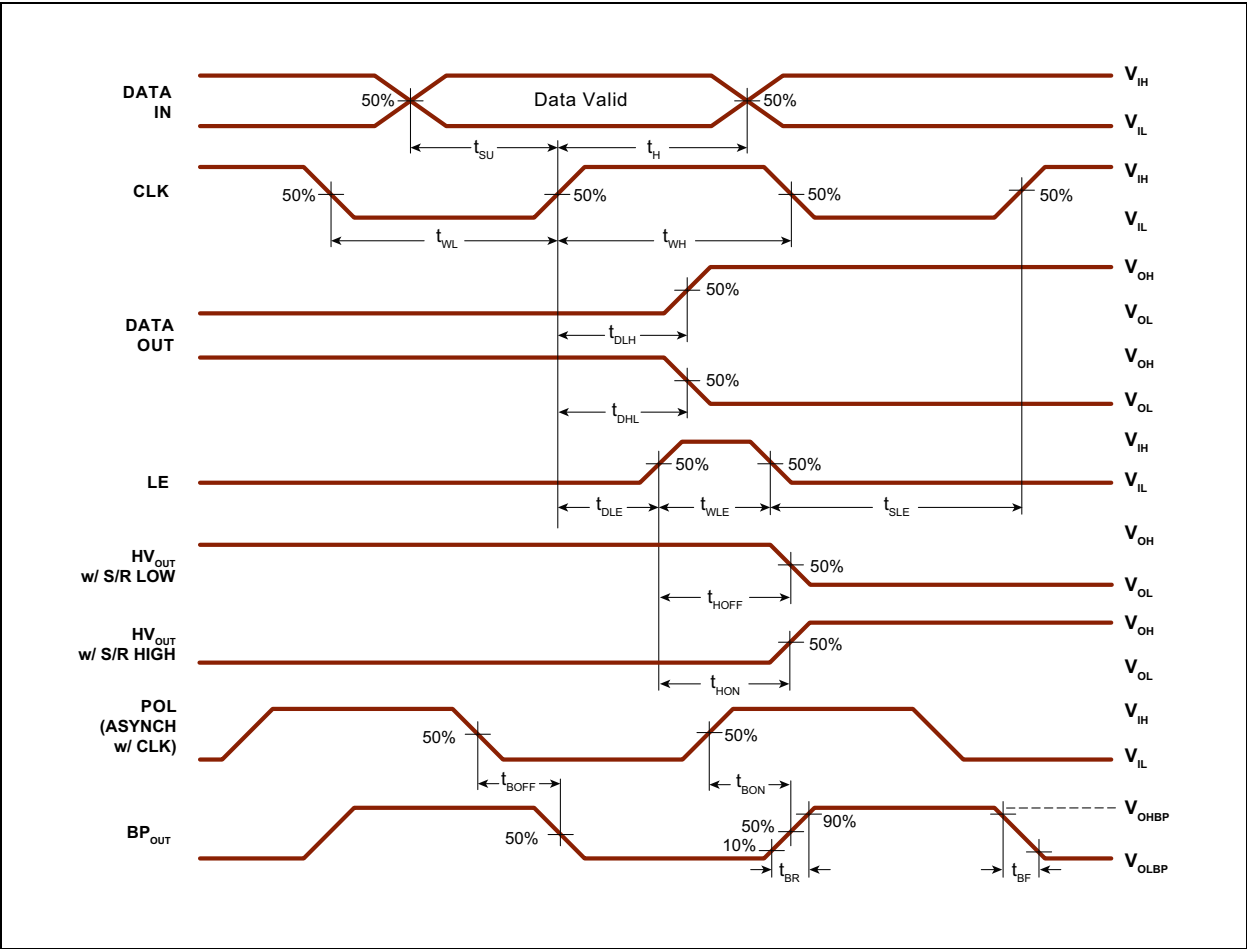
AC ELECTRICAL CHARACTERISTICS

Electrical Specifications: $V_{DD} = 5V$, $V_{PP} = 60V$, $T_A = 25^\circ C$, Logic Input Rise/Fall Time = 10 ns.						
Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Clock Frequency	f_{CLK}	—	—	5	MHz	
Clock Width, High or Low	t_{WL} , t_{WH}	100	—	—	ns	
Data Setup Time before Clock Rises	t_{SU}	25	—	—	ns	
Data Hold Time after Clock Rises	t_H	50	—	—	ns	
Time from Latch Enable or POL to HV _{OUT}	t_{HON} , t_{HOFF}	—	—	500	ns	$C_L = 20 \text{ pF}$
Time from POL to BP _{OUT}	t_{BON} , t_{BOFF}	—	—	500	ns	$C_L = 20 \text{ pF}$
Delay Time Clock to Data High to Low	t_{DHL}	—	—	200	ns	$C_L = 10 \text{ pF}$
Delay Time Clock to Data Low to High	t_{DLH}	—	—	200	ns	$C_L = 10 \text{ pF}$
Delay Time Clock to Latch Enable Low to High	t_{DLE}	50	—	—	ns	
Latch Enable Pulse Width	t_{WLE}	100	—	—	ns	
Latch Enable Setup Time before Clock Falls	t_{SLE}	50	—	—	ns	
BP _{OUT} Rise and Fall Time	t_{BR} , t_{BF}	10	—	1000	μs	$C_L = 350 \text{ pF}$
BP _{OUT} Rise and Fall Time Difference	$ t_{BR} - t_{BF} $	—	—	100	μs	$C_L = 350 \text{ pF}$

TEMPERATURE SPECIFICATIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
TEMPERATURE RANGE						
Operating Ambient Temperature	T_A	-40	—	+85	$^\circ C$	
Storage Temperature	T_S	-65	—	+125	$^\circ C$	
PACKAGE THERMAL RESISTANCE						
44-lead PQFP	θ_{JA}	—	51	—	$^\circ C/W$	

Timing Waveforms



2.0 PIN DESCRIPTION

The details on the pins of HV66 44-lead PQFP are in [Table 2-1](#). Refer to [Package Type](#) for the location of pins.

TABLE 2-1: 44-LEAD PQFP PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	HVOUT11	High-voltage output
2	HVOUT12	High-voltage output
3	HVOUT13	High-voltage output
4	HVOUT14	High-voltage output
5	HVOUT15	High-voltage output
6	HVOUT16	High-voltage output
7	HVOUT17	High-voltage output
8	HVOUT18	High-voltage output
9	HVOUT19	High-voltage output
10	HVOUT20	High-voltage output
11	HVOUT21	High-voltage output
12	HVOUT22	High-voltage output
13	HVOUT23	High-voltage output
14	HVOUT24	High-voltage output
15	HVOUT25	High-voltage output
16	HVOUT26	High-voltage output
17	HVOUT27	High-voltage output
18	HVOUT28	High-voltage output
19	HVOUT29	High-voltage output
20	HVOUT30	High-voltage output
21	HVOUT31	High-voltage output
22	HVOUT32	High-voltage output
23	DATA OUT	Data output pin
24	GND	Supply ground
25	NC	No connection
26	$\overline{\text{BL}}$	Blanking pin
27	POL	Polarity pin
28	LE	Latch enable pin
29	VDD	Logic supply voltage
30	CLK	Clock pin
31	DIR	Direction pin
32	DATA IN	Data input pin
33	VPP	High-voltage power supply
34	BPOUT	Back plane output
35	HVOUT1	High-voltage output
36	HVOUT2	High-voltage output

TABLE 2-1: 44-LEAD PQFP PIN FUNCTION TABLE (CONTINUED)

Pin Number	Pin Name	Description
37	HVOUT3	High-voltage output
38	HVOUT4	High-voltage output
39	HVOUT5	High-voltage output
40	HVOUT6	High-voltage output
41	HVOUT7	High-voltage output
42	HVOUT8	High-voltage output
43	HVOUT9	High-voltage output
44	HVOUT10	High-voltage output

3.0 FUNCTIONAL DESCRIPTION

Follow the steps in [Table 3-1](#) to power up and power down the HV66.

TABLE 3-1: POWER-UP AND POWER-DOWN SEQUENCE

Power-up		Power-down	
Step	Description	Step	Description
1	Connect ground.	1	Remove V_{PP} . (Note 1)
2	Apply V_{DD} .	2	Remove all inputs.
3	Set all inputs (Data, CLK, EN, etc.) to a known state.	3	Remove V_{DD} .
4	Apply V_{PP} . (Note 1)	4	Disconnect ground.

Note 1: The V_{PP} should not drop below V_{DD} during operation.

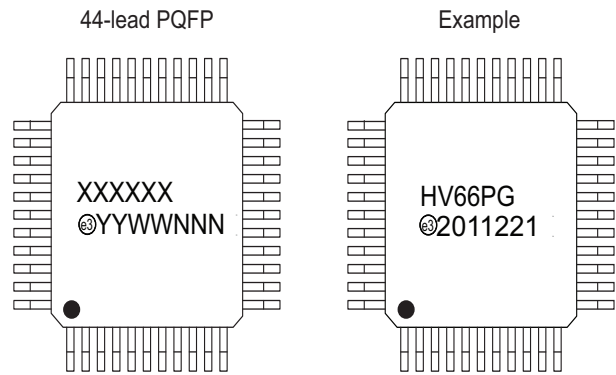
TABLE 3-2: TRUTH FUNCTION TABLE

Function	Inputs						Outputs			
	Data	CLK	LE	$\overline{BL}$	POL	DIR	Shift Register		High-voltage Output	Data Out
							1	2...32	1	2...32
Load S/R, R/L Shift	L or H	↑	L	Ignore	Ignore	H	Data → $Q_1... → Q_{32}$		Ignore	Q_{32}
	L or H	↑	L	Ignore	Ignore	L	$Q_1 ← ... Q_{32} ←$ Data		Ignore	Q_1
Load Latches	X	H or L	H	H	H	X	*...*		*...*	No Change
	X	H or L	H	H	L	X	*...*		*...*	No Change
Transparent Mode	L or H	↑	H	H	H	H	Data → $Q_1... → Q_{32}$		*...*	Q_{32}
	L or H	↑	H	H	L	H	Data → $Q_1... → Q_{32}$		*...*	Q_{32}
	L or H	↑	H	H	H	L	$Q_1 ← ... Q_{32} ←$ Data		*...*	Q_1
	L or H	↑	H	H	L	L	$Q_1 ← ... Q_{32} ←$ Data		*...*	Q_1
Blank Control	X	X	X	L	L	X	X		L...L	Ignore
	X	X	X	L	H	X	X		H...H	Ignore

Note: H = High-logic level
 L = Low-logic level
 X = Irrelevant
 Ignore = The state of the specific input or output is irrelevant to demonstrate the occurred event.
 ↑ = Low-to-high transition
 * = Dependent on the previous stage's state before the last CLK or last LE high

4.0 PACKAGE MARKING INFORMATION

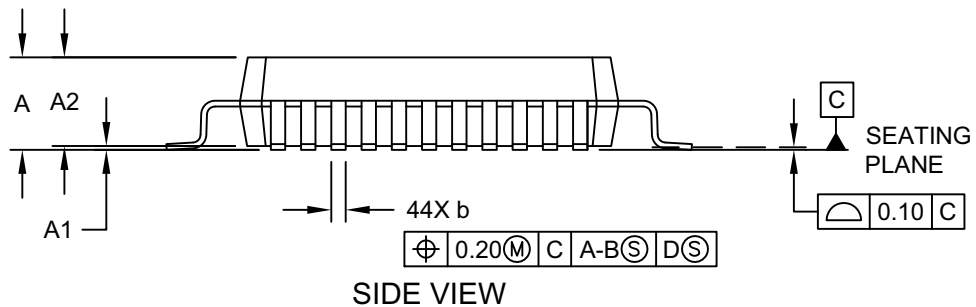
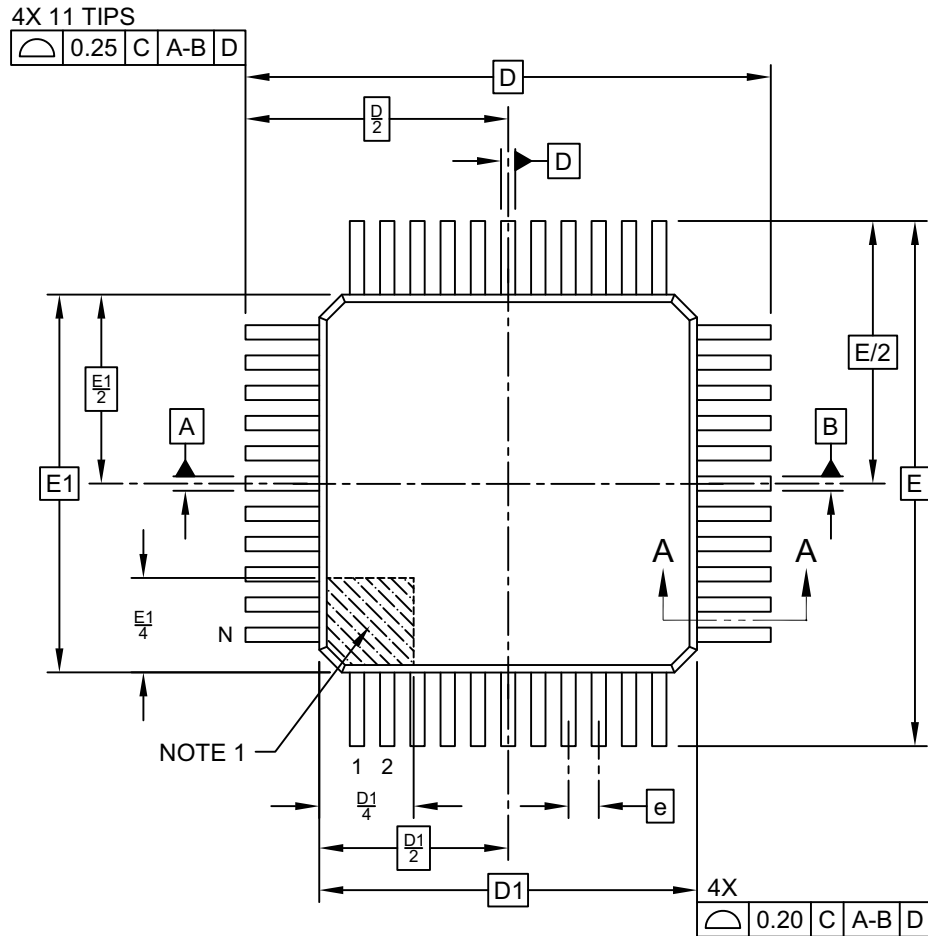
4.1 Packaging Information



Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	ⓔ3	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (ⓔ3) can be found on the outer packaging for this package.
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.	

44-Lead Plastic Metric Quad Flatpack (KW) - 10x10x2.0 mm Body, 3.9 mm Footprint [PQFP]

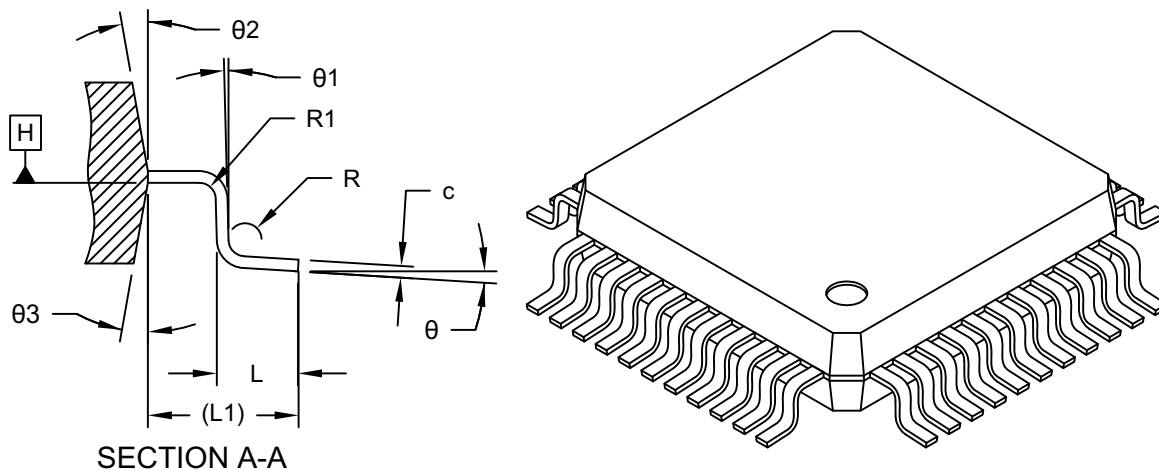
Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-119 Rev A Sheet 1 of 2

44-Lead Plastic Metric Quad Flatpack (KW) - 10x10x2.0 mm Body, 3.9 mm Footprint [PQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



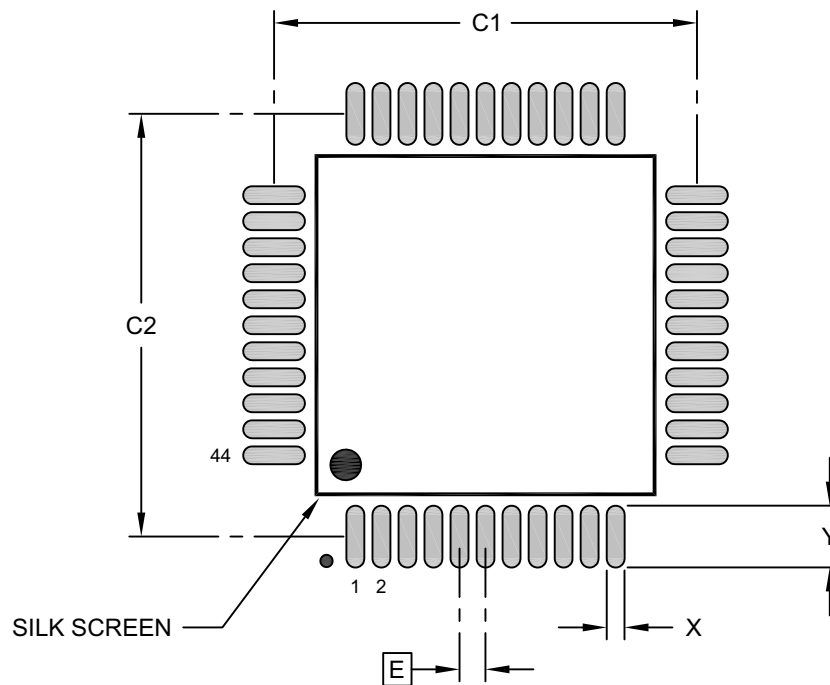
Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N	44		
Pitch	e	0.80 BSC		
Overall Height	A	-	-	2.35
Standoff §	A1	-	-	0.25
Molded Package Thickness	A2	1.95	2.00	2.10
Overall Length	D	13.90 BSC		
Molded Package Length	D1	10.00 BSC		
Overall Width	E	13.90 BSC		
Molded Package Width	E1	10.00 BSC		
Terminal Width	b	0.30	-	0.45
Terminal Thickness	c	0.11	-	0.23
Foot Length	L	0.73	0.88	1.03
Footprint	L1	1.95 REF		
Lead Bend Radius	R	0.13	-	0.30
Lead Bend Radius	R1	0.13	-	-
Foot Angle	θ	0°	3.5°	7°
Lead Angle	θ1	0°	-	-
Mold Draft Angle	θ2	5°	-	16°
Mold Draft Angle	θ3	5°	-	16°

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Chamfers at corners are optional; size may vary.
- Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
- Dimensioning and tolerancing per ASME Y14.5M
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 - REF: Reference Dimension, usually without tolerance, for information purposes only.
- § – Significant Characteristic

44-Lead Plastic Metric Quad Flatpack (KW) - 10x10x2.0 mm Body, 3.9 mm Footprint [PQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.80 BSC		
Contact Pad Spacing	C1		13.00	
Contact Pad Spacing	C2		13.00	
Contact Pad Width (Xnn)	X			0.55
Contact Pad Length (Xnn)	Y			1.90

Notes:

- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
- For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2119 Rev A

APPENDIX A: REVISION HISTORY

Revision B (February 2026)

- Removed the HV66PJ-G option and related information throughout the document.

Revision A (January 2020)

- Converted Supertex Doc # DSFP-HV66 to Microchip DS20005886B
- Removed “HVC MOS[®] Technology” from the Features section
- Changed the package marking format
- Updated the 44-lead PQFP PG M919 and 44-lead PLCC PJ M903 media types
- Made minor changes throughout the document

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