
Implementing SD[™] Express with PCI1xxxx Controllers

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1.0 INTRODUCTION

SD[™] Express cards use a PCIe[®] physical interface and NVMe protocol to allow for faster transfer speeds and simplified integration into PCIe systems, including those implemented with Microchip PCI11414/PCI11400/PCI11010/PCI11010/PCI12000 bridge controllers.

This application note describes the important requirements and system design aspects essential for allowing SD Express connectivity with the PCI1xxxx.

1.1 Sections

This document covers the following topics:

- [Section 2.0, SD[™] Express Background](#)
- [Section 3.0, Integrating SD Express with PCI1xxxx Products](#)
- [Section 4.0, PCI1xxxx + SD Express Sample Schematics](#)

1.2 References

Consult the following documents when using this application note:

- *PCI12000 Data Sheet*
- *PCI11010 Data Sheet*
- *PCI11101 Data Sheet*
- *PCI11400 Data Sheet*
- *PCI11414 Data Sheet*
- PCI Express[®] Base Specification Revision 4.0, Version 1.0 9 (may require access)
- SD Specification Version 9.0 (may require access)

2.0 SD™ EXPRESS BACKGROUND

2.1 SD Specification 7.0

The SD Express bus was released in June 2018 with SD specification 7.0. It uses a single PCIe lane to provide Full-duplex 985 MB/s transfer speed. Supporting cards must also implement the NVM Express storage access protocol. The Express bus can be implemented by SDHC™, SDXC™, and SDUC™ cards. For legacy application use, SD Express cards must also support High-Speed bus and UHS-I bus. The express bus reuses the pin layout of UHS-II cards and reserves the space for additional two pins that may be introduced in the future.

2.2 SD Specification 8.0

Released in May 2020, the Version 8.0 of the SD Specification added SD Express support for two PCIe lanes. This is enabled through an additional row of contacts. The speeds were also increased to support PCIe 4.0 transfer rates.

2.3 Speed Comparisons

The varied DS speeds are detailed in [Table 1](#).

TABLE 1: SD™ EXPRESS SPEED COMPARISON

PCIe® Speed	Lanes	Specifications	Speed
3.1 at 8 Gbps	x1	SD v7.0	985 MB/s
	x2	SD v8.0	1970 MB/s
4.0 at 8 Gbps	x1	SD v8.0	1970 MB/s
	x2	SD v8.0	3940 MB/s

Note 1: PCI1xxxx only supports 3.1 x1 speeds.

2.4 SD Express Cards and Pinout

[Figure 1](#) shows examples of standard and microSD™ Express Cards and their pinouts. Refer to [Table 2](#) for the pin details.

FIGURE 1: SD™ EXPRESS CARD FORM FACTORS

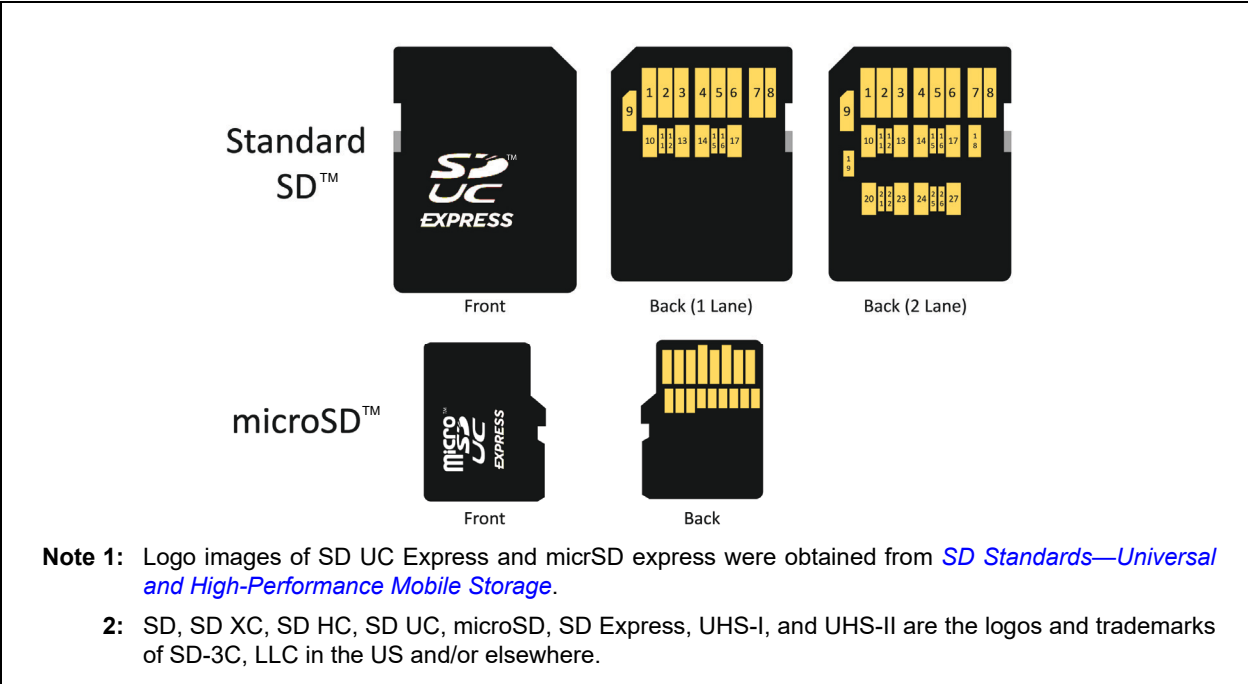


TABLE 2: STANDARD/MICROSD™ EXPRESS 1-LANE CARD PINS

Pin Number	Name	Description
1	PERST#	PCIe functional Reset
2	CMD (legacy mode)	Legacy SD Command. Used in backward compatibility mode only.
3	VSS1	GND
4	VDD1	3.3V supply
5	CLK (legacy mode)	Legacy SD Clock. Used in backward compatibility mode only.
6	VSS2	GND
7	REFCLK+	Card differential clock input
8	REFCLK-	Card differential clock input
9	CLKREQ#	REF CLK request signal. Asserted low to request supply of clock on REFCLK +/- pins.
10	VSS3	GND
11	PCIe TX-	Card differential data input
12	PCIe TX+	Card differential data input
13	VSS4	GND
14	VDD2	1.8V supply
15	PCIe RX-	Card differential data output
16	PCIe RX+	Card differential data output
17	VSS5	GND

TABLE 3: STANDARD SD™ EXPRESS 2-LANE CARD (ADDITIONAL PINS ONLY)

Pin Number	Name	Description
18	VDD3	Optional 1.2V supply
19	VDD1a	3.3V supply
20	VSS6	GND
21	PCIe TX1-	Card differential data input (second lane)
22	PCIe TX1+	Card differential data input (second lane)
23	VSS7	GND
24	VDD2a	1.8V supply
25	PCIe RX1-	Card differential data output (second lane)
26	PCIe RX1+	Card differential data output (second lane)
27	VSS8	GND

2.5 SD Express Card Slot

In addition to supporting all the pins of an SD Express card, SD Express card slots have the following:

- A metal shield connected to GND on the PCB layout
- A card detect pin shorted to GND when a card is physically inserted into the slot
- A write-protect detect pin (standard SD card slots only), which detects the position of the “Lock” switch. The SD controller reads the state of the pin to discover if writing to the card is permitted.

2.6 SD Express Card Power Requirements

SD Express cards require 3.3V and 1.8V power rails. Refer to [Table 4](#).

Note: An optional 1.2V rail named VDD3 is also specified. This can be used instead of the 1.8V rail of both the SD Express host and card that support it.

TABLE 4: SD™ EXPRESS CARD POWER REQUIREMENTS

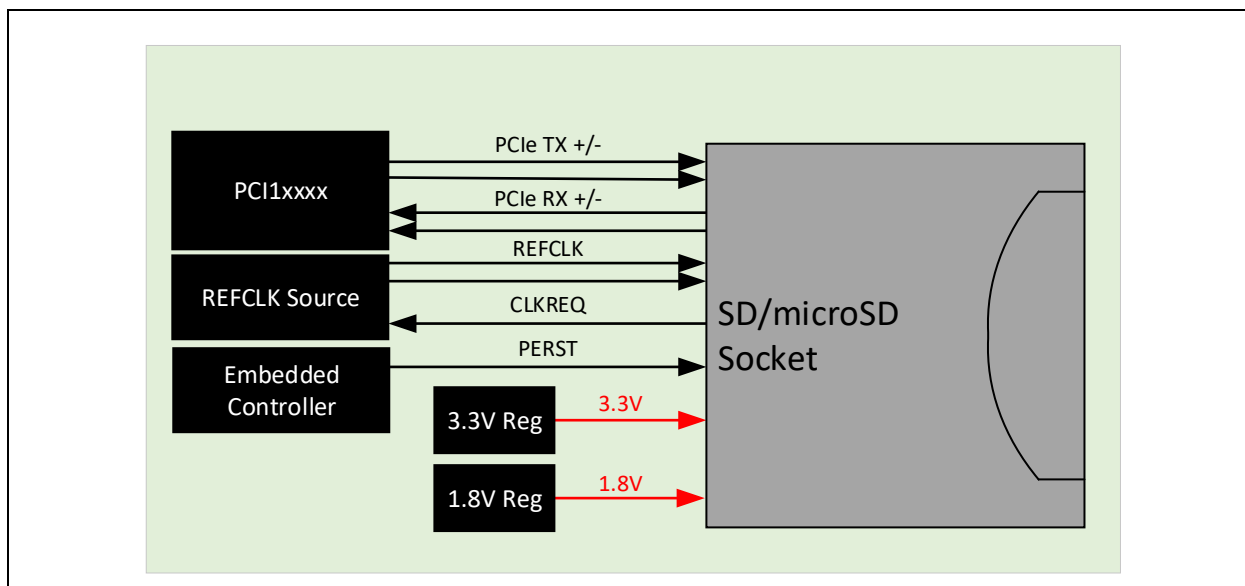
Power Rail	Range	Amperage (Peak)	Amperage (Normal)
VDD1	2.7V to 3.6V	600 mA	400 mA
VDD2	1.7V to 1.95V	600 mA	400 mA

3.0 INTEGRATING SD EXPRESS WITH PCI1XXXX PRODUCTS

3.1 PCIe® Connections

PCI1xxxx downstream ports support PCIe v3.1 speeds (2.5/5/8Gbps). SD Express slots and cards which support PCIe v4.0 and dual lane implementations operate in backward compatibility modes at reduced speed/lane width to align PCI1xxxx capabilities. See [Figure 2](#).

FIGURE 2: PCI1XXXX SD™ EXPRESS BLOCK DIAGRAM



3.2 Power Sequencing

SD Express cards require that a 3.3V power rail be supplied and become stable before the 1.8V power supply is enabled. The SD Express card slot has an insertion detection pin, which is shorted to ground when a card is inserted into the slot. The slot can be used to control the 3.3V and 1.8V power rails.

SD Express cards use the presence of the 1.8V rail to determine when to operate in SD Express mode and enable PCIe communication.

3.3 Hot-Plug Capability

Hot-Plug capability is not supported with PCI1xxxx SD Express implementations. The SD Express card must be inserted into the slot before the PCI1xxxx is enabled and connected to a PCIe Host.

3.4 Compatibility with Legacy SD Cards

PCI1xxxx does not support legacy SD protocol and legacy SD cards.

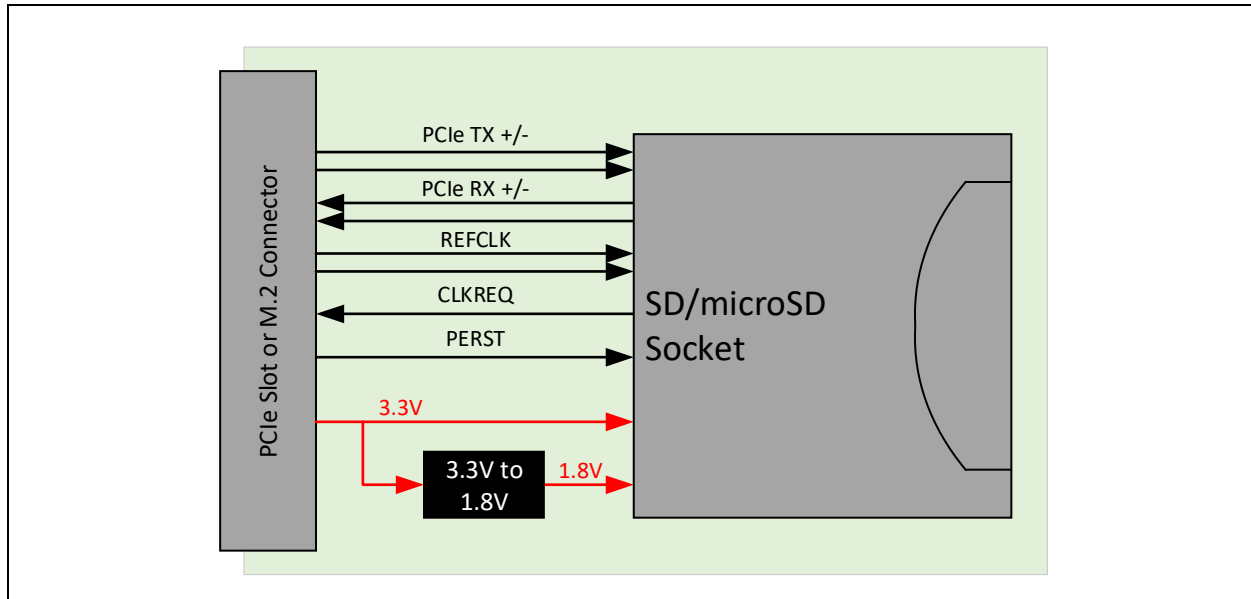
3.5 Drivers

SD Express uses standard NVME drivers which are included in most operating system distributions. The PCI1xxxx does not require additional device-specific or customized drivers or software to connect to SD Express cards.

3.6 PCIe Slot and M.2 Connector Adaptation

The PCI1xxxx can connect to SD Express through a standard PCIe slot or M.2 connector. (See [Figure 3](#).) The connections are largely the same as in a directly connected case. PCIe slots do not have provisions for 1.8V power pins, so a 1.8V regulator must be included in the adapter card.

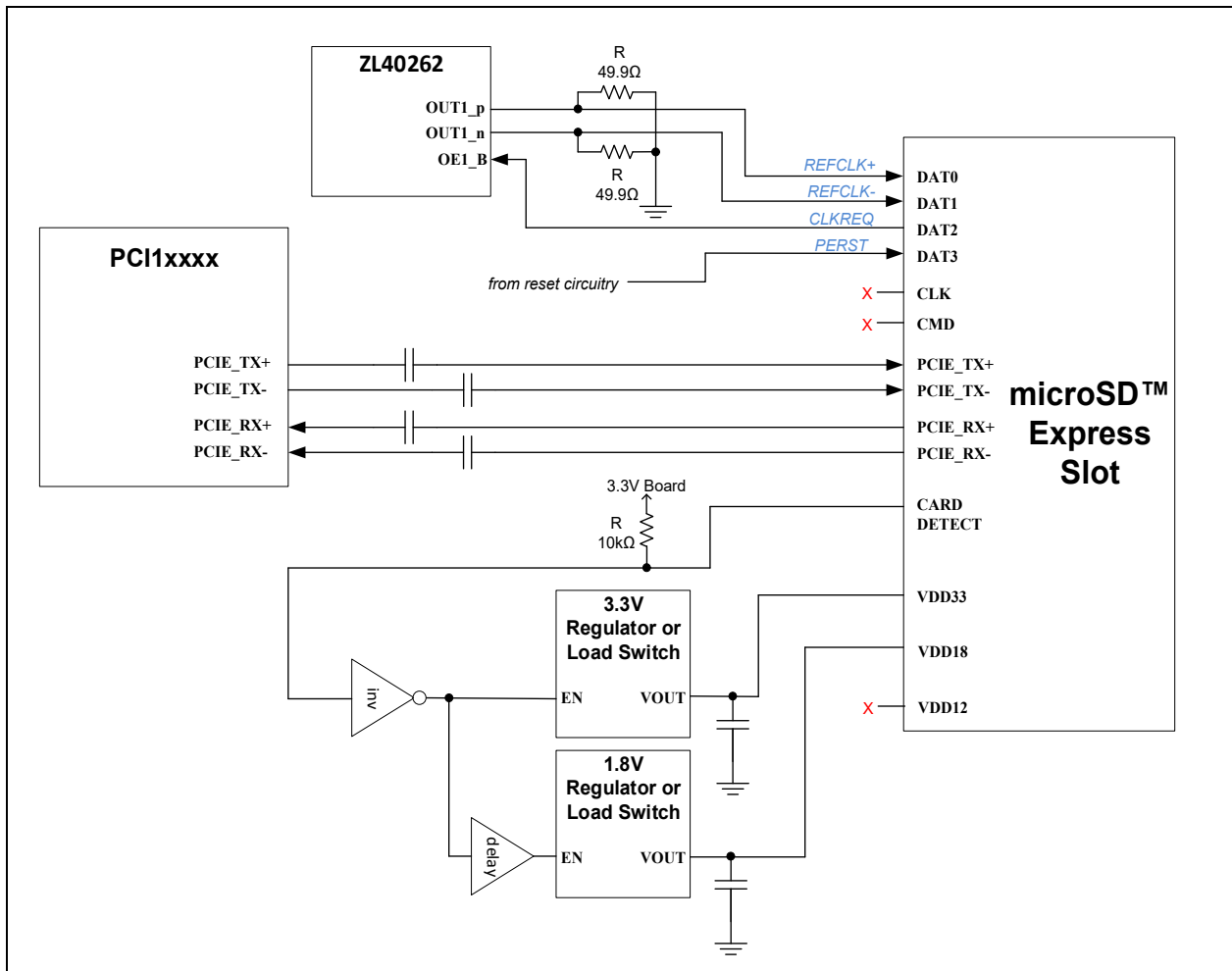
FIGURE 3: PCIE SLOT / M.2 CONNECTOR ADAPTER



4.0 PCI1XXXX + SD EXPRESS SAMPLE SCHEMATICS

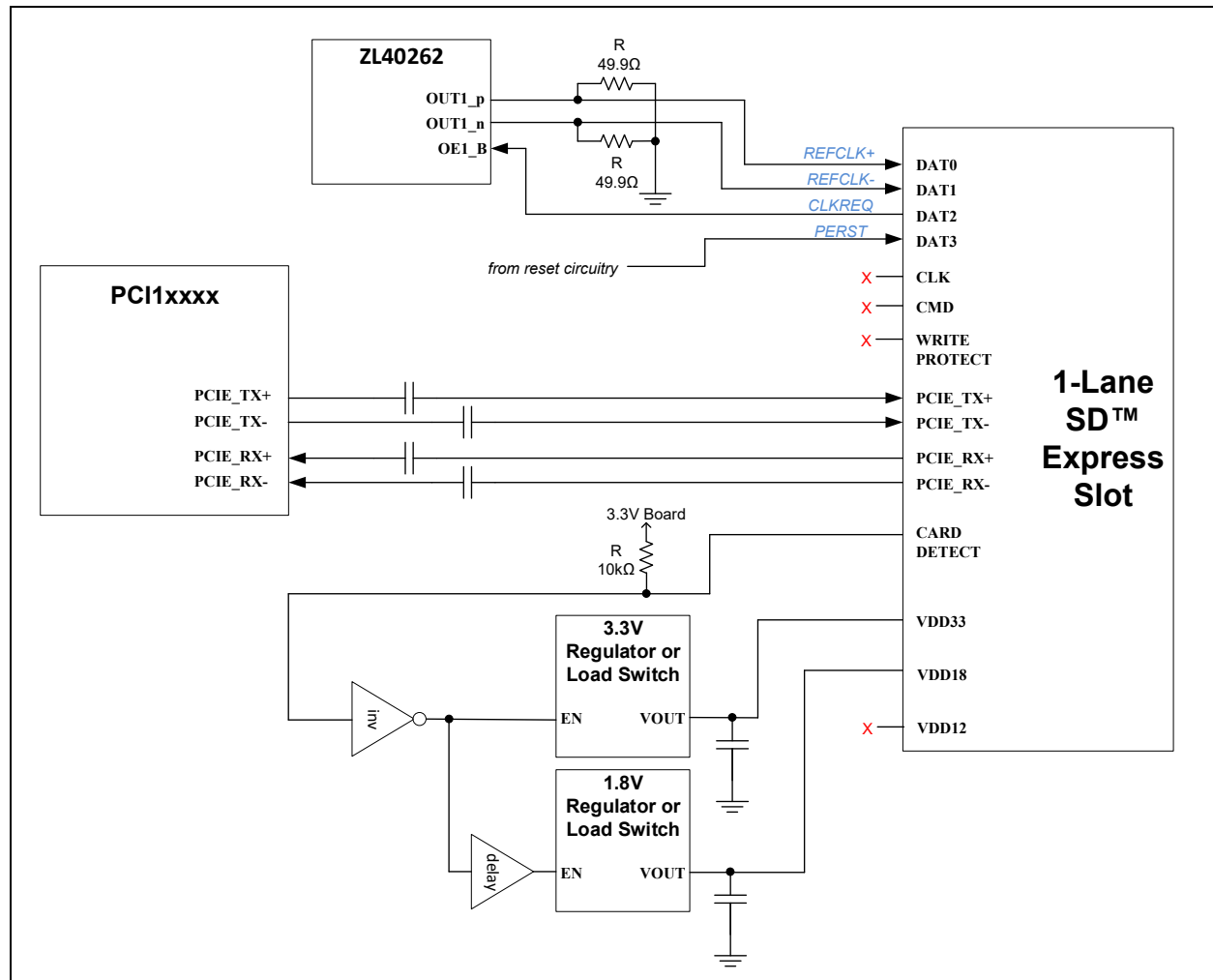
A sample schematic implementation of the PCI1xxxx connecting to a microSD Express slot is shown in [Figure 4](#).

FIGURE 4: MICROSD™ EXPRESS CARD FORM FACTORS



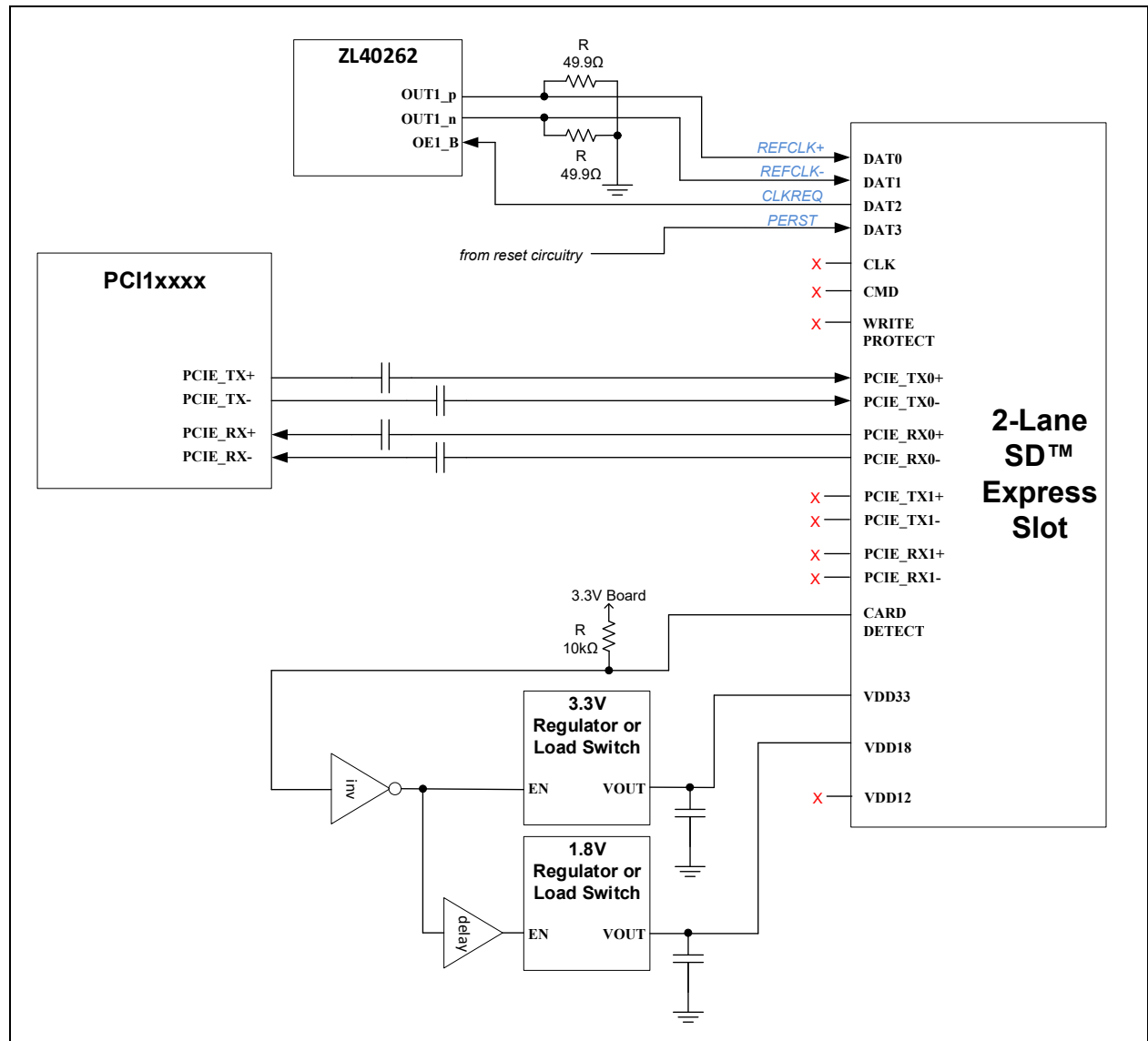
A sample schematic implementation of the PCI1xxxx connecting to one-lane SD Express slot is illustrated in [Figure 5](#).

FIGURE 5: ONE-LANE SD™ EXPRESS CARD FORM FACTORS



A sample schematic implementation of PCI1xxxx connecting to a two-lane SD Express slot is shown in [Figure 6](#).

FIGURE 6: TWO-LANE SD™ EXPRESS CARD FORM FACTORS



APPENDIX A: APPLICATION NOTE REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00005298B (10-25-2024)	All	Removed the “Confidential” marking from the document. Updated heading format.
DS00005298A (02-29-2024)	Initial release	

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