

7.9 GHz–11 GHz 12W BARE DIE GaN POWER AMPLIFIER

ICP1040



Product Overview

MICROCHIP’s ICP1040 is a two-stage MMIC power amplifier in bare die form, fabricated using GaN on SiC technology. ICP1040 operates from 7.9 GHz – 11GHz with 41 dBm output power, 40% typical PAE and 22 dB small signal gain. ICP1040 is well suited to commercial and defense applications.

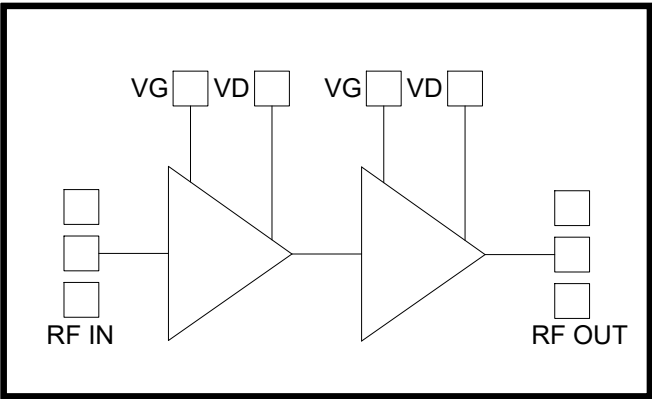
Key Features

- **Frequency Range:** 7.9 GHz – 11GHz
- **P_{out}:** 41 dBm, Pulsed (100 μs, 10%) and P_{in} = 24 dBm
- **P_{out}:** 41 dBm, CW and P_{in} = 24 dBm
- **PAE:** 40%
- **Small signal gain:** 22 dB
- **Bias:** V_D = 28V, I_{DQ} = 100 mA
- **Technology:** GaN on SiC
- **Lead-free and RoHS compliant**
- **Pulsed or CW operation**
- **Die Size:** 3.08 mm × 1 mm
- **Integrated power detector**

Applications

- Test and measurement
- Aerospace and defense
- Point-to-point radio

Functional Block Diagram



Electrical Specifications

Parameter	Conditions	Min.	Typ.	Max.	Units
Frequency		7.9		11	GHz
Output power at P _{sat} (CW)	P _{in} = 24 dBm		41		dBm
Gain at P _{sat} (CW)	P _{in} = 24 dBm		15		dB
PAE at P _{sat} (CW)	P _{in} = 24 dBm		38		%
Drain current at P _{sat}			1200	1400	mA
Gate voltage (V _G) for IDQ		-2.2		-2.6	V
Small signal gain			22		dB
Input return loss			8		dB
IM3	P _{out} =40 dBm		-20		dBc
Output power at P _{sat} (pulsed)	P _{in} = 24 dBm		41		dBm
Gain at P _{sat} (pulsed)	P _{in} = 24 dBm		15		dB
PAE at P _{sat} (pulsed)	P _{in} = 24 dBm		40		%

Test Conditions: V_D=28V, I_{DQ}=100mA, T_A=25°C

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1. Electrical Specification

1.1. Absolute Maximum Ratings

Parameter	Absolute Maximum
Drain voltage (V_D)	32V
Drain - Source Breakdown Voltage (V_{DSBKD})	120V
Gate voltage (V_G)	-8 to 1.5V
Gate voltage (I_G)	3.75 mA
Drain current (CW) $T_A = 25\text{ }^{\circ}\text{C}$	2.3A
Power dissipation (CW) $T_A = 25\text{ }^{\circ}\text{C}$	55.5W
Power dissipation (CW) $T_A = 85\text{ }^{\circ}\text{C}$	42.2W
CW input power 50 Ω $T_A = 25\text{ }^{\circ}\text{C}$	+30 dBm
Channel temperature	275 $^{\circ}\text{C}$
Storage temperature	-65 $^{\circ}\text{C}$ to +150 $^{\circ}\text{C}$
Input power VSWR (3:1), $V_D = 24\text{V}$, $I_{DQ} = 150\text{ mA}$	30 dBm
Eutectic die attach temperature (30s)	320 $^{\circ}\text{C}$

Thermal and Reliability

Parameter	Value
Thermal resistance	4.5 $^{\circ}\text{C/W}$

- Assumes silver sintered epoxy attach (15 μm thick) mounted on CuMo carrier.
- Base temperature is assumed at the top of the CuMo carrier.
- Thermal resistance calculated using IR measurement of the channel temperature.

Note:

Exceeding any one or combination of these limits may cause permanent damage to this device.

Microchip Technology Inc. does not recommend sustained operation near these survivability limits.

1.2. Small Signal Performance

Typical Data over T_A

Test conditions: $V_D = 28V$, $I_{DQ} = 100\text{ mA}$

Figure 1-1. S_{21}

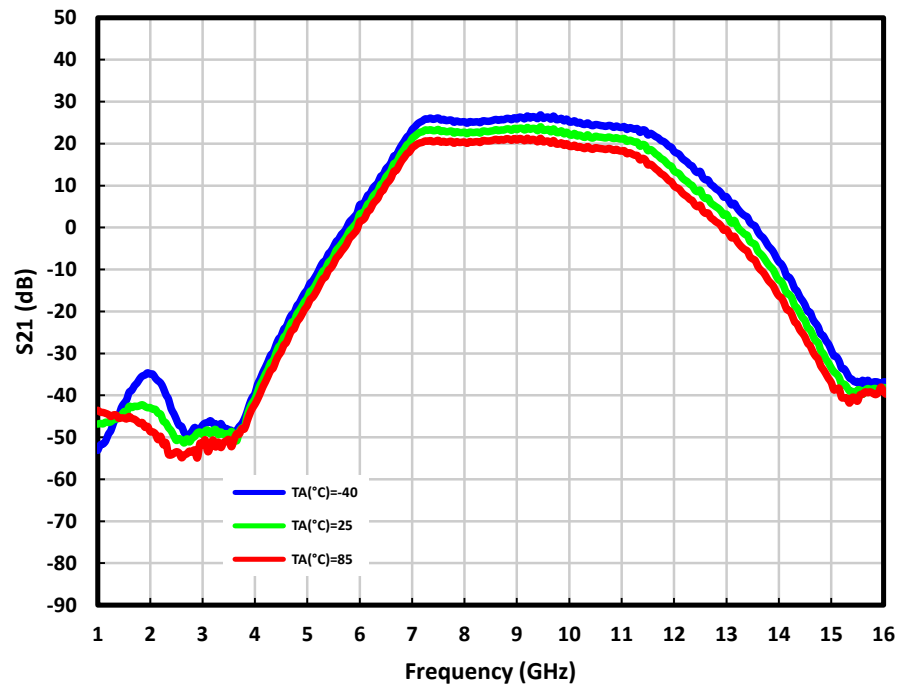


Figure 1-2. S_{11}

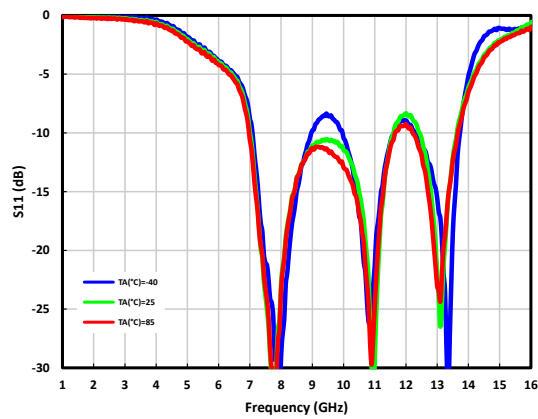
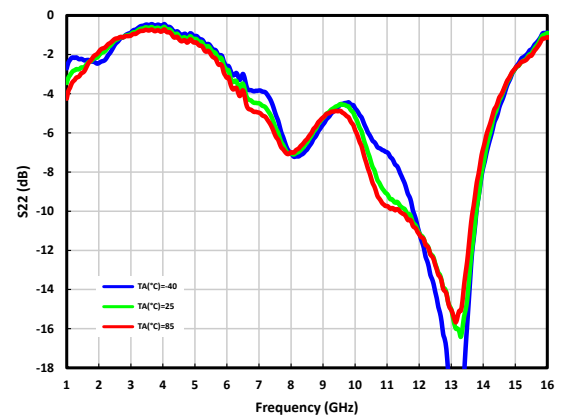


Figure 1-3. S_{22}



Typical Data over T_A

Test conditions: $V_D = 24V$, $I_{DQ} = 100\text{ mA}$

Figure 1-4. S_{21}

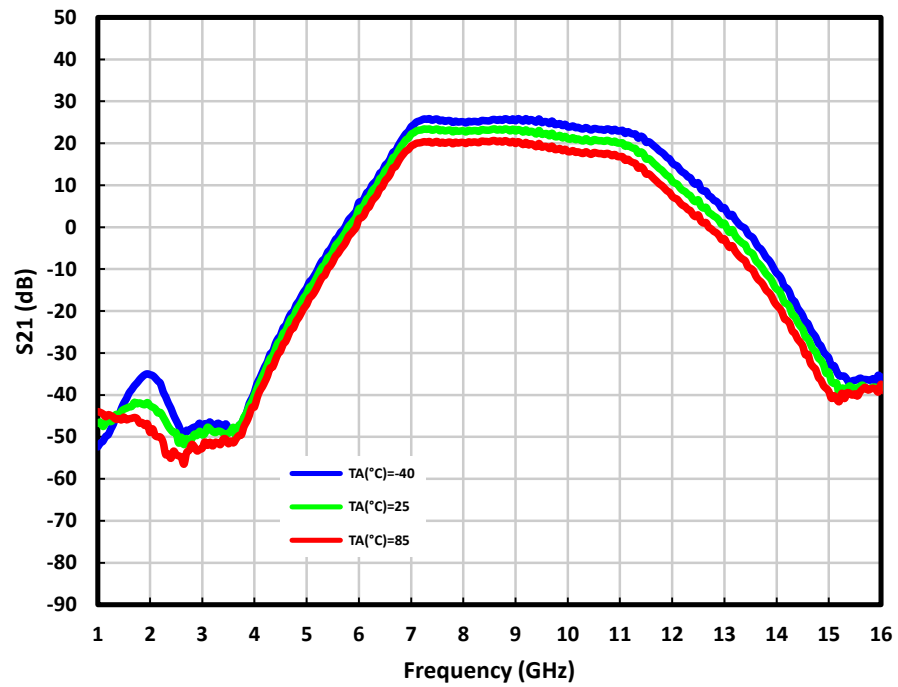


Figure 1-5. S_{11}

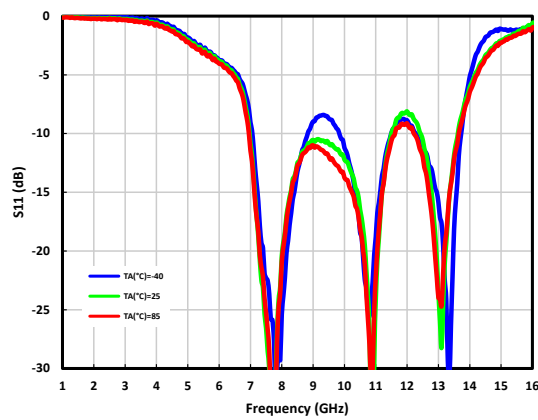
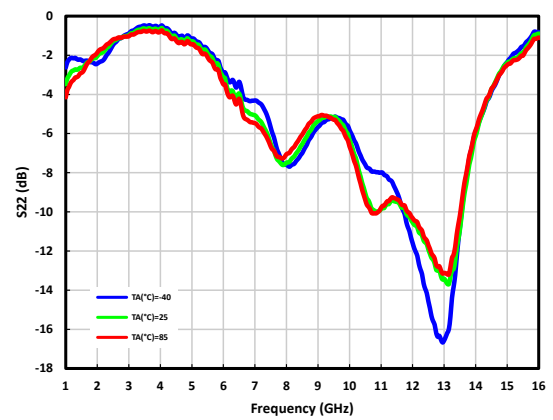


Figure 1-6. S_{22}



1.3. Large Signal Performance

Typical CW power data

Test Conditions: $V_D = 28V$, $I_{DQ} = 100\text{ mA}$, $T_A = 25\text{ }^\circ\text{C}$, CW

Figure 1-7. P_{out} vs. P_{in}

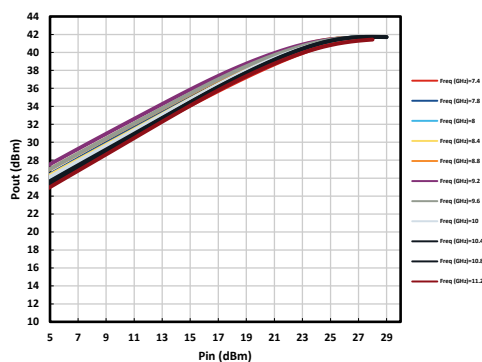


Figure 1-8. Gain vs. P_{out}

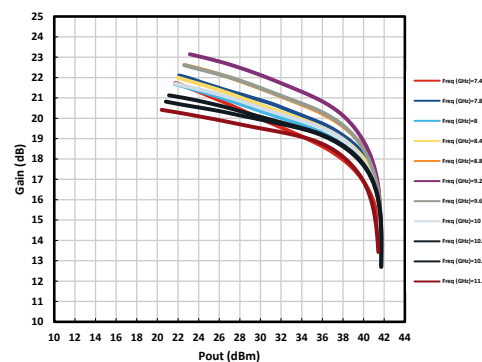


Figure 1-9. PAE vs. P_{out}

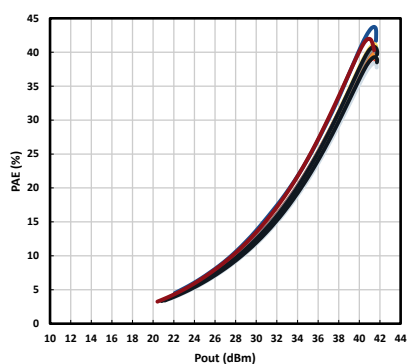


Figure 1-10. I_d vs. P_{out}

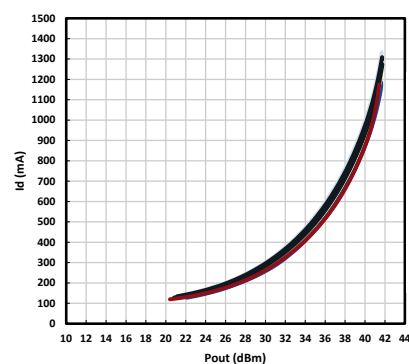


Figure 1-11. V_{diff} ($V_{REF} - V_{DET}$) vs. P_{out}

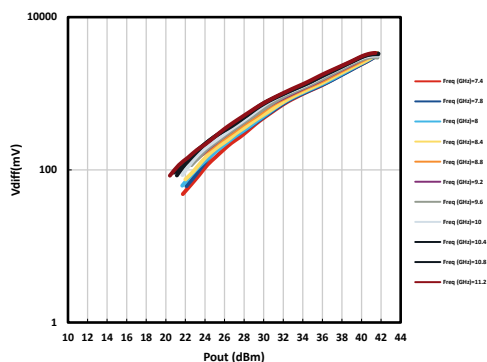


Figure 1-12. P_{out} vs. Freq

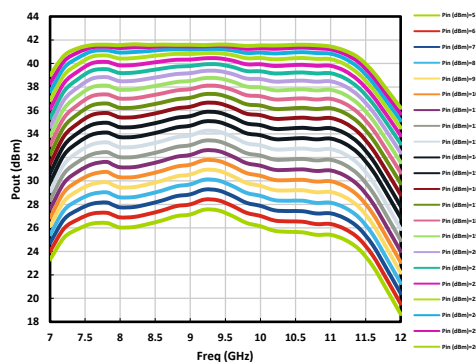
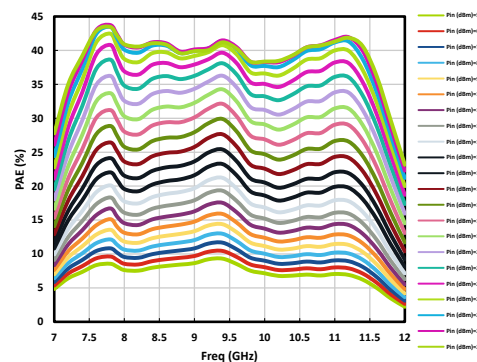


Figure 1-13. PAE vs. Freq



Typical CW Power Data over temperature

Test Conditions: $V_D = 28V$, $I_{DQ} = 100\text{ mA}$, CW

Figure 1-14. P_{out} vs P_{in} at 8GHz

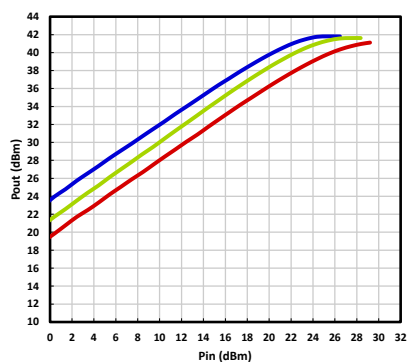


Figure 1-15. Gain vs P_{out} at 8GHz

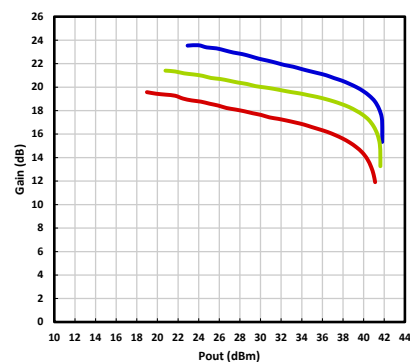


Figure 1-16. PAE vs P_{out} at 8GHz

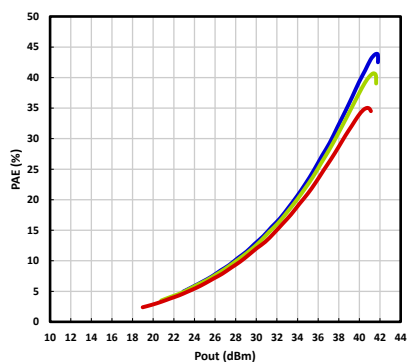


Figure 1-17. I_d vs P_{out} at 8GHz

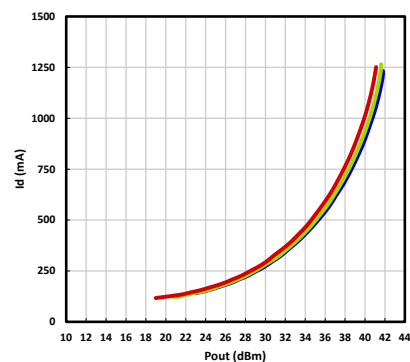


Figure 1-18. V_{diff} ($V_{REF} - V_{DET}$) vs P_{out} at 8GHz

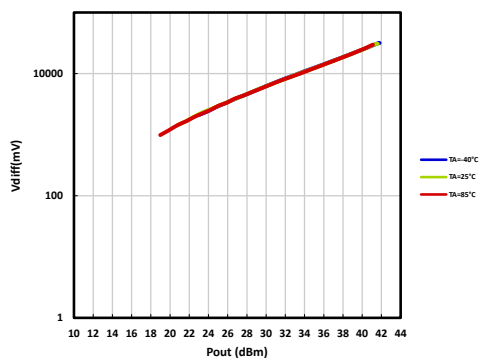


Figure 1-19. P_{out} vs P_{in} at 9.2GHz

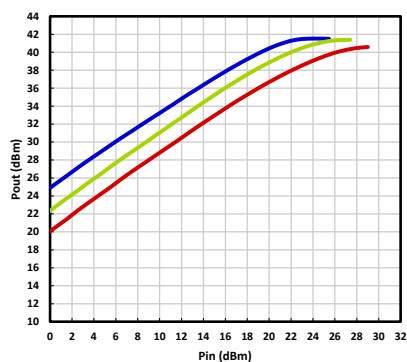


Figure 1-20. Gain vs P_{out} at 9.2GHz

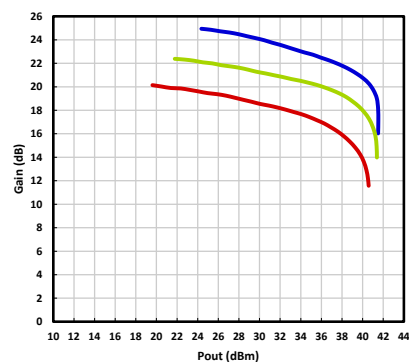


Figure 1-21. PAE vs P_{out} at 9.2GHz

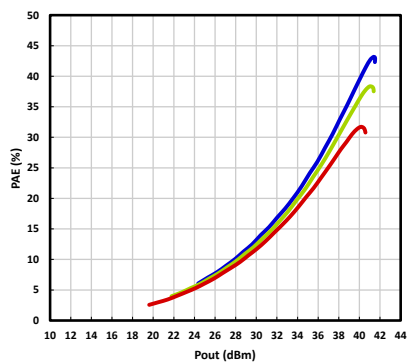


Figure 1-22. I_d vs P_{out} at 9.2GHz

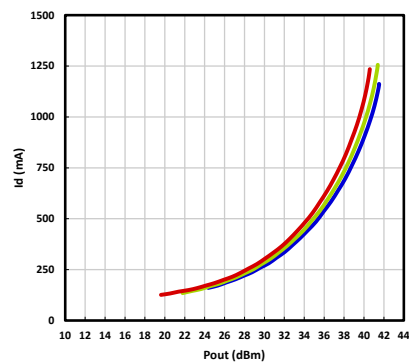


Figure 1-23. V_{diff} ($V_{REF} - V_{DET}$) vs P_{out} at 9.2GHz

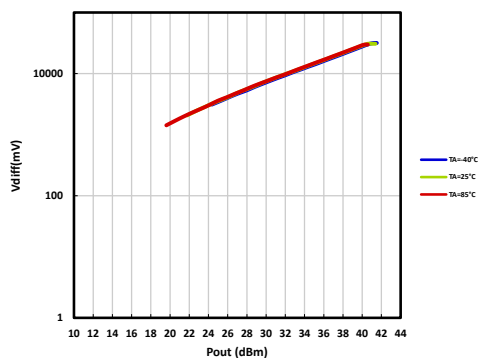


Figure 1-24. P_{out} vs P_{in} at 11.2GHz

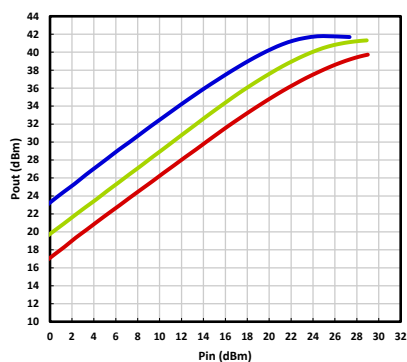


Figure 1-25. Gain vs P_{out} at 11.2GHz

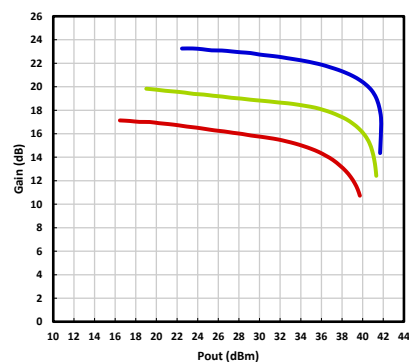


Figure 1-26. PAE vs P_{out} at 11.2GHz

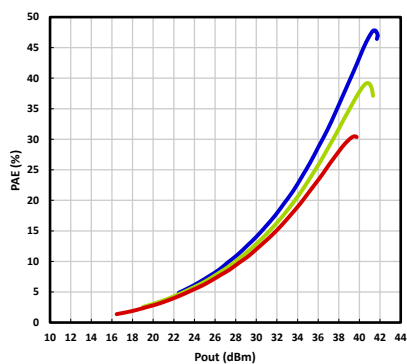


Figure 1-27. I_d vs P_{out} at 11.2GHz

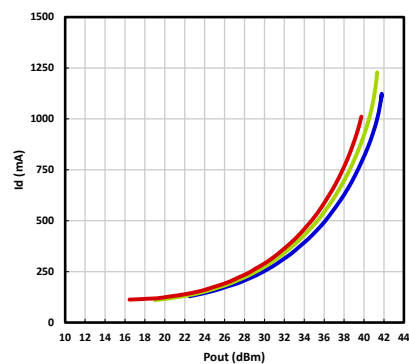
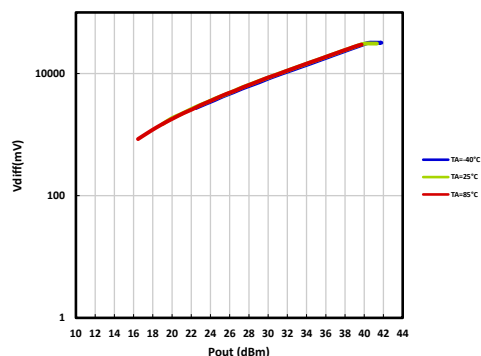


Figure 1-28. V_{diff} ($V_{REF} - V_{DET}$) vs P_{out} at 11.2GHz



Typical CW Power Data over V_d

Test Conditions: $V_D = 20, 24$ and $28V$, $I_{DQ} = 100$ mA, $T_A = 25$ °C, CW

Figure 1-29. Gain vs P_{out} at 8GHz

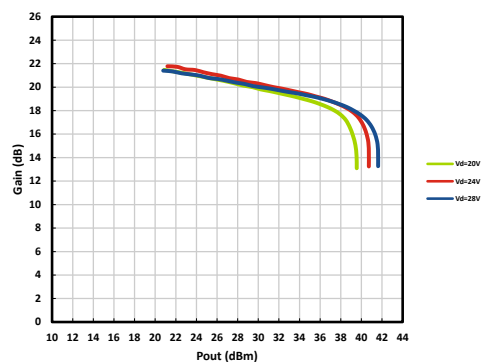


Figure 1-30. PAE vs P_{out} at 8GHz

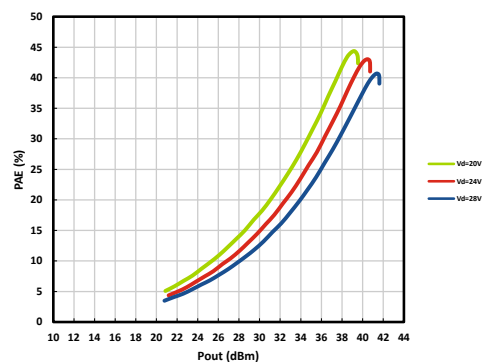


Figure 1-31. Gain vs P_{out} at 9.2GHz

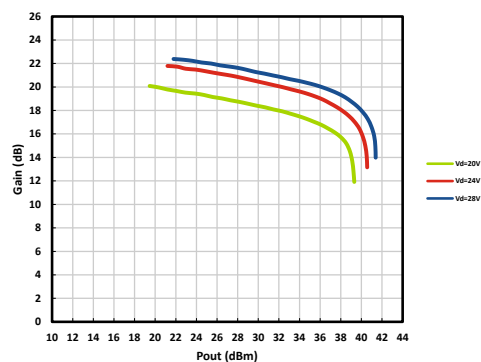


Figure 1-32. PAE vs P_{out} at 9.2GHz

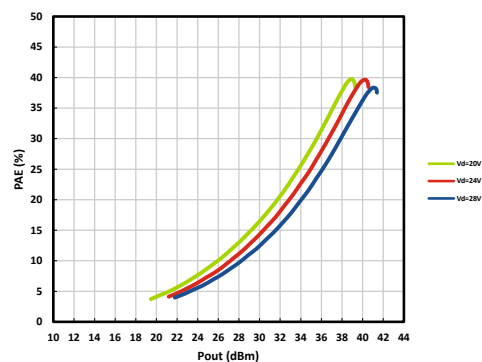


Figure 1-33. Gain vs Pout at 11.2GHz

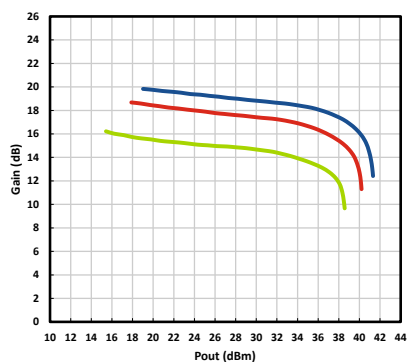
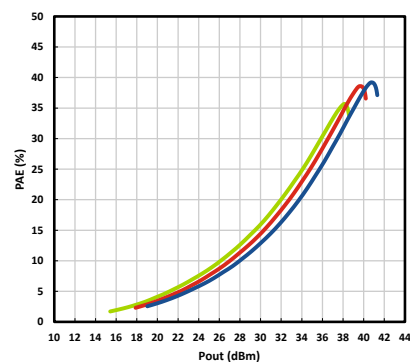


Figure 1-34. PAE vs Pout at 11.2GHz



Typical CW Power Data over I_{DQ}

Test Conditions: $V_D = 28V$, $I_{DQ} = 50, 100$ and 200 mA, CW

Figure 1-35. Gain vs Pout at 8GHz

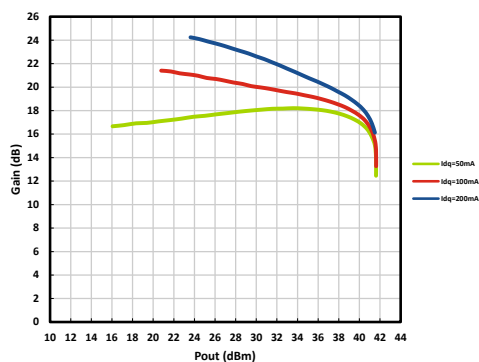


Figure 1-36. PAE vs Pout at 8GHz

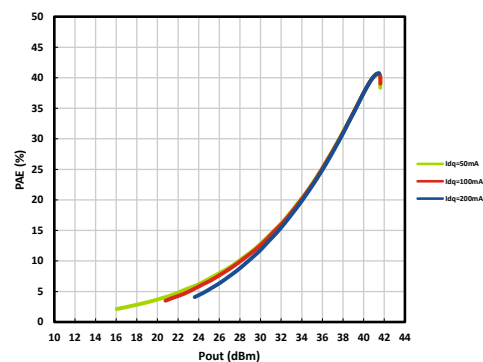


Figure 1-37. Gain vs Pout at 9.2GHz

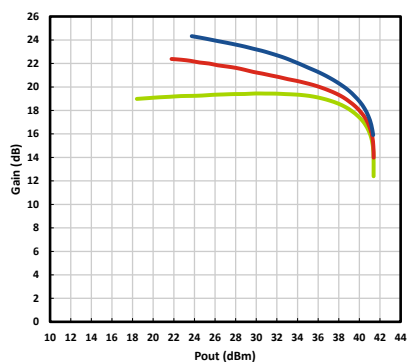


Figure 1-38. PAE vs Pout at 9.2GHz

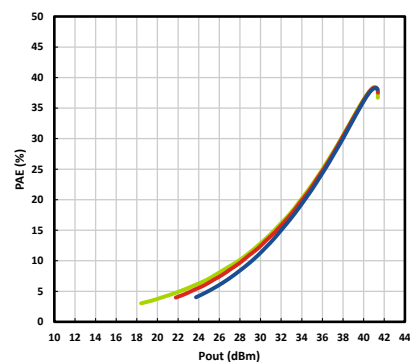


Figure 1-39. Gain vs Pout at 11.2GHz

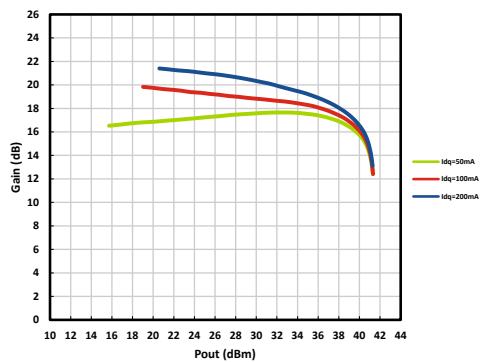
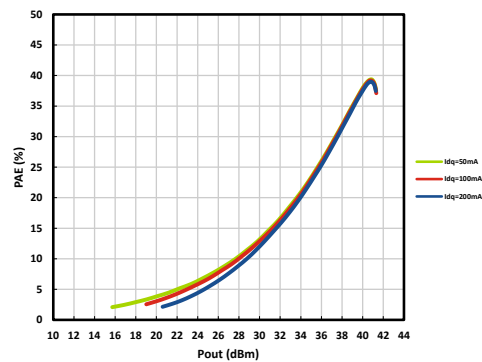


Figure 1-40. PAE vs Pout at 11.2GHz



Typical Pulsed power data

Test Conditions: $V_D = 28V$, $I_{DQ} = 100\text{ mA}$, $T_A = 25\text{ }^{\circ}\text{C}$, Pulsed 10% Duty Cycle 1 ms period

Figure 1-41. P_{out} vs. P_{in}

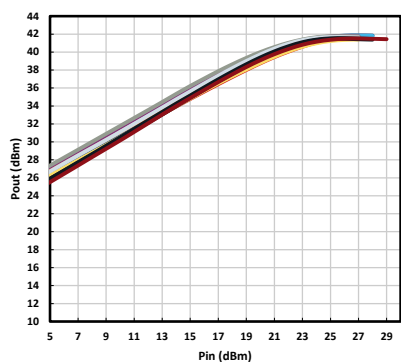


Figure 1-42. Gain vs. P_{out}

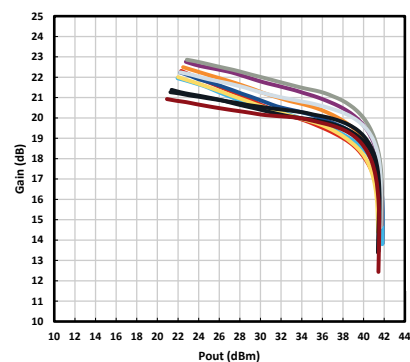


Figure 1-43. PAE vs. P_{out}

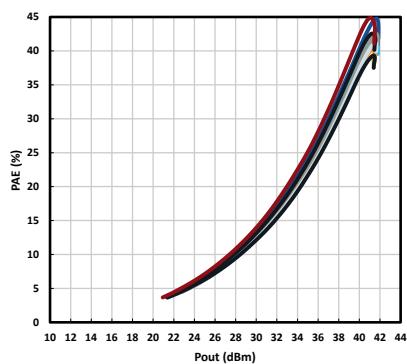


Figure 1-44. I_d vs. P_{out}

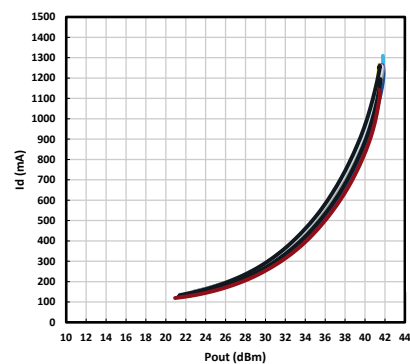


Figure 1-45. V_{diff} ($V_{REF} - V_{DET}$) vs. P_{out}

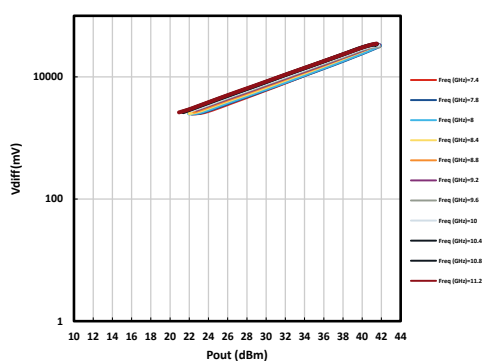


Figure 1-46. P_{out} vs. Freq

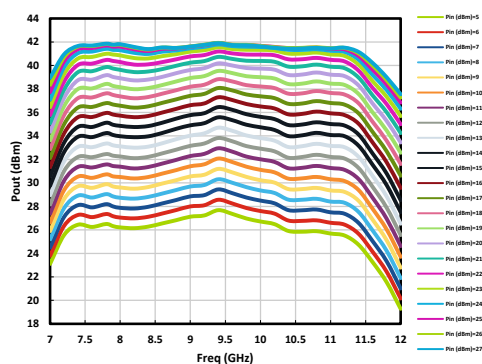
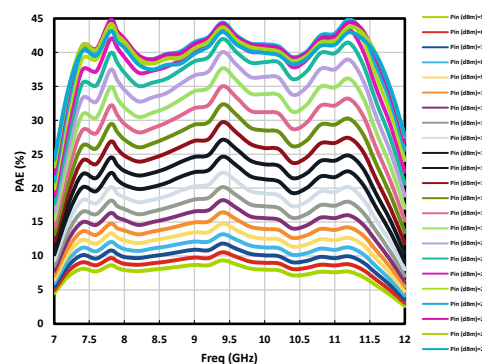


Figure 1-47. PAE vs. Freq



Typical Pulsed Power Data over temperature

Test Conditions: $V_D = 28V$, $I_{DQ} = 100\text{ mA}$, Pulsed 10% Duty Cycle 1 ms period

Figure 1-48. P_{out} vs P_{in} at 8GHz

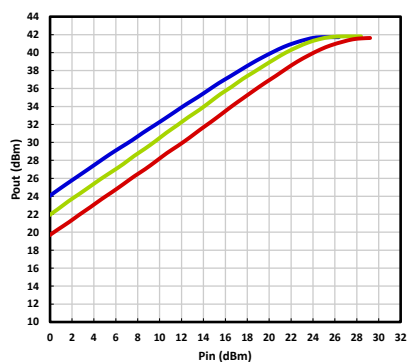


Figure 1-49. Gain vs P_{out} at 8GHz

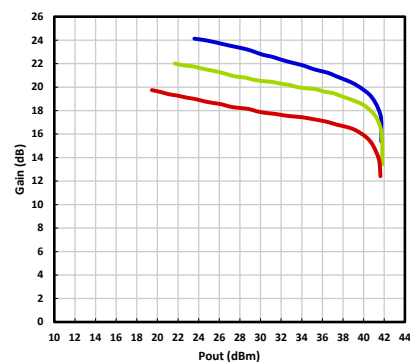


Figure 1-50. PAE vs P_{out} at 8GHz

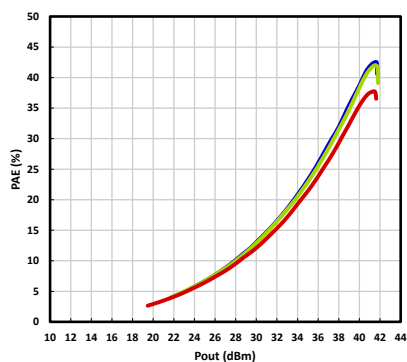


Figure 1-51. I_d vs P_{out} at 8GHz

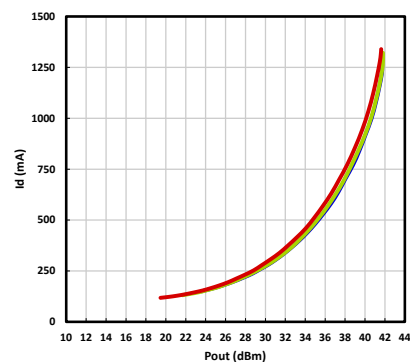


Figure 1-52. V_{diff} ($V_{REF} - V_{DET}$) vs P_{out} at 8GHz

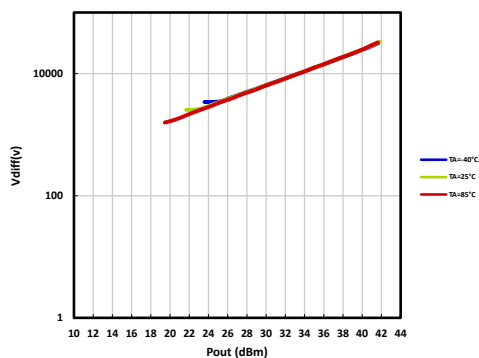


Figure 1-53. P_{out} vs P_{in} at 9.2GHz

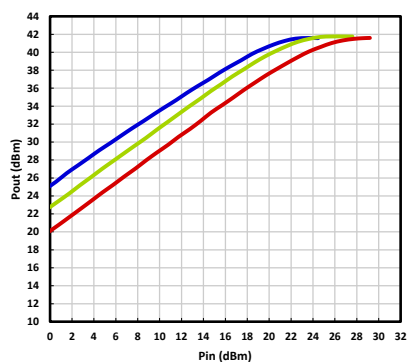


Figure 1-54. Gain vs P_{out} at 9.2GHz

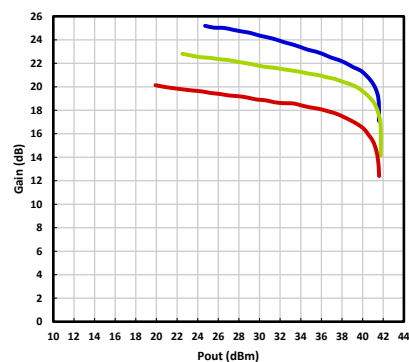


Figure 1-55. PAE vs P_{out} at 9.2GHz

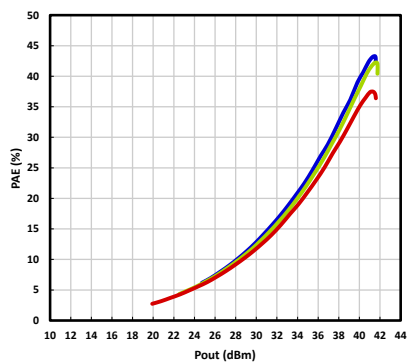


Figure 1-56. I_d vs P_{out} at 9.2GHz

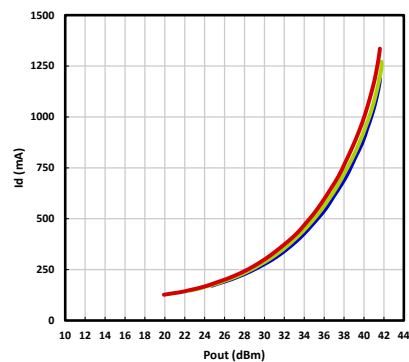


Figure 1-57. V_{diff} ($V_{REF} - V_{DET}$) vs P_{out} at 9.2GHz

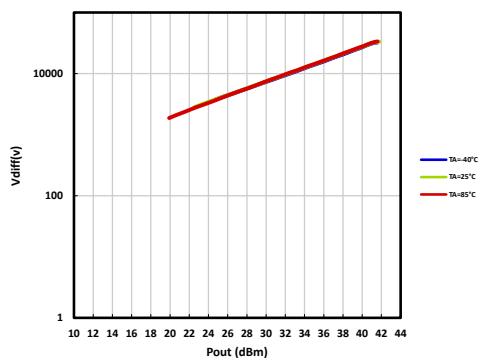


Figure 1-58. P_{out} vs P_{in} at 11.2GHz

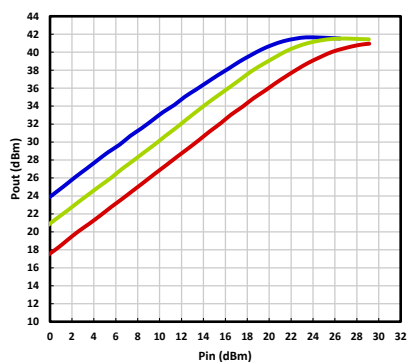


Figure 1-59. Gain vs P_{out} at 11.2GHz

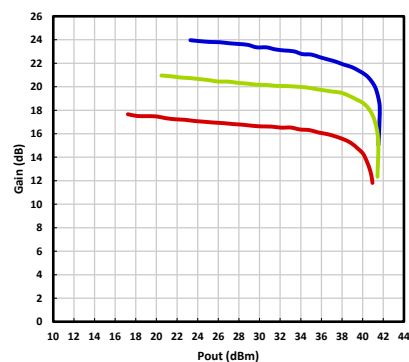


Figure 1-60. PAE vs P_{out} at 11.2GHz

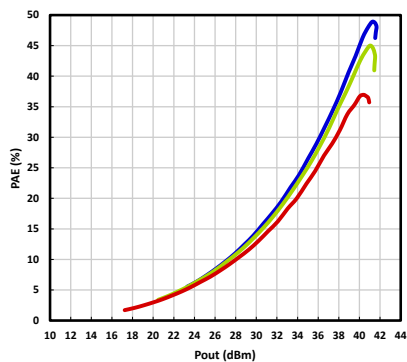


Figure 1-61. I_d vs P_{out} at 11.2GHz

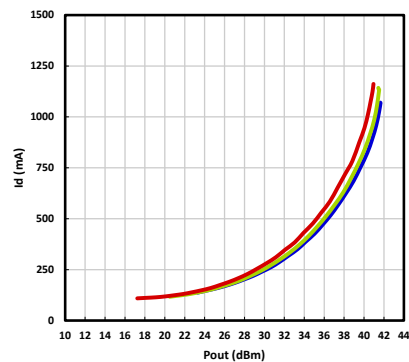
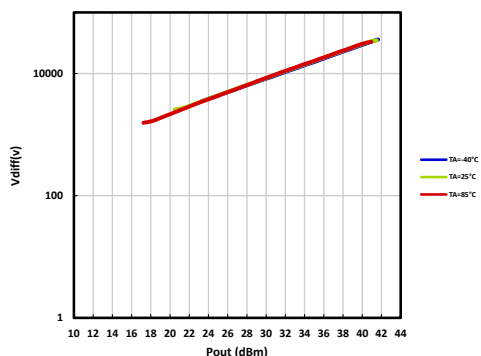


Figure 1-62. V_{diff} ($V_{REF} - V_{DET}$) vs P_{out} at 11.2GHz



Typical Pulsed Power Data over V_d

Test Conditions: $V_D = 20, 24$ and $28V$, $I_{DQ} = 100$ mA, $T_A = 25$ °C, Pulsed 10% Duty Cycle 1 ms period

Figure 1-63. Gain vs P_{out} at 8GHz

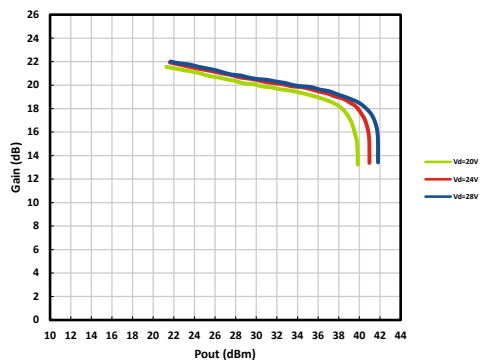


Figure 1-64. PAE vs P_{out} at 8GHz

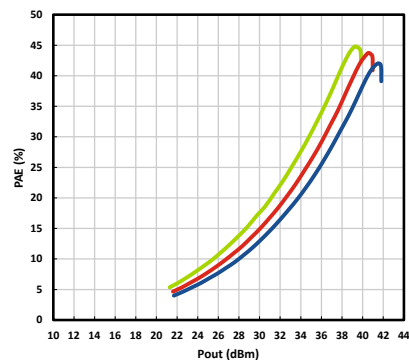


Figure 1-65. Gain vs P_{out} at 9.2GHz

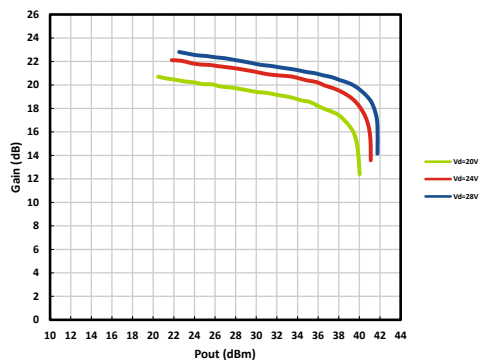


Figure 1-66. PAE vs P_{out} at 9.2GHz

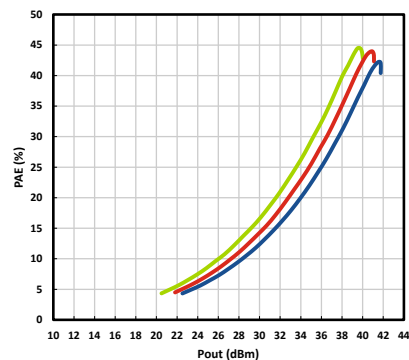


Figure 1-67. Gain vs Pout at 11.2GHz

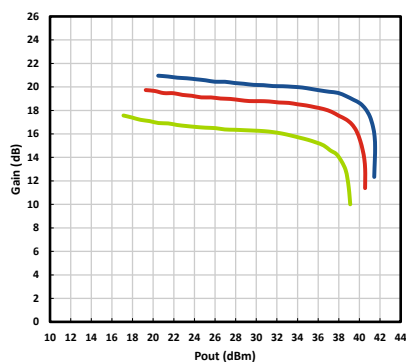
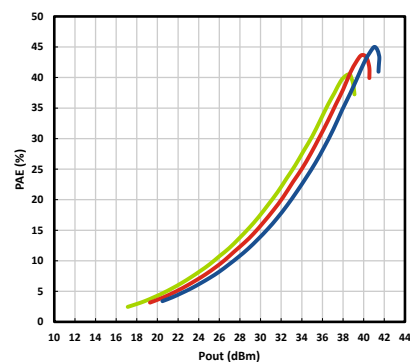


Figure 1-68. PAE vs Pout at 11.2GHz



Typical Pulsed Power Data over I_{DQ}

Test Conditions: $V_D = 28V$, $I_{DQ} = 50, 100$ and 200 mA, Pulsed 10% Duty Cycle 1 ms period

Figure 1-69. Gain vs Pout at 8GHz

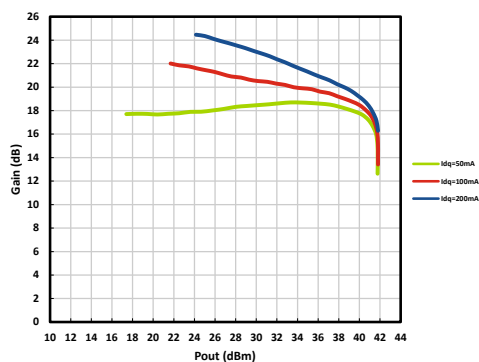


Figure 1-70. PAE vs Pout at 8GHz

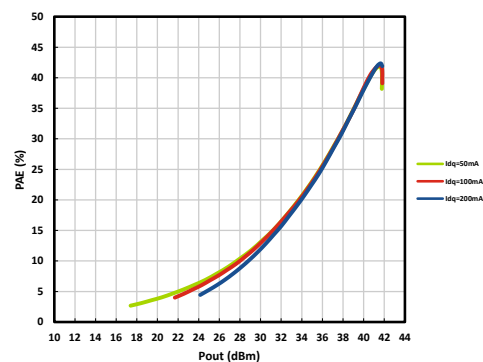


Figure 1-71. Gain vs Pout at 9.2GHz

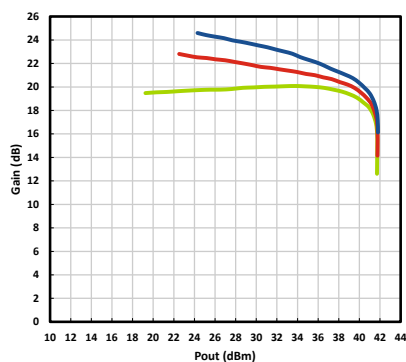


Figure 1-72. PAE vs Pout at 9.2GHz

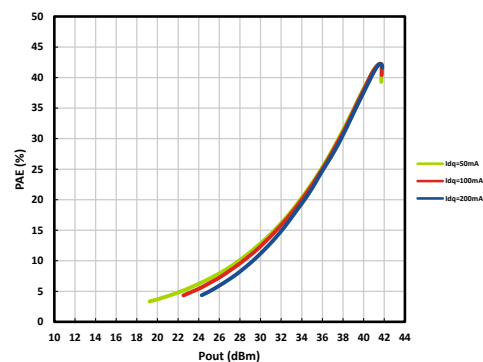


Figure 1-73. Gain vs Pout at 11.2GHz

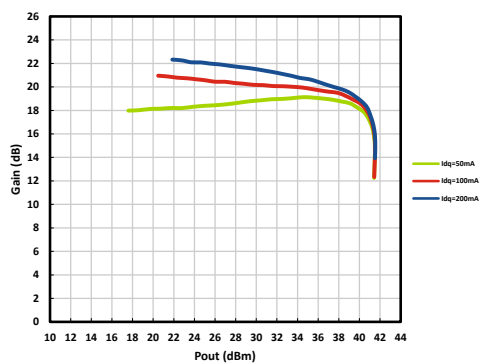
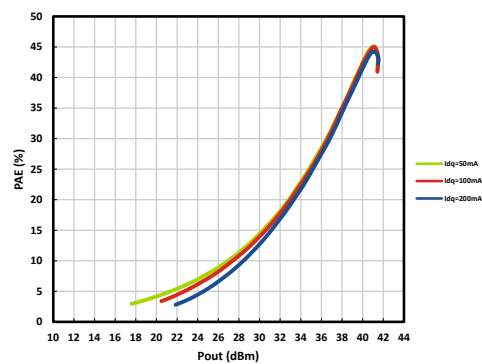


Figure 1-74. PAE vs Pout at 11.2GHz



Typical IMD3 Data over temperature

Test Conditions: tone spacing= 10 MHz, $I_{DQ}=100\text{mA}$, $T_A = -40, 25$ and 85°C

Figure 1-75. IM3 vs Pout total at 8GHz

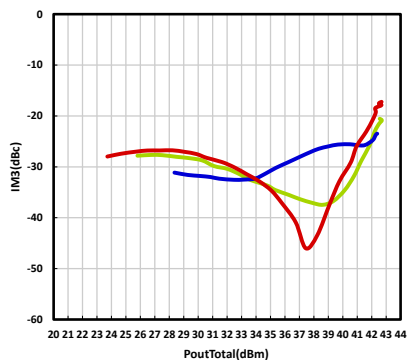


Figure 1-76. IM3 vs Pout total at 9.2GHz

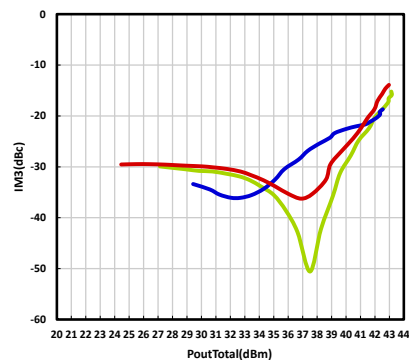


Figure 1-77. IM3 vs Pout total at 10GHz

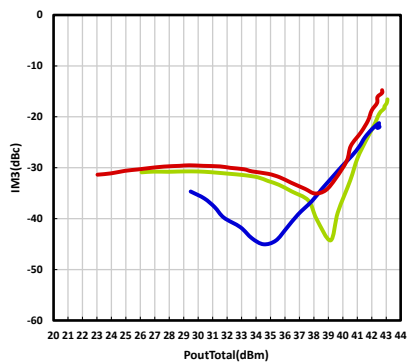
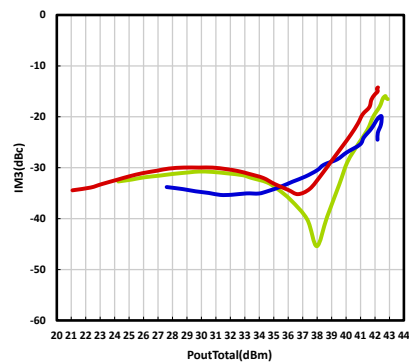


Figure 1-78. IM3 vs Pout total at 11.2GHz



Typical IMD3 Data over Vd

Test Conditions: tone spacing= 10 MHz, $I_{DQ}=100\text{mA}$, $T_A=25^\circ\text{C}$

Figure 1-79. IM3 vs Pout total at 8GHz

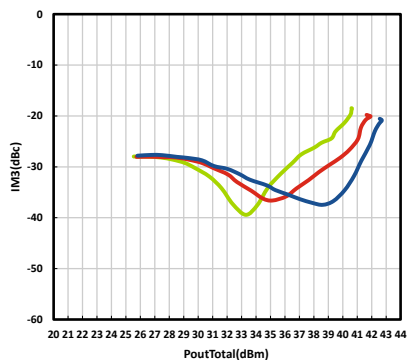


Figure 1-80. IM3 vs Pout total at 9.2GHz

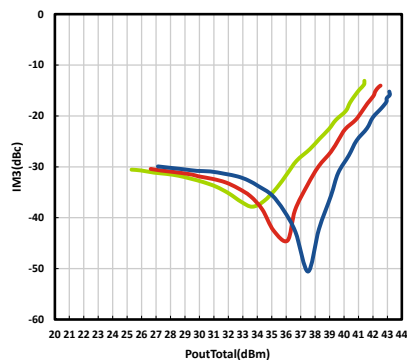


Figure 1-81. IM3 vs Pout total at 10GHz

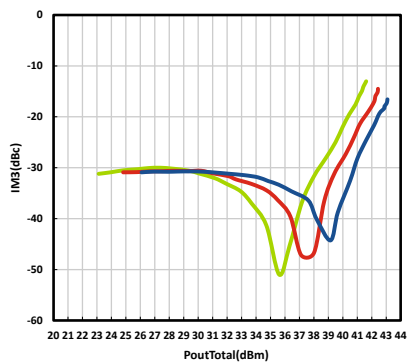
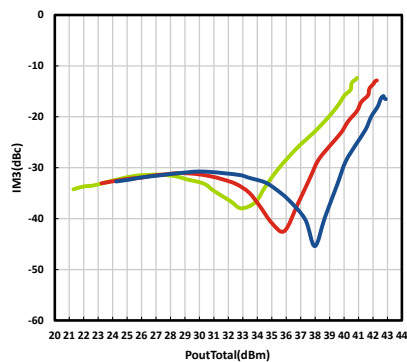


Figure 1-82. IM3 vs Pout total at 11.2GHz



Typical IMD3 Data over Idq

Test Conditions: tone spacing= 10 MHz, Vd=28V, T_A =25°C

Figure 1-83. IM3 vs Pout total at 8GHz

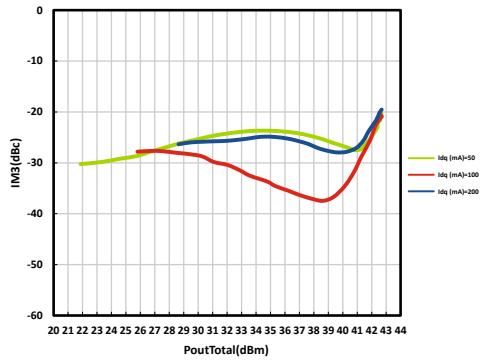


Figure 1-84. IM3 vs Pout total at 9.2GHz

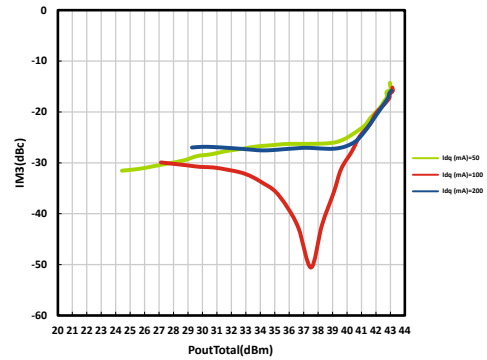


Figure 1-85. IM3 vs Pout total at 10GHz

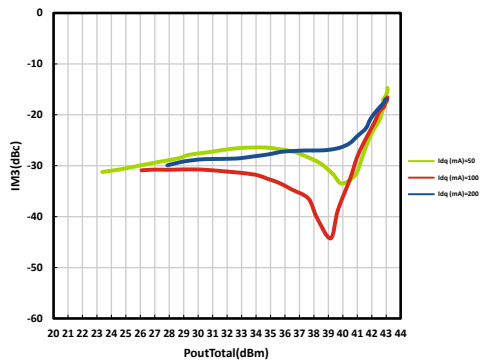
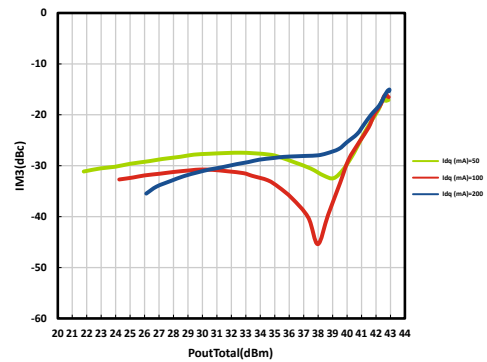
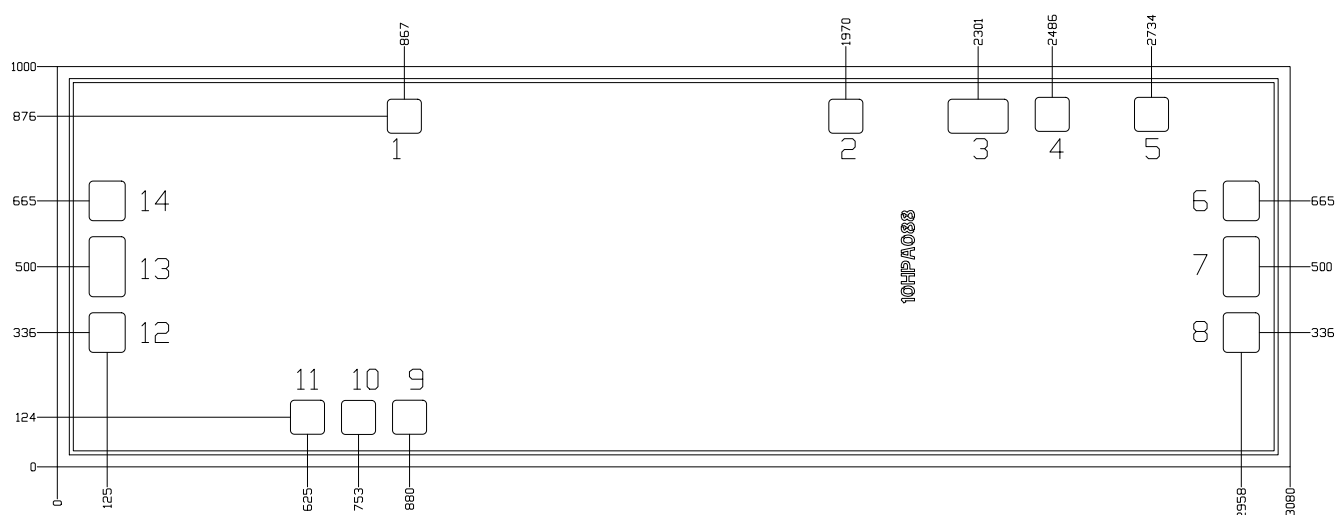


Figure 1-86. IM3 vs Pout total at 11.2GHz



2. Mechanical Drawing

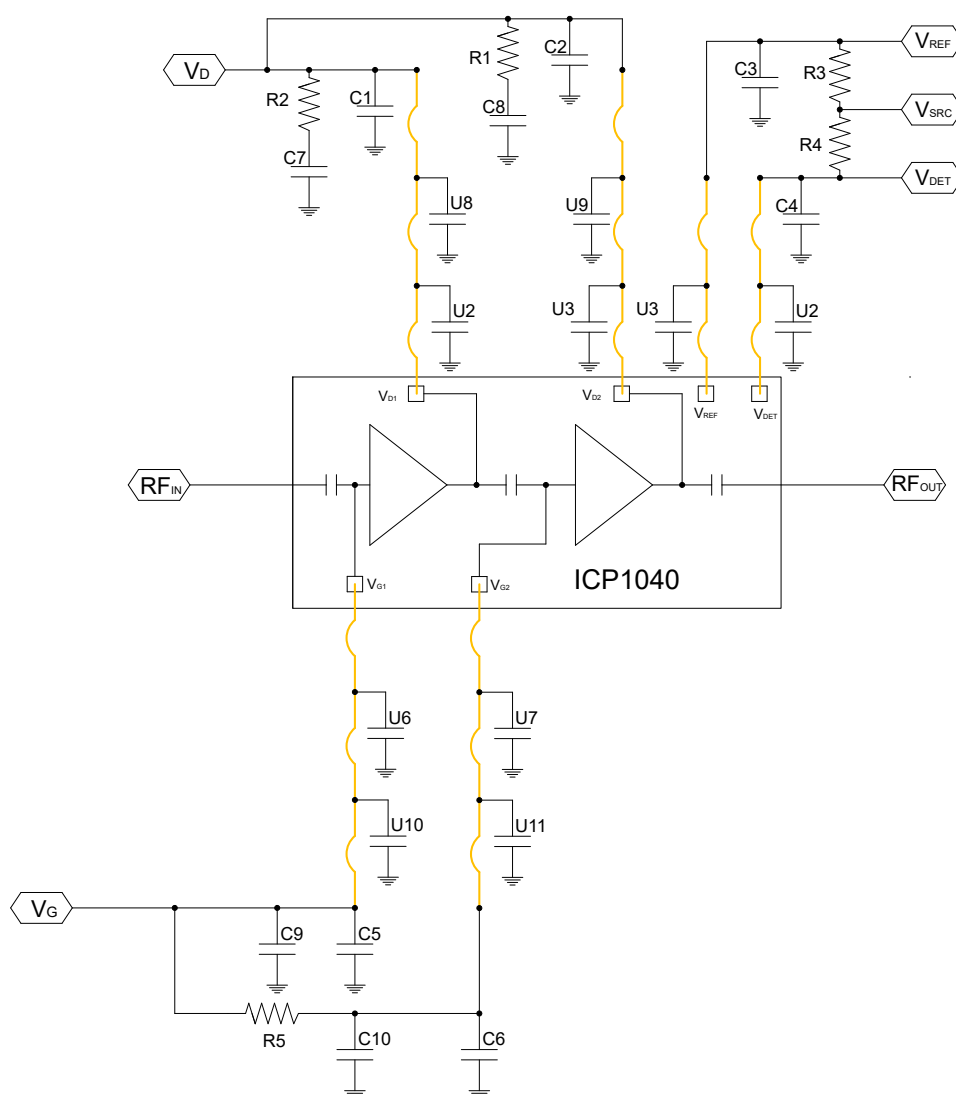


Units: μm | Thickness: 100 μm | Backside of Die is RF and DC ground

Pad No.	Pad Dimension	Function	Description
1	85x85	$V_{D1}^{(1)}$	First stage drain voltage, decoupling and bypass caps required
2	85x85	GND	Ground connection
3	150x85	$V_{D2}^{(1)}$	Second stage drain voltage, decoupling and bypass caps required
4	85x85	REF ⁽³⁾	Detector circuit reference voltage
5	85x85	DET ⁽³⁾	Detector circuit voltage output
6, 8, 12, 14	90x100	GND	Ground connection
7	90x150	RF _{OUT}	RF output, 50 Ω , DC blocked
9	85x85	$V_{G2}^{(2)}$	Second stage gate bias, decoupling and bypass caps required
10	85x85	GND	Ground connection
11	85x85	$V_{G1}^{(2)}$	First stage gate bias, decoupling and bypass caps required
13	90x150	RF _{IN}	RF input, 50 Ω , DC blocked

1. V_{D1} and V_{D2} can be connected together in application
2. V_{G1} and V_{G2} can be connected together in application
3. Applications requiring power detector may use these pads, otherwise pins should be Not Connected

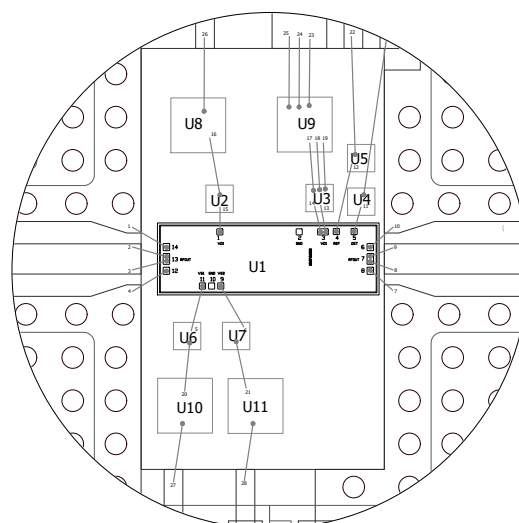
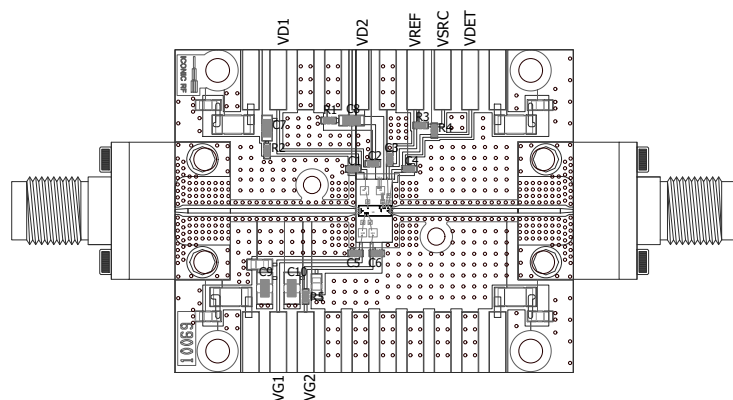
3. Application Circuit



Bill of materials

Component ID	Value	Details	Manufacturer Part No.
U1		ICP1040 MMIC	10HPA088
U2 - U7	100 pF	Johanson 100 pF SLC capacitor	500U01A101MT4W
U8 - U11	10000 pF	10 nF SLC capacitor	V30BZ682M1SX
C1 - C4	10 nF	10 nF capacitor, 10% 50V, 0402	Various
C5, C6	100 nF	100 nF capacitor, 10% 50V, 0402	Various
C7 - C10	10 uF	10 uF capacitor, 10% 35V, 0603	Various
R1, R2, R5	0Ω	0Ω resistor	Various
R3, R4	100kΩ	100kΩ resistor	Various

4. Evaluation Board



DETAIL A - BONDING

PCB Construction	Details
Top and bottom layer	0.5 oz. Cu + ENEPIG
Electroless nickel	3 μm – 6 μm
Electroless palladium	0.05 μm – 0.3 μm
Immersion gold	0.04 μm – 0.06 μm

Key Features	Details
Dielectric	RO4003C
Overall thickness	Approx. 0.27 mm
VIA plating thickness	>15 μm
50 Ω line width	420 μm

5. Other considerations

Assembly Guidance

Interconnect Assembly Notes	Die Attach using Eutectic
- Ball bonding is preferred technique. - Force, time, and ultrasonic parameters are critical. - Aluminum wire bonding is not recommended. - Bond wire diameter of 1mil is recommended.	- Flux-less gold-tin (AuSn) (80% Au, 20% Sn with a melting point of 280 °C) preform is preferred between the die and attached surface. - Recommended preform should be approximately 0.0012" thick. - Die bonder using heated collet with a temperature of 310 °C and die scrubbing should be used to ensure wetting and prevent formation of voids. - Exposure to extreme temperature should be kept to a minimum. - The optimum die attach environment is nitrogen atmosphere.
Die Attach of Component using Adhesive	Re-flow Process
- Vacuum collets are preferred method of pickup. - Pickup method must consider the avoidance of die air bridges. - Die suitable for eutectic and epoxy die attach. - Where epoxy is used, high thermal conductivity Silver Sintered Epoxy is recommended. - Kyocera CT2700R7S - Namics H9888-3	- Maximum temperature 320 °C for 30 seconds. - Material matching for coefficient of thermal expansion is crucial for long-term reliability

Optimum RF power performance achieved by minimizing output RF bond wire length.

For optimum RF and thermal performance, Microchip recommends that the die assembly base plate be adequately bolted to a forced-air heat sink using a thermal graphite interface pad (Graphite Interface Material GCSP-017-G 170 µm thick) for optimal heat transfer. There are many variables of the second-level assembly between the die base plate and heat sink that Microchip is unable to control and the following guidance is provided as information only. Fixing bolts should be provided as close to the die as possible to ensure an optimum pressure between the base plate and the heat sink. The bolting screws used to attach the PCB assembly to the heat sink must include washers and be tightened with a suitable tightening pattern to ensure a uniform pressure. It is advised that all surfaces be cleaned and be free of grease and dust prior to fully aligning the assembly with all screws located and tightened to finger tight. Further torquing of the screws must be achieved in multiple phases using a star shaped pattern to a recommended torque of 2.5 N/m.

Biasing

Bias-up procedure	Bias-down procedure
- Set V_G to -5V - Set V_D to 28V - Adjust V_G positive until I_D quiescent is 100 mA - Limit I_D to 2A - Apply RF signal	- Turn off RF - Turn off V_D, allow drain capacitors to discharge - Turn off V_G

6. Ordering, Shipping, and Handling

Handling Recommendations

Integrated circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. It is recommended to follow all procedures and guidelines outlined in the Microsemi application note AN01: GaAs MMIC Handling and Die Attach Recommendations.

Ordering Information

For additional ordering information, contact your Microchip sales representative.

Part Number	Description
ICP1040-1-110I	7.9-11GHz 12W Bare Die GaN Power Amplifier in Gelpak Format
EV76C83A	Dev Tool for ICP1040-1-110I, Fully Assembled Evaluation Board with RF Test Data

7. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 7-1. Revision History

Revision	Date	Description
A	07/2025	Document created.
B	05/2026	Measurement charts updated

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