

General Description

The MIC2790, MIC2791, and MIC2793 are ideal for monitoring highly accurate core voltages that require rapid response in the event of a fault condition. The voltage supervisor IC features a manual reset input, enable input (MIC2793 only), a capacitor-programmable reset timeout delay, and both an active-low and active-high reset output.

The MIC2790/1/3 monitor system voltages that are in the range of 0.4V to 5.5V, with a typical sense accuracy of 0.5% at +25°C and $\pm 1.0\%$ across -40°C to $+125^{\circ}\text{C}$. The IC asserts a reset output when the sense voltage drops below the threshold or when the manual reset is pulled to a logic low. The active-low reset stays low for the duration of the reset timeout delay once the sense voltage returns to normal and the manual reset transitions to a logic high state. The reset timeout delay period is programmable from 1ms to 10s with an external capacitor.

The MIC2790/1/3 operate from a low supply voltage of 1.5V to 5.5V and is rated to operate over the temperature range of -40°C to $+125^{\circ}\text{C}$. The MIC2790 is available in a 6-lead TSOT-23 package or a 6-lead $2\text{mm} \times 2\text{mm} \times 0.55\text{mm}$ UDFN package. The MIC2791 is available in a tiny 6-lead $1.6\text{mm} \times 1.6\text{mm} \times 0.55\text{mm}$ UDFN package. The MIC2793 is available in a 8-lead $2\text{mm} \times 2\text{mm} \times 0.55\text{mm}$ UDFN package.

Features

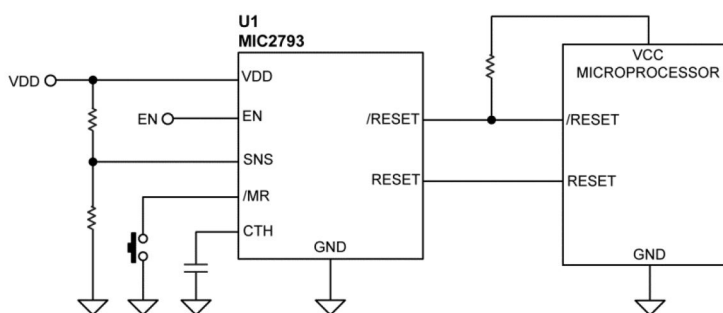
- 1.5V to 5.5V Operating Supply Voltage Range
- Ultra-Fast Propagation Delay (1 μs Typically)
- 0.4V Reference Voltage (SNS Pin)
 - $\pm 1.0\%$ Threshold Accuracy from -40°C to $+125^{\circ}\text{C}$
 - Monitored Voltage Range from 0.4V to 5.5V
- Programmable Reset Timeout Delay (from 1ms to 10 sec.)
- Manual Reset Input with an Internal Pull-Up Resistor
- Active-High Enable Input Pin (MIC2793 Only)
- The MIC2790/1/3 Feature Multiple Output Options:
 - Open-Drain Active-Low (/RESET)
 - Push-Pull Active-Low (/RESET)
 - Push-Pull Active-High (RESET)
- -40°C to $+125^{\circ}\text{C}$ Junction Temperature Range
- 6-Lead TSOT-23 (MIC2790)
- 6-Lead $2\text{mm} \times 2\text{mm}$ UDFN (MIC2790)
- 6-Lead $1.6\text{mm} \times 1.6\text{mm}$ UDFN (MIC2791)
- 8-Lead $2\text{mm} \times 2\text{mm}$ UDFN (MIC2793)

Applications

- Telecom
- Computers/Servers
- Medical Equipment
- Portable Devices
- Set-Top Boxes
- Critical Microprocessor Monitoring

Typical Application

Figure 1. Typical Application Circuit



Functional Block Diagram

Figure 2. Functional Block Diagram

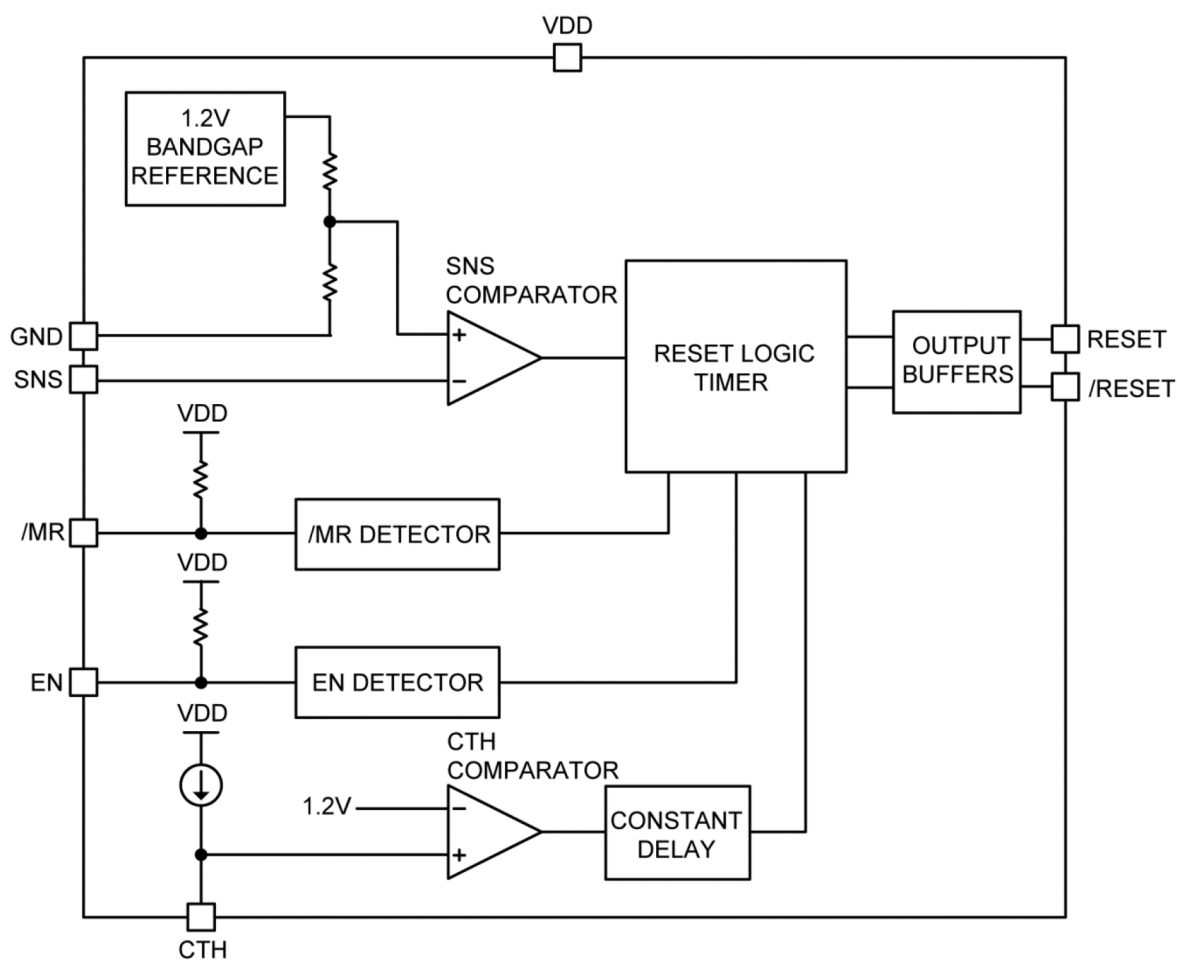


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1. Electrical Characteristics

Table 1-1. Absolute Maximum Ratings

Supply Voltage (V_{DD})	-0.3V to +6.0V
SNS	-0.3V to +4.5V
/MR, EN, C_{TH}	-0.3V to V_{DD}
RESET, /RESET	-0.3V to V_{DD}
ESD Ratings	ESD Sensitive (Note 1)
Notice: Exceeding the absolute maximum ratings may damage the device.	
1. Devices are ESD sensitive. Handling precautions are recommended. Human body model, 1.5k Ω in series with 100pF.	

Table 1-2. Operating Ratings

Supply Voltage (V_{DD})	+1.5V to +5.5V
SNS	0V to +4.0V
/MR, EN, C_{TH}	0V to V_{DD}
RESET, /RESET	0V to V_{DD}
Notice: The device is not guaranteed to function outside its operating ratings.	

Table 1-3. Electrical Characteristics

V _{DD} = 3.3V, R _{/RESET} = 100kΩ, C _{TH} = 1nF, T _A = +25°C; bold values valid for -40°C ≤ T _A ≤ +125°C, unless noted. (Note 1)						
Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Supply Specifications						
Supply Voltage	V _{DD}	1.5	—	5.5	V	/RESET output valid
Supply Current	I _{DD}	—	40	70	μA	V _{DD} = EN = /MR = 3.3V; RESET and /RESET not asserted
		—	50	80		V _{DD} = EN = /MR = 5V; RESET and /RESET not asserted
Sense Specifications						
Sense Threshold Voltage	V _{TH}	—	0.4	—	V	—
Sense Threshold Accuracy		-1.0	—	+1.0	%	—
Hysteresis	V _{HYST}	-2.5	±1.5	+2.5	%	Sense rising
Sense Input Bias Current	I _{SNS}	-15	—	+15	nA	—
RESET and /RESET Output Specifications						
SNS to RESET and /RESET Propagation Delay	t _{P_SNS}	—	1	2.2	μs	SNS = V _{TH} × 1.05 to V _{TH} × 0.95, Note 2
/RESET Logic Low Output Voltage	V _{OL}	—	—	0.3	V	I _{OL} = 1mA (open-drain only)
RESET Logic High Output Voltage	V _{OH}	>0.9 × V _{DD}	—	—	V	I _{OH} ≤ 1mA (push-pull only)
/RESET Leakage Current	I _{OH}	—	—	1	μA	/RESET not asserted (open-drain only)
RESET and /RESET Timeout Delay	t _D	0.45	1.05	1.8	ms	C _{TH} = 100pF
		0.5	1.2	1.9	sec	C _{TH} = 180nF
/MR Input Specifications						

Table 1-3. Electrical Characteristics (continued)

V_{DD} = 3.3V, R_{/RESET} = 100kΩ, C_{TH} = 1nF, T_A = +25°C; bold values valid for -40°C ≤ T_A ≤ +125°C, unless noted. (Note 1)						
Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
/MR Internal Pull-Up Resistance	R _{/MR}	—	90	—	kΩ	—
/MR to RESET and /RESET Propagation Delay	t _{P_/MR}	—	100	—	ns	—
/MR Logic Low Input Voltage	V _{IL}	—	—	0.5	V	—
/MR Logic High Input Voltage	V _{IH}	1.2	—	—	V	—
EN Input Specifications (MIC2793 Only)						
EN Internal Pull-Up Resistance	R _{EN}	—	90	—	kΩ	—
EN to RESET and /RESET Propagation Delay	t _{P_EN}	—	100	—	ns	/MR = logic low
EN Logic Low Input Voltage	V _{ENL}	—	—	0.5	V	—
EN Logic High Input Voltage	V _{ENH}	1.2	—	—	V	—
1. Specification for packaged product only. 2. SNS to RESET and/or /RESET propagation delay is the delay time for SNS voltage to transition from V _{TH} × 1.05 to V _{TH} × 0.95 to RESET and/or /RESET.						

Table 1-4. Temperature Specifications

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Junction Temperature Range	T _J	-40	—	+125	°C	—
Storage Temperature Range	T _S	-55	—	+150	°C	—
Lead Temperature	T _{LEAD}	—	—	+260	°C	Soldering, 10 sec.
Package Thermal Resistances						
Thermal Resistance, 6-Lead TSOT-23	θ _{JA}	—	177.2	—	°C/W	—
Thermal Resistance, 6-Lead 1.6mm x 1.6mm UDFN	θ _{JA}	—	92.4	—	°C/W	—
Thermal Resistance, 6-Lead 2mm x 2mm UDFN	θ _{JA}	—	90	—	°C/W	—
Thermal Resistance, 8-Lead 2mm x 2mm UDFN	θ _{JA}	—	90	—	°C/W	—

2. Pin Description

Figure 2-1. 6-Lead TSOT-23 (D6)

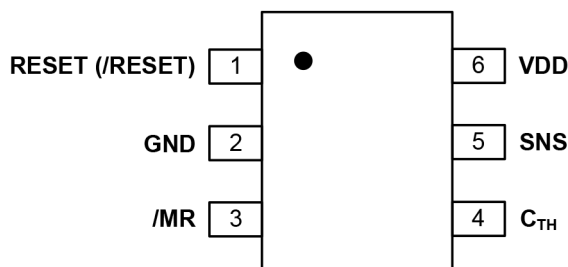


Figure 2-2. 6-Lead 1.6mm x 1.6mm UDFN (MT)

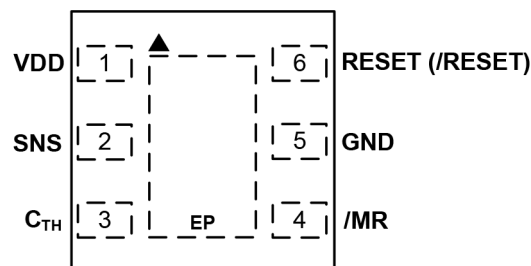


Figure 2-3. 6-Lead 2mm x 2mm UDFN (MT)

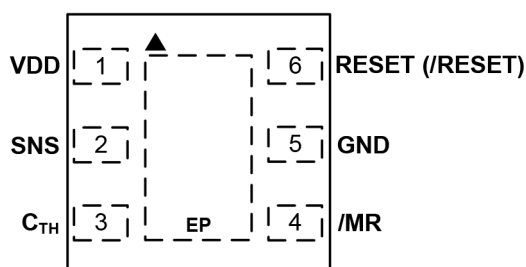


Figure 2-4. 8-Lead 2mm x 2mm UDFN (MT)

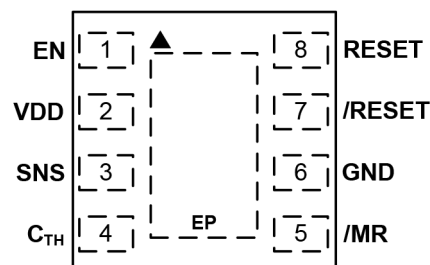


Table 2-1. Pin Descriptions

Pin Number TSOT-23 (6L)	Pin Number 1.6mm x 1.6mm (6L)	Pin Number 2mm x 2mm (6L)	Pin Number 2mm x 2mm (8L)	Pin Name	Pin Function
1	6	6	7	/RESET	/RESET is an active-low output pin and is available in an open-drain or push-pull configuration. In the open-drain configuration, a pull-up resistor to VDD is required and /RESET pin is asserted low when /MR is set to a logic low or the SNS voltage decreases below the threshold voltage. /RESET will remain low for the reset timeout delay after $SNS > (V_{TH} + V_{HYS})$ and /MR is set to a logic high. The push-pull configuration does not require a pull-up resistor and behaves exactly the same as the open-drain configuration.
1	6	6	8	RESET	Reset is an active-high push-pull output and is asserted high when /MR is set to a logic low or the SNS voltage decreases below the threshold voltage. RESET will remain high for the reset timeout delay after $SNS > (V_{TH} + V_{HYS})$ and /MR is set to a logic high.
2	5	5	6	GND	Supply Ground.

Table 2-1. Pin Descriptions (continued)

Pin Number TSOT-23 (6L)	Pin Number 1.6mm x 1.6mm (6L)	Pin Number 2mm x 2mm (6L)	Pin Number 2mm x 2mm (8L)	Pin Name	Pin Function
3	4	4	5	/MR	Manual reset is an active-low input logic level pin and is internally pulled to VDD through a 90k Ω pull-up resistor. Pulling the /MR input to a logic low asserts RESET and /RESET pins. /RESET will remain low and RESET will remain high for the reset timeout delay after /MR is pulled to logic high.
4	3	3	4	CTH	Programmable timeout delay. Connect a capacitor to ground to set a user-defined reset delay time.
5	2	2	3	SNS	Voltage monitor input. Connect the Sense pin to the voltage to be monitored through a resistor divider. When this voltage decreases below the threshold voltage, V_{TH} , /RESET is asserted low and RESET is asserted high.
6	1	1	2	VDD	Supply voltage pin. Bypass with a 1 μ F capacitor from this pin to GND.
—	—	—	1	EN	Enable input function is only available in the MIC2793 version. This pin enables the /MR input function and RESET and /RESET outputs. When EN is in a logic low state, the reset outputs are deasserted. The EN pin has an internal 90k Ω pull-up resistor to VDD.
—	EP	EP	EP	ePAD	Exposed Pad. Connect to ground plane.

3. Typical Operating Characteristics

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Figure 3-1. Supply Current vs. Supply Voltage

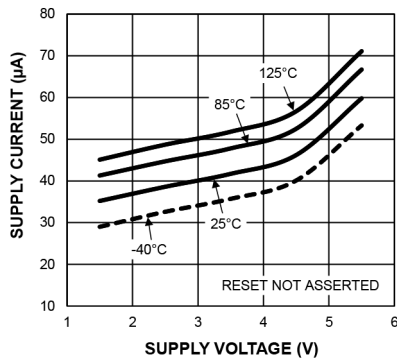


Figure 3-2. Reset Timeout Delay vs. Supply Voltage

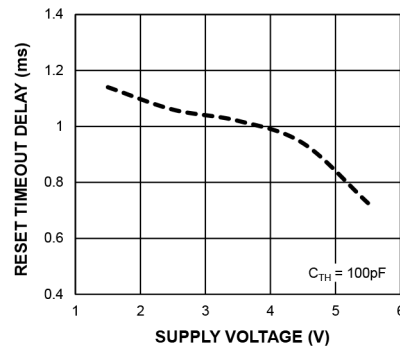


Figure 3-3. Reset Timeout Delay vs. Supply Voltage

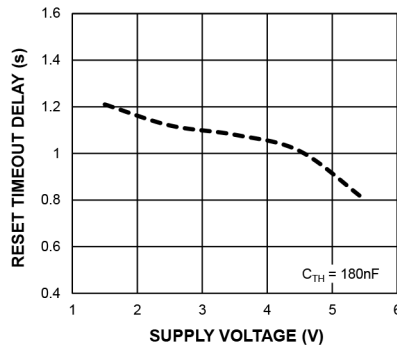


Figure 3-4. Reset Timeout Delay vs. C_{TH}

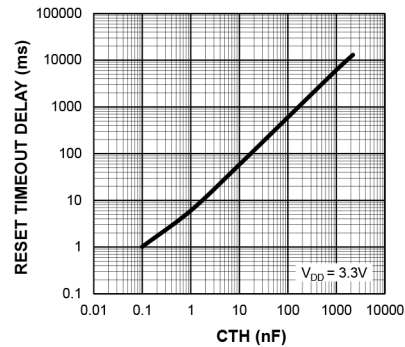


Figure 3-5. Reset Timeout Delay vs. Temperature

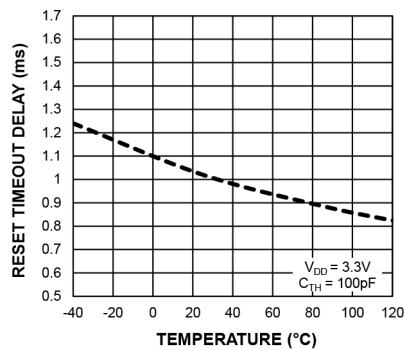


Figure 3-6. Reset Timeout Delay vs. Temperature

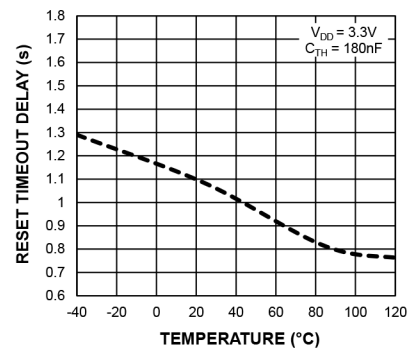


Figure 3-7. Normalized SNS Threshold vs. Supply Voltage

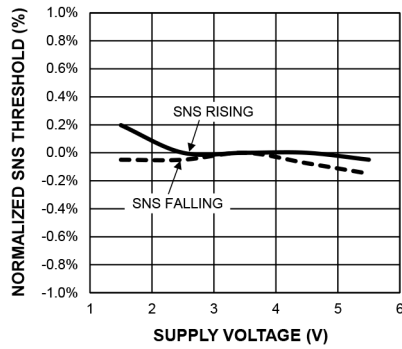


Figure 3-8. Normalized SNS Threshold vs. Temperature

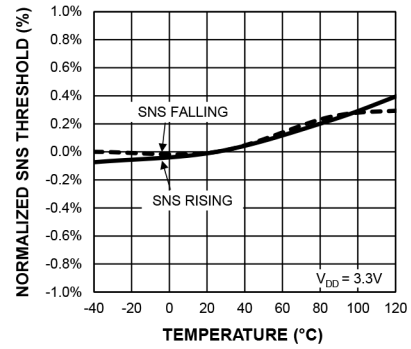


Figure 3-9. C_{TH} Charging Current vs. Supply Voltage

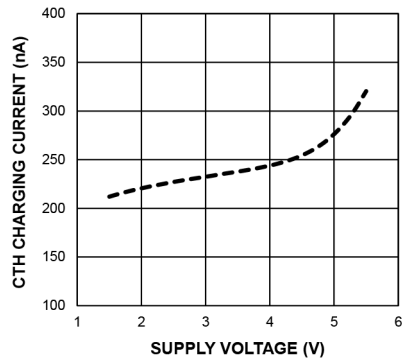
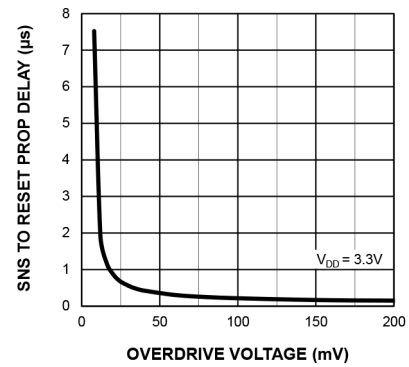


Figure 3-10. SNS to RESET Propagation Delay vs. Overdrive Voltage



4. Timing Diagrams

Figure 4-1. Timeout and Propagation Delay from SNS to RESET and /RESET

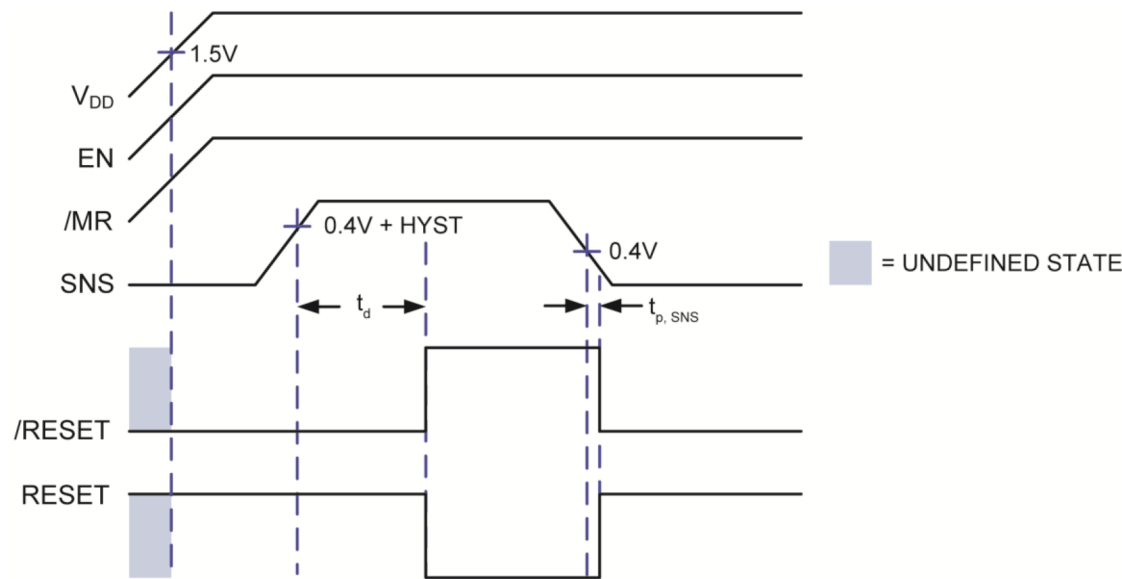


Figure 4-2. Timeout and Propagation Delay from /MR to RESET and /RESET

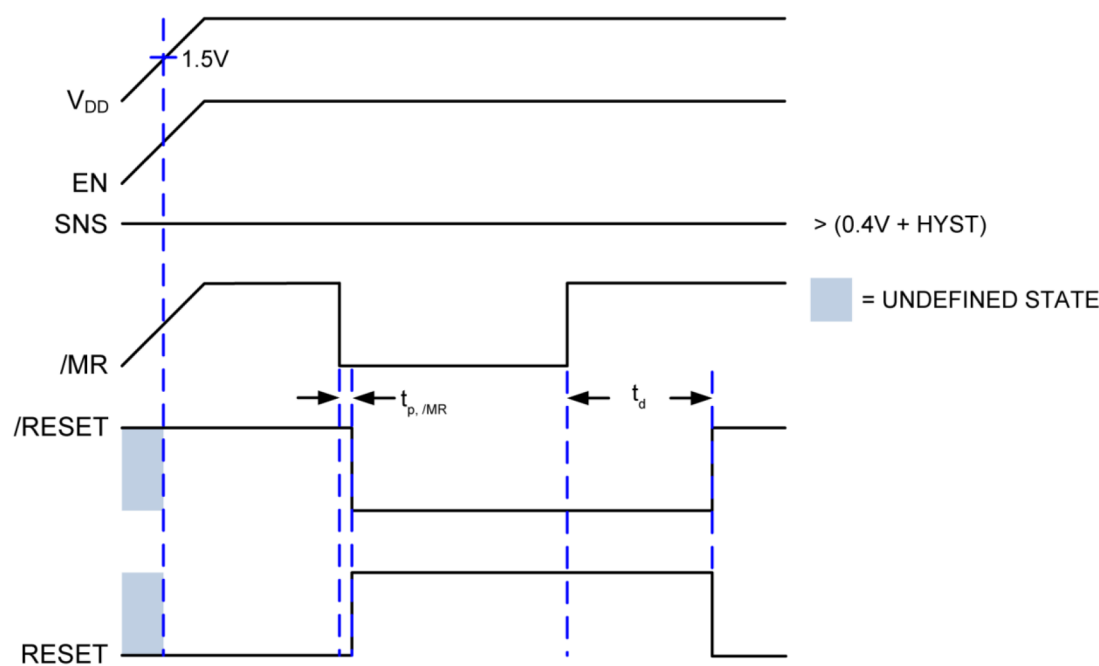
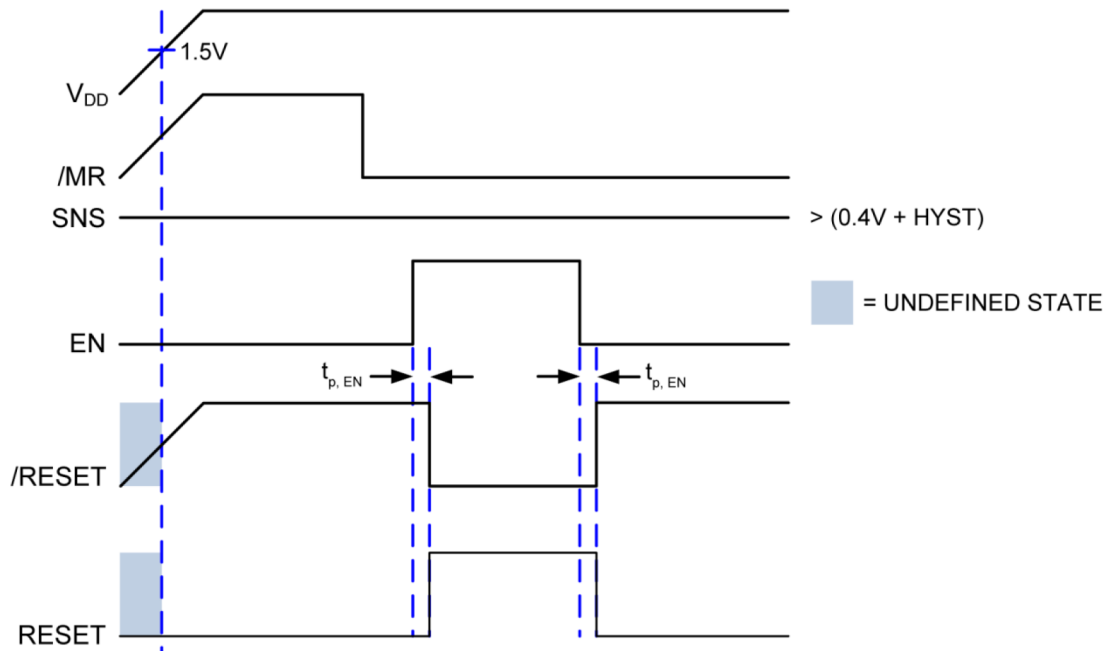


Figure 4-3. Hold and Propagation Delay from EN to RESET and /RESET



5. Functional Description

5.1. Design and Product Advantages

The MIC2790/1/3 are highly accurate supervisor circuits with an ultra-fast propagation delay of 2.2μs (maximum) over the temperature range of -40°C to +125°C. Additional features in the MIC2790/1/3 include a manual reset input pin, a capacitor-programmable reset timeout delay, and both an active-low and active-high reset output. The capacitor-programmable reset delay helps protect against accidental system glitch during a reset timeout.

5.2. VDD

The input supply (VDD) pin provides power to the comparators and logic timers. The VDD operating range is 1.5V to 5.5V. A ceramic input capacitor of 1μF with a minimum voltage rating of 6.3V is recommended between VDD and GND. Refer to the [PCB Layout Recommendations](#) section for details.

5.3. EN

The enable (EN) pin feature is only available in the MIC2793 and has an internal 90kΩ pull-up resistor to VDD. A logic high signal on the EN pin enables the reset logic outputs, while a logic low signal disables the reset outputs. See [Figure 4-3](#) for more information.

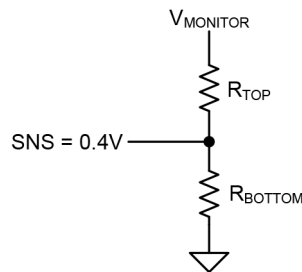
5.4. CTH

CTH is a programmable timeout delay pin. Connect a capacitor to Ground to set a reset timeout delay ranging from 1ms to 10 seconds. Refer to [Figure 3-4](#) for examples.

5.5. SNS

The sense (SNS) input pin monitors the user's voltage through a resistor divider network as shown in the following figure.

Figure 5-1. Resistor Divider on SNS Pin



To set R_{TOP} and R_{BOTTOM} , use the following equation and set an arbitrary R_{TOP} value greater than 100kΩ and solve for R_{BOTTOM} or vice versa.

Equation 5-1. Calculating R_{TOP} or R_{BOTTOM}

$$V_{MONITOR} = 0.4V \times \left(1 + \frac{R_{TOP}}{R_{BOTTOM}} \right)$$

5.6. GND

The ground (GND) pin is the return path for VDD, logic gates, and output pins. Refer to the [PCB Layout Recommendations](#) section for details.

5.7. /MR

The manual reset (/MR) pin is an active-low input that is internally pulled to VDD with a 90kΩ resistor. When /MR is asserted to a logic-low level, /RESET will transition to a logic low state while RESET will transition to a logic high state. See the [Timing Diagrams](#) section for more information.

5.8. /RESET

/RESET is an active-low output and is available in two output configurations: open-drain or push-pull. The open-drain configuration requires an external pull-up resistor, while the push-pull does not.

/RESET is asserted low when /MR is set to a logic-low or the SNS voltage decreases below the threshold voltage. /RESET will remain low for the programmed reset timeout delay after $SNS > (V_{TH} + V_{HYST})$ and /MR is set to a logic-high, and then /RESET will transition high to indicate normal regulation. See the [Timing Diagrams](#) section for more information.

5.9. RESET

RESET is an active-high push-pull output and is asserted high when /MR is set to a logic low or the SNS voltage decreases below the threshold voltage. RESET will remain high for the programmed reset timeout delay after $SNS > (V_{TH} + V_{HYST})$ and /MR is set to a logic high, and then RESET will transition low to indicate normal regulation. See the [Timing Diagrams](#) section for more information.

6. Typical Application Schematic

Figure 6-1. Typical Application Schematic

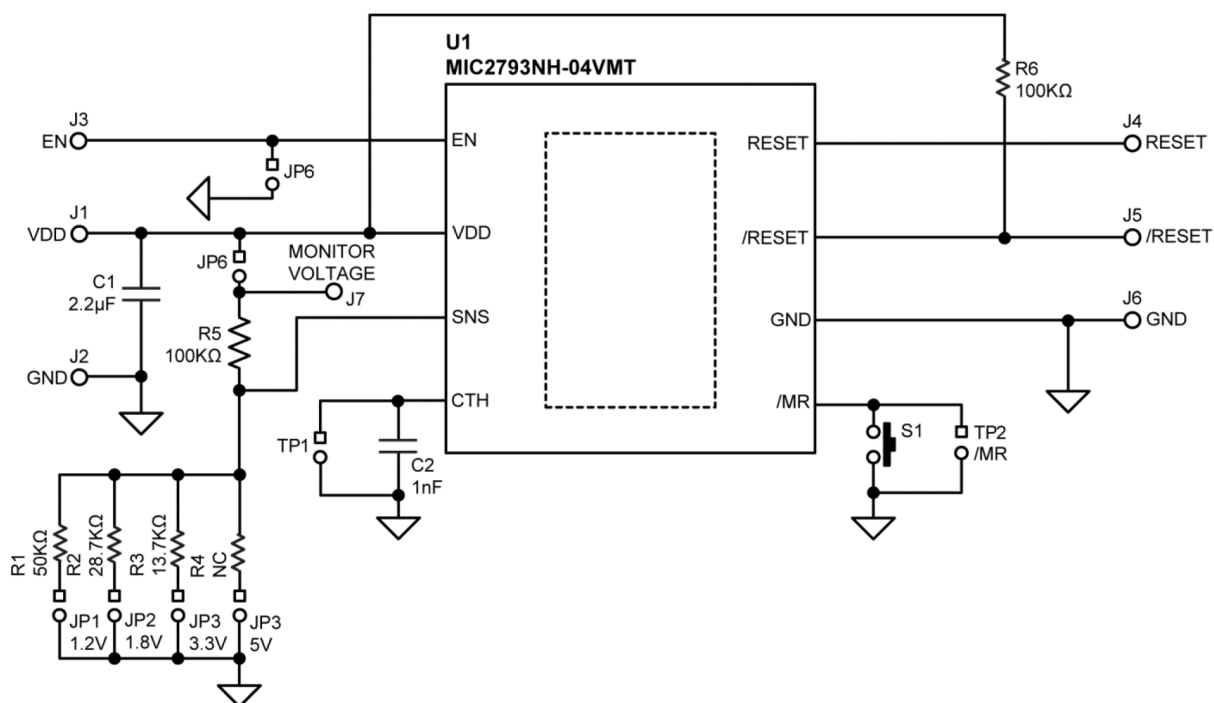


Table 6-1. Bill of Materials

Item	Part Number	Manufacturer	Description	Qty.
C1	06036D225KAT2A	AVX	2.2μF, 6.3V, X5R, 0603	1
	GRM188R60J225KE19D	Murata		
	C1608X5R0J225KT	TDK		
C2	01016D102KAT2A	AVX	1nF, 6.3V, X5R, 0603	1
	GRM155R60J102KA01D	Murata		
	C0402X5R0J102K020BC	TDK		
R1	CRCW060350K0FKEA	Vishay Dale	50kΩ, 1%, 1/10W, 0603	1
R2	CRCW060328K7FKEA	Vishay Dale	28.7kΩ, 1%, 1/10W, 0603	1
R3	CRCW060313K7FKEA	Vishay Dale	13.7kΩ, 1%, 1/10W, 0603	1
R5, R6	CRCW06031003FKEA	Vishay Dale	100kΩ, 1%, 1/10W, 0603	2
U1	MIC2793NH-04VMT	Microchip Technology Inc.	Supervisor with High-Accuracy, Ultra-Fast Propagation Delay, and Capacitor-Programmable Reset Delay	1

7. PCB Layout Recommendations

Figure 7-1. Top Layer

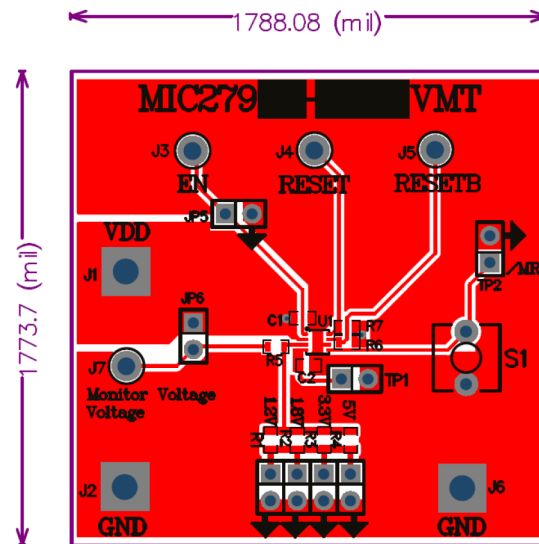
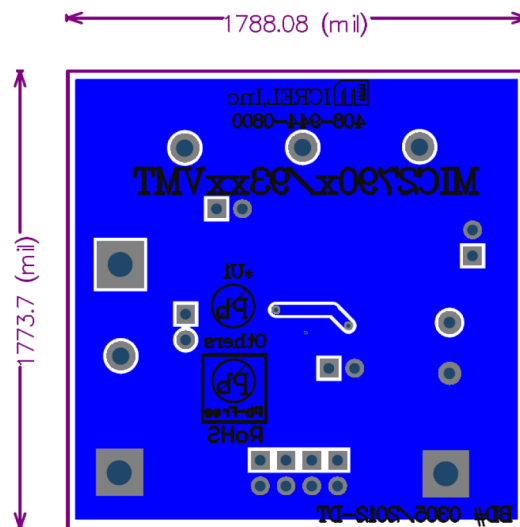


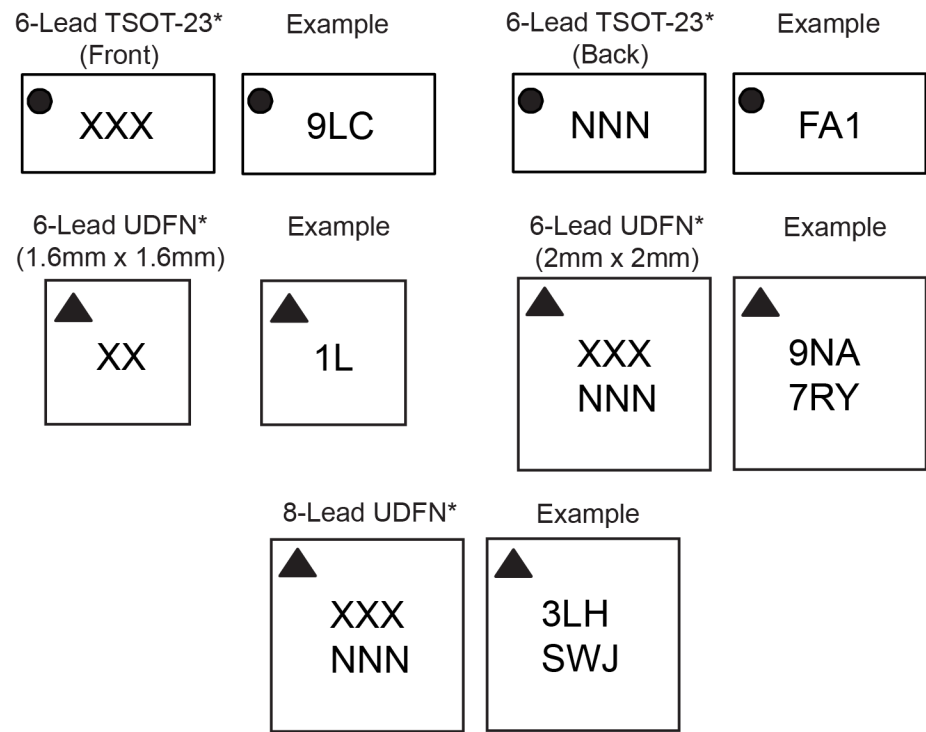
Figure 7-2. Bottom Layer



8. Package Information

8.1. Package Marking Drawings

Figure 8-1. Package Marking Drawings



Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.	
	Underbar (_) and/or Overbar (¯) symbol may not be to scale.	

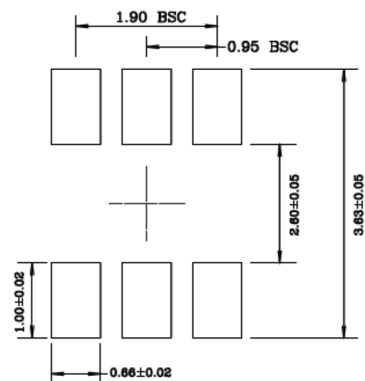
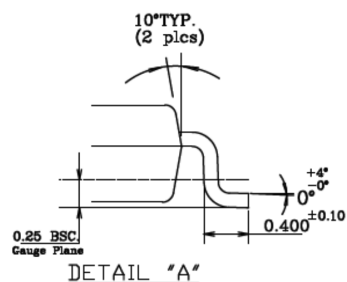
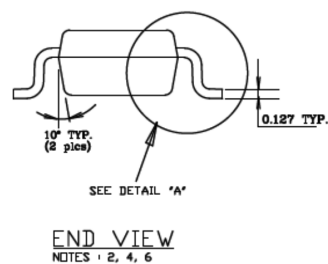
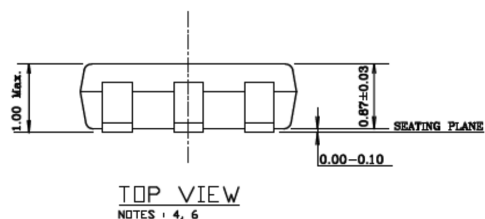
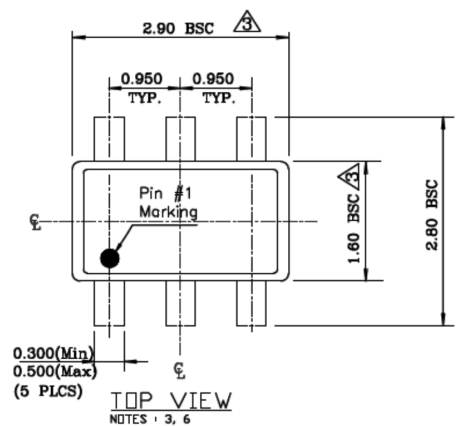
Note: If the full seven-character YYWWNNN code cannot fit on the package, the following truncated codes are used based on the available marking space: 6 Characters = YWWNNN; 5 Characters = WWNNN; 4 Characters = WNNN; 3 Characters = NNN; 2 Characters = NN; 1 Character = N

8.2. Package Outline Drawings

TITLE

6 LEAD TSOT PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	TSOT-6LD-PL-1	UNIT	MM
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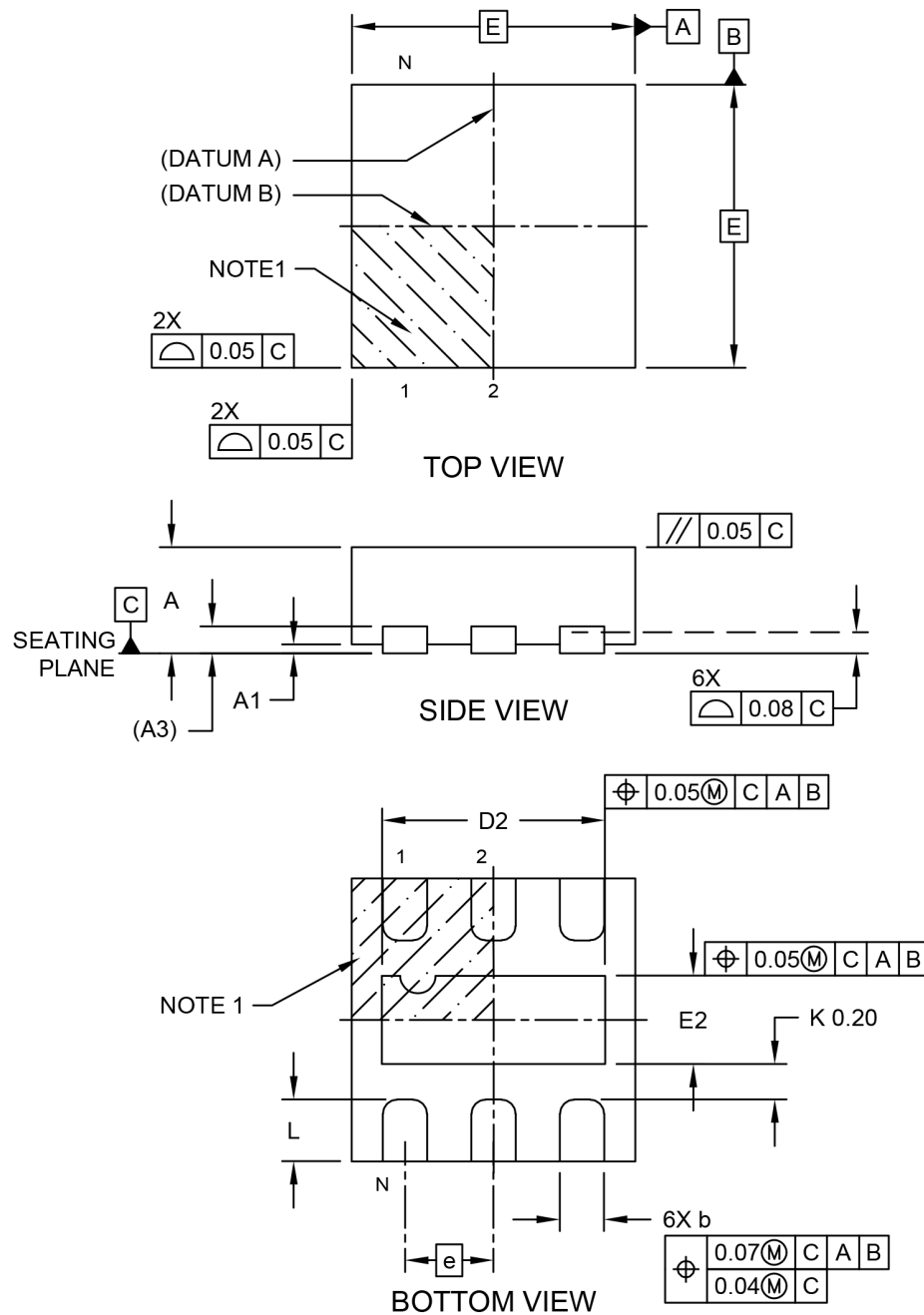
NOTE:

1. Dimensions and tolerances are as per ANSI Y14.5M, 1994.
2. Die is facing up for mold. Die is facing down for trim/form, ie. reverse trim/form.
3. Dimensions are exclusive of mold flash and gate burr.
4. The footlength measuring is based on the gauge plane method.
5. All specification comply to Jedec Spec M0193 Issue C.
6. All dimensions are in millimeters.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>.

**6-Lead Ultra Thin Plastic Dual Flat, No Lead (HKA) - 1.6x1.6x0.6 mm Body [UDFN]
With 1.26x0.50 mm Exposed Pad; Micrel Legacy Package TDFN1616-6LD-PL-1**

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

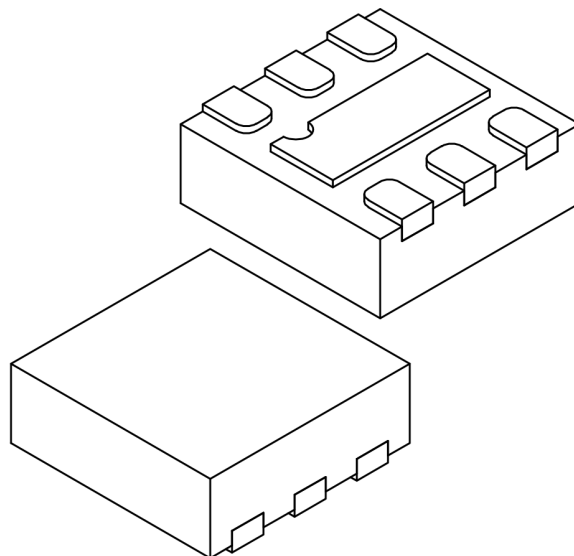


Microchip Technology Drawing C04-1154 Rev A Sheet 1 of 2

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**6-Lead Ultra Thin Plastic Dual Flat, No Lead (HKA) - 1.6x1.6x0.6 mm Body [UDFN]
With 1.26x0.50 mm Exposed Pad; Micrel Legacy Package TDFN1616-6LD-PL-1**

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N	6		
Pitch	e	0.50 BSC		
Overall Height	A	0.50	0.55	0.60
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3	0.152 REF		
Overall Length	D	1.60 BSC		
Exposed Pad Length	D2	1.21	1.26	1.31
Overall Width	E	1.60 BSC		
Exposed Pad Width	E2	0.45	0.50	0.55
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.30	0.35	0.40
Terminal-to-Exposed-Pad	K	0.20	—	—

Notes:

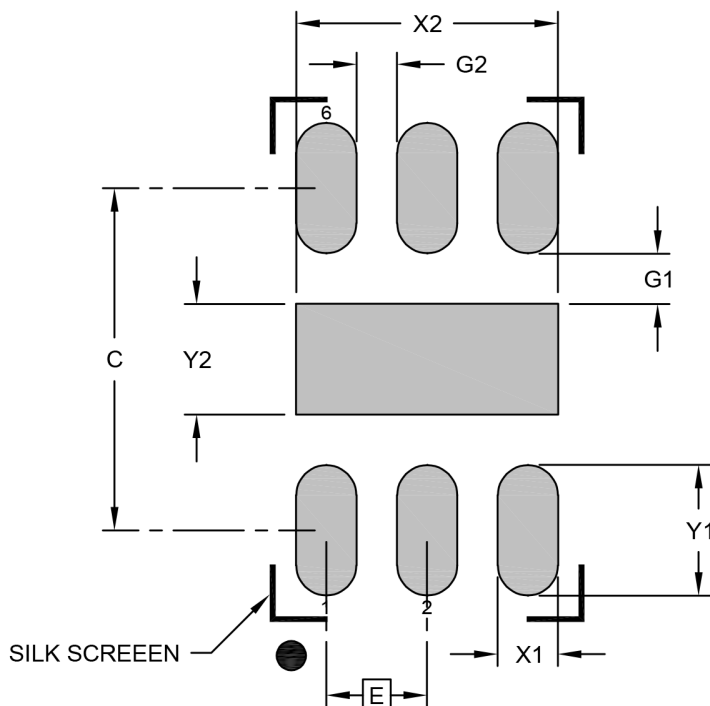
- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated
- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1154 Rev A Sheet 2 of 2

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**6-Lead Ultra Thin Plastic Dual Flat, No Lead (HKA) - 1.6x1.6x0.6 mm Body [UDFN]
With 1.26x0.50 mm Exposed Pad; Micrel Legacy Package TDFN1616-6LD-PL-1**

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Center Pad Width	X2			1.30
Center Pad Length	Y2			0.55
Contact Pad Spacing	C		1.70	
Contact Pad Width (X6)	X1			0.30
Contact Pad Length (X6)	Y1			0.65
Contact Pad to Center Pad (X6)	G1	0.25		
Contact Pad to Contact Pad (X4)	G2	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

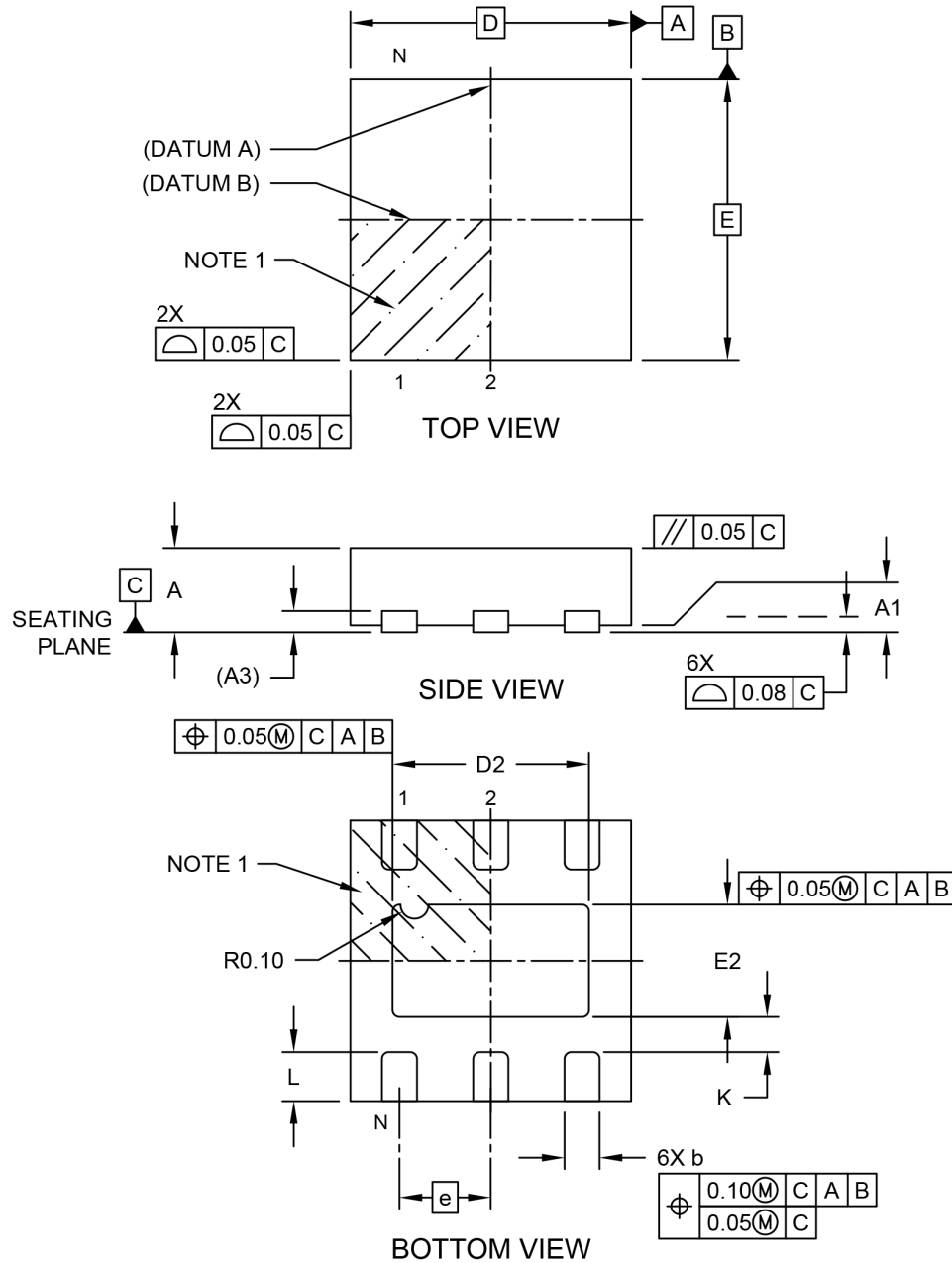
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-3154 Rev A

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**6-Lead Ultra Thin Plastic Dual Flat, No Lead Package (HSA) - 2x2x0.6 mm Body [UDFN]
Micrel Legacy Package TDFN22-6LD-PL-1**

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

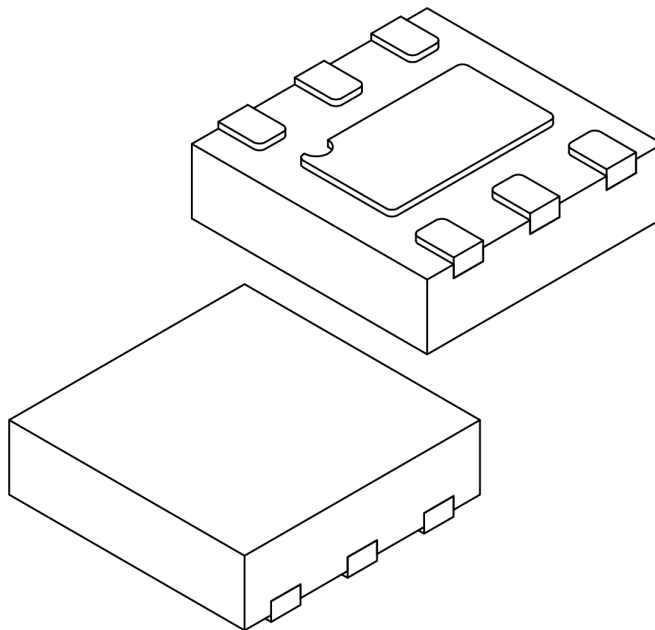


Microchip Technology Drawing C04-1156-HSA Rev A Sheet 1 of 2

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6-Lead Ultra Thin Plastic Dual Flat, No Lead Package (HSA) - 2x2x0.6 mm Body [UDFN] Micrel Legacy Package TDFN22-6LD-PL-1

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



		Units	MILLIMETERS		
Dimension Limits			MIN	NOM	MAX
Number of Terminals	N		6		
Pitch	e		0.65 BSC		
Overall Height	A		0.50	0.55	0.60
Standoff	A1		0.00	0.02	0.05
Terminal Thickness	A3		0.152 REF		
Overall Length	D		2.00 BSC		
Exposed Pad Length	D2		1.35	1.40	1.45
Overall Width	E		2.00 BSC		
Exposed Pad Width	E2		0.75	0.80	0.85
Terminal Width	b		0.20	0.25	0.30
Terminal Length	L		0.30	0.35	0.40
Terminal-to-Exposed-Pad	K		0.20	-	-

Notes:

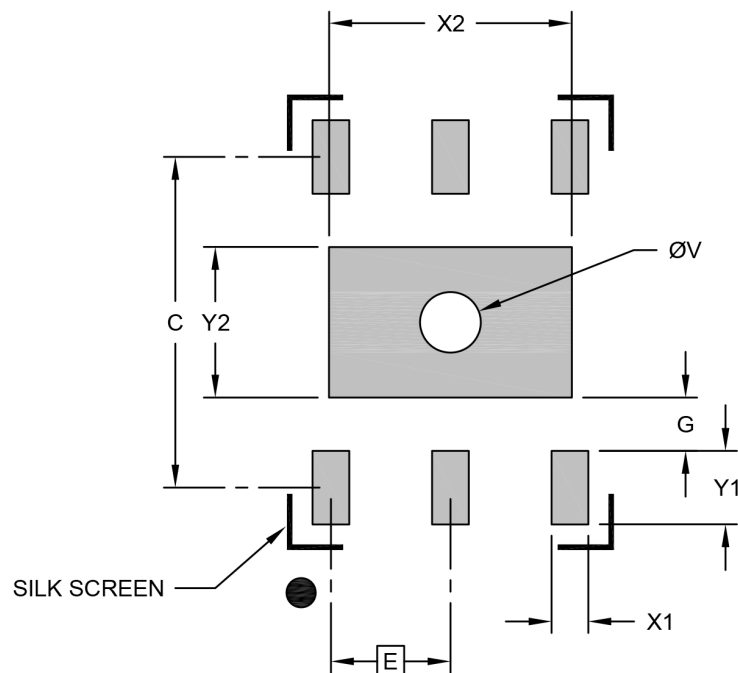
- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated
- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1156-HSA Rev A Sheet 2 of 2

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6-Lead Ultra Thin Plastic Dual Flat, No Lead Package (HSA) - 2x2x0.6 mm Body [UDFN] Micrel Legacy Package TDFN22-6LD-PL-1

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Center Pad Width	X2			1.32
Center Pad Length	Y2			0.82
Contact Pad Spacing	C		1.80	
Contact Pad Width (X6)	X1			0.20
Contact Pad Length (X6)	Y1			0.40
Contact Pad to Center Pad (X6)	G	0.29		
Thermal Via Diameter	V		0.33	

Notes:

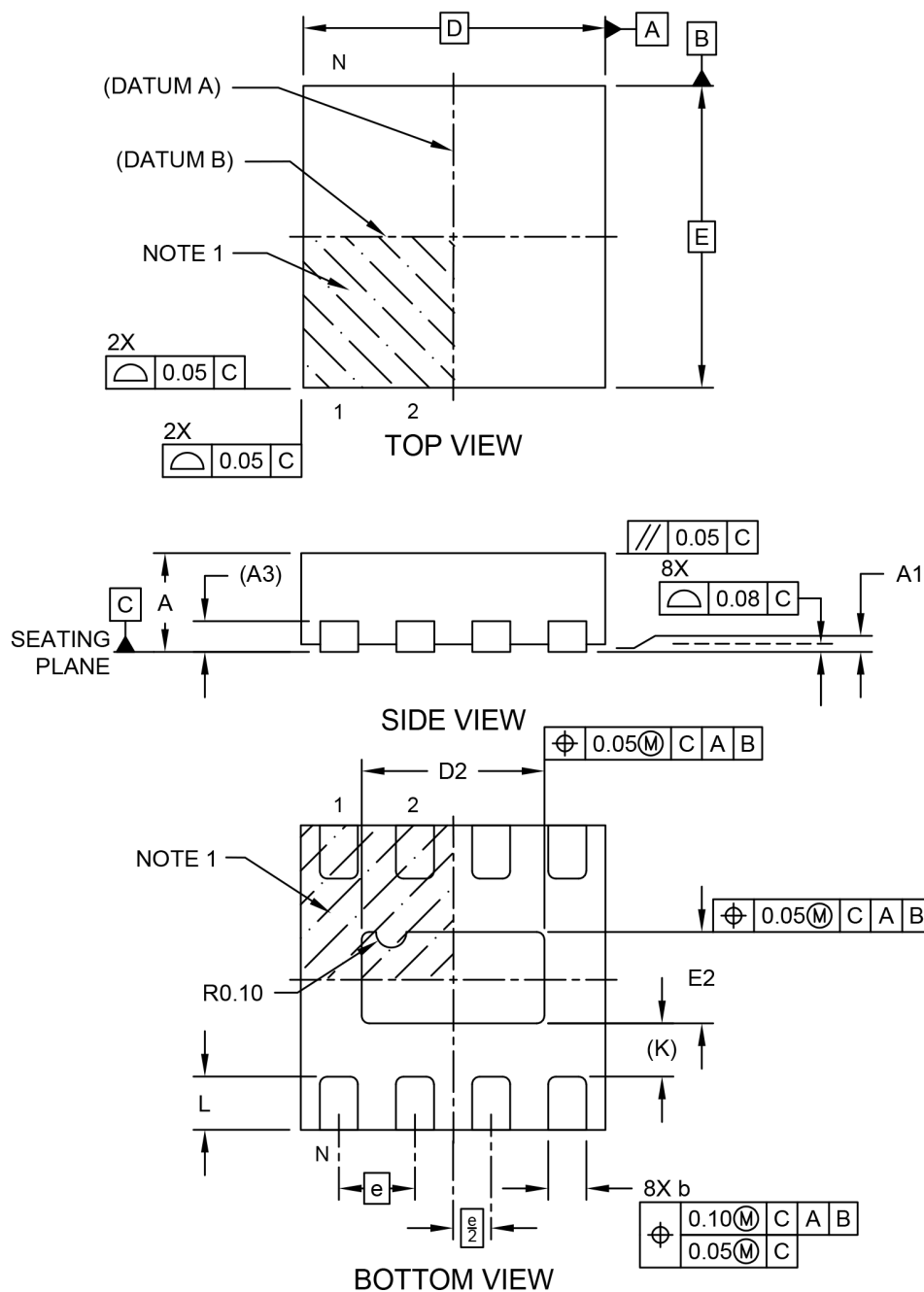
- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
- For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-3156-HSA Rev A

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8-Lead Ultra Thin Plastic Dual Flat, No Lead Package (HYA) - 2x2 mm Body [UDFN] With 1.2x0.6 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

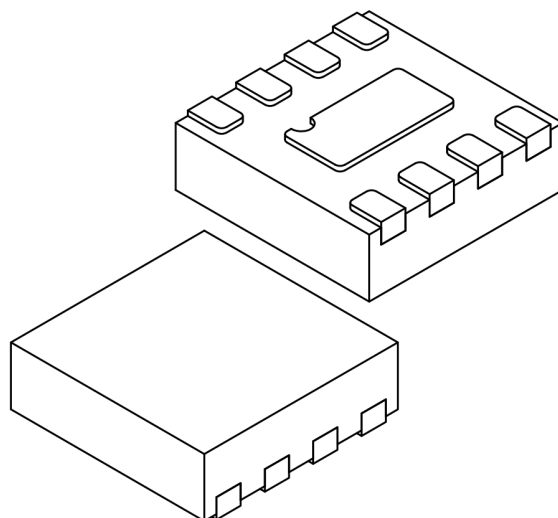


Microchip Technology Drawing C04-1158-HYA Rev C Sheet 1 of 2

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8-Lead Ultra Thin Plastic Dual Flat, No Lead Package (HYA) - 2x2 mm Body [UDFN] With 1.2x0.6 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N	8		
Pitch	e	0.50 BSC		
Overall Height	A	0.50	0.55	0.60
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3	0.152 REF		
Overall Length	D	2.00 BSC		
Exposed Pad Length	D2	1.10	1.20	1.30
Overall Width	E	2.00 BSC		
Exposed Pad Width	E2	0.50	0.60	0.70
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.30	0.35	0.40
Terminal-to-Exposed-Pad	K	0.35 REF		

Notes:

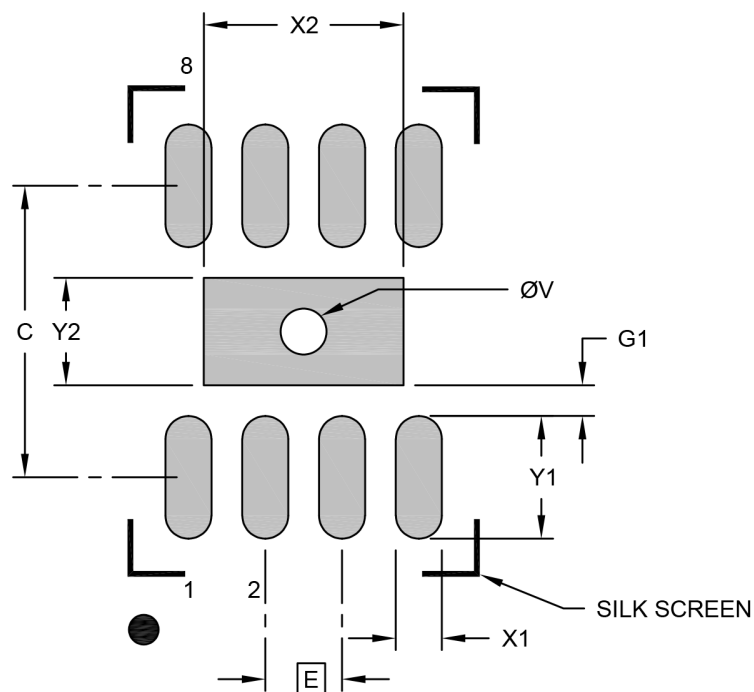
- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated
- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1158-HYA Rev C Sheet 2 of 2

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8-Lead Very Thin Plastic Dual Flat, No Lead Package (HYA) - 2x2 mm Body [UDFN] Micrel Legacy Package

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Optional Center Pad Width	X2			1.30
Optional Center Pad Length	Y2			0.70
Contact Pad Spacing	C		1.90	
Contact Pad Width (X8)	X1			0.30
Contact Pad Length (X8)	Y1			0.80
Contact Pad to Center Pad (X8)	G1	0.20		
Thermal Via Diameter	V		0.30	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-3158-HYA Rev. C

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9. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision	Date	Section	Description
DS20007151A	06/2026	—	Converted Micrel document MIC2790/1/3 to Microchip data sheet DS20007151A. Minor text changes throughout.

10. Product Identification System

PART NO.	XX	-XXX	XX	-XX
Device	Output	SNS Threshold Voltage	Package	Media Type
Device:	MIC2790: Supervisor with High-Accuracy, Ultra-Fast Propagation Delay, and Capacitor-Programmable Reset Delay MIC2791: Supervisor with High-Accuracy, Ultra-Fast Propagation Delay, and Capacitor-Programmable Reset Delay in 1.6mm x 1.6mm UDFN Package MIC2793: Supervisor with High-Accuracy, Ultra-Fast Propagation Delay, Capacitor-Programmable Reset Delay, and Active High Enable Pin			
Output:	H = Open-Drain /RESET Output (Active-Low) L = Push-Pull /RESET Output (Active-Low) N = Push-Pull RESET Output (Active-High) LH = Push-Pull /RESET Output (Active-Low) and Push-Pull RESET Output (Active-High) (MIC2793 only) NH = Open-Drain /RESET Output (Active-Low) and Push-Pull RESET Output (Active-High) (MIC2793 only)			
SNS Threshold Voltage:	04V = 0.4V			
Package:	D6 = 6-Lead TSOT-23 (MIC2790 only) MT = 6-Lead 1.6mm x 1.6mm UDFN (MIC2791 only) MT = 6-Lead 2mm x 2mm UDFN (MIC2790 only) MT = 8-Lead 2mm x 2mm UDFN (MIC2793 only)			
Media Type:	TR = 500/Reel (TSOT-23 only) TR = 5,000/Reel (UDFN only)			

Examples:

- MIC2790N-04VDG-TR: MIC2790, Open-Drain /RESET Output (Active-Low), 0.4V SNS Threshold Voltage, 6-Lead TSOT-23, 500/Reel
- MIC2791L-04VMT-TR: MIC2791, L = Push-Pull /RESET Output (Active-Low), 0.4V SNS Threshold Voltage, 6-Lead 1.6mm x 1.6mm UDFN, 5,000/Reel
- MIC2793NH-04VMT-TR: MIC2793, Open-Drain /RESET Output (Active-Low) and Push-Pull RESET Output (Active-High), 0.4V SNS Threshold Voltage, 8-Lead 2mm x 2mm UDFN, 5,000/Reel

Note:

Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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