EMC1464

Four Channel 1°C Temperature Sensor with Beta Compensation

Features

- Programmable SMBus Address
- Support for Diodes requiring the BJT/Transistor: Supports advanced process substrate thermal diodes such as CPU, GPU and FPGACPU thermal diodes
- Pin Compatible with EMC1414 and EMC1444
- Automatically Determines External Diode Type and Optimal Settings
- Resistance Error Correction
- Up to 3 External Temperature Monitors:
  - ±1°C max accuracy (20°C < T_{DIODE} < 110°C)
  - 0.125°C resolution
  - Supports up to 2.2 nF diode filter capacitor
- Internal Temperature Monitor:
  - ±1°C accuracy
  - 0.125°C resolution
- 3.3V Supply Voltage
- Programmable Temperature Limits for:
  - $\overline{\text{ALERT}}$: 85°C default high limit and 0°C default low limit
  - $\overline{\text{THERM}}$: 125°C default
- Available in the Following Package Types:
  - 10-Lead 3 mm x 3 mm VDFN
  - 10-Lead 2.5 mm x 2 mm VDFN

  Lead-Free RoHS Compliant Packages

Typical Applications

- Notebook Computers
- Desktop Computers
- Industrial
- Embedded Applications

General Description

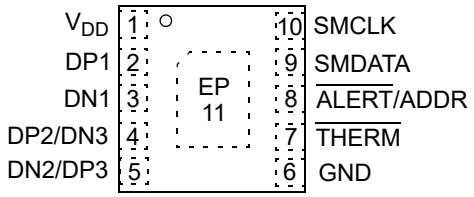
The EMC1464 is a high accuracy, low cost, System Management Bus (SMBus) temperature sensor. Advanced features such as Resistance Error Correction (REC), Beta Compensation (to support CPU diodes requiring the BJT/transistor model) and automatic diode type detection combine to provide a robust solution for complex environmental monitoring applications.

The EMC1464 monitors four temperature channels (three external and one internal), providing ±1°C accuracy for both external and internal diode temperatures.

REC automatically eliminates the temperature error caused by series resistance, allowing greater flexibility in routing thermal diodes. Beta Compensation eliminates temperature errors caused by low, variable beta transistors common in today's fine geometry processors. The automatic beta detection feature monitors the external diode/transistor and determines the optimum sensor settings for accurate temperature measurements, regardless of processor technology. This frees the user from providing unique sensor configurations for each temperature monitoring application. These advanced features, plus ±1°C measurement accuracy, provide a low-cost, highly flexible and accurate solution for critical temperature monitoring applications.

Package Type

EMC1464
10-Lead VDFN*



* Includes Exposed Thermal Pad (EP), see Table 3-1.

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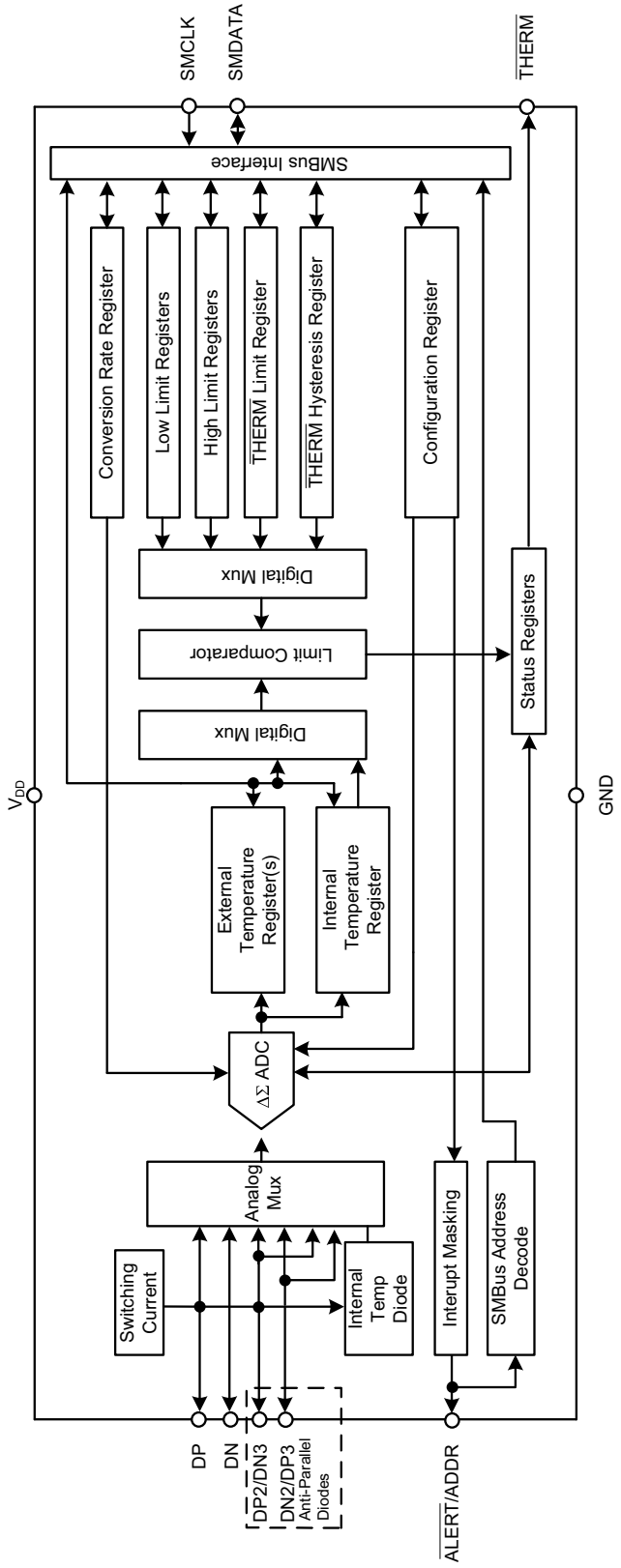
EMC1464 – Functional Block Diagram



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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Supply Voltage (V_{DD}) ..... -0.3V to +4V
Voltage on 5V tolerant pins (V_{5VT_pin}) ..... -0.3V to +5.5V
Voltage on 5V tolerant pins ($|V_{5VT_pin}$ - VDD|) ..... 0V to +3.6V(**Note 1**)
Voltage on any other pin to ground ..... -0.3V to V_{DD} +0.3V
Storage Temperature ..... -55°C to +150°C
Operating Temperature ..... -40°C to +125°C
Lead Temperature ..... refer to JEDEC Spec. J-STD-020
ESD Rating All pins, HBM 2000V
Junction Temperature (T_J) ..... -40°C to +125°C

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: For the 5V tolerant pins that have a pull-up resistor (SMCLK, SMDATA, $\overline{\text{THERM}}$ and $\overline{\text{ALERT}}$), the pull-up voltage must not exceed 3.6V when the device is unpowered.

ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, V_{DD} = 3.0V to 3.6V, T_A = -40°C to 125°C, all typical values at T_A = 27°C.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
DC Power						
Supply Voltage	V_{DD}	3.0	3.3	3.6	V	xLI = xHI = 0V
Supply Current	I_{DD}	—	430	850	µA	1 conversion/sec. dynamic averaging disabled
		—	930	1200		4 conversions/sec. dynamic averaging enabled
		—	1120	—		≥ 16 conversions/sec. dynamic averaging enabled
Standby Supply Current	I_{DD}	—	170	230	µA	Device in Standby mode no SMBus communications $\overline{\text{ALERT}}$ and $\overline{\text{THERM}}$ pins not asserted
Internal Temperature Monitor						
Temperature Accuracy	—	—	±0.25	±1	°C	-5°C < T_A < 100°C
		—	±0.5	±2	°C	-40°C < T_A < 125°C
Temperature Resolution	—	—	0.125	—	°C	
External Temperature Monitor						
Temperature Accuracy	—	—	±0.25	±1	°C	+20°C < T_{DIODE} < +110°C 0°C < T_A < 100°C
		—	—	±2	°C	-40°C < T_{DIODE} < 127°C
Temperature Resolution	—	—	0.125	—	°C	

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ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, V_{DD} = 3.0V to 3.6V, T_A = -40°C to 125°C, all typical values at T_A = 27°C.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Conversion Time, all channels	t_{CONV}	—	190	—	ms	Default settings
Capacitive Filter	C_{FILTER}	—	2.2	2.7	nF	Connected across external diode
$\overline{\text{ALERT}}$ and $\overline{\text{THERM}}$ Pins						
Output Low Voltage	V_{OL}	0.4	—	—	V	I_{SINK} = 8 mA
Leakage Current	I_{LEAK}	—	—	±5	µA	$\overline{\text{ALERT}}$ and $\overline{\text{THERM}}$ pins Device powered or unpowered T_A < 85°C, Pull-Up Voltage ≤ 3.6V

SMBUS ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, V_{DD} = 3.0V to 3.6V, T_A = -40°C to 125°C, all typical values at T_A = 27°C.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
SMBus Interface						
Input High Voltage	V_{IH}	2.0	—	V_{DD}	V	5V tolerant
Input Low Voltage	V_{IL}	-0.3	—	0.8	V	5V tolerant
Leakage Current	I_{LEAK}	—	—	±5	µA	Device in Standby mode no SMBus communications $\overline{\text{ALERT}}$ and $\overline{\text{THERM}}$ pins not asserted
Hysteresis	—	—	420	—	mV	
Input Capacitance	C_{IN}	—	5	—	pF	
Output Low Sink Current	I_{OL}	8.2	—	15	mA	SMDATA = 0.4V
SMBus Timing						
Clock Frequency	f_{SMB}	10	—	400	kHz	
Spike Suppression	t_{SP}	—	—	50	ns	
Bus Free Time Stop-to-Start	t_{BUF}	1.3	—	—	µs	
Hold Time: Start	$t_{HD:STA}$	0.6	—	—	µs	
Setup Time: Start	$t_{SU:STA}$	0.6	—	—	µs	
Setup Time: Stop	$t_{SU:STO}$	0.6	—	—	µs	
Data Hold Time	$t_{HD:DAT}$	0	—	—	µs	When transmitting to the master
Data Hold Time	$t_{HD:DAT}$	0.3	—	—	µs	When receiving from the master
Data Setup Time	$t_{SU:DAT}$	100	—	—	ns	
Clock Low Period	t_{LOW}	1.3	—	—	µs	
Clock High Period	t_{HIGH}	0.6	—	—	µs	
Clock/Data Fall Time	t_{FALL}	—	—	300	ns	Min = 20 + 0.1 C_{LOAD} ns
Clock/Data Rise Time	t_{RISE}	—	—	300	ns	Min = 20 + 0.1 C_{LOAD} ns
Capacitive Load	C_{LOAD}	—	—	400	pF	Per bus line
Timeout	$t_{TIMEOUT}$	25	—	35	ms	Disabled by default

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TEMPERATURE CHARACTERISTICS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Specified Temperature Range (**Note 1**)	T_A	-40	—	+125	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	
Storage Temperature Range	T_S	-55	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance 10LD 3 mm x 3 mm VDFN	θ_{JA}	—	89	—	°C/W	
Thermal Resistance 10LD 2.5 mm x 2 mm VDFN	θ_{JA}	—	89	—	°C/W	

Note 1: Operation in this range must not cause T_J to exceed Maximum Junction Temperature (+125°C).

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

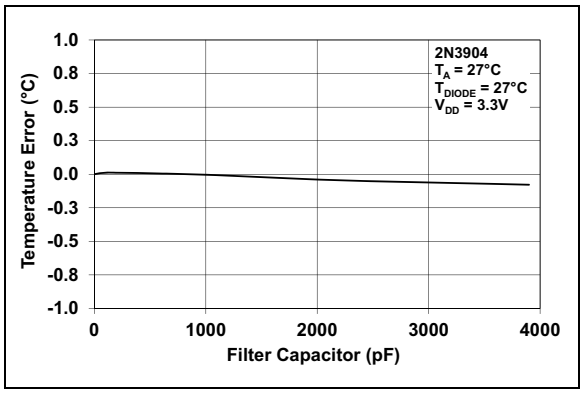

FIGURE 2-1: *Temperature Error vs. Filter Capacitor.*

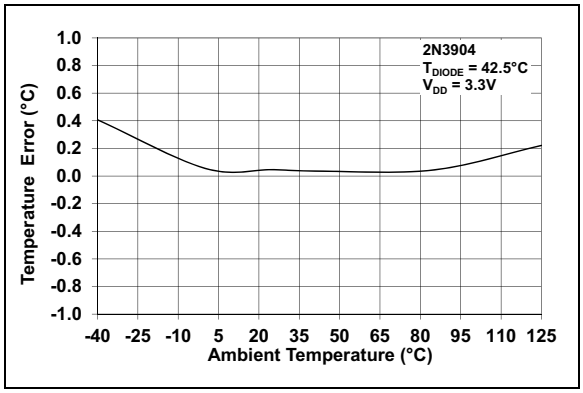

FIGURE 2-2: *Temperature Error vs. Ambient Temperature.*

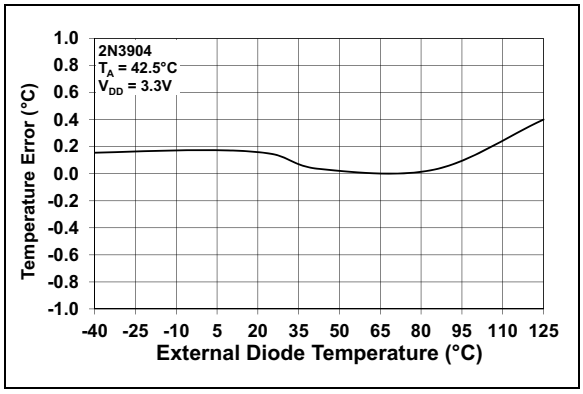

FIGURE 2-3: *Temperature Error vs. External Diode Temperature.*

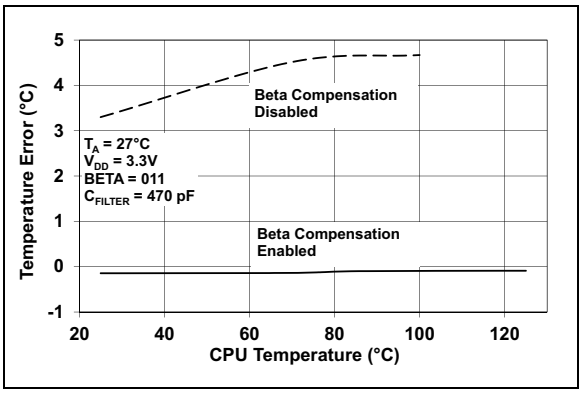

FIGURE 2-4: *Temperature Error vs. CPU Temperature, Typical 65 nm CPU from Major Vendor.*

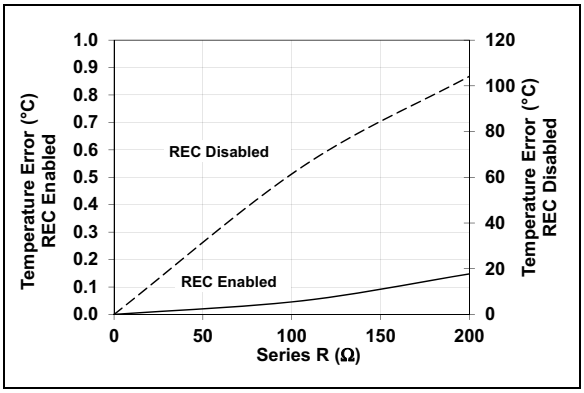

FIGURE 2-5: *Temperature Error vs. Series Resistance.*

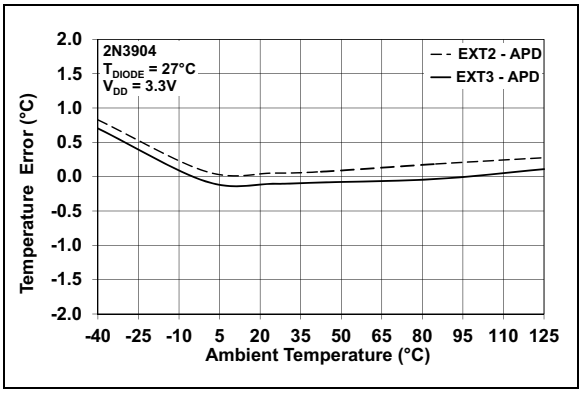

FIGURE 2-6: *Temperature Error vs. Ambient Temperature.*

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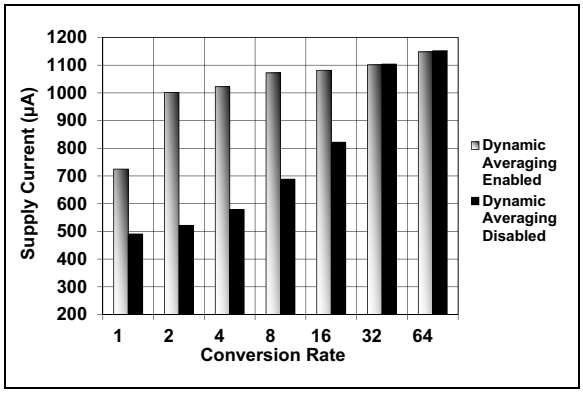

FIGURE 2-7: *Supply Current vs. Conversion Rate.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE (Note 1)

VDFN-10LD	Symbol	Type	Description
1	V_{DD}	Power	Power Supply
2	DP1	AIO	External Diode 1 Positive (Anode) Connection
3	DN1	AIO	External Diode 1 Negative (Cathode) Connection
4	DP2/DN3	AIO	External Diode 2 Positive (Anode) Connection/External Diode 3 Negative (Cathode) Connection for Anti-Parallel Diodes
5	DN2/DP3	AIO	External Diode 2 Negative (Cathode) Connection/External Diode 3 Positive (Anode) Connection for Anti-Parallel Diodes
6	GND	Power	Ground
7	$\overline{\text{THERM}}$	OD (5V)	Critical $\overline{\text{THERM}}$ Output Signal Requires pull-up resistor.
8	$\overline{\text{ALERT}}$/ADDR	OD (5V)	$\overline{\text{ALERT}}$ - Active Low Digital Output Signal Requires pull-up resistor.
			ADDR Selects SMBus address based on pull-up resistor.
9	SMDATA	DIOD (5V)	SMBus Data Input/Output Requires pull-up resistor.
10	SMCLK	DI (5V)	SMBus Clock Input Requires pull-up resistor.
11	Exposed Pad	—	Not internally connected, but grounding recommended

Note 1: For the 5V tolerant pins that have a pull-up resistor (SMCLK, SMDATA, $\overline{\text{THERM}}$, and $\overline{\text{ALERT}}$), the voltage difference between V_{DD} and the pull-up voltage must never exceed 3.6V.

The pin types are described in Table 3-2.

TABLE 3-2: PIN TYPES

Pin Type	Description
Power	This pin is used to supply power or ground to the device.
AIO	Analog Input/Output This pin is used as an I/O for analog signals.
DI	Digital Input This pin is used as a digital input. This pin is 5V tolerant.
DIOD	Digital Input/Open Drain Output This pin is used as a digital I/O. When used as an output, it is open drain and requires a pull-up resistor. This pin is 5V tolerant.
OD	Open Drain Digital Output This pin is used as a digital output. It is open drain and requires a pull-up resistor. This pin is 5V tolerant.

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4.0 FUNCTIONAL DESCRIPTION

The EMC1464 is an SMBus temperature sensor. The EMC1464 monitors one internal diode and up to three externally connected temperature diodes.

Thermal management is performed in cooperation with a host device. This consists of the host reading the temperature data of both the external and internal temperature diodes of the EMC1464 and using that data to control the speed of one or more fans.

The EMC1464 has two levels of monitoring. The first provides a maskable $\overline{\text{ALERT}}$ signal to the host when the measured temperatures exceed user programmable limits. This allows the EMC1464 to be used as an independent thermal watchdog to warn the host of temperature hot spots without direct control by the host. The second level of monitoring provides a non-maskable interrupt on the $\overline{\text{THERM}}$ pin if the measured temperatures meet or exceed a second programmable limit.

For the EMC1464, External Diode channels 2 and 3 are only compatible with general purpose diodes (such as a 2N3904). Figure 4-1 shows a system-level block diagram of the EMC1464.

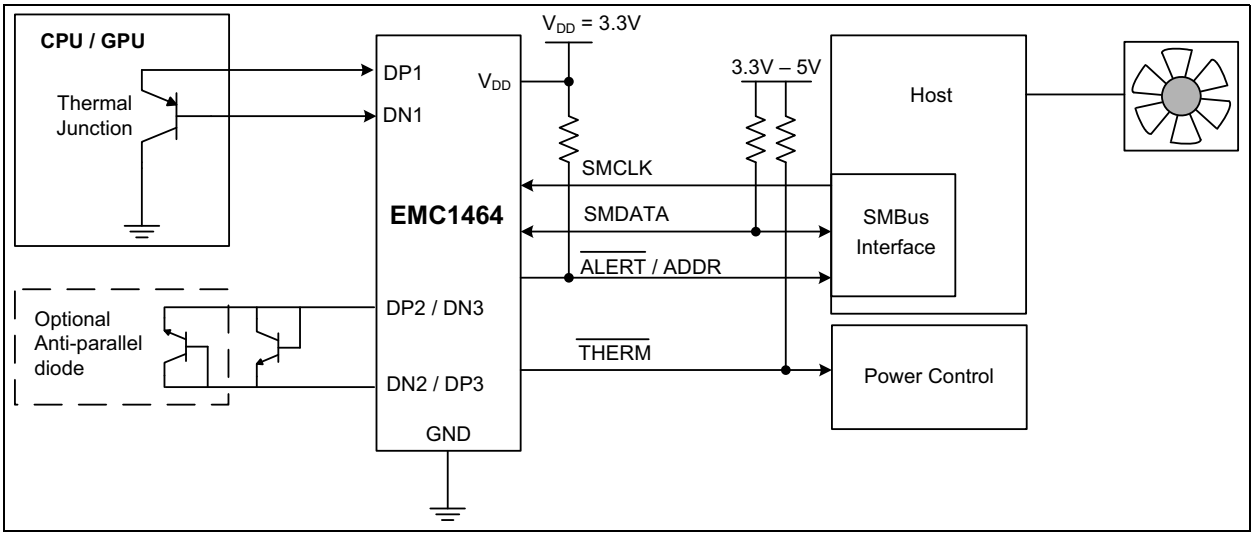

FIGURE 4-1: *EMC1464 - System-Level Block Diagram.*

4.1 Modes of Operation

The EMC1464 has two modes of operation:

- Active (Run) – in this mode of operation, the ADC is converting on all temperature channels at the programmed conversion rate. The temperature data is updated at the end of every conversion and the limits are checked. In Active mode, writing to the one-shot register will do nothing.
- Standby (Stop) – in this mode of operation, the majority of circuitry is powered down to reduce supply current. The temperature data is not updated and the limits are not checked. In this mode of operation, the SMBus is fully active and the part will return requested data. Writing to the one-shot register will enable the device to update all temperature channels. Once all the channels are updated, the device will return to the Standby mode.

4.1.1 CONVERSION RATES

The EMC1464 may be configured for different conversion rates based on the system requirements. The conversion rate is configured as described in **Section 6.5 "Conversion Rate Register"**. The default conversion rate is 4 conversions per second. Other available conversion rates are shown in Table 6-3.

4.1.2 DYNAMIC AVERAGING

Dynamic averaging causes the EMC1464 to measure the external diode channels for an extended time based on the selected conversion rate. This functionality can be disabled for increased power savings at the lower conversion rates (see **Section 6.4 "Configuration Register"**. When dynamic averaging is enabled, the device will automatically adjust the sampling and measurement time for the external diode channels. This allows the device to average 2x or 16x longer than the normal 11-bit operation (nominally 21 ms per channel) while still maintaining the selected conversion rate. The benefits of dynamic averaging are improved noise rejection due to the longer integration time, as well as less random variation of the temperature measurement.

When enabled, the dynamic averaging applies when a one-shot command is issued. The device will perform the desired averaging during the one-shot operation according to the selected conversion rate.

When enabled, the dynamic averaging will affect the average supply current based on the chosen conversion rate as shown in Table 4-1.

TABLE 4-1: EMC1464 – SUPPLY CURRENT VS. CONVERSION RATE

Conversion Rate	Average Supply Current		Averaging Factor (based on 11-bit operation)	
	Enabled (Default)	Disabled	Enabled (Default)	Disabled
1/16s	660 µA	430 µA	16x	1x
1/8s	660 µA	430 µA	16x	1x
1/4s	660 µA	430 µA	16x	1x
1/2s	660 µA	430 µA	16x	1x
1/s	660 µA	430 µA	8x	1x
2/s	930 µA	475 µA	4x	1x
4/s (default)	950 µA	510 µA	2x	1x
8/s	1010 µA	630 µA	1x	1x
16/s	1020 µA	775 µA	0.5x	0.5x
32/s	1050 µA	1050 µA	0.25x	0.25x
64/s	1100 µA	1100 µA	0.125x	0.125x

4.2 $\overline{\text{ALERT}}$ Output

The $\overline{\text{ALERT}}$ pin is an open drain output and requires a pull-up resistor to V_{DD}.

It has two modes of operation:

- interrupt mode
- comparator mode

The mode of the $\overline{\text{ALERT}}$ output is selected via the ALERT/COMP bit in the Configuration Register (see **Section 6.4 "Configuration Register"**).

4.2.1 $\overline{\text{ALERT}}$ PIN INTERRUPT MODE

When configured to operate in Interrupt mode, the $\overline{\text{ALERT}}$ pin asserts low when an out-of-limit measurement (≥ high limit or < low limit) is detected on any diode or when a diode fault is detected. The $\overline{\text{ALERT}}$ pin will remain asserted as long as an out-of-limit condition remains. Once the out-of-limit condition has been removed, the $\overline{\text{ALERT}}$ pin will remain asserted until the appropriate status bits are cleared.

The $\overline{\text{ALERT}}$ pin can be masked by setting the MASK_ALL bit. When the $\overline{\text{ALERT}}$ pin has been masked, it will be deasserted and remain deasserted until the MASK_ALL bit is cleared by the user. Any interrupt conditions that occur while the $\overline{\text{ALERT}}$ pin is masked will update the Status Register normally. There are also individual channel masks (see **Section 6.12 "Consecutive Alert Register"**).

The $\overline{\text{ALERT}}$ pin is used as an interrupt signal or as an SMBus Alert signal that allows an SMBus target to communicate an error condition to the master. One or more $\overline{\text{ALERT}}$ outputs can be hard-wired together.

4.2.2 $\overline{\text{ALERT}}$ PIN COMPARATOR MODE

When the $\overline{\text{ALERT}}$ pin is configured to operate in Comparator mode, it will be asserted if any of the measured temperatures exceeds the respective high limit. The $\overline{\text{ALERT}}$ pin will remain asserted until all temperatures drop below the corresponding high limit minus the Therm Hysteresis value.

When the $\overline{\text{ALERT}}$ pin is asserted in Comparator mode, the corresponding high limit status bits will be set. Reading these bits will not clear them until the $\overline{\text{ALERT}}$ pin is deasserted. Once the $\overline{\text{ALERT}}$ pin is deasserted, the status bits will be automatically cleared.

The MASK_ALL bit will not block the $\overline{\text{ALERT}}$ pin in this mode; however, the individual channel masks (see **Section 6.11 "Channel Mask Register"**) will prevent the respective channel from asserting the $\overline{\text{ALERT}}$ pin.

4.2.3 $\overline{\text{ALERT}}$ PIN CONSIDERATIONS

Because of the decode method used to determine the SMBus Address, it is important that the pull-up resistance on the $\overline{\text{ALERT}}$ pin be within the tolerances shown in Table . Additionally, the pull-up resistor on the $\overline{\text{ALERT}}$ pin must be connected to the same 3.3V supply that drives the V_{DD} pin.

For 15 ms after power up, the $\overline{\text{ALERT}}$ pin must not be pulled low or the SMBus Address will not be decoded properly. If the system requirements do not permit this condition, the $\overline{\text{ALERT}}$ pin must be isolated from its hard-wired OR'd bus during this time.

One method of isolating this pin is shown in Figure 4-2.

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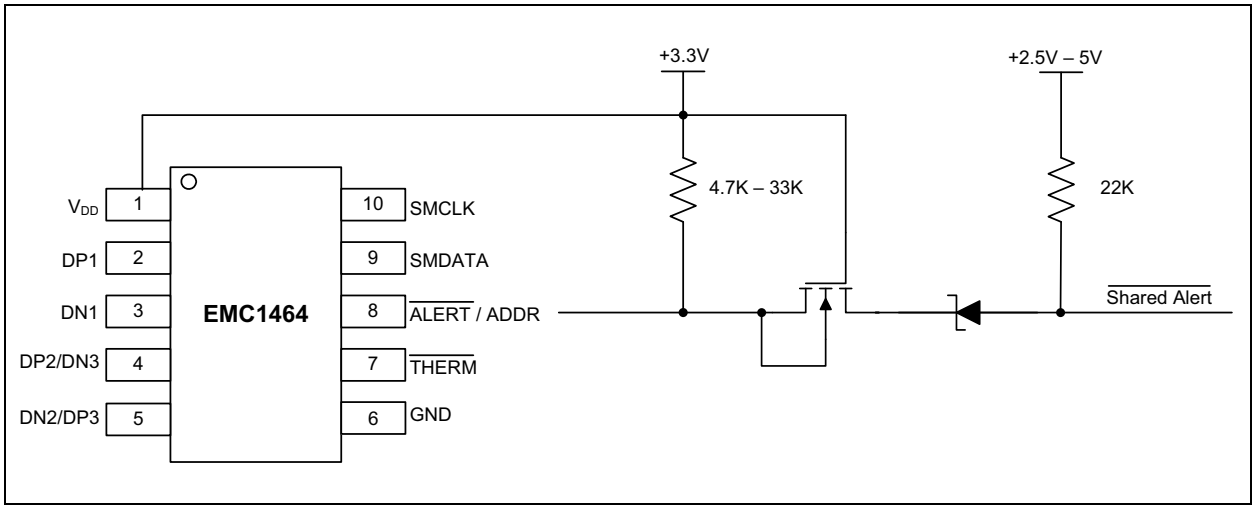

FIGURE 4-2: *Isolating the ALERT pin.*

4.3 Temperature Measurement

The EMC1464 can monitor the temperature of up to three externally connected diodes.

The device contains programmable High, Low, and Therm limits for all measured temperature channels. If the measured temperature goes below the Low limit or above the High limit, the ALERT pin can be asserted (based on user settings). If the measured temperature meets or exceeds the Therm Limit, the THERM pin is asserted unconditionally, providing two tiers of temperature detection.

4.3.1 BETA COMPENSATION

The EMC1464 is configured to monitor the temperature of basic diodes (e.g., 2N3904) or CPU thermal diodes. It automatically detects the type of external diode (CPU diode or diode connected transistor) and determines the optimal setting to reduce temperature errors introduced by beta variation. Compensating for this error is also known as implementing the transistor or BJT model for temperature measurement.

For discrete transistors configured with the collector and base shorted together, the beta is generally sufficiently high such that the percent change in beta variation is very small. For example, a 10% variation in beta for two forced emitter currents with a transistor whose ideal beta is 50 would contribute approximately 0.25°C error at 100°C. However, for substrate transistors where the base-emitter junction is used for temperature measurement and the collector is tied to the substrate, the proportional beta variation will cause a large error. For example, a 10% variation in beta for two forced emitter currents with a transistor whose ideal beta is 0.5 would contribute approximately 8.25°C error at 100°C.

4.3.2 RESISTANCE ERROR CORRECTION (REC)

Parasitic resistance in series with the external diodes will limit the accuracy obtainable from temperature measurement devices. The voltage developed across this resistance by the switching diode currents cause the temperature measurement to read higher than the true temperature. Contributors to series resistance are PCB trace resistance, on die (i.e., on the processor) metal resistance, bulk resistance in the base, and emitter of the temperature transistor. Typically, the error caused by series resistance is +0.7°C per ohm. The EMC1464 automatically corrects up to 100 ohms of series resistance.

4.3.3 PROGRAMMABLE EXTERNAL DIODE IDEALITY FACTOR

The EMC1464 is designed for external diodes with an ideality factor of 1.008. Not all external diodes, processor or discrete, will have this exact value. This variation of the ideality factor introduces error in the temperature measurement that must be corrected. This correction is typically done using programmable offset registers. Since an ideality factor mismatch introduces an error that is a function of temperature, this correction is only accurate within a small range of temperatures. To provide maximum flexibility to the user, the EMC1464 features a 6-bit register for each external diode where the ideality factor of the diode used is programmed to eliminate errors across all temperatures.

Note:	When monitoring a substrate transistor or CPU diode and beta compensation is enabled, the Ideality Factor should not be adjusted. Beta Compensation automatically corrects for most ideality errors.

4.4 Diode Faults

The EMC1464 detects an open on the DP and DN pins, and a short across the DP and DN pins. For each temperature measurement made, the device checks for a diode fault on the external diode channel(s). When a diode fault is detected, the ALERT pin asserts (unless masked, see **Section 4.5 "Consecutive Alerts"**) and the temperature data reads 00h in the MSB and LSB registers. Note: the low limit will not be checked. A diode fault is defined as one of the following: an open between DP and DN, a short from V_{DD} to DP, or a short from V_{DD} to DN.

If a short occurs across DP and DN or a short occurs from DP to GND, the low limit status bit is set and the ALERT pin asserts (unless masked). This condition is indistinguishable from a temperature measurement of 0.000°C (-64°C in extended range) resulting in temperature data of 00h in the MSB and LSB registers.

If a short from DN to GND occurs (with a diode connected), temperature measurements will continue as normal with no alerts.

4.5 Consecutive Alerts

The EMC1464 contains multiple consecutive alert counters. One set of counters applies to the ALERT pin and the second set of counters applies to the THERM pin. Each temperature measurement channel has a separate consecutive alert counter for each of the ALERT and THERM pins. All counters are user programmable and determine the number of consecutive measurements that a temperature channel(s) must be out-of-limit or reporting a diode fault before the corresponding pin is asserted.

See **Section 6.12 "Consecutive Alert Register"** for more details on the consecutive alert function.

4.6 Digital Filter

To reduce the effect of noise and temperature spikes on the reported temperature, the External Diode 1 channel uses a programmable digital filter. This filter can be configured as Level 1, Level 2, or Disabled (default) (see **Section 6.18 "Filter Control Register"**). The typical filter performance is shown in Figure 4-3 and Figure 4-4.

4.7 Temperature Measurement Results and Data

The temperature measurement results are stored in the internal and external temperature registers. These are then compared with the values stored in the high and low limit registers. Both external and internal temperature measurements are stored in 11-bit format with the 8 MSbs stored in a high byte register and the 3 LSbs stored in the 3 MSb positions of the low byte register. All other bits of the low byte register are set to zero.

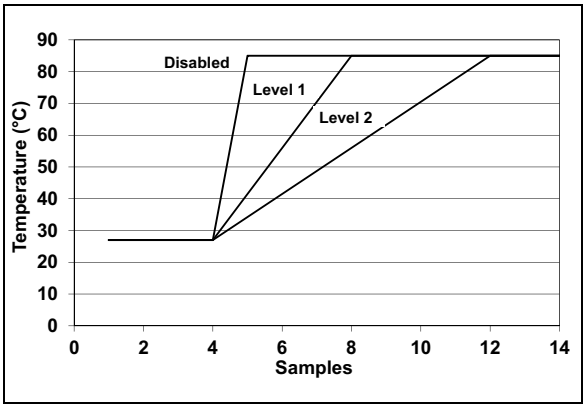

FIGURE 4-3: *Temperature Filter Step Response.*

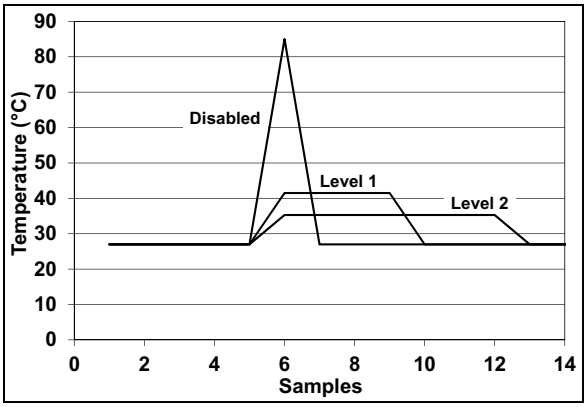

FIGURE 4-4: *Temperature Filter Impulse Response.*

The EMC1464 has two selectable temperature ranges – the default range and the extended range.

The default range is from 0°C to +127°C. The temperature is represented as a binary number that is able to report a temperature from 0°C to +127.875°C in 0.125°C steps.

The extended range is an extended temperature range from -64°C to +191°C. The data format is a binary number offset by 64°C. The extended range is used to measure temperature diodes with a large known offset (such as AMD processor diodes) where the diode temperature plus the offset would be equivalent to a temperature higher than +127°C.

Table 4-2 shows the default and extended range formats.

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TABLE 4-2: TEMPERATURE DATA FORMAT

Temperature (°C)	Default Range 0°C to +127°C	Extended Range -64°C to +191°C
Diode Fault	000 0000 0000	000 0000 0000
-64	000 0000 0000	000 0000 0000 (2)
-1	000 0000 0000	001 1111 1000
0	000 0000 0000 (1)	010 0000 0000
0.125	000 0000 0001	010 0000 0001
1	000 0000 1000	010 0000 1000
64	010 0000 0000	100 0000 0000
65	010 0000 1000	100 0000 1000
127	011 1111 1000	101 1111 1000
127.875	011 1111 1111	101 1111 1111
128	011 1111 1111 (3)	110 0000 0000
190	011 1111 1111	111 1111 0000
191	011 1111 1111	111 1111 1000
≥ 191.875	011 1111 1111	111 1111 1111 (4)

Note 1: In default range, all temperatures < 0°C will be reported as 0°C.

2: In extended range, all temperatures < -64°C will be reported as -64°C.

3: In default range, all temperatures > +127.875°C will be reported as +127.875°C.

4: In extended range, all temperatures > +191.875°C will be reported as +191.875°C.

4.8 Anti-Parallel Diode Connections

The EMC1464 supports reading two external diodes on the same set of pins (DP2, DN2). These diodes are connected as shown in Figure 4-1. Due to the anti-parallel connection of these diodes, both diodes will be reverse biased by a V_{BE} voltage (approximately 0.7V). Because of this reverse bias, only discrete thermal diodes (such as 2N3904) are recommended to be placed on these pins.

4.9 External Diode Connections

The EMC1464 can be configured to measure a CPU substrate transistor, a discrete 2N3904 thermal diode, or an AMD processor diode on the External Diode 1 channel only. The diodes can be connected as indicated in Figure 4-5.

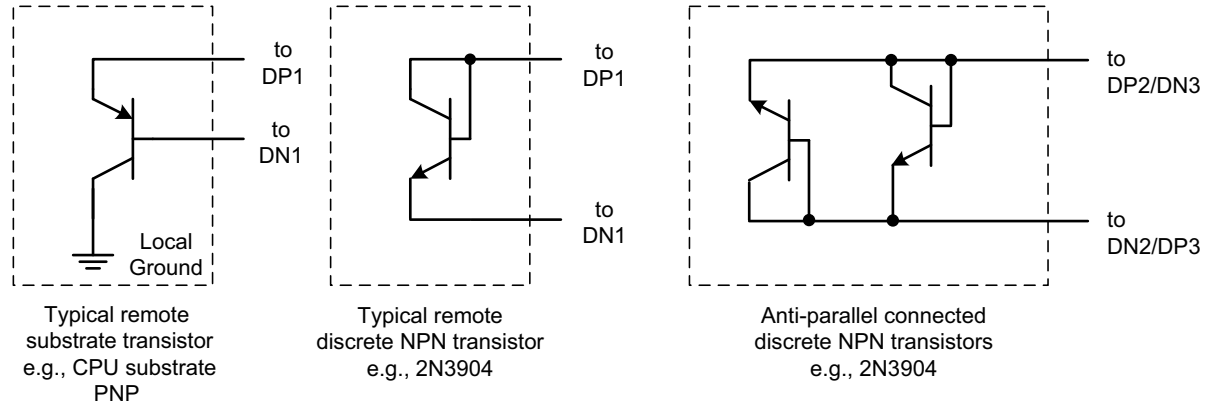

FIGURE 4-5: *Diode Configurations.*

5.0 SYSTEM MANAGEMENT BUS INTERFACE PROTOCOL

5.1 Communications Protocol

The EMC1464 communicates with a host controller, such as an SMSC SIO, through the SMBus. The SMBus is a two-wire serial communication protocol between a computer host and its peripheral devices. A detailed timing diagram is shown in Figure 5-1.

For the first 15 ms after power-up the device may not respond to SMBus communications.

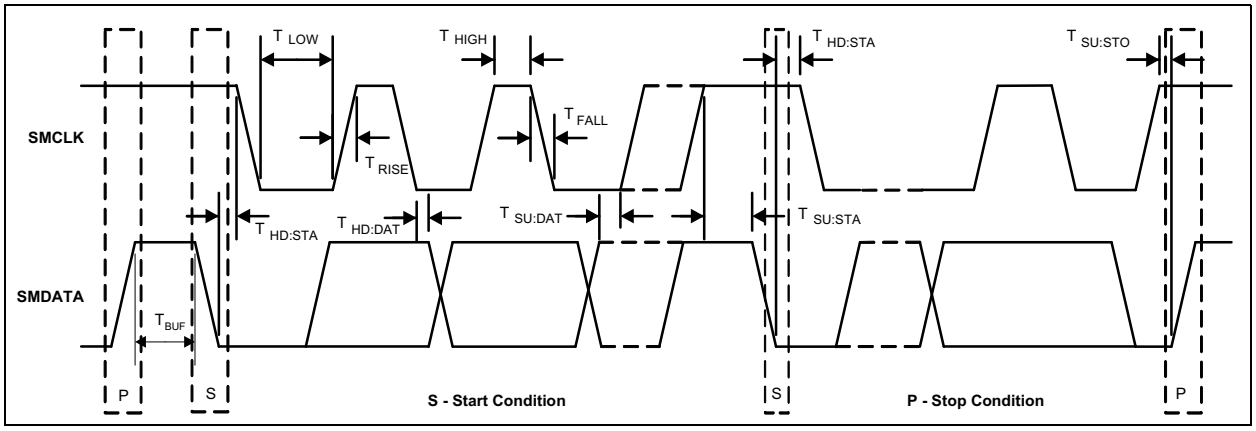

FIGURE 5-1: *SMBus Timing Diagram.*

5.1.1 SMBUS START BIT

The SMBus Start bit is defined as a transition of the SMBus Data line from a logic '1' state to a logic '0' state while the SMBus Clock line is in a logic '1' state.

5.1.2 SMBUS ADDRESS AND RD/$\overline{\text{WR}}$ BIT

The SMBus Address Byte consists of the 7-bit client address followed by the RD/$\overline{\text{WR}}$ indicator bit. If this RD/$\overline{\text{WR}}$ bit is a logic '0', the SMBus Host is writing data to the client device. If this RD/$\overline{\text{WR}}$ bit is a logic '1', the SMBus Host is reading data from the client device.

The EMC1464-A SMBus target address is determined by the pull-up resistor on the $\overline{\text{ALERT}}$ pin, as shown in Table .

The Address decode is performed by pulling known currents from V_{DD} through the external resistor, causing the pin voltage to drop, based on the respective current/resistor relationship. This pin voltage is compared against a threshold that determines the value of the pull-up resistor.

5.1.3 SMBUS DATA BYTES

All SMBus data bytes are sent, MSb first, and composed of 8-bits of information.

TABLE 5-1: SMBUS ADDRESS DECODE

Pull-Up Resistor on $\overline{\text{Alert}}$ Pin (±5%)	SMBus Address
4.7k	1111_100(r/$\overline{\text{w}}$)b
6.8k	1011_100(r/$\overline{\text{w}}$)b
10k	1001_100(r/$\overline{\text{w}}$)b
15k	1101_100(r/$\overline{\text{w}}$)b
22k	0011_100(r/$\overline{\text{w}}$)b
33k	0111_100(r/$\overline{\text{w}}$)b

5.1.4 SMBUS ACK AND NACK BITS

The SMBus client will acknowledge all data bytes that it receives. This is done by the client device pulling the SMBus data line low after the 8th bit of each byte that is transmitted. This applies to the Write Byte protocol.

The Host will NACK (not acknowledge) the last data byte to be received from the client by holding the SMBus data line high after the 8th data bit has been sent.

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5.1.5 SMBUS STOP BIT

The SMBus Stop bit is defined as a transition of the SMBus Data line from a logic '0' state to a logic '1' state while the SMBus clock line is in a logic '1' state. When the device detects an SMBus Stop bit and it has been communicating with the SMBus protocol, it will reset its client interface and prepare to receive further communications.

5.1.6 SMBUS TIMEOUT

The EMC1464 supports SMBus Timeout. If the clock line is held low for longer than $t_{TIMEOUT}$, the device will reset its SMBus protocol. This function can be enabled by setting the TIMEOUT bit (see **Section 6.12 "Consecutive Alert Register"**)

5.1.7 SMBUS AND I^{2}C COMPATIBILITY

The EMC1464 is compatible with SMBus and I^{2}C. The major differences between SMBus and I^{2}C devices are highlighted here.

- EMC1464 supports I^{2}C fast mode at 400 kHz. This covers the SMBus maximum time of 100 kHz.
- Minimum frequency for SMBus communications is 10 kHz.
- The SMBus client protocol will reset if the clock is held at a logic '0' for longer than 30 ms. This time-out functionality is disabled by default in the EMC1464 and can be enabled by writing to the TIMEOUT bit. I^{2}C does not have a timeout.
- I^{2}C devices do not support the Alert Response Address functionality (which is optional for SMBus).

Attempting to communicate with the EMC1464 SMBus interface with an invalid target address or an invalid protocol elicits no response from the device and does not affect its register contents. Stretching of the SMCLK signal is supported, provided other devices on the SMBus control the timing.

For more information, refer to the SMBus 2.0 and I^{2}C specifications. For information on using the EMC1464 in an I^{2}C system, refer to AN14.0 *"Microchip Dedicated Slave Devices in I^{2}C Systems"* (DS00001853).

5.2 SMBus Protocols

The device supports Write Byte, Read Byte, Send Byte, Receive Byte and the Alert Response Address as valid protocols, as shown in this section.

All of these protocols use the convention in Table 5-2.

TABLE 5-2: SMBUS PROTOCOL FORMAT

Data Sent to Device	Data Sent to Host
# of bits sent	# of bits sent

5.2.1 WRITE BYTE PROTOCOL

The Write Byte protocol is used to write one byte of data to the registers, as shown in Table 5-3.

TABLE 5-3: SMBUS WRITE BYTE PROTOCOL

Start	Target Address	WR	ACK	Register Address	ACK	Register Data	ACK	Stop
1 → 0	YYYY_YYY	0	0	XXh	0	XXh	0	0 → 1

5.2.2 READ BYTE PROTOCOL

The Read Byte protocol is used to read one byte of data from the registers, as shown in Table 5-4.

TABLE 5-4: SMBUS READ BYTE PROTOCOL

Start	Target Address	WR	ACK	Register Address	ACK	Start	Target Address	RD	ACK	Register Data	NACK	Stop
1 → 0	YYYY_YYY	0	0	XXh	0	1 → 0	YYYY_YYY	1	0	XX	1	0 → 1

5.2.3 SEND BYTE PROTOCOL

The Send Byte protocol is used to set the internal address register pointer to the correct address location. No data is transferred during the Send Byte protocol, as shown in Table 5-5.

TABLE 5-5: SMBUS SEND BYTE PROTOCOL

Start	Target Address	WR	ACK	Register Address	ACK	Stop
1 → 0	YYYY_YYY	0	0	XXh	0	0 → 1

5.2.4 RECEIVE BYTE PROTOCOL

The Receive Byte protocol is used to read data from a register when the internal register address pointer is known to be at the right location (e.g., set via Send Byte). This is used for consecutive reads of the same register, as shown in Table 5-6.

TABLE 5-6: SMBUS RECEIVE BYTE PROTOCOL

Start	Target Address	RD	ACK	Register Data	NACK	Stop
1 → 0	YYYY_YYY	1	0	XXh	1	0 → 1

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5.3 Alert Response Address (ARA) Protocol

The $\overline{\text{ALERT}}$ output can be used as a processor interrupt or as an SMBus Alert.

When it detects that the $\overline{\text{ALERT}}$ pin is asserted, the host will send the Alert Response Address (ARA) to the general address of 0001_100xb. All devices with active interrupts will respond with their client address, as shown in Table 5-7.

TABLE 5-7: SMBUS ALERT RESPONSE ADDRESS PROTOCOL

Start	Alert Response Address	RD	ACK	Device Address	NACK	Stop
1 → 0	0001_100	1	0	YYYY_YYY	1	0 → 1

The EMC1464 will respond to the ARA in the following ways:

- Send Target Address and verify that full target address was sent (i.e., the SMBus communication from the device was not prematurely stopped due to a bus contention event).
- Set the MASK_ALL bit to clear the $\overline{\text{ALERT}}$ pin.

Note: The ARA does not clear the Status register. If the MASK_ALL bit is cleared prior to the Status Register being cleared, the $\overline{\text{ALERT}}$ pin will be reasserted.

6.0 REGISTER DESCRIPTION

The registers shown in Table 6-1 are accessible through the SMBus. An entry of '—' indicates that the bit is not used and will always read '0'.

TABLE 6-1: REGISTER SET IN HEXADECIMAL ORDER

Register Address	Register Name	R/W	Function	Default Value	Page
00h	Internal Diode Data High Byte	R	Stores the integer data for Internal Diode	00h	20
01h	External Diode 1 Data High Byte	R	Stores the integer data for External Diode	00h	
02h	Status	R	Stores status bits for Internal Diode and External Diodes	00h	21
03h	Configuration	R/W	Controls the general operation of the device (mirrored at address 09h)	00h	22
04h	Conversion Rate	R/W	Controls the conversion rate for updating temperature data (mirrored at address 0Ah)	06h (4/sec)	23
05h	Internal Diode High Limit	R/W	Stores the 8-bit high limit for Internal Diode (mirrored at address 0Bh)	55h (85°C)	24
06h	Internal Diode Low Limit	R/W	Stores the 8-bit low limit for Internal Diode (mirrored at address 0Ch)	00h (0°C)	
07h	External Diode 1 High Limit High Byte	R/W	Stores the integer portion of the high limit for External Diode 1 (mirrored at register 0Dh)	55h (85°C)	
08h	External Diode 1 Low Limit High Byte	R/W	Stores the integer portion of the low limit for External Diode 1 (mirrored at register 0Eh)	00h (0°C)	
09h	Configuration	R/W	Controls the general operation of the device (mirrored at address 03h)	00h	22
0Ah	Conversion Rate	R/W	Controls the conversion rate for updating temperature data (mirrored at address 04h)	06h (4/sec)	23
0Bh	Internal Diode High Limit	R/W	Stores the 8-bit high limit for Internal Diode (mirrored at address 05h)	55h (85°C)	24
0Ch	Internal Diode Low Limit	R/W	Stores the 8-bit low limit for Internal Diode (mirrored at address 06h)	00h (0°C)	
0Dh	External Diode 1 High Limit High Byte	R/W	Stores the integer portion of the high limit for External Diode 1 (mirrored at register 07h)	55h (85°C)	
0Eh	External Diode 1 Low Limit High Byte	R/W	Stores the integer portion of the low limit for External Diode 1 (mirrored at register 08h)	00h (0°C)	
0Fh	One Shot	W	A write to this register initiates a one-shot update	00h	25
10h	External Diode 1 Data Low Byte	R	Stores the fractional data for External Diode 1	00h	20
11h	Scratchpad	R/W	Scratchpad register for software compatibility	00h	25
12h	Scratchpad	R/W	Scratchpad register for software compatibility	00h	
13h	External Diode 1 High Limit Low Byte	R/W	Stores the fractional portion of the high limit for External Diode 1	00h	24
14h	External Diode 1 Low Limit Low Byte	R/W	Stores the fractional portion of the low limit for External Diode 1	00h	
15h	External Diode 2 High Limit High Byte	R/W	Stores the integer portion of the high limit for External Diode 2	55h (85°C)	
16h	External Diode 2 Low Limit High Byte	R/W	Stores the integer portion of the low limit for External Diode 2	00h (0°C)	
17h	External Diode 2 High Limit Low Byte	R/W	Stores the fractional portion of the high limit for External Diode 2	00h	24
18h	External Diode 2 Low Limit Low Byte	R/W	Stores the fractional portion of the low limit for External Diode 2	00h	

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TABLE 6-1: REGISTER SET IN HEXADECIMAL ORDER (CONTINUED)

Register Address	Register Name	R/W	Function	Default Value	Page
19h	External Diode 1 Therm Limit	R/W	Stores the 8-bit critical temperature limit for External Diode 1	7Dh (125°C)	26
1Ah	External Diode 2 Therm Limit	R/W	Stores the 8-bit critical temperature limit for External Diode 2	7Dh (125°C)	
1Bh	External Diode Fault	R-C	Stores status bits indicating which external diode detected a diode fault	00h	27
1Fh	Channel Mask Register	R/W	Controls the masking of individual channels	00h	28
20h	Internal Diode Therm Limit	R/W	Stores the 8-bit critical temperature limit for Internal Diode	7Dh (125°C)	26
21h	Therm Hysteresis	R/W	Stores the 8-bit hysteresis value that applies to all Therm limits	0Ah (10°C)	
22h	Consecutive Alert	R/W	Controls the number of out-of-limit conditions that must occur before an interrupt is asserted	70h	29
23h	External Diode 2 Data High Byte	R	Stores the integer data for External Diode 2	00h	20
24h	External Diode 2 Data Low Byte	R	Stores the fractional data for External Diode 2	00h	
25h	External Diode 1 Beta Configuration	R/W	Stores the Beta Compensation circuitry settings for External Diode 1	08h	31
27h	External Diode 1 Ideality Factor	R/W	Stores the ideality factor for External Diode 1	12h (1.008)	32
28h	External Diode 2 Ideality Factor	R/W	Stores the ideality factor for External Diode 2	12h (1.008)	
29h	Internal Diode Data Low Byte	R	Stores the fractional data for Internal Diode	00h	20
2Ah	External Diode 3 High Byte	R	Stores the integer data for External Diode 3	00h	20
2Bh	External Diode 3 Low Byte	R	Stores the fractional data for External Diode 3	00h	
2Ch	External Diode 3 High Limit High Byte	R/W	Stores the integer portion of the high limit for External Diode 3	55h (85°C)	24
2Dh	External Diode 3 Low Limit High Byte	R/W	Stores the integer portion of the low limit for External Diode 3	00h (0°C)	
2Eh	External Diode 3 High Limit Low Byte	R/W	Stores the fractional portion of the high limit for External Diode 3	00h	
2Fh	External Diode 3 Low Limit Low Byte	R/W	Stores the fractional portion of the low limit for External Diode 3	00h	
30h	External Diode 3 Therm Limit	R/W	Stores the 8-bit critical temperature limit for External Diode 3	7Dh (125°C)	26
31h	External Diode 3 Ideality Factor	R/W	Stores the ideality factor for External Diode 3	12h (1.008)	32
35h	High Limit Status	R-C	Status bits for High limits	00h	34
36h	Low Limit Status	R-C	Status bits for Low limits	00h	35
37h	Therm Limit Status	R	Status bits for Therm limits	00h	36
40h	Filter Control	R/W	Controls the digital filter setting for External Diode channel	00h	37
FDh	Product ID	R	Stores a fixed value that identifies the device	65h	38
FEh	Manufacturer ID	R	Stores a fixed value that represents Microchip	5Dh	38
FFh	Revision	R	Stores a fixed value that represents the revision number	06h	38

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6.1 Data Read Interlock

When any temperature channel high byte register is read, the corresponding low byte is copied into an internal 'shadow' register. The user is free to read the low byte at any time and be guaranteed that it will correspond to the previously read high byte. Even if the low byte is not read, reading from the same high byte register again will automatically refresh this stored low byte data.

6.2 Temperature Data Registers

As shown in Table 6-2, all temperatures are stored as an 11-bit value with the high byte representing the integer value and the low byte representing the fractional value left justified to occupy the MSbs.

TABLE 6-2: TEMPERATURE DATA REGISTERS

Register Address	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
00h	Internal Diode High Byte	R	128	64	32	16	8	4	2	1	00h
29h	Internal Diode Low Byte	R	0.5	0.25	0.125	—	—	—	—	—	00h
01h	External Diode 1 High Byte	R	128	64	32	16	8	4	2	1	00h
10h	External Diode 1 Low Byte	R	0.5	0.25	0.125	—	—	—	—	—	00h
23h	External Diode 2 High Byte	R	128	64	32	16	8	4	2	1	00h
24h	External Diode 2 Low Byte	R	0.5	0.25	0.125	—	—	—	—	—	00h
2Ah	External Diode 3 High Byte	R	128	64	32	16	8	4	2	1	00h
2Bh	External Diode 3 Low Byte	R	0.5	0.25	0.125	—	—	—	—	—	00h

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6.3 Status Register

The Status register reports general error conditions. To identify specific channels, refer to **Section 6.9**, **Section 6.15**, **Section 6.16**, and **Section 6.17**. The individual Status Register bits are cleared when the appropriate High Limit, Low Limit or Therm Limit register has been read or cleared.

Name	Bits	Address	Type	Default
Status	8	02h	R/W	00h

REGISTER 6-1: STATUS REGISTER, ADDRESS 02h

R-0	U-0	U-0	R-0	R-0	R-0	R-0	U-0
BUSY	—	—	HIGH	LOW	FAULT	THERM	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **BUSY:** This bit indicates that the ADC is currently converting. This bit does not cause either the $\overline{\text{ALERT}}$ or $\overline{\text{THERM}}$ pin to be asserted

bit 6-5 **Unimplemented:** Read as ‘0’

bit 4 **HIGH:** This bit is set when any of the temperature channels exceeds its programmed high limit. See the High Limit Status Register for specific channel information, section **Section 6.15**. When set, this bit will assert the $\overline{\text{ALERT}}$ pin.

bit 3 **LOW:** This bit is set when any of the temperature channels drops below its programmed low limit. See the Low Limit Status Register for specific channel information, section **Section 6.16**. When set, this bit will assert the $\overline{\text{ALERT}}$ pin.

bit 2 **FAULT:** This bit is asserted when a diode fault is detected on any of the external diode channels. See the External Diode Fault Register for specific channel information, section **Section 6.10**. When set, this bit will assert the $\overline{\text{ALERT}}$ pin.

bit 1 **THERM:** This bit is set when any of the temperature channels exceeds its programmed Therm Limit. See the Therm Limit Status Register for specific channel information, section **Section 6.17**. When set, this bit will assert the $\overline{\text{THERM}}$ pin.

bit 0 **Reserved**: Read as ‘0’

6.4 Configuration Register

The Configuration register controls the basic operation of the device. This register is fully accessible at either address.

Name	Bits	Address	Type	Default
Configuration	8	03h 09h	R/W	00h

REGISTER 6-2: CONFIGURATION REGISTER, ADDRESS 03h AND 09h

R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
MASK_ALL	RUN/STOP	ALERT/COMP	RECD1	RECD2	RANGE	DAVG_DIS	APDD
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **MASK_ALL:** Masks the $\overline{\text{ALERT}}$ pin from asserting

1 = The $\overline{\text{ALERT}}$ pin is masked. It will not be asserted for any interrupt condition unless it is configured in Comparator mode. The Status Registers will be updated normally. **(Default)**

0 = The $\overline{\text{ALERT}}$ pin is not masked. If any of the appropriate status bits are set, the $\overline{\text{ALERT}}$ pin will be asserted.

bit 6 **RUN/STOP:** Controls Active/Standby modes

1 = The device is in Standby mode and not converting

0 = The device is in Active mode and converting on all channels **(Default)**

bit 5 **ALERT/COMP:** Controls the operation of the $\overline{\text{ALERT}}$ pin

1 = The $\overline{\text{ALERT}}$ pin operates in Comparator mode as described in **Section 4.2.2**. In this mode, the MASK_ALL bit is ignored.

0 = The $\overline{\text{ALERT}}$ pin operates as described in **Section 4.2** **(Default)**

bit 4 **RECD1:** Disables the Resistance Error Correction (REC) for External Diode 1

1 = REC is disabled for External Diode 1

0 = REC is enabled for External Diode 1 **(Default)**

bit 3 **RECD2:** Disables the Resistance Error Correction (REC) for External Diode 2 and External Diode 3

1 = REC is disabled for External Diode 2 and External Diode 3

0 = REC is enabled for External Diode 2 and External Diode 3 **(Default)**

bit 2 **RANGE:** Configures the measurement range and data format of temperature channels

1 = The temperature measurement range is -64°C to +191.875°C and the data format is offset binary (see Table 4-2)

0 = The temperature measurement range is 0°C to +127.875°C and the data format is binary **(Default)**

bit 1 **DAVG_DIS:** Disables the dynamic averaging feature on all temperature channels

1 = The dynamic averaging feature is disabled. All temperature channels will be converted with a maximum averaging factor of 1x (equivalent to 11-bit conversion). For higher conversion rates, this averaging factor will be reduced as shown in Table 6-3.

0 = The dynamic averaging feature is enabled. All temperature channels will be converted with an averaging factor that is based on the conversion rate as shown in Table 6-3. **(Default)**

bit 0 **APDD**: The ALERT pin operates as described in **Section 4.2**

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6.5 Conversion Rate Register

The Conversion Rate register controls how often the temperature measurement channels are updated and compared against the limits. This register is fully accessible at either address.

Name	Bits	Address	Type	Default
Conversion Rate	8	04h 0Ah	R/W	06h (4/sec)

REGISTER 6-3: CONVERSION RATE REGISTER, ADDRESS 04h AND 0 Ah

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	CONV<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-4 **Unimplemented:** Read as ‘0’

bit 3-0 **CONV<3:0>:** Determine the conversion rate as per Table 6-3

TABLE 6-3: CONVERSION RATE

CONV<3:0>					Conversions/sec.
HEX	**3**	**2**	**1**	**0**	
0h	0	0	0	0	1/16
1h	0	0	0	1	1/6
2h	0	0	1	0	1/4
3h	0	0	1	1	1/2
4h	0	1	0	0	1
5h	0	1	0	1	2
6h	0	1	1	0	4 (default)
7h	0	1	1	1	8
8h	1	0	0	0	16
9h	1	0	0	1	32
Ah	1	0	1	0	64
Bh – Fh	All others				1

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6.6 Limit Registers

The device contains both high and low limits for all temperature channels. If the measured temperature exceeds the high limit, the corresponding status bit is set and the $\overline{\text{ALERT}}$ pin is asserted. Likewise, if the measured temperature is less than or equal to the low limit, the corresponding status bit is set and the $\overline{\text{ALERT}}$ pin is asserted.

The data format for the limits must match the selected data format for the temperature; so that if the extended temperature range is used, the limits must be programmed in the extended data format.

The limit registers with multiple addresses are fully accessible at either address.

When the device is in Standby mode, updating the limit registers will have no effect until the next conversion cycle occurs. This can be initiated via a Write to the One Shot register (see **Section 6.8 "One Shot Register"**) or by clearing the RUN/STOP bit (see **Section 6.4 "Configuration Register"**).

REGISTER 6-4: TEMPERATURE LIMIT REGISTERS

Register Address	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
05h 0Bh	Internal Diode High Limit	R/W	128	64	32	16	8	4	2	1	55h (85°C)
06h 0Ch	Internal Diode Low Limit	R/W	128	64	32	16	8	4	2	1	00h (0°C)
07h 0Dh	External Diode 1 High Limit High Byte	R/W	128	64	32	16	8	4	2	1	55h (85°C)
13h	External Diode 1 High Limit Low Byte	R/W	0.5	0.25	0.125	—	—	—	—	—	00h
08h 0Eh	External Diode 1 Low Limit High Byte	R/W	128	64	32	16	8	4	2	1	00h (0°C)
14h	External Diode 1 Low Limit Low Byte	R/W	0.5	0.25	0.125	—	—	—	—	—	00h
15h	External Diode 2 High Limit High Byte	R/W	128	64	32	16	8	4	2	1	55h (85°C)
16h	External Diode 2 Low Limit High Byte	R/W	128	64	32	16	8	4	2	1	00h (0°C)
17h	External Diode 2 High Limit Low Byte	R/W	0.5	0.25	0.125	—	—	—	—	—	00h
18h	External Diode 2 Low Limit Low Byte	R/W	0.5	0.25	0.125	—	—	—	—	—	00h
2Ch	External Diode 3 High Limit High Byte	R/W	128	64	32	16	8	4	2	1	55h (85°C)
2Dh	External Diode 3 Low Limit High Byte	R/W	128	64	32	16	8	4	2	1	00h (0°C)
2Eh	External Diode 3 High Limit Low Byte	R/W	0.5	0.25	0.125	—	—	—	—	—	00h
2Fh	External Diode 3 Low Limit Low Byte	R/W	0.5	0.25	0.125	—	—	—	—	—	00h

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6.7 Scratchpad Registers

The Scratchpad registers are Read/Write registers that are used for place holders to be software compatible with legacy programs. Reading from the registers will return what is written to them.

SCRATCHPAD REGISTERS

Register Address	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
11h	Scratchpad	R/W	7	6	5	4	3	2	1	0	00h
12h	Scratchpad	R/W	7	6	5	4	3	2	1	0	00h

6.8 One Shot Register

The One Shot register is used to initiate a one-shot command. Writing to the one shot register when the device is in Standby mode and the BUSY bit (in Status Register) is '0', will immediately cause the ADC to update all temperature measurements. Writing to the One Shot Register while the device is in Active mode will have no affect.

REGISTER 6-5: ONE SHOT REGISTER

Register Address	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
0Fh	One Shot	W	Writing to this register initiates a single conversion cycle. Data is not stored and always reads 00h.								00h

6.9 Therm Limit Registers

The Therm Limit registers are used to determine whether a critical thermal event has occurred. If the measured temperature exceeds the Therm Limit, the $\overline{\text{THERM}}$ pin is asserted. The limit setting must match the chosen data format of the temperature reading registers.

Unlike the $\overline{\text{ALERT}}$ pin, the $\overline{\text{THERM}}$ pin cannot be masked. Additionally, the $\overline{\text{THERM}}$ pin will be released once the temperature drops below the corresponding threshold minus the Therm Hysteresis.

REGISTER 6-6: THERM LIMIT REGISTERS

Register Address	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
19h	External Diode 1 Therm Limit	R/W	128	64	32	16	8	4	2	1	7Dh (125°C)
1Ah	External Diode 2 Therm Limit	R/W	128	64	32	16	8	4	2	1	7Dh (125°C)
20h	Internal Diode Therm Limit	R/W	128	64	32	16	8	4	2	1	7Dh (125°C)
21h	Therm Hysteresis	R/W	128	64	32	16	8	4	2	1	0Ah (10°C)
30h	External Diode 3 Therm Limit	R/W	128	64	32	16	8	4	2	1	7Dh (125°C)

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6.10 External Diode Fault Register

The External Diode Fault register indicates which of the external diodes caused the FAULT bit in the Status register to be set. This register is cleared when read.

Name	Bits	Address	Type	Default
External Diode Fault	8	1Bh	R-C	00h

REGISTER 6-7: EXTERNAL DIODE FAULT REGISTER, ADDRESS 1Bh

U-0	U-0	U-0	U-0	R-C	R-C	R-C	U-0
—	—	—	—	E3FLT	E2FLT	E1FLT	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-4	**Unimplemented**: Read as ‘0’
bit 3	**E3FLT:** This bit is set if External Diode 3 channel reported a diode fault
bit 2	**E2FLT:** This bit is set if External Diode 2 channel reported a diode fault
bit 1	**E1FLT:** This bit is set if External Diode 1 channel reported a diode fault
bit 0	**Unimplemented**: Read as ‘0’

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6.11 Channel Mask Register

The Channel Mask register controls individual channel masking. When a channel is masked, the $\overline{\text{ALERT}}$ pin will not be asserted when the masked channel reads a diode fault or out-of-limit error. The channel mask does not mask the $\overline{\text{THERM}}$ pin.

Name	Bits	Address	Type	Default
Channel Mask	8	1Fh	R/W	00h

REGISTER 6-8: CHANNEL MASK REGISTER, ADDRESS 1Fh

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	E3MASK	E2MASK	E1MASK	INTMASK
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-4 **Unimplemented**: Read as ‘0’

bit 3 **E3MASK:** Masks the $\overline{\text{ALERT}}$ pin from asserting when External Diode 3 channel is out of limit or reports a diode fault

1 = External Diode 3 channel will not cause the $\overline{\text{ALERT}}$ pin to be asserted if it is out of limit or reports a diode fault

0 = External Diode 3 channel will cause the $\overline{\text{ALERT}}$ pin to be asserted if it is out of limit or reports a diode fault **(Default)**

bit 2 **E2MASK:** Masks the $\overline{\text{ALERT}}$ pin from asserting when External Diode 2 channel is out of limit or reports a diode fault

1 = External Diode 2 channel will not cause the $\overline{\text{ALERT}}$ pin to be asserted if it is out of limit or reports a diode fault

0 = External Diode channel will cause the $\overline{\text{ALERT}}$ pin to be asserted if it is out of limit or reports a diode fault **(Default)**

bit 1 **E1MASK:** Masks the $\overline{\text{ALERT}}$ pin from asserting when External Diode 1 channel is out of limit or reports a diode fault

1 = External Diode 2 channel will not cause the $\overline{\text{ALERT}}$ pin to be asserted if it is out of limit or reports a diode fault

0 = External Diode channel will cause the $\overline{\text{ALERT}}$ pin to be asserted if it is out of limit or reports a diode fault **(Default)**

bit 0 **INTMASK:** Masks the $\overline{\text{ALERT}}$ pin from asserting when Internal Diode temperature is out of limit

1 = Internal Diode channel will not cause the $\overline{\text{ALERT}}$ pin to be asserted if it is out of limit

0 = Internal Diode channel will cause the $\overline{\text{ALERT}}$ pin to be asserted if it is out of limit **(Default)**

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6.12 Consecutive Alert Register

The Consecutive ALERT register determines how many times an out-of-limit error or diode fault must be detected in consecutive measurements before the $\overline{\text{ALERT}}$ or $\overline{\text{THERM}}$ pin is asserted. Additionally, the Consecutive Alert register controls the SMBus Timeout functionality.

Name	Bits	Address	Type	Default
Consecutive Alert	8	22h	R/W	70h

REGISTER 6-9: CONSECUTIVE ALERT REGISTER, ADDRESS 22h

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
TIMEOUT	CTHRM<2:0>			CALRT<2:0>			—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **TIMEOUT:** Determines whether the SMBus Timeout function is enabled

1 = The SMBus Timeout feature is enabled. If the SMCLK line is held low for more than $t_{TIMEOUT}$, the device will reset the SMBus protocol.

0 = The SMBus Timeout feature is disabled. The SMCLK line can be held low indefinitely without the device resetting its SMBus protocol. **(Default)**

bit 6-4 **CTHRM<2:0>:** Determines the number of consecutive measurements that must exceed the corresponding Therm Limit before the $\overline{\text{THERM}}$ pin is asserted. All temperature channels use this value to set the respective counters. The consecutive Therm counter is incremented whenever any measurement exceeds the corresponding Therm Limit.

If the temperature drops below the Therm Limit, the counter is reset. If a number of consecutive measurements above the Therm Limit occurs, the $\overline{\text{THERM}}$ pin is asserted low.

When the $\overline{\text{THERM}}$ pin has been asserted, the consecutive therm counter will not reset until the corresponding temperature drops below the Therm Limit minus the Therm Hysteresis value.

The bits are decoded as shown in Table 6-4. The default setting is 4 consecutive out-of-limit conversions

bit 3-1 **CALRT<2:0>:** Determine the number of consecutive measurements that must have an out-of-limit condition or diode fault before the $\overline{\text{ALERT}}$ pin is asserted. Both temperature channels use this value to set the respective counters. The bits are decoded as shown in Table 6-4. The default setting is 1 consecutive out-of-limit conversion.

bit 0 **Unimplemented**: Read as ‘0’

An out-of-limit condition (i.e., HIGH, LOW, or FAULT) occurring on the same temperature channel in consecutive measurements will increment the consecutive alert counter. The counters will also be reset if an out-of-limit condition or diode fault condition does not occur in a consecutive reading.

If the $\overline{\text{ALERT}}$ pin is configured as an interrupt, when the consecutive alert counter reaches its programmed value, the following will occur:

- STATUS bit(s) for that channel and the last error condition(s) (i.e., E1HIGH, or E2LOW and/or E2FAULT) will be set to '1'
- $\overline{\text{ALERT}}$ pin will be asserted
- consecutive alert counter will be cleared
- measurements will continue

If the $\overline{\text{ALERT}}$ pin is configured as a comparator, the consecutive alert counter will ignore diode fault and low limit errors, and only increment if the measured temperature exceeds the High Limit. Additionally, when the consecutive alert counter reaches the programmed limit, the $\overline{\text{ALERT}}$ pin will be asserted, but the counter will not be reset. It will remain set until the temperature drops below the High Limit minus the Therm Hysteresis value.

For example, if the CALRT<2:0> bits are set for 4 consecutive alerts on an EMC1464 device, the high limits are set at 70°C, and none of the channels are masked, the $\overline{\text{ALERT}}$ pin will be asserted after the following four measurements:

- Internal Diode reads 71°C, and both external diode reads 69°C
  Consecutive alert counter for INT is incremented to 1.
- Both the Internal Diode and the External Diode 1 read 71°C, and External Diode 2 reads 68°C
  Consecutive alert counter for INT is incremented to 2 and for EXT1 is set to 1.
- The External Diode 1 reads 71°C, and both the Internal Diode and External Diode 2 read 69°C
  Consecutive alert counters for INT and EXT2 are cleared and EXT1 is incremented to 2.
- The Internal Diode reads 71°C, and both external diodes read 71°C
  Consecutive alert counter for INT is set to 1, EXT2 is set to 1, and EXT1 is incremented to 3.
- The Internal Diode reads 71°C and both external diodes read 71°C
  Consecutive alert counter for INT is incremented to 2, EXT2 is set to 2, and EXT1 is incremented to 4. The appropriate status bits are set for EXT1, and the $\overline{\text{ALERT}}$ pin is asserted. EXT1 counter is reset to 0 and all other counters hold the last value until the next temperature measurement.

TABLE 6-4: CONSECUTIVE ALERT/THERM SETTINGS

2	1	0	Number of Consecutive Out-of-Limit Measurements
0	0	0	1 (default for CALRT<2:0>)
0	0	1	2
0	1	1	3
1	1	1	4 (default for CTHRM<2:0>)

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6.13 Beta Configuration Register

This register is used to set the Beta Compensation factor that is used for External Diode 1. Beta Compensation cannot be enabled for External Diode 2 and 3.

Name	Bits	Address	Type	Default
Beta Configuration	8	25h	R/W	08h

BETA CONFIGURATION REGISTER, ADDRESS 25h

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	ENABLE	BETA<2:0>		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-4 **Unimplemented**: Read as ‘0’

bit 3 **ENABLE:** Enables the Beta Compensation factor auto-detection function. Beta Compensation cannot be enabled for External Diode 2 or 3.

bit 2-0 **BETA<2:0>:** These bits always reflect the current beta configuration settings. If auto-detection circuitry is enabled, these bits will be updated automatically and writing to these bits will have no effect. If the auto-detection circuitry is disabled, these bits will determine the beta configuration setting.

Care should be taken when setting the BETA<2:0> bits when the auto-detection circuitry is disabled. If the Beta Compensation factor is set at a beta value that is higher than the transistor beta, the circuit may introduce measurement errors. When measuring a discrete thermal diode (such as the 2N3904) or a CPU diode that functions like a discrete thermal diode (such as AMD processor diode), the BETA<2:0> bits should be set to ‘111b’.

TABLE 6-5: CPU BETA VALUES

HEX	Enable	BETA<2:0>			Minimum Beta
		2	1	0	
0h	0	0	0	0	0.11
1h	0	0	0	1	0.18
2h	0	0	1	0	0.25
3h	0	0	1	1	0.33
4h	0	1	0	0	0.43
5h	0	1	0	1	1.00
6h	0	1	1	0	2.33
7h	0	1	1	1	Disabled
8h – Fh	1	X	X	X	Auto-Detection

6.14 External Diode Ideality Factor Registers

These registers store the ideality factors that are applied to external diodes. Table 6-6 defines each setting and the corresponding ideality factor. Beta Compensation and Resistance Error Correction automatically correct for most diode ideality errors; therefore, it is not recommended that these settings be updated without consulting Microchip.

Name	Bits	Address	Type	Default
External Diode Ideality Factor	8	27h	R/W	12h

REGISTER 6-10: EXTERNAL DIODE IDEALITY FACTOR REGISTERS

Register Address	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
27h	External Diode 1 Ideality Factor	R/W	—	—	IDEALITY<5:0>						12h
28h	External Diode 2 Ideality Factor	R/W	—	—	IDEALITY2<5:0>						12h
31h	External Diode 3 Ideality Factor	R/W	—	—	IDEALITY3<5:0>						12h

TABLE 6-6: IDEALITY FACTOR LOOK-UP TABLE (DIODE MODEL)

Setting	Factor	Setting	Factor	Setting	Factor
08h	0.9949	18h	1.0159	28h	1.0371
09h	0.9962	19h	1.0172	29h	1.0384
0Ah	0.9975	1Ah	1.0185	2Ah	1.0397
0Bh	0.9988	1Bh	1.0200	2Bh	1.0410
0Ch	1.0001	1Ch	1.0212	2Ch	1.0423
0Dh	1.0014	1Dh	1.0226	2Dh	1.0436
0Eh	1.0027	1Eh	1.0239	2Eh	1.0449
0Fh	1.0040	1Fh	1.0253	2Fh	1.0462
10h	1.0053	20h	1.0267	30h	1.0475
11h	1.0066	21h	1.0280	31h	1.0488
12h	1.0080	22h	1.0293	32h	1.0501
13h	1.0093	23h	1.0306	33h	1.0514
14h	1.0106	24h	1.0319	34h	1.0527
15h	1.0119	25h	1.0332	35h	1.0540
16h	1.0133	26h	1.0345	36h	1.0553
17h	1.0146	27h	1.0358	37h	1.0566

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For CPU substrate transistors that require the BJT transistor model, the ideality factor behaves somewhat differently than for discrete diode-connected transistors. Refer to Table 6-7 when using a CPU substrate transistor.

TABLE 6-7: SUBSTRATE DIODE IDEALITY FACTOR LOOK-UP TABLE (BJT MODEL)

Setting	Factor	Setting	Factor	Setting	Factor
08h	0.9869	18h	1.0079	28h	1.0291
09h	0.9882	19h	1.0092	29h	1.0304
0Ah	0.9895	1Ah	1.0105	2Ah	1.0317
0Bh	0.9908	1Bh	1.0120	2Bh	1.0330
0Ch	0.9921	1Ch	1.0132	2Ch	1.0343
0Dh	0.9934	1Dh	1.0146	2Dh	1.0356
0Eh	0.9947	1Eh	1.0159	2Eh	1.0369
0Fh	0.9960	1Fh	1.0173	2Fh	1.0382
10h	0.9973	20h	1.0187	30h	1.0395
11h	0.9986	21h	1.0200	31h	1.0408
12h	1.0000	22h	1.0213	32h	1.0421
13h	1.0013	23h	1.0226	33h	1.0434
14h	1.0026	24h	1.0239	34h	1.0447
15h	1.0039	25h	1.0252	35h	1.0460
16h	1.0053	26h	1.0265	36h	1.0473
17h	1.0066	27h	1.0278	37h	1.0486

Note: When measuring a 65 nm Intel CPU, the Ideality Setting should be the default 12h. When measuring a 45 nm Intel CPU, the Ideality Setting should be 15h.

6.15 High Limit Status Register

The Limit Status register will clear all bits. Reading from the register will also clear the HIGH status bit in the Status register.

Name	Bits	Address	Type	Default
High Limit Status	8	35h	R-C	00h

High Limit Status Register contains the status bits that are set when a temperature channel high limit is exceeded. If any of these bits are set, the HIGH status bit in the Status Register is set. Reading from the High

The $\overline{\text{ALERT}}$ pin will be set if the programmed number of consecutive alert counts have been met and any of these status bits are set.

The status bits will remain set until read, unless the $\overline{\text{ALERT}}$ pin is configured as a comparator output (see **Section 4.2.2**).

REGISTER 6-11: HIGH LIMIT STATUS REGISTER, ADDRESS 35h

U-0	U-0	U-0	U-0	R-C	R-C	R-C	R-C
—	—	—	—	E3HIGH	E2HIGH	E1HIGH	IHIGH
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-4	**Unimplemented**: Read as ‘0’
bit 3	**E3HIGH:** This bit is set when the External Diode 3 channel exceeds its programmed high limit
bit 2	**E2HIGH:** This bit is set when the External Diode 2 channel exceeds its programmed high limit
bit 1	**E1HIGH:** This bit is set when the External Diode 1 channel exceeds its programmed high limit
bit 0	**IHIGH:** This bit is set when the Internal Diode channel exceeds its programmed high limit

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6.16 Low Limit Status Register

The Low Limit Status register contains the status bits that are set when a temperature channel drops below its corresponding low limit. If any of these bits are set, then the LOW status bit in the Status register is set.

Name	Bits	Address	Type	Default
Low Limit Status	8	36h	R-C	00h

Reading from the Low Limit Status Register will clear all bits. Reading from the register will also clear the LOW status bit in the Status Register.

REGISTER 6-12: LOW LIMIT STATUS REGISTER, ADDRESS 36h

U-0	U-0	U-0	U-0	R-C	R-C	R-C	R-C
—	—	—	—	E3LOW	E2LOW	E1LOW	ILOW
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-4	**Unimplemented**: Read as ‘0’
bit 3	**E3LOW:** This bit is set when the External Diode 3 channel drops below its programmed low limit
bit 2	**E2LOW:** This bit is set when the External Diode 2 channel drops below its programmed low limit
bit 1	**E1LOW:** This bit is set when the External Diode 1 channel drops below its programmed low limit
bit 0	**ILOW:** This bit is set when the Internal Diode channel drops below its programmed low limit

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6.17 Therm Limit Status Register

The Therm Limit Status register contains the status bits that are set when a temperature channel Therm Limit is exceeded. If any of these bits are set, the THERM status bit in the Status register is set.

Name	Bits	Address	Type	Default
Therm Limit Status	8	37h	R-C	00h

Reading from the Therm Limit Status register will not clear the status bits. Once the temperature drops below the Therm Limit minus the Therm Hysteresis, the corresponding status bits will be automatically cleared. The THERM bit in the Status register will be cleared when all individual channel THERM bits are cleared.

REGISTER 6-13: THERM LIMIT STATUS REGISTER, ADDRESS 37h

U-0	U-0	U-0	U-0	R-C	R-C	R-C	R-C
—	—	—	—	E3THERM	E2THERM	E1THERM	ITHERM
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-4 **Unimplemented**: Read as ‘0’

bit 3 **E3THERM:** This bit is set when the External Diode 3 channel exceeds its programmed Therm Limit. When set, this bit will assert the $\overline{\text{THERM}}$ pin.

bit 2 **E2THERM:** his bit is set when the External Diode 2 channel exceeds its programmed Therm Limit. When set, this bit will assert the $\overline{\text{THERM}}$ pin.

bit 1 **E1THERM:** his bit is set when the External Diode 1 channel exceeds its programmed Therm Limit. When set, this bit will assert the $\overline{\text{THERM}}$ pin.

bit 0 **ITHERM:** This bit is set when the Internal Diode channel exceeds its programmed Therm Limit. When set, this bit will assert the $\overline{\text{THERM}}$ pin.

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6.18 Filter Control Register

The Filter Configuration register controls the digital filter on the External Diode channel.

Name	Bits	Address	Type	Default
Filter Control	8	40h	R/W	00h

REGISTER 6-14: FILTER CONTROL REGISTER, ADDRESS 40h

U-0	U-0	U-0	U-0	U-0	U-0	R/W	R/W
—	—	—	—	—	—	FILTER<1:0>	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-2 **Unimplemented**: Read as ‘0’

bit 1-0 **FILTER<1:0>:** These bits control the level of digital filtering that is applied to the External Diode temperature measurement as shown in Table 6-8. See Figure 4-3 and Figure 4-4 for examples of the filter behavior.

TABLE 6-8: FILTER DECODE

FILTER<1:0>		Averaging
1	0	
0	0	Disabled (default)
0	1	Level 1
1	0	Level 1
1	1	Level 2

6.19 Product ID Register

The Product ID Register holds a unique value that identifies the device.

REGISTER 6-15: PRODUCT ID REGISTER

Register Address	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
FDh	Product ID	R	0	1	1	0	0	1	0	1	65h

6.20 Manufacturer ID Register

The Manufacturer ID register contains an 8-bit Word that identifies Microchip Technology Incorporated as the manufacturer of the EMC1464.

REGISTER 6-16: MANUFACTURER ID REGISTER

Register Address	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
FEh	Microchip ID	R	0	1	1	1	1	0	1		5Dh

6.21 Revision Register

The Revision register contains an 8-bit Word that identifies the die revision.

REGISTER 6-17: REVISION REGISTER

Register Address	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
FFh	Revision	R	0	0	0	0	0	1	1	0	06h

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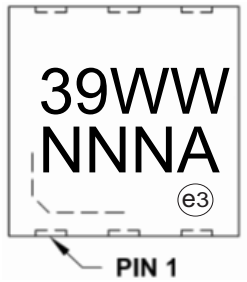
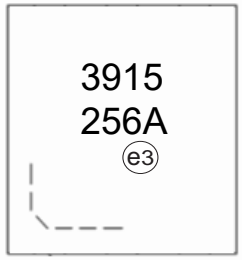
7.0 PACKAGING INFORMATION

7.1 Package Marking Information

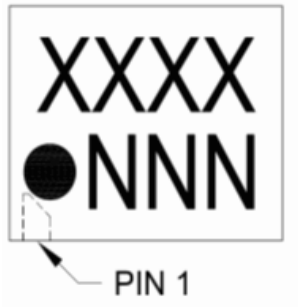
10-Lead VDFN (3x3 mm)



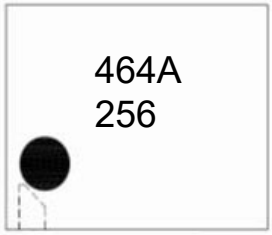
Example



10-Lead VDFN (2.5x2 mm)



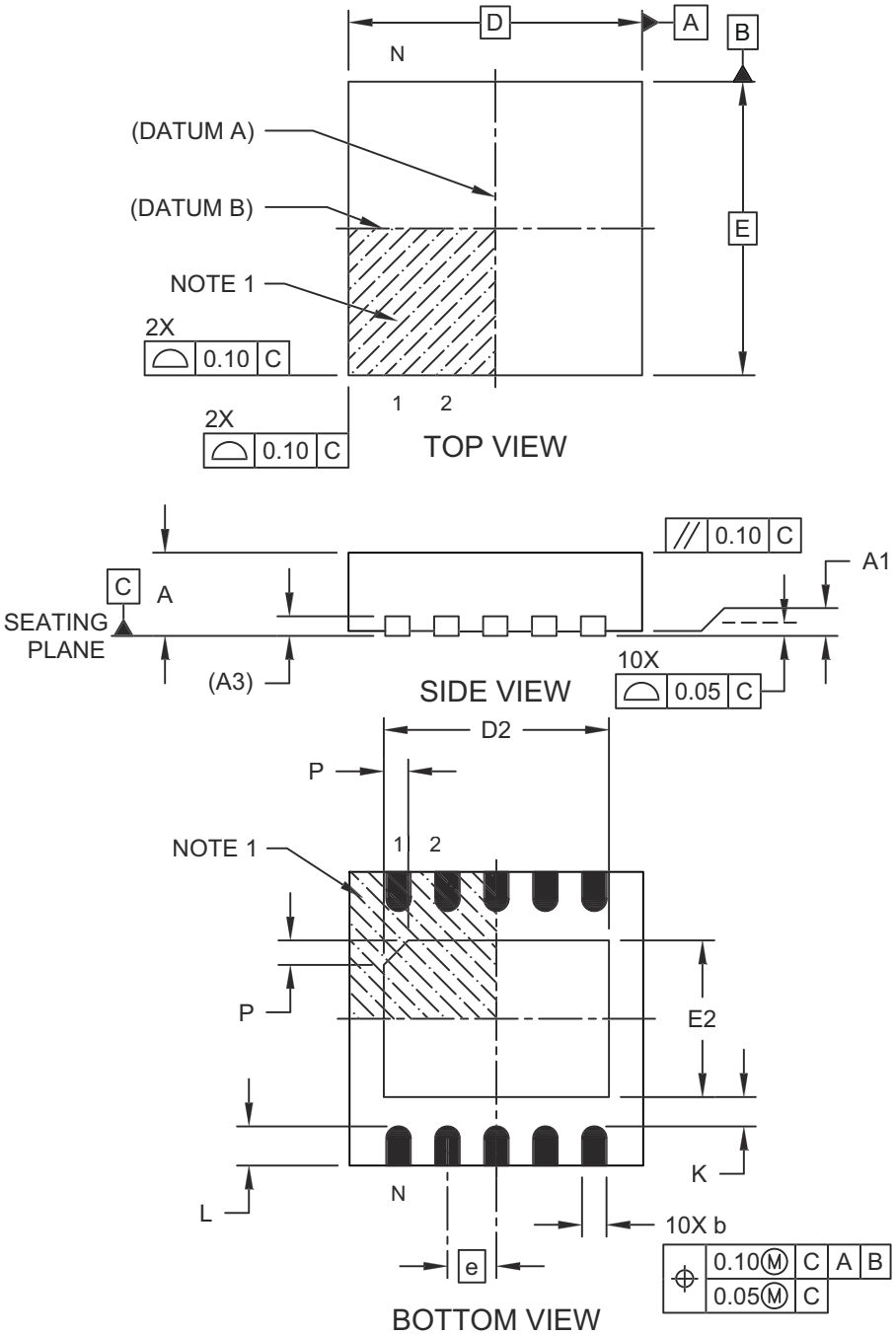
Example



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	e3	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.	

10-Lead Very Thin Plastic Dual Flat, No Lead Package (9Q) - 3x3 mm Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-00206 Rev D Sheet 1 of 2

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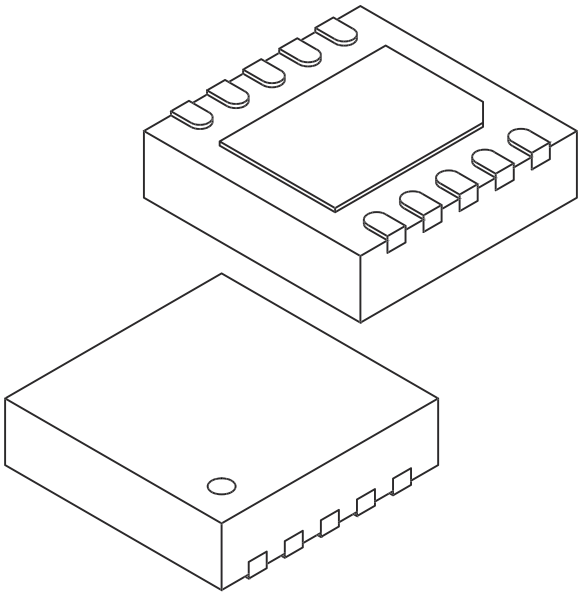
10-Lead Very Thin Plastic Dual Flat, No Lead Package (9Q) - 3x3 mm Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N	10		
Pitch	e	0.50 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	(A3)	0.20 REF		
Overall Length	D	3.00 BSC		
Exposed Pad Length	D2	2.20	2.30	2.40
Overall Width	E	3.00 BSC		
Exposed Pad Width	E2	1.50	1.60	1.70
Exposed Pad Chamfer	P	-	0.25	-
Terminal Width	b	0.18	0.25	0.30
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K	0.25	0.30	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

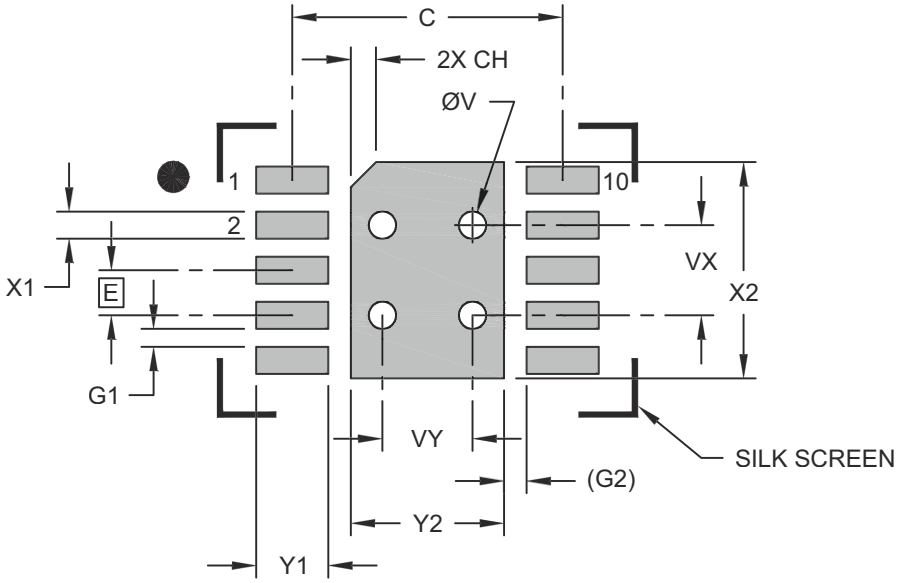
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-00206 Rev D Sheet 2 of 2

10-Lead Very Thin Plastic Dual Flat, No Lead Package (9Q) - 3x3 mm Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	Y2			1.70
Optional Center Pad Length	X2			2.40
Contact Pad Spacing	C		3.00	
Center Pad Chamfer	CH		0.28	
Contact Pad Width (X10)	X1			0.30
Contact Pad Length (X10)	Y1			0.80
Contact Pad to Contact Pad (X8)	G1	0.20		
Contact Pad to Center Pad (X10)	G2		0.25 REF	
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	VX		1.00	
Thermal Via Pitch	VY		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerances, for reference only.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-02206 Rev D

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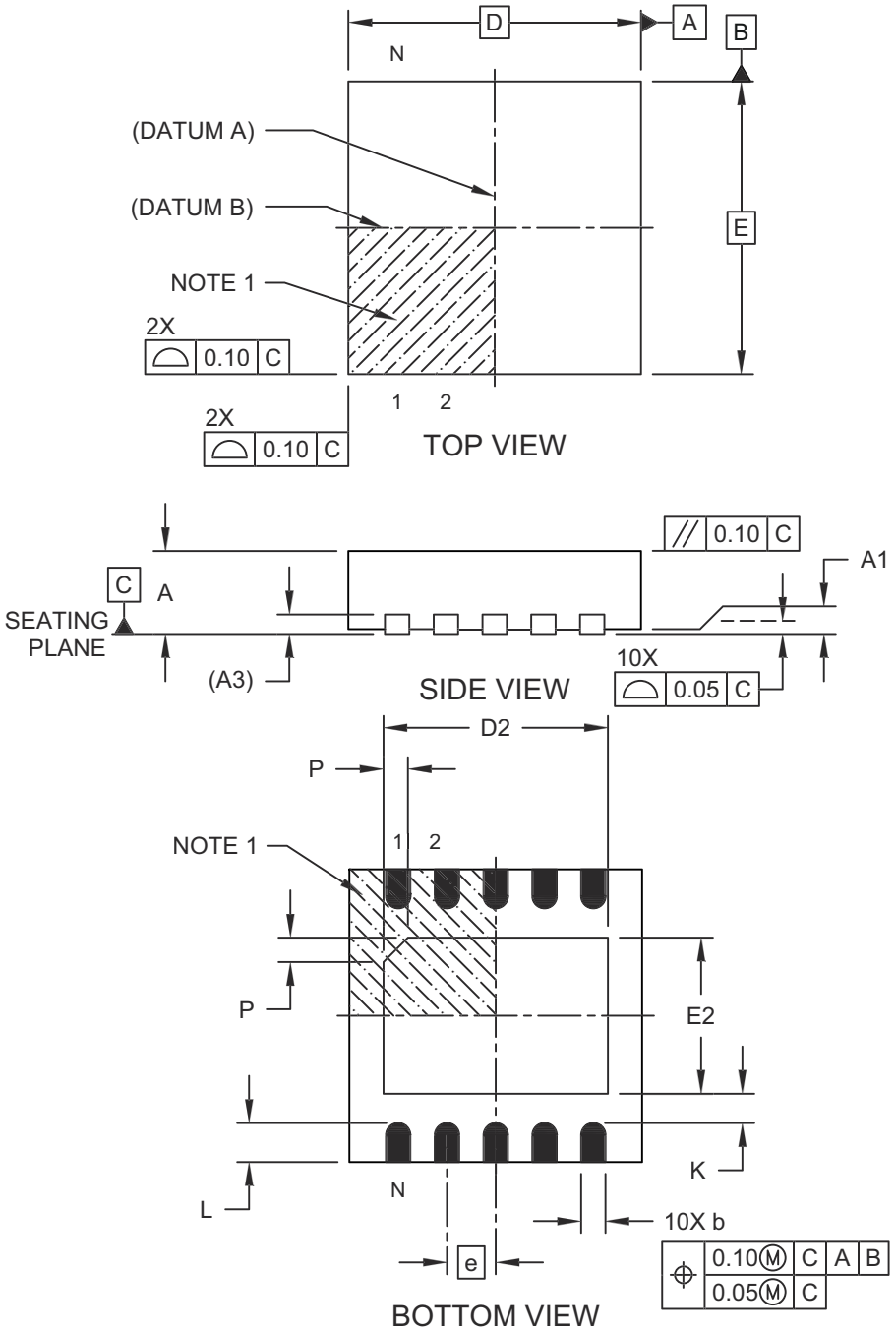
10-Lead Very Thin Plastic Dual Flat, No Lead Package (9QX) - 3x3 mm Body [VDFN]

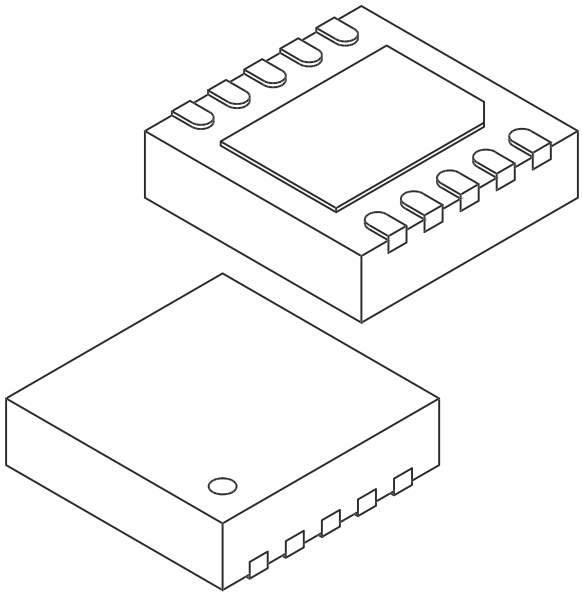
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-00206 Rev D Sheet 1 of 2

10-Lead Very Thin Plastic Dual Flat, No Lead Package (9QX) - 3x3 mm Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N	10		
Pitch	e	0.50 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	(A3)	0.20 REF		
Overall Length	D	3.00 BSC		
Exposed Pad Length	D2	2.20	2.30	2.40
Overall Width	E	3.00 BSC		
Exposed Pad Width	E2	1.50	1.60	1.70
Exposed Pad Chamfer	P	-	0.25	-
Terminal Width	b	0.18	0.25	0.30
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K	0.25	0.30	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-00206 Rev D Sheet 2 of 2

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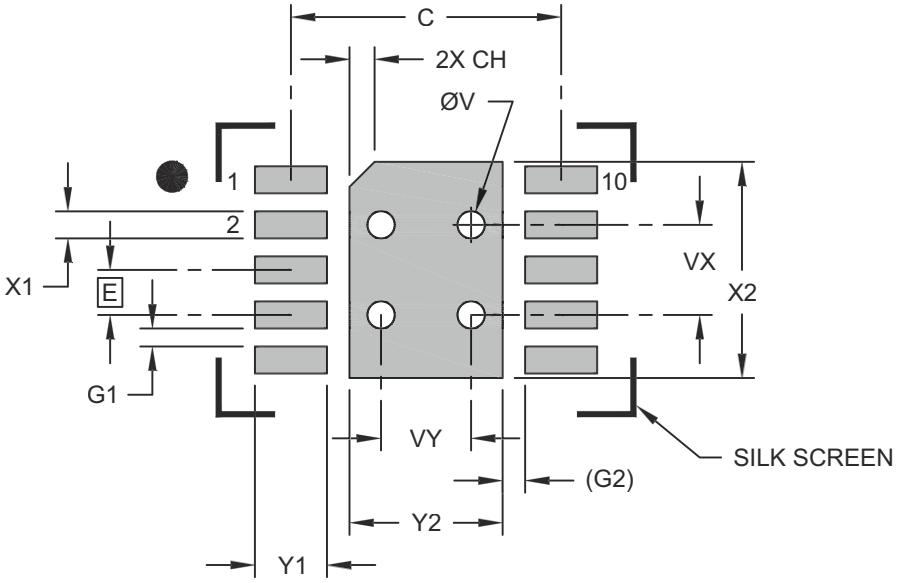
10-Lead Very Thin Plastic Dual Flat, No Lead Package (9QX) - 3x3 mm Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	Y2			1.70
Optional Center Pad Length	X2			2.40
Contact Pad Spacing	C		3.00	
Center Pad Chamfer	CH		0.28	
Contact Pad Width (X10)	X1			0.30
Contact Pad Length (X10)	Y1			0.80
Contact Pad to Contact Pad (X8)	G1	0.20		
Contact Pad to Center Pad (X10)	G2		0.25 REF	
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	VX		1.00	
Thermal Via Pitch	VY		1.00	

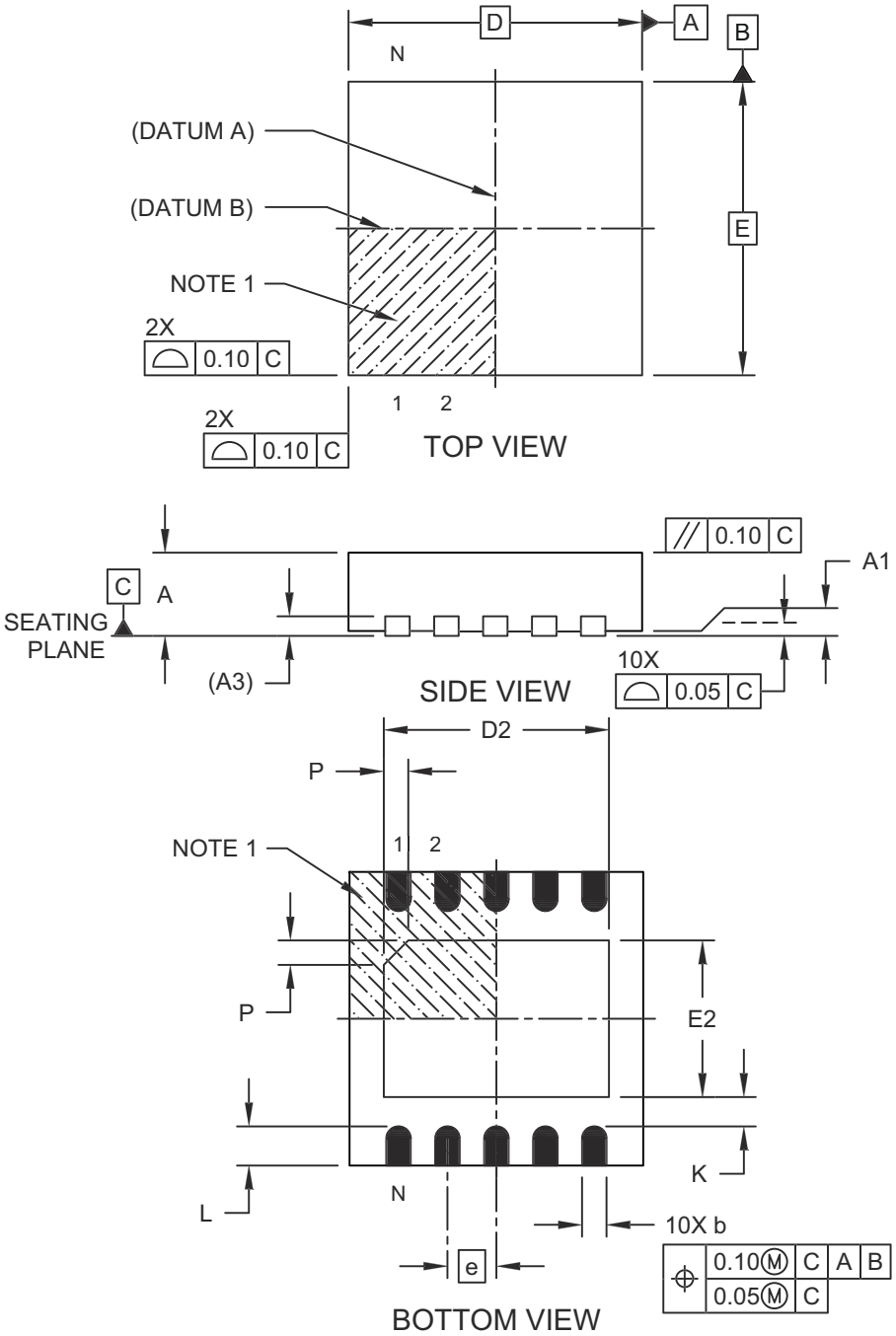
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerances, for reference only.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-02206 Rev D

10-Lead Very Thin Plastic Dual Flat, No Lead Package (QSX) - 3x3 mm Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-00206 Rev D Sheet 1 of 2

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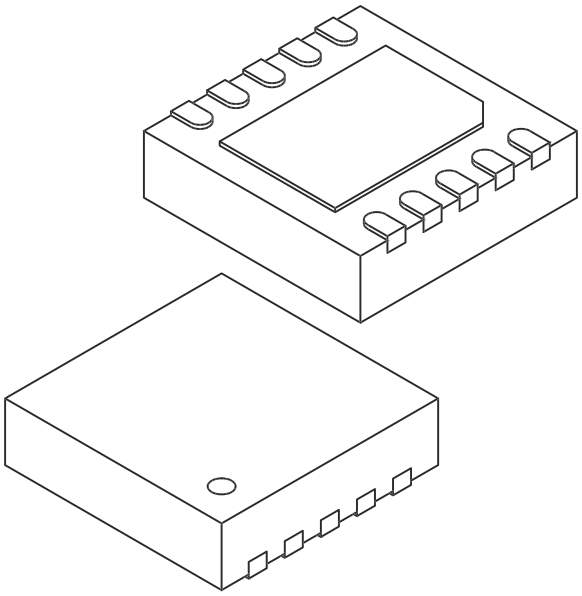
10-Lead Very Thin Plastic Dual Flat, No Lead Package (QSX) - 3x3 mm Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N	10		
Pitch	e	0.50 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	(A3)	0.20 REF		
Overall Length	D	3.00 BSC		
Exposed Pad Length	D2	2.20	2.30	2.40
Overall Width	E	3.00 BSC		
Exposed Pad Width	E2	1.50	1.60	1.70
Exposed Pad Chamfer	P	-	0.25	-
Terminal Width	b	0.18	0.25	0.30
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K	0.25	0.30	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

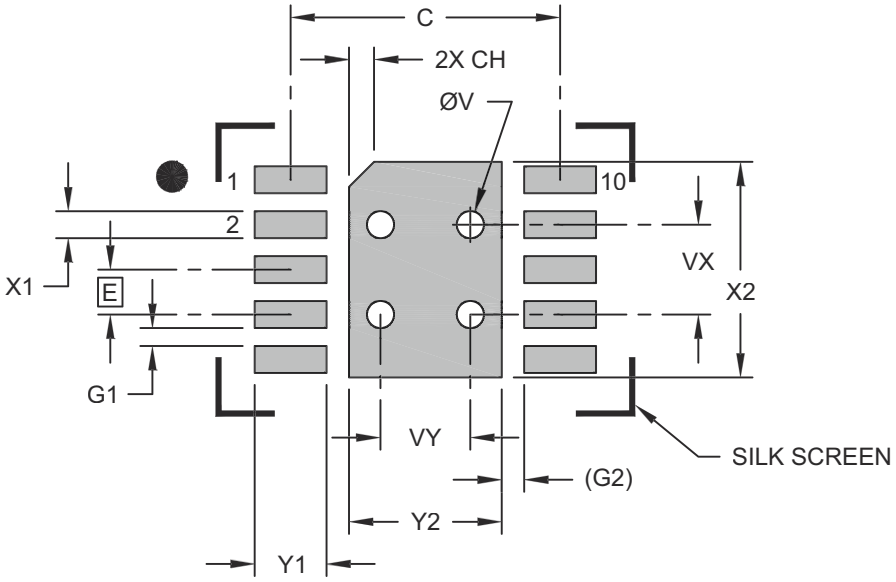
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-00206 Rev D Sheet 2 of 2

10-Lead Very Thin Plastic Dual Flat, No Lead Package (QSX) - 3x3 mm Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	Y2			1.70
Optional Center Pad Length	X2			2.40
Contact Pad Spacing	C		3.00	
Center Pad Chamfer	CH		0.28	
Contact Pad Width (X10)	X1			0.30
Contact Pad Length (X10)	Y1			0.80
Contact Pad to Contact Pad (X8)	G1	0.20		
Contact Pad to Center Pad (X10)	G2		0.25 REF	
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	VX		1.00	
Thermal Via Pitch	VY		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerances, for reference only.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-02206 Rev D

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APPENDIX A: REVISION HISTORY

Revision B (October 2025)

- First public release of this document.

Revision A (November 2012)

- Internal release only.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO. – **X** – **XX** **X** [1]

Device | **I²C Address Designator** | **Package Code** | **Tape and Reel**

Device:	EMC1464:		Multiple Channel 1°C Temperature Sensor with Beta Compensation
I²C Address Designator	A	=	Adjustable I²C Address
Package Code:	AIA	=	Former SMSC Package Designator for the Very Thin Plastic Dual Flat, 10-Lead, 3x3 mm Body VDFN No Lead Package
Tape and Reel	TR Blank	= Tape and Reel [1] = Tube	

PART NO. **X** [1] – **X** **X** / **XX**

Device | **Tape and Reel** | **I²C Address Designator** | **Temperature Range** | **Package Code**

Device:	EMC1464:		Multiple Channel 1°C Temperature Sensor with Beta Compensation
Tape and Reel	T Blank	= =	Tape and Reel [1] Tube
I²C Address Designator	A	=	Adjustable I²C Address
Temperature Range	E	=	Extended Temperature -40°C to +125°C
Package Code:	9R	=	Very Thin Plastic Dual Flat, 10-Lead 2.5x2 mm Body VDFN No Lead Package

Examples:

a) EMC1464-A-AIA-TR: Multiple Channel 1°C Temperature Sensor, Adjustable I²C Address, 3x3 mm Body, 10-Lead VDFN package, Tape and Reel

b) EMC1464T-AE/9R: Multiple Channel 1°C Temperature Sensor, Tape and Reel, Adjustable I²C Address, Extended Temperature, 2.5x2 mm Body, 10-Lead VDFN package

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

Order Numbers

Ordering Number	Package	Features	Reel Quantity	SMBus Address
EMC1464-A-AIA-TR	10-pin VDFN 3x3 mm Lead-Free RoHS compliant	Up to four temperature sensors $\overline{\text{ALERT}}$ and $\overline{\text{THERM}}$ pins 125°C default Therm limit Programmable SMBus address	5,000 pcs	Selectable via $\overline{\text{ALERT}}$ pull-up
EMC1464T-AE/9R	10-pin VDFN 2.5x2 mm Lead-Free RoHS compliant	Up to four temperature sensors $\overline{\text{ALERT}}$ and $\overline{\text{THERM}}$ pins 125°C default Therm limit Programmable SMBus address	3,000 pcs	Selectable via $\overline{\text{ALERT}}$ pull-up

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