

General Description

The MIC26400 is a constant-frequency, synchronous buck regulator that features a unique adaptive ON-time control architecture. The MIC26400 operates over an input supply range of 4.5V to 26V and provides a regulated output at up to 5A of output current. The output voltage is adjustable down to 0.8V with a typical accuracy of $\pm 1\%$, and the device operates at a switching frequency of 300kHz.

Microchip's Hyper Speed Control® architecture allows for ultra-fast transient response while reducing the output capacitance and also makes (High V_{IN})/(Low V_{OUT}) operation possible. This adaptive t_{ON} ripple control architecture combines the advantages of fixed frequency operation and fast transient response in a single device.

The MIC26400 offers a full suite of protection features to ensure protection of the IC during fault conditions. These include undervoltage lockout to ensure proper operation under power-sag conditions, internal soft-start to reduce inrush current, foldback current limit, "hiccup" mode short-circuit protection, and thermal shutdown.

Features

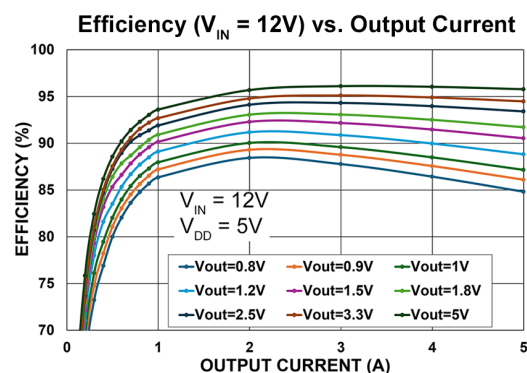
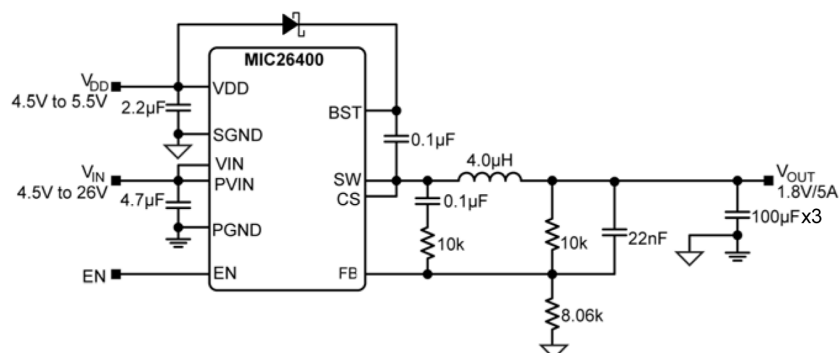
- Hyper Speed Control® Architecture Enables:
 - High Delta V Operation ($V_{IN} = 26V$ and $V_{OUT} = 0.8V$)
 - Small Output Capacitance
- 4.5V to 26V Input Voltage
- Adjustable Output from 0.8V to 5.5V ($\pm 1\%$ Accuracy)
- Any Capacitor™ Stable: Zero ESR to High ESR Output Capacitance
- 5A Output Current Capability
- 300kHz Switching Frequency
- Internal Compensation
- Up to 97% Efficiency
- 6ms Internal Soft-Start
- Foldback Current Limit and "Hiccup" Mode Short-Circuit Protection
- Thermal Shutdown
- Supports Safe Start-Up into a Pre-Biased Load
- $-40^{\circ}C$ to $+125^{\circ}C$ Junction Temperature Range
- 28-Lead 5mm x 6mm VQFN Package

Applications

- Distributed Power Systems
- Communications/Networking Infrastructure
- Set-Top Box, Gateways, and Routers
- Printers, Scanners, Graphics Cards, and Video Cards

Typical Application Circuit

Figure 1. Typical Application Circuit



Functional Block Diagram

Figure 2. Functional Block Diagram

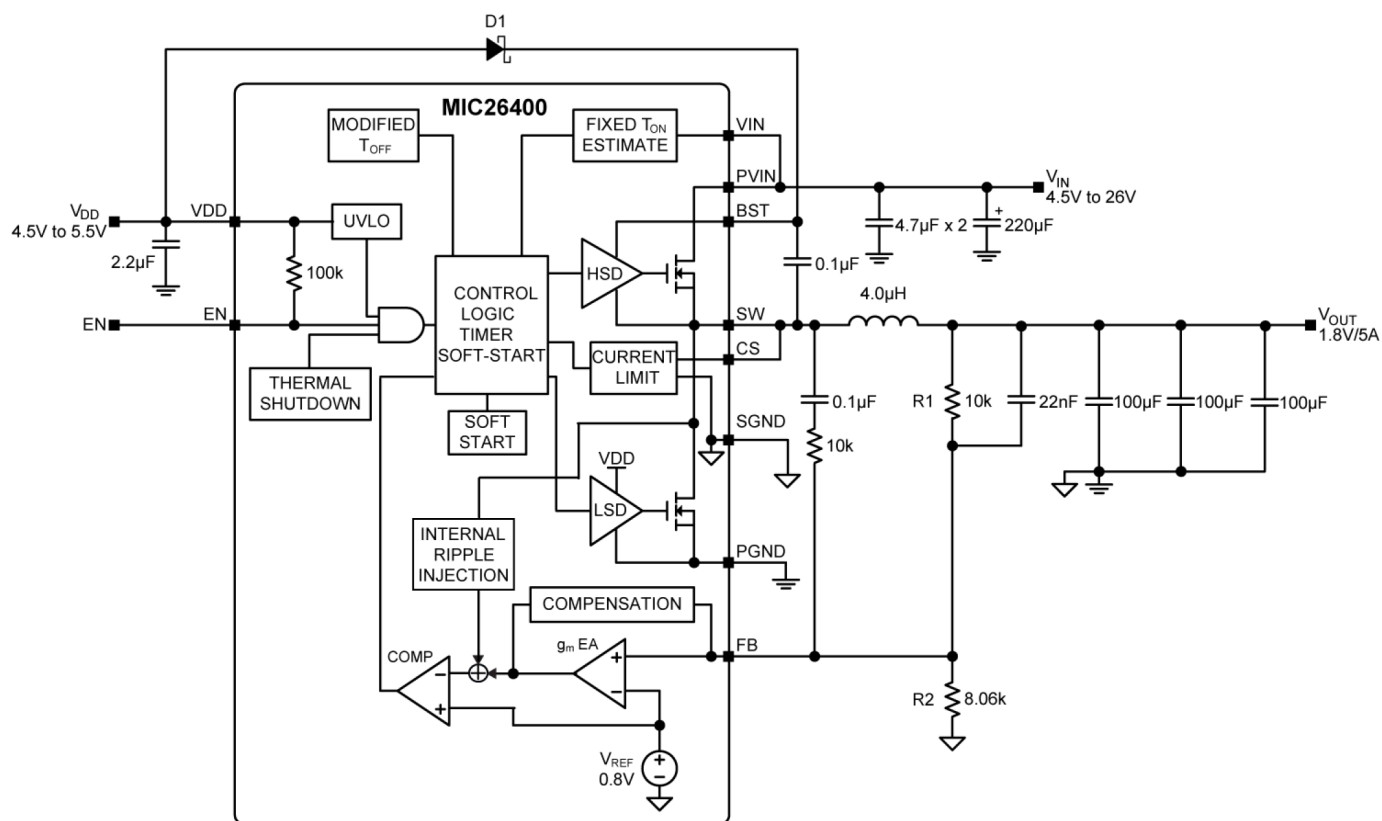


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1. Electrical Characteristics

Table 1-1. Absolute Maximum Ratings

PV _{IN} to PGND	-0.3V to +28V
V _{IN} to PGND	-0.3V to PV _{IN}
V _{DD} to PGND	-0.3V to +6V
V _{SW} , V _{CS} to PGND	-0.3V to (PV _{IN} + 0.3V)
V _{BST} to V _{SW}	-0.3V to +6V
V _{BST} to PGND	-0.3V to +34V
V _{EN} to PGND	-0.3V to (V _{DD} + 0.3V)
V _{FB} to PGND	-0.3V to (V _{DD} + 0.3V)
PGND to SGND	-0.3V to +0.3V
Notes:	
1. Exceeding the absolute maximum rating may damage the device.	
2. Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5kΩ in series with 100pF.	

Table 1-2. Operating Ratings

Supply Voltage (PV _{IN} , V _{IN})	+4.5V to +26V
Output Voltage (V _{OUT})	+0.8V to +5.5V
Bias Voltage (V _{DD})	+4.5V to +5.5V
Enable Input (V _{EN})	0V to V _{DD}
Maximum Power Dissipation	Note 2
1. The device is not guaranteed to function outside the operating range.	
2. $P_{D(MAX)} = (T_{J(MAX)} - T_A)/\theta_{JA}$, where θ_{JA} depends upon the printed circuit layout. See the Application Information section for more information.	

Table 1-3. Electrical Characteristics

PV _{IN} = V _{IN} = 12V, V _{DD} = 5V; V _{BST} - V _{SW} = 5V; T _A = 25°C, unless noted. Bold values valid for -40°C ≤ T_J ≤ +125°C. (Note 1)					
Parameter	Min.	Typ.	Max.	Units	Conditions
Power Supply Input					
Input Voltage Range (V _{IN} , PV _{IN})	4.5	—	26	V	—
V_{DD} Bias Voltage					
Operating Bias Voltage (V _{DD})	4.5	5	5.5	V	—
Undervoltage Lockout Trip Level	2.4	2.7	3.2	V	V _{DD} rising
UVLO Hysteresis	—	50	—	mV	—
Quiescent Supply Current	—	1.4	3	mA	V _{FB} = 1.5V (non-switching)
Shutdown Supply Current	—	0.7	2	mA	V _{DD} = V _{BST} = 5.5V, V _{IN} = 26V, SW = unconnected, V _{EN} = 0V
Reference					
Feedback Reference Voltage	0.792	0.8	0.808	V	0°C ≤ T _J ≤ 85°C (±1.0%)
	0.788	0.8	0.812	V	-40°C ≤ T _J ≤ 125°C (±1.5%)
Load Regulation	—	0.2	—	%	I _{OUT} = 0A to 5A
Line Regulation	—	0.1	—	%	V _{IN} = 4.5V to 26V
FB Bias Current	—	5	—	nA	V _{FB} = 0.8V
Enable Control					
EN Logic Level High	—	1.2	—	V	4.5V < V _{DD} < 5.5V

Table 1-3. Electrical Characteristics (continued)

PV_{IN} = V_{IN} = 12V, V_{DD} = 5V; V_{BST} - V_{SW} = 5V; T_A = 25°C, unless noted. Bold values valid for -40°C ≤ T_J ≤ +125°C. (Note 1)					
Parameter	Min.	Typ.	Max.	Units	Conditions
EN Logic Level Low	—	0.78	—	V	4.5V < V _{DD} < 5.5V
EN Bias Current	—	50	—	μA	V _{EN} = 0V
Oscillator					
Switching Frequency	225	300	375	kHz	Note 2
Maximum Duty Cycle	—	87	—	%	Note 3, V _{FB} = 0V
Minimum Duty Cycle	—	0	—	%	V _{FB} > 0.8V
Minimum Off Time	—	360	—	ns	—
Soft-Start					
Soft-Start Time	—	6	—	ms	—
Short-Circuit Protection					
Current Limit Threshold	—	16	—	A	V _{FB} = 0.8V
Short Circuit Current	—	6	—	A	V _{FB} = 0V
Internal FETs					
Top-MOSFET R _{DS(ON)}	—	22.6	—	mΩ	I _{SW} = 1A
Bottom-MOSFET R _{DS(ON)}	—	13.6	—	mΩ	I _{SW} = 1A
SW Leakage Current	—	—	60	μA	V _{IN} = 26V, V _{SW} = 26V, V _{EN} = 0V, V _{BST} = 31.5V
V _{IN} Leakage Current	—	—	25	μA	V _{IN} = 26V, V _{SW} = 0V, V _{EN} = 0V, V _{BST} = 31.5V
Thermal Protection					
Overtemperature Shutdown	—	155	—	°C	T _J rising
Overtemperature Shutdown Hysteresis	—	10	—	°C	—
1. Specification for packaged product only. 2. Measured in test mode. 3. The maximum duty cycle is limited by the fixed mandatory off-time (t _{OFF}) of typically 360ns.					

Table 1-4. Temperature Specifications

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Junction Temperature Range	T _J	-40	—	+125	°C	—
Maximum Junction Temperature	T _{J(MAX)}	—	—	+150	°C	—
Storage Temperature Range	T _{STORE}	-65	—	+150	°C	—
Lead Temperature	T _{LEAD}	—	—	+260	°C	Soldering, 10 sec.
Package Thermal Resistances						
Thermal Resistance, VQFN 28-Ld	θ _{JA}	—	36	—	°C/W	—

2. Typical Operating Characteristics

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: All tests have been performed without the RC Snubber. Please refer to the [Evaluation Board Schematic](#).

Figure 2-1. V_{IN} Operating Supply Current vs. Input Voltage

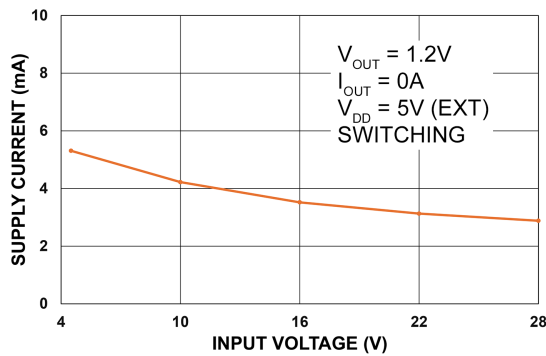


Figure 2-2. V_{IN} Shutdown Current vs. Input Voltage

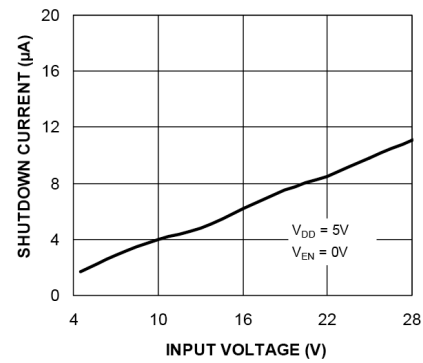


Figure 2-3. V_{DD} Operating Supply Current vs. Input Voltage

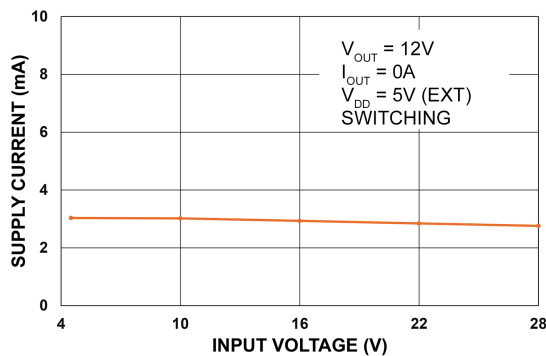


Figure 2-4. Feedback Voltage vs. Input Voltage

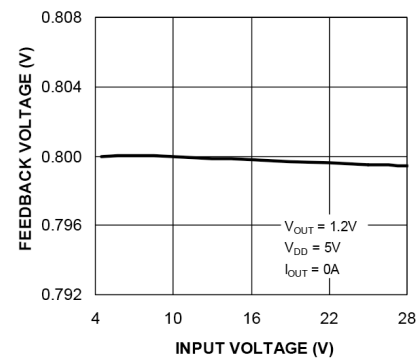


Figure 2-5. Total Regulation vs. Input Voltage

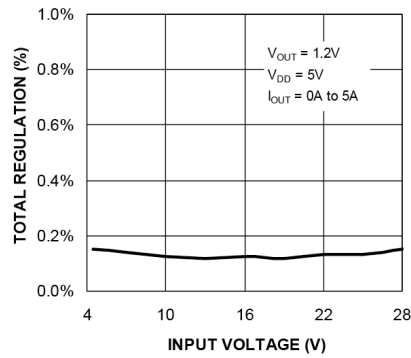


Figure 2-6. Current Limit vs. Input Voltage

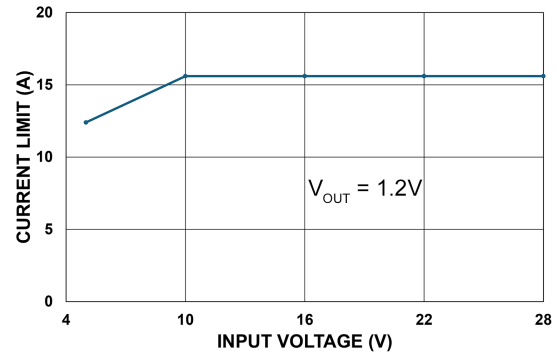


Figure 2-7. Switching Frequency vs. Input Voltage

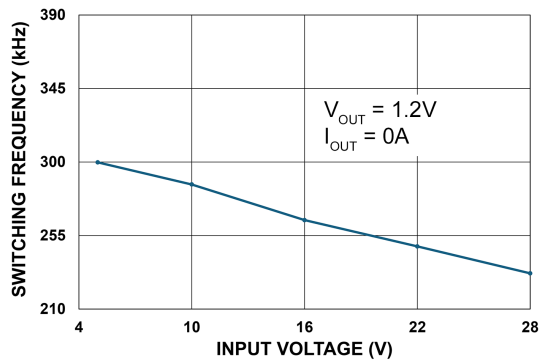


Figure 2-8. V_{DD} Operating Supply Current vs. Temperature

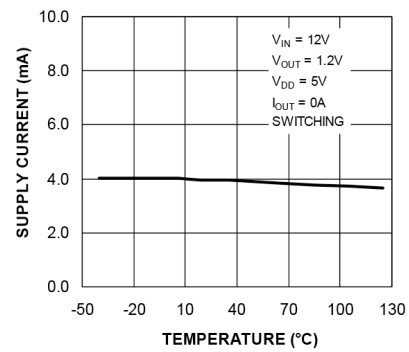


Figure 2-9. V_{DD} Shutdown Current vs. Temperature

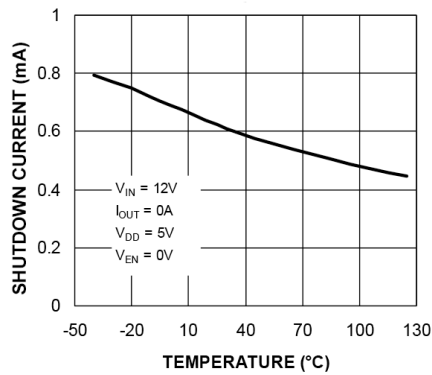


Figure 2-10. V_{DD} UVLO Threshold vs. Temperature

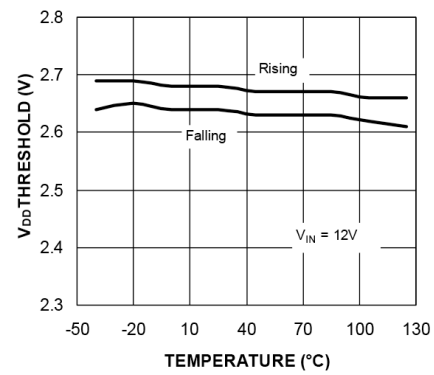


Figure 2-11. V_{IN} Operating Supply Current vs. Temperature

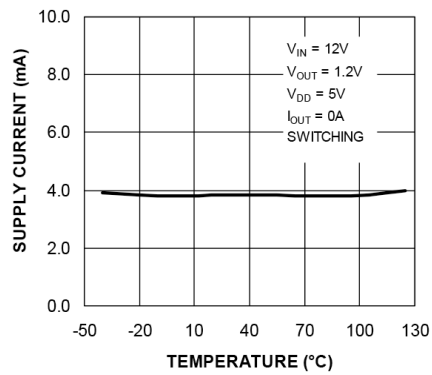


Figure 2-12. V_{IN} Shutdown Current vs. Temperature

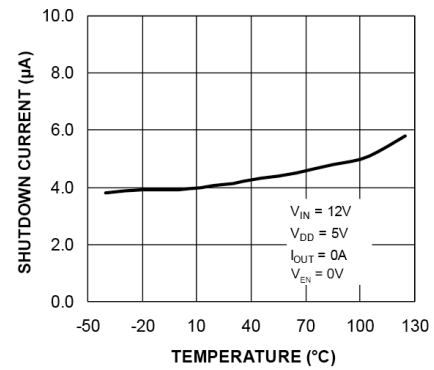


Figure 2-13. Current Limit vs. Temperature

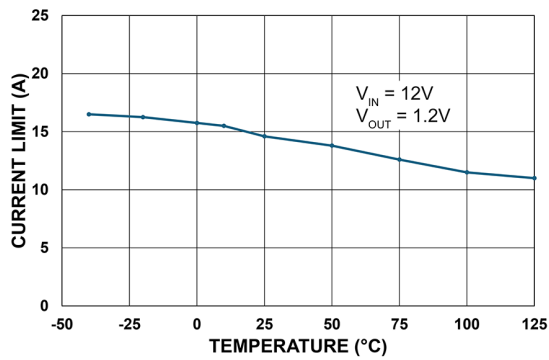


Figure 2-14. Feedback Voltage vs. Temperature

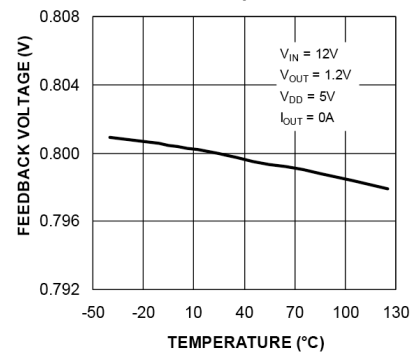


Figure 2-15. Load Regulation vs. Temperature

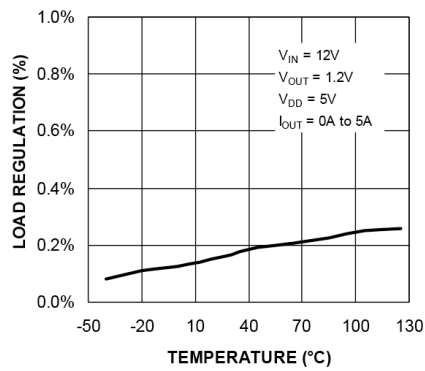


Figure 2-16. Line Regulation vs. Temperature

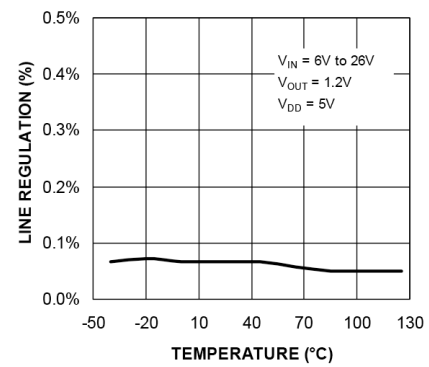


Figure 2-17. Switching Frequency vs. Temperature

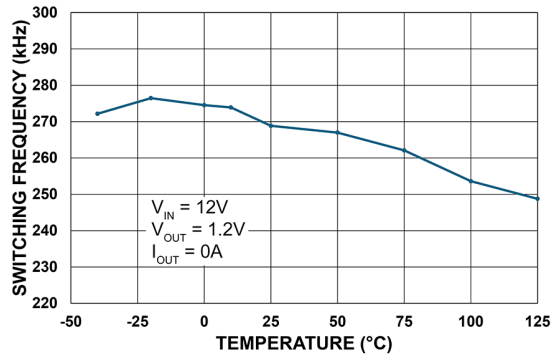


Figure 2-18. EN Bias Current vs. Temperature

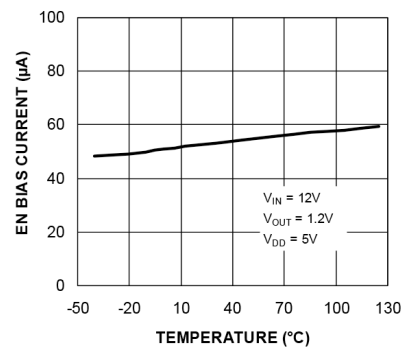


Figure 2-19. Efficiency vs. Output Current

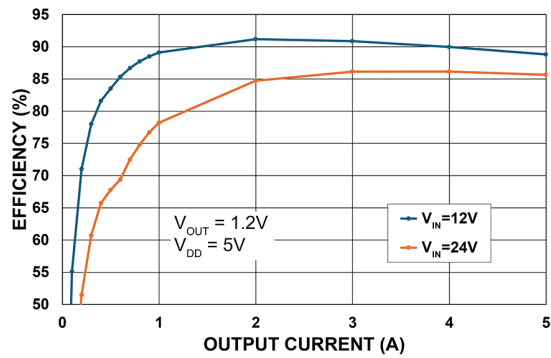


Figure 2-20. Feedback Voltage vs. Output Current

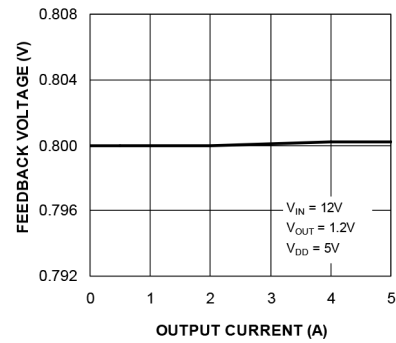


Figure 2-21. Output Voltage vs. Output Current

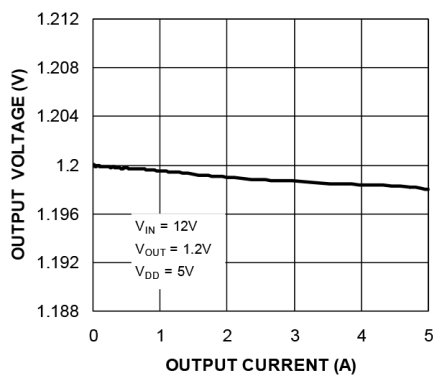


Figure 2-22. Line Regulation vs. Output Current

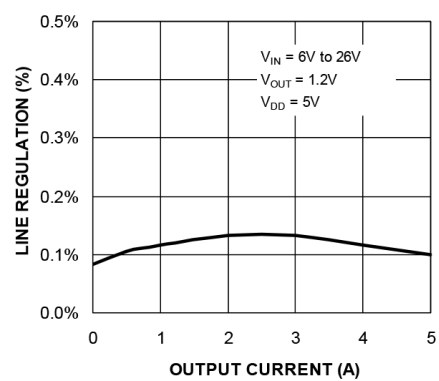


Figure 2-23. Switching Frequency vs. Output Current

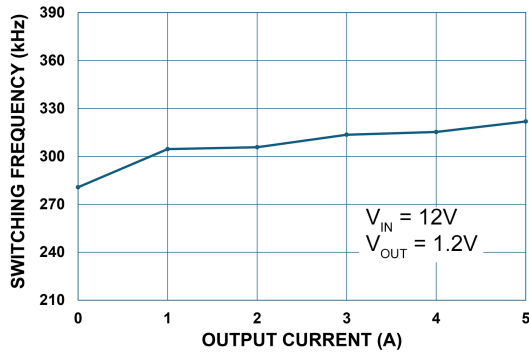
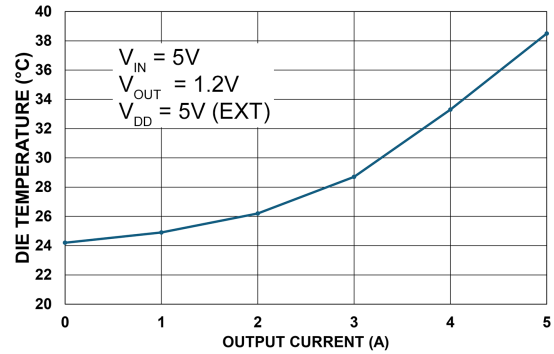
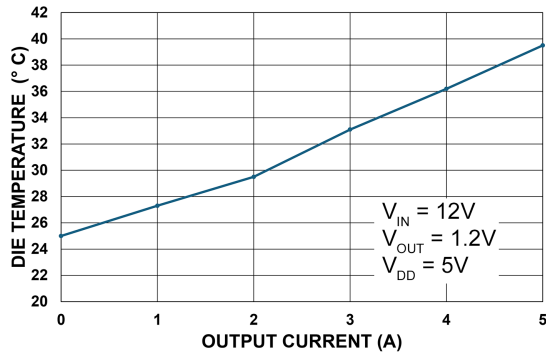


Figure 2-24. Die Temperature ($V_{IN} = 5V$) vs. Output Current



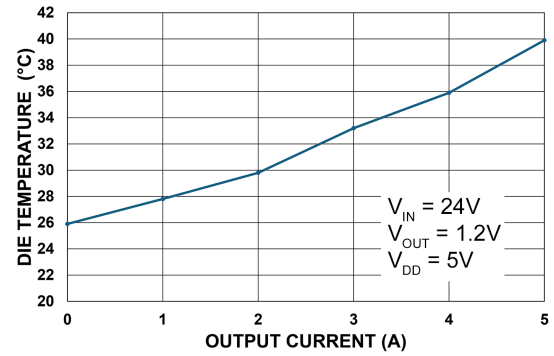
Note1

Figure 2-25. Die Temperature ($V_{IN} = 12V$) vs. Output Current



Note1

Figure 2-26. Die Temperature ($V_{IN} = 24V$) vs. Output Current



Note1

Figure 2-27. Efficiency ($V_{IN} = 5V$) vs. Output Current

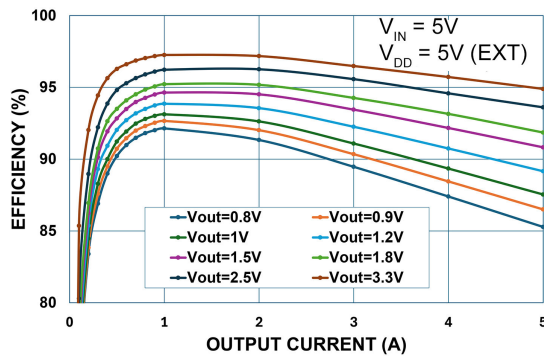


Figure 2-28. Efficiency ($V_{IN} = 12V$) vs. Output Current

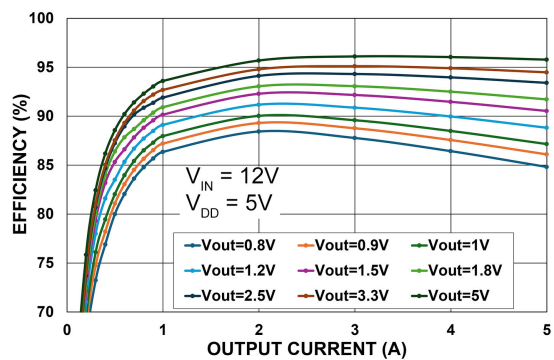


Figure 2-29. Efficiency ($V_{IN} = 24V$) vs. Output Current

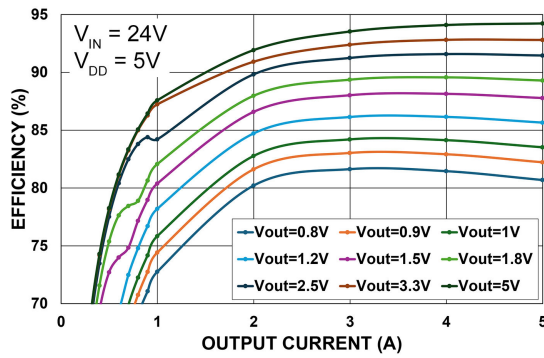


Figure 2-30. IC Power Dissipation ($V_{IN} = 5V$) vs. Output Current

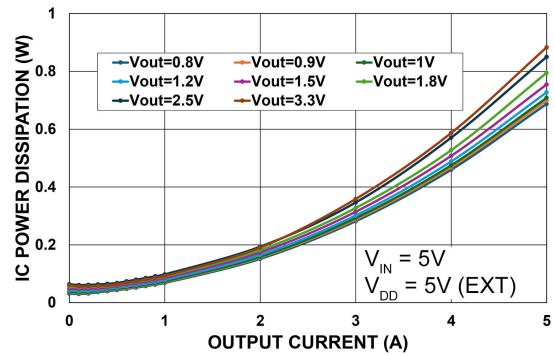


Figure 2-31. IC Power Dissipation ($V_{IN} = 12V$) vs. Output Current

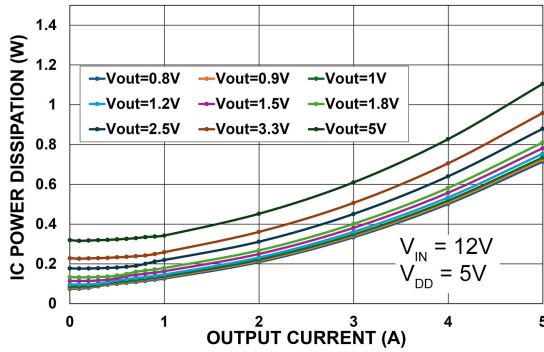


Figure 2-32. IC Power Dissipation ($V_{IN} = 24V$) vs. Output Current

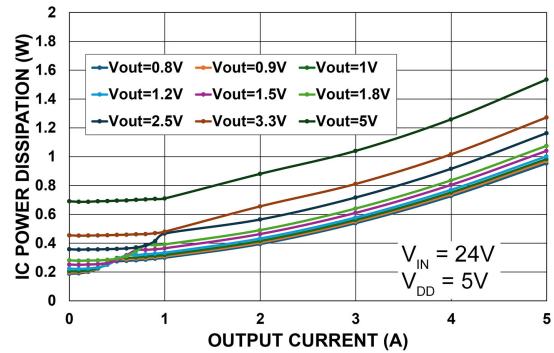
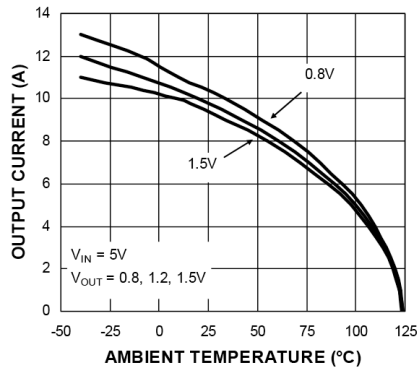
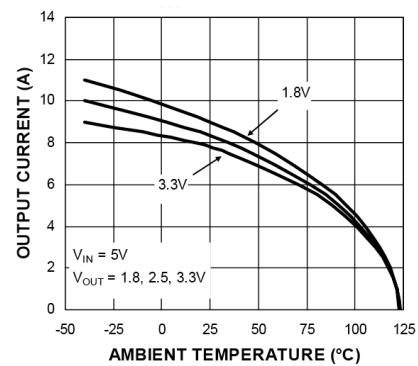


Figure 2-33. Thermal Derating vs. Ambient Temperature



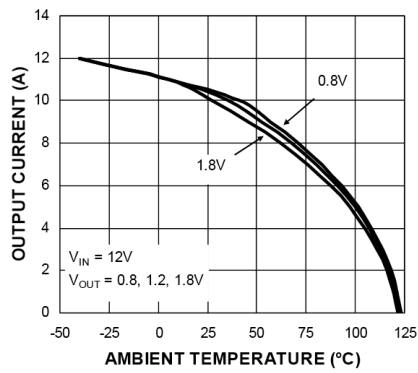
Note1

Figure 2-34. Thermal Derating vs. Ambient Temperature



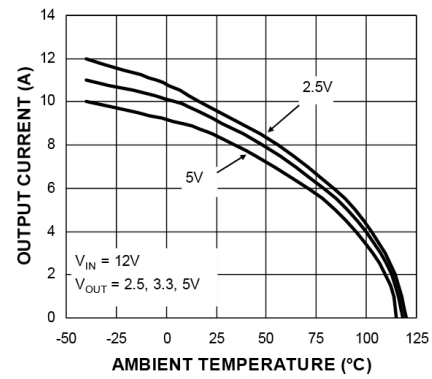
Note1

Figure 2-35. Thermal Derating vs. Ambient Temperature



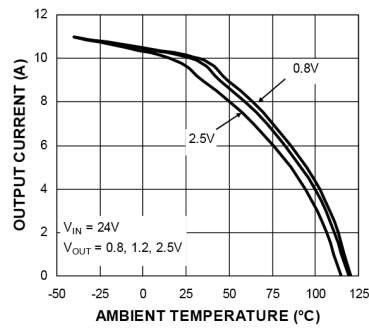
Note1

Figure 2-36. Thermal Derating vs. Ambient Temperature



Note1

Figure 2-37. Thermal Derating vs. Ambient Temperature



Note1

Figure 2-38. V_{IN} Soft Turn-On

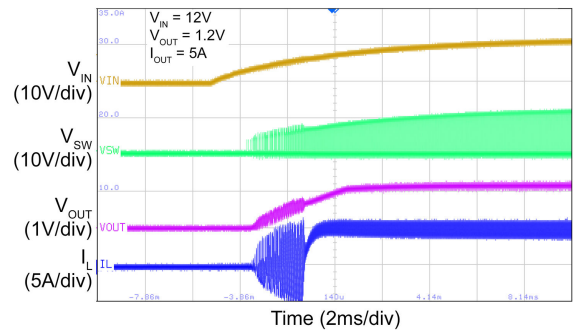


Figure 2-39. V_{IN} Soft Turn-Off

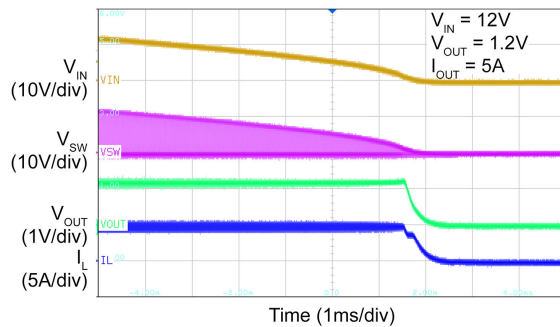


Figure 2-40. V_{EN} Enable Turn-On Delay and Rise Time

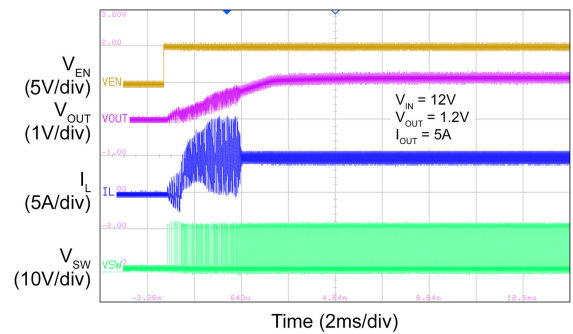


Figure 2-41. V_{EN} Enable Turn-Off Delay and Fall Time

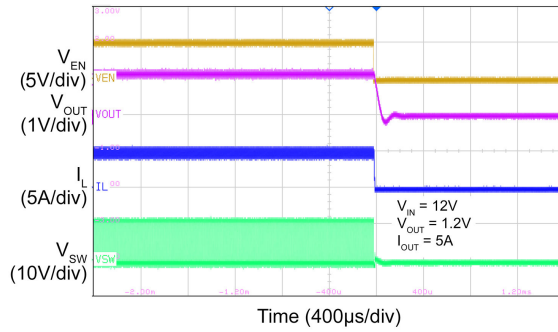


Figure 2-42. V_{IN} Start-Up with Pre-Biased Output

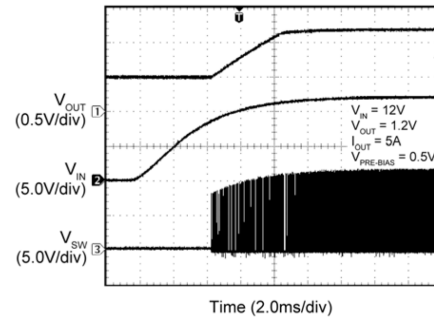


Figure 2-43. V_{EN} Enable Turn-On/Turn-Off

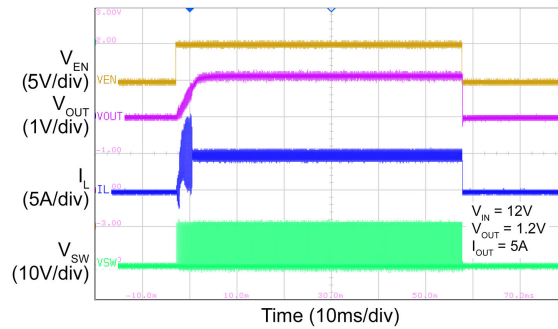


Figure 2-44. V_{EN} Enable Thresholds

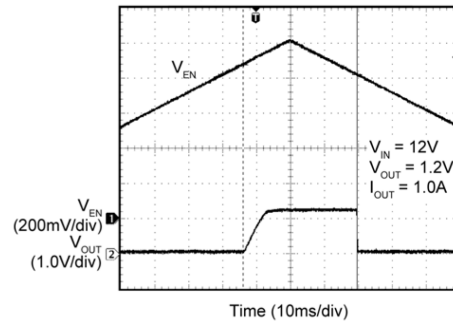


Figure 2-45. V_{DD} UVLO Thresholds

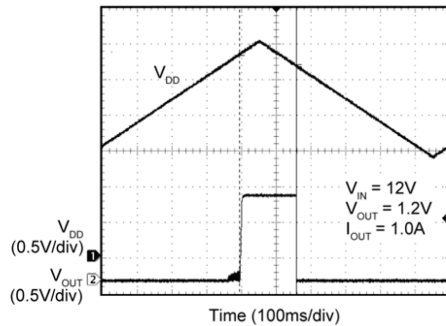


Figure 2-46. Power-Up into Short Circuit

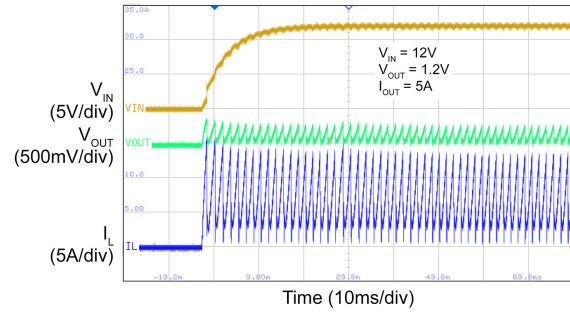


Figure 2-47. Enabled into Short Circuit

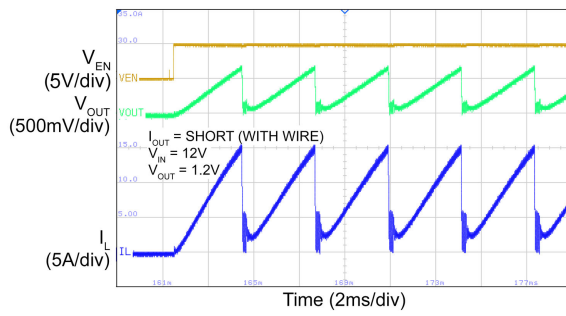


Figure 2-48. Short Circuit

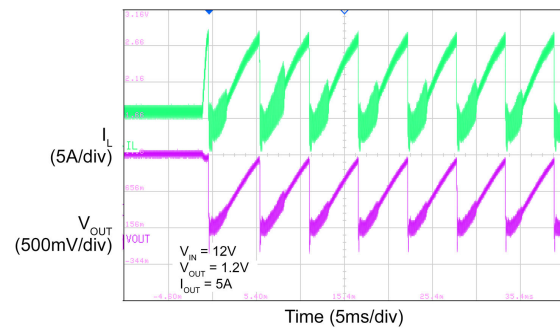


Figure 2-49. Output Recovery Short Circuit

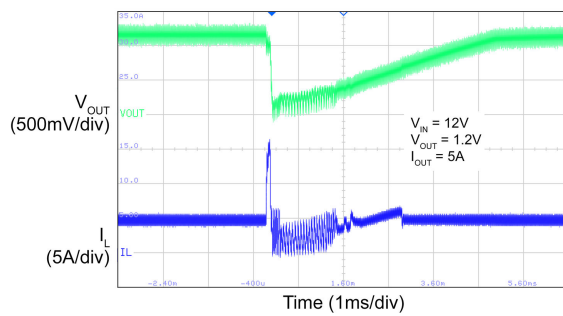


Figure 2-50. Peak Current Limit Threshold

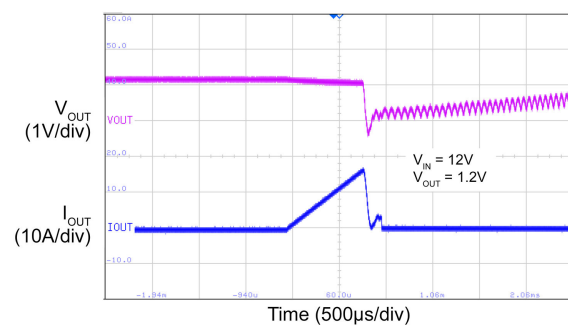


Figure 2-51. Output Recovery from Thermal Shutdown

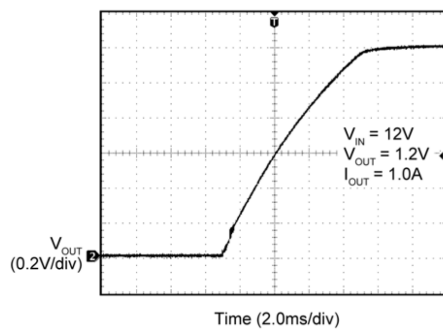


Figure 2-52. Switching Waveforms, $I_{OUT} = 5A$

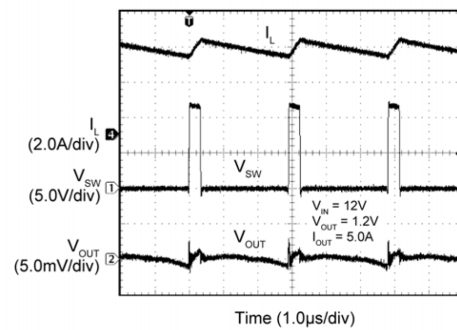


Figure 2-53. Switching Waveforms, $I_{OUT} = 0A$

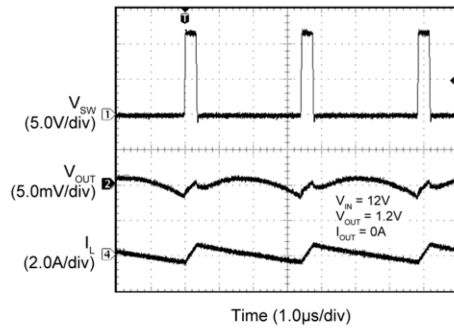
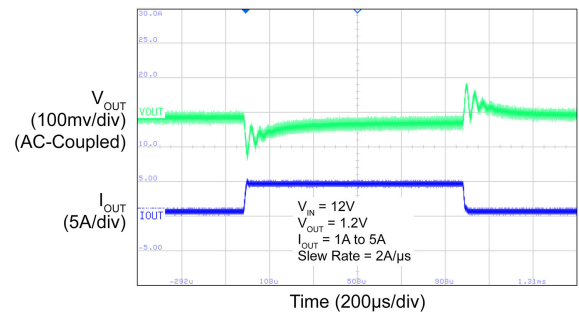


Figure 2-54. Transient Response



Notes:

1. The temperature measurement was taken at the hottest point on the MIC26400 case mounted on a 5 square inch 4-layer, 0.062", FR-4 PCB with 2oz. finish copper weight per layer, see the [Thermal Measurements](#) section. Actual results will depend upon the size of the PCB, ambient temperature, and proximity to other heat emitting components.

3. Pin Description

Figure 3-1. Pin Configuration

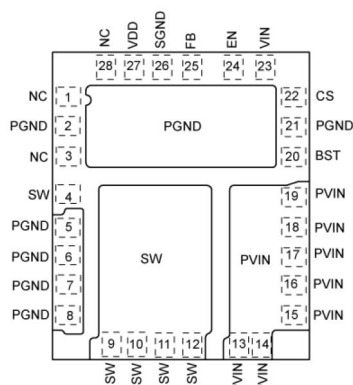


Table 3-1. Pin Descriptions

Pin Number	Pin Name	Pin Function
13, 14, 15, 16, 17, 18, 19	PVIN	High-Side Internal N-Channel MOSFET Drain Connection (Input): The PVIN operating voltage range is from 4.5V to 26V. Input capacitors between the PVIN pins and the power ground (PGND) are required. Note that the connections must be kept short.
24	EN	Enable (Input): A logic level control of the output. The EN pin is CMOS-compatible. Logic high or floating = enable, logic low = shutdown. In the off state, the VDD supply current of the device is reduced (typically 0.7mA).
25	FB	Feedback (Input): Input to the transconductance amplifier of the control loop. The FB pin is regulated to 0.8V. A resistor divider connecting the feedback to the output is used to adjust the desired output voltage.
26	SGND	Signal Ground. SGND must be connected directly to the ground planes. Do not route the SGND pin to the PGND Pad on the top layer. See the PCB Layout Guidelines section for details.
27	VDD	VDD Bias (Input): Power to the internal reference and control sections of the MIC26400. The VDD operating voltage range is from 4.5V to 5.5V. A 2.2μF ceramic capacitor from the VDD pin to SGND must be placed next to the IC.
2, 5, 6, 7, 8, 21	PGND	Power Ground. PGND is the ground path for the MIC26400 buck converter power stage. The PGND pin connects to the source of the low-side N-Channel internal MOSFET, the negative terminals of input capacitors, and the negative terminals of output capacitors. The loop for the power ground should be as small as possible and separate from the Signal Ground (SGND) loop.
22	CS	Current Sense (Input): High current output driver return. The CS pin connects directly to the switch node. Due to the high speed switching on this pin, the CS pin should be routed away from sensitive nodes. CS pin also senses the current by monitoring the voltage across the low-side internal MOSFET during OFF-time.
20	BST	Bootstrap (Input): Bootstrapped voltage to the high-side N-channel internal MOSFET driver. A Schottky diode is connected between the VDD pin and the BST pin. A boost capacitor of 0.1μF is connected between the BST pin and the SW pin.
4, 9, 10, 11, 12	SW	Switch Node (Output): Internal connection for the high-side MOSFET source and low-side MOSFET drain.
23	VIN	Power Supply Voltage (Input): Requires a bypass capacitor to PGND.
1, 3, 28	NC	No Connect.

4. Functional Description

The MIC26400 is an adaptive ON-time synchronous step-down DC/DC regulator. It is designed to operate over a wide input voltage range from 4.5V to 26V and to provide a regulated output voltage at up to 5A of output current. A modified adaptive ON-time control scheme is employed in order to obtain a nearly constant switching frequency and to simplify the control compensation. Overcurrent protection is implemented without the use of an external sense resistor. The device includes an internal soft-start function that reduces the power supply input surge current at start-up by controlling the output voltage rise time.

4.1. Theory of Operation

The [Functional Block Diagram](#) illustrates the control loop of the MIC26400. The output voltage is sensed by the MIC26400 feedback pin FB via the voltage divider R1 and R2, and compared to a 0.8V reference voltage, V_{REF} , at the error comparator through a low gain transconductance (g_m) amplifier. If the feedback voltage decreases and the output of the g_m amplifier is below 0.8V, then the error comparator will trigger the control logic and generate an ON-time period. The ON-time period length is predetermined by the "FIXED t_{ON} ESTIMATION" circuitry in the block diagram:

Equation 4-1.

$$t_{ON(ESTIMATED)} = \frac{V_{OUT}}{V_{IN} \times 300kHz}$$

Where:

V_{OUT} = The output voltage.

V_{IN} = The power stage input voltage.

At the end of the ON-time period, the internal high-side driver turns off the high-side MOSFET and the low-side driver turns on the low-side MOSFET. The OFF-time period length depends upon the feedback voltage, in most cases. When the feedback voltage decreases and the output of the g_m amplifier is below 0.8V, the ON-time period is triggered and the OFF-time period ends. If the OFF-time period determined by the feedback voltage is less than the minimum OFF-time $t_{OFF(MIN)}$, which is about 360ns, the MIC26400 control logic will apply the $t_{OFF(MIN)}$ instead. $t_{OFF(MIN)}$ is required to maintain enough energy in the boost capacitor (C_{BST}) to drive the high-side MOSFET. The maximum duty cycle is obtained from the 360ns $t_{OFF(MIN)}$:

Equation 4-2.

$$D_{MAX} = \frac{t_S - t_{OFF(MIN)}}{t_S} = 1 - \frac{360ns}{t_S}$$

Where:

$t_S = 1/300kHz = 3.33\mu s$.

Microchip does not recommend using MIC26400 with an OFF-time close to $t_{OFF(MIN)}$ during steady-state operation. Also, as V_{OUT} increases, the internal ripple injection will increase and reduce the line regulation performance. Therefore, the maximum output voltage of the MIC26400 should be limited to 5.5V. Please refer to the [Setting Output Voltage](#) section for more details.

The actual ON-time and resulting switching frequency will vary with the part-to-part variation in the rise and fall times of the internal MOSFETs, the output load current, and variations in the V_{DD} voltage. Also, the minimum t_{ON} results in a lower switching frequency in high V_{IN} to V_{OUT} applications, such as 26V to 1.0V. The minimum t_{ON} measured on the MIC26400 evaluation board is about 184ns. During load transients, the switching frequency is changed due to the varying OFF-time.

To illustrate the control loop operation, we will analyze both the steady-state and load transient scenarios. For easy analysis, the gain of the g_m amplifier is assumed to be 1. With this assumption, the inverting input of the error comparator is the same as the feedback voltage.

Figure 4-1 shows the MIC26400 control loop timing during steady-state operation. During steady-state, the g_m amplifier senses the feedback voltage ripple, which is proportional to the output voltage ripple and the inductor current ripple, to trigger the ON-time period. The ON-time is predetermined by the t_{ON} estimator. The termination of the OFF-time is controlled by the feedback voltage. At the valley of the feedback voltage ripple, which occurs when V_{FB} falls below V_{REF} , the OFF period ends and the next ON-time period is triggered through the control logic circuitry.

Figure 4-1. Control Loop Timing

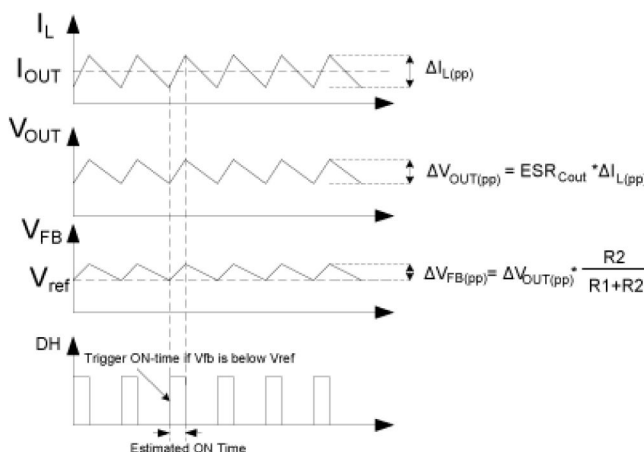
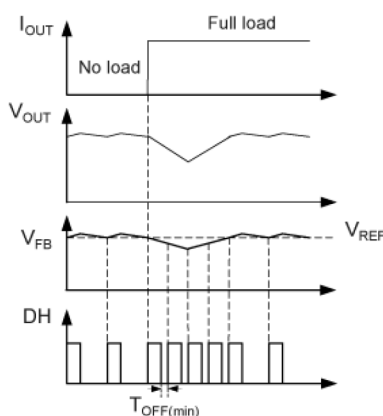


Figure 4-2 shows the operation of the MIC26400 during a load transient. The output voltage drops due to the sudden load increase, which causes V_{FB} to be less than V_{REF} . This will cause the error comparator to trigger an ON-time period. At the end of the ON-time period, a minimum OFF-time, $t_{OFF(MIN)}$, is generated to charge C_{BST} because the feedback voltage is still below V_{REF} . Then, the next ON-time period is triggered due to the low feedback voltage. Therefore, the switching frequency changes during the load transient, but returns to the nominal fixed frequency once the output has stabilized at the new load current level. With the varying duty cycle and switching frequency, the output recovery time is fast and the output voltage deviation is small in MIC26400 converter.

Figure 4-2. Load Transient Response



Unlike true current-mode control, the MIC26400 uses the output voltage ripple to trigger an ON-time period. The output voltage ripple is proportional to the inductor current ripple if the ESR of the

output capacitor is large enough. The MIC26400 control loop has the advantage of eliminating the need for slope compensation.

In order to meet the stability requirements, the MIC26400 feedback voltage ripple should be in phase with the inductor current ripple and large enough to be sensed by the g_m amplifier and the error comparator. The recommended feedback voltage ripple is 20mV~100mV. If a low-ESR output capacitor is selected, the feedback voltage ripple may be too small to be sensed by the g_m amplifier and the error comparator. Also, the output voltage ripple and the feedback voltage ripple are not necessarily in phase with the inductor current ripple if the ESR of the output capacitor is very low. In these cases, ripple injection is required to ensure proper operation. Please refer to the [Ripple Injection](#) section for more details about the ripple injection technique.

4.2. Soft-Start

Soft-start reduces the power supply input surge current at start-up by controlling the output voltage rise time. The input surge appears while the output capacitor is charged up. A slower output rise time will draw a lower input surge current.

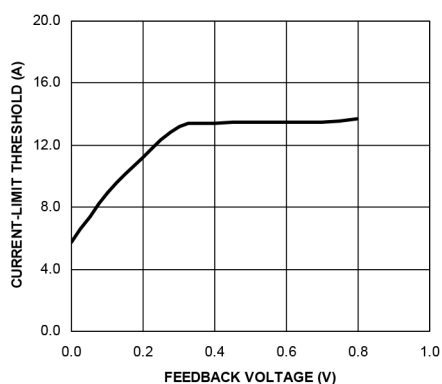
The MIC26400 implements an internal digital soft-start by making the 0.8V reference voltage, V_{REF} , ramp from 0% to 100% in about 6ms with 9.7mV steps. Therefore, the output voltage is controlled to increase slowly by a stair-case V_{FB} ramp. Once the soft-start cycle ends, the related circuitry is disabled to reduce current consumption. VDD must be powered up at the same time or after VIN to make the soft-start function correctly.

4.3. Current Limit

The MIC26400 uses the $R_{DS(ON)}$ of the internal low-side power MOSFET to sense over-current conditions. This method will avoid adding cost, board space, and power losses taken by a discrete current sense resistor. The low-side MOSFET is used because it displays much lower parasitic oscillations during switching than the high-side MOSFET.

In each switching cycle of the MIC26400 converter, the inductor current is sensed by monitoring the low-side MOSFET in the OFF period. If the inductor current is greater than the current limit threshold, then the MIC26400 turns off the high-side MOSFET and a soft-start sequence is triggered. This mode of operation is called “hiccup mode” and its purpose is to protect the downstream load in case of a hard short. The current limit threshold has a foldback characteristic related to the feedback voltage, as shown in [Figure 4-3](#).

Figure 4-3. Current Limit Foldback Characteristic



4.4. VDD

The MIC26400 requires an external VDD supply to bias the internal reference and control circuitry. This supply can be provided either through the on-board regulator circuit on the evaluation board or from an independent external power supply. The regulator derives the VDD rail from the input voltage. At higher input voltages, the power dissipated in this regulator increases proportionally, reducing the converter efficiency. In such conditions, the regulator can be disabled, allowing VDD to be supplied directly from an external source. Bypassing the regulator reduces bias-related power losses and improves the overall efficiency of the converter.

4.5. MOSFET Gate Drive

The [Functional Block Diagram](#) shows a bootstrap circuit, consisting of D1 (a Schottky diode is recommended) and C_{BST} . This circuit supplies energy to the high-side drive circuit. Capacitor C_{BST} is charged, while the low-side MOSFET is on, and the voltage on the SW pin is approximately 0V. When the high-side MOSFET driver is turned on, energy from C_{BST} is used to turn the MOSFET on. As the high-side MOSFET turns on, the voltage on the SW pin increases to approximately V_{IN} . Diode D1 is reverse biased and C_{BST} floats high while continuing to keep the high-side MOSFET on. The bias current of the high-side driver is less than 10mA, so a 0.1 μ F to 1 μ F capacitor is sufficient to hold the gate voltage with minimal droop for the power stroke (high-side switching) cycle, (i.e. $\Delta BST = 10\text{mA} \times 3.33\mu\text{s} / 0.1\mu\text{F} = 333\text{mV}$). When the low-side MOSFET is turned back on, C_{BST} is recharged through D1. A small resistor R_G , which is in series with C_{BST} , can be used to slow down the turn-on time of the high-side N-channel MOSFET.

The drive voltage is derived from the V_{DD} supply voltage. The nominal low-side gate drive voltage is V_{DD} and the nominal high-side gate drive voltage is approximately $V_{DD} - V_{DIODE}$, where V_{DIODE} is the voltage drop across D1. An approximate 30ns delay between the high-side and low-side driver transitions is used to prevent current from simultaneously flowing unimpeded through both MOSFETs.

5. Application Information

5.1. Inductor Selection

Values for inductance, peak, and RMS currents are required to select the output inductor. The input and output voltages and the inductance value determine the peak-to-peak inductor ripple current. Generally, higher inductance values are used with higher input voltages. Larger peak-to-peak ripple currents will increase the power dissipation in the inductor and MOSFETs. Larger output ripple currents will also require more output capacitance to smooth out the larger ripple current. Smaller peak-to-peak ripple currents require a larger inductance value and, therefore, a larger and more expensive inductor. A good compromise between size, loss, and cost is to set the inductor ripple current to be equal to 20% of the maximum output current. The inductance value is calculated by the equation below:

Equation 5-1.

$$L = \frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{V_{IN(MAX)} \times f_{SW} \times 20\% \times I_{OUT(MAX)}}$$

Where:

f_{SW} = Switching frequency, 300kHz.

20% = The ratio of AC ripple current to DC output current.

$V_{IN(MAX)}$ = The maximum power stage input voltage.

The peak-to-peak inductor current ripple is:

Equation 5-2.

$$\Delta I_{L(PP)} = \frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{V_{IN(MAX)} \times f_{SW} \times L}$$

The peak inductor current is equal to the average output current plus one half of the peak-to-peak inductor current ripple.

Equation 5-3.

$$I_{L(PK)} = I_{OUT(MAX)} + 0.5 \times \Delta I_{L(PP)}$$

The RMS inductor current is used to calculate the I^2R losses in the inductor.

Equation 5-4.

$$I_{L(RMS)} = \sqrt{I_{OUT(MAX)}^2 + \frac{\Delta I_{L(PP)}^2}{12}}$$

Maximizing efficiency requires the proper selection of core material and minimizing the winding resistance. The high frequency operation of the MIC26400 requires the use of ferrite materials for all but the most cost sensitive applications. Lower cost iron powder cores may be used but the increase in core loss will reduce the efficiency of the power supply. This is especially noticeable at low output power. The winding resistance decreases efficiency at the higher output current levels. The winding resistance must be minimized, although this usually comes at the expense of a larger inductor. The power dissipated in the inductor is equal to the sum of the core and copper losses. At higher output loads, the core losses are usually insignificant and can be ignored. At lower output currents, the core losses can be a significant contributor. Core loss information is usually available from the magnetics vendor. Copper loss in the inductor is calculated by the equation below:

Equation 5-5.

$$P_{INDUCTOR(CU)} = I_{L(RMS)}^2 \times R_{WINDING}$$

The resistance of the copper wire, $R_{WINDING}$, increases with temperature. The value of the winding resistance used should be at the operating temperature.

Equation 5-6.

$$R_{WINDING(HT)} = R_{WINDING(20^{\circ}C)} \times (1 + 0.0042 \times (T_H - T_{20^{\circ}C}))$$

Where:

T_H = Temperature of the wire under full load.

$T_{20^{\circ}C}$ = Ambient temperature.

$R_{WINDING(20^{\circ}C)}$ = Room temperature winding resistance (usually specified by the manufacturer).

5.2. Output Capacitor Selection

The type of the output capacitor is usually determined by its ESR (equivalent series resistance). Voltage and RMS current capability are two other important factors for selecting the output capacitor. Recommended capacitor types are tantalum, low-ESR aluminum electrolytic, OS-CON, and POSCAP. The output capacitor's ESR is usually the main cause of the output ripple. The output capacitor ESR also affects the control loop from a stability point of view. The maximum value of ESR is calculated:

Equation 5-7.

$$ESR_{C_{OUT}} \leq \frac{\Delta V_{OUT(PP)}}{\Delta I_{L(PP)}}$$

Where:

$\Delta V_{OUT(PP)}$ = Peak-to-peak output voltage ripple.

$\Delta I_{L(PP)}$ = Peak-to-peak inductor current ripple.

The total output ripple is a combination of the ESR and output capacitance. The total ripple is calculated below:

Equation 5-8.

$$\Delta V_{OUT(PP)} = \sqrt{\left(\frac{\Delta I_{L(PP)}}{C_{OUT} \times f_{SW} \times 8}\right)^2 + (\Delta I_{L(PP)} \times ESR_{C_{OUT}})^2}$$

Where:

C_{OUT} = The output capacitance value.

f_{SW} = The switching frequency.

As described in the [Theory of Operation](#) section, the MIC26400 requires at least 20mV peak-to-peak ripple at the FB pin to make the g_m amplifier and the error comparator behave properly. Also, the output voltage ripple should be in phase with the inductor current. Therefore, the output voltage ripple caused by the output capacitors value should be much smaller than the ripple caused by the output capacitor ESR. If low-ESR capacitors, such as ceramic capacitors, are selected as the output capacitors, a ripple injection method should be applied to provide the enough feedback voltage ripple. Please refer to the [Ripple Injection](#) section for more details.

The voltage rating of the capacitor should be twice the output voltage for a tantalum and 20% greater for aluminum electrolytic or OS-CON. The output capacitor RMS current is calculated below:

Equation 5-9.

$$I_{COUT(RMS)} = \frac{\Delta I_{L(PP)}}{\sqrt{12}}$$

The power dissipated in the output capacitor is:

Equation 5-10.

$$P_{DISS(COUT)} = I_{COUT(RMS)}^2 \times ESR_{COUT}$$

5.3. Input Capacitor Selection

The input capacitor for the power stage input should be selected for ripple current rating and voltage rating. Tantalum input capacitors may fail when subjected to high inrush currents, caused by turning the input supply on. A tantalum input capacitor's voltage rating should be at least two times the maximum input voltage to maximize reliability. Aluminum electrolytic, OS-CON, and multilayer polymer film capacitors can handle the higher inrush currents without voltage derating. The input voltage ripple will primarily depend on the input capacitor's ESR.

The peak input current is equal to the peak inductor current, so:

Equation 5-11.

$$\Delta V_{IN} = I_{L(PK)} \times ESR_{CIN}$$

The input capacitor must be rated for the input current ripple. The RMS value of the input capacitor current is determined at the maximum output current. Assuming the peak-to-peak inductor current ripple is low:

Equation 5-12.

$$I_{CIN(RMS)} \approx I_{OUT(MAX)} \times \sqrt{D \times (1 - D)}$$

The power dissipated in the input capacitor is:

Equation 5-13.

$$P_{DISS(CIN)} = I_{CIN(RMS)}^2 \times ESR_{CIN}$$

5.4. Ripple Injection

The V_{FB} ripple required for proper operation of the MIC26400 g_m amplifier and error comparator is 20mV to 100mV. However, the output voltage ripple is generally designed as 1% to 2% of the output voltage. For a low output voltage, such as 1V, the output voltage ripple is only 10mV to 20mV and the feedback voltage ripple is less than 20mV. If the feedback voltage ripple is so small that the g_m amplifier and error comparator can't sense it, the MIC26400 will lose control and the output voltage is not regulated. In order to have some amount of V_{FB} ripple, a ripple injection method is applied for low output voltage ripple applications.

The applications are divided into three situations according to the amount of the feedback voltage ripple:

1) Enough ripple at the feedback voltage due to the large ESR of the output capacitors.

As shown in [Figure 5-1](#), the converter is stable without any ripple injection. The feedback voltage ripple is:

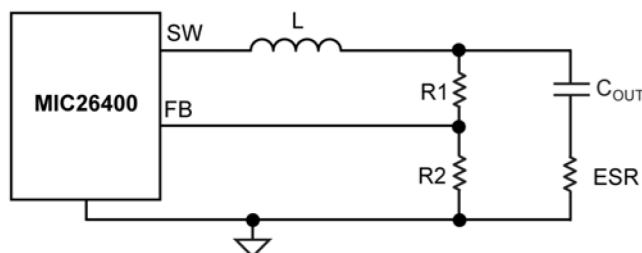
Equation 5-14.

$$\Delta V_{FB(PP)} = \frac{R1}{R1 + R2} \times ESR_{C_{OUT}} \times \Delta I_{L(PP)}$$

Where:

$\Delta I_{L(PP)}$ = The peak-to-peak value of the inductor current ripple.

Figure 5-1. Enough Ripple at FB



2) Inadequate ripple at the feedback voltage due to the small ESR of the output capacitors.

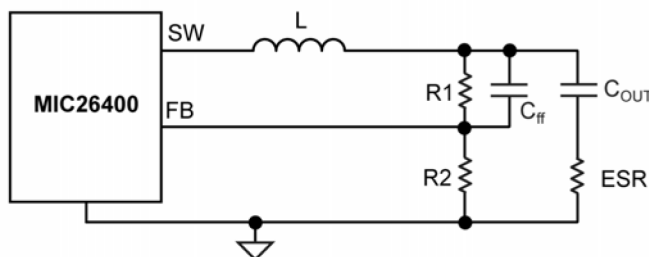
The output voltage ripple is fed into the FB pin through a feed-forward capacitor, C_{FF} in this situation, as shown in [Figure 5-2](#). The typical C_{FF} value is between 1nF and 100nF.

With the feed-forward capacitor, the feedback voltage ripple is very close to the output voltage ripple:

Equation 5-15.

$$\Delta V_{FB(PP)} \approx ESR \times \Delta I_{L(PP)}$$

Figure 5-2. Inadequate Ripple at FB



3) Virtually no ripple at the FB pin voltage due to the very low ESR of the output capacitors.

In this situation, the output voltage ripple is less than 20mV. Therefore, additional ripple is injected into the FB pin from the switching node SW via a resistor R_{INJ} and a capacitor C_{INJ} , as shown in [Figure 5-3](#). The injected ripple is:

Equation 5-16.

$$\Delta V_{FB(PP)} = V_{IN} \times K_{DIV} \times D \times (1 - D) \times \frac{1}{f_{SW} \times \tau}$$

Equation 5-17.

$$K_{DIV} = \frac{R1//R2}{R_{INJ} + R1//R2}$$

Where:

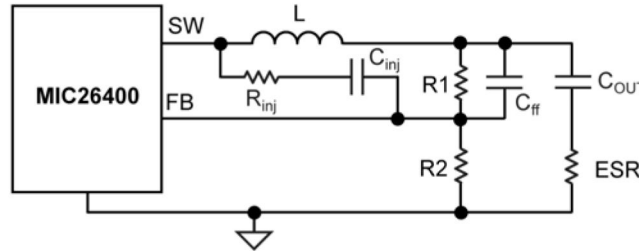
V_{IN} = The power stage input voltage.

D = Duty cycle.

f_{SW} = Switching frequency.

$\tau = (R1 // R2 // R_{INJ}) \times C_{FF}$

Figure 5-3. Invisible Ripple at FB



In the two previous equations, it is assumed that the time constant associated with C_{FF} must be much greater than the switching period:

Equation 5-18.

$$\frac{1}{f_{SW} \times \tau} = \frac{T}{\tau} < < 1$$

If the voltage divider resistors $R1$ and $R2$ are in the $k\Omega$ range, a C_{FF} of 1nF to 100nF can easily satisfy the large time constant requirements. Also, a 100nF injection capacitor C_{INJ} is used in order to be considered as short for a wide range of the frequencies.

The process of sizing the ripple injection resistor and capacitors is:

Step 1. Select C_{FF} to feed all output ripples into the feedback pin and make sure the large time constant assumption is satisfied. Typical choice of C_{FF} is 1nF to 100nF if $R1$ and $R2$ are in the $k\Omega$ range.

Step 2. Select R_{INJ} according to the expected feedback voltage ripple using the following equations.

Equation 5-19.

$$K_{DIV} = \frac{\Delta V_{FB(PP)}}{V_{IN}} \times \frac{f_{SW} \times \tau}{D \times (1 - D)}$$

Then the value of R_{INJ} is obtained using:

Equation 5-20.

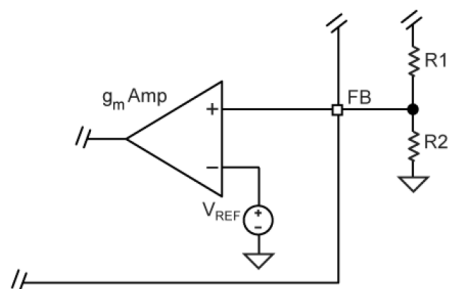
$$R_{INJ} = (R1 // R2) \times \left(\frac{1}{K_{DIV}} - 1 \right)$$

Step 3. Select C_{INJ} as 100nF, which could be considered as short for a wide range of the frequencies.

5.5. Setting Output Voltage

The MIC26400 requires two resistors to set the output voltage as shown in Figure 5-4.

Figure 5-4. Voltage Divider Configuration



The output voltage is determined by the following equation:

Equation 5-21.

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right)$$

Where:

$$V_{FB} = 0.8V$$

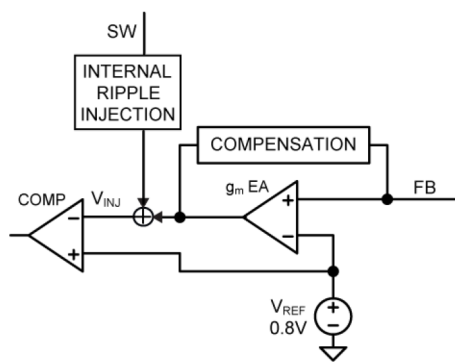
A typical value of R1 can be between 3kΩ and 10kΩ. If R1 is too large, it may allow noise to be introduced into the voltage feedback loop. If R1 is too small in value, it will decrease the efficiency of the power supply, especially at light loads. Once R1 is selected, R2 can be calculated using:

Equation 5-22.

$$R2 = \frac{V_{FB} \times R1}{V_{OUT} - V_{FB}}$$

In addition to the external ripple injection added at the FB pin, internal ripple injection is added at the inverting input of the comparator inside the MIC26400, as shown in Figure 5-5. The inverting input voltage V_{INJ} is clamped to 1.2V. As V_{OUT} is increased, the swing of V_{INJ} will be clamped. The clamped V_{INJ} reduces the line regulation because it is reflected back as a DC error on the FB terminal. Therefore, the maximum output voltage of the MIC26400 should be limited to 5.5V to avoid this line regulation problem.

Figure 5-5. Internal Ripple Injection



5.6. Thermal Measurements

Measuring the IC's case temperature is recommended to ensure it is within its operating limits. Although this might seem like a very elementary task, it is easy to get erroneous results. The most common mistake is to use the standard thermocouple that comes with a thermal meter. This thermocouple wire gauge is large, typically 22 gauge, and behaves like a heatsink, resulting in a lower case measurement.

Two methods of temperature measurement are using a smaller thermocouple wire or an infrared thermometer. If a thermocouple wire is used, it must be constructed of 36 gauge wire or higher (smaller wire size) to minimize the wire heat-sinking effect. In addition, the thermocouple tip must be covered in either thermal grease or thermal glue to ensure that the thermocouple junction makes good contact with the case of the IC.

Wherever possible, an infrared thermometer is recommended. An optional stand makes it easy to hold the beam on the IC for long periods of time.

6. PCB Layout Guidelines

PCB Layout is critical to achieve reliable, stable, and efficient performance. A ground plane is required to control EMI and minimize the inductance in power, signal, and return paths.

To minimize EMI and output noise, the following guidelines should be followed to ensure proper operation of the MIC26400 converter.

6.1. IC

- The 2.2 μ F ceramic capacitor, which is connected to the VDD pin, must be located right at the IC. The VDD pin is very noise sensitive and placement of the capacitor is critical. Use wide traces to connect to the VDD and PGND pins.
- The signal ground pin (SGND) must be connected directly to the ground planes. Do not route the SGND pin to the PGND pad on the top layer.
- Place the IC close to the point of load (POL).
- Use wide traces to route the input and output power lines.
- Signal and power grounds should be kept separate and connected at only one location.

6.2. Input Capacitor

- Place the input capacitors on the same side of the board and as close to the IC as possible.
- Keep both the PVIN and PGND connections short.
- Place several vias to the ground plane close to the input capacitor ground terminal.
- Use either X7R or X5R dielectric input capacitors. Do not use Y5V or Z5U type capacitors.
- Do not replace the ceramic input capacitor with any other type of capacitor. Any type of capacitor can be placed in parallel with the input capacitor.
- If a Tantalum input capacitor is placed in parallel with the input capacitor, it must be recommended for switching regulator applications and the operating voltage must be derated by 50%.
- In "Hot-Plug" applications, a Tantalum or Electrolytic bypass capacitor must be used to limit the overvoltage spike seen on the input supply when power is suddenly applied.

6.3. Inductor

- Keep the inductor connection to the switch node (SW) short.
- Do not route any digital lines underneath or close to the inductor.
- Keep the switch node (SW) away from the feedback (FB) pin.
- The CS pin should be connected directly to the SW pin to accurately sense the voltage across the low-side MOSFET.
- To minimize noise, place a ground plane underneath the inductor.

6.4. Output Capacitor

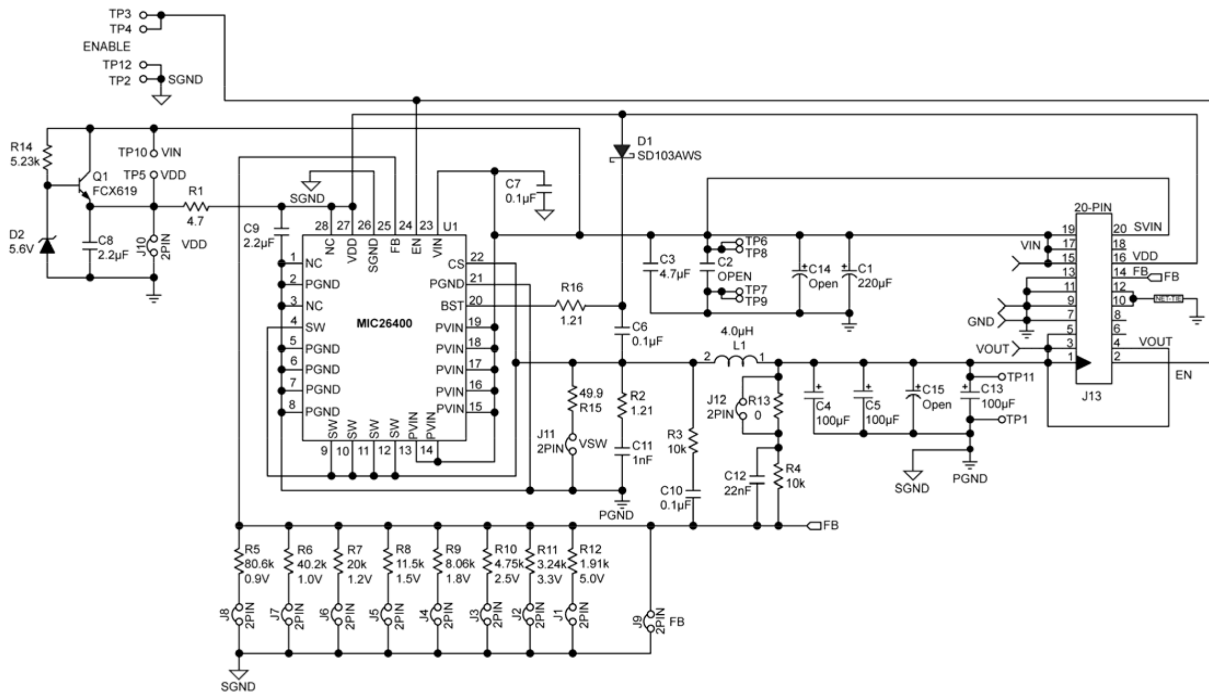
- Use a wide trace to connect the output capacitor ground terminal to the input capacitor ground terminal.
- The control loop performance may vary with changes in the output capacitor value and ESR. Contact the factory if the output capacitor differs from the components listed in the BOM.
- The feedback trace should be separate from the power trace and connected as close as possible to the output capacitor. Sensing a long, high current load trace can degrade the DC load regulation.

6.5. RC Snubber (Optional)

- Place the RC snubber on the same side of the board and as close to the SW pin as possible.

7. Evaluation Board Schematic

Figure 7-1. Schematic of MIC26400 Evaluation Board



Note: J13, R13, R15 are for testing purposes.

Table 7-1. Bill of Materials

Item	Part Number	Manufacturer	Description	Qty.
C1	B41125A7227M	EPCOS	220µF Aluminum Capacitor, SMD, 35V	1
C2	Open	—	—	—
C3	12105C475KAZ2A	AVX	4.7µF Ceramic Capacitor, X7R, Size 1210, 50V	1
C4, C5, C13	GRM32ER71H475KA88L	Murata	100µF Ceramic Capacitor, X5R, Size 1210, 6.3V	3
	12106D107MAT2A	AVX		
C6, C7, C10	GRM32ER60J107ME20L	Murata	0.1µF Ceramic Capacitor, X7R, Size 0603, 50V	3
	06035C104KAT2A	AVX		
	GRM188R71H104KA93D	Murata		
C8, C9	C1608X7R1H104K	TDK	2.2µF Ceramic Capacitor, X7R, Size 0805, 10V	2
	0805ZC225MAT2A	AVX		
	GRM21BR71A225KA01L	Murata		
C11	C2012X7R1A225K	TDK	1nF Ceramic Capacitor, X7R, Size 0603, 50V	1
	06035C102KAT2A	AVX		
	GRM188R71H102KA01D	Murata		
	C1608X7R1H102K	TDK		

Table 7-1. Bill of Materials (continued)

Item	Part Number	Manufacturer	Description	Qty.
C12	06035C223KAZ2A	AVX	22nF Ceramic Capacitor, X7R, Size 0603, 50V	1
	GRM188R71H223K	Murata		
	C1608X7R1H223K	TDK		
C14	Open	—	—	—
C15	Open	—	—	—
D1	SD103AWS-7	Diodes Inc.	Small Signal Schottky Diode	1
	SD103AWS	Vishay		
D2	CMDZ5L6	Central Semi	5.6V Zener Diode	1
L1	HCF1305-4R0-R	Cooper Bussmann	4.0μH Inductor, 12A Saturation Current	1
Q1	FCX619	ZETEX	50V NPN Transistor	1
R1	CRCW06034R75FKEA	Vishay Dale	4.75Ω Resistor, Size 0603, 1%	1
R2, R16	CRCW08051R21FKEA	Vishay Dale	1.21Ω Resistor, Size 0805, 1%	2
R3, R4	CRCW060310K0FKEA	Vishay Dale	10kΩ Resistor, Size 0603, 1%	2
R5	CRCW060380K6FKEA	Vishay Dale	80.6kΩ Resistor, Size 0603, 1%	1
R6	CRCW060340K2FKEA	Vishay Dale	40.2kΩ Resistor, Size 0603, 1%	1
R7	CRCW060320K0FKEA	Vishay Dale	20kΩ Resistor, Size 0603, 1%	1
R8	CRCW060311K5FKEA	Vishay Dale	11.5kΩ Resistor, Size 0603, 1%	1
R9	CRCW06038K06FKEA	Vishay Dale	8.06kΩ Resistor, Size 0603, 1%	1
R10	CRCW06034K75FKEA	Vishay Dale	4.75kΩ Resistor, Size 0603, 1%	1
R11	CRCW06033K24FKEA	Vishay Dale	3.24kΩ Resistor, Size 0603, 1%	1
R12	CRCW06031K91FKEA	Vishay Dale	1.91kΩ Resistor, Size 0603, 1%	1
R13	CRCW06030000FKEA	Vishay Dale	0Ω Resistor, Size 0603, 5%	1
R14	CRCW06035K23FKEA	Vishay Dale	5.23kΩ Resistor, Size 0603, 1%	1
R15	CRCW060349R9FKEA	Vishay Dale	49.9Ω Resistor, Size 0603, 1%	1
U1	MIC26400YJL	Microchip Technology Inc.	26V/5A Hyper Speed Control® Synchronous Buck DC/DC Regulator	1

8. PCB Layout

Figure 8-1. Evaluation Board Top Layer

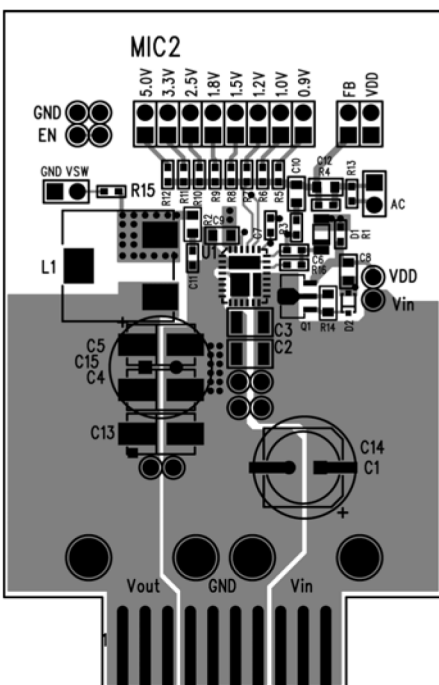


Figure 8-2. Evaluation Board Mid-Layer 1 (Ground Plane)

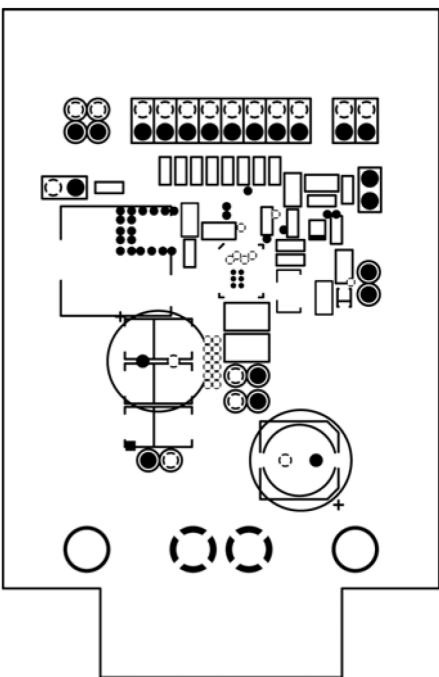


Figure 8-3. Evaluation Board Mid-Layer 2

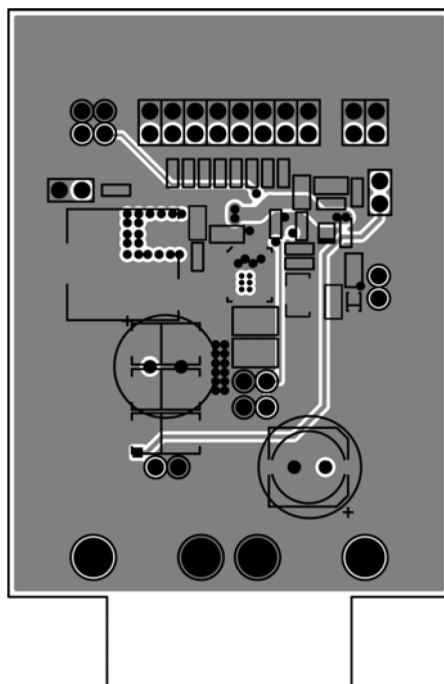
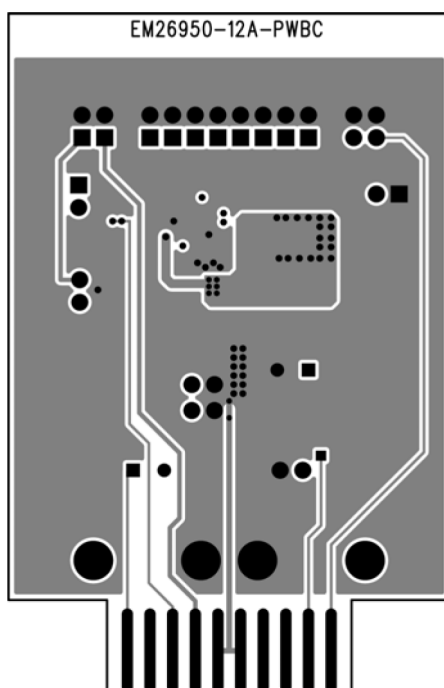


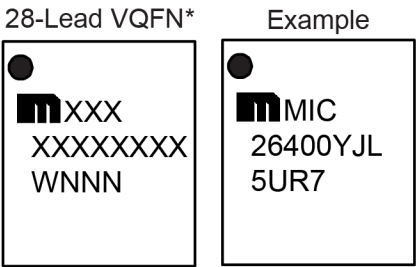
Figure 8-4. Evaluation Board Bottom Layer



9. Package Information

9.1. Package Marking Drawing

Figure 9-1. Package Marking Drawing



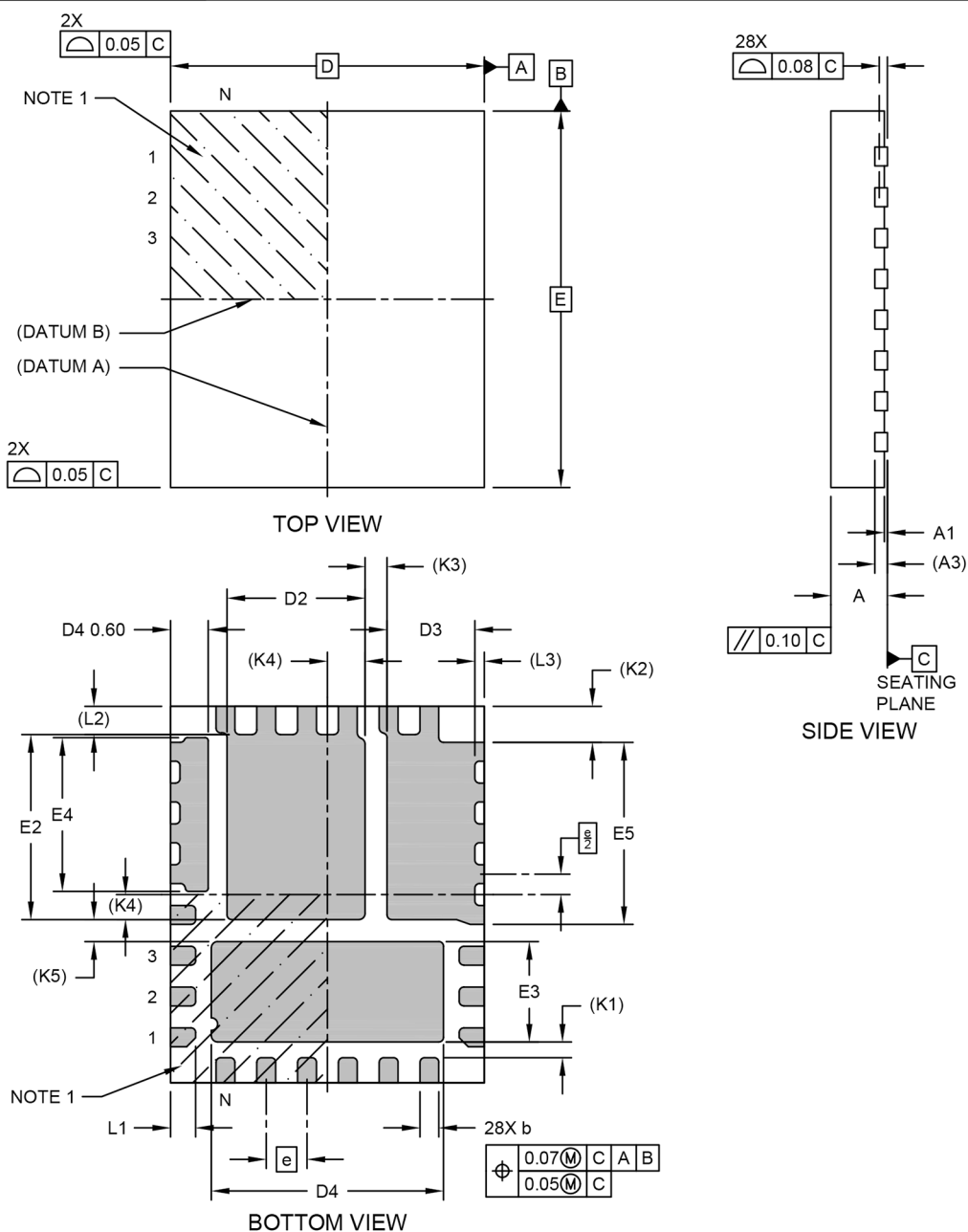
Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	•, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.	
	Underbar (_) and/or Overbar (¯) symbol may not be to scale.	

Note: If the full seven-character YYWWNNN code cannot fit on the package, the following truncated codes are used based on the available marking space: 6 Characters = YWWNNN; 5 Characters = WWNNN; 4 Characters = WNNN; 3 Characters = NNN; 2 Characters = NN; 1 Character = N

9.2. Package Outline Drawing

28-Lead Very Thin Plastic Quad Flat, No Lead Package (PKA) - 5x6x0.9 mm Body [VQFN] With Multiple Exposed Pads and Fused Terminals; Micrel Legacy QFN56-28LD-PL-1

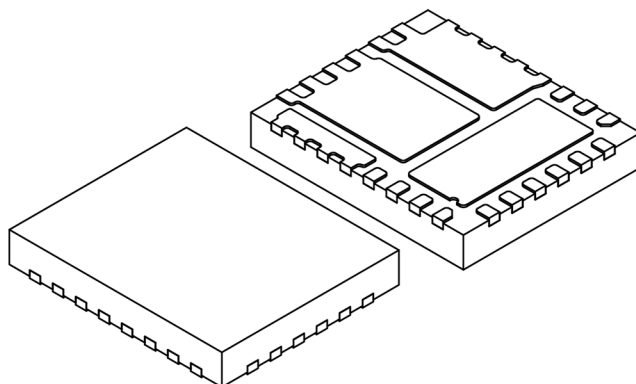
Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-01120 Rev B Sheet 1 of 2

**28-Lead Very Thin Plastic Quad Flat, No Lead Package (PKA) - 5x6x0.9 mm Body [VQFN]
With Multiple Exposed Pads and Fused Terminals; Micrel Legacy QFN56-28LD-PL-1**

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N	28		
Pitch	e	0.65 BSC		
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3	0.20 REF		
Overall Length	D	5.00 BSC		
Exposed Pad Length	D2	2.15	2.20	2.25
Exposed Pad Length	D3	1.35	1.40	1.45
Exposed Pad Length	D4	3.65	3.70	3.75
Overall Width	E	6.00 BSC		
Exposed Pad Width	E2	2.90	2.95	3.00
Exposed Pad Width	E3	1.575	1.60	1.625
Exposed Pad Width	E4	2.40	2.45	2.50
Exposed Pad Width	E5	2.85	2.90	2.95
Terminal Width	b	0.25	0.30	0.35
Terminal Length	L1	0.35	0.40	0.45
Terminal Length	L2	0.45 REF		
Terminal Length	L3	0.15 REF		
Terminal to Exposed Pad	K1	0.25 REF		
Body Edge to Exposed Pad	K2	0.575 REF		
Exposed Pad to Exposed Pad	K3	0.035 REF		
Exposed Pad Offset	K4	0.40 REF		
Exposed Pad to Exposed Pad	K5	0.35 REF		

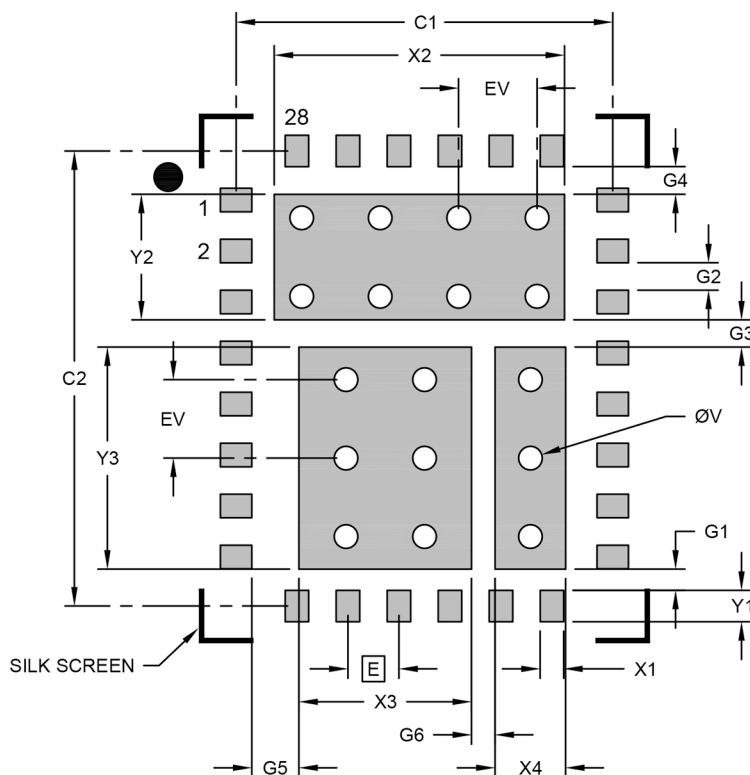
Notes:

1. The Pin 1 visual index feature may vary, but it must be located within the hatched area.
2. The package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. The theoretically exact value is shown without tolerances.
REF: Reference Dimension, usually without tolerance, is for information purposes only.

Microchip Technology Drawing C04-01120 Rev B Sheet 2 of 2

**28-Lead Very Thin Plastic Quad Flat, No Lead Package (PKA) - 5x6x0.9 mm Body [VQFN]
With Multiple Exposed Pads and Fused Terminals; Micrel Legacy QFN56-28LD-PL-1**

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS			Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC			Contact Pad Spacing	C2		5.80	
Center Pad Width	X2			3.70	Contact Pad to Center Pad	G1	0.12		
Center Pad Width	X3			2.20	Contact Pad to Contact Pad	G2	0.35		
Center Pad Width	X4			0.90	Center Pad to Center Pad	G3	0.35		
Center Pad Length	Y2			1.60	Contact Pad to Center Pad	G4	0.35		
Center Pad Length	Y3			2.83	Contact Pad to Center Pad	G5	0.60		
Contact Pad Width	X1			0.30	Center Pad to Center Pad	G6	0.13		
Contact Pad Length	Y1			0.40	Thermal Via Diameter	V		0.30	
Contact Pad Spacing	C1		4.80		Thermal Via Pitch	EV		1.00	

Notes:

- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. The theoretically exact value is shown without tolerances.
- For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during the reflow process.

Microchip Technology Drawing C04-03120 Rev B

10. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision	Date	Section	Description
DS20007156A	06/2026	—	Converted Micrel document MIC26400 to Microchip data sheet DS20007156A. Minor text changes throughout.

11. Product Identification System

PART NO.	X	XX	-XX
Device	Junction Temperature Range	Package	Media Type
Device:	MIC26400: 5A Hyper Speed Control® Synchronous DC/DC Buck Regulator		
Junction Temperature Range:	Y = -40°C to +125°C		
Package:	JL = 28-Lead 5mm x 6mm VQFN		
Media Type:	TR = 1,000/Reel		

Example:

- MIC26400YJL-TR: MIC26400, -40°C to +125°C Temperature Range, 28-Lead 5mm x 6mm VQFN, 1,000/Reel

Note:

Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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