

32-Channel Serial to Parallel Converter With High Voltage Push-Pull Outputs

HV9708 Obsolete Device



Description

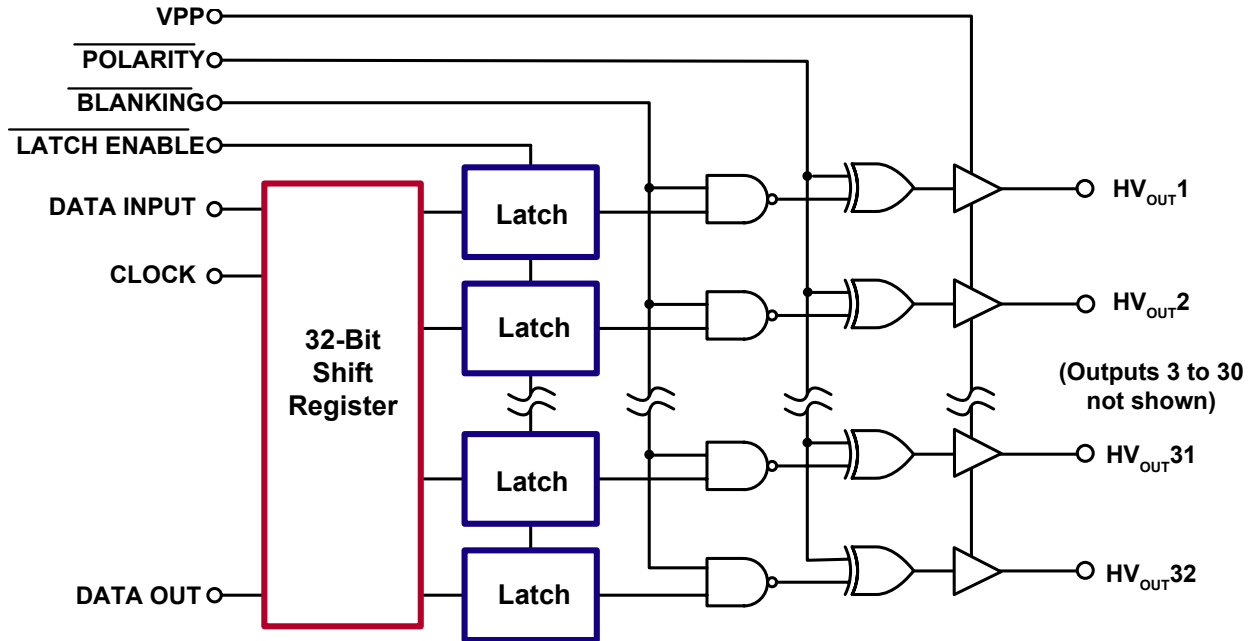
The HV9708 is a low voltage serial to high voltage parallel converters with push-pull outputs. This device has been designed for use as a driver for AC-electroluminescent displays. It can also be used in any application requiring multiple output, high voltage current sourcing and sinking capabilities such as driving plasma panels, vacuum fluorescent, or large matrix LCD displays. The inputs are fully CMOS compatible.

This device consists of a 32-bit shift register, 32 latches, and control logic to perform the polarity select and blanking of the outputs. HV_{OUT1} is connected to the first stage of the shift register through the polarity and blanking logic. Data is shifted through the shift register on the logic low to high transition of the clock. The HV9708 shifts data in the clockwise direction when viewed from the top of the package. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register (HV_{OUT32}). Operation of the shift register is not affected by the $\overline{LE}$ (latch enable), $\overline{BE}$ (blanking), or the $\overline{PE}$ (polarity) in-puts. Transfer of data from the shift register to the latch occurs when the $\overline{LE}$ (latch enable) input is high. The data in the latch is stored when $\overline{LE}$ is low.

Features

- Processed with HVCMOS® Technology
- Output Voltages up to 80V
- Low Power Level Shifting
- Shift Register Speed 8.0 MHz
- Latched Data Outputs
- 5.0V CMOS Compatible Inputs
- Forward and Reverse Shifting Options
- Diode to V_{PP} Allows Efficient Power Recovery

Block Diagram



1. Pin Configuration

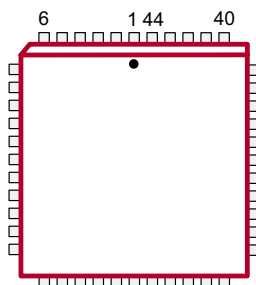
Pin	Function	Function
1	HV _{OUT} 17	High voltage outputs. High voltage push-pull outputs, which, depending on controlling low voltage data, can drive loads either to a GND, or to V _{PP} rail levels.
2	HV _{OUT} 16	
3	HV _{OUT} 15	
4	HV _{OUT} 14	
5	HV _{OUT} 13	
6	HV _{OUT} 12	
7	HV _{OUT} 11	
8	HV _{OUT} 10	
9	HV _{OUT} 9	
10	HV _{OUT} 8	
11	HV _{OUT} 7	
12	HV _{OUT} 6	
13	HV _{OUT} 5	
14	HV _{OUT} 4	
15	HV _{OUT} 3	
16	HV _{OUT} 2	
17	HV _{OUT} 1	
18	Data Out	Serial data output Data output for cascading to the data input of the next device.
19	N/C	No connect.
20	N/C	
21	Polarity	
22	CLK	Data shift register clock. Inputs are shifted into the shift register on the positive edge of the clock.
23	GND	Logic and high voltage ground.
24	VPP	High voltage power rail.
25	VDD	Low voltage logic power rail.
26	Latch Enable	Latch enable input. When $\overline{LE}$ is high, shift register data is transferred into a data latch. When $\overline{LE}$ is low, data is latched, and new data can be clocked into the shift register.
27	Data In	Serial data input. Data needs to be present before each rising edge of the clock.
28	Blanking	
29	N/C	No connect.

Pin Configuration (continued)

Pin	Function	Function
30	HV _{OUT} 32	High voltage outputs. High voltage push-pull outputs, which, depending on controlling low voltage data, can drive loads either to a GND, or to V _{PP} rail levels.
31	HV _{OUT} 31	
32	HV _{OUT} 30	
33	HV _{OUT} 29	
34	HV _{OUT} 28	
35	HV _{OUT} 27	
36	HV _{OUT} 26	
37	HV _{OUT} 25	
38	HV _{OUT} 24	
39	HV _{OUT} 23	
40	HV _{OUT} 22	
41	HV _{OUT} 21	
42	HV _{OUT} 20	
43	HV _{OUT} 19	
44	HV _{OUT} 18	

Package Type

44-Lead PLCC



2. Electrical Characteristics

2.1. Absolute Maximum Ratings

Parameter	Value
Supply Voltage, V_{DD}	-0.5V to +7.0V
Supply Voltage, V_{PP}	-0.5V to +90V
Logic Input Levels	-0.5V to $V_{DD}+0.5V$
Ground Current ¹	1.5A
Continuous Total Power Dissipation ²	1200 mW
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Notes:	
1. Duty cycle is limited by the total power dissipated in the package.	
2. For operation above 25°C ambient derate linearly to maximum operating temperature at 20 mW/°C.	

Note: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions, beyond those indicated in the operational sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2.2. Recommended Operating Conditions

Parameter	Sym	Min	Max	Units
Logic Voltage Supply	V_{DD}	4.5	5.5	V
High Voltage Supply	V_{PP}	8.0	80	V
Input High Voltage	V_{IH}	$V_{DD} - 0.5$	V_{DD}	V
Input Low Voltage	V_{IL}	0	0.5	V
Clock Frequency	f_{CLK}	0	8.0	MHz
Operating Free-air Temperature Range	T_A	-40	+85	°C

2.3. DC Characteristics

Electrical Specifications: $V_{PP} = 60V$, $V_{DD} = 5.0V$, $T_A = 25^\circ C$, unless otherwise specified.					
Parameter	Sym	Min	Max	Units	Conditions
V_{PP} Supply Current	I_{PP}	—	100	μA	HV _{OUTPUTS} High to Low
I_{DD} Supply Current (Quiescent)	I_{DDQ}	—	100	μA	All Inputs = V_{DD} or GND
I_{DD} Supply Current (Operating)	I_{DD}	—	15	mA	$V_{DD} = V_{DDmax}$, $f_{CLK} = 8.0$ MHz
Shift Register Output Voltage	$V_{OH(Data)}$	$V_{DD} - 0.5$	—	V	$I_O = -100 \mu A$
Shift Register Output Voltage	$V_{OL(Data)}$	—	0.5	V	$I_O = 100 \mu A$
Current Leakage, Any Input	I_{IH}	—	1.0	μA	Input = V_{DD}
Current Leakage, Any Input	I_{IL}	—	-1.0	μA	Input = GND
HV Output Clamp Diode Voltage	V_{OC}	—	-1.5	V	$I_{OC} = -5.0$ mA
HV Output When Sourcing	V_{OH}	52	—	V	$I_{OH} = -20$ mA, 0 to 70°C
HV Output When Sinking	V_{OL}	—	4.0	V	$I_{OL} = 5.0$ mA, 0 to 70°C

2.4. AC Characteristics

Electrical Specifications: $V_{PP} = 60V$, $V_{DD} = 5.0V$, $T_A = 25^\circ C$, unless otherwise specified.					
Parameter	Sym	Min	Max	Units	Conditions
Clock Frequency	f_{CLK}	—	8.0	MHz	
Clock Width, High or Low	t_{WL} or t_{WH}	62	—	ns	
Setup Time Before CLK Rises	t_{SU}	25	—	ns	
Hold Time After CLK Rises	t_H	10	—	ns	
Data Output Delay After L to H CLK	$t_{DLH}(\text{Data})$	—	110	ns	CL = 15 pF
Data Output Delay After H to L CLK	$t_{DHL}(\text{Data})$	—	110	ns	CL = 15 pF
$\overline{LE}$ Delay After L to H CLK	t_{DLE}	50	—	ns	
Width of $\overline{LE}$ Pulse	t_{WLE}	50	—	ns	
$\overline{LE}$ Setup Time Before L to H CLK	t_{SLE}	50	—	ns	
Delay From $\overline{LE}$ to HV_{OUT} , L to H	t_{ON}	—	500	ns	
Delay From $\overline{LE}$ to HV_{OUT} , H to L	t_{OFF}	—	500	ns	

2.5. Thermal Characteristics

Package	θ_{ja}
44-Lead PLCC	$37^\circ C/W$

3. Functional Description

Power-Up Sequence

1. Connect ground.
2. Apply V_{DD} .
3. Set all inputs (Data, CLK, Enable, etc.) to a known state.
4. Apply V_{PP} .

Power-down sequence should be the reverse of the above.

Note: The V_{PP} should not drop below V_{DD} during operations.

Figure 3-1. Input and Output Equivalent Circuits

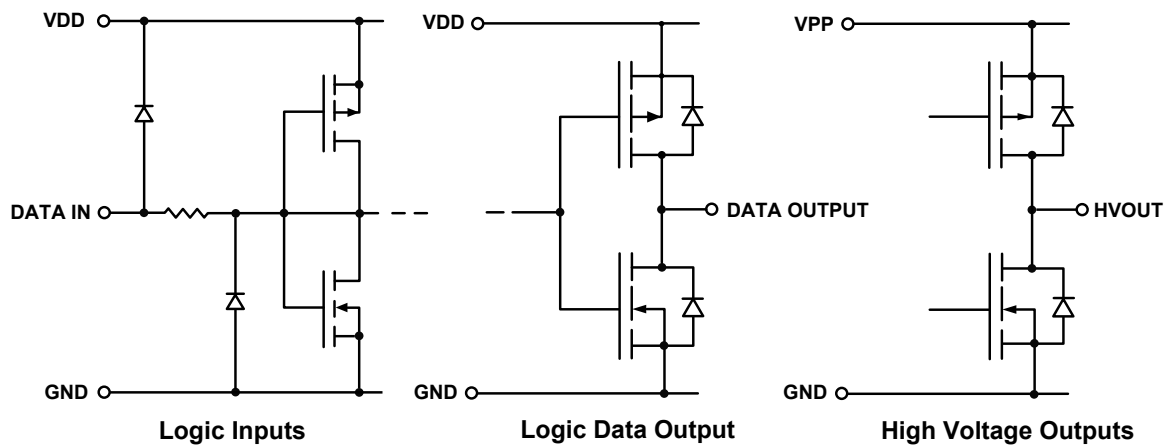


Figure 3-2. Switching Waveforms

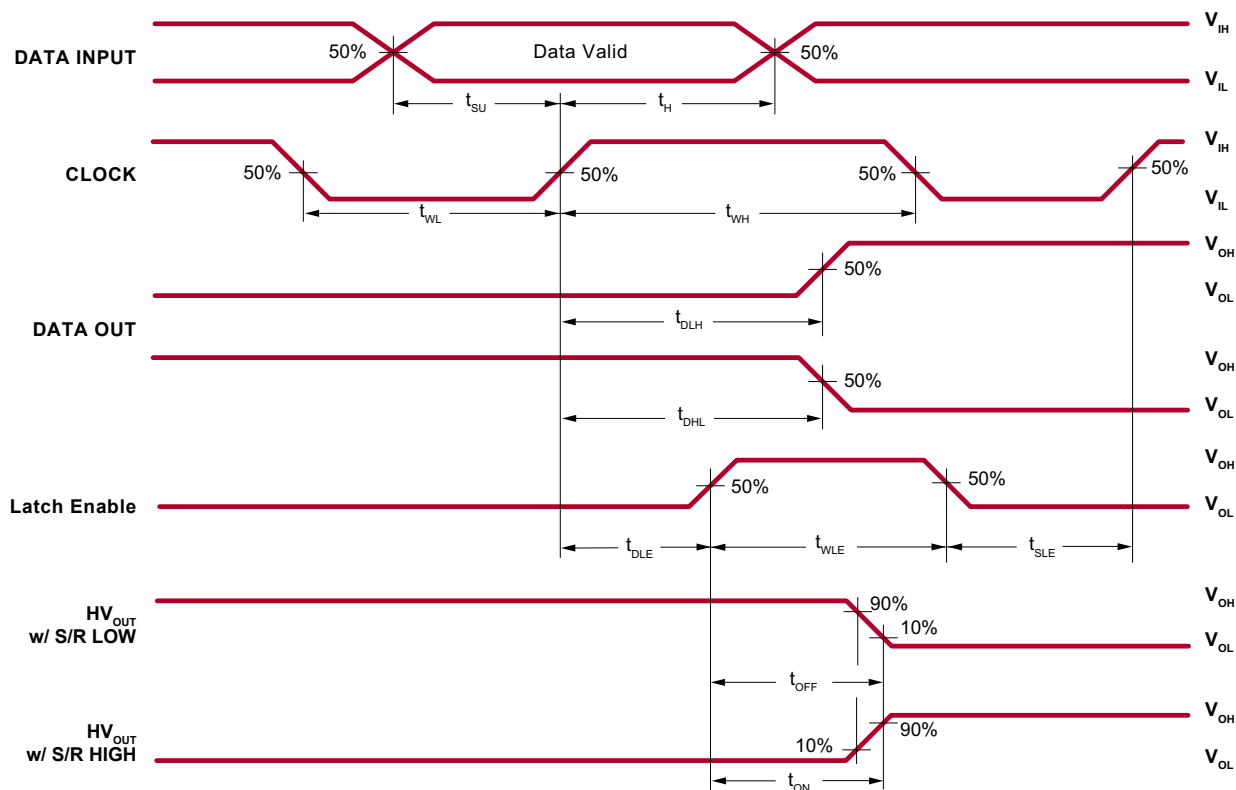


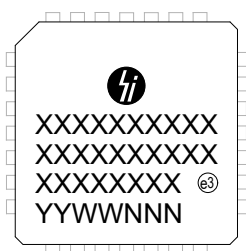
Table 3-1. Function Table

Function	Inputs					Outputs		
	Data	CLK	$\overline{LE}$	$\overline{BL}$	$\overline{POL}$	Shift Reg 1 2...8	HV Outputs 1 2...8	Data Out •
All on	X	X	X	L	L	• •...•	H H...H	•
All off	X	X	X	L	H	• •...•	L L...L	•
Invert Mode	X	X	L	H	L	• •...•	$\overline{• •...•}$	•
Load S/R	H OR L	↑	L	H	H	H or L •...•	• •...•	•
Load Latches	X	X	↑	H	H	• •...•	• •...•	•
	X	X	↑	H	L	• •...•	$\overline{• •...•}$	•
Transparent Latch Mode	L	↑	H	H	H	L •...•	L •...•	•
	H	↑	H	H	H	H •...•	H •...•	•

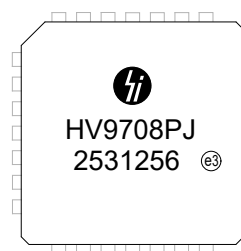
Note: H= high level, L = low level, X = irrelevant, ↑ = low-to-high transition, • = dependent on previous stage's state before the last CLK or last $\overline{LE}$ high.

4. Packaging Information

44-Lead PLCC



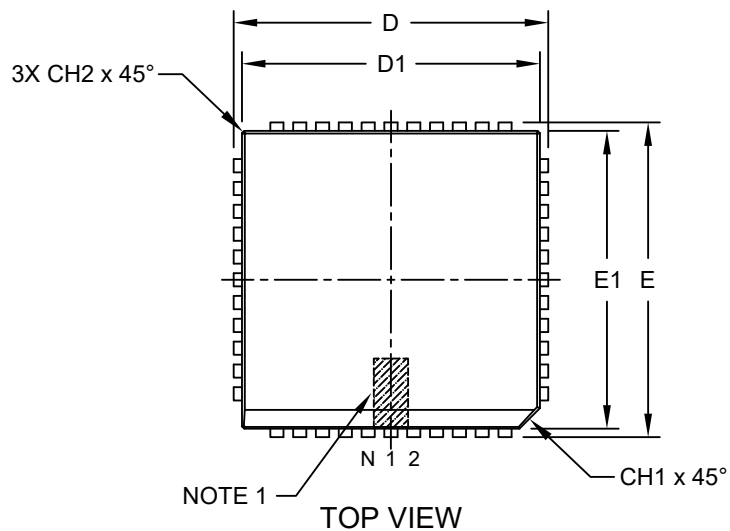
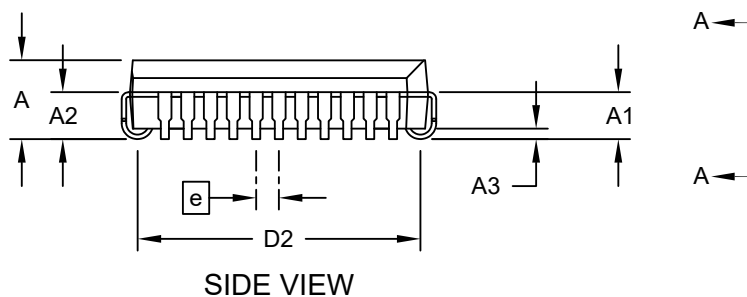
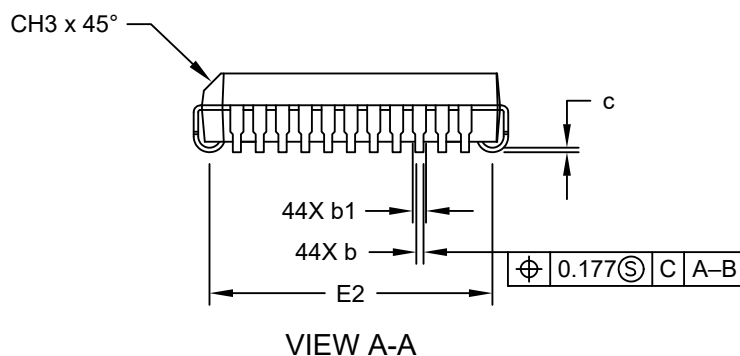
Example



Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or not include the corporate logo.		

44-Lead Plastic Leaded Chip Carrier (T2X) - Square [PLCC]

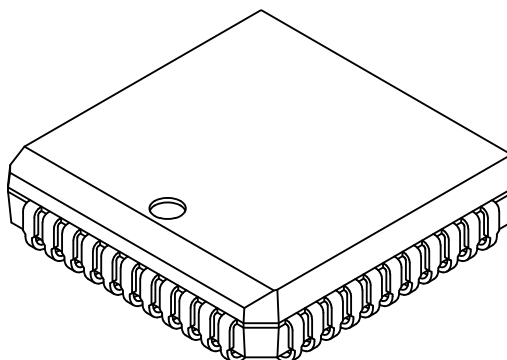
Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-048-T2X Rev D Sheet 1 of 2

44-Lead Plastic Leaded Chip Carrier (T2X) - Square [PLCC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		INCHES			MILLIMETERS'		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	N	44			44		
Pitch	e	.050			1.27		
Overall Height	A	.165	.172	.180	4.19	4.37	4.57
Contact Height	A1	.090	.105	.120	2.29	2.67	3.05
Molded Package to Contact	A2	.062	-	.083	1.57	-	2.11
Standoff §	A3	.020	-	-	0.51	-	-
Corner Chamfer	CH1	.042	-	.048	1.07	-	1.22
Chamfers	CH2	-	-	.020	-	-	0.51
Side Chamfer	CH3	.042	-	.056	1.07	-	1.42
Overall Width	E	.685	.690	.695	17.40	17.53	17.65
Overall Length	D	.685	.690	.695	17.40	17.53	17.65
Molded Package Width	E1	.650	.653	.656	16.51	16.59	16.66
Molded Package Length	D1	.650	.653	.656	16.51	16.59	16.66
Footprint Width	E2	.582	.610	.638	14.78	15.49	16.21
Footprint Length	D2	.582	.610	.638	14.78	15.49	16.21
Lead Thickness	c	.0075	-	.0125	0.19	-	0.32
Upper Lead Width	b1	.026	-	.032	0.66	-	0.81
Lower Lead Width	b	.013	-	.021	0.33	-	0.53

Notes:

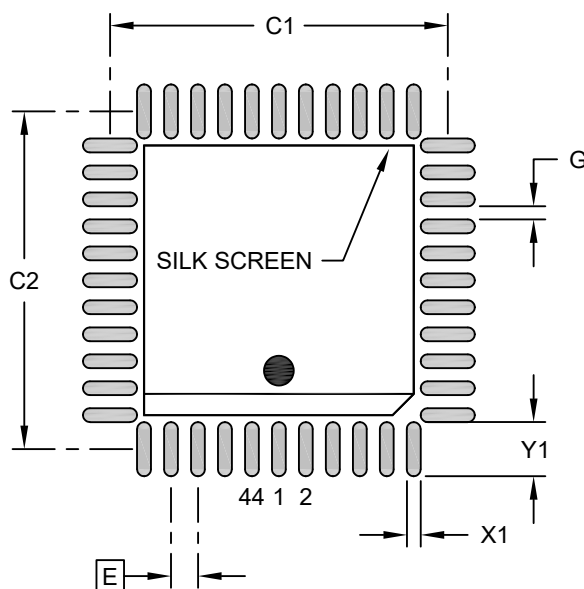
- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic
- Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005" per side.
- Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-048-T2X Rev D Sheet 2 of 2

44-Lead Plastic Leaded Chip Carrier (T2X) - Square [PLCC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		.050 BSC	
Contact Pad Spacing	C1		.626	
Contact Pad Spacing	C2		.626	
Contact Pad Width (X44)	X1			.026
Contact Pad Length (X44)	Y1			.100
Contact Pad to Center Pad (X40)	G	.008		

Notes:

- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
- For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2048-T2X Rev D

5. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision	Date	Section	Description
A	09/2025		Initial Revision

6. Product Identification System

To order or obtain information, for example, on pricing or delivery, contact Microchip: <https://www.microchip.com/en-us/about/contact-us>.

<u>PART NO.</u>	<u>XX</u>	<u>-X</u>	<u>XXX</u>
Device	Package	PB Free	Tape & Reel
Device:	HV9708		
Package:	PJ		= 44-Lead PLCC Package
PB Free	G		(Pb)-free / RoHS compliant package
Tape & Reel Option:	Blank		= 27/Tube

Examples:

- HV9708PJ-G: 44-Lead PLCC, Tube

Notes:

1. Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.
2. Small form-factor packaging options may be available. Please check www.microchip.com/packaging for small-form factor package availability, or contact your local Sales Office.

Microchip Information

Trademarks

The “Microchip” name and logo, the “M” logo, and other names, logos, and brands are registered and unregistered trademarks of Microchip Technology Incorporated or its affiliates and/or subsidiaries in the United States and/or other countries (“Microchip Trademarks”). Information regarding Microchip Trademarks can be found at <https://www.microchip.com/en-us/about/legal-information/microchip-trademarks>.

ISBN: 979-8-3371-2076-8

Legal Notice

This publication and the information herein may be used only with Microchip products, including to design, test, and integrate Microchip products with your application. Use of this information in any other manner violates these terms. Information regarding device applications is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. Contact your local Microchip sales office for additional support or, obtain additional support at www.microchip.com/en-us/support/design-help/client-support-services.

THIS INFORMATION IS PROVIDED BY MICROCHIP “AS IS”. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTIES OF NON-INFRINGEMENT, MERCHANTABILITY, AND FITNESS FOR A PARTICULAR PURPOSE, OR WARRANTIES RELATED TO ITS CONDITION, QUALITY, OR PERFORMANCE.

IN NO EVENT WILL MICROCHIP BE LIABLE FOR ANY INDIRECT, SPECIAL, PUNITIVE, INCIDENTAL, OR CONSEQUENTIAL LOSS, DAMAGE, COST, OR EXPENSE OF ANY KIND WHATSOEVER RELATED TO THE INFORMATION OR ITS USE, HOWEVER CAUSED, EVEN IF MICROCHIP HAS BEEN ADVISED OF THE POSSIBILITY OR THE DAMAGES ARE FORESEEABLE. TO THE FULLEST EXTENT ALLOWED BY LAW, MICROCHIP’S TOTAL LIABILITY ON ALL CLAIMS IN ANY WAY RELATED TO THE INFORMATION OR ITS USE WILL NOT EXCEED THE AMOUNT OF FEES, IF ANY, THAT YOU HAVE PAID DIRECTLY TO MICROCHIP FOR THE INFORMATION.

Use of Microchip devices in life support and/or safety applications is entirely at the buyer’s risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Microchip Devices Code Protection Feature

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
- Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip products are strictly prohibited and may violate the Digital Millennium Copyright Act.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is “unbreakable”. Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.