

Product Overview

ICP1137 is a 2-stage MMIC power amplifier in bare die form, fabricated using GaN on SiC technology. ICP1137 operates from 2 GHz – 18 GHz with 37 dBm output power, 20% PAE, and 18 dB small signal gain. ICP1137 is well suited to commercial, test and measurement, and defense applications.

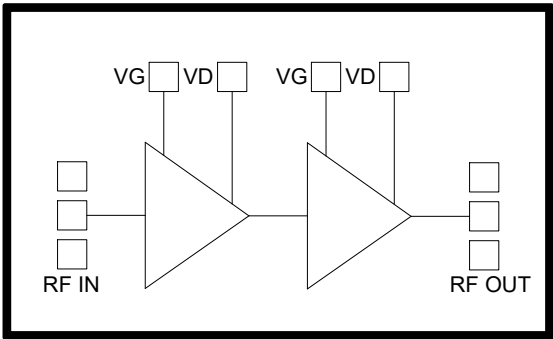
Key Features

- Frequency range: 2 GHz – 18 GHz
- P_{out} : 37 dBm at 26 dBm P_{in}
- PAE: 20%
- Small signal gain: 18 dB
- Bias: $V_D = 24V$, $I_{DQ} = 114\text{ mA}$
- Technology: GaN on SiC
- Lead-free and RoHS compliant
- Chip dimensions: 4.7 mm × 3.0 mm

Applications

- Test and measurement
- Aerospace and defense

Functional Block Diagram



Electrical Specifications

Parameter	Min.	Typ.	Max.	Units	Conditions ¹
Frequency	2		18	GHz	
Output power at P_{sat}	36.3	37		dBm	$P_{in} = 26\text{ dBm}$
Gain	10.3	11		dB	$P_{in} = 26\text{ dBm}$
Power added efficiency, PAE at P_{sat}	15	20		%	$P_{in} = 26\text{ dBm}$
Drain current at P_{sat}		1100	1200	mA	$P_{in} = 26\text{ dBm}$
Small signal gain, S_{21}		18		dB	
Input return loss		12		dB	
Output return loss		10		dB	
Drain voltage		24		V	

(1) Test Conditions unless otherwise stated: $V_D = 24V$, $I_{DQ} = 114\text{ mA}$, $T_A = 25\text{ }^{\circ}\text{C}$, CW

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1. Electrical Specification

1.1. Absolute Maximum Ratings

Parameter	Absolute Maximum
Drain voltage (V_D)	30V
Gate voltage (V_G)	-5V to 0V
Gate current (I_G)	25 mA
Drain current (CW) $T_A=25^{\circ}\text{C}$	2.4A
Power dissipation (CW) $T_A = 25^{\circ}\text{C}$	71.4W
Power dissipation (CW) $T_A = 85^{\circ}\text{C}$	54.0W
CW input power 50Ω, $T_A = 25^{\circ}\text{C}$	+26 dBm
Channel temperature	275 °C
Storage temperature	-65 °C to +150 °C
Input power VSWR (2:1) $V_D = 20\text{V}$, $I_{DQ} = 114\text{ mA}$ $V_D = 24\text{V}$, $I_{DQ} = 114\text{ mA}$	+27 dBm
Eutectic die attach temperature (30s)	320 °C

Note:

Exceeding any one or combination of these limits may cause permanent damage to this device. Microchip Technology Inc. does not recommend sustained operation near these survivability limits.

1.2. Thermal and Reliability

Parameter	Value
Thermal resistance	3.5 °C/W

Note:

- Assumes silver-sintered epoxy attach (15 μm thick) mounted on CuMo carrier.
- Base temperature is assumed at the top of the CuMo carrier.
- Thermal resistance calculated using IR measurement of the channel temperature.

1.3. Ordering and Handling

Ordering Information

For additional ordering information, contact your Microchip sales representative.

Part Number	Description
ICP1137-1-110I	Bare die in Gel-Pak trays
EV19A69A	Evaluation board development tool for ICP1137-1-110I

Handling Recommendations

Integrated circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

1.4. Small Signal Performance

Test conditions unless otherwise stated: $V_D = 18V - 24V$, $I_{DQ} = 114\text{ mA}$, $T_A = 25\text{ }^{\circ}\text{C}$

Figure 1-1. Input Return Loss vs. Frequency

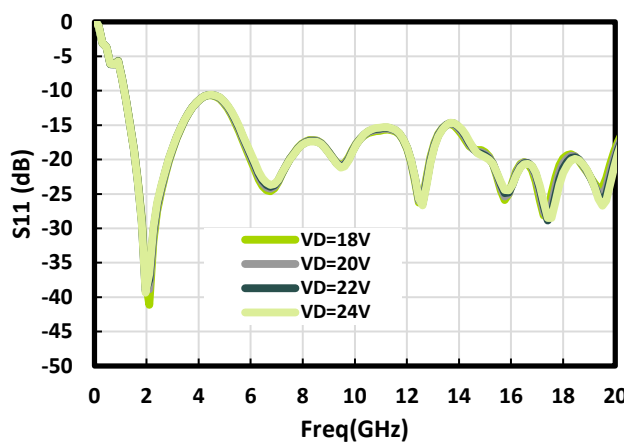


Figure 1-2. Output Return Loss vs. Frequency

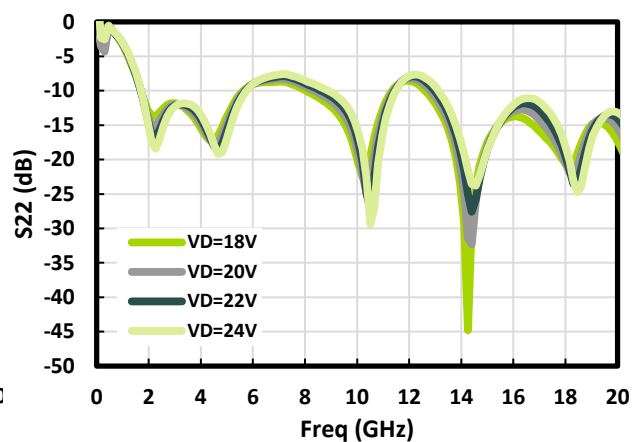


Figure 1-3. Gain vs. Frequency

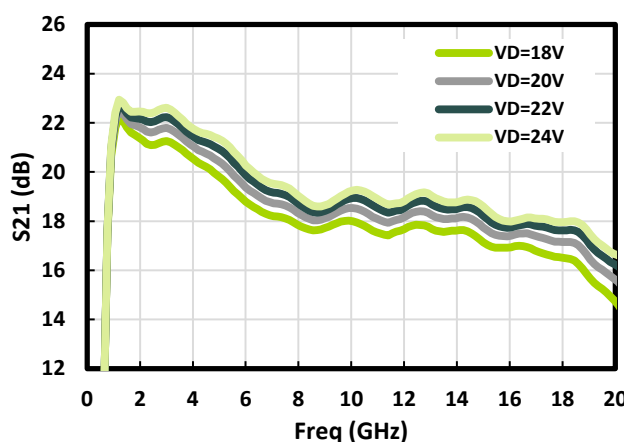
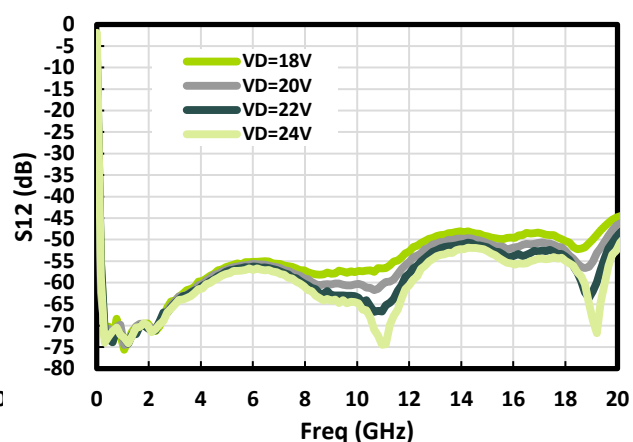


Figure 1-4. Reverse Isolation vs. Frequency



1.5. Large Signal Performance

Typical Power Data

Test conditions: $V_D = 24V$, $I_{DQ} = 114\text{ mA}$, $T_A = 25\text{ }^\circ\text{C}$, CW

Figure 1-5. P_{out} vs. Frequency

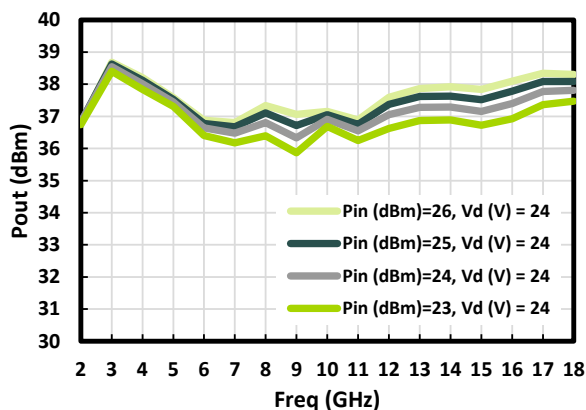


Figure 1-6. Gain vs. Frequency

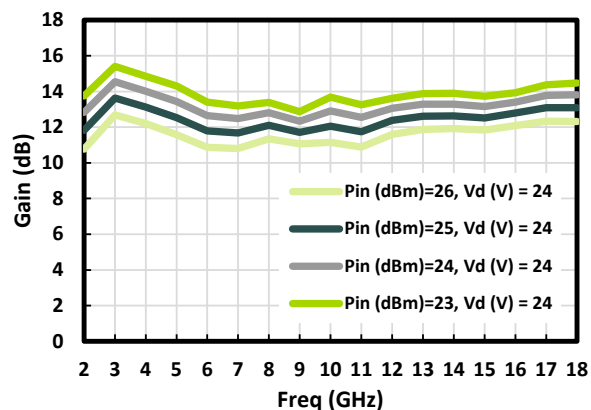


Figure 1-7. PAE vs. Frequency

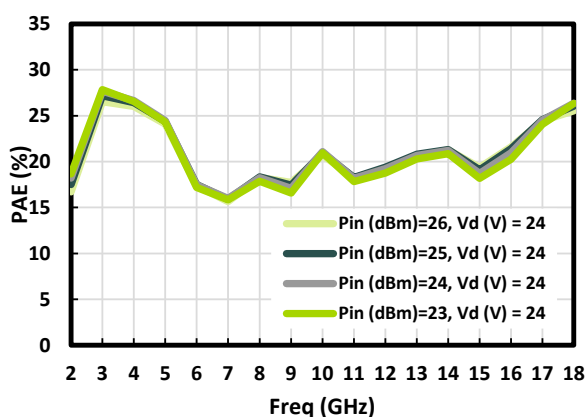
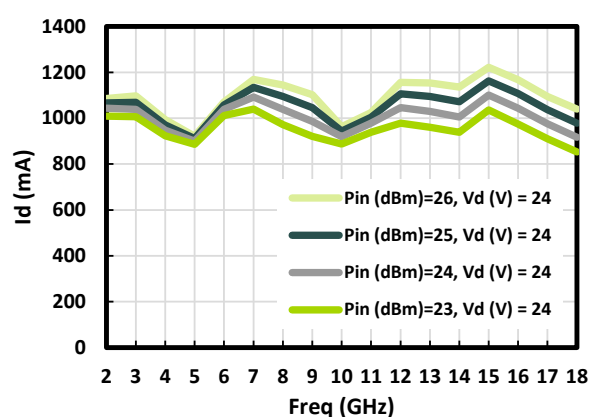


Figure 1-8. I_d vs. Frequency



Typical Power Data

Test conditions: $V_D = 20V$, $I_{DQ} = 114 \text{ mA}$, $T_A = 25^\circ\text{C}$, CW

Figure 1-9. P_{out} vs. Frequency

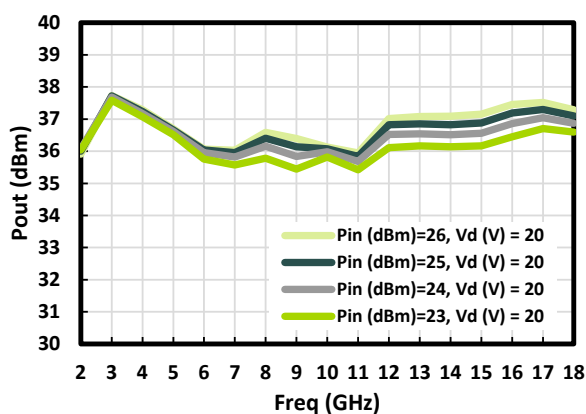


Figure 1-10. Gain vs. Frequency

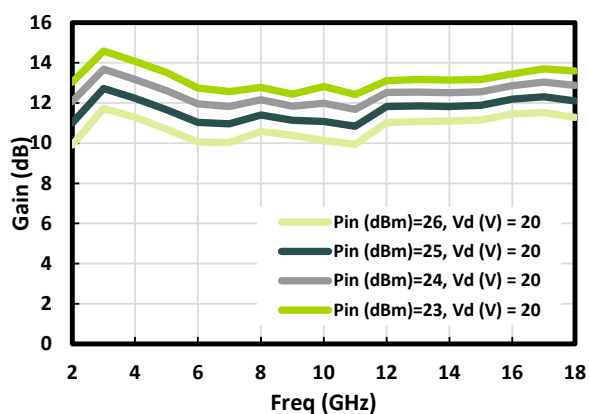


Figure 1-11. PAE vs. Frequency

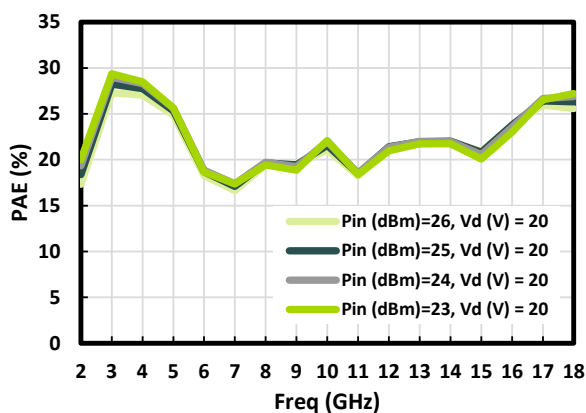
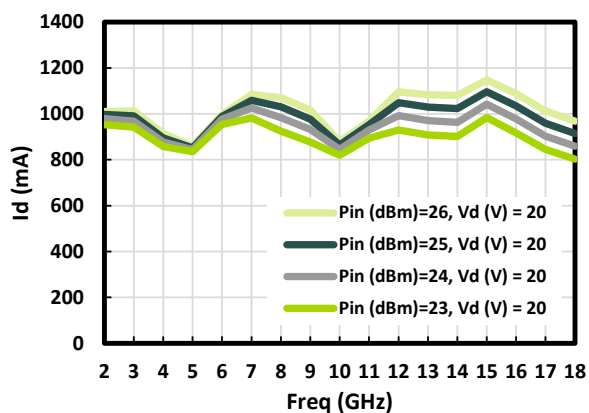


Figure 1-12. I_d vs. Frequency



Typical Power Data

Test conditions: $V_D = 24V$, $I_{DQ} = 114\text{ mA}$, $T_A = 25\text{ }^{\circ}\text{C}$, CW

Figure 1-13. P_{out} vs. P_{in}

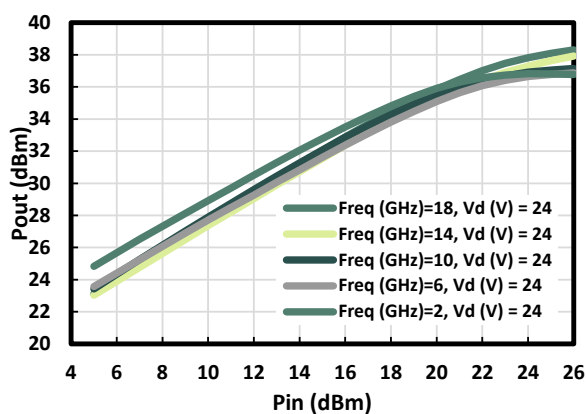


Figure 1-14. Gain vs. P_{in}

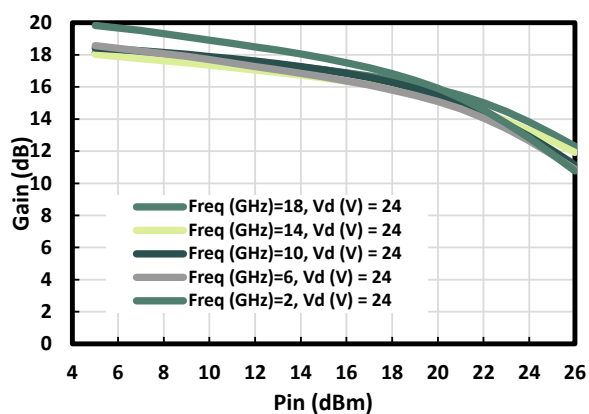


Figure 1-15. PAE vs. P_{in}

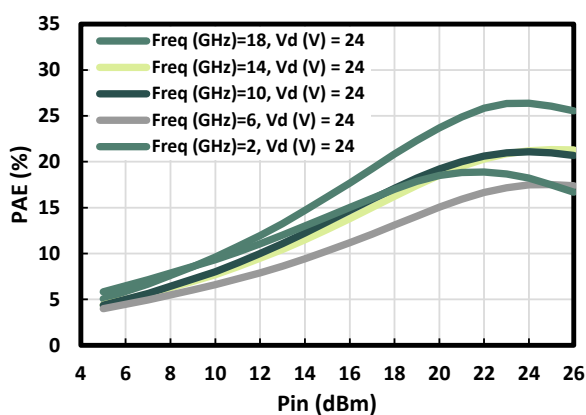
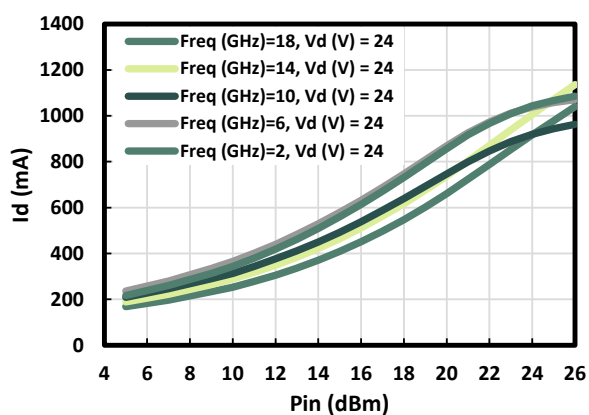


Figure 1-16. I_d vs. P_{in}



Typical Power Data

Test conditions: $V_D = 18V - 24V$, $I_{DQ} = 114\text{ mA}$, $T_A = 25^\circ\text{C}$, CW

Figure 1-17. P_{out} vs. Frequency

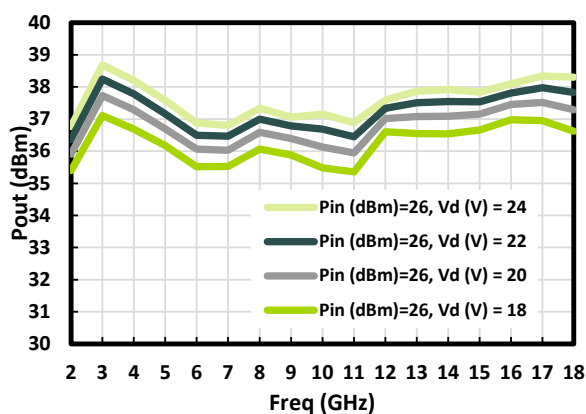


Figure 1-18. Gain vs. Frequency

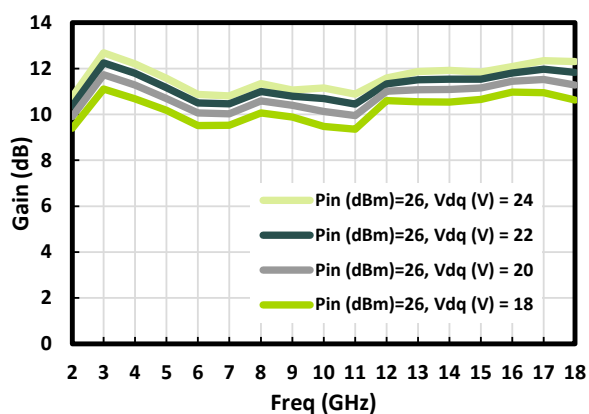


Figure 1-19. PAE vs. Frequency

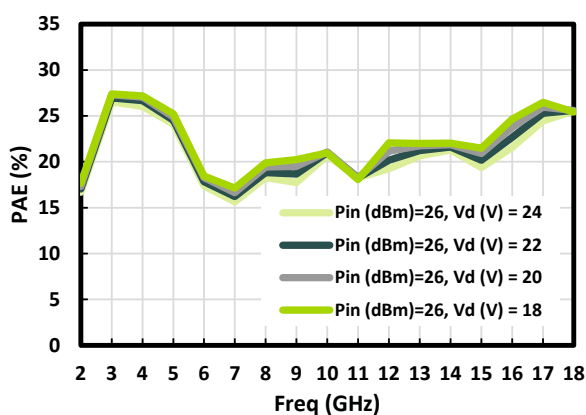
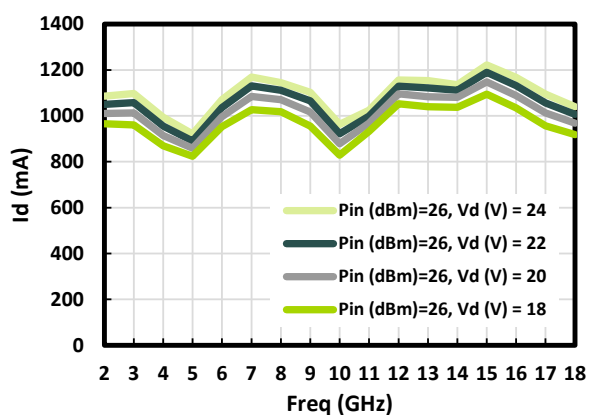


Figure 1-20. I_d vs. Frequency



Typical Power Data

Test conditions: $V_D = 24V$, $I_{DQ} = 114 \text{ mA}$, $T_A = -40^\circ\text{C}$, 25°C , 85°C , CW

Figure 1-21. P_{out} vs. Frequency

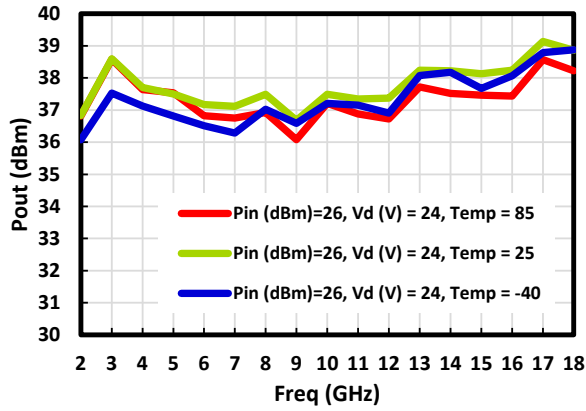


Figure 1-22. Gain vs. Frequency

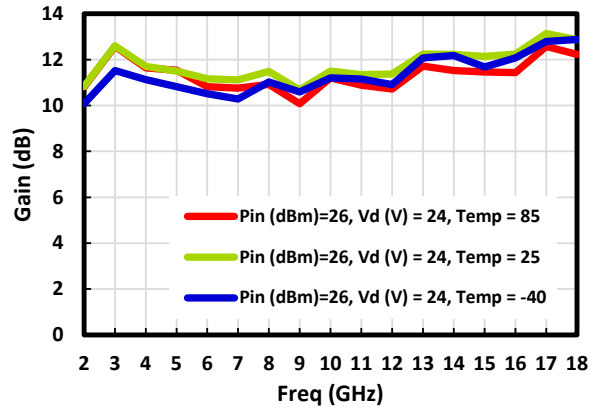


Figure 1-23. PAE vs. Frequency

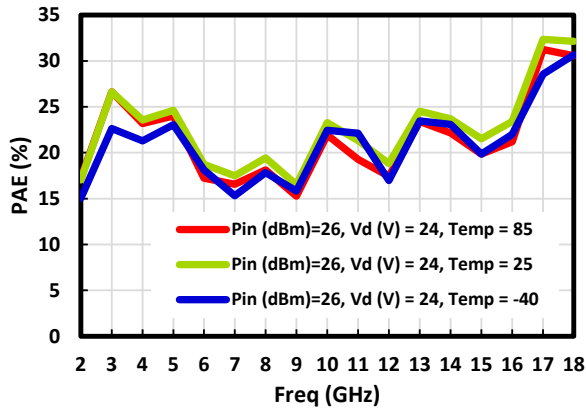
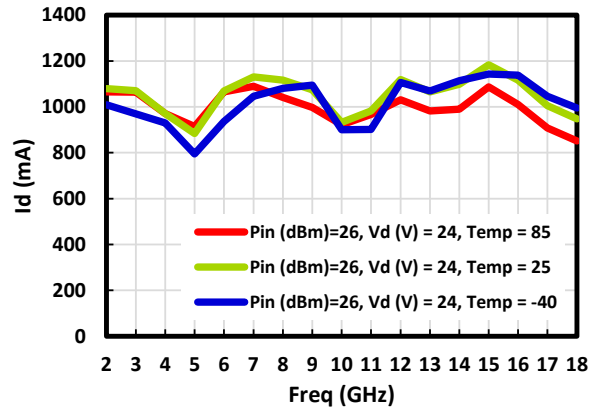


Figure 1-24. I_d vs. Frequency



Typical Power Data

Test conditions: $V_D = 24V$, $I_{DQ} = 114\text{ mA}$, $T_A = -40\text{ }^{\circ}\text{C}$, $25\text{ }^{\circ}\text{C}$, $85\text{ }^{\circ}\text{C}$, CW

Figure 1-25. P_{out} vs. P_{in} 2 GHz

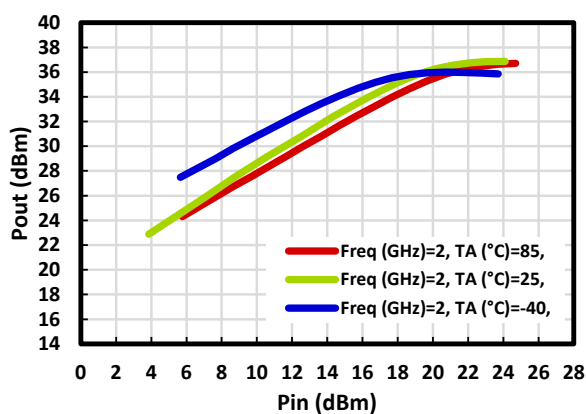


Figure 1-26. Gain vs. P_{in} 2 GHz

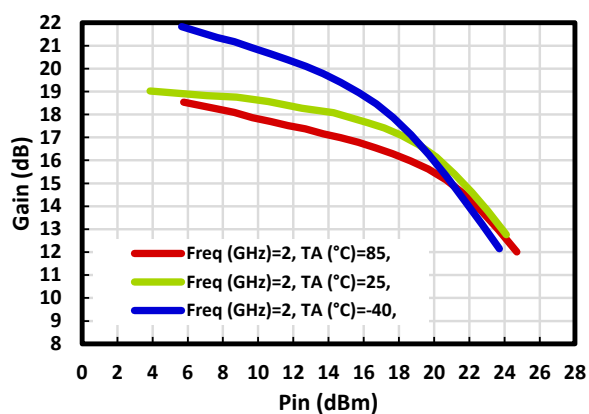


Figure 1-27. P_{out} vs. P_{in} 12 GHz

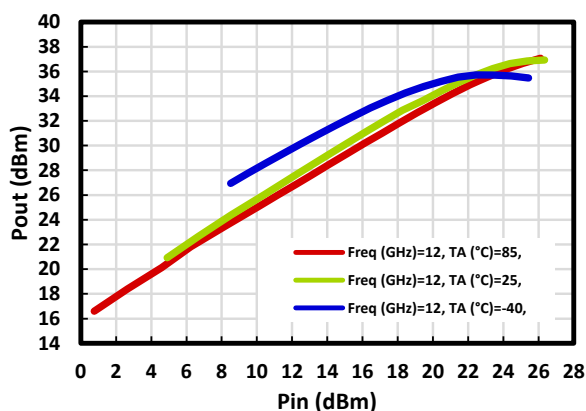


Figure 1-28. Gain vs. P_{in} 12 GHz

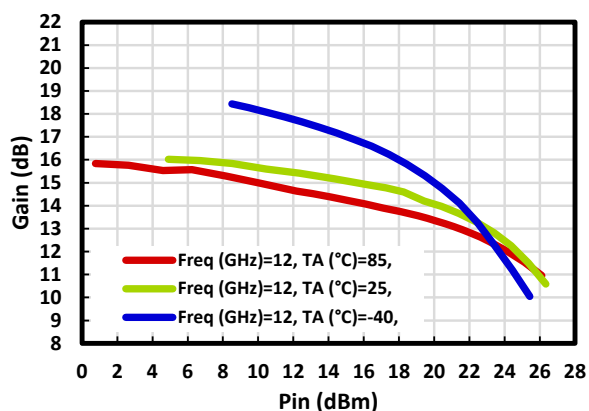


Figure 1-29. P_{out} vs. P_{in} 18 GHz

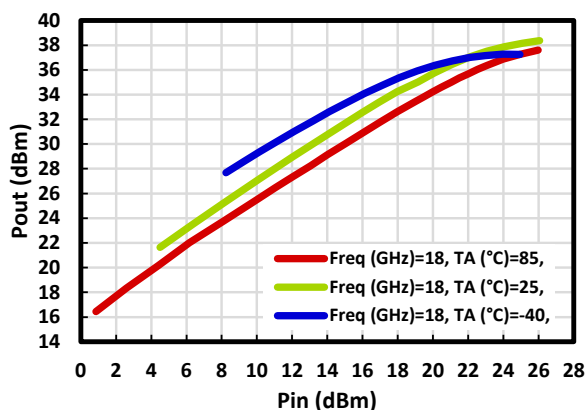
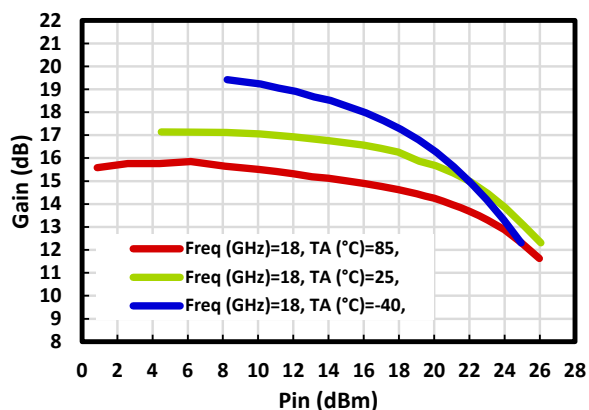


Figure 1-30. Gain vs. P_{in} 18 GHz



Typical Power Data

Test conditions: $V_D = 24V$, $I_{DQ} = 114\text{ mA}$, $T_A = -40\text{ }^{\circ}\text{C}$, $25\text{ }^{\circ}\text{C}$, $85\text{ }^{\circ}\text{C}$, CW

Figure 1-31. PAE vs. P_{in} 2 GHz

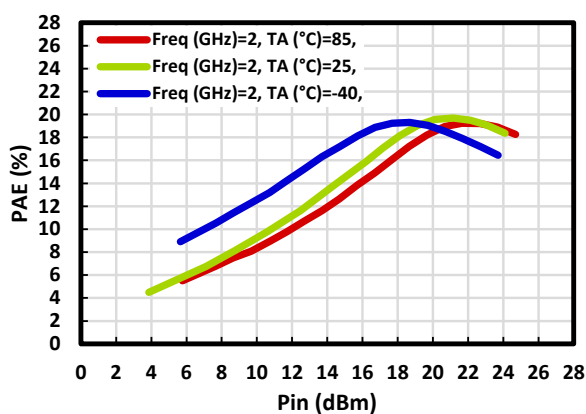


Figure 1-32. I_d vs. P_{in} 2 GHz

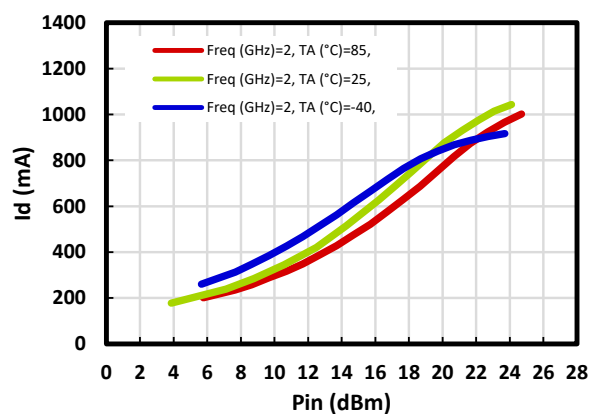


Figure 1-33. PAE vs. P_{in} 12 GHz

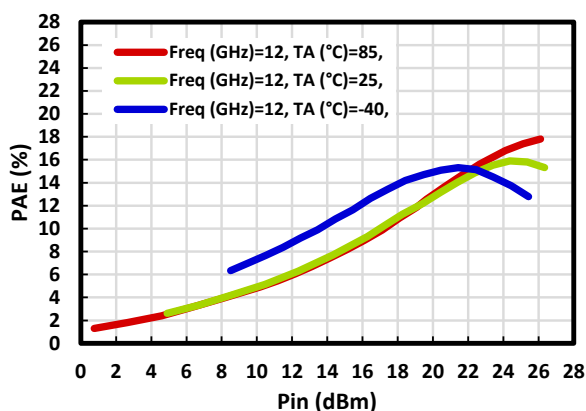


Figure 1-34. I_d vs. P_{in} 12 GHz

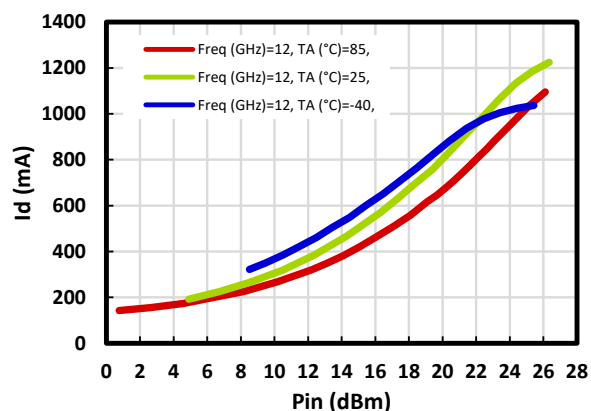


Figure 1-35. PAE vs. P_{in} 18 GHz

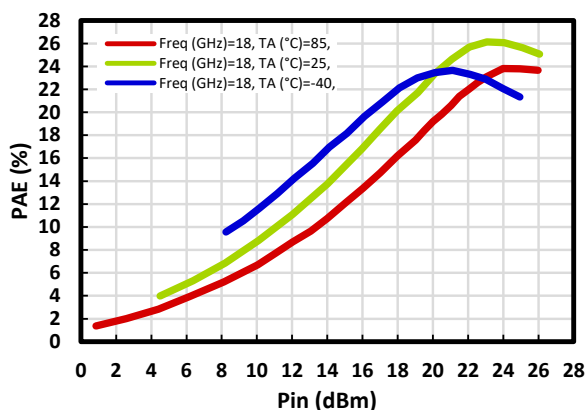
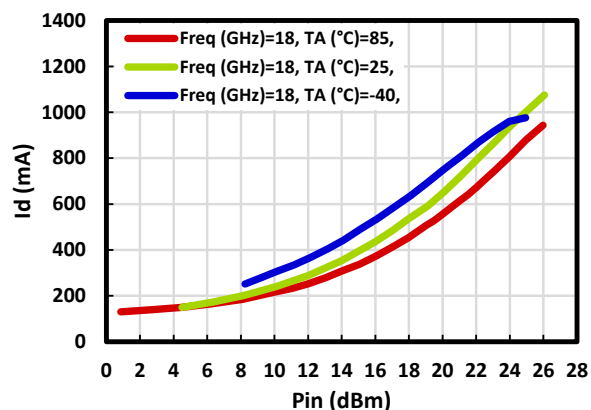


Figure 1-36. I_d vs. P_{in} 18 GHz



Typical Data

Test conditions: $V_D = 20V$, $I_{DQ} = 114 \text{ mA}$, $T_A = -40^\circ\text{C}$, 25°C , 85°C , CW

Figure 1-37. P_{out} vs. Frequency

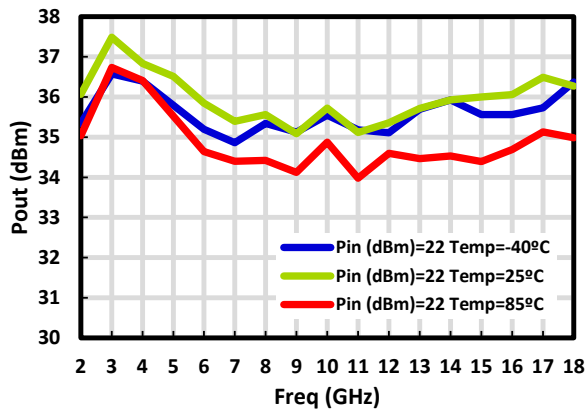


Figure 1-38. Gain vs. Frequency

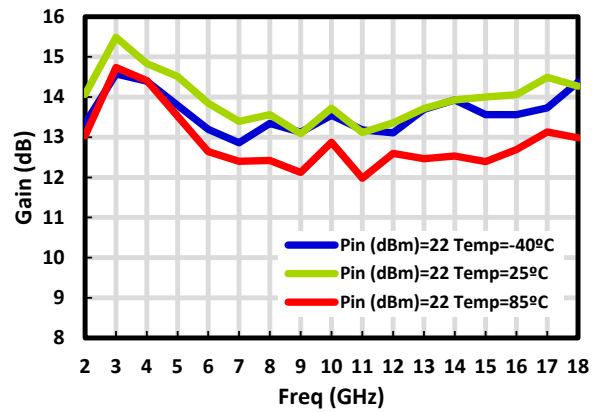


Figure 1-39. PAE vs. Frequency

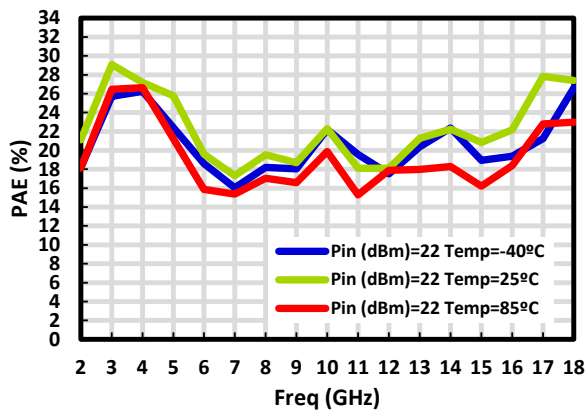
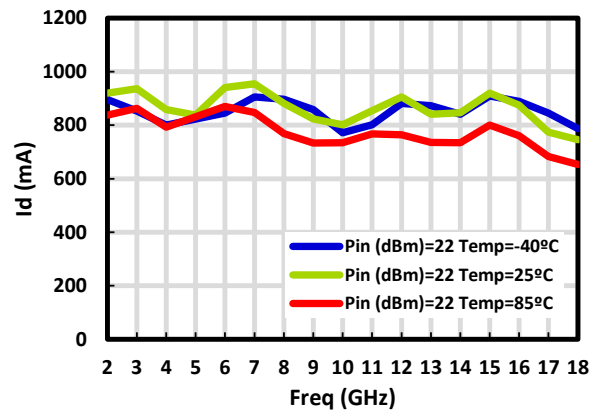


Figure 1-40. I_d vs. Frequency



Typical Data

Test conditions: $V_D = 20V$, $I_{DQ} = 114\text{ mA}$, $T_A = -40\text{ }^{\circ}\text{C}$, $25\text{ }^{\circ}\text{C}$, $85\text{ }^{\circ}\text{C}$, CW

Figure 1-41. P_{out} vs. P_{in} 2 GHz

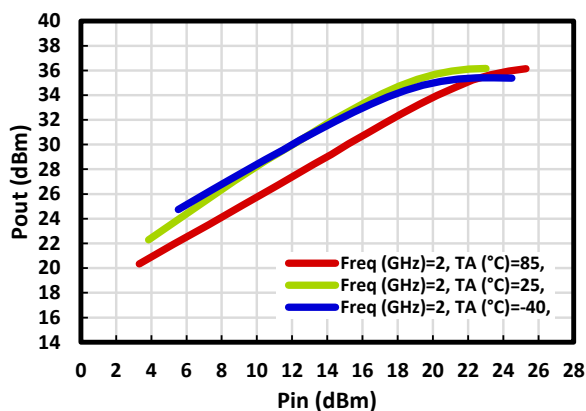


Figure 1-42. Gain vs. P_{in} 2 GHz

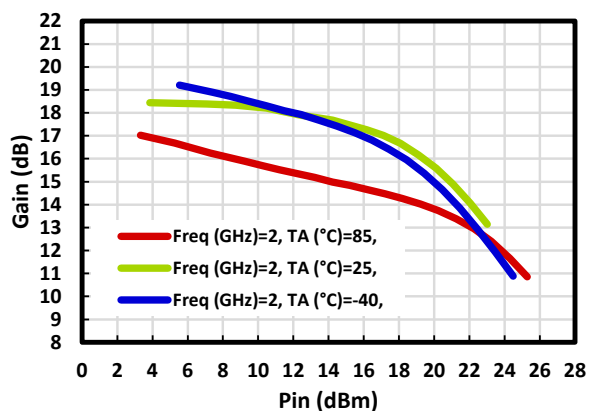


Figure 1-43. P_{out} vs. P_{in} 12 GHz

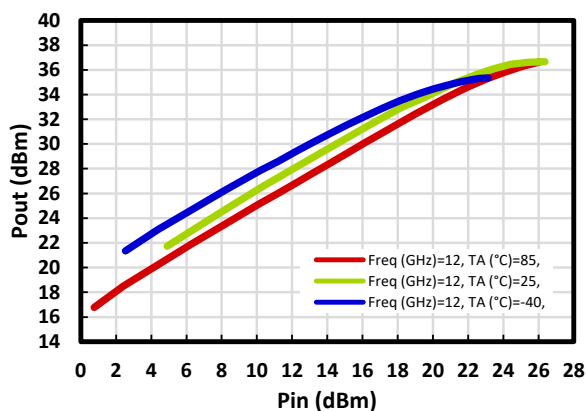


Figure 1-44. Gain vs. P_{in} 12 GHz

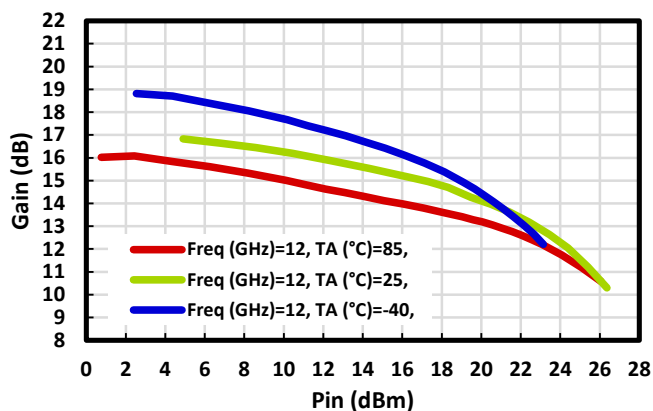


Figure 1-45. P_{out} vs. P_{in} 18 GHz

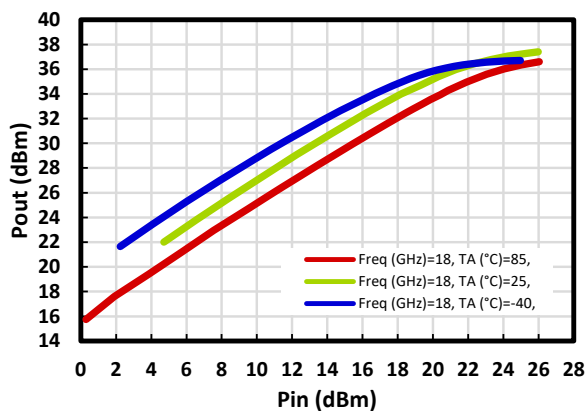
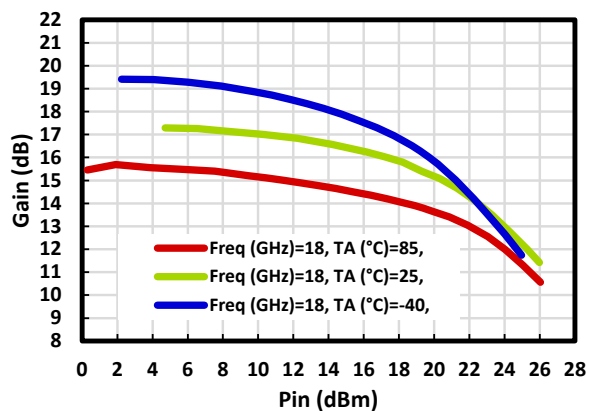


Figure 1-46. Gain vs. P_{in} 18 GHz



Typical Data

Test conditions: $V_D = 20V$, $I_{DQ} = 114\text{ mA}$, $T_A = -40\text{ }^{\circ}\text{C}$, $25\text{ }^{\circ}\text{C}$, $85\text{ }^{\circ}\text{C}$, CW

Figure 1-47. PAE vs. P_{in} 2 GHz

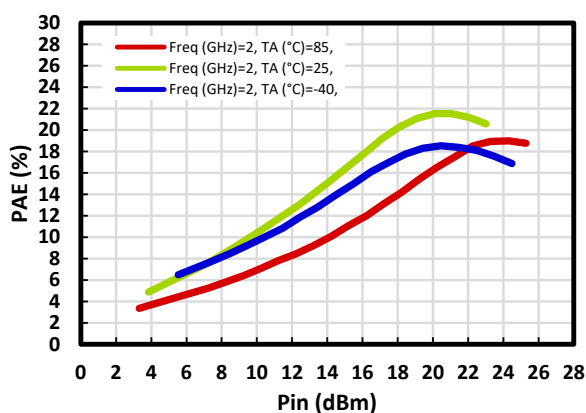


Figure 1-48. I_d vs. P_{in} 2 GHz

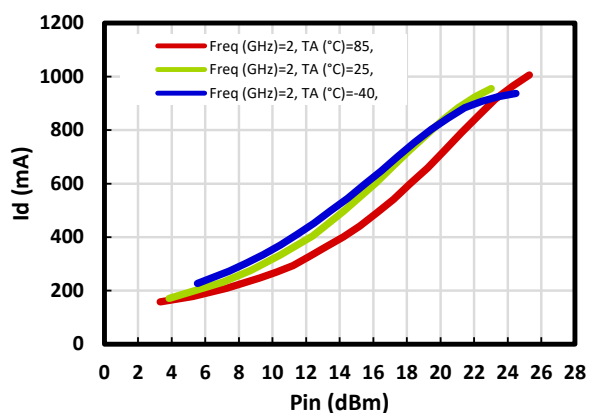


Figure 1-49. PAE vs. P_{in} 12 GHz

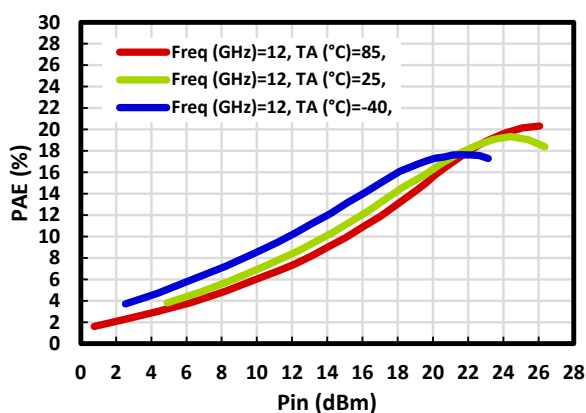


Figure 1-50. I_d vs. P_{in} 12 GHz

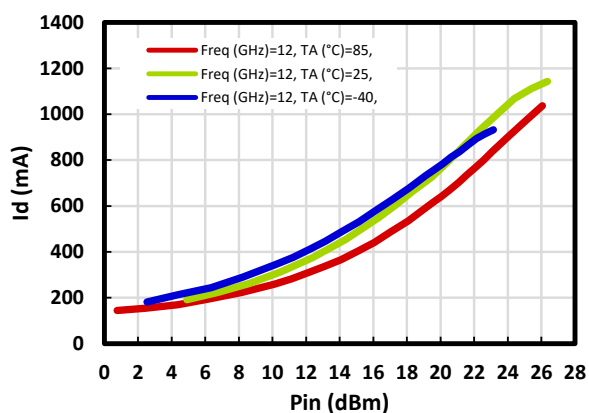


Figure 1-51. PAE vs. P_{in} 18 GHz

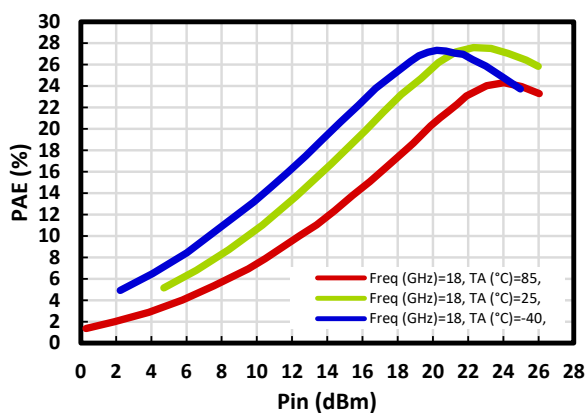
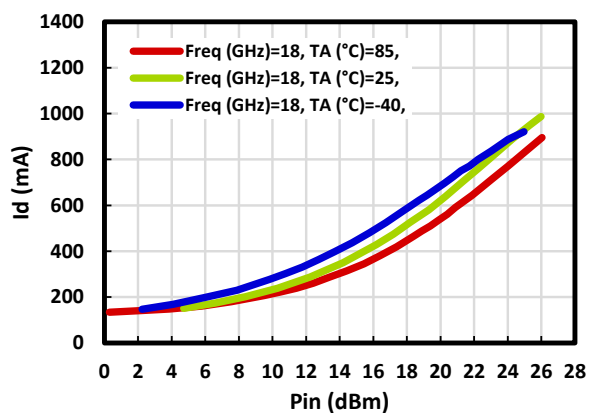
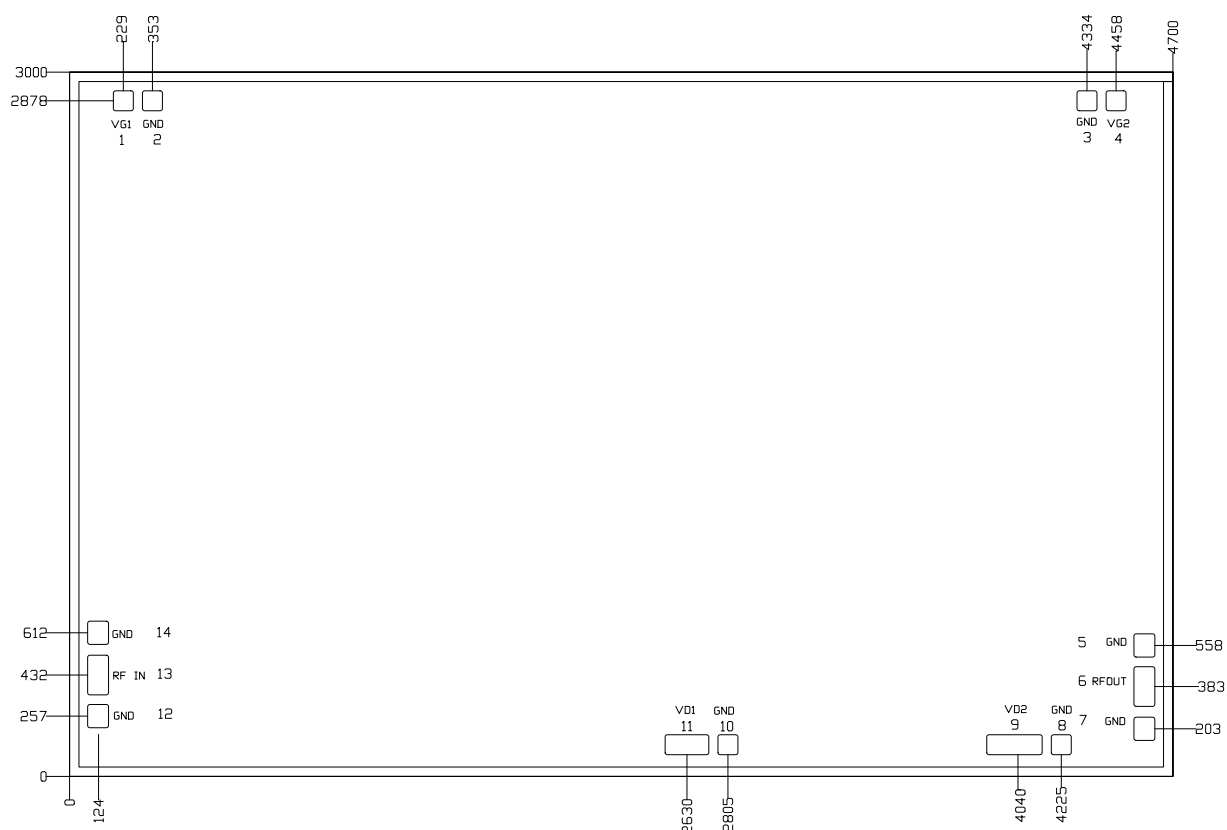


Figure 1-52. I_d vs. P_{in} 18 GHz



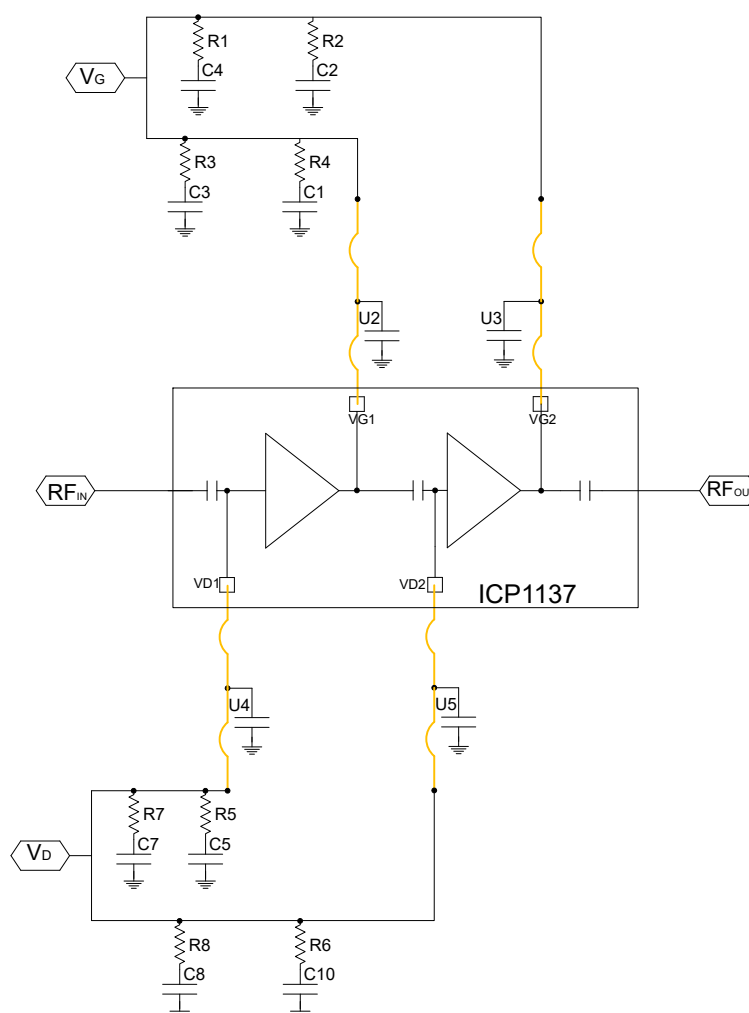
2. Mechanical Drawing



Units: μm | Thickness: 100 μm | Backside of Die is RF and DC ground

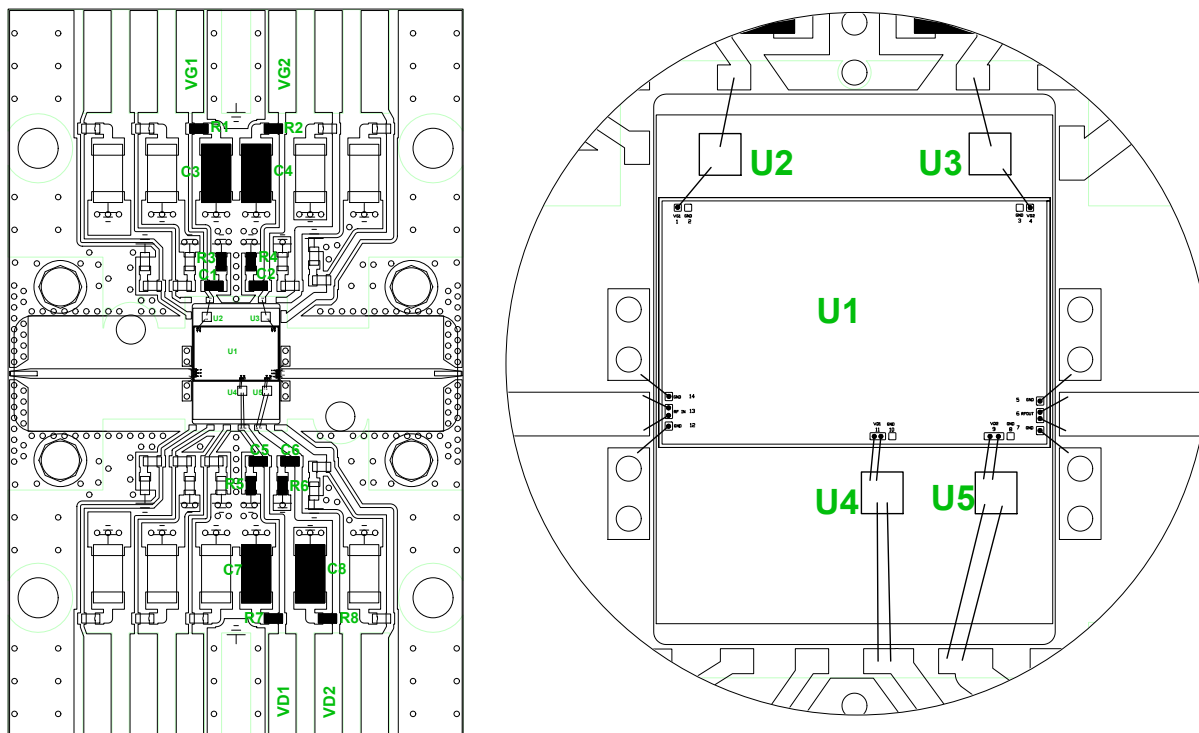
Pad No	Pad size (μm)	Function	Description
1	86x86	VG1	First stage gate bias, decoupling and bypass caps required
2,3	86x86	GND	Ground
4	86x86	VG2	Second stage gate bias, decoupling and bypass caps required
6	69x169	RF Out	50 Ohm RF Output, DC Blocked
5,7,8	86x86	GND	Ground
9	86x236	VD2	Second stage drain voltage, decoupling and bypass caps required
10	86x86	GND	Ground
11	86x186	VD1	First stage drain voltage, decoupling and bypass caps required
13	69x169	RF In	50 ohm RF Input, DC blocked
12,14	86x86	GND	Ground

3. Application Circuit



Component ID	Value	Details	Manufacturer Part No.
U2 - U5	100 pF	100 pF SLC capacitor	
C1, C2, C5, C10	10 nF	10 nF capacitor, 10%, 50V, 0402	Various
C3, C4, C7, C8	10 μ F	10 μ F capacitor, 10%, 50V, 1206	Various
R1 - R8	0 Ω	0 Ω resistor, 0402	Various

4. Assembly Drawing



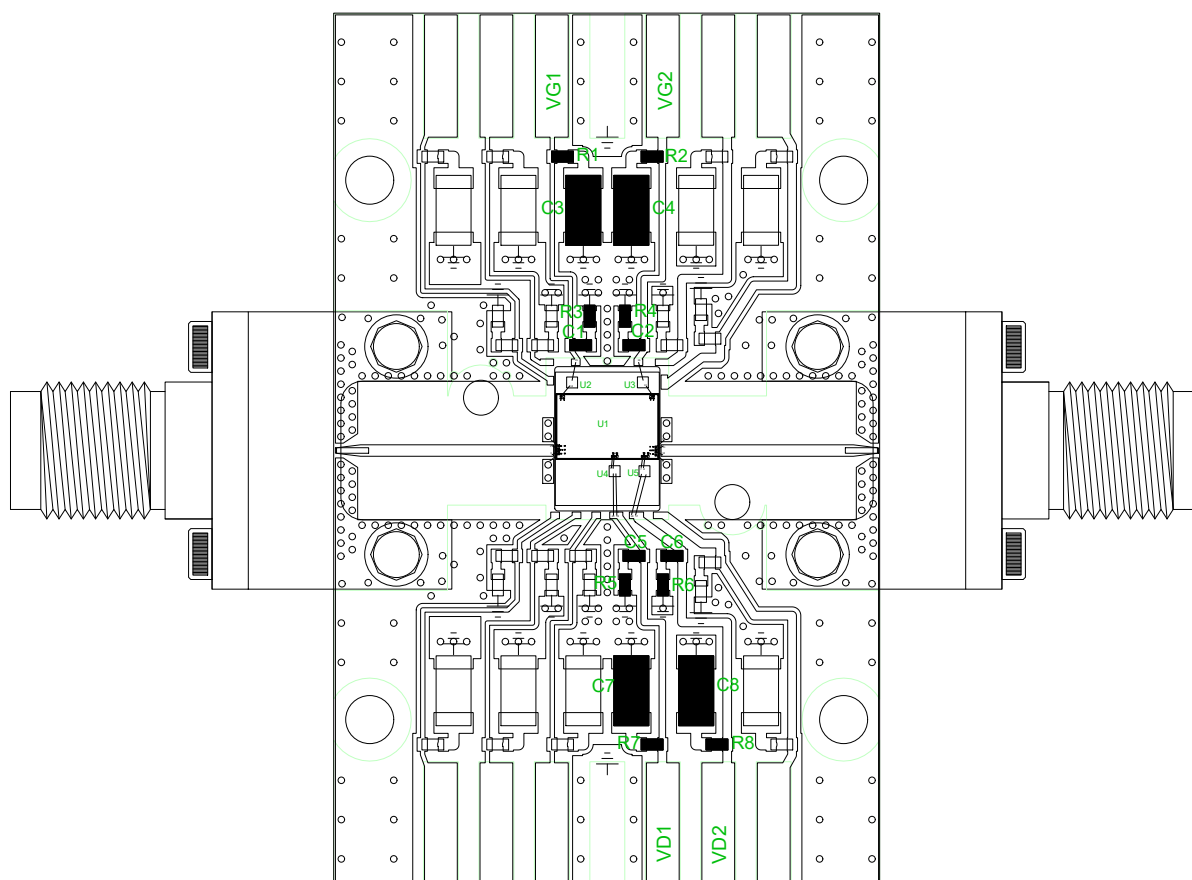
Evaluation board construction

PCB Construction	Details	Key Features	Details
Top and bottom layer	0.5 oz Cu + ENEPIG	Dielectric	RO4350B 10Mils (254µm)
Electroless nickel	3 µm – 6 µm	Via drilling	0.3 mm
Electroless palladium	0.05 µm – 0.3 µm	VIA plating thickness	50 µm – 70µm
Immersion gold	0.04 µm – 0.06µm	50Ω line width	525 µm

Interconnect assembly Notes	Die attach using Eutectic
- Ball bonding is the preferred technique. - Force, time, and ultrasonic parameters are critical. - Aluminum wire bonding is not recommended. - Bond wire diameter of 1 mil is recommended.	- Flux-less gold-tin (AuSn) (80% Au, 20% Sn with a melting point of 280 °C) preform is preferred between the die and attached surface. - Recommended preform should be approximately 0.0012 inches thick. - Die bonder using heated collet with a temperature of 310 °C and die scrubbing should be used to ensure wetting and prevent formation of voids. - Exposure to extreme temperature should be kept to a minimum. - The optimum die attach environment is nitrogen atmosphere.
Die attach of component using adhesive	Re-flow Process
- Vacuum collets are the preferred method of pickup. - Pickup method must consider the avoidance of die air bridges. - Die suitable for eutectic and epoxy die attach. - Where epoxy is used, high-thermal conductivity silver-sintered epoxy is recommended:- - Kyocera CT2700R7S	- Maximum temperature 320 °C for 30 seconds. - Material matching for coefficient of thermal expansion is crucial for long-term reliability

Assembly Guidance Continued

For optimum RF and thermal performance it is recommended that the die assembly base plate is adequately bolted to a forced air heat sink using a thermal graphite interface pad (Graphite Interface Material GCSP-017-G 170 µm thick) for optimal heat transfer. There are many variables of the second-level assembly between the die base plate and heat sink that are unable to be controlled and the following guidance is provided as information only. Fixing bolts should be provided as close to the die as possible to ensure a optimum pressure between the base plate and the heat sink. The bolting screws used to attach the PCB assembly to the heat sink must include washers and be tightened with a suitable tightening pattern to ensure a uniform pressure. It is advised all surfaces be cleaned and be free of grease and dust prior to fully aligning the assembly with all screws located and tightened to finger tight. Further torquing of the screws must be achieved in multiple phases using a star-shaped pattern to a recommended torque of 2.5 N/m.



Bias-Up Procedure	Handling Procedures
1. Set $V_G = -5V$ 2. Set V_D to 20V - 24V 3. Adjust V_G positive until I_D quiescent is 114 mA 4. Apply RF signal	Please observe the following precautions to avoid damage:
Bias-Down Procedure	Static Sensitivity
1. Turn off RF. 2. Turn off V_D, allow drain capacitor to discharge. 3. Turn off V_G.	Integrated circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

Note:

Optimum RF power performance achieved by minimizing output RF bond wire length.

5. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 5-1. Revision History

Revision	Date	Description
A	05/2026	Document created.

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