

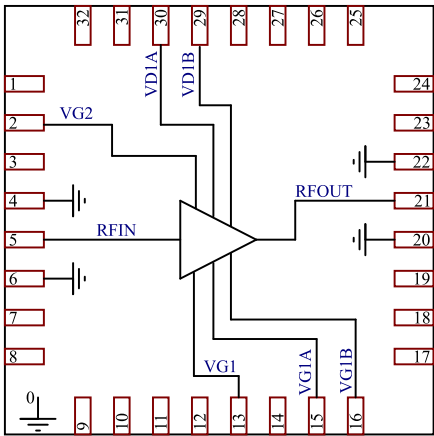
Product Overview

MMA041PP5 is a DC to 27 GHz Gallium Arsenide (GaAs) Monolithic Microwave Integrated Circuit (MMIC) Pseudomorphic High Electron Mobility Transistor (PHEMT) Distributed Low-Noise Amplifier that is packaged in a plastic 5x5 mm QFN. When nominally biased at 6V and 150 mA, the amplifier delivers a Gain of 18.5 dB, 2 dB Noise Figure, 21 dBm P1dB, and 35 dBm OIP3. The MMA041PP5 amplifier's RF input and output ports are DC-Coupled and nominally matched to 50Ω. The amplifier can be easily integrated into a variety of applications including Test and Measurement Instrumentation, Military and Warfare (EW, ECM, ECCM), Aerospace and Defense, SATCOM, and other Communication Infrastructures.

Key Features

- Broadband performance: DC to 27 GHz
- High Gain: 18.5 dB
- Low Noise Figure: 2 dB
- High Output IP3: +35 dBm
- High Input Power: +22 dBm
- 50Ω matched I/O
- 32-lead 5 mm × 5 mm × 1.2 mm plastic QFN package

Amplifier Functional Diagram



Applications

- Test and Measurement Instrumentation
- Electronic Warfare (EW), Electronic Countermeasures (ECM), and Electronic Counter-Countermeasures (ECCM)
- Military, A&D, SATCOM space
- Telecom infrastructure
- Wideband microwave radios
- Microwave and mm-Wave communication systems

Performance Overview

Parameter	Typ.	Units
Frequency range	DC – 27	GHz
Gain	18.5	dB
NF	2	dB
Output IP3	35	dBm
P1dB	21	dBm

Export Classification: EAR99

Curve Performances

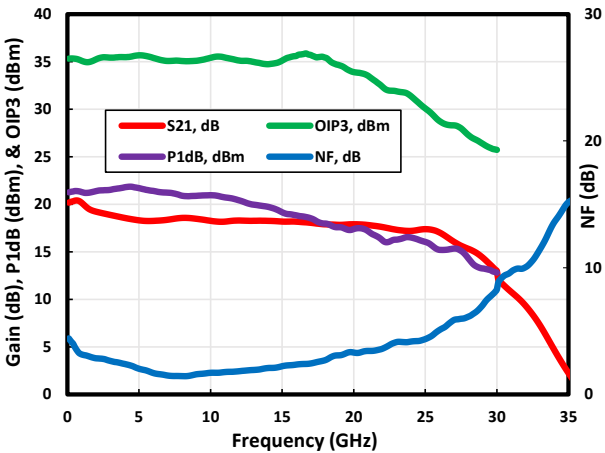


Table of Contents

Product Overview.....	1
1. Electrical Specifications.....	3
1.1. Typical Electrical Performance.....	3
1.2. Absolute Maximum Ratings.....	4
1.3. Typical Performance Curves.....	4
2. Package Specifications.....	14
3. Evaluation PCB.....	15
4. Ordering, Shipping and Handling.....	18
4.1. Handling Recommendations.....	18
4.2. Ordering Information.....	18
4.3. Packing Information.....	18
5. Revision History.....	19
Microchip Information.....	20
Trademarks.....	20
Legal Notice.....	20
Microchip Devices Code Protection Feature.....	20

1. Electrical Specifications

1.1. Typical Electrical Performance

Table 1-1. Typical Electrical Performance at 25 °C, $V_{DD} = +6V$, $I_{DD} = 150\text{ mA}$ (Unless otherwise mentioned)

Parameter	Frequency Range	Min	Typ.	Max	Units
Frequency range		DC		27	GHz
Gain	DC – 6 GHz	18	19		dB
	6 – 12 GHz	17	18.5		
	12 – 20 GHz	17	18		
	20 – 27 GHz		17		
Gain flatness	4 – 12 GHz		± 0.5		dB
	12 – 20 GHz		± 0.25		
Noise Figure	3 – 6 GHz		2.2	3.5	dB
	6 – 12 GHz		1.7	2	
	12 – 20 GHz		2	3.5	
	20 – 27 GHz		4		
Input Return Loss	DC – 6 GHz		17		dB
	6 – 12 GHz		15		
	12 – 20 GHz		15		
	20 – 27 GHz		12		
Output Return Loss	DC – 6 GHz		35		dB
	6 – 12 GHz		35		
	12 – 20 GHz		35		
	20 – 27 GHz		30		
P1dB	DC – 6 GHz	20	21		dBm
	6 – 12 GHz	19	21		
	12 – 20 GHz	17.5	20		
	20 – 27 GHz		17		
P_{sat}	DC – 6 GHz		23		dBm
	6 – 12 GHz		23		
	12 – 20 GHz		22		
	20 – 27 GHz		18		
OIP3 (7V, 180 mA)	DC – 6 GHz		35		dBm
	6 – 12 GHz		35		
	12 – 20 GHz		35		
	20 – 27 GHz		30		
OIP2 (low) (2 nd Order Intercept point F2-F1)			45		dBm
V_{DD} (Drain Voltage Supply)			6		V
I_{DD} (Drain Current)			150		mA
V_{GG} (Gate Voltage Bias)			- 0.4		V

1.2. Absolute Maximum Ratings

The following table shows the absolute maximum ratings of the MMA041PP5 device at 25 °C, unless otherwise specified. Exceeding any of the maximum ratings potentially could cause damage or latent defects to the device.

Table 1-2. Absolute Maximum Ratings

Parameter	Rating
Drain bias voltage (V_{DD})	8V
Gate Bias Voltage (V_G)	-2V to 0.5V
RF Input Power (P_{in})	22 dBm
Channel Temperature	165 °C
V_{DD} Current (I_{DD})	300 mA
DC Power Dissipation ($T = + 85\text{ °C}$)	2.4W
Thermal Resistance	18 °C/W
Operating Temperature	- 55 °C to + 85 °C
Storage Temperature	- 65 °C to + 150 °C



ESD Sensitive Device

1.3. Typical Performance Curves

1.3.1. Typical Performance vs. Temperature

The graphs shown in Figures 1-1 through 1-30 represent the Typical Performance versus Temperature curves of the MMA041PP5 under specific bias conditions. All measurements were taken using the Test Circuit shown in [Figure 3-2](#).

Figure 1-1. Gain vs. Temperature at 5V/100 mA

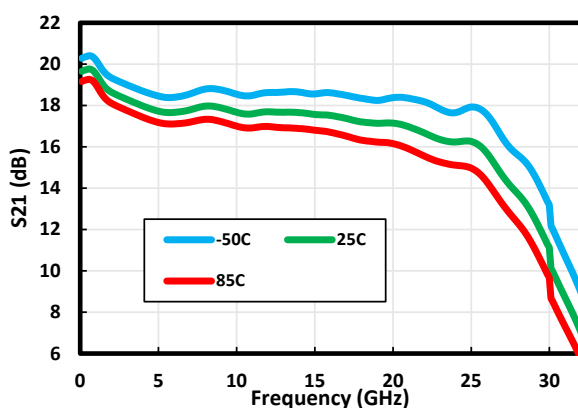


Figure 1-2. Gain vs. Temperature at 6V/150 mA

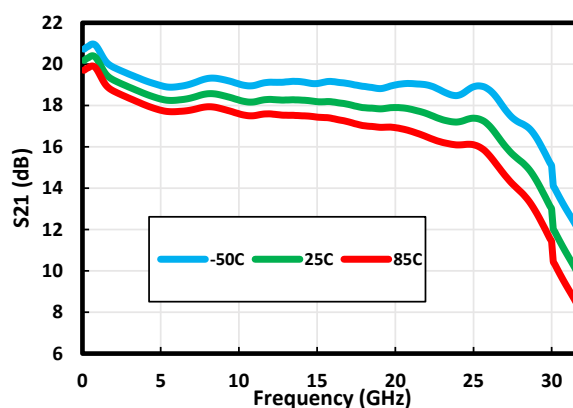


Figure 1-3. Gain vs. Temperature at 7V/180 mA

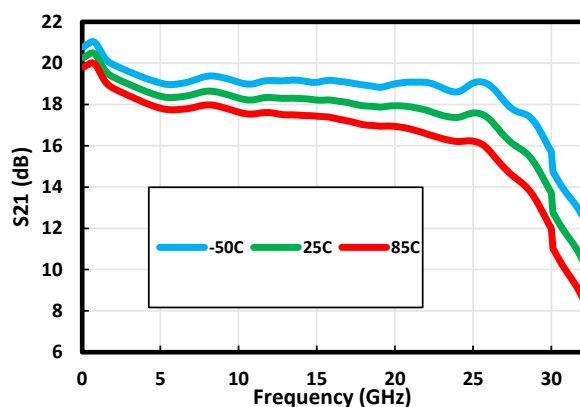


Figure 1-4. S11 vs. Temperature at 5V/120 mA

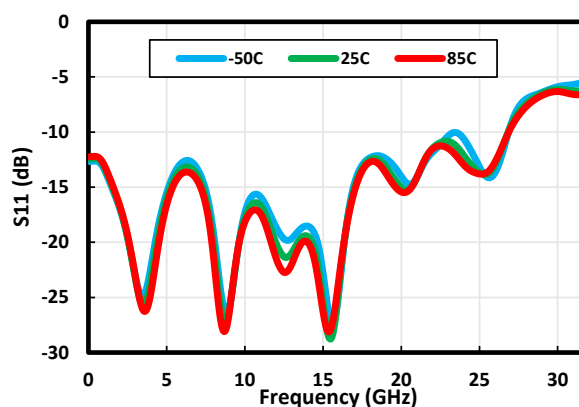


Figure 1-5. S11 vs. Temperature at 6V/150 mA

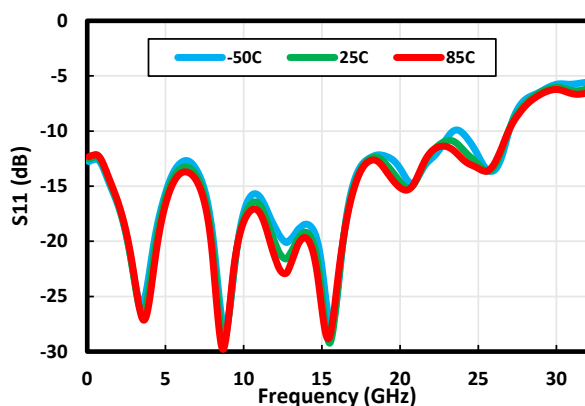


Figure 1-6. S11 vs. Temperature at 7V/180 mA

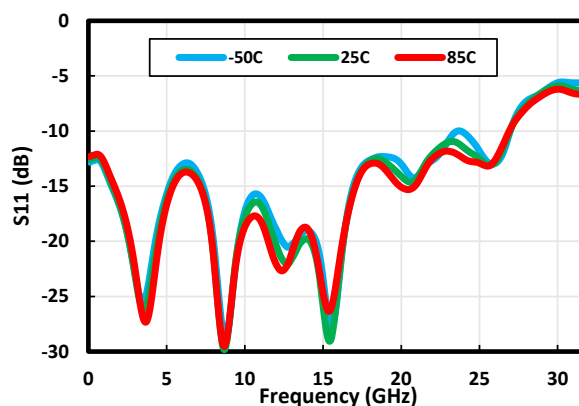


Figure 1-7. S22 vs. Temperature at 5V/120 mA

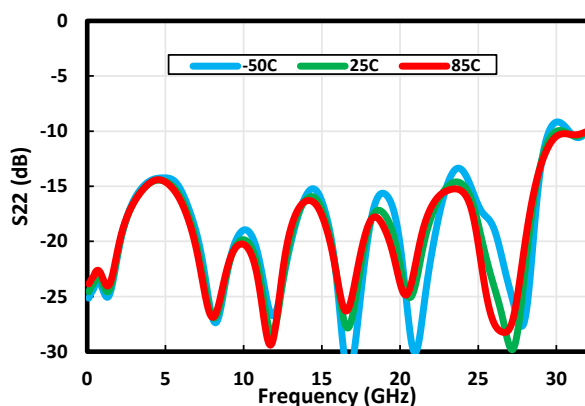


Figure 1-8. S22 vs. Temperature at 6V/150 mA

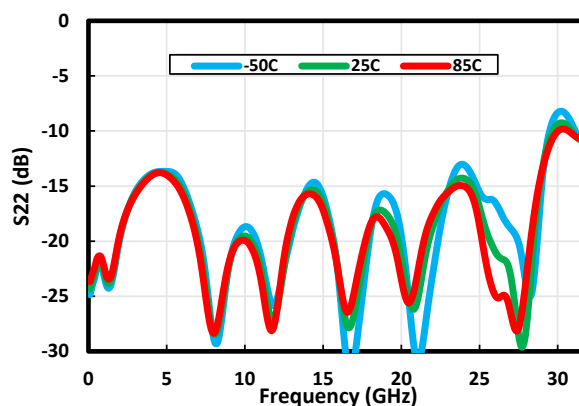


Figure 1-9. S22 vs. Temperature at 7V/180 mA

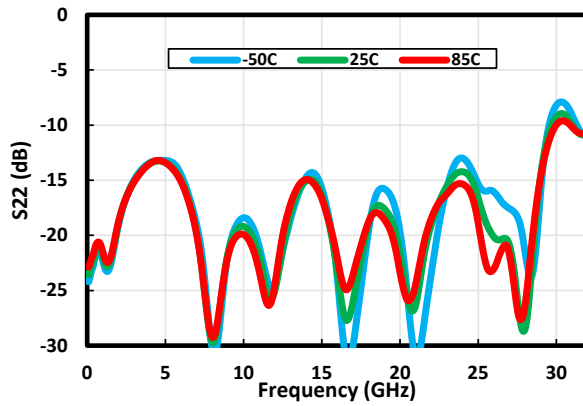


Figure 1-10. S12 vs. Temperature at 5V/120 mA

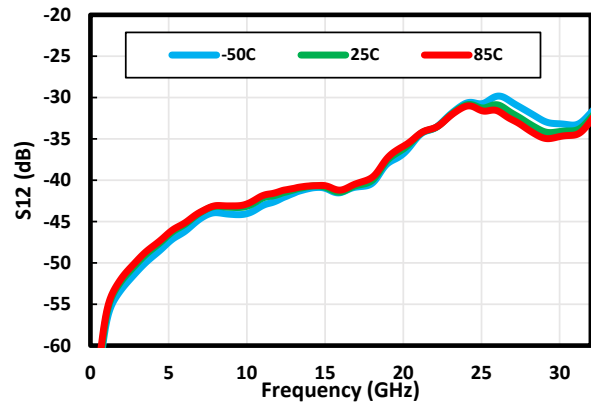


Figure 1-11. S12 vs. Temperature at 6V/150 mA

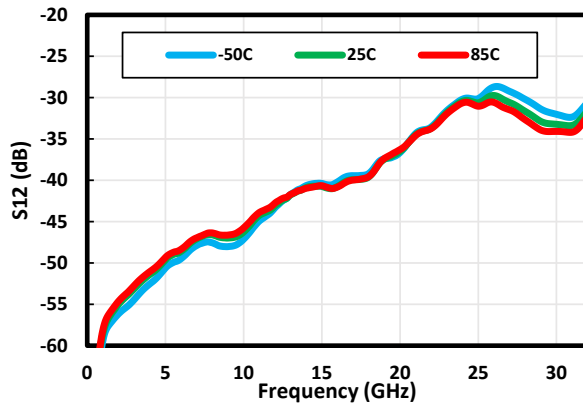


Figure 1-12. S12 vs. Temperature at 7V/180 mA

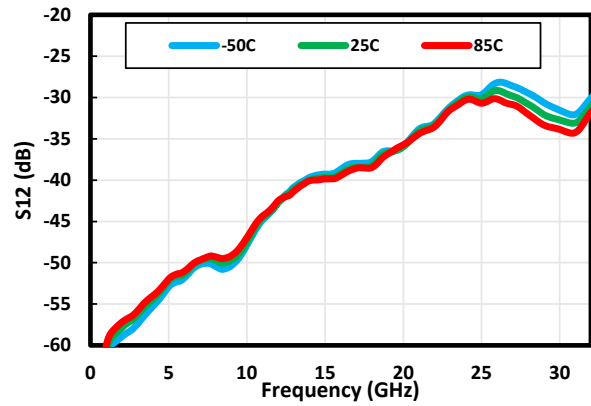


Figure 1-13. Noise Figure vs. Temperature at 5V/120 mA

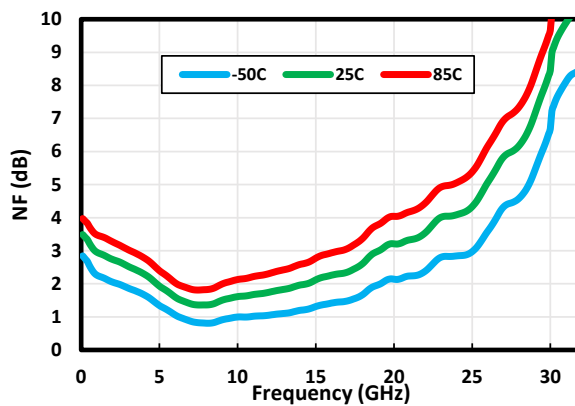


Figure 1-14. Noise Figure vs. Temperature at 6V/150 mA

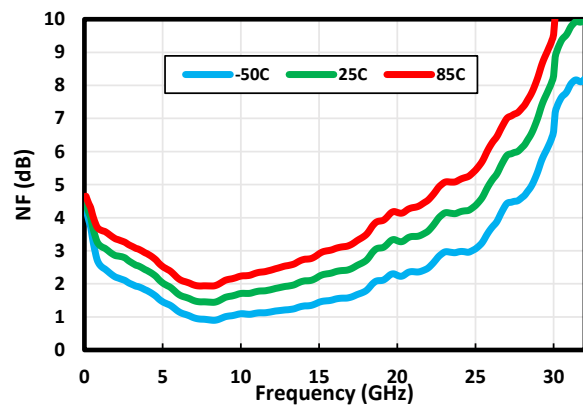


Figure 1-15. Noise Figure vs. Temperature at 7V/180 mA

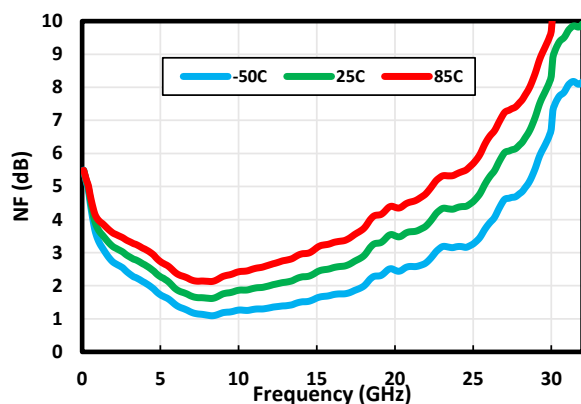


Figure 1-16. P1dB vs. Temperature at 5V/120 mA

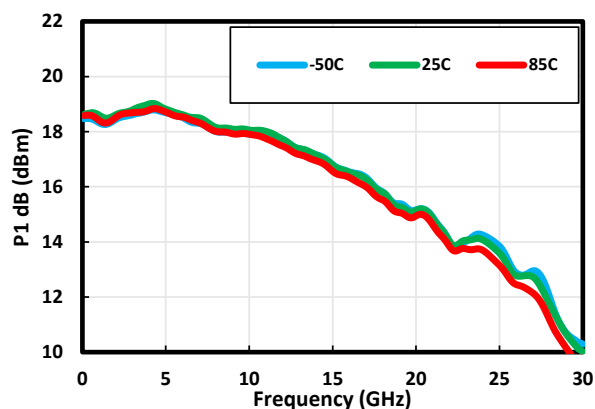


Figure 1-17. P1dB vs. Temperature at 6V/150 mA

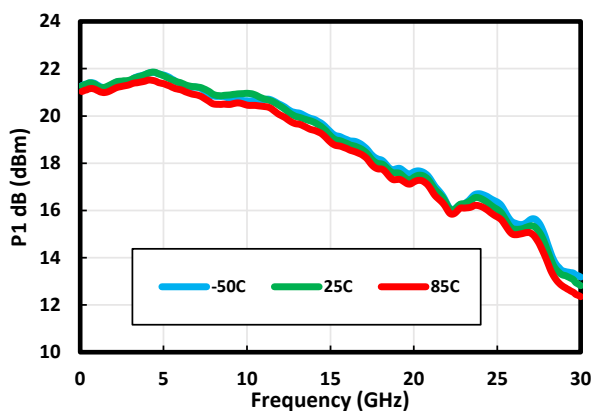


Figure 1-18. P1dB vs. Temperature at 7V/180 mA

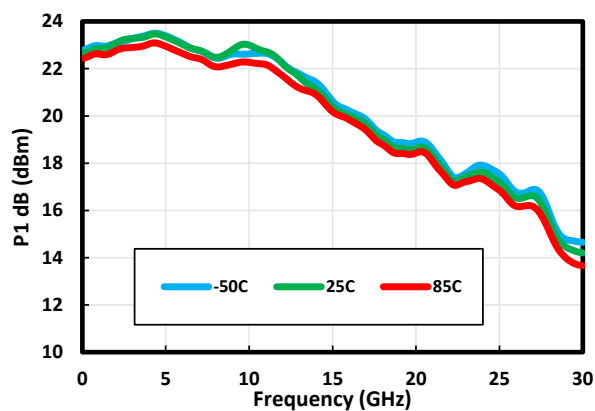


Figure 1-19. Psat vs. Temperature at 5V/12 mA

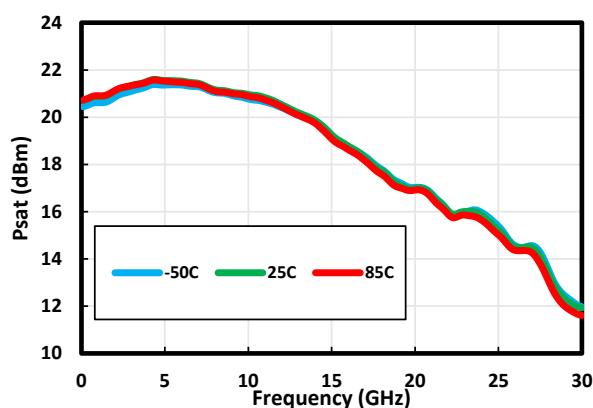


Figure 1-20. Psat vs. Temperature at 6V/150 mA

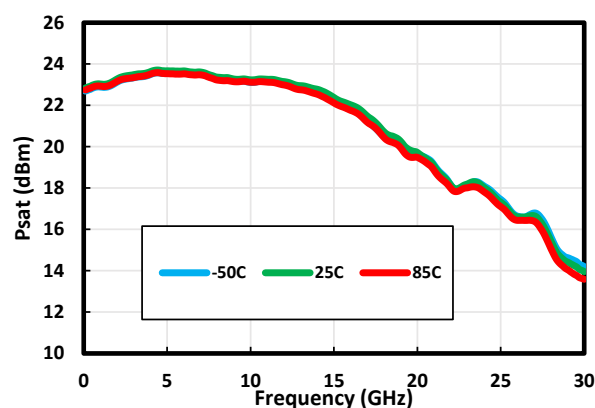


Figure 1-21. Psat vs. Temperature at 7V/180 mA

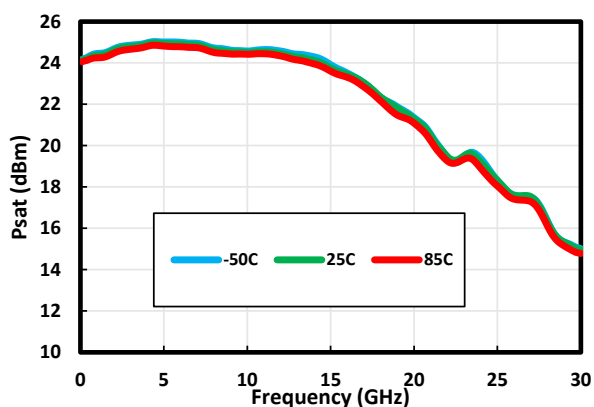


Figure 1-22. OIP3 vs. Temperature at 5V/120 mA

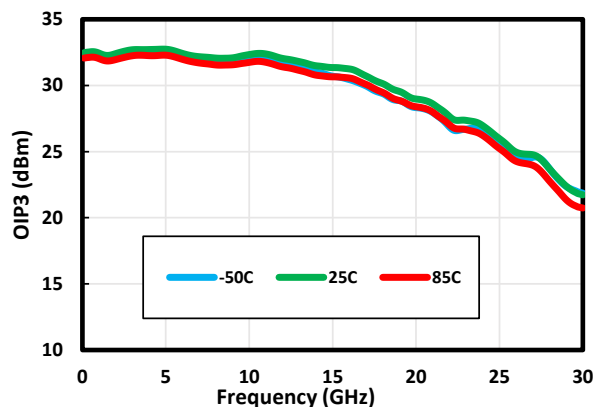


Figure 1-23. OIP3 vs. Temperature at 6V/150 mA

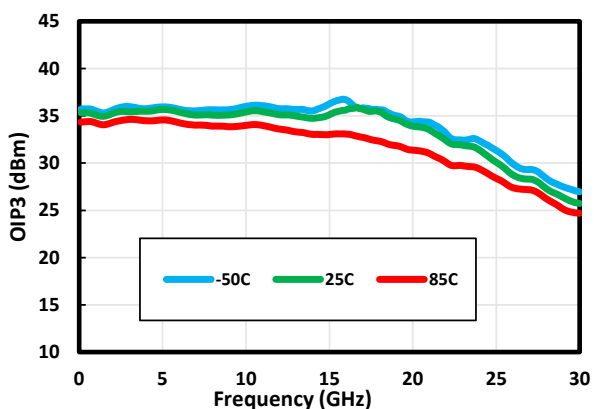


Figure 1-24. OIP3 vs. Temperature at 7V/180 mA

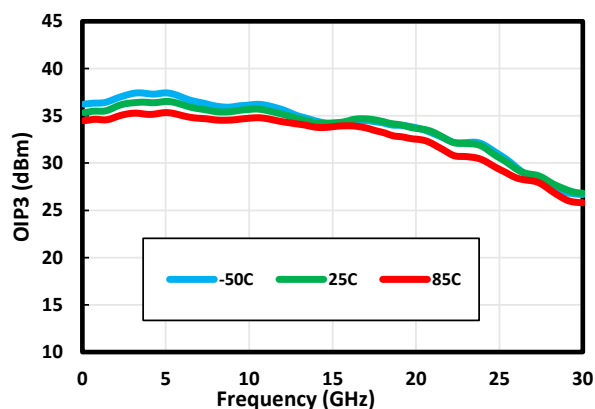


Figure 1-25. OIP2 vs. Temperature at 5V/120 mA

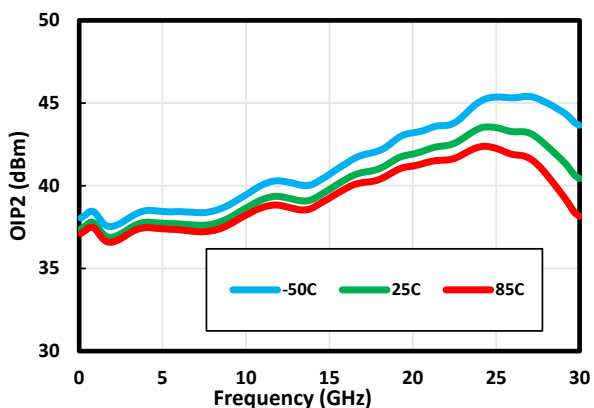


Figure 1-26. OIP2 vs. Temperature at 6V/150 mA

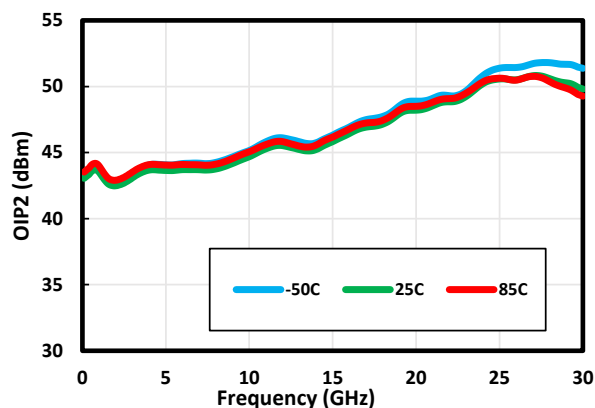


Figure 1-27. OIP2 vs. Temperature at 7V/180 mA

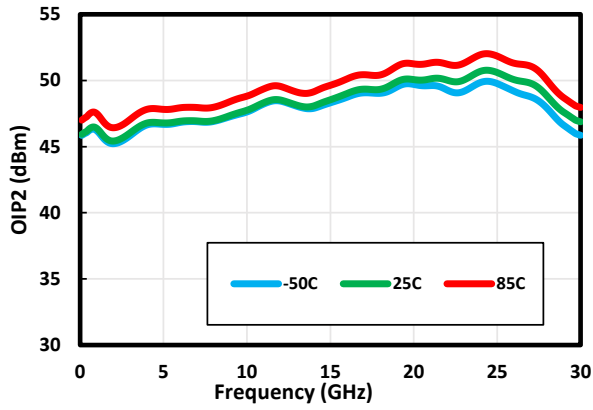


Figure 1-28. IM3 vs. Temperature at 5V/120 mA

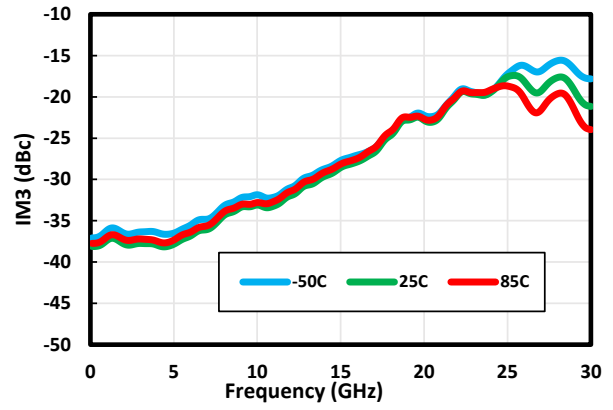


Figure 1-29. IM3 vs. Temperature at 6V/150 mA

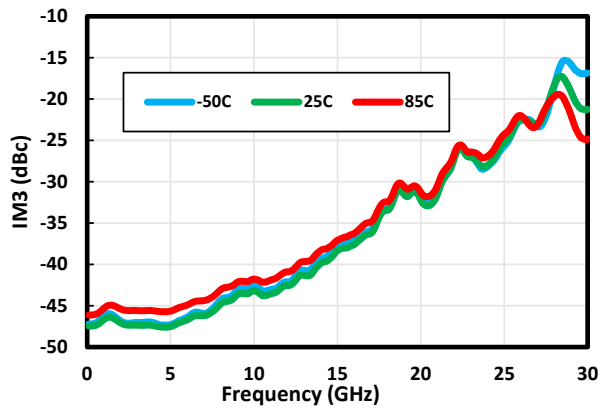
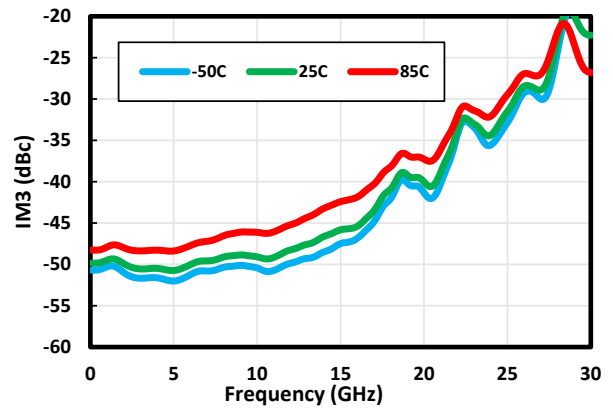


Figure 1-30. IM3 vs. Temperature at 7V/180 mA



1.3.2. Typical Performance vs. Bias

The graphs shown in Figures 1-31 through 1-40 represent the Typical Performance versus Bias curves of the MMA041PP5 under constant temperature of 25 °C. All measurements were taken using the Test Circuit shown in Figure 3-2.

Figure 1-31. Gain vs. V_{DD}/I_{DD}

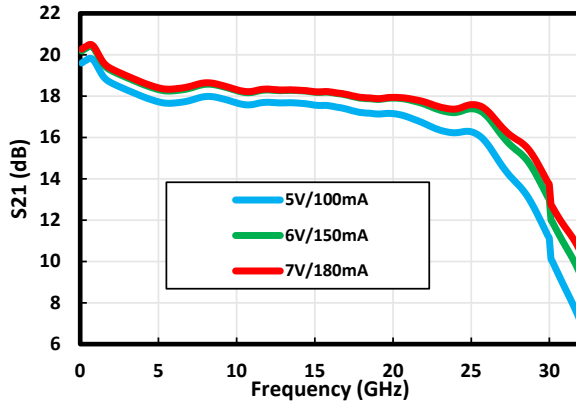


Figure 1-32. NF vs. V_{DD}/I_{DD}

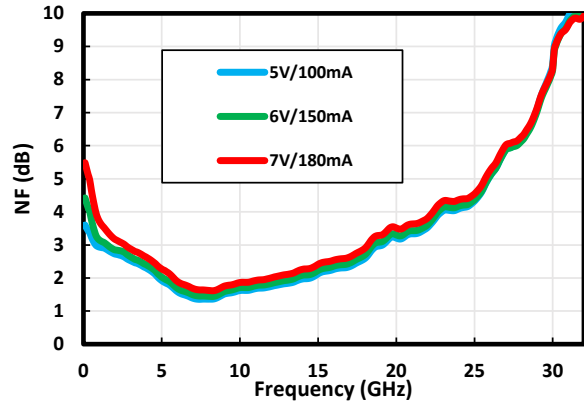


Figure 1-33. S11 vs. V_{DD}/I_{DD}

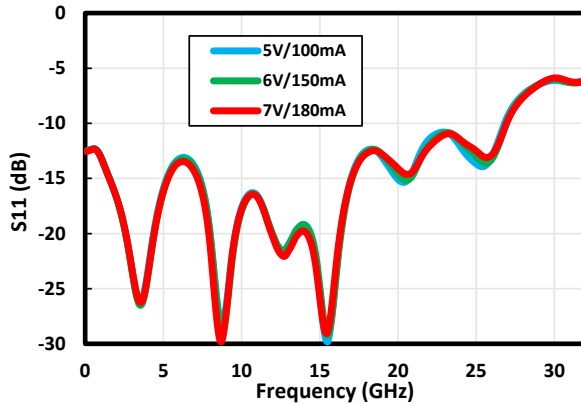


Figure 1-34. S22 vs. V_{DD}/I_{DD}

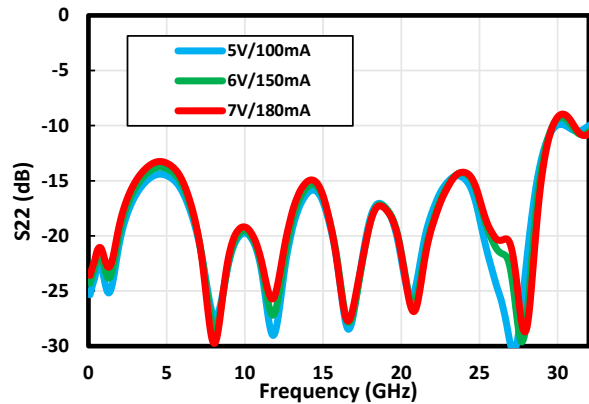


Figure 1-35. S12 vs. V_{DD}/I_{DD}

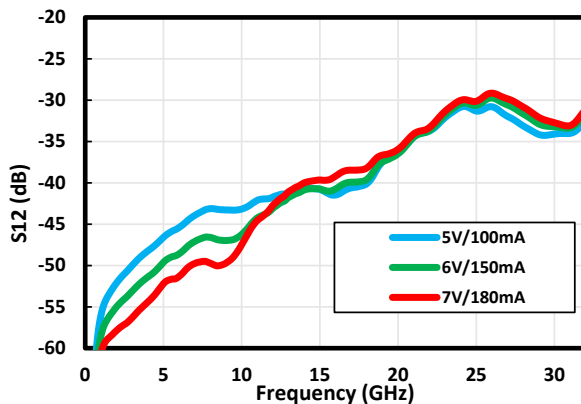


Figure 1-36. P1dB vs. V_{DD}/I_{DD}

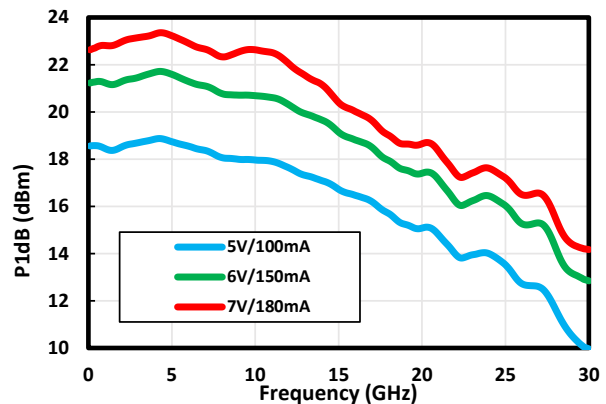


Figure 1-37. P_{sat} vs. V_{DD}/I_{DD}

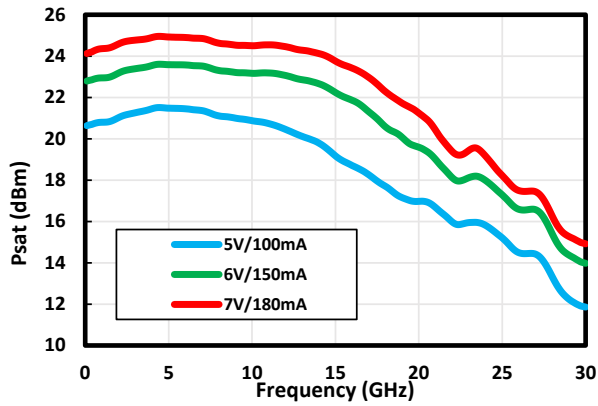


Figure 1-38. OIP3 vs. V_{DD}/I_{DD}

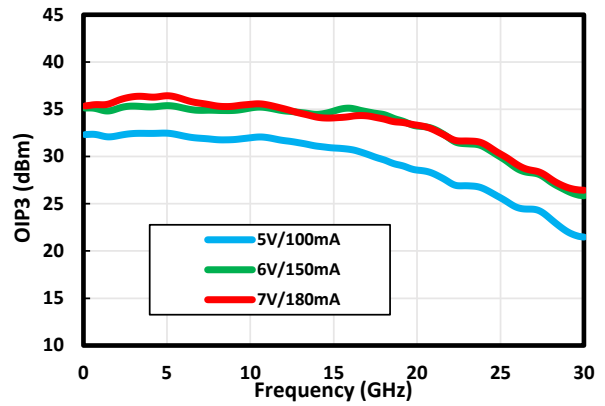


Figure 1-39. OIP2 Low at $\Delta = 10$ MHz V_{DD}/I_{DD}

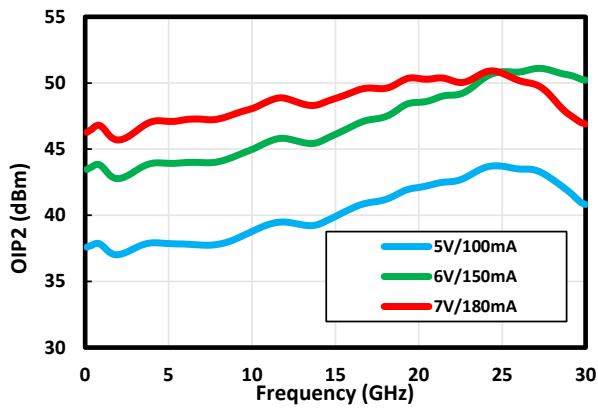
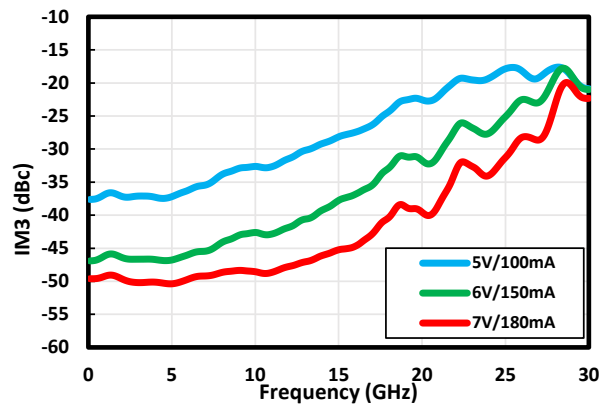


Figure 1-40. IM3 vs. V_{DD}/I_{DD} , 10 dBm (per tone)



1.3.3. Typical Performance vs. Power

The graphs shown in Figures 1-41 through 1-49 represent the Typical Performance versus Output Power curves of the MMA041PP5 under constant temperature 25 °C. All measurements were taken using the Test Circuit shown in Figure 3-2.

Figure 1-41. IM2 vs. Power at 5V/100 mA

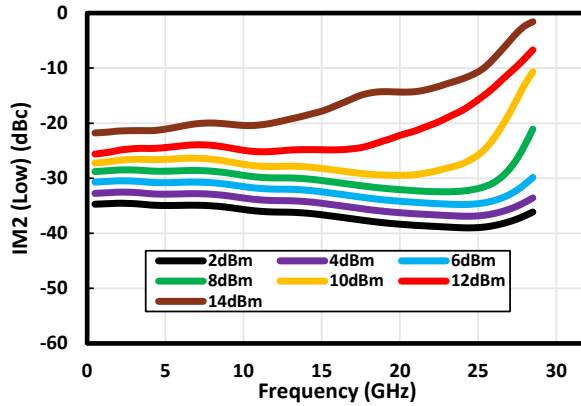


Figure 1-42. IM2 vs. Power at 6V/150 mA

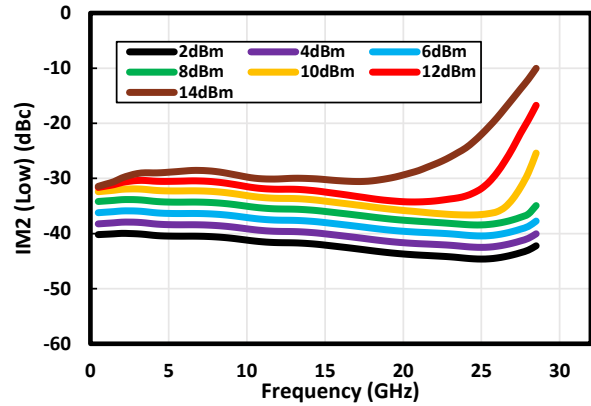


Figure 1-43. IM2 vs. Power at 7V/180 mA

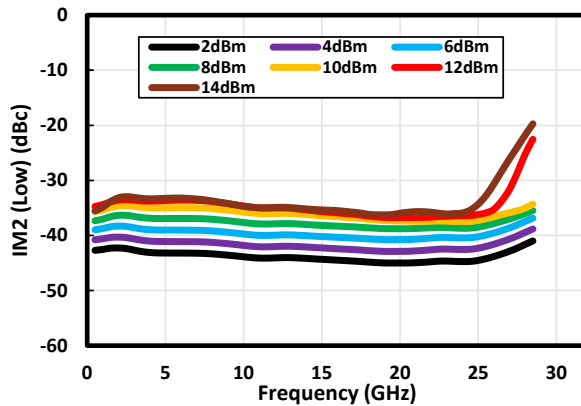


Figure 1-44. IM3 vs. Power at 5V/100 mA

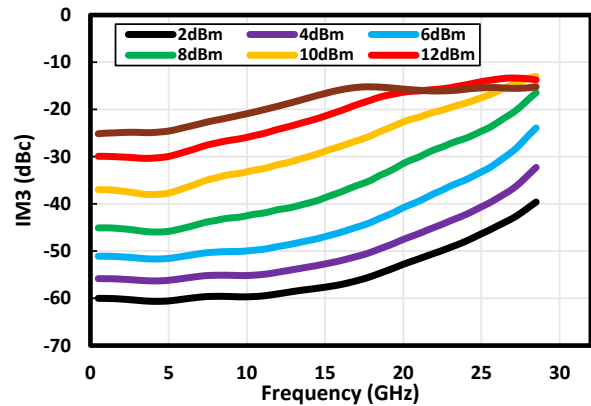


Figure 1-45. IM3 vs. Power at 6V/150 mA

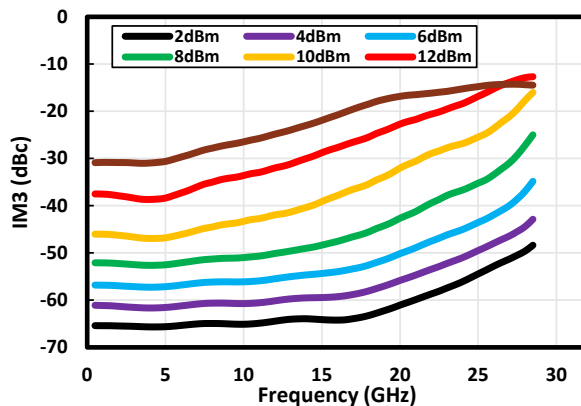


Figure 1-46. IM3 vs. Power at 7V/180 mA

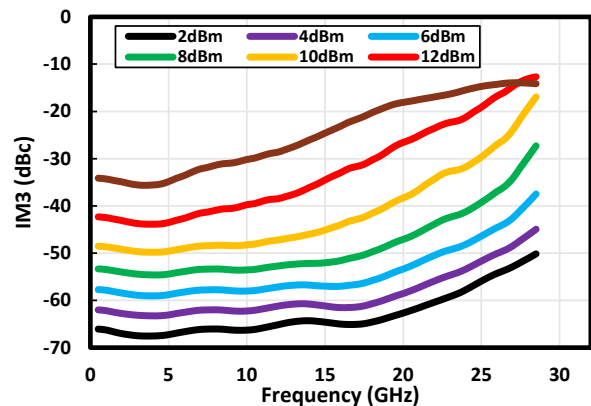


Figure 1-47. 2nd Harmonic vs. Power at 5V/100 mA

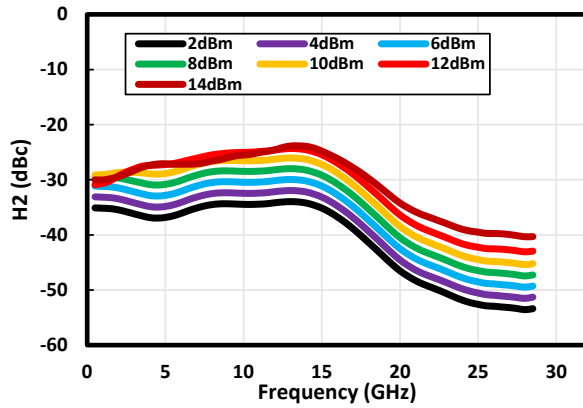


Figure 1-48. 2nd Harmonic vs. Power at 6V/150 mA

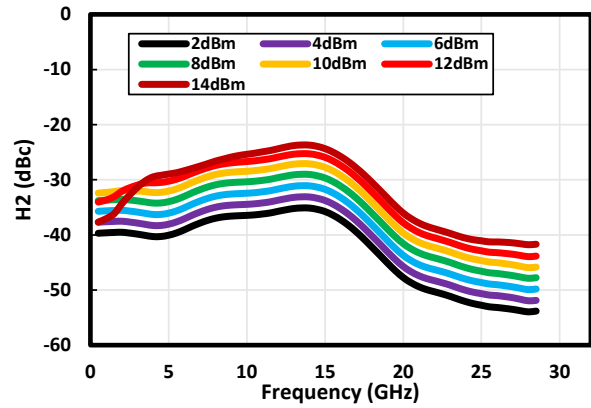
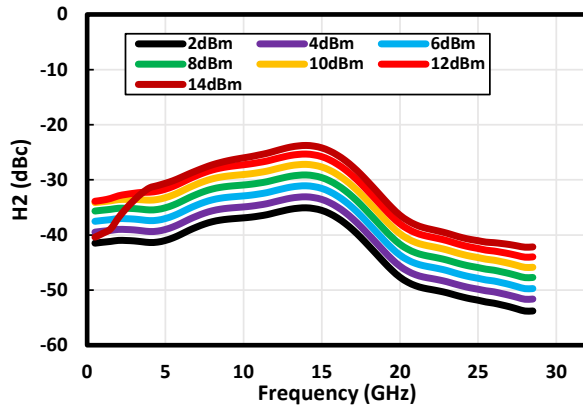


Figure 1-49. 2nd Harmonic vs. Power at 7V/180 mA



2. Package Specifications

The following illustration shows the package outline of the MMA041PP5 device. Dimensions are in millimeters [inches].

Figure 2-1. Package Outline Drawing (mm[Inches])

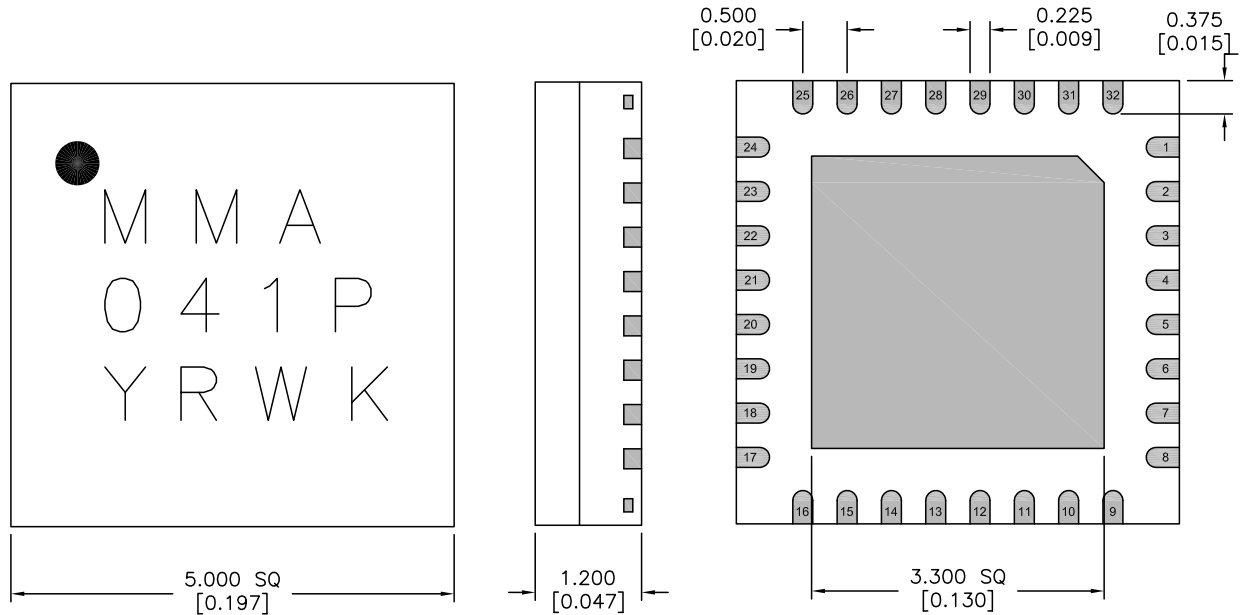


Table 2-1. Package Information

Package	5X5 mm 32L Plastic QFN
Lead Frame	C194 Cu
Plating	Ni: 0.50 μ m min Pd: 0.02 μ m min Au: 0.05 μ m max
Package Body Material	RoHS Compliant Low-stress injection molded plastic

Table 2-2. PIN Description

PIN Number	Pad Name	Pad Description
2	V _{GG}	Second Gate Bias. Connect to V _{D1A} (Pin 30); Could optionally be used for gain or linearity control by applying external bias in the range of V _{DD} +/-20%
5	RF _{IN} + V _{G1}	RF Input (DC-Coupled) nominally matched to 50 Ω . Requires an external bias-T if intended for VG1 Gate bias instead of using Pin 13.
13	V _{G1}	Gate control for amplifier. Adjust to achieve IDD = 150 mA
15, 16	V _{G1A} , V _{G1B}	Low-frequency termination. Connect bypass capacitors per application circuit.
21	RF _{OUT} + V _{DD}	RF Output (DC-Coupled) nominally matched to 50 Ω . Requires an external bias-T if intended to bias V _{DD} on the RF Output.
30, 29	V _{D1A} , V _{D1B}	Low-frequency termination. Connect bypass capacitors per application circuit below. (Do NOT apply V _{DD} bias to this connections)
4, 6, 20, 22	RF/DC GND	Should be connected to PCB RF/DC Ground
Backside Paddle	RF/DC GND	Must be connected to RF/DC Ground
1, 3, 7, 8, 9, 10, 11, 12, 14, 17, 18, 19, 23, 24, 25, 26, 27, 28, 31, 32	N/C	Not-Connected Pins. It is recommended to merge with the RF ground on the PCB. Proper ground vias should be used to avoid "RF bridges". If this is not possible, it would be OK to leave them unconnected.

3. Evaluation PCB

Figure 3-1. Amplifier Functional Schematic

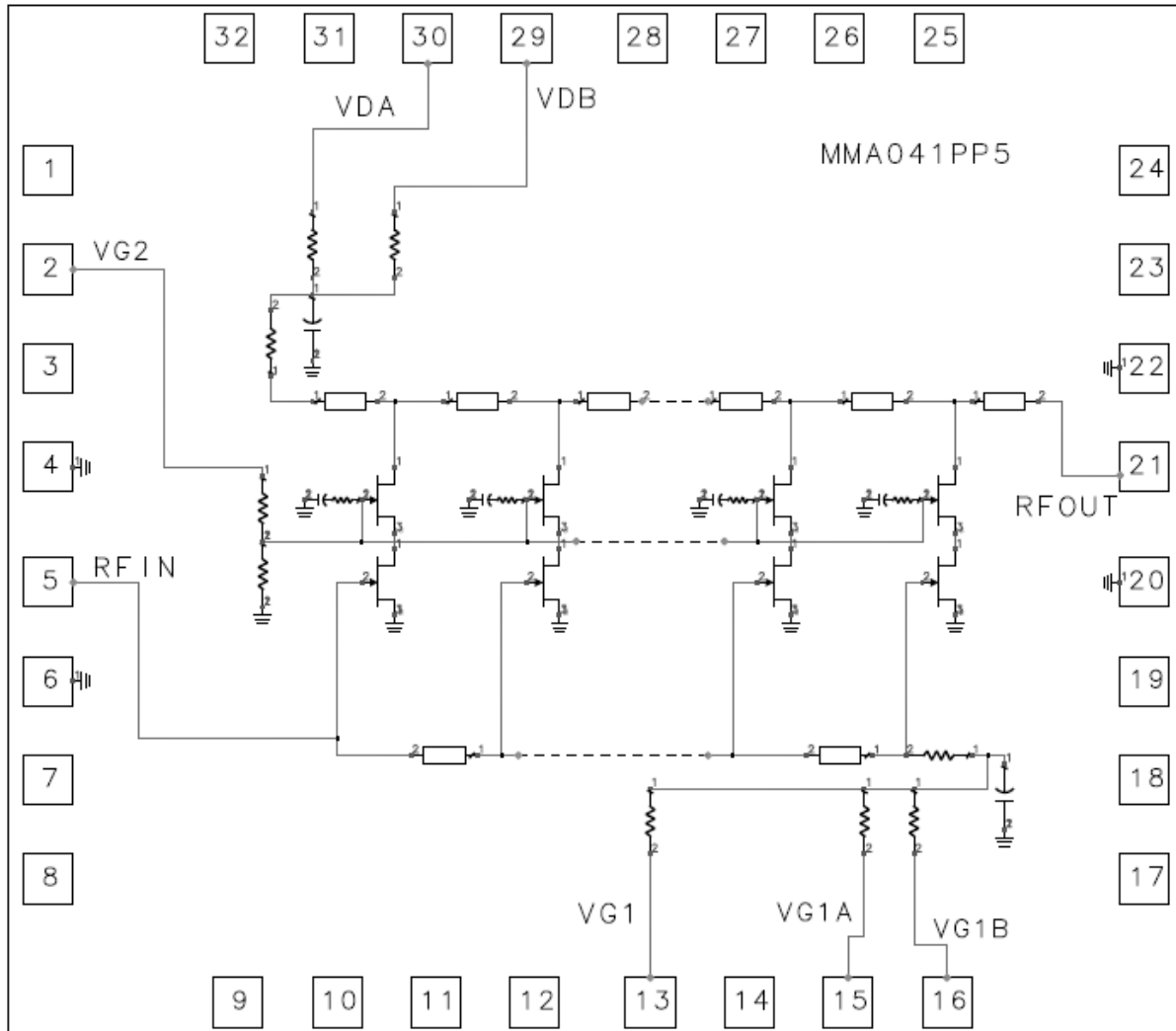


Figure 3-2. MMA041PP5E: Eval PCB

DESCRIPTION

- ① Optional 2.92mm connectors for through calibration
- ② Ground pins
- ③ Jumper for VGG pin to VDA pin connect
- ④ RF + DC Input (2.92mm connector)
- ⑤ Ground pins
- ⑥ VG1 access pin
- ⑦ VG1 Label
- ⑧ RF + DC Output (2.92mm connector)
- ⑨ Part Number Label

MMA041PP5E Bias Procedure

Step	Instruction
1	Make sure all DC and RF connections are attached before activating any DC voltage power supplies.
2	Make sure ESD precaution jumper from VG1 to GND on H2 header is removed.
3	Make sure VGG to VDA jumper is in place on H1 or, if using external power supply, VGG power supply is connected to marked pin on H1.
4	DC supply for VDD should be fed through an external bias-T on the RF + DC output port.
	<i>Note: DC supply for VG1 could be attached either through an external bias-T on the RF + DC input port or through the marked pin on H2.</i>
5	Set VG1 at -1.0V.
	<i>Note: If using VGG externally, it should be on soon after VG1. The range of VGG should be at VDD +/-20%.</i>
6	Set VDD according to your applications plan with current compliance at 300mA.
7	Power supply sequencing should always be VG1, VGG (if used externally), then VDD (VDD is always last on and first off).
8	Adjust VG1 gradually increasing voltage by 0.01V steps until IDD reaches desired application range.
	CAUTION: If external bias-T used on the RF + DC Output is showing a very low cut-off frequency, precautions should be made to avoid fast changes of the IDD current otherwise DC spikes, caused by transitions, could exceed the VDD maximum level and damage the part.

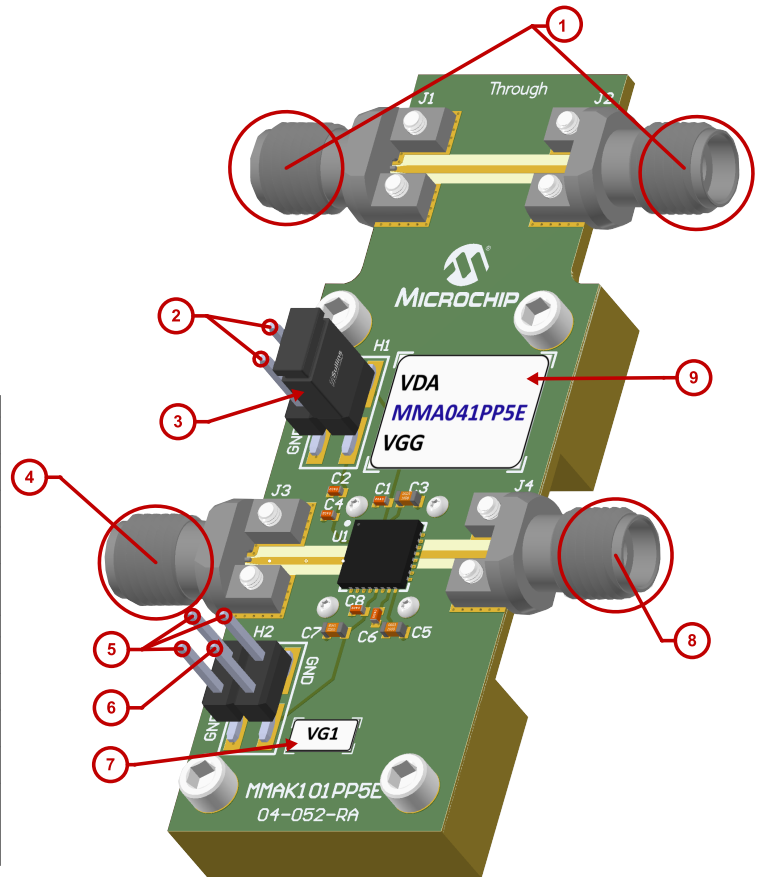


Figure 3-3. MMA041PP5E: Eval PCB Schematic

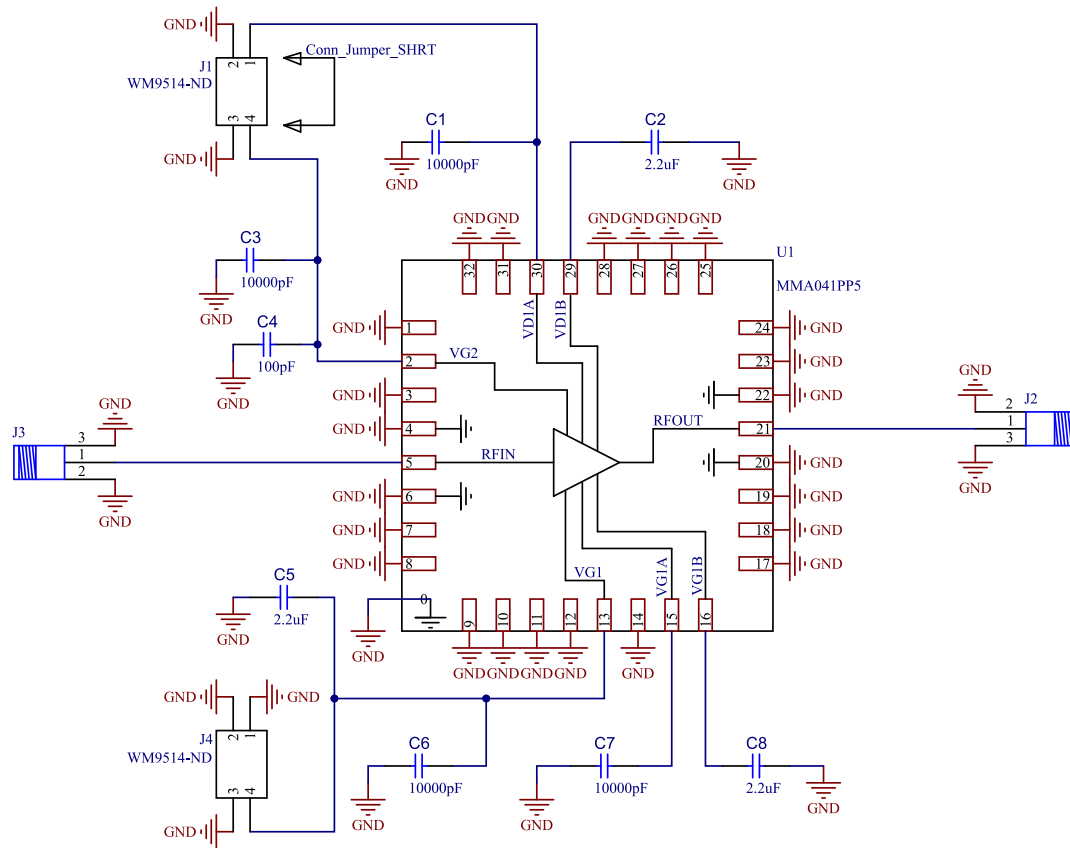


Table 3-1. Bill of Material

Item Num.	Component designator	Description	Mnf. Part Num.	Mnf.	Qty.
1	U1	5 X 5 32 Leads QFN	MMA041PP5	Microchip	1
2	C4	100 pF $\pm 10\%$ 25V Ceramic Capacitor X7R 0402	C0402C101K3GACT U	KEMET	1
3	C2, C5, C8	2.2 μ F $\pm 10\%$ 16V Ceramic Capacitor X5R 0603	C1608X5R1C225K0 80AB	TDK	3
4	C1, C3, C6, C7	10000 pF $\pm 10\%$ 50V Ceramic Capacitor X7R 0402	CC0402KRX7R9BB1 03	Yageo	4
5	J2, J3, J5, J6	Connector, 2.9mm Jack PCB Edge Mount .012 pin	25-146-1000-90	Winchester Interconnect	4
6	J1, J4	Connector Unshrouded Header, 2x2, 2.54mm	15-91-2040	Molex	2
7	JUMP1	Connector, 2 Position Shunt, Black, Closed Top 2.54mm	SPC02SYAN	Sullins	1

4. Ordering, Shipping and Handling

4.1. Handling Recommendations

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. It is recommended to follow all procedures and guidelines outlined in the Microchip application note AN01: GaAs MMIC Handling and Die Attach Recommendations

4.2. Ordering Information

For additional ordering information, contact your Microchip sales representative.

Part Number	Package	Note
MMA041AA	Die	Refer to corresponding MMA041AA Datasheet
MMA041PP5	5 mm × 5 mm, 32L Plastic QFN	
MMA041PP5E	Eval PCB	

4.3. Packing Information

Part Number	Description
MMA041PP5-TR	Tape and Reel

Note: Contact your Microchip sales representative for the minimum quantity order

5. Revision History

Table 5-1. Revision History

Revision	Date	Description
A	05/2026	Document migrated from Microsemi template to Microchip template; Assigned Microchip literature number DS-00006410A, which replaces Microsemi literature number MSCC-0341-DS-00102-2.00-0718
Initial release	03/2022	Document migrated to Microchip format.

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ISBN: 979-8-3371-2984-6

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