
Single Port 10/100/1000 Ethernet Transceiver with SGMII, IEEE 1588, SyncE and TSN Support

Features

- Single Port Gigabit Ethernet Transceiver
- SGMII Ver. 1.8 MAC Interface
- Synchronous Ethernet (SyncE) Support
 - Configurable recovered clock outputs
 - Fast Link Failure (FLF) indication
- On-Chip LDO Controller to Support Single 2.5V or 3.3V Supply Operation
- Jumbo Frame Support Up to 16 KB
- 25 MHz Reference Clock Output
- Time Sensitive Networking (TSN) Frame Preemption support per IEEE 802.3™-2022 clause 99
- 1588™-2008/PTP
 - Layer 2, UDP/IPv4 and UDP/IPv6 formats
 - Tagged and non-tagged frame formats
 - One-step and two-step modes of operation
 - ± 8 ns PTP accuracy
 - OC TimeTransmitter/TimeReceiver, BC, and TC all supported
- IEEE 802.3-2022 Energy Efficient Ethernet (EEE)
 - Low-Power Idle (LPI) Mode
- IEEE 802.3-2022 Auto-Negotiation for Speed, Duplex, and Energy Efficient Ethernet (EEE)
- IEEE 802.3-2022 Express and Preemptible Frames, enabling Switch/SoC Support of IEEE 802.1Qb-2022 Frame Preemption
- Two Programmable LED Outputs for Link, Activity, and Speed
- SOF Pulses provided for each arriving and departing frame device port
- Coma mode to Eliminate Port Link Bouncing at Startup and Synchronize LEDs
- 16 GPIOs
- LinkMD® TDR-based Cable Diagnostic to Identify Faulty Copper Cabling
- Auto-Downshift, enabling slower speed linkup if fault conditions prevent higher speed linkup
- Signal Quality Indication
- Loopback modes for Diagnostics
- Automatic MDI/MDI-X Crossover to Detect and Correct Pair Swaps, Pair Skew, and Pair Polarity
- Management Data Input/Output (MDIO) Interface for PHY Register Configuration
- Interrupt Pin Option
- Die Temperature Monitor
- ActiPHY® Power Management
 - Energy Detect Power Down
 - Chip Power Down
 - EEE Low Power Idle mode
 - Smart power savings up to 20 mW for cables <70m
- Operating Voltages
 - Digital Core (VDDCORE): 1.1V (On-chip 1.1V LDO with External FET)
 - Analog Operation: 3.3V, 2.5V (VDDAH) and 1.1V (VDDAL)
 - VDD I/O (VDDIO): 3.3V, 2.5V, or 1.8V
 - (VDDAH): 3.3V or 2.5V
- 56-pin VQFN (8 × 8 mm) Package
- Temperature Support
 - Commercial temperature range (0° to +70°C)
 - Extended Industrial temperature range (-40° to +105°C)

Target Applications

- Enterprise/SMB Switches
- Industrial Switches
- Cellular Infrastructure
- Routers
- Wi-Fi Access Points
- Gateways
- FPGA Based Systems
- General Embedded

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1.0 PREFACE

1.1 General Terms

TABLE 1-1: GENERAL TERMS

Term	Description
1000BASE-T	1 Gbps Ethernet over twisted pair, IEEE 802.3 compliant
100BASE-TX	100 Mbps Ethernet over twisted pair, IEEE 802.3 compliant
10BASE-T	10 Mbps Ethernet over twisted pair, IEEE 802.3 compliant
10BASE-Te	Energy-efficient version of 10BASE-T, IEEE 802.3 compliant
ADC	Analog-to-Digital Converter
AFE	Analog Front End
AGC	Automatic Gain Control
AN	Auto-Negotiation
AWG	Additive White Gaussian
BC	IEEE-1588 Boundary Clock
BER	Bit Error Rate
Byte	8 bits
CF	IEEE-1588 Correction Field
DPLL	Digital Phase-Locked Loop
DCQ	Dynamic Channel Quality
DSP	Digital Signal Processing
E2E TC	IEEE-1588 End to End TC
EDPD	Energy-Detect Power-Down
EEC	Ethernet Equipment Clock
EEE	Energy Efficient Ethernet
EMI	Electromagnetic interference
ePPS	Embedded Pulse Per Second
FCS	Frame Check Sequence
FIFO	First In First Out buffer
FLF	Fast Link Failure
FLP	Fast Link Pulse
GMII	Gigabit Media Independent Interface
GPIO	General Purpose I/O

TABLE 1-1: GENERAL TERMS (CONTINUED)

Term	Description
HBM	Human Body Model. Simulates ESD from humans.
Host	External System (includes processor, application software, etc.)
ISI	Inter-symbol interference
JTP	Jitter Test Pattern
LDO	Linear Drop-Out regulator
LFSR	Linear Feedback Shift Register
LPI	Low Power Idle
LSB	Least significant byte
LTC	IEEE-1588 Local Time Counter
MAC	Media Access Controller
MCH	Microchip Control Header, proprietary extension to PCH
MDI	Medium Dependent Interface
MDIO	Management Data Input/Output
MDIX	Media Dependent Interface with crossover
MII	Media Independent Interface
MLT-3	Multi-Level Transmission Encoding (3-levels). A tri-level encoding method where a change in the logic level represents a code bit "1" and the logic output remaining at the same level represents a code bit "0"
N/A	Not Applicable
NC	No Connect
NLP	Normal Link Pulse
MMD	MDIO Manageable Device
MSE	Mean Squared Error
OC	IEEE-1588 Ordinary Clock
OCXO	Oven Controlled Crystal (Xtal) Oscillator
PAM5	5-level Pulse Amplitude Modulation
P2P TC	IEEE-1588 Peer to Peer TC
PCH	Packet Control Header, standard format
PCS	Physical Coding Sublayer
PEC	Packet-based Equipment Clock
PHY	Physical layer

TABLE 1-1: GENERAL TERMS (CONTINUED)

Term	Description
PLL	Phase-Locked Loop
POR	Power On Ready
PTP	Precision Time Protocol
SGMII	Serial Gigabit Media Independent Interface
RESERVED	Refers to a reserved bit field or address. Unless otherwise noted, reserved bits must always be zero for write operations. Unless otherwise noted, values are not guaranteed when reading reserved bits. Unless otherwise noted, do not read or write to reserved addresses.
SerDes	Serializer/Deserializer
SFD	Start of Frame Delimiter. The 8-bit value indicating the end of the preamble of an Ethernet frame.
SMD	Start mPacket Delimiter
SNR	Signal to Noise Ratio
SoC	System-on-Chip
SOF	Start of Frame
SPD	Start of Packet Delimiter. Used in SGMII
	Software Power-Down
SPI	Serial Peripheral Interface
SQI	Signal Quality Index
TC	IEEE-1588 Transparent Clock. See E2E TC and P2P TC.
TDR	Time Domain Reflectometry
TOD	Time Of Day
TQFP	Thin Quad Flat Pack
TS	Timestamp
TSN	Time Sensitive Networking
TSU	Time Stamp Unit
UDP	User Datagram Protocol. A connectionless protocol run on top of IP networks.
UTP	Unshielded Twisted Pair

1.2 Buffer Types

TABLE 1-2: BUFFER TYPE DESCRIPTIONS

Buffer	Description
AI	Analog input
AO	Analog output
AIO	Analog bidirectional
GND	Ground pin
ICLK	Crystal oscillator input pin
OCLK	Crystal oscillator output pin
SRL	Slew Rate Limited output
VIS	Variable voltage Schmitt-triggered input
VO4	Variable voltage output with 4 mA sink and 4 mA source
VOD4	Variable voltage open-drain output with 4 mA sink
VO12	Variable voltage output with 12 mA sink and 12 mA source
VOD12	Variable voltage open-drain output with 12 mA sink
VOS4	Variable voltage open-source with 4 mA source
PU	70 k Ω (typical) internal pull-up. Unless otherwise noted in the pin description, internal pull-ups are always enabled. Note: Internal pull-up resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled high, an external resistor must be added.
PD	70 k Ω (typical) internal pull-down. Unless otherwise noted in the pin description, internal pull-downs are always enabled. Note: Internal pull-down resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled low, an external resistor must be added.
P	Power pin

Note: Digital signals are not 5V tolerant unless specified.

1.3 Reference Documents

1. *IEEE Standard for Ethernet*, IEEE 802.3-2022, <https://standards.ieee.org/ieee/802.3/10422/>
2. *IEEE Standard for a Precision Clock Synchronization Protocol for Networked Measurement and Control Systems*, IEEE 1588-2008, <https://standards.ieee.org/standard/1588-2008.html>
3. *IEEE Standard for Ethernet Amendment 5: Specification and Management Parameters for Interspersing Express Traffic*, IEEE 802.3br™-2016, https://standards.ieee.org/standard/802_3br-2016.html
4. *IEEE Standard for Local and Metropolitan Area Networks Bridges and Bridged Networks Amendment 26: Frame Preemption*, IEEE 802.1Qbu™-2016, https://standards.ieee.org/standard/802_1Qbu-2016.html
5. *ITU-T Timing and Synchronization Aspects in Packet Networks*, ITU-T G.8261 08/2013, <https://www.itu.int/rec/T-REC-G.8261>
6. *Cisco SGMII Specification*, ENG-46158 Rev 1.8

The LAN8842 is designed for two primary target applications:

- [Switch Application](#)
- [SoC Application](#)

Figure 2-2 details a 50 Gbps industrial Ethernet switch configuration example that is based on the Microchip VSC7546 SparX-5i, two LAN88x4 PHYs, and two LAN8842 PHYs. This 4x10G + 10x1G is an example configuration for the 64 Gbps Switch SKU. The SparX-5i industrial Ethernet switch family is available in 64 Gbps through 200 Gbps and supports Q/USGMII and SGMII serial interfaces.

FIGURE 2-2: SWITCH APPLICATION

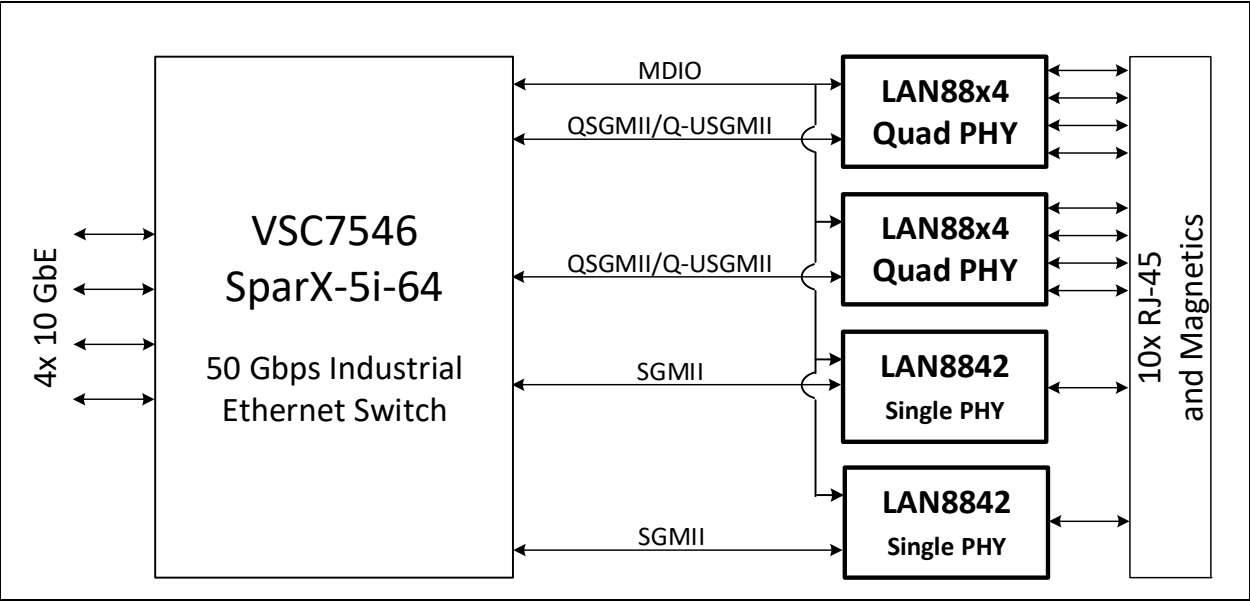
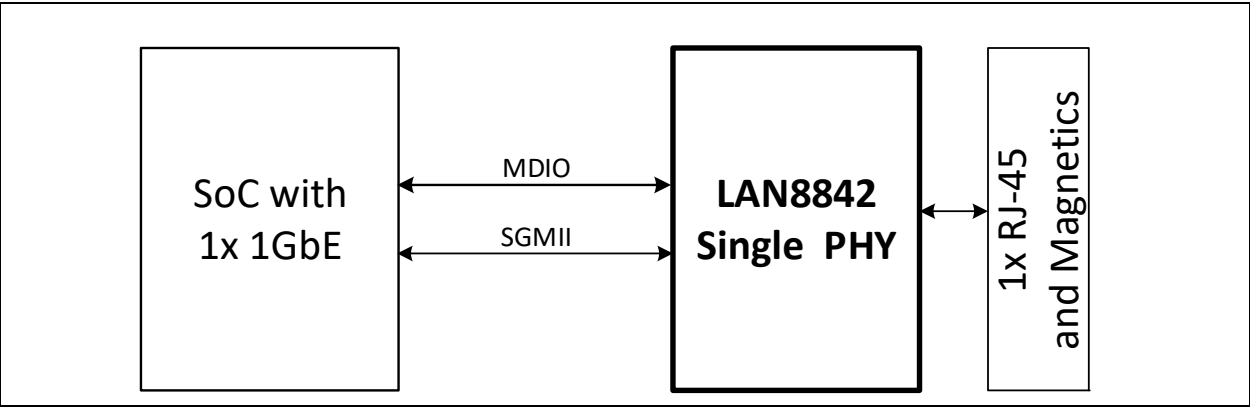


Figure 2-3 details a typical 1 Gbps industrial Ethernet System-on-Chip (SoC) application using a single LAN8842 PHY.

FIGURE 2-3: SOC APPLICATION



3.0 PIN DESCRIPTIONS AND CONFIGURATION

3.1 Pin Assignments

FIGURE 3-1: PIN ASSIGNMENTS (TOP VIEW)

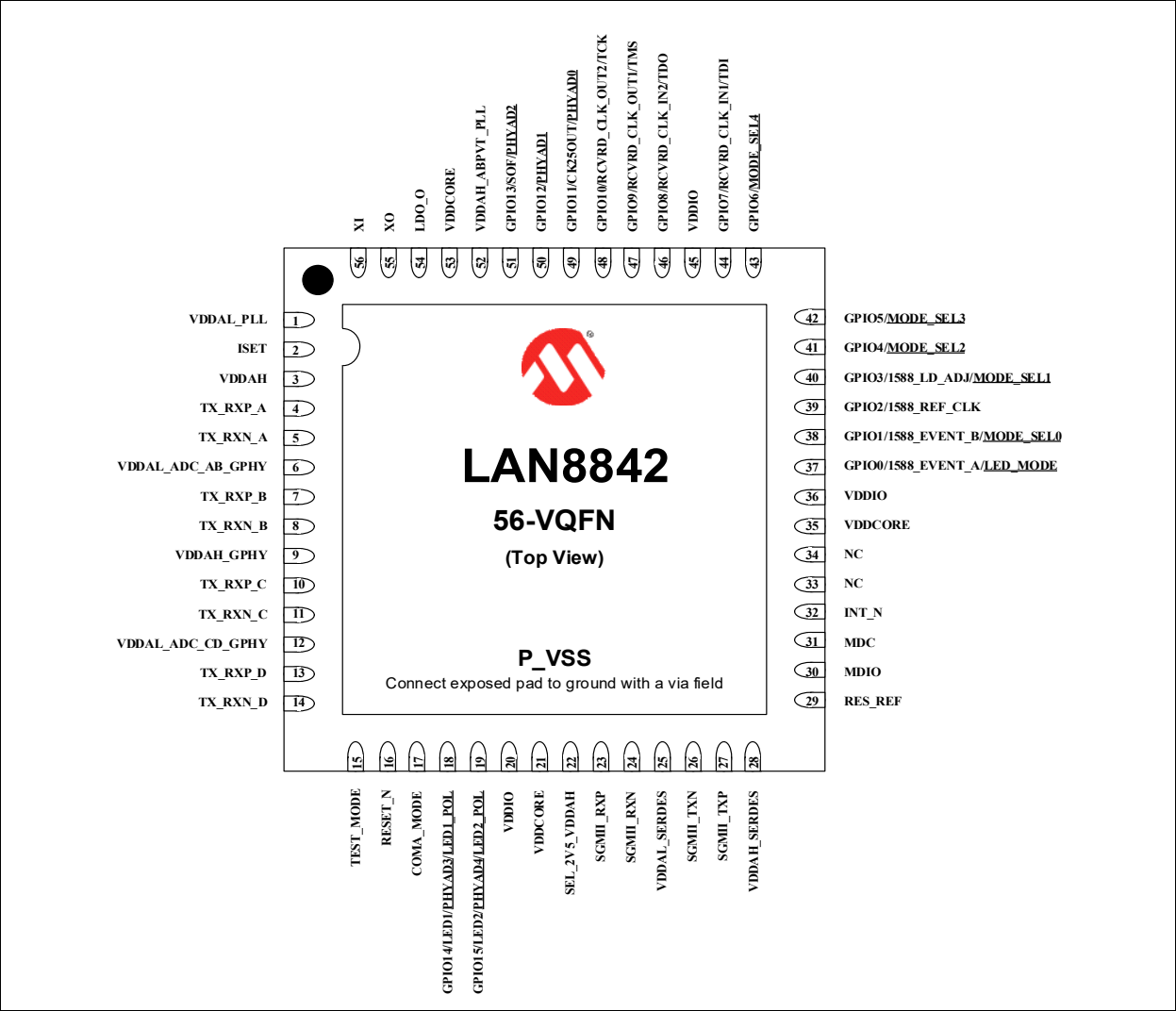


TABLE 3-1: PIN ASSIGNMENTS

Pin Num.	Pin Name	Pin Num.	Pin Name
1	VDDAL_PLL	29	RES_REF
2	ISET	30	MDIO
3	VDDAH	31	MDC
4	TX_RXP_A	32	INT_N
5	TX_RXN_A	33	NC
6	VDDAL_ADC_AB_GPHY	34	NC
7	TX_RXP_B	35	VDDCORE
8	TX_RXN_B	36	VDDIO
9	VDDAH_GPHY	37	GPIO0/1588_EVENT_A/LED_MODE
10	TX_RXP_C	38	GPIO1/1588_EVENT_B/MODE_SEL0
11	TX_RXN_C	39	GPIO2/1588_REF_CLK
12	VDDAL_ADC_CD_GPHY	40	GPIO3/1588_LD_ADJ/MODE_SEL1
13	TX_RXP_D	41	GPIO4/MODE_SEL2
14	TX_RXN_D	42	GPIO5/MODE_SEL3
15	TEST_MODE	43	GPIO6/MODE_SEL4
16	RESET_N	44	GPIO7/RCVRD_CLK_IN1/TDI
17	COMA_MODE	45	VDDIO
18	GPIO14/LED1/PHYAD3/LED1_POL	46	GPIO8/RCVRD_CLK_IN2/TDO
19	GPIO15/LED2/PHYAD4/LED2_POL	47	GPIO9/RCVRD_CLK_OUT1/TMS
20	VDDIO	48	GPIO10/RCVRD_CLK_OUT2/TCK
21	VDDCORE	49	GPIO11/CK25OUT/PHYAD0
22	SEL_2V5_VDDAH	50	GPIO12/PHYAD1
23	SGMII_RXP	51	GPIO13/SOF/PHYAD2
24	SGMII_RXN	52	VDDAH_ABPVT_PLL
25	VDDAL_SERDES	53	VDDCORE
26	SGMII_TXN	54	LDO_O
27	SGMII_TXP	55	XO
28	VDDAH_SERDES	56	XI
Exposed Pad (P_VSS) must be connected to ground.			

3.2 Pin Descriptions

This section contains descriptions of the various LAN8842 pins. The “_N” symbol in the signal name indicates that the active, or asserted, state occurs when the signal is at a low voltage level. For example, **RESET_N** indicates that the reset signal is active low. When “_N” is not present after the signal name, the signal is asserted when at the high voltage level. The pin buffer type definitions are detailed in [Section 1.2, "Buffer Types"](#).

The pin function descriptions have been broken into functional groups as follows:

- [Ethernet Media Interface Pins](#)
- [SGMII Interface Pins](#)
- [System Clock and Synchronous Ethernet Pins](#)
- [IEEE 1588 Pins](#)
- [Miscellaneous Pins](#)
- [Configuration Strap Input Pins](#)
- [Power and Ground Pins](#)

TABLE 3-2: ETHERNET MEDIA INTERFACE PINS

Name	Symbol	Buffer Type	Description
TX/RX Positive Channel A	TX_RXP_A	AIO	Channel A positive signal of differential pair
TX/RX Negative Channel A	TX_RXN_A	AIO	Channel A negative signal of differential pair
TX/RX Positive Channel B	TX_RXP_B	AIO	Channel B positive signal of differential pair
TX/RX Negative Channel B	TX_RXN_B	AIO	Channel B negative signal of differential pair
TX/RX Positive Channel C	TX_RXP_C	AIO	Channel C positive signal of differential pair
TX/RX Negative Channel C	TX_RXN_C	AIO	Channel C negative signal of differential pair
TX/RX Positive Channel D	TX_RXP_D	AIO	Channel D positive signal of differential pair
TX/RX Negative Channel D	TX_RXN_D	AIO	Channel D negative signal of differential pair

TABLE 3-3: SGMII INTERFACE PINS

Name	Symbol	Buffer Type	Description
SGMII Transmitter Output Positive	SGMII_TXP	AO	SGMII PHY to MAC positive signal of differential pair
SGMII Transmitter Output Negative	SGMII_TXN	AO	SGMII PHY to MAC negative signal of differential pair
SGMII Receiver Input Positive	SGMII_RXP	AI	SGMII MAC to PHY positive signal of differential pair
SGMII Receiver Input Negative	SGMII_RXN	AI	SGMII MAC to PHY negative signal of differential pair

TABLE 3-4: SYSTEM CLOCK AND SYNCHRONOUS ETHERNET PINS

Name	Symbol	Buffer Type	Description
Crystal Input / System Reference Clock Input	XI	ICLK	When using a 25 MHz crystal, this input is connected to one lead of the crystal. When using a 25 MHz system reference clock, this is the input from the external 25 MHz oscillator.
Crystal Output	XO	OCLK	When using a 25 MHz crystal, this output is connected to one lead of the crystal. When using a 25 MHz system reference clock source, this pin is not connected.
System Clock Output	CK25OUT	VO4 (PD)	Buffered copy of GPHY internal 25 MHz reference clock. This pin is shared with other functions.
Recovered Clock Output 1	RCVRD_CLK_OUT1	SRL (PD)	Recovered clock output 2.5, 25, or 125 MHz. Can be configured to always output 2.5 MHz regardless of the PHY speed. This pin is shared with other functions.
Recovered Clock Output 2	RCVRD_CLK_OUT2	SRL (PD)	Recovered clock output 2.5, 25, or 125 MHz. Can be configured to always output 2.5 MHz regardless of the PHY speed. This pin is shared with other functions.
Recovered Clock Input 1	RCVRD_CLK_IN1	VIS (PD)	Recovered clock input 2.5, 25, or 125 MHz. This pin is shared with other functions.
Recovered Clock Input 2	RCVRD_CLK_IN2	VIS (PD)	Recovered clock input 2.5, 25, or 125 MHz. This pin is shared with other functions.

TABLE 3-5: IEEE 1588 PINS

Name	Symbol	Buffer Type	Description
1588 Load/Adjust Input	1588_LD_ADJ	VIS (PD)	This input controls loading and adjusting of the 1588 LTC. This pin is shared with other functions.
1588 Reference Clock Input	1588_REF_CLK	VIS (PD)	10, 25, or 125 MHz. This input optionally supports ePPS format, where the PPS is combined with the clock. This pin is shared with other functions.
1588 LTC Event A	1588_EVENT_A	SRL (PD)	When asserted, this pin signals that 1588 LTC Event A has occurred. This pin can also be configured to provide a 1588 PPS Out. This pin is shared with other functions.
1588 LTC Event B	1588_EVENT_B	SRL (PD)	When asserted, this pin signals that 1588 LTC Event B has occurred. This pin can also be configured to provide a 1588 PPS Out. This pin is shared with other functions.

TABLE 3-6: MISCELLANEOUS PINS

Name	Symbol	Buffer Type	Description
Management Interface Clock	MDC	VIS	PHY Management clock input.
Management Interface Data	MDIO	VIS/ VO12 VOD12	PHY Management data interface. Note: An external pull-up resistor to VDDIO in the range of 1.0 kΩ to 4.7 kΩ is required (1.0 kΩ for high-speed MDIO operation). The buffer type (push-pull or open-drain/open-source) depends on the setting of the MDIO Buffer Type bit in the Output Control register, as well as the <code>disable_mdo_drv</code> bit in direct register 17.
PHY Interrupt	INT_N	VO4/ VOD4 (PU)	Programmable interrupt output. The buffer type (push-pull or open-drain) depends on the setting of the INT Buffer Type bit in the Output Control register and defaults to open-drain. The polarity depends on the setting of the Intr Polarity Invert bit in the Control register and defaults to active low.
Start of Frame Pin	SOF	SRL (PD)	RX and TX Start of Frame indicator. A pulse indicates Start of Frame is detected on the selected transmit or receive port. Pin can be configured via the GPIO SOF Select register. This pin is shared with other functions.
General Purpose I/O	GPIO[15:0]	VIS/VO4/ VOD4 (PD)	General purpose I/O. These I/Os are shared with various other functions. The buffer type (push-pull or open-drain/open-source), direction, and pull-down/pull-up depend on the settings in the GPIO registers. Note: GPIO[6:5] are pulled up so MODE_SEL[4:3] defaults to 11000.
System Reset	RESET_N	VIS (PU)	Chip reset (active low). At power-up, RESET_N must not be deasserted until all power and clocks have been stable for the specified minimum duration. Hardware pin configurations are strapped-in at the de-assertion (rising edge) of RESET_N . See Table 3-8, "Configuration Strap Input Pins" for details.
LED 1	LED1	VO4/ VOD4/ VOS4 (PD)	Programmable LED 1 output. The polarity of this pin depends on the LED1_POL configuration strap which is shared with this pin.
LED 2	LED2	VO4/ VOD4/ VOS4 (PD)	Programmable LED 2 output. The polarity of this pin depends on the LED2_POL configuration strap which is shared with this pin.
Coma Mode Control	COMA_MODE	VIS (PD)	Drive high to activate Coma mode. After port is configured, drive low to enable normal operation. Hold low to disable this feature.

TABLE 3-6: MISCELLANEOUS PINS (CONTINUED)

Name	Symbol	Buffer Type	Description
Voltage Regulator Bypass for SerDes, Temperature Monitor, and 1588 PLL	SEL_2V5_VDDAH	VIS (PD)	Voltage regulator bypass for SerDes, Temperature Monitor, and 1588 PLL: 0: SerDes, Temperature Monitor, and 1588 PLL powered from 3.3V VDDAH_SERDES and VDDAH_ABPVT_PLL , using internal 3.3V to 2.5V regulators 1: SerDes, Temperature Monitor, and 1588 PLL powered directly from 2.5V VDDAH_SERDES and VDDAH_ABPVT_PLL (regulators bypassed) Note: This pin must be permanently tied high/low.
LDO Controller Output	LDO_O	AO	On-chip +1.1V LDO controller output. This pin drives the input gate of a P-channel MOSFET to generate +1.1V for the device's core voltages. Note: If the system provides 1.1V, this pin is not used and can be left unconnected.
SerDes Bias Resistor	RES_REF	AI	This pin must be connected to ground through a 200Ω 1% 100 ppm/°C resistor.
PHY Bias Resistor	ISET	AI	This pin must be connected to ground through a 6.04 kΩ 1% resistor.
Test Mode	TEST_MODE	VIS (PD)	For normal operation, this pin must be pulled-down to ground.
No Connect	NC	-	For normal operation, this pin must be left unconnected.

TABLE 3-7: JTAG PINS

Name	Symbol	Buffer Type	Description
JTAG Mux Select	TMS	SRL	JTAG test mode select
JTAG Clock	TCK	SRL	JTAG test clock
JTAG Data Input	TDI	SRL	JTAG data input
JTAG Data Output	TDO	SRL	JTAG data output

TABLE 3-8: CONFIGURATION STRAP INPUT PINS

Name	Symbol	Buffer Type	Description
PHY Base Address Configuration Straps	<u>PHYAD[4:0]</u>	VIS (PD)	Configures the PHY Management base address, used with MDIO bus transactions. The PHY base address, <u>PHYAD[4:0]</u> , is sampled and latched at power-up/reset and is configurable to any value from 0 to 1Fh. Each PHY address bit is configured as follows: Pulled-up = 1 Pulled-down = 0 Note: Refer to Section 3.3.2, "PHY Address (PHYAD[4:0])" for additional information.

TABLE 3-8: CONFIGURATION STRAP INPUT PINS (CONTINUED)

Name	Symbol	Buffer Type	Description
LED Polarity Configuration Straps	<u>LED1_POL</u> <u>LED2_POL</u>	VIS (PD)	Configures LED polarity as Active High or Active Low. Since the LED pins are shared with configuration straps, the default polarity of the LED pins is determined during strap loading. If the strap value on a pin is a 0, the LED is set as active high (LED_x_POL=1), since it is assumed that a LED to ground is used as the pull-down. If the strap value on a pin is 1, the LED is set as active low (LED_x_POL=0), since it is assumed that a LED to VDDIO is used as the pull-up. Note: When using a LED as a pull-down/pull-up strap, an external supplemental resistor may be needed to ensure a valid high or low level. Refer to Section 3.3.4, "LED Polarity (LED[2:1]_POL)" for additional information.
Device Mode Configuration Straps	<u>MODE_SEL[4:0]</u>	VIS	Configures the specific functional mode of the PHY. The MODE[4:0] configuration straps are sampled and latched at power-up/reset and are defined in Section 3.3.1, "Device Mode Select (MODE_SEL[4:0])".
LED Mode Configuration Strap	<u>LED_MODE</u>	VIS (PD)	Configures the device's LED behavior as Individual or Tri-Color. Both LEDs are configured with identical behavior. The LED_MODE configuration strap is sampled and latched at power-up/reset and is defined as follows: 0: Tri-color-LED mode 1: Individual-LED mode Refer to Section 3.3.3, "LED Mode Select (LED_MODE)" for additional information.

TABLE 3-9: POWER AND GROUND PINS

Name	Symbol	Buffer Type	Description
+3.3/2.5V Analog Power Supply	VDDAH	P	+3.3/2.5V analog I/O power supply. Note: VDDAH, VDDAH_GPHY, VDDAH_SERDES, and VDDAH_ABPVT_PLL must operate at the same voltage.
+3.3/2.5V GPHY Analog Power Supply	VDDAH_GPHY	P	+3.3/2.5V GPHY analog I/O power supply. Note: VDDAH, VDDAH_GPHY, VDDAH_SERDES, and VDDAH_ABPVT_PLL must operate at the same voltage.
+3.3/2.5V SerDes Analog Power Supply	VDDAH_SERDES	P	+3.3/2.5V SerDes analog I/O power supply. Note: VDDAH, VDDAH_GPHY, VDDAH_SERDES, and VDDAH_ABPVT_PLL must operate at the same voltage.
+3.3/2.5V Analog Power Supply	VDDAH_ABPVT_PLL	P	+3.3/2.5V analog I/O power supply. Note: VDDAH, VDDAH_GPHY, VDDAH_SERDES, and VDDAH_ABPVT_PLL must operate at the same voltage.
+1.1V GPHY Analog Power Supply	VDDAL_ADC_AB_GPHY	P	+1.1V GPHY analog power supply
+1.1V GPHY Analog Power Supply	VDDAL_ADC_CD_GPHY	P	+1.1V GPHY analog power supply
+1.1V Analog Power Supply	VDDAL_PLL	P	+1.1V analog power supply
+1.1V SerDes Analog Power Supply	VDDAL_SERDES	P	+1.1V SerDes analog power supply
+3.3/2.5/1.8V Variable I/O Power Supply Input	VDDIO	P	+3.3/2.5/1.8V variable I/O digital power supply input. Note: All VDDIO pins must operate at the same voltage.
+1.1V Digital Core Power Supply Input	VDDCORE	P	+1.1V digital core power supply input.
Paddle Ground	P_VSS	GND	Common ground. This exposed paddle must be connected to the ground plane with a via array.

3.3 Configuration Straps

Configuration straps allow various features of the device to be automatically configured to user defined values. Configuration straps are latched upon the release of pin reset (**RESET_N**). Configuration straps do not include internal resistors and require the use of external resistors.

Note: The system designer must ensure that configuration strap pins meet timing requirements. Configuration strap pins not set at the correct voltage level prior to being latched may capture incorrect strap values.

Note: When externally pulling configuration straps high, the strap must be tied to **VDDIO**.

APPLICATION NOTE: All straps must be pulled-up or pulled-down externally on the PCB to enable the desired operational state.

3.3.1 DEVICE MODE SELECT (**MODE_SEL[4:0]**)

The **MODE_SEL[4:0]** configuration straps select the device mode as follows:

Note: 1000BT Half Duplex is not advertised in any of the below device modes.

Note: When no strap-based configured is wanted, it is recommended to set **MODE_SEL[4:0]** to either 0x18 (single-port system) or 0x19 (multi-port system). Both values enable 1000FD 100FD/HD 10FD/HD with EEE.

TABLE 3-10: DEVICE MODE SELECTIONS

Legend:	
1000FD = 1000BASE-T Full Duplex	
100FD = 100BASE-TX Full Duplex	
100HD = 100BASE-TX Half Duplex	
10FD = 10BASE-T Full Duplex	
10HD = 10BASE-T Half Duplex	
"X" means "is advertised by auto-negotiation" (for example 10BT FD and 10BT HD are both available auto-negotiation results when MODE_SEL = 10000).	
Test Modes	
MODE_SEL [4:0]	Mode
00010	RESERVED
00011	RESERVED
00100	RESERVED
00101	RESERVED
00110	RESERVED
00111	RESERVED
Functional Modes	
Power Down	
01000	Software Power Down PLL Enabled
01001	RESERVED
Auto-Negotiation Disabled, Auto MDIX Disabled, EEE Disabled	
01010	1000FD Master
01011	100FD
01100	100HD

TABLE 3-10: DEVICE MODE SELECTIONS (CONTINUED)

Auto-Negotiation Enabled, Auto MDIX Enabled, EEE Disabled, Asym and Sym Pause												
		Auto-Negotiation Advertisement								10BT cat3/5	AMDIX	
		1000BT			100BT			10BT				Asym / Sym Pause
		FD	Single / Multi	EEE	FD	HD	EEE	FD	HD			
10000	1000FD Single Port 100FD/HD 10FD/HD	X	S		X	X		X	X	X	cat3	X
10001	1000FD Multi Port 100FD/HD 10FD/HD	X	M		X	X		X	X	X	cat3	X
10010	1000FD Single Port	X	S							X	N/A	X
10011	1000FD Multi Port	X	M							X	N/A	X
10100	100FD/HD				X	X				X	N/A	X
10101	100FD				X					X	N/A	X
10110	100HD					X				X	N/A	X
10111	100FD/HD 10FD/HD				X	X		X	X	X	cat3	X
Auto-Negotiation Enabled, Auto MDIX Enabled, EEE Enabled, Asym and Sym Pause												
		Auto-Negotiation Advertisement								10BT cat3/5	AMDIX	
		1000BT			100BT			10BT				Asym / Sym Pause
		FD	Single / Multi	EEE	FD	HD	EEE	FD	HD			
11000	1000FD Single Port 100FD/HD 10FD/HD	X	S	X	X	X	X	X	X	X	cat5	X
11001	1000FD Multi Port 100FD/HD 10FD/HD	X	M	X	X	X	X	X	X	X	cat5	X
11010	1000FD Single Port	X	S	X						X	N/A	X
11011	1000FD Multi Port	X	M	X						X	N/A	X
11100	100FD/HD				X	X	X			X	N/A	X
11101	100FD				X		X			X	N/A	X
11111	100FD/HD 10FD/HD				X	X	X	X	X	X	cat5	X
RESERVED												
00000	RESERVED											
00001	RESERVED											
01101	RESERVED											
01110	RESERVED											
01111	RESERVED											
11110	RESERVED											

3.3.2 PHY ADDRESS (**PHYAD[4:0]**)

The **PHYAD[4:0]** configuration straps set the base value of the PHY's management address.

3.3.3 LED MODE SELECT (**LED_MODE**)

The **LED_MODE** configuration strap selects between Individual-LED (pulled-up) or Tri-color-LED (pulled-down)

modes. The two LEDs are configured with identical behavior. The **LED_MODE** configuration strap is sampled and latched at power-up/reset and is defined as follows:

0: Tri-color-LED mode

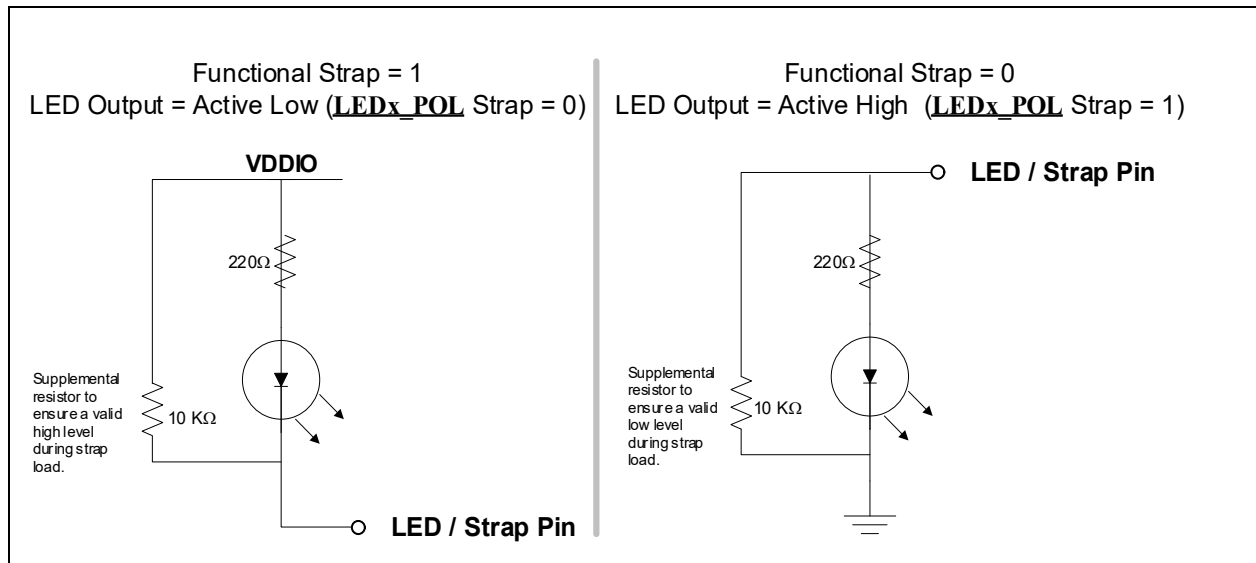
1: Individual-LED mode

LED operation is described in [Section 5.21, "LEDs"](#).

3.3.4 LED POLARITY (**LED[2:1]_POL**)

The **LED[2:1]_POL** configuration straps set the default polarity of the LED pins. When a LED pin is used as a function mode strap (for example a PHY address bit), the default LED pin polarity is automatically selected based on the inverse of the strap value. A LED, via a resistor, is then used as a pull-up or pull-down. This is shown in [Figure 3-2](#).

FIGURE 3-2: STRAP ON LED WITH POLARITY



4.0 DEVICE CONNECTIONS

The following example device connection information and diagrams are included in this section:

- [Voltage Regulator and Power Connections](#)
- [Ethernet Media Interface](#)

4.1 Voltage Regulator and Power Connections

The LAN8842 integrates an optional LDO controller for use with an external P-channel MOSFET to generate the 1.1V supply from an existing 2.5V or 3.3V source. Use of the LDO controller and MOSFET is not required.

Note: An external 1.1V supply can be alternatively utilized.

The SerDes, PVT Monitor, and 1588 PLL are all configurable to run from 2.5V or 3.3V power, as determined by the `SEL_2V5_VDDAH` input pin. The `VDDAH_SERDES` and `VDDAH_ABPVT_PLL` pins must always be at the same voltage (2.5V or 3.3V).

Note: The SerDes and PVT Monitor make use of the `SEL_2V5_VDDAH` pin, whereas the 1588 PLL does not require this pin.

4.1.1 MOSFET SELECTION

The selected MOSFET should exceed the following minimum requirements:

- P-channel
- 500 mA (continuous current)
- 3.3V or 2.5V (source – input voltage)
- 1.1V (drain – output voltage)

The V_{GS} for the MOSFET must be operating in the constant current saturated region and not towards the threshold voltage for the cut-off region of the MOSFET, $V_{GS(th)}$.

A capacitor between 1.1V and ground is required for proper LDO operation.

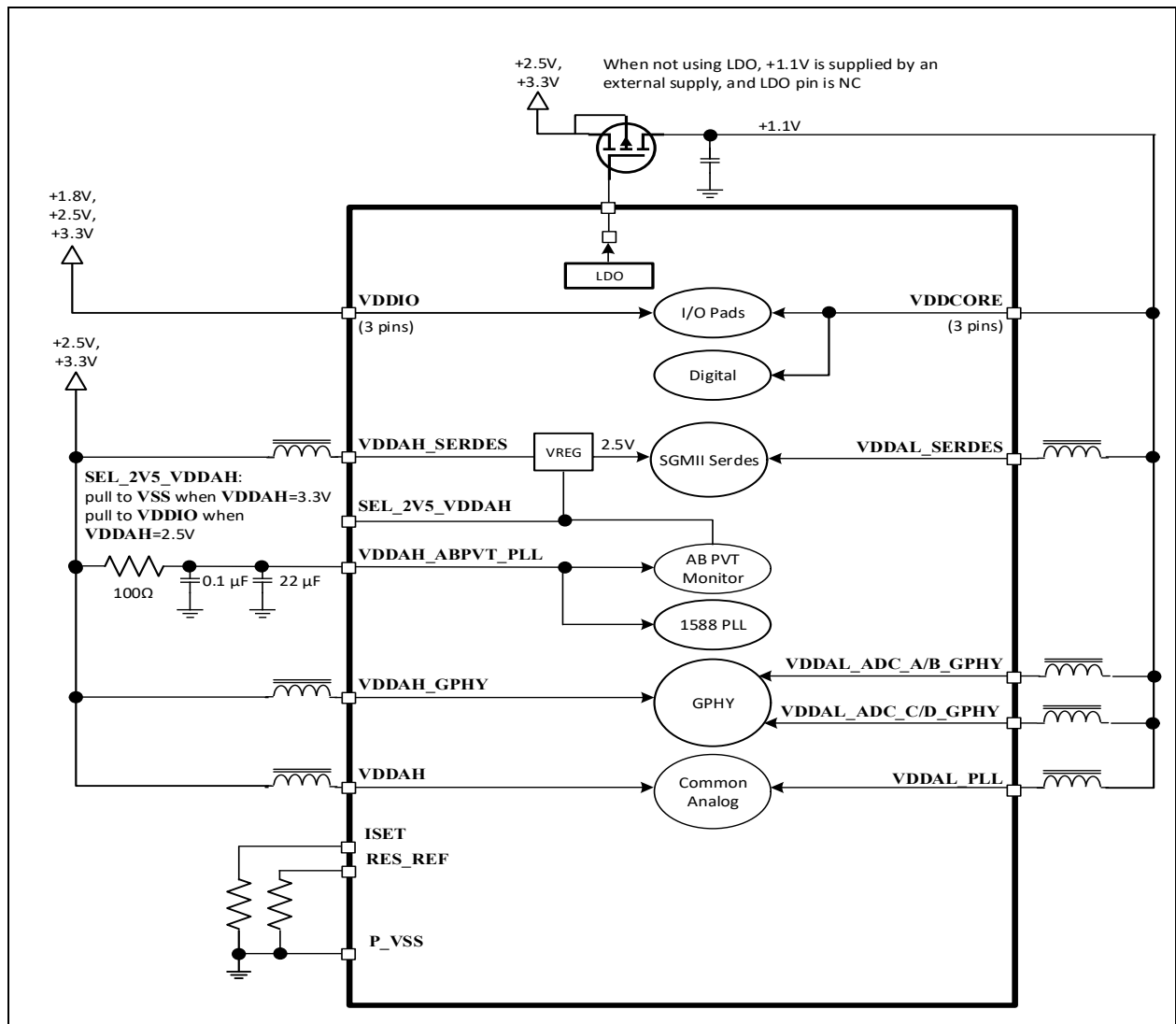
4.1.2 LDO DISABLE

The LDO controller is enabled by default. It may alternatively be disabled via internal register settings, by setting the LDO Enable bit to 1 in the EP 29 Analog Control Register 11. An external source of 1.1V is necessary if the LDO is disabled.

4.1.3 POWER CONNECTIONS

[Figure 4-1](#) illustrates the device power connections.

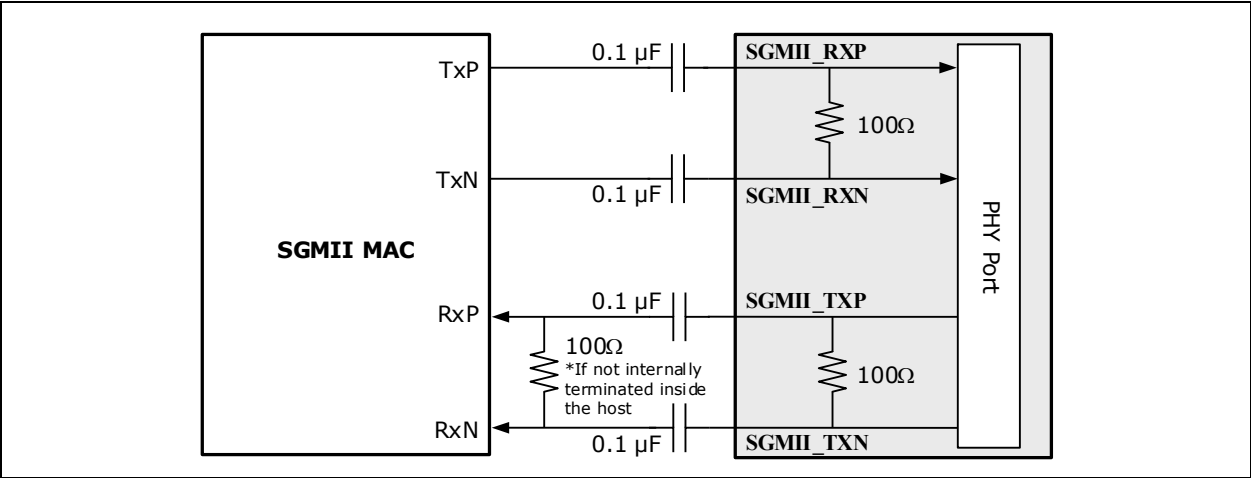
FIGURE 4-1: POWER CONNECTIONS



4.2 SGMII MAC Interface

Figure 4-3 illustrates the device SGMII MAC interface connections.

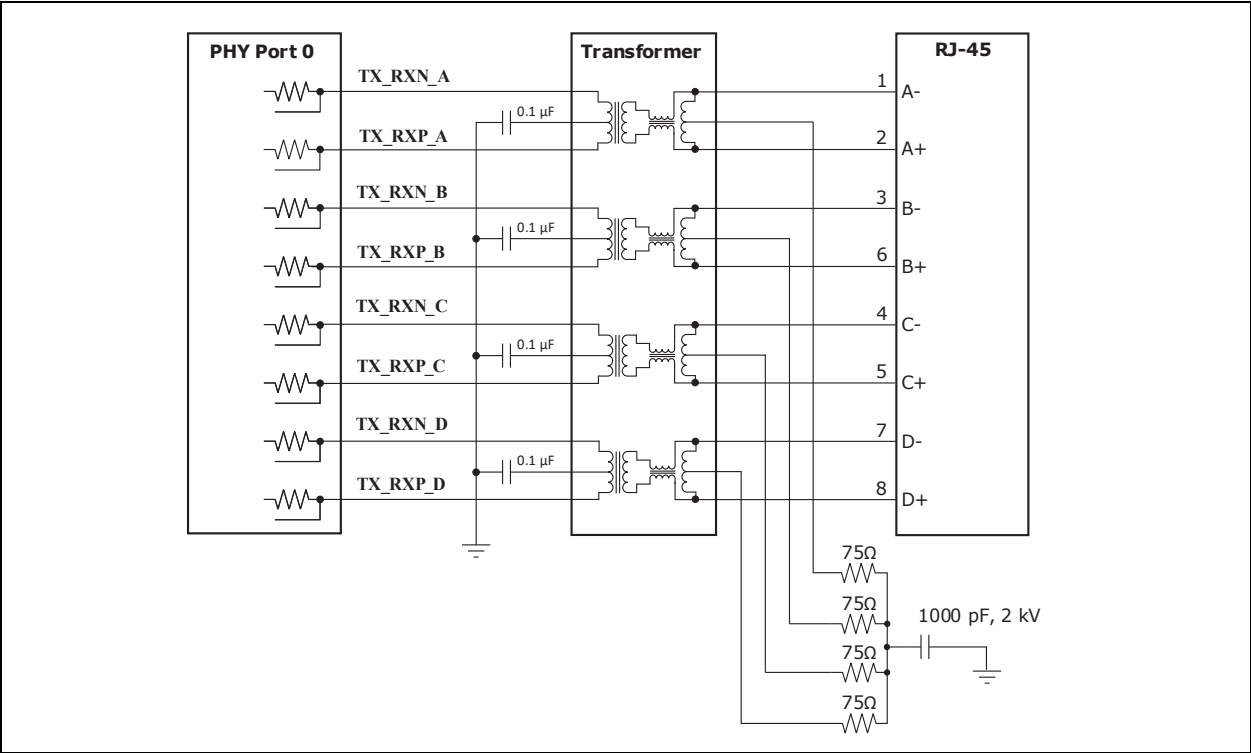
FIGURE 4-2: SGMII MAC INTERFACE CONNECTIONS



4.3 Ethernet Media Interface

Figure 4-3 illustrates the device Ethernet media interface connections.

FIGURE 4-3: ETHERNET MEDIA INTERFACE CONNECTIONS



Note: The device supports integrated connector magnetics with ganged center taps.

5.0 FUNCTIONAL DESCRIPTIONS

This section provides additional details of the major features supported by the LAN8842:

- 10BASE-T/100BASE-TX Transceiver
- 1000BASE-T Transceiver
- Auto MDI/MDIX (Pair-Swap)
- Alignment and Polarity Detection/Correction
- Wave Shaping, Slew-Rate Control, and Partial Response
- Auto-Negotiation
- Signal Quality Index
- LinkMD Cable Diagnostics
- Auto-Downshift
- SGMII
- PLL/Clocks and Resets
- Synchronous Ethernet
- IEEE 1588 (PTP)
- Energy Efficient Ethernet (EEE)
- IEEE 802.3-2022 Frame Preemption
- Loopbacks
- Start of Frame Indication
- MIIM (MDIO) Interface
- Interrupts
- GPIOs
- LEDs
- ActiPHY Power Management
- JTAG
- Coma Mode

5.1 10BASE-T/100BASE-TX Transceiver

5.1.1 100BASE-TX TRANSMIT

The 100BASE-TX transmit function performs parallel-to-serial conversion, 4B/5B coding, scrambling, NRZ-to-NRZI conversion, and MLT-3 encoding and transmission.

The circuitry starts with a parallel-to-serial conversion, which converts the MII data from the MAC into a 125 MHz serial bit stream. The data and control stream is then converted into 4B/5B coding, followed by a scrambler. The serialized data is further converted from NRZ-to-NRZI format, and then transmitted in MLT-3 current output. The output current is set by an external 6.04 k Ω 1% resistor for the 1:1 transformer ratio.

The output signal has a typical rise/fall time of 4 ns and complies with the ANSI TP-PMD standard regarding amplitude balance, and overshoot. The wave-shaped 10BASE-T output is also incorporated into the 100BASE-TX transmitter.

5.1.2 100BASE-TX RECEIVE

The 100BASE-TX receiver function performs adaptive equalization, DC restoration, MLT-3-to-NRZI conversion, data and clock recovery, NRZI-to-NRZ conversion, de-scrambling, 4B/5B decoding, and serial-to-parallel conversion.

The receiving side starts with the equalization filter to compensate for inter-symbol interference (ISI) over the twisted pair cable. Because the amplitude loss and phase distortion are a function of the cable length, the equalizer must adjust its characteristics to optimize performance. In this design, the variable equalizer makes an initial estimation based on comparisons of incoming signal strength against some known cable characteristics, then tunes itself for optimization. This is an ongoing process and self-adjusts against environmental changes such as temperature variations.

Next, the equalized signal goes through a DC-restoration and data-conversion block. The DC-restoration circuit compensates for the effect of baseline wander and improves the dynamic range. The differential data conversion circuit converts the MLT-3 format back to NRZI. The slicing threshold is also adaptive.

The clock-recovery circuit extracts the 125 MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal into the NRZ format. This signal is sent through the de-scrambler followed by the 4B/5B decoder. Finally, the NRZ serial data is converted to the MII/GMII or Reduced Gigabit Media Independent Interface format and provided as the input data to the MAC.

5.1.3 SCRAMBLER/DE-SCRAMBLER (100BASE-TX ONLY)

The purpose of the scrambler is to spread the power spectrum of the signal to reduce electromagnetic interference (EMI) and baseline wander. Transmitted data is scrambled using an 11-bit wide Linear Feedback Shift Register (LFSR). The scrambler generates a 2047-bit non-repetitive sequence, then the receiver de-scrambles the incoming data stream using the same sequence as at the transmitter.

5.1.4 10BASE-T TRANSMIT

The 10BASE-T output drivers are incorporated into the 100BASE-TX drivers to allow for transmission with the same magnetic. The drivers perform internal wave-shaping and pre-emphasis, and output signals with typical amplitude of 2.5V peak for standard 10BASE-T mode and 1.75V peak for energy-efficient 10BASE-Te mode. The 10BASE-T/10BASE-Te signals have harmonic contents that are at least 31 dB below the fundamental frequency when driven by an all-ones Manchester-encoded signal.

5.1.5 10BASE-T RECEIVE

On the receive side, input buffer and level-detecting squelch circuits are used. A differential input receiver circuit and a Phase-Locked Loop (PLL) perform the decoding function. The Manchester-encoded data stream is separated into clock signal and NRZ data. A squelch circuit rejects signals with levels less than 300 mV or with short pulse widths to prevent noises at the receive inputs from falsely triggering the decoder. When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the device decodes a data frame. The receiver clock is maintained active during idle periods between receiving data frames.

The device removes all 7 bytes of the preamble and presents the received frame starting with the Start of Frame Delimiter (SFD) to the MAC.

Auto-polarity correction is provided for the receiving differential pair to automatically swap and fix the incorrect $\pm$ polarity wiring in the cabling.

5.2 1000BASE-T Transceiver

The 1000BASE-T transceiver is based on a mixed-signal/digital-signal processing (DSP) architecture, which includes the analog front-end, digital channel equalizers, trellis encoders/decoders, echo cancelers, cross-talk cancelers, precision clock recovery scheme, and power-efficient line drivers.

5.2.1 ANALOG ECHO-CANCELLATION CIRCUIT

In 1000BASE-T mode, the analog echo-cancellation circuit helps to reduce the near-end echo. This analog hybrid circuit relieves the burden of the ADC and the adaptive equalizer.

This circuit is disabled in 10BASE-T/100BASE-TX mode.

5.2.2 AUTOMATIC GAIN CONTROL (AGC)

In 1000BASE-T mode, the AGC circuit provides initial gain adjustment to boost up the signal level. This pre-conditioning circuit is used to improve the signal-to-noise ratio of the receive signal.

5.2.3 ANALOG-TO-DIGITAL CONVERTER (ADC)

In 1000BASE-T mode, the ADC digitizes the incoming signal. ADC performance is essential to the overall performance of the transceiver.

This circuit is disabled in 10BASE-T/100BASE-TX mode.

5.2.4 TIMING RECOVERY CIRCUIT

In 1000BASE-T mode, the mixed-signal clock recovery circuit together with the digital PLL is used to recover and track the incoming timing information from the received data. The digital PLL has very low long-term jitter to maximize the signal-to-noise ratio of the receive signal.

The 1000BASE-T slave PHY must transmit the exact receive clock frequency recovered from the received data back to the 1000BASE-T master PHY. Otherwise, the master and slave will not be synchronized after long transmission. This also helps to facilitate echo cancellation and NEXT removal.

5.2.5 ADAPTIVE EQUALIZER

In 1000BASE-T mode, the adaptive equalizer provides the following functions:

- Detection for partial response signaling
- Removal of NEXT and ECHO noise
- Channel equalization

Signal quality is degraded by residual echo that is not removed by the analog hybrid because of impedance mismatch. The device uses a digital echo canceler to further reduce echo components on the receive signal.

In 1000BASE-T mode, data transmission and reception occurs simultaneously on all four pairs of wires (four channels). This results in high-frequency cross-talk coming from adjacent wires. The device uses three NEXT cancelers on each receive channel to minimize the cross-talk induced by the other three channels.

In 10BASE-T/100BASE-TX mode, the adaptive equalizer needs only to remove the inter-symbol interference and recover the channel loss from the incoming data.

5.2.6 TRELLIS ENCODER AND DECODER

In 1000BASE-T mode, the transmitted 8-bit data is scrambled into 9-bit symbols and further encoded into 4D-PAM5 symbols. The initial scrambler seed is determined by the specific PHY address to reduce EMI when more than one device is used on the same board. On the receiving side, the idle stream is examined first. The scrambler seed, pair skew, pair order, and polarity must be resolved through the logic. The incoming 4D-PAM5 data is then converted into 9-bit symbols and de-scrambled into 8-bit data.

5.3 Auto MDI/MDIX (Pair-Swap)

The Automatic MDI/MDI-X feature eliminates the need to determine whether to use a straight cable or a crossover cable between the device and its link partner. This auto-sense function detects the MDI/MDI-X pair mapping from the link partner, and assigns the MDI/MDI-X pair mapping of the device accordingly.

[Table 5-1](#) shows the device 10/100/1000 pin configuration assignments for MDI/MDI-X pin mapping.

TABLE 5-1: MDI/MDI-X PIN MAPPING

Pin (RJ-45 Pair)	MDI			MDI-X		
	1000BASE-T	100BASE-T	10BASE-T	1000BASE-T	100BASE-T	10BASE-T
TX_RXP/N_A_x (1, 2)	A+/-	TX+/-	TX+/-	B+/-	RX+/-	RX+/-
TX_RXP/N_B_x (3, 6)	B+/-	RX+/-	RX+/-	A+/-	TX+/-	TX+/-
TX_RXP/N_C_x (4, 5)	C+/-	Not Used	Not Used	C+/- (Note 5-1)	Not Used	Not Used
TX_RXP/N_D_x (7, 8)	D+/-	Not Used	Not Used	D+/- (Note 5-1)	Not Used	Not Used

Note 5-1 Default value is shown in the table. C pair can be swapped with D pair via register settings.

Auto-MDIX detection is enabled in the device by default.

Auto-MDIX can be disabled by setting the swapoff bit in the Digital Debug Control 1 register. The MDI/MDI-X mode may then be manually selected by the mdi_set bit in the Digital Debug Control 1 register.

The Auto-MDIX status bits are located in the Digital AX/AN Status register.

An isolation transformer with symmetrical transmit and receive data paths is recommended to support Auto MDI/MDI-X.

5.4 Alignment and Polarity Detection/Correction

In 1000BASE-T mode, the device supports 50 ns $\pm$ 10 ns difference in propagation delay between pairs of channels in accordance with the IEEE 802.3 standard, and automatically corrects the data skew so the corrected four pairs of data symbols are synchronized.

Additionally, the device detects and corrects polarity errors on all MDI pairs, a useful capability that exceeds the requirements of the standard. Polarity detection and correction applies to 10BASE-T and 1000BASE-T and is not required for 100BASE-TX.

5.5 Wave Shaping, Slew-Rate Control, and Partial Response

In communication systems, signal transmission encoding methods are used to provide the noise-shaping feature and to minimize distortion and error in the transmission channel.

- For 1000BASE-T, a special partial-response signaling method is used to provide the band-limiting feature for the transmission path.
- For 100BASE-TX, a simple slew-rate control method is used to minimize EMI.
- For 10BASE-T, pre-emphasis is used to extend the signal quality through the cable.

5.6 Auto-Negotiation

The device conforms to the auto-negotiation protocol, defined in Clause 28 of the IEEE 802.3 Specification [1].

Auto-negotiation allows UTP link partners to select the highest common mode of operation.

During auto-negotiation, link partners advertise capabilities across the UTP link to each other, and then compare their own capabilities with those they received from their link partners. The highest speed and duplex setting that is common to the two link partners is selected as the operating mode.

The following list shows the speed and duplex operation mode from highest to lowest:

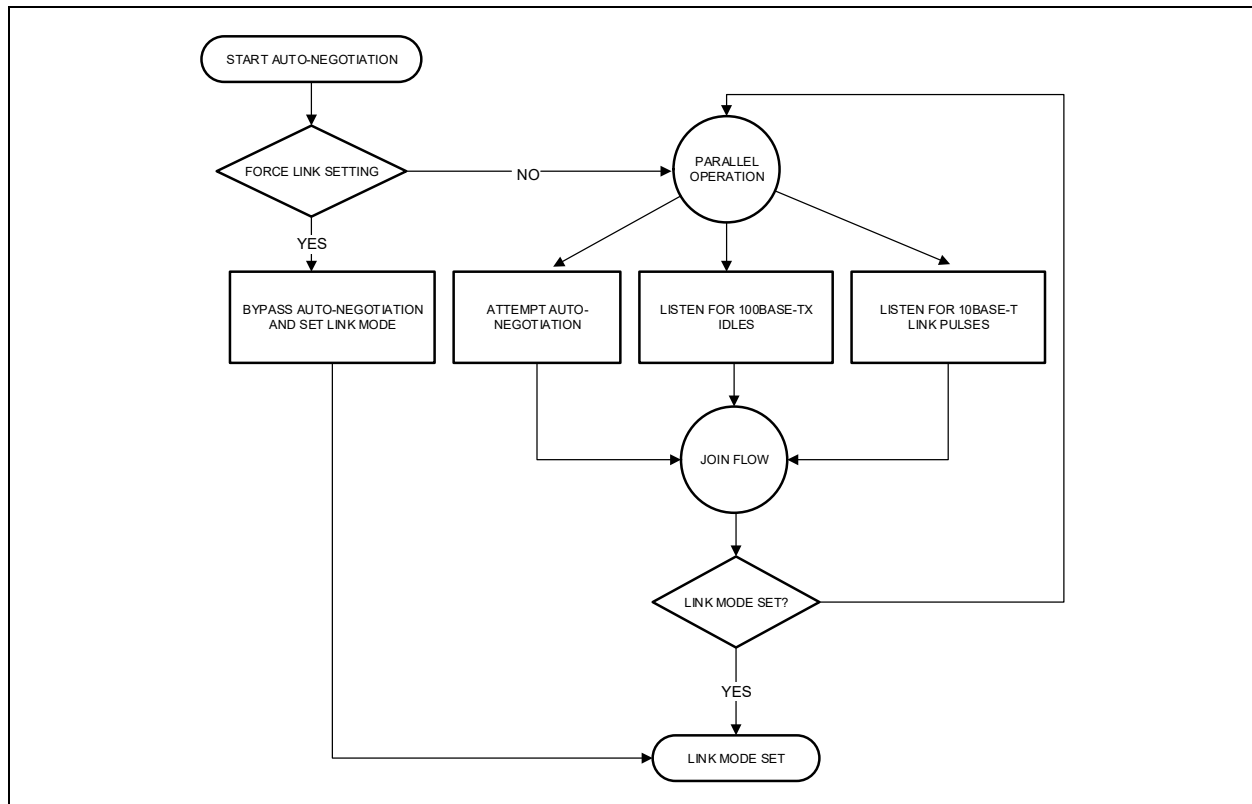
- Priority 1: 1000BASE-T, full-duplex
- Priority 2: 1000BASE-T, half-duplex ([Note 5-2](#))
- Priority 3: 100BASE-TX, full-duplex
- Priority 4: 100BASE-TX, half-duplex
- Priority 5: 10BASE-T, full-duplex
- Priority 6: 10BASE-T, half-duplex

Note 5-2 The device does not support 1000BASE-T, half-duplex and may not be enabled to advertise such.

If auto-negotiation is not supported or the device's link partner is forced to bypass auto-negotiation for 10BASE-T and 100BASE-TX modes, the device sets its operating mode by observing the input signal at its receiver. This is known as parallel detection, and allows the device to establish a link by listening for a fixed signal protocol in the absence of the auto-negotiation advertisement protocol.

The auto-negotiation link-up process is shown in [Figure 5-1](#).

FIGURE 5-1: AUTO-NEGOTIATION FLOW CHART



For 1000BASE-T mode, auto-negotiation is required and always used to establish a link. During 1000BASE-T auto-negotiation, the master and slave configuration is first resolved between link partners. Then the link is established with the highest common capabilities between link partners.

Auto-negotiation is enabled by default after power-up or hardware reset. After that, auto-negotiation can be enabled or disabled through the Basic Control register, bit[12]. If auto-negotiation is disabled, the speed is set by the Basic Control register, bits[6, 13] and the duplex is set by the Basic Control register, bit[8].

If the speed is changed on the fly, the link goes down and either auto-negotiation and parallel detection initiate until a common speed between the device and its link partner is re-established for a link.

If the link is already established and there is no change of speed on the fly, the changes (for example, duplex and pause capabilities) will not take effect unless either auto-negotiation is restarted through the Basic Control register, bit[9], or a link-down to link-up transition occurs (that is, disconnecting and reconnecting the cable).

After auto-negotiation is completed, the link status is updated in the Basic Status register, bit[2], and the link partner capabilities are updated in Registers 5h, 6h, 8h, and Ah.

The auto-negotiation finite state machines use interval timers to manage the auto-negotiation process. The duration of these timers under normal operating conditions is summarized in [Table 5-2](#).

TABLE 5-2: AUTO-NEGOTIATION TIMERS

Auto-Negotiation Interval Timers	Time Duration
Transmit Burst Interval	16 ms
Transmit Pulse Interval	68 μ s
FLP Detect Minimum Time	17.2 μ s
FLP Detect Maximum Time	185 μ s
Receive Minimum Burst Interval	6.8 ms

TABLE 5-2: AUTO-NEGOTIATION TIMERS (CONTINUED)

Auto-Negotiation Interval Timers	Time Duration
Receive Maximum Burst Interval	112 ms
Data Detect Minimum Interval	35.4 μ s
Data Detect Maximum Interval	95 μ s
Normal Link Pulse (NLP) Test Minimum Interval	4.5 ms
NLP Test Maximum Interval	30 ms
Link Loss Time	52 ms
Break Link Time	1480 ms
Parallel Detection Wait Time	830 ms
Link Enable Wait Time	1000 ms

5.6.1 AUTO-NEGOTIATION NEXT PAGE USAGE

The device supports “Next Page” capability which is used to negotiate Gigabit Ethernet and Energy Efficient Ethernet functionality as well as to support software controlled pages.

As described in IEEE 802.3 Annex 40C “Add-on interface for additional Next Pages”, the device will autonomously send and receive the Gigabit Ethernet and Energy Efficient Ethernet next pages and then optionally send and receive software controlled next pages.

Gigabit Ethernet next pages consist of one message and two unformatted pages. The message page contains an 8 as the message code. The first unformatted page contains the information from the Auto-Negotiation Master Slave Control register. The second unformatted page contains the Master-Slave Seed value used to resolve the Master-Slave selection. The result of the Gigabit Ethernet next pages exchange is stored in Auto-Negotiation Master Slave Status register.

Gigabit Ethernet next pages are always transmitted, regardless of the advertised settings in the Auto-Negotiation Master Slave Control register.

Energy Efficient Ethernet (EEE) next pages consist of one message and one unformatted page. The message page contains a 10 as the message code (this value can be overridden in the EEE Message Code register). The unformatted page contains the information from the EEE Advertisement register. The result of the Gigabit Ethernet next pages exchange is stored in EEE Link Partner Ability register.

EEE next pages are transmitted only if the advertised setting in the EEE Advertisement register is not zero.

APPLICATION NOTE: The Gigabit Ethernet and EEE next pages may be viewed in Auto-Negotiation Next Page RX register as they are exchanged.

Following the EEE next page exchange, software controlled next pages are exchanged when the Next Page bit in the Auto-Negotiation Advertisement register is set. Software controlled next page status is monitored via the Auto-Negotiation Expansion register and Auto-Negotiation Next Page RX register.

5.6.2 PARALLEL DETECT DUPLEX

Normally, and according to IEEE 802.3, when parallel detection is used to establish the link, the resulting operation is set to half duplex. An option exists to force this result to full duplex. This is enabled by setting the LP Force 100 FD Override and/or LP Force 10 FD Override bits in the Parallel Detect Full Duplex Override register.

5.7 Signal Quality Index

5.7.1 BACKGROUND

MLT-3 modulation is used for data transmission in 100BASE-TX and PAM5 modulation is used for data transmission in 1000BASE-T.

Logically, 100BASE-TX (MLT-3) and 1000BASE-T (PAM5) have signal values of $\{-1, 0, +1\}$ and $\{-2, -1, 0, +1, +2\}$, respectively. These logic levels are mapped to slicer reference levels of $\{-128, 0, 128\}$ for 100BASE-TX and $\{-128, -64, 0, 64, 128\}$ for 1000BASE-T. The middle points (the compare thresholds) are $\{-64, 64\}$ for 100BASE-TX and are $\{-96, -32, 32, 96\}$ for 1000BASE-T.

Ideally, each receive data sample would be the maximum distance from the compare thresholds, with error values of 0. But because of noise and imperfection in real applications, the sampled data may be off from its ideal. The closer to the compare threshold, the worse the signal quality.

The slicer error is a measurement of how far the processed data is off from its ideal location. The largest instantaneous slicer error for 1000BASE-T is ± 32 . The largest instantaneous slicer error for 100BASE-TX is ± 64 .

A higher absolute slicer error means a degraded signal receiving condition.

5.7.2 NON OPEN ALLIANCE LOW PASS FILTERED ERROR

Note: All registers references in this section are in Extended Page 1.

With this method, the slicer error is converted into an absolute value and then filtered by a programmable low pass filter. This is similar to taking the average of absolute slicer error over a long moving time window.

This mode is enabled by setting the `sqi_enable` bit in the Dynamic Channel Quality (DCQ) Configuration register.

For each data sample, the difference between the absolute slicer error (scaled by $\times 2$ (before squaring) for 1000BASE-T) and the current filtered value is added back into the current filtered value. The `sqi_squ_mode_en` bit in the DCQ Configuration register is used to square the (scaled) slicer error.

The `sqi_kp` field in the DCQ Configuration register sets the weighting of the add back as a divide by $2^{\text{sqi_kp}}$, effectively setting the filter bandwidth. As the `sqi_kp` value is increased, the weighing is decreased, and the mean slicer error value takes a longer time to settle to a stable value. Also, as the `sqi_kp` value is increased, there will be less variation in the mean slicer error value reported.

The filtered error value is saved every 1.0 ms (125,000 symbols).

In order to capture the current error value, the DCQ Read Capture bit in the DCQ Configuration register needs to be written as a high with the desired cable pair specified in the DCQ Channel Number field of the same register. The DCQ Read Capture bit immediately self-clears and the result is available in the Mean Slicer Error register.

A software based lookup table (derived empirically in lab conditions) may be used to report a Signal Quality Index (SQI) number.

5.7.3 OPEN ALLIANCE TC1/TC12 DCQ MEAN SQUARE ERROR

Note: All registers references in this section are in Extended Page 1.

This section defines the implementation of section 6.1.1 of the TC1 and TC12 specifications. The PHY can provide detailed information of the dynamic signal quality by means of an MSE value. This mode is enabled by setting the `sqi_enable` bit in the DCQ Configuration register.

With this method, the slicer error is converted into a squared value and then filtered by a programmable low pass filter. This is similar to taking the average of absolute slicer error over a long moving time window.

For each data sample, the difference between the absolute slicer error (scaled by $\times 2$ (before squaring) for 1000BASE-T) and the current filtered value is added back into the current filtered value.

The `sqi_squ_mode_en` bit in the DCQ Configuration register must be set to choose square mode.

The `sqi_kp` field in the DCQ Configuration register sets the weighting of the add back as a divide by $2^{\text{sqi_kp}}$, effectively setting the filter bandwidth. As the `sqi_kp` value is increased, the weighing is decreased, and the mean slicer error value takes a longer time to settle to a stable value. Also, as the `sqi_kp` value is increased, there will be less variation in the mean slicer error value reported.

The `scale611` field in the DCQ Configuration register is used to set a divide by factor (divide by 2^{scale611}) such that the Mean Squared Error (MSE) value is linearly scaled to the range of 0 to 511. If the divide by factor is too small, the MSE value is capped at a maximum of 511.

The filtered error value is saved every 1.0 ms (125,000 symbols).

In order to capture the MSE value, the DCQ Read Capture bit in the DCQ Configuration register needs to be written as a high with the desired cable pair specified in the DCQ Channel Number field of the same register. The DCQ Read Capture= bit will immediately self-clear and the result will be available in the DCQ Mean Square Error register.

In addition to the current MSE value the worst case MSE value since the last read of DCQ Mean Square Error register is stored in DCQ Mean Square Error Worst Case register.

5.7.4 OPEN ALLIANCE TC1/TC12 DCQ SIGNAL QUALITY INDEX

Note: All registers references in this section are in Extended Page 1.

This section defines the implementation of section 6.1.2 of the TC1 and TC12 specifications. This mode builds upon the [OPEN Alliance TC1/TC12 DCQ Mean Square Error](#) method by mapping the MSE value onto a simple quality index. This mode is enabled by setting the sqi_enable bit, in the DCQ Configuration register.

Note: As in the [OPEN Alliance TC1/TC12 DCQ Mean Square Error](#) method, the sqi_squ_mode_en bit in the DCQ Configuration register must be set to choose square mode.

Note: As above in the [OPEN Alliance TC1/TC12 DCQ Mean Square Error](#) method, the scale611 field in the DCQ Configuration register is used to set the divide by factor (divide by 2^{scale611}) such that the MSE value is linearly scaled to the range of 0 to 511.

The MSE value is compared to the thresholds set in the DCQ SQI Table Registers to provide an SQI value between 0 (worst value) and 7 (best value) as follows:

TABLE 5-3: MSE TO SQI MAPPING

MSE Value		SQI Value
Greater Than	Less Than or Equal To	
—	SQI_TBL7.SQI_VALUE	7
SQI_TBL7.SQI_VALUE	SQI_TBL6.SQI_VALUE	6
SQI_TBL6.SQI_VALUE	SQI_TBL5.SQI_VALUE	5
SQI_TBL5.SQI_VALUE	SQI_TBL4.SQI_VALUE	4
SQI_TBL4.SQI_VALUE	SQI_TBL3.SQI_VALUE	3
SQI_TBL3.SQI_VALUE	SQI_TBL2.SQI_VALUE	2
SQI_TBL2.SQI_VALUE	SQI_TBL1.SQI_VALUE	1
SQI_TBL1.SQI_VALUE	—	0

In order to capture the SQI value, the DCQ Read Capture bit in the DCQ Configuration register needs to be written as a high with the desired cable pair specified in the DCQ Channel Number field of the same register. The DCQ Read Capture bit will immediately self-clear and the result will be available in the DCQ SQI register.

In addition to the current SQI, the worst case (lowest) SQI since the last read is available in the SQI Worst Case field.

The correlation between the SQI values stored in the DCQ SQI register and an according Signal to Noise Ratio (SNR) based on Additive White Gaussian (AWG) noise (bandwidth of 80 MHz @ 100 Mbps / 550 MHz @ 1000 Mbps) is shown in [Table 5-4](#) and [Table 5-5](#). The bit error rates to be expected in the case of white noise as interference signal is shown in the table as well for information purposes.

A link loss only occurs if the SQI value is 0.

TABLE 5-4: 1000M SQI PERFORMANCE

SQI Value	Link State	Bit Error Rate (BER)
7	Up	< 10^{-10} No frame drops
6	Up	
5	Up	
4	Up	> 10^{-10} Frame drops may occur
3	Up	
2	Up	
1	Up	
0	Intermittent / Down	Heavy frame drops may occur

TABLE 5-5: 100M SQI PERFORMANCE

SQI Value	Link State	Bit Error Rate (BER)
7	Up	< 10^{-10} No frame drops
6	Up	
5	Up	
4	Up	
3	Up	
2	Up	
1	Up	
0	Intermittent / Down	> 10^{-10} Frame drops may occur

5.7.5 OPEN ALLIANCE TC1/TC12 DCQ PEAK MSE VALUE

Note: All registers references in this section are in Extended Page 1.

This section defines the implementation of section 6.1.3 of the TC1 and TC12 specifications. The peak MSE value is intended to identify transient disturbances, which are typically in the microsecond range. This mode is enabled by setting the `sqi_enable` bit, in the DCQ Configuration register.

With this method, the slicer error is converted into a squared value and then filtered by a programmable low pass filter. This is similar to taking the average of absolute slicer error over a moving time window.

For each data sample, the difference between the absolute slicer error (scaled by x2 (before squaring) for 1000BASE-T) and the current filtered value is added back into the current filtered value.

Note: The `sqi_squ_mode_en` bit in the DCQ Configuration register must be set to choose square mode.

The `sqi_kp3` field in the DCQ Configuration register sets the weighting of the add back as a divide by $2^{(sqi_kp3)}$, effectively setting the filter bandwidth. As the `sqi_kp3` value is increased, the weighing is decreased, and the mean slicer error value takes a longer time to settle to a stable value.

Every 1.0 ms (125,000 symbols), the highest filtered value over that previous 1.0 ms period is saved.

The scale613 field in the DCQ Configuration register is used to set a divide by factor (divide by $2^{\text{scale613}+3}$) such that the peak MSE value is linearly scaled to the range of 0 to 63. If the divided by factor is too small, the peak MSE value is capped at a maximum of 63.

In order to capture the peak MSE value, the DCQ Read Capture bit in the DCQ Configuration register needs to be written as a high with the desired cable pair specified in the DCQ Channel Number field of the same register. The DCQ Read Capture bit will immediately self-clear and the result will be available in the DCQ Peak MSE register.

In addition to the current peak MSE value, the worst case peak MSE value since the last read of DCQ Peak MSE register is stored in the same register.

5.8 LinkMD Cable Diagnostics

The LinkMD function uses Time Domain Reflectometry (TDR) to analyze the cabling plant for common cabling problems, such as open circuits, short circuits, and impedance mismatches as well as the distance to the fault. Each of the four twisted pairs are tested separately.

LinkMD operates by sending a pulse of known amplitude and duration down the selected differential pair, then analyzing the polarity and shape of the reflected signal to determine the type of fault: open circuit for a positive/non-inverted amplitude reflection and short circuit for a negative/inverted amplitude reflection. The time duration for the reflected signal to return provides the approximate distance to the cabling fault. The LinkMD function processes this TDR information and presents it as a numerical value that can be translated to a cable distance.

LinkMD is initiated by accessing the Cable Diagnostic register. To test each individual cable pair, set the cable pair in the Cable Diagnostics Test Pair (VCT_PAIR[1:0]) field of the Cable Diagnostic register, along with setting the Cable Diagnostics Test Enable (VCT_EN) bit. The Cable Diagnostics Test Enable (VCT_EN) bit will selfclear when the test is concluded.

The test results (for the pair just tested) are available in the Cable Diagnostic register. With the bit[9:0] Definition (VCT_SEL[1:0]) field set to '0', the Cable Diagnostics Status (VCT_ST[1:0]) field will indicate a Normal (properly terminated), Open or Short condition, or Failed test.

If the test result was Open or Short, the Cable Diagnostics Data or Threshold (VCT_DATA[7:0]) field indicates the distance to the fault in meters as approximately:

- distance to fault = $(\text{VCT_DATA} - 22) * 4 / \text{cable propagation velocity}$

This provides an accuracy of $\pm 2\%$ to 3% for short and medium cables and $\pm 5\%$ to 6% for long cables. Inaccuracy is due to cable pitch differences between cable manufacturers, where cable pitch is the number of wire twists per unit cable length.

Link MD supports diagnostic cable testing in the following three scenarios:

- [LinkMD with No Link Partner](#)
- [LinkMD with Fully Passive Link Partner](#)
- [LinkMD with Partially Active Link Partner](#)

5.8.1 LINKMD WITH NO LINK PARTNER

In this scenario, the remote end of the cable is unplugged.

Prior to running the cable diagnostics, perform a software reset via the Basic Control Register. After reset, the following must be configured:

- Auto Negotiation disabled via the Digital Debug Control 1 Register
- Auto MDI/MDI-X disabled via the Digital Debug Control 1 Register
- Full Duplex set via the Basic Control Register
- Link Speed set to 1000 Mbps via the Basic Control Register
- Master-Slave configuration set to Slave via the Auto Negotiation Master Slave Control Register

Wait 10ms prior to testing the pairs.

In this scenario, for each of the four twisted pairs, LinkMD should only return Open or Short along with a distance.

- Open with "distance" providing the correct cable length indicates a good cable
- Short, or Open with any other distance indicates a bad cable

After running the cable diagnostics, perform another software reset via the Basic Control Register

5.8.2 LINKMD WITH FULLY PASSIVE LINK PARTNER

In this scenario, the remote end of the cable is connected to a Link Partner. The Link Partner must be powered down or configured to be in the following passive state:

- Auto Negotiation disabled
- Auto MDI/MDI-X disabled

Prior to running the cable diagnostics, perform a software reset via the Basic Control Register. After reset, the following must be configured:

- Auto Negotiation disabled via the Digital Debug Control 1 Register
- Auto MDI/MDI-X disabled via the Digital Debug Control 1 Register
- Full Duplex set via the Basic Control Register
- Link Speed set to 1000 Mbps via the Basic Control Register
- Master-Slave configuration set to Slave via the Auto Negotiation Master Slave Control Register

Wait 10ms prior to testing the pairs.

In this scenario, for each of the four twisted pairs, LinkMD will return Open or Short along with a distance, or Normal.

- Normal indicates a good cable which is properly terminated at the Link Partner. Due to no TDR reflections, no cable distance is available with this result (VCT[7:0] is invalid).
- Open or Short indicates a bad cable or improper Link Partner termination. VCT[7:0] indicates the distance to the cable fault.

After running the cable diagnostics, perform another software reset via the Basic Control Register.

5.8.3 LINKMD WITH PARTIALLY ACTIVE LINK PARTNER

In this scenario, the remote end of the cable is connected to a Link Partner. The Link Partner is powered up and in the following state:

- Auto Negotiation may be enabled, disabled, or unknown
- Auto MDI/MDI-X is disabled, but we are able to selectively configure MDI or MDI-X, as required for the LinkMD tests

Prior to running the cable diagnostics, perform a software reset via the Basic Control Register. After reset, the following must be configured:

- Auto Negotiation disabled via the Digital Debug Control 1 Register
- Auto MDI/MDI-X disabled via the Digital Debug Control 1 Register
- Full Duplex set via the Basic Control Register
- Link Speed set to 1000 Mbps via the Basic Control Register
- Master-Slave configuration set to Slave via the Auto Negotiation Master Slave Control Register

Wait 10ms prior to testing the pairs.

The LinkMD test is first run with the Link Partner in MDI mode on twisted pairs B, C, and D.

The LinkMD test is then run with the Link Partner in MDI-X mode on twisted pair A.

- Normal indicates a good cable which is properly terminated at the Link Partner. Due to no TDR reflections, no cable distance is available with this result (VCT[7:0] is invalid).
- Open or Short indicates a bad cable or improper Link Partner termination. VCT[7:0] indicates the distance to the cable fault.

After running the cable diagnostics, perform another software reset via the Basic Control Register.

APPLICATION NOTE: If the Cable Diagnostics Status (VCT_ST[1:0]) field indicates Failed, it is generally due to multiple pulses being received after sending out a single pulse. In this Partially Active test, the Link Partner is allowed to be in the Auto-Negotiation state, but if the Link Partner is mistakenly in forced 1000BASE-T or 100BASE-TX mode, the test will fail.

APPLICATION NOTE: Any signal received from a link partner will interfere with the TDR test. Energy detection must first be checked on each wire pair by using the procedure in [Section 5.22.2, "Energy-Detect Power-Down Mode"](#).

5.9 Auto-Downshift

Under certain fault conditions (e.g. cable break in wiring pair C or D), standard Auto-Negotiation will loop forever attempting to link at 1 Gbps without ever fully linking up. Auto-Downshift extends standard ANEG to allow slower speed linkup under such conditions.

If Auto-Downshift is enabled (ENABLE_AUTO_DOWN_SPEED=1), a hardware counter counts the number of attempted 1 Gbps linkups. After four failures, ANEG will be restarted but advertising 100 Mbps as the maximum capable speed.

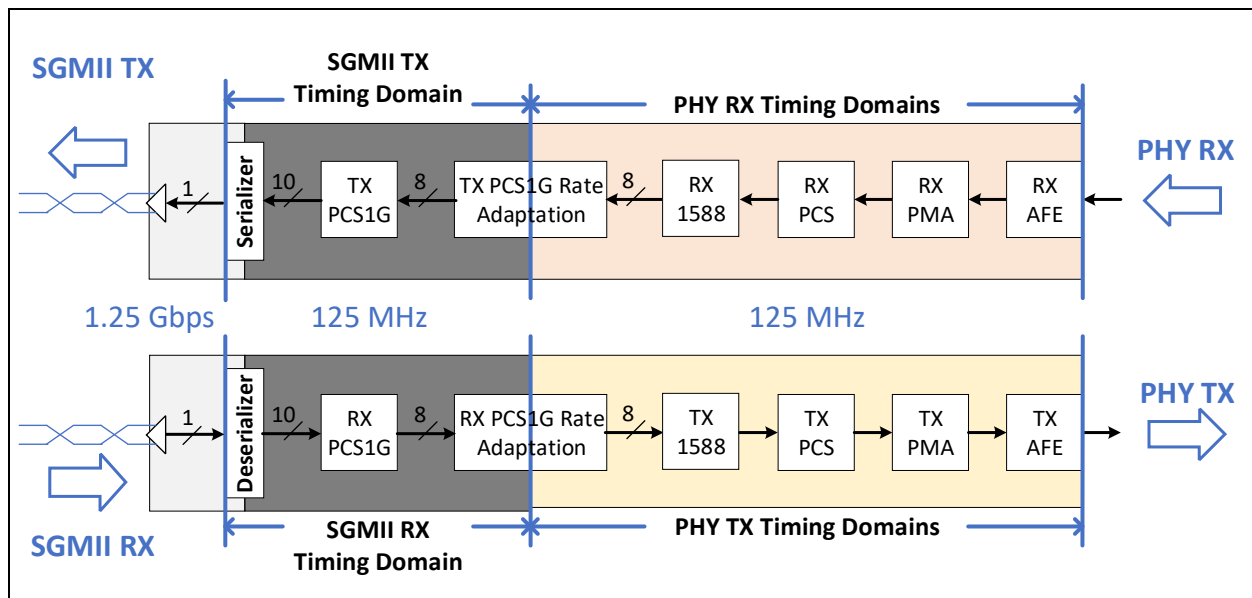
If 100 Mbps fails to link after four attempts, ANEG will be restarted but advertising 10 Mbps as the maximum capable speed.

If 10Mbps fails to link after four attempts, ANEG might loop forever as there is no slower speed.

5.10 SGMII

The device provides a SGMII interface that adheres to the SGMII Specification Rev. 1.8 [6] (ENG-46158). SGMII is a serial chip-chip connection that connects the LAN8842 PHY port with a MAC in the Switch or SoC. Figure 5-2 illustrates SGMII operation, with the switch/SoC connection on the left and the LAN8842 connection on the right.

FIGURE 5-2: SGMII SYSTEM DIAGRAM



The device PHY connects to an SGMII “PCS1G” block (shown in Figure 5-2 as a separate TX PCS1G and RX PCS1G). The PCS1G includes a Jitter Test Pattern (JTP) Generator and Checker. The JTP Generator supports the following test patterns:

- High Frequency Test Pattern – repeated transmission of D21.5 code group
- Low Frequency Test Pattern – repeated transmission of K28.7 code group
- Mixed Frequency Test Pattern – repeated transmission of K28.5 code group
- Long Continuous Random Test Pattern – 1524 byte frames
- Short Continuous Random Test Pattern – 360 byte frames

The JTP Checker provides Checker Lock and Error Detected indications, as well as an error count.

Note: PHY TX and RX directions are relative to the Ethernet Media Interfaces. SGMII TX and RX directions are relative to the SGMII SerDes interface. So device frames received from the Ethernet Media Interfaces are processed in RX GPHY and 1588 blocks, and in TX SGMII blocks.

Note: Frame Preemption operates as follows (consistent with the SGMII specification and SparX-5i operation):

- If PCH/MCH is enabled, the SMD/SFD symbols are overwritten by the PCH/MCH. So the SMD/SFD values are instead signaled via the PCH/MCH.
- If PCH/MCH is disabled, the SMD/SFD values are passed transparently through the SGMII interface as a normal part of the preamble.

In both cases, SPD always appears ahead of each frame across SGMII. Refer to [Section 5.13, "IEEE 1588 \(PTP\)"](#) for format details.

Note: If Energy Efficient Ethernet (EEE) is enabled, it is controlled using LPI symbols, which pass transparently through SGMII.

Note: Coma mode disables the SGMII Tx and RX clocks, effectively silencing the SGMII Interface.

The following SGMII preamble formats are supported:

- In PCH/MCH mode, all frames on the PCS1G GMII from the 1588 TSU towards MAC must have exactly 8 bytes of preamble (including 'h55, SFD/SMD, and FRAG_COUNT if applicable). The 1588 TSU module will reconstruct the field to be 8 bytes if it isn't already, including ensuring an even number of nibbles (integer number of bytes) exists.
- In PCH/MCH mode, all frames on the PCS1G GMII from MAC towards the 1588 TSU must have 8 bytes of preamble (including 'h55, SFD/SMD, and FRAG_COUNT if applicable). The 1588 TSU is not required to perform any preamble reconstruction or nibble alignment.

Note, in PCH/MCH mode the first preamble byte will be 10-bit encoded 'hFB crossing the SerDes.

- In non PCH/MCH mode, frames on the PCS1G GMII from the 1588 TSU towards the MAC do not need to have 8 bytes of preamble. The 1588 TSU module will however ensure an even number of nibbles (integer number of bytes) exists.
- In non PCH/MCH mode, frames on the PCS1G GMII from MAC towards the 1588 TSU must have an integer number of preamble bytes, but do not need to have exactly 8 bytes of preamble. The 1588 TSU is not required to perform any preamble reconstruction or nibble alignment.

Note, in non PCH/MCH mode the first preamble byte will be 10-bit encoded 'hFB crossing the SerDes.

SGMII operates on the following clock domains:

- SGMII Tx functions (PHY to MAC direction) operate on the SGMII Tx clock domain, derived in the SerDes MPLL using the internal System PLL clock as reference.
- SGMII Rx functions (MAC to PHY direction) operate on the SGMII Rx clock domain, derived by the SerDes Rx CDR function.
- PHY Tx functions, from each Rx PCS1G Rate Adapter to each Tx 1588 Timestamp Engine or PCS, operate on the PHY Tx clock domain.
- PHY Rx functions, from the Rx 1588 Timestamp Engine or PCS to the Tx PCS1G Rate Adapter, operate on the PHY Rx clock domain.
- Control and Status Registers operate on the System clock domain.

SGMII loopbacks are discussed in [Section 5.16.4, "SGMII Loopback"](#).

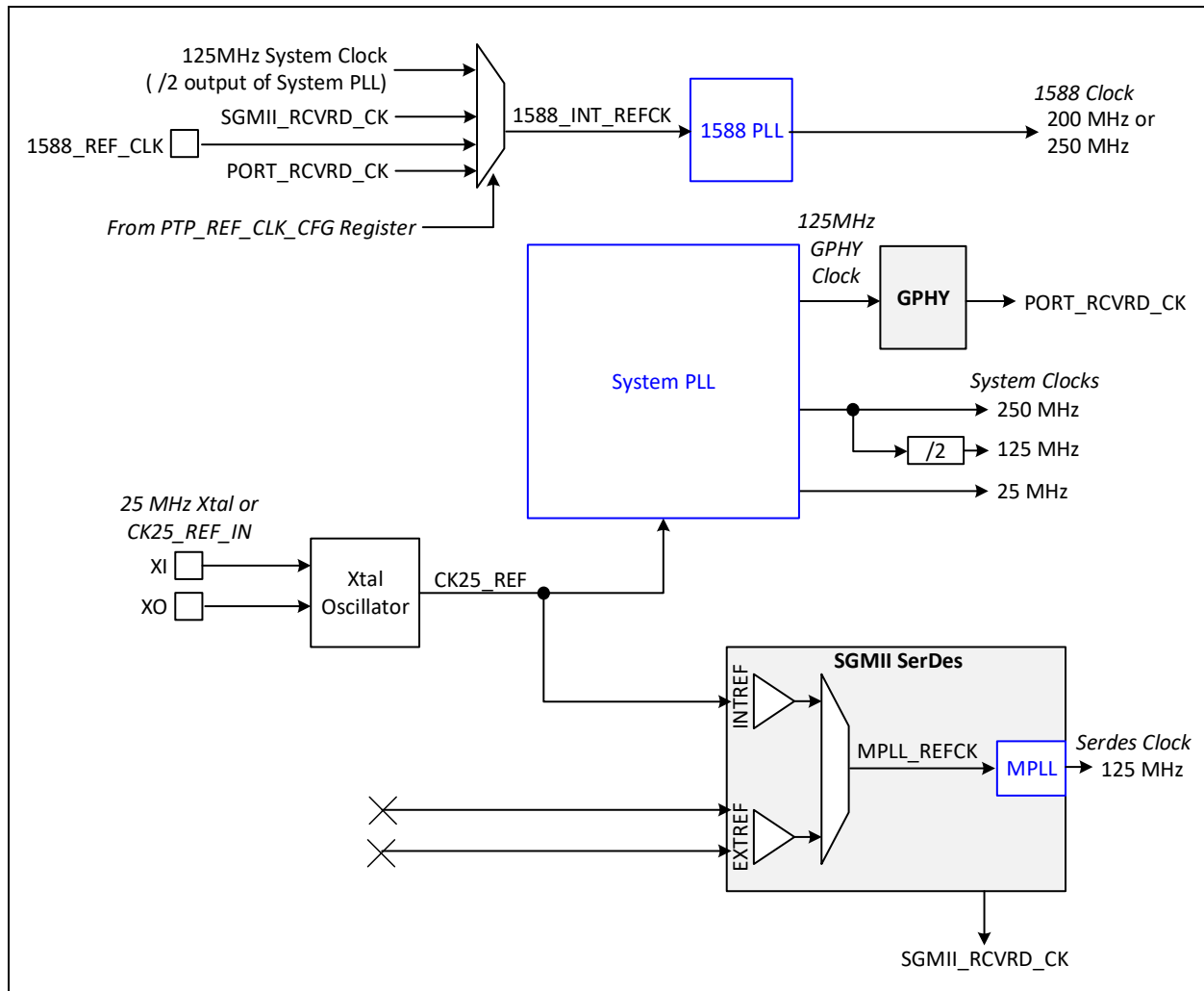
5.11 PLL/Clocks and Resets

The device provides the following PLLs:

- **System PLL:** Generates the internal system clocks and clocks required for the internal PHY. See [Section 5.11.1, "System Clocks"](#) for additional information.
- **1588 PLL:** Generates the internal 1588 clock. See [Section 5.11.2, "1588 Clock"](#) for additional information.
- **SGMII SerDes MPLL:** Generates the clocks needed by the SerDes. See [Section 5.11.3, "SGMII SerDes Clock"](#) for additional information.

Note: Coma mode has no effect on the system clocks, which will keep running even when COMA Mode is asserted. SerDes clocks, 1588 clock, and GPHY port recovered clocks are all killed by COMA Mode. Refer to [Section 5.24, "Coma Mode"](#) for additional information.

FIGURE 5-3: LAN8842 CLOCKS



5.11.1 SYSTEM CLOCKS

System clocks are generated by the System PLL and are used for many common (not port-specific) functions such as SGMII TX and configuration registers. These clocks are also selectable by the PHY port for use as PHY TX timing.

The System PLL generates the following clocks:

- 250 MHz system clock
- 25 MHz system clock

The System PLL can use any of the following as its input reference clock:

- 25 MHz Crystal
- 25 MHz system single-ended reference clock input

5.11.2 1588 CLOCK

The 1588 clock is used for 1588 common functions such as the 1588 LTC. This PLL performs the following functions:

- Ensures 50/50 duty cycle of internal 1588 clock. Since both edges are used by some logic, this helps with timing closure and contributes to accuracy.
- Balances out internal insertion and clock distribution delays, which contributes to accuracy.
- Enables high precision timestamping with any supported 1588 reference frequency (250 MHz reference not)

required).

- Enables use of input ePPS as implemented by the Microchip SparX-5i, improving accuracy and simplifying system considerations.
- Enables highest precision timestamping based on 250 MHz when the 1588 reference clock is not frequency-locked to port timing (and therefore has some ppm frequency differences).
- Enables slightly reduced precision timestamping based on 200 MHz when the 1588 reference clock is frequency-locked to port timing. In this case, the 250 MHz clock must not be used as it introduces static timestamping errors which cannot be filtered, so a slightly reduced frequency is used to ensure port clock and timestamping clock edges drift relative to each other.
Note that timestamping is based on both 1588 clock edges, so 200 MHz clock indicates sampling every 2.5 ns. The PTP timestamping engine assumes sampling at a whole-nanosecond rate, so an additional 0.5 ns of time-stamp error may result when using 200 MHz.

The 1588 PLL can use any of these as its input reference clock:

- 1588 reference clock input (10, 25, or 125 MHz)
- 125 MHz System clock
- 125 MHz SGMII RX recovered timing
- 25 MHz or 125 MHz recovered port timing (2.5 MHz not supported)

5.11.3 SGMII SERDES CLOCK

The 125 MHz SGMII SerDes clock is generated by the SerDes MPLL.

The SGMII SerDes MPLL can use the 25 MHz system clock (from crystal or single-ended external clock input) as its input reference clock:

5.11.4 RESETS

The device supports the following software resets from configuration registers:

- Chip hard and soft resets (all logic and macros in the chip)
 - Chip soft reset (EP4.9) does not reset the Gigabit PHY. If needed, the GPHY Hard Macro soft reset must be used for this.
 - GPHY resistor calibration is also run based on the chip hard reset.
- SGMII hard and soft resets (SGMII SerDes and PCS1Gs)
- SGMII SerDes transmitter and receiver resets
- 1588 Local Time Clock hard and soft resets
- 1588 PLL reset
- Port hard and soft resets (with port logic and macros)
 - Neither port hard reset (EP5.80) nor soft reset (EP5.81) will reset the GPHY. If needed, the GPHY Macro hard or soft reset must be used for this.
- Gigabit PHY hard macro hard and soft resets
- 1588 Timestamp Engine hard and soft resets

The device also provides a **RESET_N** input pin. This pin must adhere to the timing requirements detailed in [Section 6.6.2, "Power Sequence Timing"](#) and [Section 6.6.3, "Reset Pin Configuration Strap Timing"](#). Release from reset is based on the **RESET_N** input pin transitioning from low to high.

5.11.5 POWER ON READY (POR) WITH OVER/UNDER VOLTAGE PROTECTION

POR monitors three voltages (Refer to [Table 6-9](#) for the exact specification):

- +1.1V Analog Power Supply (on **VDDAL_x**) set for ~0.8V (typical) - it is assumed that **VDDCORE** and **VDDAL_x** are externally connected, therefore VDD is indirectly monitored.
- +2.5 / 3.3V Analog Power Supply (on **VDDAH_x**) set for ~2.1V (typical)
- Variable I/O Power Supply (on **VDDIO**) set for ~1.5V (typical)

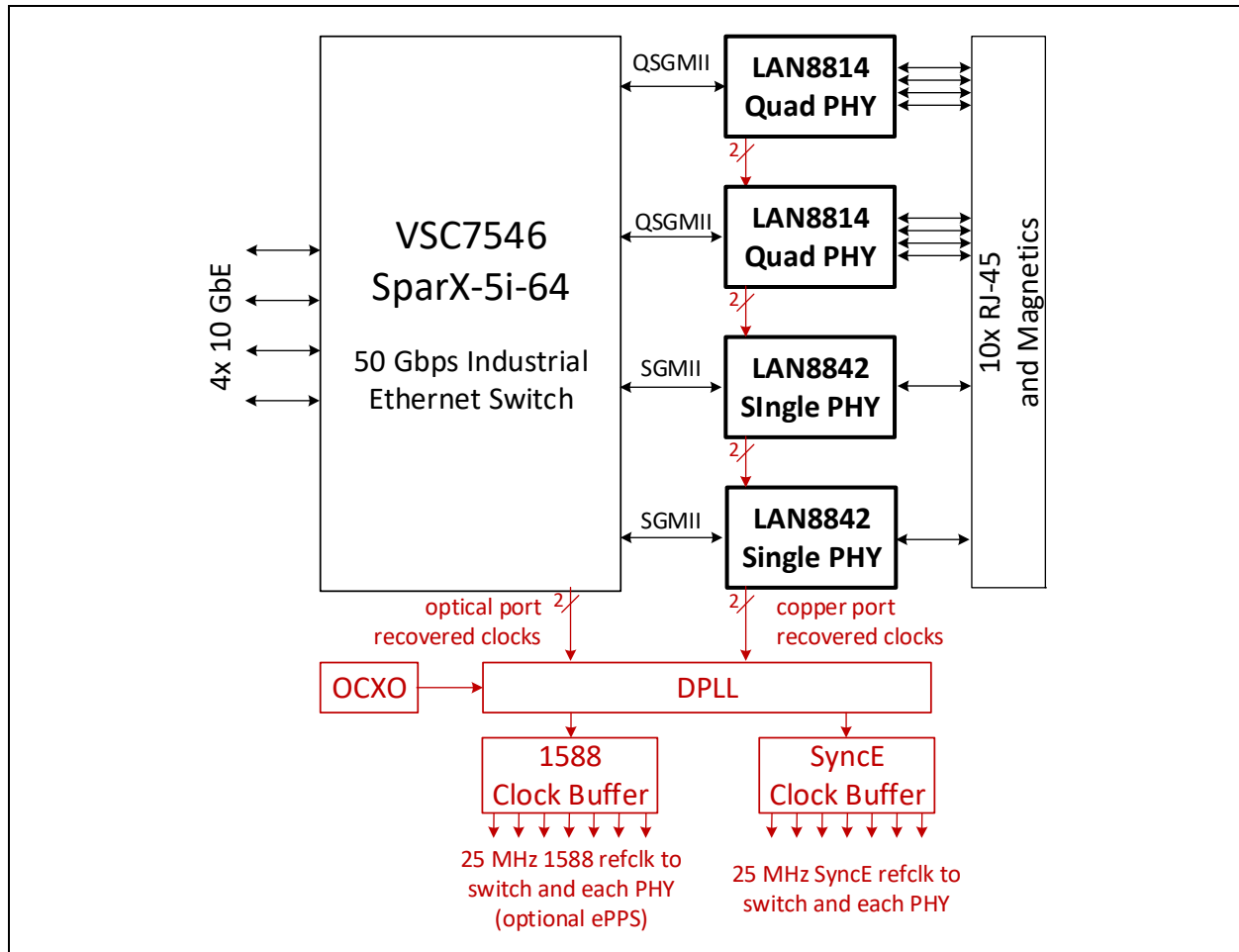
The POR circuits have a "dead zone" between bottom range of valid operational voltage and where POR trips (e.g., -15%/20%). The Over/Under Voltage Protection enables tightening this range to just under the bottom of the supply range.

5.12 Synchronous Ethernet

The device supports Synchronous Ethernet (SyncE), as specified by ITU-T G.8261.

Figure 5-4 illustrates Synchronous Ethernet and IEEE-1588 in an Ethernet switch system. A system may have both SyncE and 1588, SyncE only, 1588 only, or neither SyncE nor 1588. Oscillator and Digital Phase-Locked Loop (DPLL) selection will vary accordingly. IEEE 1588 is discussed in Section 5.13, "IEEE 1588 (PTP)".

FIGURE 5-4: SYNCHRONOUS ETHERNET AND IEEE 1588 SYSTEM DIAGRAM



SyncE requirements for such a system are:

- Ability to select any timing source as the Primary timing reference, and any other timing source as the Secondary timing reference.
- Each multi-port device (NOT LAN8842) in this system must therefore provide two recovered timing outputs. Each of the two outputs must be able to select any port recovered timing, or either of the two recovered timing inputs. The two recovered timing outputs from each PHY are daisy-chained through the PHYs, ultimately providing two recovered timing outputs to the DPLL (the combined PHY functionality is two 10:1 recovered clock muxes toward the DPLL). The external DPLL provides cleanup, frequency conversion, failover between Primary/Secondary/ Holdover, etc.
- As a single-port device, the LAN8842 only has recovered timing from a single port. But in this system example, it must still support daisy-chaining of two recovered clocks from upstream devices and pass two recovered clock options downstream toward the DPLL.
- Ability to use a local high-quality oscillator as a timing reference, which might be Primary or Secondary or to provide a holdover timing mode when both Primary and Secondary are not available. In Figure 5-4, the Oven Controlled Crystal (Xtal) Oscillator (OCXO) provides this function.
- Ability to use the 1588 Packet-based Equipment Clock (PEC) as a SyncE timing reference, typically this is the

Secondary timing reference. Recovering timing from 1588 packets is called “syntonization”.

- Ability to use the selected timing reference as the transmit timing on the port. The SyncE clock buffer provides this fanout to the switch and all PHYs. For the LAN8842, this is connected to the system reference clock input.
- The external DPLL must monitor any backup timing source for quality before failing over to it. There are many specifications on allowable timing degradations (e.g., jitter and wander) and timeframes during a timing failover. These are handled by the external DPLL and are beyond the scope of this document, but the timing failure must be detected and the external DPLL notified within a small number of milliseconds.
 - FLF clock output squelching is used to meet these requirements.

Each device transmit port can run directly on its own recovered receive timing, or on a clock reference from the System PLL.

5.12.1 FAST LINK FAILURE

To aid Synchronous Ethernet applications, the device can indicate unstable link operation leading to link failure in ~1 ms. By comparison, standard IEEE 1000BASE-T link failure detection requires a minimum of 750 ms, which is unacceptable for Synchronous Ethernet applications.

If enabled, the PHY detects FLF and indicates the result via:

- An internal signal used to squelch the associated recovered clock output
- An internal register which can be read by software
- An interrupt to software (if enabled)
- If enabled, FLF may also be used directly as a link down indication

FLF is supported at all three port speeds as follows:

- At 1000 Mbps, FLF is asserted when remote receiver status goes low (part of the scrambled idles), or when the local descrambler loses lock.
- At 100 Mbps, FLF is asserted when the local descrambler loses lock.
- At 10 Mbps, FLF is asserted when remote link status (NLP) is not received in time to maintain Link Up.

At 100 and 1000 Mbps, FLF performance will be < 1 ms, measured by forcing the remote link partner off (e.g., reset or power-down). FLF is measured from the time the remote link partner is off until the time the local FLF signal is asserted.

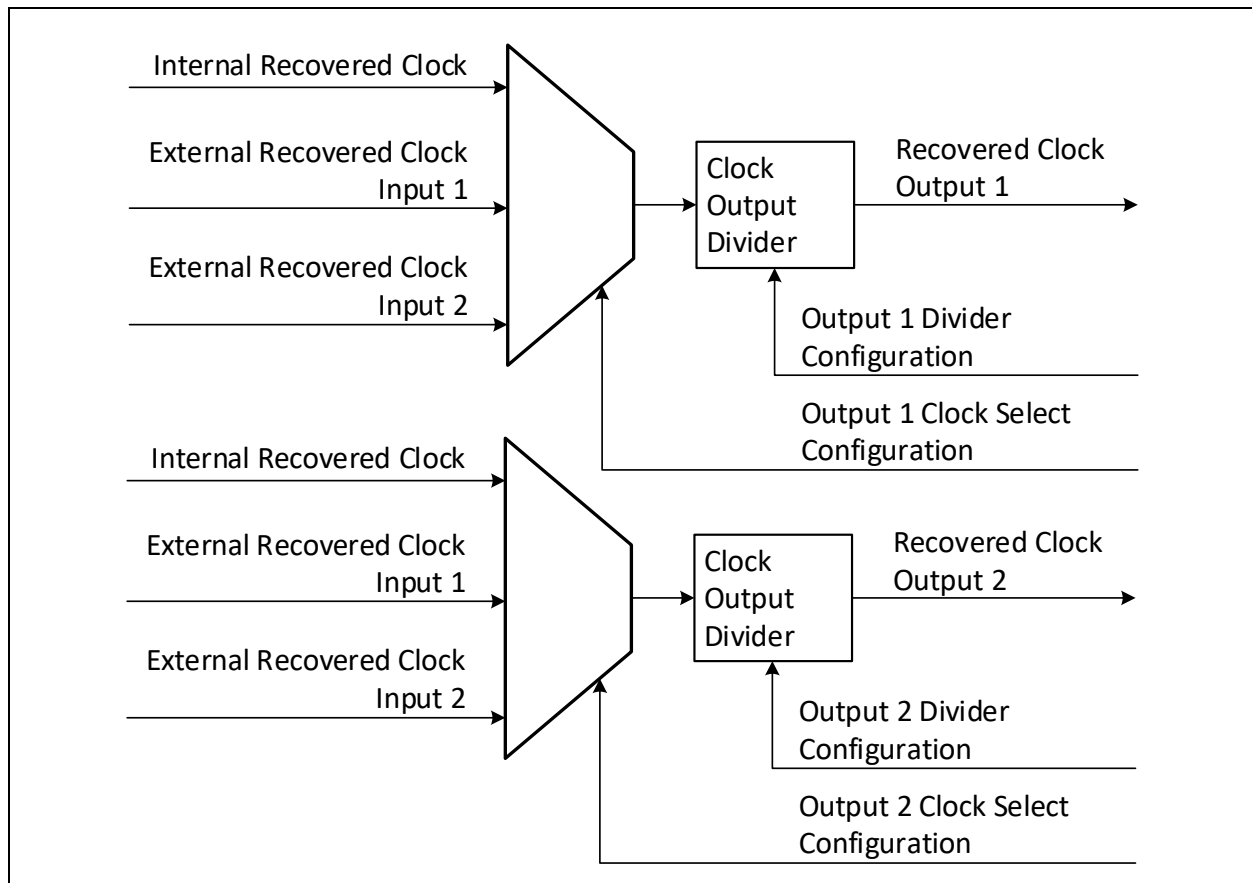
At 10 Mbps, FLF performance is limited by the rate of NLP pulses which are specified in 802.3 as 16 ± 8 ms. FLF at 10 Mbps will be 100 ms.

5.12.2 SYNCHRONOUS ETHERNET RECOVERED CLOCK OUTPUTS AND INPUTS

Two recovered receive clock outputs are provided from the device, one from the port or two from the recovered timing inputs. The frequency of the recovered receive clocks depends on the speed of the PHY port (2.5 MHz, 25 MHz, or 125 MHz). The output has the option to squelch the recovered clock if:

- The associated link is down
- The associated link is determined to be unstable based on the FLF feature
- The associated link is in 10BASE-T or 1000BASE-T Master mode
- The output is disabled by software

FIGURE 5-5: SYNC RECOVERED CLOCK OUTPUTS



In addition, each recovered clock output supports a configurable divider capable of always providing 2.5 MHz as per the [Table 5-6](#).

TABLE 5-6: RECOVERED CLOCK DIVIDERS

Clock Output Mux Source	Port Speed	Internal RX Port Clock Frequency	Clock Output Divider ()	Clock Output Frequency
Internal Port	10 Mbps	2.5 MHz	/ 1	2.5 MHz
	100 Mbps	25 MHz	/ 10	2.5 MHz
	1000 Mbps	125 MHz	/ 50	2.5 MHz
Recovered Clock External Input	Any	N/A	/ 1	Same as external input

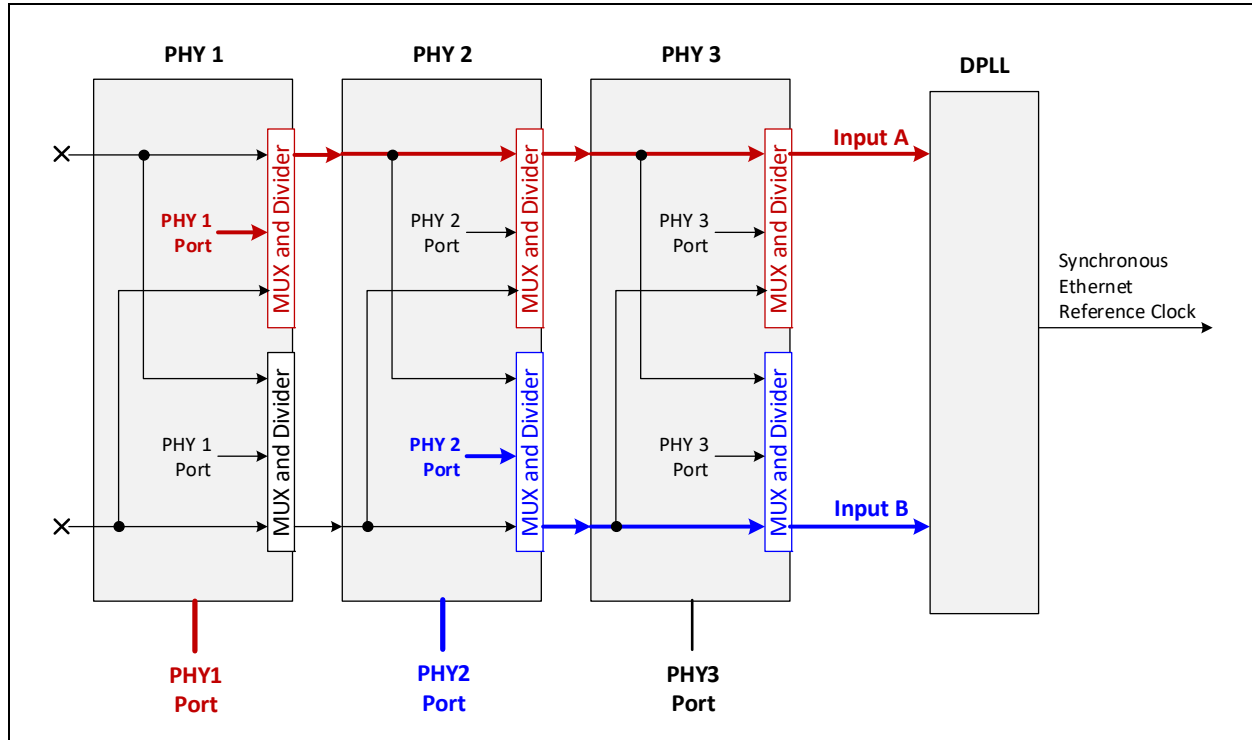
Note 5-3 These are the settings configured by a customer desiring 2.5 MHz clock output frequency for all port speeds. It is also possible to configure / 1 for all port speeds.

For applications with multiple PHY devices, the recovered output clocks can be daisy-chained as shown in [Figure 5-6](#). [Figure 5-6](#) illustrates a three port application using three LAN8842 PHYs. Synchronous Ethernet is configured to use recovered line timing from PHY1_Port0 as the primary reference, and the recovered line timing from PHY2_Port0 as the secondary reference. Due to the daisy-chaining of recovered line clocks, a DPLL with only two inputs can be used, saving DPLL component cost and board layout complications.

In daisy-chained applications, it is recommended that the PHY providing the recovered line clock provides a 2.5 MHz recovered clock output, and the daisy-chain PHY Dividers are set to divide-by-one. This ensures minimal duty cycle distortion through the recovered clock daisy-chain.

To use Synchronous Ethernet Recovered Clock Inputs and Outputs, they must be enabled as GPIOs and GPIO Alternate Functions. The GPIO Buffer Type and GPIO Direction must also be set appropriately.

FIGURE 5-6: SYNCHRONOUS ETHERNET RECOVERED CLOCK DAISY-CHAINING



5.13 IEEE 1588 (PTP)

The device provides hardware support for the IEEE 1588-2008 (v2) Precision Time Protocol (PTP), allowing time synchronization with remote Ethernet devices, packet time stamping and time driven event generation.

Note: Support for the IEEE 1588-2002 (v1) packet format is not provided.

Note on terminology: IEEE 1588 terminology has been updated to align with draft amendment P1588g/D1.2 (March 2022) *Master-Slave Optional Alternative Terminology*. Using this updated terminology, the components of a PTP network are described below:

- **Ordinary Clock (OC):** A PTP instance that has one PTP port, which is operating as either a timeTransmitter or a timeReceiver. A Grandmaster Clock is a special case of an OC/timeTransmitter which is the primary timing source for a given PTP domain.
- **Boundary Clock (BC):** A PTP instance which terminates PTP timing on its timeReceiver port and distributes the recovered PTP timing on one or more timeTransmitter port(s).
- **Transparent Clock (TC):** A PTP instance which passes timing transparently. A TC can be either End to End (E2E TC) or Peer to Peer (P2P TC), and may also be combined with an OC function.

The device port may function as a timeTransmitter or a timeReceiver clock per the IEEE 1588-2008 specification. End-to-end and peer-to-peer link delay mechanisms are supported as are one-step and two-step operations.

A 48-bit seconds and 30-bit nanoseconds tunable Local Time Counter is provided that is used as the time source for all PTP timestamp related functions. A 1588 Local Time Events sub-module provides 1588 Local Time Counter comparison based interrupt generation and timestamp-related GPIO event generation. GPIO pins, when configured as an input, can

be used to trigger a timestamp capture or the setting of the tunable Local Time Counter. When configured as an output, the GPIO pins can provide a signal based on a 1588 Local Time Target compare event. All features of the IEEE 1588 unit can be monitored and configured via their respective configuration and status registers.

IEEE 1588-2008 specifies a Precision Time Protocol (PTP) used by OC, BC, and TC devices to pass time information in order to achieve clock synchronization. Ten network message types are defined:

- Sync
- Follow_Up
- Delay_Req
- Delay_Resp
- Pdelay_Req
- Pdelay_Resp
- Pdelay_Resp_Follow_Up
- Announce
- Signaling
- Management

The first seven message types are used for clock synchronization. Using these messages, the protocol software may calculate the offset and network delay between timestamps, adjusting the timeReceiver clock frequency as needed. Refer to the IEEE 1588-2008 protocol for message definitions and proper usage.

A PTP domain is segmented into PTP sub-domains, which are then segmented into PTP communication paths. Within each PTP communication path there is a maximum of one timeTransmitter clock, which is the source of time for each timeReceiver clock. The determination of which clock is the timeTransmitter and which clock(s) is(are) the timeReceiver(s) is not fixed, but determined by the IEEE 1588-2008 protocol. Similarly, each PTP sub-domain may have only one timeTransmitter clock, referred to as the Grandmaster Clock.

PTP communication paths are conceptually equivalent to Ethernet collision domains and may contain devices which extend the network. However, unlike Ethernet collision domains, the PTP communication path does not stop at a network switch, bridge, or router. This leads to a loss of precision when the network switch/bridge/router introduces a variable delay. Boundary clocks are defined which conceptually bypass the switch/bridge/router (either physically or via device integration). Essentially, a boundary clock acts as a timeReceiver to an upstream timeTransmitter, and as a timeTransmitter to a one or more down stream timeReceiver(s). A boundary clock may contain multiple ports, but a maximum of one timeReceiver port is permitted.

Although boundary clocks solve the issue of the variable delay influencing the synchronization accuracy, they add clock jitter as each boundary clock tracks the clock of its upstream timeTransmitter. Another approach that is supported is the concept of transparent clocks. These devices measure the delay they have added when forwarding a message (the residence time) and report this additional delay either in the forwarded message (one-step) or in a subsequent message (two-step).

The PTP relies on the knowledge of the path delays between the timeTransmitter and the timeReceiver. With this information, and the knowledge of when the timeTransmitter has sent the packet, a timeReceiver can calculate its clock offset from the timeTransmitter and make appropriate adjustments. There are two methods of obtaining the network path delay. Using the end-to-end method, packets are exchanged between the timeReceiver and the timeTransmitter. Any intermediate variable bridge or switch delays are compensated by the transparent clock method described above. Using the round trip time and accounting for the residence time reported, the timeReceiver can calculate the mean delay from the timeTransmitter. Each timeReceiver sends and receives its own messages and calculates its own delay. While the end-to-end method is the simplest, it does add burden on the timeTransmitter since the timeTransmitter must process packets from each timeReceiver in the system. This is amplified when boundary clocks are replaced by transparent clocks. Also, the end-to-end delays must be recalculated if there is a change in the network topology. Using the peer-to-peer method, packets are exchanged only between adjacent timeTransmitter, timeReceiver and transparent clocks. Each peer pair calculates the receive path delay. As time synchronization packets are forwarded between the timeTransmitter and the timeReceiver, the transparent clock adds the pre-measured receive path delay into the residence time. The final receiver adds its receive path delay. Using the peer-to-peer method, the full path delay is accounted for without the timeTransmitter having to service each timeReceiver. The peer-to-peer method better supports network topology changes since each path delay is kept up-to-date regardless of the port status.

High-level IEEE-1588 system operation is illustrated in [Section 5.12, "Synchronous Ethernet"](#). [Figure 5-4](#) is applicable to both the Switch and SoC applications, where the SoC application is a subset of what is shown (fewer PHYs), and noting there are functional differences that don't appear in the diagram but are described in this section.

Note, the SoC application also supports simplified 1588 operation using only the internal PLL with no external DPLL. In this lightweight configuration, 1588 software is still required and full 1588 accuracy is available. Recovered clock jitter and wander performance will be significantly worse compared to having an external DPLL, and it is not possible to maintain separate SyncE and 1588 timing.

Any timing source including the OCXO or Synchronous Ethernet Equipment Clock (EEC) might be selected as the reference clock into the 1588 Packet-based Equipment Clock (PEC). The output of the PEC provides the 1588 reference clock used in the Switch/SoC and PHY 1588 functions. The EEC function is related to SyncE, while to PEC function is related to PTP/1588.

System operation requires the same Time of Day (TOD) (within acceptable accuracy tolerances) exists in the switch and PHYs. Software is able to adjust the 1588 reference clock phase and frequency in the internal PLL or external DPLL, as well as the 1588 TOD in each device.

The device provides one 1588 Timestamp Engine instance, operating off the following clock domains:

- RX processing functions operate on the port's PHY RX clock domain.
- TX processing functions operate on the port's PHY TX clock domain.
- Control/Status Registers operate on the System clock domain.

The device also provides one instance of 1588 common functions, operating off the following clock domains:

- 1588 LTC, PPS and Event functions operate on the 1588 clock domain

The device support two basic 1588 operating modes:

- [1588 Standalone Mode Operation](#), in which the full classification and 1588 processing capabilities are available. This mode is to be used where the host device is not an advanced Microchip switch or other 1588 engine capable of operating with PCH or MCH headers.
- [1588 PCH Mode Operation](#), in which no classification is available and only limited 1588 processing capabilities are used. This mode is to be used where the host device is an advanced Microchip switch (SparX-5i, etc.) or other 1588 engine capable of operating with PCH or MCH headers.

5.13.1 1588 OPERATION WITH FRAME PREEMPTION

The device supports 1588 timestamping of unfragmented e-frames. Timestamping of 1588 e-frames works in the presence of fragmented or unfragmented p-frames.

5.13.2 1588 STANDALONE MODE OPERATION

5.13.2.1 Standalone Mode RX

In Standalone mode RX, arriving 1588 frames are identified and parsed, and the arrival timestamp is captured and placed into the Timestamp FIFO for use in the RX or TX frame modification block, which modifies PTP Message Timestamps and correctionField (CF).

To interoperate with legacy VSC 1588 PHYs (such as VSC8584 or VSC8574) using E2E TC mode, arriving 1588 frames are identified and parsed, and the arrival timestamp is captured and placed in the PTP Message header four-byte Reserved field. The format is 30-bit subseconds with the upper two Reserved bits set to zero, compatible with legacy VSC timestamping PHYs.

UDP checking and updating is as follows:

- UDP/IPv4: verify zero or valid checksum. If invalid, force FCS error. If valid, clear to zero.
- UDP/IPv6: verify non-zero (if enabled) and valid checksum. If invalid, force FCS error. If valid, update checksum pad types (if enabled).

FCS checking and updating is as follows:

- Incrementally update FCS based on all frame modifications. If arriving FCS or UDP checksum fails, ensure departing FCS fails.

5.13.2.2 Standalone Mode TX

In Standalone mode TX, departing 1588 frames are identified and parsed, and the departure timestamp captured and placed into the Timestamp FIFO for use in the TX frame modification block which modifies PTP Message Timestamps and correctionField.

To interoperate with legacy VSC 1588 PHYs using E2E TC mode, departing 1588 frames are identified and parsed. The departure timestamp is captured and the 30-bit subseconds arrival timestamp is extracted from the PTP Message header four-byte Reserved field. The arrival timestamp and departure timestamp are placed into the Timestamp FIFO for use in the TX frame modification block, which updates the PTP Message correctionField as follows:

$CF = A \text{ (original CF of the frame)} + \text{departure timestamp} + \text{TX delay} - \text{arrival timestamp}$

TX delay accounts for all known fixed/static plus variable delays from the TX timestamping point to the TX PHY port.

The device also updates the Ethernet FCS and UDP checksum pad bytes (if IPv6 and enabled) accordingly. If IPv4 and enabled, the device clears the UDP checksum field to zeros.

5.13.3 1588 PCH MODE OPERATION

PCH is a standardized header supporting two-step operation using a Frame Signature. Frames with a valid Frame Signature are processed as 1588 frames. MCH is a non-standard extension of PCH enabling one-step operation in a PHY without classification capabilities. The MCH processing essentially implements a TC between the PHY and the switch, where the switch has subtracted an arrival value from CF, and the PHY adds the departure timestamp to CF. All other 1588 operations are performed in the switch.

5.13.3.1 PCH Mode RX

In PCH mode RX, arriving 1588 frames are not identified or parsed by the device. All arriving frames are given an arrival timestamp, which is in the ENT RSRV30 format (30 lsbits of the 32bit nanosecond LTC time, located in the 1588-2019 msgTypeSpecific bytes). The preamble is replaced with a PCH/MCH TX header containing the arrival timestamp as shown in [Figure 5-7](#), and this is passed to the SGMII TX functions. Note, SGMII TX and 1588 RX are the same direction, which is PHY to MAC. In this mode, arriving frames must have a minimum of three preamble bytes (e.g., 0x55, 0x55, 0x55) to be properly handled and passed along toward SGMII.

FIGURE 5-7: PCH / MCH TX HEADER FORMAT (TOWARD SGMII)

SGMII Format (same Tx and Rx): standard Ethernet preamble									
	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	
IDLE (0x00)	SPD 0xfb	0x55	0x55	0x55	0x55	0x55	0x55	SFD or SMD	Packet Data

SGMII Tx Format: PCH / MCH Header									
	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	
IDLE (0x00)	SPD 0xfb	PktTyp[1:0] SubPort ID[3:0] ExtTy[1:0]	Extension [39:32]	Extension [31:0] Arrival TimeStamp				CRC[7:0]	Packet Data

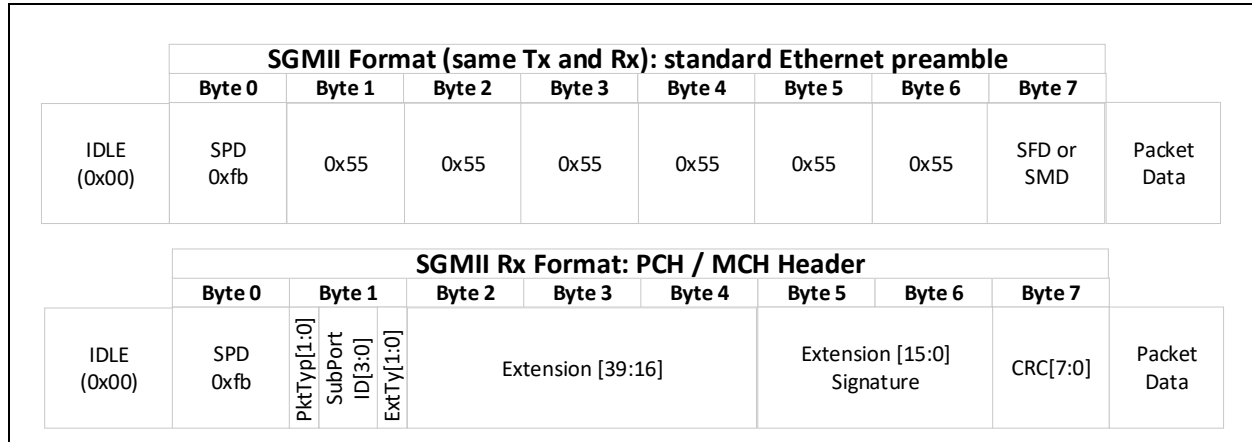
PCH/MCH Bytes 1 and 2 control frame preemption and timestamping. The following values are used:

- PktTyp[1:0]=00 (other values reserved)
- SubPortID[3:0]= 0
- ExtTy[1:0]=01 (preemption disabled on this PHY port) or 10 (preemption enabled on this PHY port). ExtTy will be the same value for all frames on a port.
- Extension[39:32] convey preemption state. Refer to the SGMII specification for details.
 - Preemption Verify and Respond mPackets are passed transparently across the SGMII using Extension values. The device does not generate or respond to these mPackets, it is left to the SGMII link partner to handle Preemption Verification.
- Extension[31:0]=[0,0,30-bit arrival subseconds]
- CRC[7:0]=CRC-8 covering PCH/MCH as per SGMII specification

5.13.3.2 PCH Mode TX

In PCH mode TX, departing frames arrive from the SGMII RX functions with their preamble replaced with a PCH or MCH RX header. 1588 frames of interest are identified by the device based on PCH or MCH header fields. Note, SGMII RX and 1588 TX are the same direction, MAC to PHY.

FIGURE 5-8: PCH / MCH RX HEADER FORMAT (FROM SGMII)



PCH/MCH Bytes 2-4 control frame preemption and timestamping. The following values are used:

- PktTyp[1:0] = '00'
- SubPortID[3:0] = 0
- Extension[39:32] = convey preemption state. Refer to the SGMII specification for details.
 - Preemption Verify and Respond mPackets are passed transparently across the SGMII using Extension values. The device does not generate or respond to these mPackets, it is left to the SGMII link partner to handle Preemption Verification.
- PCH (preemption enabled, PCH only supports two-step):
 - All frames on the port are expected to have ExtTy[1:0] = '10'.
 - However, frames with ExtTy[1:0] = '00' are treated as valid unfragmented frames. These frames will be passed to the line with valid preambles and will not be counted as Extension Type Mismatch errors.
 - Frames with ExtTy[1:0] = '01' or '11' are treated as invalid frames. They are counted as Extension Type Mismatch errors and discarded by the transmit PHY.
 - Extension[31] = indicates a departure timestamp is to be captured for this frame
 - Extension[15:0] = Signature (two-step Frame Signature)
- PCH (preemption disabled, PCH only supports two-step):
 - All frames on the port are expected to have ExtTy[1:0] = '00' or '01'.
 - ExtTy[1:0] = '00' indicates a frame not needing timestamp functions.
 - ExtTy[1:0] = '01' indicates a frame needing timestamp functions.
 - Frames having ExtTy[1:0] = '10' or '11' are treated as invalid frames. They are counted as Extension Type Mismatch errors and discarded by the transmit PHY.
 - Extension[31] = unused/ignore (ExtTy indicates when a departure timestamp is to be captured for this frame)
 - Extension[15:0] = Signature (two-step Frame Signature)
- MCH: Extension[31] = unused/ignore (DataCmd indicates when a departure timestamp operation is to be performed)
- Extension[30:16] = unused/ignore
- MCH: Extension[15] = indicates one-step or two-step
- MCH (preemption enabled):
 - All frames on the port are expected to have ExtTy[1:0] = '10'.
 - However, frames with ExtTy[1:0] = '00' are treated as valid unfragmented frames. These frames will be passed to the line with valid preambles and will not be counted as Extension Type Mismatch errors.

- Frames with ExtTy[1:0] = '01' or '11' are treated as invalid frames. They are counted as Extension Type Mismatch errors and discarded by the transmit PHY.
- MCH (preemption disabled):
 - All frames on the port are expected to have ExtTy[1:0] = '01'.
 - However, frames with ExtTy[1:0] = '00' are treated as valid unfragmented frames. These frames will be passed to the line with valid preambles and will not be counted as Extension Type Mismatch errors.
- Frames with ExtTy[1:0] = '10' or '11' are treated as invalid frames. They are counted as Extension Type Mismatch errors and discarded by the transmit PHY. MCH (two-step):
 - Extension[15] = '0'
 - Extension[14:10] = Signature (Frame Signature for two-step operation)
 - Extension[9] = unused/ignore
 - Extension[8:7] = unused/ignore
 - Extension[6:0] = unused/ignore
- MCH (one-step):
 - Extension[15] = '1'
 - Extension[14:10] = unused/ignore
 - Extension[9] = UdpFix. UdpFix = '1' indicates this is a PTP/UDP/IPv6 frame and the two UDP checksum pad bytes are to be incrementally updated.
 - Extension[8:7] = DataCmd[1:0]. DataCmd[1:0] = '10' indicates this is a PTP frame to be timestamped and the correctionField must be updated using the ADD48_CF (48-bit add) operation. Other values of DataCmd[1:0] are unused by the device and must be ignored (these frames are not timestamped).
 - Extension[6:0] = DataOfs[6:0]. For PTP frames where the correctionField must be updated, this provides the sixteen-bit location of the correctionField, starting with the first 16 bits of packet data following MCH CRC(7:0).
- CRC[7:0] = CRC-8 covering PCH/MCH as per SGMII specification

As previously stated, PCH is a standardized header supporting two-step operation using a Frame Signature. Frames with a valid Frame Signature are processed as 1588 frames. For these frames the departure 80-bit timestamp is captured and placed into the Timestamp FIFO along with the Signature [15:0] field to be read by software over MDIO. Note, the 80-bit timestamp is really only 78 bits, with two bits always set to '00b'.

MCH is a non-standard extension of PCH enabling one-step operation in a PHY without classification capabilities. Frames with MCH DataCmd = '01' = ADD48_CF (48-bit add) are processed as 1588 frames. For these frames, the departure 80-bit timestamp (78 bits plus two bits always set to '00b') is captured and placed into the Timestamp FIFO, along with the following MCH fields:

- For two-step frames, the Signature[14:0] field is put into the Timestamp FIFO along with the departure timestamp and is read by software over MDIO.

PCH/MCH frame signature is read by software via the PTP_TX_MSG_HEADER2 register. Departure timestamp is read by software via the PTP_TX_SYNC_SEC_HI/MID/LO and PTP_TX_SYNC_NS_HI/LO registers.

The MCH processing essentially implements a TC between the PHY and the switch, where the switch has subtracted an arrival value from CF, and the PHY adds the departure timestamp to CF. All other 1588 operations are performed in the switch.

5.13.4 1588 LOCAL TIME COUNTER

The device contains a single 1588 LTC on the port's 1588 Timestamp Engine.

The 1588 LTC is 48 bits of seconds and 30 bits of nanoseconds, plus 32 bits of sub-nanoseconds for precise adjustment. The 1588 LTC runs from a reference clock, which can be either free running to any PHY timing (e.g., 250 MHz based on an independent reference), or locked to PHY timing but not at a frequency which is a direct multiple (e.g., 200 MHz based on the same reference clock as PHY timing).

The 1588 LTC is able to be set (initial load) and adjusted using configuration registers, the external **1588_LD_ADJ** pin, and the ePPS. LTC updates from the external **1588_LD_ADJ** pin and ePPS are configurable to be either one-shot or static (repeating).

The following LTC TOD load options are supported:

- Software-based: TOD is loaded from PTP_LTC_SET_x registers when software writes to the PTP_LTC_LOAD register.

- 1PPS: TOD is loaded from PTP_LTC_SET_x registers when a rising edge is detected on the **1588_LD_ADJ** pin.
- 1PPS with TOD: TOD is loaded when a 1PPS rising edge is detected on the **1588_LD_ADJ** pin, and the TOD is also serially encoded on the same pin.
- ePPS: TOD is loaded from PTP_LTC_SET_x registers when a PPS is detected on the **1588_REF_CLK** pin.

5.13.5 EXTERNAL 1588 INTERFACE

The device provides the following 1588 I/O pins:

- **1588_REF_CLK**: This input pin can provide an independent reference clock to use with the 1588 LTC functions. Other reference clock options are also supported.
 - This pin also supports Embedded 1 Pulse Per Second (ePPS) capability, where the PPS is coded into the clock signal by moving the falling edge of the clock signal at the appropriate time. ePPS is supported by Microchip Timing products and the SparX-5 at 25 MHz clock.
- **1588_LD_ADJ**: This input pin can be used to synchronize one or more LAN8842 1588 LTCs with the system 1588 TOD. This pin controls initial setting (load) and incremental update (adjust) of the internal 1588 LTC. It supports the "1PPS" and "1PPS with TOD" modes described in [Section 5.13.4, "1588 Local Time Counter"](#). Note that while this signal is typically a 1PPS, it can also be a non-repeating signal or a signal which repeats at some rate other than 1 Hz.
- **1588_EVENT_A, 1588_EVENT_B**: These output pins provide notification that a configurable 1588 LTC Event has occurred. The notification is triggered when the internal 1588 LTC has reached the software-configured Event TOD.
 - Either of these pins can also be used as a 1588 PPS OUT signal
- 1588 Event LTC Capture pins: Up to eight GPIOs can be designated as PTP GPIO Capture pins. A transition in the state of any of these input pins causes the 1588 LTC value to be latched in its corresponding set of software-readable PTP GPIO Capture registers, and optionally generate an interrupt. Refer to [Section 5.20, "GPIOs"](#) for details.

The 1PPS with TOD format is as follows (refer to [Section 6.6.12, "1588 1PPS Format and Timing"](#) for additional information.):

- 1PPS: Rising edge indicates the 1PPS position, the pulse width is 1 μ s.
- Waiting: a gap of 20 μ s (logic low) between PPS and TOD
- TOD: 16 TOD octets, each occupies 10 μ s consisting of a start bit (logic high), eight TOD bits (LSB-first) and a stop bit (logic low).
 - The first six octets are Seconds in IEEE 1588-2008 format. The device will use these octets to load the LTC.
 - The next six octets are Date in 0xYYMMHHMMSS decimal format. These octets are ignored by the device.
 - The final four octets are Reserved. These octets are ignored by the device.
- Idle: a gap of 999819 μ s (logic low) between TOD and the next PPS rising edge

The ePPS format is detailed in [Section 6.6.10, "1588_REF_CLK Reference Clock Timing"](#).

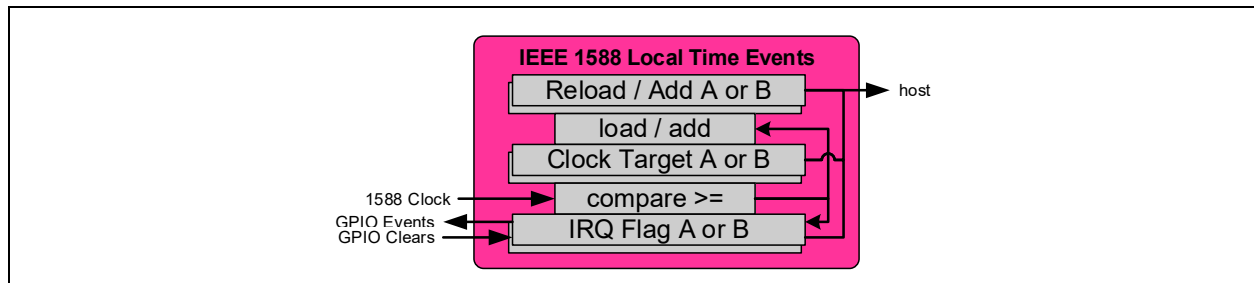
To use external 1588 Interface pins they must be enabled as GPIOs and GPIO Alternate Functions. GPIO Buffer Type and GPIO Direction must also be set appropriately.

5.13.6 1588 LOCAL TIME EVENTS

The Local Time Target reload function (RELOAD_ADD = '1') allows the Host to pre-load the next trigger time in advance. The add function (RELOAD_ADD = '0') allows for a automatic repeatable event. The 1588 Local Time Events block is responsible for generating and controlling all 1588 Local Time related events. Two Local Time event channels, A and B, are available.

A block diagram of the 1588 Local Time Events is shown in Figure 5-9.

FIGURE 5-9: 1588 LOCAL TIME EVENTS TARGET BLOCK DIAGRAM



For each Local Time event channel, a comparator compares the 1588 Local Time Counter with a Local Time Target loaded in the PTP LTC Target x Seconds High/Low Registers (PTP_LTC_TARGET_SEC_HI/LO_x) and PTP LTC Target x Nanoseconds High/Low Registers (PTP_LTC_TARGET_NS_HI/LO_x). Only the lower 32 bits of seconds is considered.

The Local Time Target register set requires four 16-bit write cycles, one to each quarter, before the register set is affected. The writes may be in any order. There is a register set for each Local Time event channel (A and B).

The Local Time Target can be read by setting the LTC Target Read (PTP_LTC_TARGET_READ) bit in the PTP Command and Control register (PTP_CMD_CTL). This saves the current value of the both Local Time Targets (A and B) into the PTP LTC Target x Seconds High/Low Registers (PTP_LTC_TARGET_SEC_HI/LO_x) and PTP LTC Target x Nanoseconds High/Low Registers (PTP_LTC_TARGET_NS_HI/LO_x) where they can be read.

When the 1588 Local Time Counter reaches or passes the Local Time Target for a Local Time event channel, a Local Time event occurs, which triggers the following:

- The maskable interrupt for that Local Time event channel (PTP Timer Interrupt A (PTP_TIMER_INT_A) or PTP Timer Interrupt B (PTP_TIMER_INT_B)) is set in the PTP Interrupt Status register (PTP_INT_STS).
- The PTP LTC Target x Actual Nanoseconds High/Low Registers is loaded from the nanoseconds portion of the 1588 Local Time Counter.

APPLICATION NOTE: Since the Local Time Target compare is a “greater than or equals to” function, it is possible that it triggers with the 1588 Local Time Counter exceeding the Local Time Target value. These registers can be used to account for the variation.

- The Reload/Add A (RELOAD_ADD_A) or Reload/Add B (RELOAD_ADD_B) bit in the PTP General Configuration register (PTP_GENERAL_CONFIG) is checked to determine the new Local Time Target behavior:
 - RELOAD_ADD = ‘1’:

The new Local Time Target is loaded from the Reload/Add Registers (PTP LTC Target x Reload/Add Seconds High/Low Registers (PTP_LTC_TARGET_RELOAD_SEC_HI/LO_x) and PTP LTC Target x Reload/Add Nanoseconds High/Low Registers (PTP_LTC_TARGET_RELOAD_NS_HI/LO_x)).
 - RELOAD_ADD = ‘0’:

The Local Time Target is incremented by the Reload/Add Registers (PTP LTC Target x Reload/Add Seconds High/Low Registers (PTP_LTC_TARGET_RELOAD_SEC_HI/LO_x) and PTP LTC Target x Reload/Add Nanoseconds High/Low Registers (PTP_LTC_TARGET_RELOAD_NS_HI/LO_x)). The Local Time Target Nanoseconds rolls over at 10^9 and the carry is added to the Local Time Target Seconds.

The Local Time Target Reload/Add register set requires four 16-bit write cycles, one to each quarter, before the register set is affected. The writes may be in any order. There is a register set for each Local Time event channel (A and B).

Note: Writing the 1588 Local Time Counter may cause the interrupt event to occur if the new 1588 Local Time Counter value is set equal to or greater than the current Local Time Target.

5.13.7 1588 GPIOs

In addition to time stamping PTP packets, the 1588 Local Time Counter value can be saved into a set of Local Time capture registers based on the GPIO inputs. The GPIO inputs can also be used to clear the 1588 Local Time Target compare event interrupt. When configured as outputs, GPIOs can be used to output a signal based on an 1588 Local Time Target compare events. Refer to [Section 5.20, "GPIOs"](#) for additional information.

5.13.8 1588 PROCESSING ENABLE/DISABLE

1588 chip functions such as Local Time Counter are enabled when the PTP Enable (PTP_ENABLE) bit in the PTP Command and Control register (PTP_CMD_CTL) is set.

1588 packet processing functions (detection, frame modification, etc.) are enabled on the port using the Time-Stamp Unit Enable (TSU_ENABLE) bit in the port TSU General Configuration register (TSU_GENERAL_CONFIG).

APPLICATION NOTE: The setting of PTP Enable (PTP_ENABLE) without setting Time-Stamp Unit Enable (TSU_ENABLE) allows the 1588 Local Time Counter, Local Time Target and GPIOs, etc. to be used without network interaction.

APPLICATION NOTE: 1588 packet processing requires TSU_ENABLE to be set for the port and PTP_ENABLE to be set for the chip. TSU functions may be initially configured by assuring PTP_ENABLE is cleared (TSU_ENABLE can be either set or cleared in this case). TSU functions may also be configured while other 1588 functions are running by assuring TSU_ENABLE is cleared (PTP_ENABLE is typically already set in this case).

If the PTP Disable (PTP_DISABLE) bit is set, any frame modifications in process are completed, however no modifications are made to subsequent frames. Once all sub-modules are idle, the PTP Enable (PTP_ENABLE) and PTP Disable (PTP_DISABLE) bits are cleared.

When the PTP Enable (PTP_ENABLE) bit goes low, the 1588 Local Time Counter is halted, no packet detection is performed, no GPIO timestamping is performed, no GPIO event indication is done and no frame modifications are performed. Ingress and egress frames are passed without any pipeline delays. Register writes are still allowed and any register status is preserved.

5.13.9 1588 TIMING

For 1588 timing information, refer to the following [Section 6.6, "AC Specifications"](#) sub-sections:

- [1588 GPIO Timing](#)
- [1588_REF_CLK Reference Clock Timing](#)
- [1588_LD_ADJ Timing](#)
- [1588 1PPS Format and Timing](#)
- [1588_EVENT_A/B Timing](#)
- [GPIO PTP Capture Timing](#)
- [RCVRD_CLK_OUT1/2 Timing](#)

5.14 Energy Efficient Ethernet (EEE)

The device implements Energy Efficient Ethernet (EEE) as described in IEEE Standard 802.3az. The specification is defined around an EEE-compliant MAC on the host side and an EEE-compliant link partner on the line side that support the special signaling associated with EEE. EEE saves power by keeping the AC signal on the copper Ethernet cable at approximately 0V peak-to-peak as often as possible during periods of no traffic activity, while maintaining the link-up status. This is referred to as Low Power Idle (LPI) mode or state.

As set by the **MODE_SEL[4:0]** configuration straps, the device has the EEE function enabled or disabled as the power-up default setting. The EEE function can be enabled or disabled by setting or clearing the following EEE advertisement bits in the EEE Advertisement register (MDIO Manageable Device (MMD) Address 7h, register 3Ch), followed by restarting auto-negotiation (writing a '1' to the Basic Control register, bit[9]):

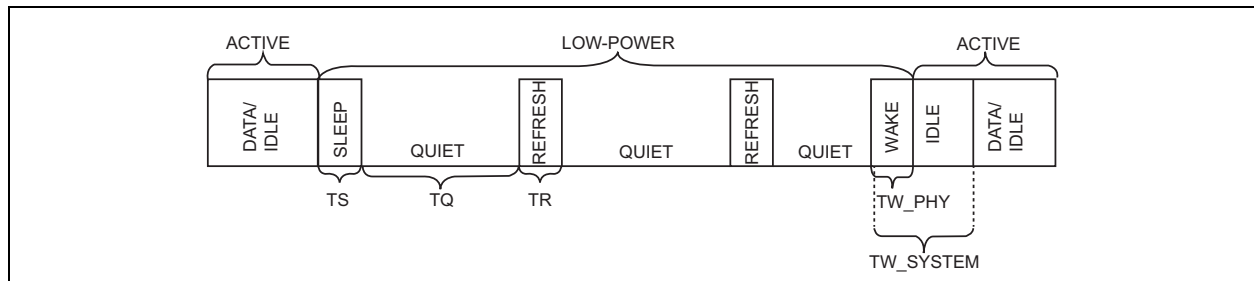
- 1000BASE-T EEE (bit[2]) = '0/1' // Disable/Enable 1000 Mbps EEE mode
- 100BASE-TX EEE (bit[1]) = '0/1' // Disable/Enable 100 Mbps EEE mode

During LPI mode, the copper link responds automatically when it receives traffic and resumes normal PHY operation immediately, without blockage of traffic or loss of packet. This involves exiting LPI mode and returning to normal 100/1000 Mbps operating mode. Wake-up times are $<16\ \mu\text{s}$ for 1000BASE-T and $<30\ \mu\text{s}$ for 100BASE-TX. The LPI state is controlled independently for transmit and receive paths, allowing the LPI state to be active (enabled) for:

- Transmit cable path only
- Receive cable path only
- Both transmit and receive cable paths

During LPI mode, refresh transmissions are used to maintain the link; power savings occur in quiet periods. Approximately every 20 to 22 milliseconds, a refresh transmission of 200 to 220 microseconds is sent to the link partner. The refresh transmissions and quiet periods are shown in Figure 5-10.

FIGURE 5-10: LPI MODE (REFRESH TRANSMISSIONS AND QUIET PERIODS)



5.14.1 TRANSMIT DIRECTION CONTROL (MAC-TO-PHY)

The PHY enters the LPI Sleep state for the transmit direction when the attached IEEE-compliant MAC asserts the LPI opcode toward the PHY. The PHY remains in the transmit LPI Sleep state until the attached IEEE-compliant MAC asserts a non-LPI opcode toward the PHY. While in the LPI Sleep state, the PHY will periodically send Refreshes to the IEEE-compliant Link Partner to maintain the Link, clock recovery, etc.

5.14.2 RECEIVE DIRECTION CONTROL (PHY-TO-MAC)

The PHY enters LPI mode for the receive direction when it receives the /P/ code bit pattern (Sleep/Refresh) from its IEEE-compliant Link Partner. The PHY will pass the Sleep Request to the attached IEEE-compliant MAC. The PHY remains in the receive LPI Sleep state while it continues to receive Refreshes from its Link Partner, and it will continue to inform the attached IEEE-compliant MAC that it is in the receive LPI Sleep state. When the PHY receives a non /P/ code bit pattern (non-refresh), it exits the receive LPI Sleep state and signals a normal frame or normal idle to the attached IEEE-compliant MAC.

5.15 IEEE 802.3-2022 Frame Preemption

IEEE Standard 802.3-2022, [1.0] specifies a method for interspersing express traffic by preempting the transmission of a normal packet, transmitting the express packet and then resuming the normal packet. The receiver likewise reassembles the fragmented normal packet.

The preemption and reassembly is performed using an mPacket format as defined in 802.3 Clause 99. This mPacket format starts with the normal preamble but supplements the normal Start of Frame Delimiter (SFD = 0xD5) with newly defined Start mPacket Delimiters (SMDs) of various values. Also added for certain mPackets is a fragment count octet.

If Frame Preemption is not in use, the SFD appears ahead of every Ethernet frame on the PHY port. If Frame Preemption is in use, one of several possible SMDs may appear in place of the SFD on the PHY port. When there is no PCH/MCH header using SGMII, the SMD and SFD characters are passed transparently across SGMII. When the PCH/MCH header is enabled, the SMD and SFD characters are passed across SGMII inside the PCH or MCH header. See the IEEE 1588 PCH mode sections for format specifics. 1588 processing is supported with Frame Preemption but only for Express frames.

Section 5.17, "Start of Frame Indication" defines SOF pulse generation support for the SMDs.

APPLICATION NOTE: Preemption is not supported at 10 Mbps.

5.16 Loopbacks

The device supports the following loopback operations to verify analog and/or digital paths:

- [Digital \(Near-End\) Loopback](#)
- [Remote \(Far-End\) Loopback](#)
- [External Connector Loopback](#)
- [SGMII Loopback](#)

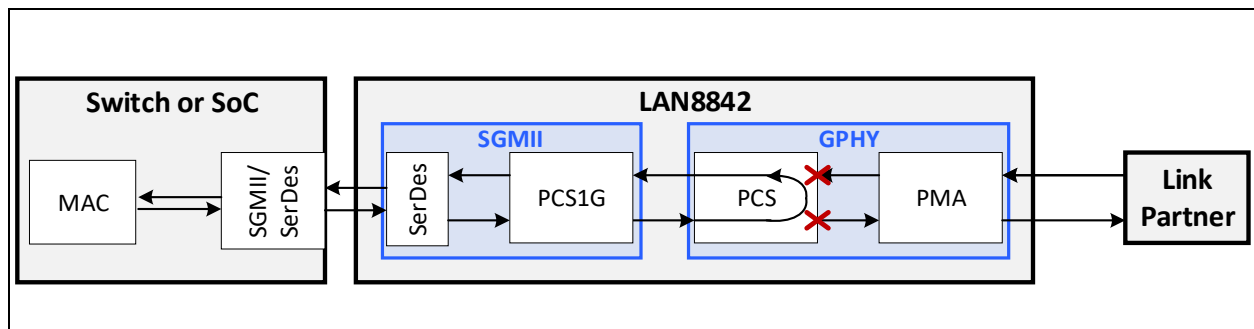
5.16.1 DIGITAL (NEAR-END) LOOPBACK

This loopback mode checks the SGMII transmit and receive data paths between the device and the external MAC, and is supported for all three speeds (10/100/1000 Mbps) at full-duplex.

The loopback data path is shown in [Figure 5-11](#).

1. SGMII MAC transmits frames to the device.
2. Frames are wrapped around inside the device.
3. The device transmits frames back to SGMII MAC.

FIGURE 5-11: DIGITAL (NEAR-END) LOOPBACK



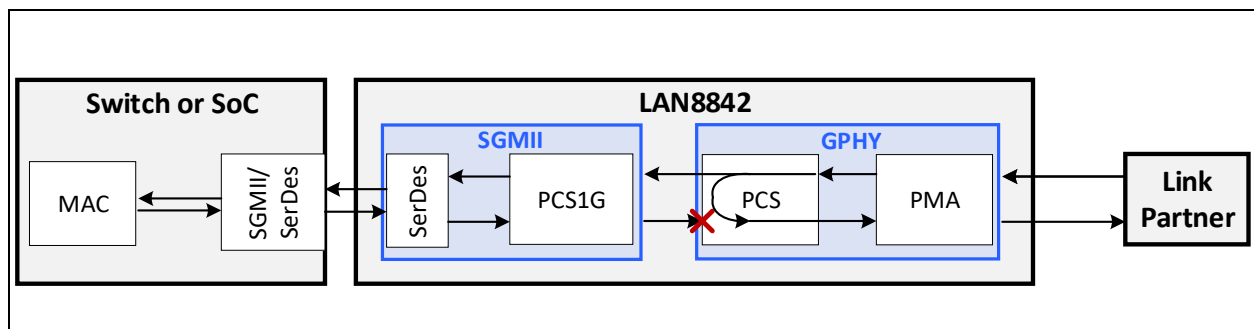
5.16.2 REMOTE (FAR-END) LOOPBACK

This loopback mode checks the line (differential pairs, transformer, RJ-45 connector, Ethernet cable) transmit and receive data paths between the device and its link partner, and is supported for 1000BASE-T full-duplex mode only.

The loopback data path is shown in [Figure 5-12](#).

1. The Gigabit PHY link partner transmits frames to the device.
2. Frames are wrapped around inside the device.
3. The device transmits frames back to the Gigabit PHY link partner.

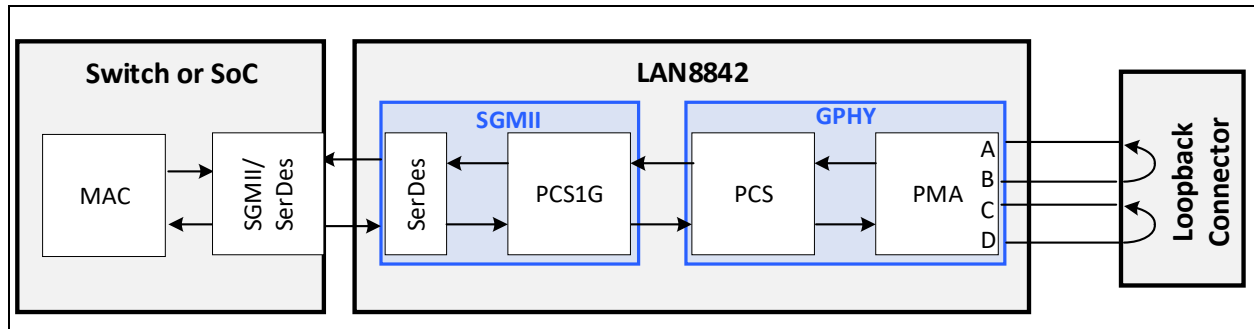
FIGURE 5-12: REMOTE (FAR-END) LOOPBACK



5.16.3 EXTERNAL CONNECTOR LOOPBACK

The external connector loopback testing feature allows the twisted pair interface to be looped back externally. This loopback tests the PHY digital and MAC connectivity. When using this feature, the PHY must be connected to a loopback connector or a loopback cable. Pair A must be connected to pair B, and pair C to pair D, as shown in Figure 5-13. The connector loopback feature functions at all available interface speeds.

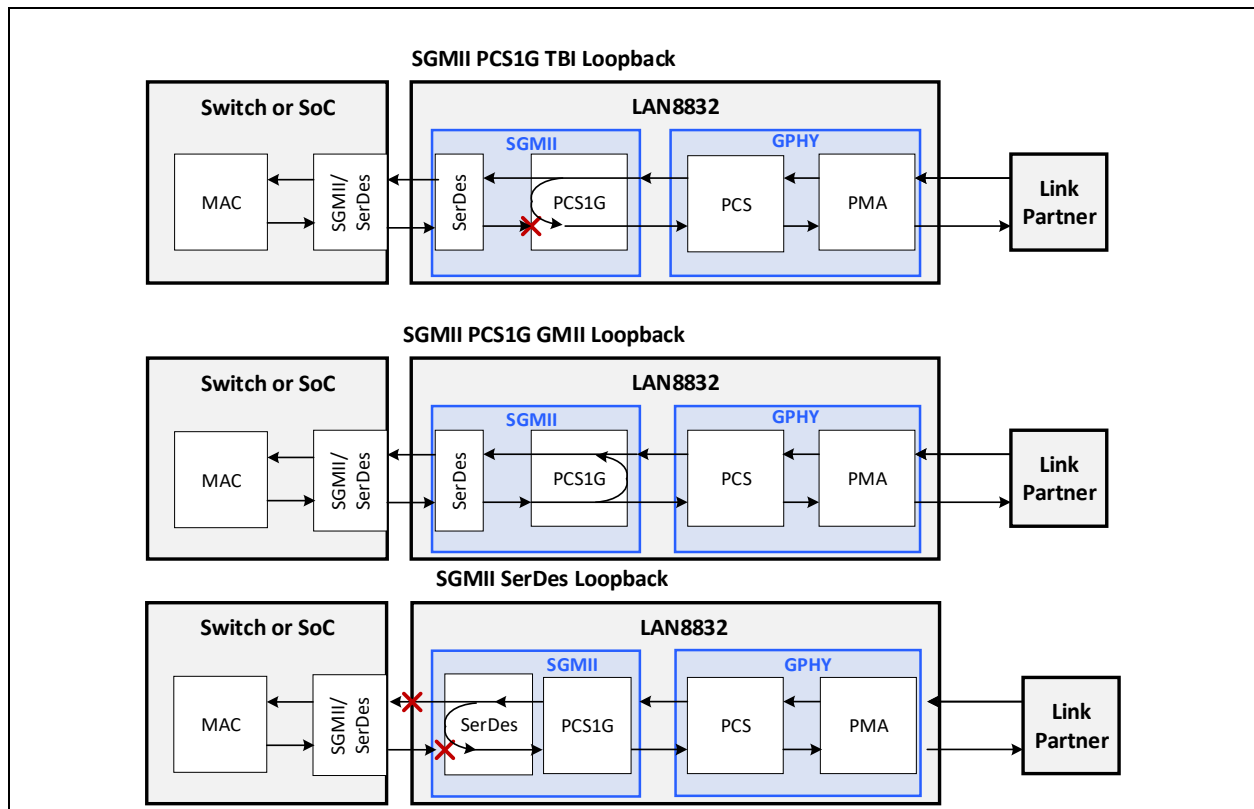
FIGURE 5-13: EXTERNAL CONNECTOR LOOPBACK



5.16.4 SGMII LOOPBACK

The SGMII loopback testing feature calls various portions of the SGMII block to be tested, as shown in Figure 5-14.

FIGURE 5-14: SGMII LOOPBACK



5.17 Start of Frame Indication

The device supports the generation of an SOF pulse for the receive and transmit paths. The SOF pulse is generated when the Start of Frame Delimiter (SFD octet 0xD5 immediately following the preamble) is detected by the PCS and can be output onto any enabled GPIO pin by setting the corresponding bits in the General Purpose IO Data Select 1 register (GPIO_DATA_SEL1) or the General Purpose IO Data Select 2 register (GPIO_DATA_SEL2). The SOF pulse is always active high. For details on SOF detection timing, refer to [Section 6.6.8, "GPIO SOF Detection Timing"](#).

Note: The GPIO needs to be enabled and its direction set as an output via the General Purpose IO Enable register (GPIO_EN) and the General Purpose IO Direction register (GPIO_DIR). The GPIO Buffer Type (GPIO_BUF) field in the General Purpose IO Buffer Type register (GPIO_BUF) also applies.

The SOF pulse can also be configured to detect 802.3-2022 SMDs. When the SOF_preemption_enable bits in MMD2 register 75 are set to "10", the SOF pulse is generated for any of the SMD values listed in 802.3-2022 *except* for the continuation frame: SMD-V (0x07), SMD-R (0x19), SMD-E (0xD5) and SMD-S[0,1,2,3] (0xE6, 0x4C, 0x7F or 0xB3). When the SOF_preemption_enable bits are set to '11', the SOF pulse is also generated for the continuation SMD values: SMD-C[0,1,2,3] (0x61, 0x52, 0x9E or 0x2A).

5.18 MIIM (MDIO) Interface

The device supports the IEEE 802.3 MII management interface, also known as the Management Data Input/Output (MDIO) interface. This interface allows upper-layer devices to monitor and control the state of the device. An external device with MIIM capability is used to read the PHY status and/or configure the PHY settings. More details about the MIIM interface can be found in Clause 22.2.4 of the IEEE 802.3 Specification [\[1\]](#).

The MIIM interface consists of the following:

- A physical connection that incorporates the clock line (**MDC**) and the data line (**MDIO**).
- A specific protocol that operates across the physical connection mentioned earlier, which allows an external controller to communicate with one or more devices. Each device is assigned a unique PHY address between 0h and 1Fh by the **PHYAD[4:0]** strapping pins. Refer to [Section 3.3.2, "PHY Address \(PHYAD\[4:0\]\)"](#) for additional information.
- A 32-register address space for direct access to IEEE-defined registers and vendor-specific registers, and for indirect access to MMD addresses and registers.

[Table 5-7](#) shows the MII management frame format for the device.

TABLE 5-7: MII MANAGEMENT FRAME FORMAT

	Preamble	Start of Frame	Read/Write OP Code	PHY Address Bits[4:0]	REG Address Bits[4:0]	TA	Data Bits[15:0]	Idle
Read	32 1's	01	10	AAAAA	RRRRR	Z0	DDDDDDDD_DDDDDDDD	Z
Write	32 1's	01	01	AAAAA	RRRRR	10	DDDDDDDD_DDDDDDDD	Z

Note: This device may respond to Clause 45 accesses and so must not be mixed with Clause 45 devices on the same MDIO bus. MDIO supports Clause 22 and the indirect Clause 45 method using Clause 22 registers. Clause 45 direct access is not supported.

5.18.1 HIGH-SPEED MDIO OPERATION

The MDIO bus can operate at standard speeds up to 2.5 MHz, as well as higher speeds up to 25 MHz. Default register values enable standard MDIO operation using open-drain MDIO drivers, which is MDIO operation up to 2.5 MHz MDC frequency with daisy-chained PHYs on the MDIO bus. Due to open-drain drivers, an external 1kΩ pull-up resistor is required.

Higher speed MDIO operation up to 25 MHz is supportable but requires reconfiguring the device to use push-pull MDIO drivers, and does not allow daisy-chaining PHYs on the MDIO bus. The reconfiguration process requires initially running the MDIO bus at 2.5 MHz using open-drain MDIO drivers and the external 1 kΩ pull-up resistor. The push-pull MDIO drivers allow operation up to 25 MHz with the 1kΩ pull-up resistor.

5.18.2 MDIO OUTPUT DRIVE MODE

The **MDIO** output pin drive mode is controlled by the MDIO Buffer Type bit in the Output Control register. When set to a '0', the **MDIO** output is open-drain. When set to '1', the **MDIO** output is push-pull.

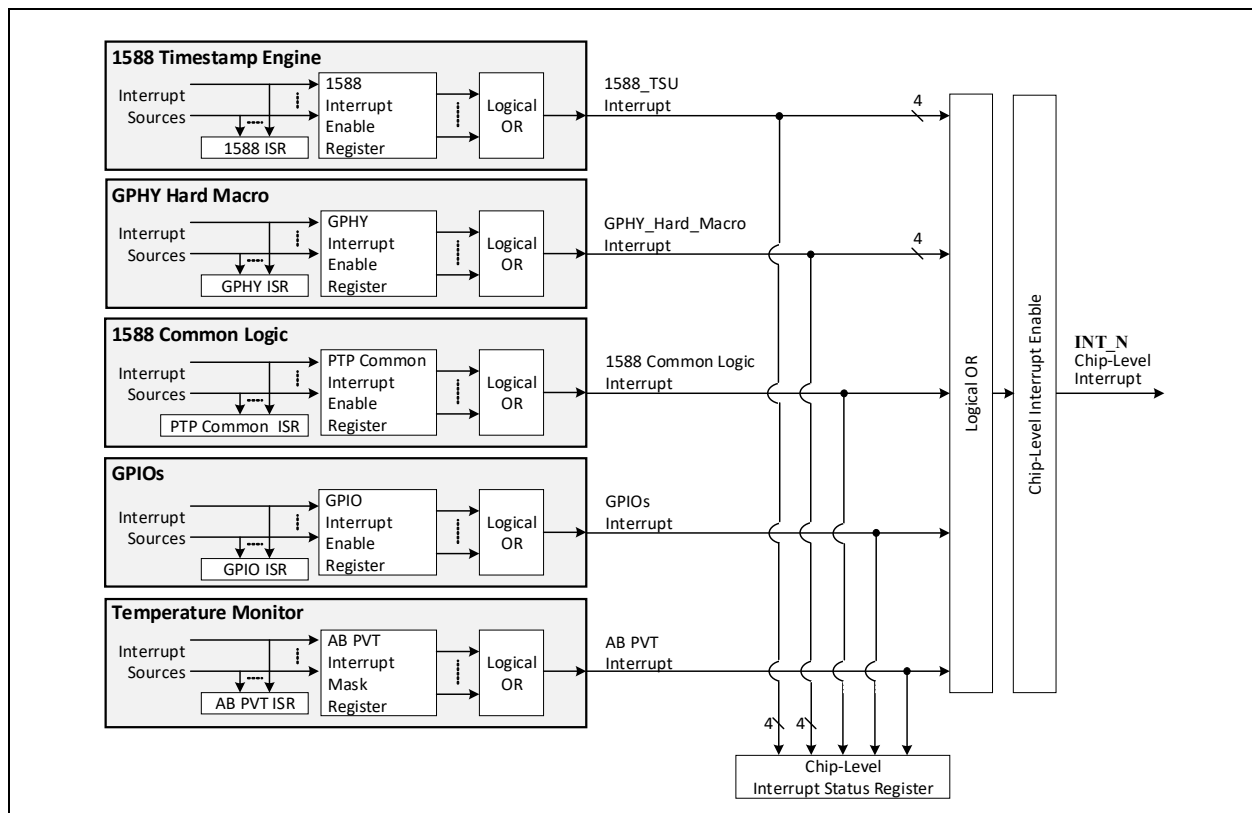
5.19 Interrupts

The **INT_N** pin is an optional interrupt signal that is used to inform the external controller that there has been a status update in the device. The Interrupt Enable register contains the interrupt control bits that enable and disable the conditions for asserting the **INT_N** signal. The Interrupt Status register contains the interrupt status bits that indicate which interrupt conditions have occurred. Most interrupt status bits are cleared upon reading. Some bits are read only and have a lower level register to indicate individual sources.

Note: Bits in the Interrupt Status register are set by the interrupt events regardless of the value of the corresponding bits in the Interrupt Enable register.

The interrupt structure of the device is detailed in [Figure 5-15](#).

FIGURE 5-15: INTERRUPT STRUCTURE



The **INT_N** buffer type is selectable between open-drain and push-pull and is configured by the INT Buffer Type field in the Output Control register. The default is open-drain.

The Intr Polarity Invert bit in the Control register sets the interrupt level to active high or active low. The default is active low. If the buffer type is set to open-drain, the polarity is forced to be active low.

5.20 GPIOs

The General Purpose I/Os (GPIOs) consist of 16 programmable input/output pins that are shared with other pins. These pins are individually configurable via the GPIO registers.

GPIOs support the following functions:

- Software-readable GPIO. The GPIO is an input and its value can be directly read via the GPIO Data register. In addition, these GPIOs can also be configured to generate interrupts and PTP GPIO Capture events, and clear the PTP Timer interrupt.
- Software-writable GPIO. The GPIO is an output and its value can be directly set via the GPIO Data register.
- GPIO Alternate Function. The GPIO pin is shared with some other function. Depending on the alternate function, the GPIO pin may be either an input or output. If the GPIO pin is an input, it can still be configured to perform any GPIO input function in addition to the alternate function.

For a pin to function as its GPIO, the GPIO must be enabled via the corresponding bit in the GPIO Enable Registers.

When configured as an input, via the GPIO Direction register (GPIO_DIR1 or GPIO_DIR2), the pin's pull-up is enabled. Each bit in the GPIO Data Registers reflects the current state of the corresponding GPIO input.

Note: Extreme care must be taken on strap input pins that may be used for General Purpose Inputs. The General Purpose Inputs must be conditioned or otherwise disabled such that they do not drive incorrect strap input values during the strap loading time.

When configured as an output, the output buffer type is selected by the corresponding bit in the GPIO Buffer Type Registers. Push/pull and open-drain output buffers are supported for each GPIO.

- When functioning as an open-drain driver, the GPIO output pin is driven low when the corresponding bit in the GPIO Data Registers is cleared to '0' and is not driven when set to '1'.
- When functioning as a push/pull output, the GPIO output pin is driven low or high by the corresponding bit in the GPIO Data Registers.

When a GPIO is set to an output, the pin's pull-up is disabled, however the pin's input buffer remains enabled. A read of the GPIO Data Registers returns the state of the GPIO inputs (not the previous values written to these registers).

5.20.1 GPIO ALTERNATE FUNCTIONS

Many GPIOs have the ability to be used as an alternate function. Once enabled as a GPIO, the alternate function is selected by the bits in the GPIO Alternate Function Select Registers.

The alternate function buffer type is still selected via the GPIO Buffer Type Registers. If the alternate function is a Port LED and the GPIO Buffer Type is open-drain, the output buffer will automatically select between open-source and open-drain based on the applicable LED Polarity.

Alternate Functions input pins can be read by software via the GPIO Data register, can generate GPIO Interrupts. [Table 5-8](#) describes the alternate function mappings. Alternate functions are each described fully in [Section 3.0, "Pin Descriptions and Configuration"](#).

TABLE 5-8: GPIO ALTERNATE FUNCTIONS

GPIO	Alternate Function	Configuration Strap	Reset State		Comments
GPIO15	LED2	<u>PHYAD4/LED2_POL</u>	In	PD	To enable LED operation with either a pull-up or pull-down, LED Polarity takes on the inverted value of the configuration strap. Refer to Section 5.21, "LEDs" and Section 3.3.4, "LED Polarity (LED[2:1]_POL)" for additional information.
GPIO14	LED1	<u>PHYAD3/LED1_POL</u>	In	PD	
GPIO13	SOF	<u>PHYAD2</u>	In	PD	
GPIO12	—	<u>PHYAD1</u>	In	PD	
GPIO11	CK25OUT	<u>PHYAD0</u>	In	PD	
GPIO10	RCVRD_CLK_OUT2	—	In	PD	—
GPIO9	RCVRD_CLK_OUT1		In	PD	
GPIO8	RCVRD_CLK_IN2		In	PD	
GPIO7	RCVRD_CLK_IN1		In	PD	
GPIO6	—	<u>MODE_SEL4</u>	In	PU	
GPIO5	—	<u>MODE_SEL3</u>	In	PU	
GPIO4	—	<u>MODE_SEL2</u>	In	PD	
GPIO3	1588_LD_ADJ	<u>MODE_SEL1</u>	In	PD	
GPIO2	1588_REF_CLK	—	In	PD	
GPIO1	1588_EVENT_B	<u>MODE_SEL0</u>	In	PD	
GPIO0	1588_EVENT_A	<u>LED_MODE</u>	In	PD	

Note: PD = Pulled Down
PU = Pulled Up

Note: The following must be considered when using GPIOs:

- Configuring a pin as a GPIO input automatically enables an internal pull-up.
- Internal pull-up resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled high, an external resistor must be added.
- Configuring a pin as a GPIO output automatically disables the internal pull-up. Open-drain outputs may require an external pull-up depending on the application.

5.20.2 GPIO INTERRUPTS

Each GPIO provides the ability to trigger a unique GPIO interrupt in the GPIO Interrupt Status Registers. Reading the GPIO Interrupt Status Registers provides the current status of all GPIO interrupts. Each interrupt is enabled by setting the corresponding bit in the GPIO Interrupt Enable Registers. The GPIO Controller aggregates the enabled interrupt values into an internal signal that is sent to the main interrupt logic and is reflected via the GPIO Interrupt bit in the Chip-level Interrupt Status register.

Bits in the GPIO Interrupt Status Registers are set by the interrupt events regardless of the value of the corresponding bits in the GPIO Interrupt Enable Registers.

Note: Upon reset, GPIOs that were outputs may generate an active interrupt status as the system settles - typically when a low GPIO pin slowly rises due to the internal pull-up. The interrupt status bits within the GPIO Interrupt Status Registers must be cleared as part of the device initialization software routine.

Each GPIO interrupt polarity can be set individually via the GPIO Interrupt Polarity Registers. When the Interrupt Polarity bit is set to '1', a high logic level on the GPIO pin will set the corresponding interrupt bit in the GPIO Interrupt Status Registers. When the Interrupt Polarity bit is set to '0', a low logic level on the GPIO pin will set the corresponding interrupt bit in the GPIO Interrupt Status Registers.

Any two GPIOs can optionally be used to clear the PTP Timer Interrupt A and PTP Timer Interrupt B, configured using the PTP GPIO Interrupt Clear Configuration register.

5.20.3 PTP GPIO CAPTURE REGISTERS

Eight GPIOs can be configured to generate PTP GPIO Capture events, stored in eight corresponding PTP GPIO Capture register sets. GPIOs [15:0] are available for this purpose and are selected via the PTP GPIO Capture Map Registers.

When a GPIO is configured as an Input and PTP GPIO Capture is enabled via the corresponding bit in the PTP GPIO Capture Enable register, a rising or falling edge on the GPIO will capture the 1588 LTC value in the corresponding PTP GPIO Capture register. Rising or falling edge capture behavior is also configured in the PTP GPIO Capture Enable Registers.

Eight PTP GPIO Capture register sets exist with each set consisting of the following (where "x" is a value between 1 and 8):

- PTP GPIO x Rising Edge LTC Seconds High Capture register
- PTP GPIO x Rising Edge LTC Seconds Low Capture register
- PTP GPIO x Rising Edge LTC Nanoseconds High Capture register
- PTP GPIO x Rising Edge LTC Nanoseconds Low Capture register
- PTP GPIO x Falling Edge LTC Seconds High Capture register
- PTP GPIO x Falling Edge LTC Seconds Low Capture register
- PTP GPIO x Falling Edge LTC Nanoseconds High Capture register
- PTP GPIO x Falling Edge LTC Nanoseconds Low Capture register

Capture status of each PTP GPIO Capture register set is provided in the PTP GPIO Capture Status register and the corresponding PTP_GPIO interrupt is asserted.

A Lock bit for each GPIO is also provided in the PTP GPIO Capture Lock register, which prevents the corresponding PTP GPIO Capture Registers from being overwritten (and another interrupt generated) if the corresponding PTP GPIO Capture Status is already set.

Software can also trigger a Manual PTP Capture into one configurable PTP GPIO Capture register set.

5.20.4 GPIO TIMING

For GPIO timing information, refer to the following [Section 6.6, "AC Specifications"](#) sub-sections:

- [GPIO Timing](#)
- [GPIO SOF Detection Timing](#)
- [1588 GPIO Timing](#)

5.21 LEDs

The device provides two programmable LEDs which are configurable to support multiple LED modes. The LED mode is configured by the **LED_MODE** configuration strap as well as the LED Control Registers 1 and 2. The supported LED modes are:

- [Individual-LED Mode](#) (LED Control Register 1, bit[6] (KSZ0931 LED mode) = '1', **LED_MODE** pulled-up)
- [Tri-color-LED Mode](#) (LED Control Register 1, bit[6] (KSZ0931 LED mode) = '1', **LED_MODE** pulled-down)
- [Enhanced LED Mode](#) (LED Control Register 1, bit[6] (KSZ0931 LED mode) = '0', **LED_MODE** unused)

To use LEDs, they must be enabled as GPIOs and GPIO Alternate Functions. The GPIOs must be configured as Outputs, and the proper output driver type selected (open-drain or push-pull). If open-drain type is selected, the output driver will automatically choose between open-source and open-drain based on LED polarity.

The **LED[2:1]_POL** configuration straps set the default polarity of the LED pins. Refer to [Section 3.3.4, "LED Polarity \(LED\[2:1\]_POL\)"](#) for additional LED polarity information. Refer to [Section 3.3.3, "LED Mode Select \(LED_MODE\)"](#) for additional **LED_MODE** information.

Note: Coma mode disables all LED functions. When the Coma mode input transitions from low to high, LED functions begin normal operation. Refer to [Section 5.24, "Coma Mode"](#) for additional information.

5.21.1 INDIVIDUAL-LED MODE

In Individual-LED mode, the **LED2** pin indicates the link status while the **LED1** pin indicates the activity status, as shown in [Table 5-9](#).

Note: The LEDs are forced off when any of the following occurs:

- The Isolate (PHY_ISO) bit in the Basic Control register is set.
- The Power Down bit in the Basic Control register is set.
- Coma mode is asserted via the **COMA_MODE** pin.

TABLE 5-9: INDIVIDUAL-LED MODE OPERATION

LED2	LED1	Definition
Inactive	Inactive	No link
Active	Inactive	Link any speed, no activity
Active	Blinking	Link any speed, TX or RX activity
Other States		N/A

5.21.2 TRI-COLOR-LED MODE

In Tri-color-LED mode, the link and activity status are indicated by the **LED2** pin for 1000BASE-T; by the **LED1** pin for 100BASE-TX; and by both **LED2** and **LED1** pins, working in conjunction, for 10BASE-T. This is summarized in [Table 5-10](#).

Note: The LEDs are forced off when any of the following occurs:

- The Isolate (PHY_ISO) bit in the Basic Control register is set.
- The Power Down bit in the Basic Control register is set.
- Coma mode is asserted via the **COMA_MODE** pin.

TABLE 5-10: TRI-COLOR-LED MODE OPERATION

LED2	LED1	Definition
Inactive	Inactive	No link
Inactive	Active	100 Mbps link, no activity
Inactive	Blinking	100 Mbps link, TX or RX activity
Active	Inactive	1000 Mbps link, no activity
Blinking	Inactive	1000 Mbps link, TX or RX activity

TABLE 5-10: TRI-COLOR-LED MODE OPERATION (CONTINUED)

LED2	LED1	Definition
Active	Active	10 Mbps link, no activity
Blinking	Blinking	10 Mbps link, TX or RX activity
Other States		N/A

5.21.3 ENHANCED LED MODE

Enhanced mode is enabled when the KSZ9031 LED mode bit in the corresponding port's LED Control Register 1 is cleared. In Enhanced LED mode, each LED can be configured to display different status information that can be selected by setting the corresponding LED Configuration field of the port's LED Control Register 2. The modes are detailed in [Table 5-11](#). The blink/pulse-stretch and other LED setting can be configured via the LED Behavior register.

- Note:** The LEDs are forced off when any of the following occurs:
- The Isolate (PHY_ISO) bit in the Basic Control register is set.
 - The Power Down bit in the Basic Control register is set.
 - Coma mode is asserted via the **COMA_MODE** pin.

TABLE 5-11: EXTENDED MODE OPERATION

Mode	LEDx	Definition
Enhanced Mode 0 (Link/Activity)	Inactive	No link
	Active	Link any speed, no activity any speed
	Blinking	Link any speed, activity any speed
Enhanced Mode 1 (Link1000/Activity)	Inactive	No 1000 Mbps link
	Active	1000 Mbps link, no 1000 Mbps activity
	Blinking	1000 Mbps link, 1000 Mbps activity
Enhanced Mode 2 (Link100/Activity)	Inactive	No 100 Mbps link
	Active	100 Mbps link, no 100 Mbps activity
	Blinking	100 Mbps link, 100 Mbps activity
Enhanced Mode 3 (Link10/Activity)	Inactive	No 10 Mbps link
	Active	10 Mbps link, no 10 Mbps activity
	Blinking	10 Mbps link, 10 Mbps activity
Enhanced Mode 4 (Link100/1000/Activity)	Inactive	No 100/1000 Mbps link
	Active	100/1000 Mbps link, no 100/1000 Mbps activity
	Blinking	100/1000 Mbps link, 100/1000 Mbps activity
Enhanced Mode 5 (Link10/1000/Activity)	Inactive	No 10/1000 Mbps link
	Active	10/1000 Mbps link, no 10/1000 Mbps activity
	Blinking	10/1000 Mbps link, 10/1000 Mbps activity

TABLE 5-11: EXTENDED MODE OPERATION (CONTINUED)

Mode	LEDx	Definition
Enhanced Mode 6 (Link10/100/Activity)	Inactive	No 10/100 Mbps link
	Active	10/100 Mbps link, no 10/100 Mbps activity
	Blinking	10/100 Mbps link, 10/100 Mbps activity
Enhanced Mode 7	N/A	Reserved
Enhanced Mode 8 (Duplex/Collision)	Inactive	Half-Duplex link or no link
	Active	Full-Duplex link
	Blinking	Half-Duplex link, collisions detected
Enhanced Mode 9 (Collision)	Inactive	No collisions detected
	Active	N/A
	Blinking	Collisions detected
Enhanced Mode 10 (Activity)	Inactive	No activity
	Active	N/A
	Blinking	Activity
Enhanced Mode 11	N/A	Reserved
Enhanced Mode 12 (Parallel Detect Fault)	Inactive	No parallel detect fault
	Active	Parallel detect fault
	Blinking	N/A
Enhanced Mode 13	N/A	Reserved
Enhanced Mode 14 (Force LED Off)	Inactive	LED off
	Active	N/A
	Blinking	N/A
Enhanced Mode 15 (Force LED On)	Inactive	N/A
	Active	LED on
	Blinking	N/A

5.22 ActiPHY Power Management

The device incorporates a number of power-management modes and features that provide methods to consume less energy. These are discussed in the following sections.

5.22.1 SMART POWER SAVING

For shorter cable lengths (< ~70 meters) the SNR is sufficiently high to allow the reduction of ADC resolution as well as DSP taps. Based on the detected cable length, the device automatically reduces power consumption by approximately 20 mW.

5.22.2 ENERGY-DETECT POWER-DOWN MODE

The device supports an Energy-Detect Power-Down (EDPD) mode to save power when there is no link partner sending signals.

In EDPD mode, the device shuts down all transceiver blocks, except for the transmitter and energy detect circuits. Power can be reduced further by extending the time interval between the transmissions of link pulses to check for the presence of a link partner. The periodic transmission of link pulses is needed to ensure the device and its link partner, when operating in the same low-power state and with Auto-MDI/MDI-X disabled, can wake up when the cable is connected between them.

By default, EDPD mode is disabled after power-up. EDPD is enabled by setting the `p_edpd_en` bit in the EDPD Control register within the MMD address space.

EDPD operation may be adjusted via the `p_edpd_mask_timer[1:0]`, `p_edpd_timer[1:0]`, and `p_EDPD_random_dis` fields in the EDPD Control register within the MMD address space.

The energy detection change status can be read from the Interrupt Status register. The current energy detection status can be read from the EDPD low power bit in the Analog Control Register 8.

While the `p_edpd_en` bit is set, the cable link status will be down, and the energy detection normally monitors pairs A and B for energy. If the link speed is forced to 1000 Mbps (by disabling auto-negotiation and setting the speed manually), the energy detection monitors all four pairs. For cable diagnostic purposes, individual wire pairs may be monitored by forcing the link speed to 1000 Mbps and selecting the wire pair using the EDPD Wire Pair Selection bits in the Analog Control Register 8.

The device's PLL is normally enabled during EDPD. It can be set to be disabled during EDPD by setting the `DGT_edpd_pll_dis` bit in MMD31 Register 19.

Normally, previous register setting are maintained when EDPD mode is cleared. With the PLL disabled, a device reset occurs following the removal of EDPD (or if the `DGT_edpd_pll_dis` bit is cleared during EDPD), in which case register settings will return to their defaults.

5.23 JTAG

An IEEE 1149.1 compliant TAP Controller supports boundary scan and various test modes.

The device includes an integrated JTAG boundary-scan test port for board-level testing. The interface consists of four pins (**TDO**, **TDI**, **TCK** and **TMS**) and includes a state machine, data register array and an instruction register. The JTAG pins are described in [Table 3-6](#). The JTAG interface conforms to the IEEE Standard 1149.1 - 2001 *Standard Test Access Port (TAP) and Boundary-Scan Architecture*.

All input and output data is synchronous to the **TCK** test clock input. TAP input signals **TMS** and **TDI** are clocked into the test logic on the rising edge of **TCK**, while the output signal **TDO** is clocked on the falling edge.

JTAG pins are multiplexed with the GPIO pins. The JTAG functionality is selected when the **TESTMODE** pin is asserted.

The implemented JTAG instructions and their op codes are shown in [Table 5-12](#). JTAG timing information is provided in [Section 6.6.6, "JTAG Timing"](#).

TABLE 5-12: JTAG OP CODES

INSTRUCTION	OP CODE
CLAMP	4'b0000
EXTEST	4'b0001
(RESERVED)	4'b0010
(RESERVED)	4'b0011
INTTEST	4'b0100
SAMPLE_PRELOAD	4'b0101
HIGHZ	4'b0110
HOST-IJTAG ACCESS	4'b0111
ID CODE	4'b1000
BYPASS	4'b1001 to 4'b1111

Note: The JTAG device ID is 004C1445h.

Note: All digital I/O pins support IEEE 1149.1 operation. Analog pins do not support IEEE 1149.1 operation.

5.24 Coma Mode

Coma mode is designed to hold the PHY in a suspended state until system initialization is complete. When enabled by driving the **COMA_MODE** pin high, all the errors, alarms, link up/down notifications, etc. are suppressed until **COMA_MODE** is driven low. This is useful in designs with multiple PHYs, as it allows all errors to be suppressed until the entire board is configured. Coma mode operates as per [Table 5-13](#).

TABLE 5-13: COMA MODE OPERATION

Chip Function	Coma Mode Active
Gigabit PHY Hard Macro	Gigabit PHY held in disabled state (except configuration registers). No data is sent to the line or MAC, no recovered clock, no interrupt/error/etc. indications given to the system.
LEDs	LEDs inactive
Interrupt	Interrupts inactive
1588 Timestamp Engines	No affect
1588 Common Functions	No affect
SGMII PCS1G Block	No affect
SerDes	No affect
System PLL	No affect
1588 PLL	No affect
SyncE Clock Mux	No affect (internal recovered clocks will be disabled, but daisy-chain recovered clock inputs may still be available)
MDIO Functions	No affect

5.24.1 SOFTWARE POWER-DOWN MODE

The device supports a Software Power-Down (SPD) mode. This mode is used to power down the device when it is not in use after power-up. SPD mode is enabled by writing a one to the Power Down bit in the Basic Control register. The device may also be placed into software power-down by default by setting the **MODE_SEL[4:0]** configuration straps to '0100x'. The device exits the SPD state after a zero is written to the Power Down bit.

In the SPD state, the device disables most internal functions. During SPD, the crystal oscillator and PLL are enabled and the internal (125 MHz and 250 MHz) clocks are gated. The standard registers (0 through 31) and the MII Management Interface operate using the crystal clock.

Previous register settings are maintained during and following the removal of SPD.

APPLICATION NOTE: The internal (125 MHz and 250 MHz) clock gating maybe overridden by setting the **spd_clock_gate_override** bit in the Digital Debug Control 2 register at the cost of increased power.

The following remain operational during SPD:

- MII Management Interface
 - Only access to the standard registers (0 through 31) is supported.
 - Access to MMD address spaces other than MMD Address Space 1 is possible if the **spd_clock_gate_override** bit is set.
 - Access to MMD Address Space 1 is not possible.

- Voltage Regulator Controller (LDO)
 - The LDO controller can be disabled by setting the active low LDO enable bit in the Analog Control Register 11. An external source of 1.2V is necessary for operation in this case.
- PLL
 - Normally the PLL is enabled during SPD. It may be disabled by setting the `spd_pll_disable` bit described below.
- Crystal Oscillator
 - Normally the Crystal Oscillator is enabled during SPD. It may be disabled by setting the `enXTALb` bit described below.
- Bandgap
 - This is always enabled.
- Internal Slow Oscillator
 - This is always enabled.

The following are normally disabled during SPD:

- ADC/PGA/TX/common bias circuits
- DLL
- TX and RX clocks
 - If the above mentioned `spd_clock_gate_override` bit is set, TX and RX clocks would be enabled. They may alternately be stopped by setting the Isolate (`PHY_ISO`) bit in the Basic Control register.

5.24.1.1 SPD Extra Power Savings

To achieve a lower power usage, the PLL may be disabled during SPD mode by setting the `spd_pll_disable` bit in the Digital Debug Control 2 register prior to entering SPD. The device may also be placed into software power-down with the PLL disabled by default by setting the **MODE_SEL[4:0]** configuration straps to '01001'.

With the PLL disabled, a device reset occurs following the removal of SPD (or if the `spd_pll_disable` bit is cleared during SPD). Register settings will return to their defaults, determined by the Operation Mode Strap Override Low register and the Operation Mode Strap Override High register.

APPLICATION NOTE: If either the `spd_pll_dis_mode` or `spd_pll_en_mode` bits in the Operation Mode Strap Override Low register are set, the device will return to SPD mode, potentially with the PLL disabled. In order to avoid this logical loop, software must clear the `spd_pll_dis_mode` and `spd_pll_en_mode` bits before exiting SPD.

To further reduce power usage, the crystal oscillator maybe disabled by setting the `enXTALb` bit in the Analog Control Register 1 after setting the `spd_pll_disable` bit and entering SPD.

Since the MII Management Interface operates using the crystal clock, once this bit is set, the device will become inaccessible. A pin reset or power cycle is required to resume operation.

6.0 OPERATIONAL CHARACTERISTICS

6.1 Absolute Maximum Ratings*

Supply Voltage (VDDAL_x, VDDTXL_SERDES, VDDCORE) (Note 6-1)	-0.5V to +1.27V
Supply Voltage (VDDAH, VDDAH_x, VDDIO) (Note 6-1)	-0.5V to +3.63V
Input Voltage (all inputs)	-0.5V to +3.63V
Output Voltage (all outputs)	-0.5V to +3.63V
Storage Temperature (T _S)	-55°C to +150°C
Lead Temperature (soldering, 10s)	+260°C
Maximum Junction Temperature (T _J)	+125°C
HBM ESD Performance	+/-5 kV

Note 6-1 When powering this device from laboratory or system power supplies, it is important that the absolute maximum ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

*Stresses exceeding those listed in this section could cause permanent damage to the device. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at any condition exceeding those indicated in [Section 6.2, "Operating Conditions**"](#), [Section 6.5, "DC Specifications"](#), or any other applicable section of this specification is not implied.

6.2 Operating Conditions**

Supply Voltage (VDDAL_x, VDDTXL_SERDES, VDDCORE @ 1.1V)	(-5%/+5%) +1.045V to +1.155V
Supply Voltage (VDDAH, VDDAH_x @ 3.3V)	(-5%/+5%) +3.135V to +3.465V
Supply Voltage (VDDAH, VDDAH_x @ 2.5V)	(-5%/+5%) +2.375V to +2.625V
Supply Voltage (VDDIO @ 3.3V)	(-5%/+5%) +3.135V to +3.465V
Supply Voltage (VDDIO @ 2.5V)	(-5%/+5%) +2.375V to +2.625V
Supply Voltage (VDDIO @ 1.8V)	(-5%/+5%) +1.71V to +1.89V
Input Voltage (all inputs)	-0.3V to +3.63V
Output Voltage (all outputs)	-0.3V to +3.63V
Ambient Operating Temperature in Still Air (T _A)	Note 6-2

Note 6-2 0°C to +70°C for commercial version, -40°C to +105°C for extended industrial version.

**Proper operation of the device is guaranteed only within the ranges specified in this section.

6.3 Power Consumption

This section details the power consumption of the device as measured during various modes of operation at various operating voltages. Power dissipation is impacted by temperature, supply voltage and external source/sink requirements. All typical measurements were taken at +25°C unless otherwise noted. All worst-case measurements were taken at +5% power supply and +125°C junction temperature.

TABLE 6-1: POWER CONSUMPTION

Interface	Condition	Combined Power Supplies	Typical	Worst Case	Units
SGMI 1000M Speed	without PTP	VDDCORE @ 1.1V, VDDIO/VDDAH/VDDAH_x @ 3.3V	594	700	mW
		VDDCORE @ 1.1V, VDDIO/VDDAH/VDDAH_x @ 2.5V	470	560	
		VDDCORE @ 1.1V, VDDIO @ 1.8V, VDDAH/VDDAH_x @ 2.5V	470	555	
	with PTP	VDDCORE @ 1.1V, VDDIO/VDDAH/VDDAH_x @ 3.3V	670	811	
		VDDCORE @ 1.1V, VDDIO/VDDAH/VDDAH_x @ 2.5V	520	635	
		VDDCORE @ 1.1V, VDDIO @1.8V, VDDAH/VDDAH_x @ 2.5V	500	600	
SGMII	100M Speed	VDDCORE @ 1.1V, VDDIO/VDDAH/VDDAH_x @ 3.3V	480	565	
	10M Speed	VDDCORE @ 1.1V, VDDIO/VDDAH/VDDAH_x @ 3.3V	365	440	
Supply Currents					
VDDCORE (1.1V Operating Current)			200	225	mA
VDDAH, VDDAH_x (2.5V Operating Current)			120	130	
VDDIO (3.3V Operating Current)			25	30	

6.4 Package Thermal Specifications

TABLE 6-2: PACKAGE THERMAL PARAMETERS

Parameter	Symbol	Value	Units	Description
Thermal Resistance Junction to Ambient	Θ_{JA}	30	°C/W	Measured in still air
		26	°C/W	Airflow 1 m/s
		23	°C/W	Airflow 2.5 m/s
Thermal Resistance Junction to Bottom of Case	Ψ_{JT}	0.3	°C/W	Measured in still air
Thermal Resistance Junction to Top of Case	Θ_{JC}	4.8	°C/W	—
Thermal Resistance Junction to Board	Θ_{JB}	17	°C/W	
Thermal Parameter Junction to Board	Ψ_{JB}	17	°C/W	Measured in still air

Note: Thermal parameters are measured or estimated for devices in a multi-layer 2S2P PCB per JESD51.

6.5 DC Specifications

TABLE 6-3: NON-VARIABLE I/O DC ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Units	Notes
ICLK Type Input Buffer						Note 6-3
Low Input Level	V_{IL}	—	—	0.5	V	
High Input Level	V_{IH}	2.0	—	—	V	
Input Leakage	I_{IH}	-10	—	10	μA	

Note 6-3 XI can optionally be driven from a 25 MHz single-ended clock oscillator to which these specifications apply.

TABLE 6-4: VARIABLE I/O DC ELECTRICAL CHARACTERISTICS VDDIO = 3.3V/2.5V/1.8V

Parameter	Symbol	Min	Typ 1.8	Typ 2.5	Typ 3.3	Max	Units	Notes
VIS Type Input Buffer								
Low Input Level	V_{IL}	—	—	—	—	$0.39 \times V_{DDIO}$	V	
High Input Level	V_{IH}	$0.63 \times V_{DDIO}$	—	—	—	—	V	
Schmitt Falling Trip Point	V_{T-}	0.67	0.8	1.1	1.46	1.68	V	
Schmitt Rising Trip Point	V_{T+}	0.8	0.94	1.25	1.62	1.85	V	
Schmitt Trigger Hysteresis ($V_{IHT} - V_{ILT}$)	V_{HYS}	109.9	149	148	164	219.4	mV	
Input Leakage ($V_{IN} = P_VSS$ or V_{DDIO})	I_{IH}	-10	—	—	—	10	μA	Note 6-4
Input Capacitance (generic guess)	C_{IN}	—	—	—	—	3	pF	
Effective Pull-Up Resistance ($V_{IN} = P_VSS$)	R_{PU}	58.9	70	—	—	83.7	k Ω	
Effective Pull-Down Resistance ($V_{IN} = V_{DDIO}$)	R_{PD}	58.7	70	—	—	84.5	k Ω	
VO12 Type Buffer								
Low Output Level	V_{OL}	—	—	—	—	0.4	V	$I_{OL} = -12$ mA
High Output Level	V_{OH}	$V_{DDIO} - 0.4$	—	—	—	—	V	$I_{OH} = 12$ mA
Output Tri-State Leakage	I_{OZ}	-10	—	—	—	10	μA	Note 6-4

TABLE 6-4: VARIABLE I/O DC ELECTRICAL CHARACTERISTICS VDDIO = 3.3V/2.5V/1.8V

Parameter	Symbol	Min	Typ 1.8	Typ 2.5	Typ 3.3	Max	Units	Notes
VOD12 Type Buffer								
Low Output Level	V_{OL}	—	—	—	—	0.4	V	$I_{OL} = -12\text{ mA}$
Output Tri-State Leakage	I_{OZ}	-10	—	—	—	10	μA	Note 6-4
VO4 Type Buffer								
Low Output Level	V_{OL}	—	—	—	—	0.4	V	$I_{OL} = -4\text{ mA}$
High Output Level	V_{OH}	VDDIO-0.4	—	—	—	—	V	$I_{OH} = 4\text{ mA}$
Output Tri-State Leakage	I_{OZ}	-10	—	—	—	10	μA	Note 6-4
VOD4 Type Buffer								
Low Output Level	V_{OL}	—	—	—	—	0.4	V	$I_{OL} = -4\text{ mA}$
Output Tri-State Leakage	I_{OZ}	-10	—	—	—	10	μA	Note 6-4
VOS4 Type Buffer								
High Output Level	V_{OH}	VDDIO-0.4	—	—	—	—	V	$I_{OH} = 4\text{ mA}$
Output Tri-State Leakage	I_{OZ}	-10	—	—	—	10	μA	Note 6-4
SRL Type Input Buffer								
Low Input Level	V_{IL}	—	—	—	—	0.4xVDDIO	V	—
High Input Level	V_{IH}	0.6xVDDIO	—	—	—	—	V	—
Schmitt Falling Trip Point	V_{T-}	0.76	0.90	1.11	1.42	1.64	V	—
Schmitt Rising Trip Point	V_{T+}	0.85	0.99	1.23	1.55	1.76	V	—
Schmitt Trigger Hysteresis ($V_{IHT} - V_{ILT}$)	V_{HYS}	60	90	121	127	150	mV	—
Input Leakage ($V_{IN} = P_VSS$ or VDDIO)	I_{IH}	-15	—	—	—	15	μA	—
Input Capacitance	C_{IN}	—	—	—	—	3	pF	—
SRL Type Output Buffer								
Low Output Level	V_{OL}	—	—	—	—	0.4	V	$I_{OL} = -5\text{ mA}$
High Output Level	V_{OH}	VDDIO-0.4	—	—	—	—	V	$I_{OH} = 5\text{ mA}$
Output Impedance	R_O	—	50	50	50	—	Ω	—

Note 6-4 This specification applies to all inputs without pull-ups or pull-downs and three-stated bi-directional pins.

TABLE 6-5: 1000BASE-T TRANSCEIVER CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Units	Notes
Peak Differential Output Voltage IEEE 802.3 clause 40.6.1.2.1	V_{OP}	670	—	820	mV	Note 6-5
Signal Amplitude Symmetry IEEE 802.3 clause 40.6.1.2.1	V_{SS}	—	—	1	%	Note 6-5
Signal Scaling IEEE 802.3 clause 40.6.1.2.1	V_{SC}	—	—	2	%	Note 6-6
Output Droop IEEE 802.3 clause 40.6.1.2.2	V_{OD}	73.1	—	—	%	Note 6-5
Transmission Distortion IEEE 802.3 clause 40.6.1.2.4	—	—	—	10	mV	Note 6-7

Note 6-5 IEEE 802.3 clause 40.6.1.1.2 Test Mode 1

Note 6-6 From 1/2 of average V_{OP} , Test Mode 1

Note 6-7 IEEE 802.3 clause 40.6.1.1.2 distortion processing

TABLE 6-6: 100BASE-TX TRANSCEIVER CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Units	Notes
Peak Differential Output Voltage ANSI X3.263 clause 9.1.2.2	V_{OUT}	± 0.95	—	± 1.05	V	Note 6-8
Signal Amplitude Symmetry ANSI X3.263 clause 9.1.4	V_{SS}	—	—	2	%	Note 6-8
Signal Rise and Fall Time ANSI X3.263 clause 9.1.6	T_{RF}	3	—	5	ns	Note 6-8
Rise and Fall Symmetry ANSI X3.263 clause 9.1.6	T_{RFS}	0	—	0.5	ns	Note 6-8
Duty Cycle Distortion ANSI X3.263 clause 9.1.8	D_{CD}	—	—	± 0.25	ns	Note 6-9
Overshoot and Undershoot ANSI X3.263 clause 9.1.3	V_{OS}	—	—	5	%	—
Output Jitter ANSI X3.263 clause 9.1.9	—	—	0.7	1.4	ns	Note 6-10
Reference Voltage of ISET (using 6.04 k Ω - 1% resistor)	V_{SET}	—	1.2	—	V	—

Note 6-8 Measured at line side of transformer, line replaced by 100 Ω ($\pm 1\%$) resistor.

Note 6-9 Offset from 16 ns pulse width at 50% of pulse peak.

Note 6-10 Peak to Peak, measured differentially.

TABLE 6-7: 10BASE-T/10BASE-Te TRANSCEIVER CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Units	Notes
Transmitter Peak Differential Output Voltage IEEE 802.3 clause 14.3.1.2.1	V_{OUT} 10BASE-T	2.2	2.5	2.8	V	Note 6-11
	V_{OUT} 10BASE-Te	1.54	—	1.96	V	Note 6-11
Output Jitter IEEE 802.3 clause 14.3.1.2.3	—	—	1.8	3.5	ns	Note 6-12
Signal Rise and Fall Time	T_{RF}	—	25	—	ns	—
Receiver Differential Squelch Threshold IEEE 802.3 clause 14.3.1.3.2	V_{DS}	300	400	—	mV	Note 6-13

Note 6-11 Measured with 100Ω resistive load.

Note 6-12 Measured differentially following the twisted-pair model with a 100Ω resistive load.

Note 6-13 5 MHz square wave.

TABLE 6-8: LDO CONTROLLER

Parameter	Symbol	Min	Typ	Max	Units	Notes
Output drive range for LDO_O to gate input of P-channel MOSFET	V_{LDO_O}	0.85	—	2.8 (Note 6-14)	V	VDDAH = 3.3V for MOSFET source voltage
		0.85	—	2.0 (Note 6-14)	V	VDDAH = 2.5V for MOSFET source voltage
Output of P-channel MOSFET	—	1.1	1.16	1.21	V	

Note 6-14 Value when LDO is enabled. V_{LDO_O} maximum may be as high as **VDDAH** when LDO is disabled.

Note: A capacitor between 1.1V and ground is required to meet the parameters in this table. See [Section 4.1.1, "MOSFET Selection"](#) for details.

TABLE 6-9: POR THRESHOLDS

POR	Conditions	Rising Threshold (Volts)			Falling Threshold (Volts)			Hysteresis (Millivolts)		
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
1.1V Ethernet PHY Analog (VDDAL)	VDDAH = 2.5V	0.84	0.89	0.92	0.84	0.89	0.92	0	50	80
	VDDAH = 3.3V	0.84	0.86	0.87	0.84	0.85	0.86	0	30	50
2.5V/3.3V Ethernet PHY Analog (VDDAH)	—	2.06	2.09	2.10	1.90	1.90	1.90	10	20	40
1.1V Digital Core (VDDCORE)	VDDIO = 1.8V Rise/Fall = 10 μ s	0.913	0.929	0.948	0.65	0.68	0.706	0.217	0.248	0.295
	VDDIO = 1.8V Rise/Fall = 10 ms	0.86	0.87	0.89	0.85	0.86	0.88	10	20	30
	VDDIO = 2.5V Rise/Fall = 10 μ s	0.916	0.933	0.954	0.644	0.677	0.704	0.221	0.256	0.308
	VDDIO = 2.5V Rise/Fall = 10 ms	0.88	0.89	0.89	0.87	0.88	0.88	0	10	20
	VDDIO = 3.3V Rise/Fall = 10 μ s	0.918	0.937	0.962	0.638	0.672	0.701	0.226	0.265	0.322
	VDDIO = 3.3V Rise/Fall = 10 ms	0.88	0.89	0.89	0.87	0.88	0.88	0	10	20

TABLE 6-9: POR THRESHOLDS (CONTINUED)

POR	Conditions	Rising Threshold (Volts)			Falling Threshold (Volts)			Hysteresis (Millivolts)		
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
3.3V/2.5V/1.8V Variable I/O (VDDIO)	VDDIO = 1.8V Rise/Fall = 10 μ s	1.62	1.8	1.98	0.815	0.997	1.167	0.453	0.802	1.164
	VDDIO = 1.8V Rise/Fall = 10 ms	1.454	1.47	1.491	1.218	1.231	1.32	0.212	0.238	0.243
	VDDIO = 2.5V Rise/Fall = 10 μ s	2.02	2.17	2.67	0.8	0.986	1.159	0.88	1.183	1.81
	VDDIO = 2.5V Rise/Fall = 10 ms	1.454	1.47	1.491	1.216	1.23	1.261	0.213	0.240	0.245
	VDDIO = 3.3V Rise/Fall = 10 μ s	2.15	2.34	3.0	0.645	0.973	1.152	1.0	1.373	2.16
	VDDIO = 3.3V Rise/Fall = 10 ms	1.46	1.49	1.52	1.30	1.31	1.32	10	30	60

6.6 AC Specifications

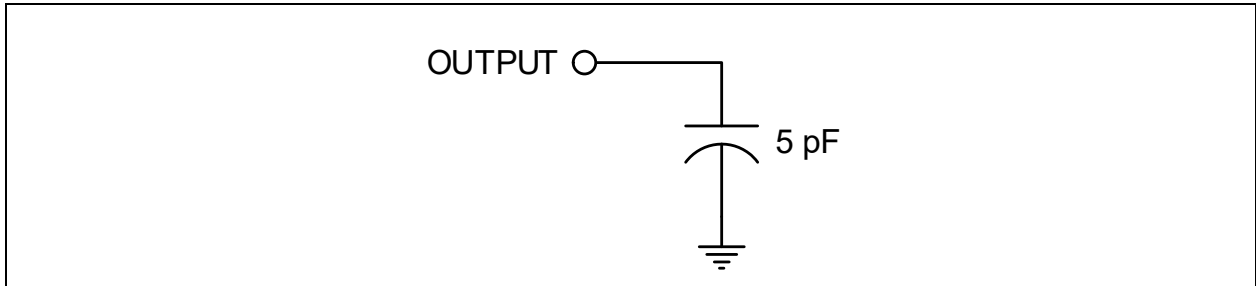
This section details the various AC timing specifications of the device.

Note: The SGMII timing adheres to the SGMII Specification. Refer to the SGMII Specification Rev. 1.8 (ENG-46158) [6] for additional SGMII timing information.

6.6.1 EQUIVALENT TEST LOAD

Output timing specifications assume a 5 pF equivalent test load, unless otherwise noted, as illustrated in Figure 6-1.

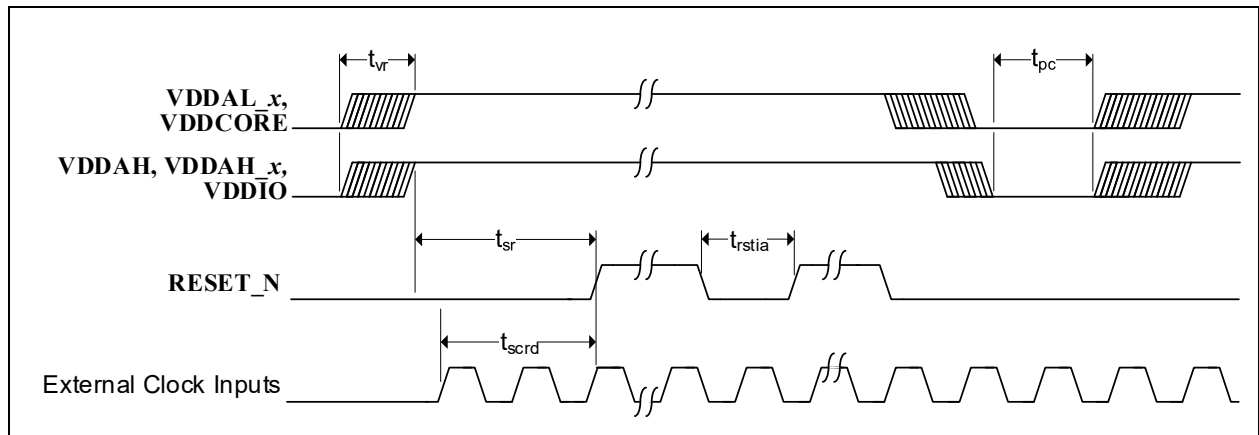
FIGURE 6-1: OUTPUT EQUIVALENT TEST LOAD



6.6.2 POWER SEQUENCE TIMING

This diagram illustrates the device power sequencing requirements.

FIGURE 6-2: POWER SEQUENCE TIMING INTERNAL REGULATORS



There is no power sequence requirement between transceiver (**VDDAH**, **VDDAH_x**), 1.1V core (**VDDCORE**, **VDDAL_x**), and digital I/O (**VDDIO**) power rails.

The power-up waveforms must be monotonic for all supply voltages to the device.

RESET_N must be held asserted following stable voltages for the minimum period specified and if re-asserted, for the minimum period specified.

Before the next power-up cycle, all supply voltages to the device must reach less than 0.4V and there must be a minimum wait time of 150 ms from power-off to power-on.

TABLE 6-10: POWER SEQUENCING TIMING VALUES

Symbol	Description	Min	Typ	Max	Units
t_{vr}	Supply voltages rise time (must be monotonic)	0.1	—	100	ms
t_{sr}	Stable supply voltages to de-assertion of reset	100	—	—	ms
t_{rstia}	RESET_N input assertion time	1	—	—	μ s
t_{scrd}	Stable external clock references to de-assertion of reset	10	—	—	ms
t_{pc}	Supply voltages cycle off-to-on time	150	—	—	ms

6.6.3 RESET PIN CONFIGURATION STRAP TIMING

Figure 6-3 illustrates the RESET_N timing requirements and its relation to the configuration straps. RESET_N must be asserted for the minimum period specified.

FIGURE 6-3: RESET_N CONFIGURATION STRAP TIMING

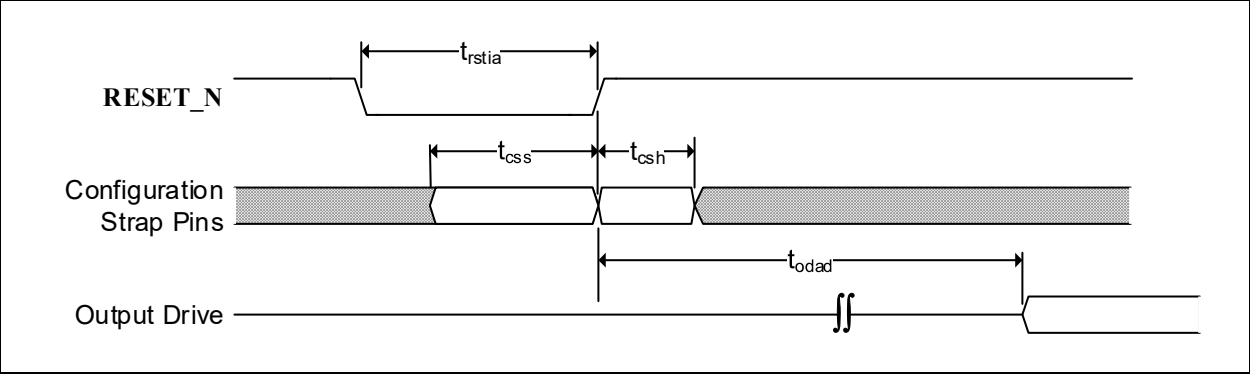


TABLE 6-11: RESET_N CONFIGURATION STRAP TIMING

Symbol	Description	Min	Typ	Max	Units
t_rstia	RESET_N input assertion time	1	—	—	μs
t_css	Configuration strap setup before RESET_N de-assertion	5	—	—	ns
t_csh	Configuration strap hold after RESET_N de-assertion	5	—	—	ns
t_odad	Output drive after RESET_N de-assertion	3.5	—	—	μs

6.6.4 AUTO-NEGOTIATION FAST LINK PULSE (FLP) TIMING

FIGURE 6-4: AUTO-NEGOTIATION FLP TIMING

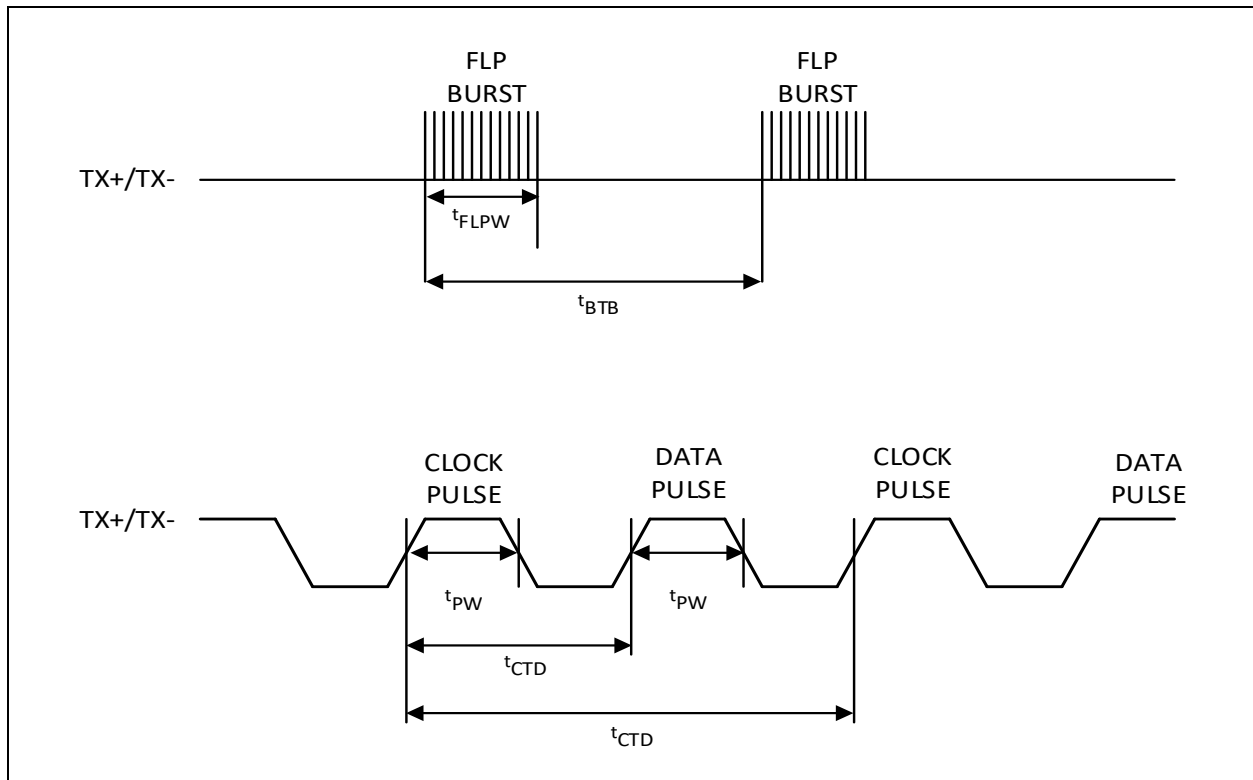


TABLE 6-12: AUTO-NEGOTIATION FLP TIMING PARAMETERS

Symbol	Description	Min	Typ	Max	Units
t_{BTB}	FLP burst to FLP burst	8	16	24	ms
t_{FLPW}	FLP burst width	–	2	–	ms
t_{PW}	Clock/Data pulse width	–	100	–	ns
t_{CTD}	Clock pulse to data pulse	55.5	64	69.5	μ s
t_{CTC}	Clock pulse to clock pulse	111	128	139	μ s
	Number of clock/data pulses per FLP burst	17	–	33	–

6.6.5 MDC/MDIO TIMING

This section specifies the MDC/MDIO timing of the device. These timing numbers are valid for high-speed MDIO operation using push-pull MDIO buffers.

FIGURE 6-5: MDC/MDIO TIMING

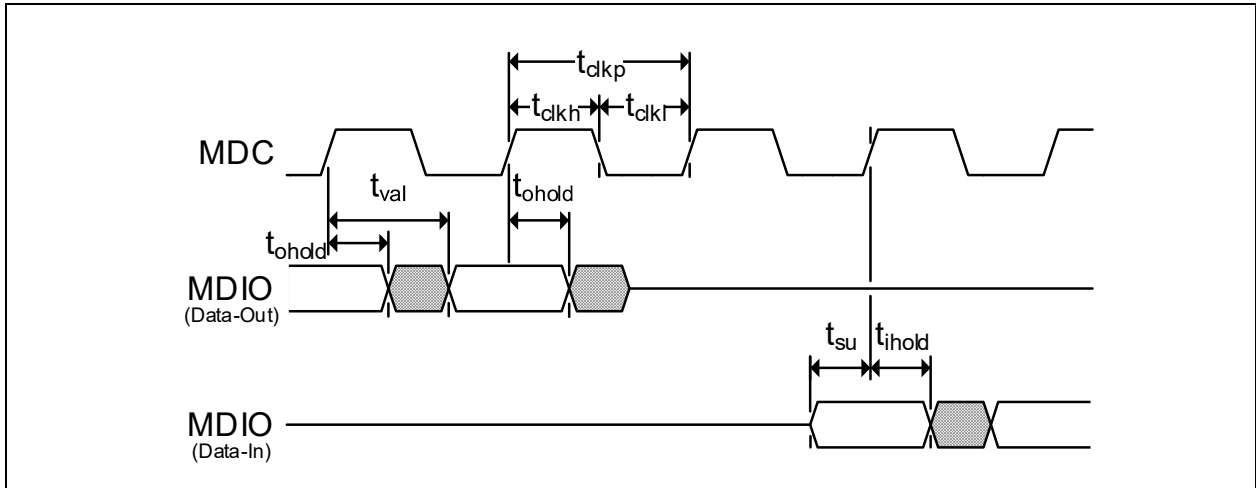


TABLE 6-13: MDC/MDIO TIMING VALUES

Symbol	Description	Min	Typ	Max	Units
t_{clkp}	MDC period	40	—	Note 6-15	ns
t_{clkh}	MDC high time	10	—	—	ns
t_{clkl}	MDC low time	10	—	—	ns
t_{val}	MDIO (read from PHY) output valid from rising MDIO of MDC	—	—	20	ns
t_{ohold}	MDIO (read from PHY) output hold from rising edge of MDC	4	—	—	ns
t_{su}	MDIO (write to PHY) input setup time to rising edge of MDC	8 Note 6-16	—	—	ns
t_{ihold}	MDIO (write to PHY) input hold time after rising edge of MDC	8 Note 6-16	—	—	ns

Note 6-15 The device can operate with MDC clock frequencies generated from bit banging in the 10s/100s of Hertz.

Note 6-16 These values provide 2 ns margin beyond the IEEE specification.

6.6.6 JTAG TIMING

This section specifies the JTAG timing of the device.

FIGURE 6-6: JTAG TIMING

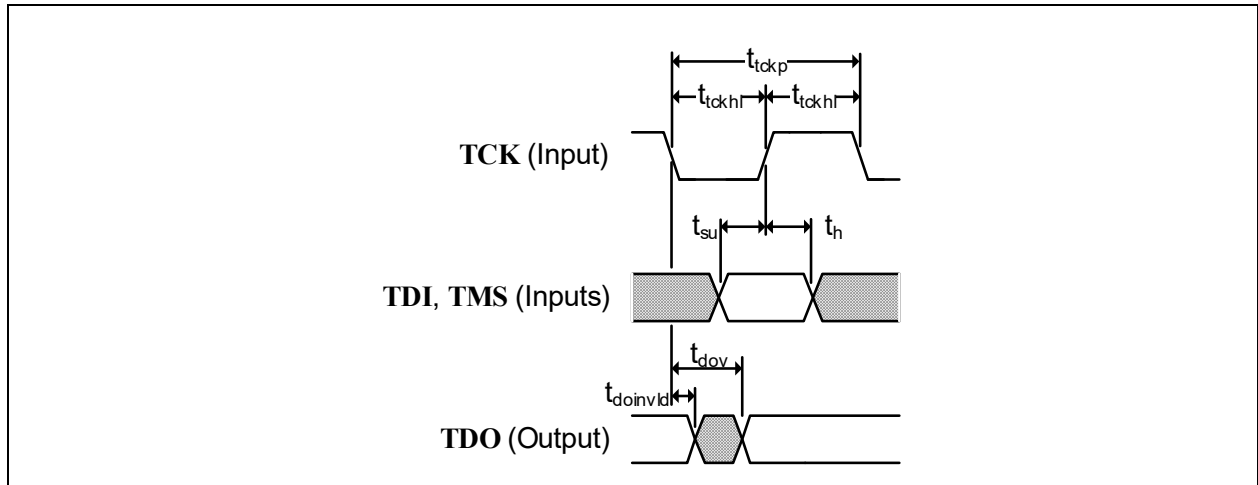


TABLE 6-14: JTAG TIMING VALUES

Symbol	Description	Min	Max	Units	Notes
t_{tckp}	TCK clock period	40	—	ns	—
t_{tckhl}	TCK clock high/low time	$t_{tckp} * 0.4$	$t_{tckp} * 0.6$	ns	
t_{su}	TDI, TMS setup to TCK rising edge	15	—	ns	
t_h	TDI, TMS hold from TCK rising edge	4	—	ns	
t_{dov}	TDO output valid from TCK falling edge	—	16	ns	
$t_{doinvld}$	TDO output invalid from TCK falling edge	0	—	ns	

Note: Timing values are with respect to an equivalent test load of 25 pF.

6.6.7 GPIO TIMING

This section specifies the general GPIO timing of the device.

TABLE 6-15: GPIO TIMING VALUES

Symbol	Description	Min	Typ	Max	Units
$t_{\text{input_pulse}}$	GPIO input pulse width	18	—	—	ns
$t_{\text{output_pulse}}$	GPIO output pulse width	14	—	—	ns
$t_{\text{input_su}}$	GPIO input setup/hold timing	N/A, treat as asynchronous (Note 6-17)			
$t_{\text{output_hold}}$	GPIO output valid/hold timing	N/A, treat as asynchronous (Note 6-17)			

Note 6-17 GPIOs must have pulse widths with a minimum of two 125 MHz clocks, but no synchronous timing relationship is specified. GPIOs configured as alternate functions may have synchronous timing relationships.

6.6.8 GPIO SOF DETECTION TIMING

This section specifies the GPIO SOF timing of the device.

FIGURE 6-7: GPIO SOF TIMING

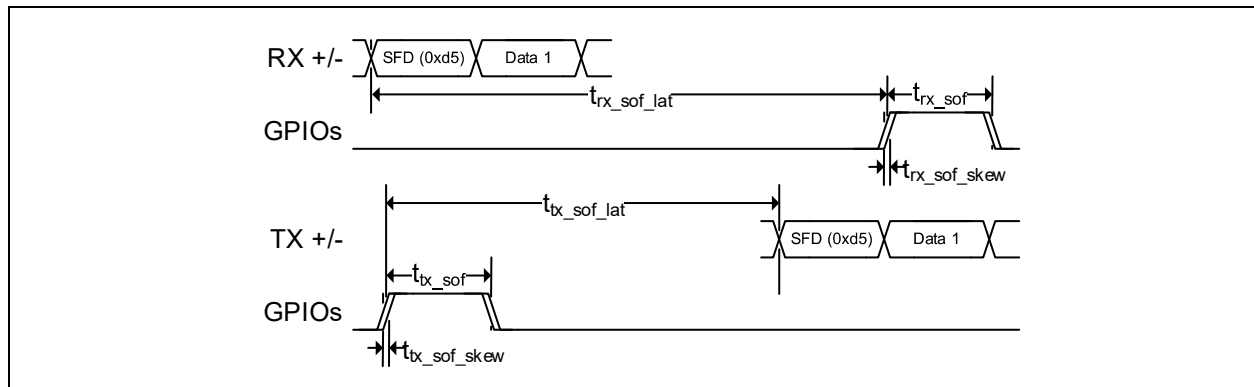


TABLE 6-16: GPIO SOF TIMING VALUES

Symbol	Description	Min	Typ	Max	Units
$t_{\text{rx_sof_lat}}$	RX SOF latency	1000M 100M 10M	—	472 2000 20000	ns
$t_{\text{rx_sof}}$	RX SOF pulse width	—	Note 6-18	—	ns
$t_{\text{rx_sof_skew}}$	RX SOF skew between GPIOs	—	0.5	1	ns
$t_{\text{tx_sof_lat}}$	TX SOF latency	1000M 100M 10M	—	59 1500 12000	ns
$t_{\text{tx_sof}}$	TX SOF pulse width	—	Note 6-18	—	ns
$t_{\text{tx_sof_skew}}$	TX SOF skew between GPIOs	—	0.5	1	ns

Note 6-18 8.8 ns for 1000BASE-T operation, 40.5 ns for 100BASE-TX operation, 400 ns for 10BASE-T operation.

6.6.9 1588 GPIO TIMING

This section specifies the 1588 GPIO timing of the device.

FIGURE 6-8: 1588 GPIO ASYNCHRONOUS INPUT AND OUTPUT TIMING

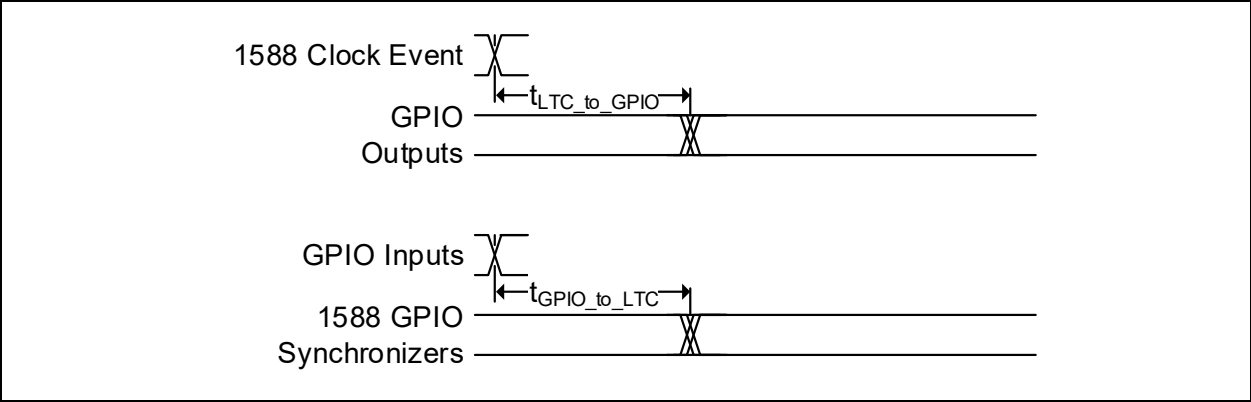


TABLE 6-17: 1588 GPIO ASYNCHRONOUS INPUT AND OUTPUT TIMING VALUES

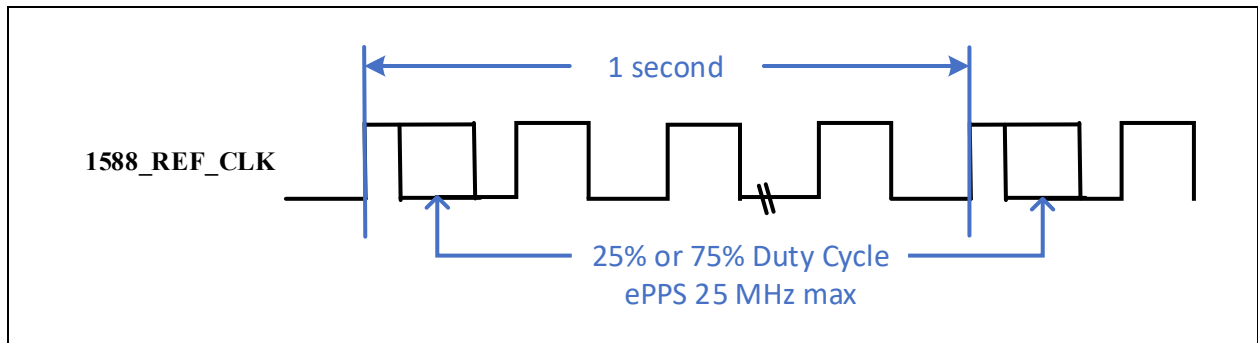
Symbol	Description	Min	Typ	Max	Units
$t_{LTC_to_GPIO}$	LTC to GPIO time	15.0		21.0	ns
$t_{GPIO_to_LTC}$	GPIO to LTC time	12.0		19.0	ns

6.6.10 1588_REF_CLK REFERENCE CLOCK TIMING

This section specifies the **1588_REF_CLK** reference clock timing of the device. In ePPS mode, a single wire carries both a reference clock and 1PPS.

- Non ePPS mode
 - Duty Cycle: (40% minimum, 50% typical, 60% maximum)
 - Jitter: < 100 ps rms
 - Frequency: 10 MHz, 25 MHz, or 125 MHz $\pm$ 50 ppm
- ePPS mode
 - Duty Cycle except for ePPS edge: (40% minimum, 50% typical, 60% maximum)
 - Duty cycle at ePPS edge: (20% minimum, 25% typical, 30% maximum) or (70% minimum, 75% typical, 80% maximum)
 - Jitter: < 100 ps rms
 - Frequency: 25 MHz $\pm$ 50 ppm

FIGURE 6-9: 1588 REFERENCE CLOCK TIMING



6.6.11 1588_LD_ADJ TIMING

This section specifies the 1588_LD_ADJ pin timing of the device.

The 1588_LD_ADJ pin can be used to synchronize one or more LAN8842 1588 LTC with the system 1588 TOD. The 1588_LD_ADJ pin controls initial setting (load) and incremental updates (adjust) of the internal 1588 LTC. It supports the “1PPS” and “1PPS with TOD” mode.

Note: 1588_LD_ADJ is typically a 1PPS, it can also be a non-repeating signal or a signal which repeats at some rate other than 1 Hz.

FIGURE 6-10: 1588_LD_ADJ TIMING

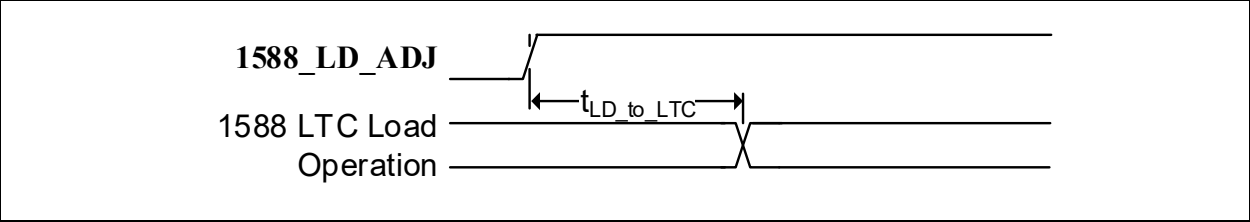


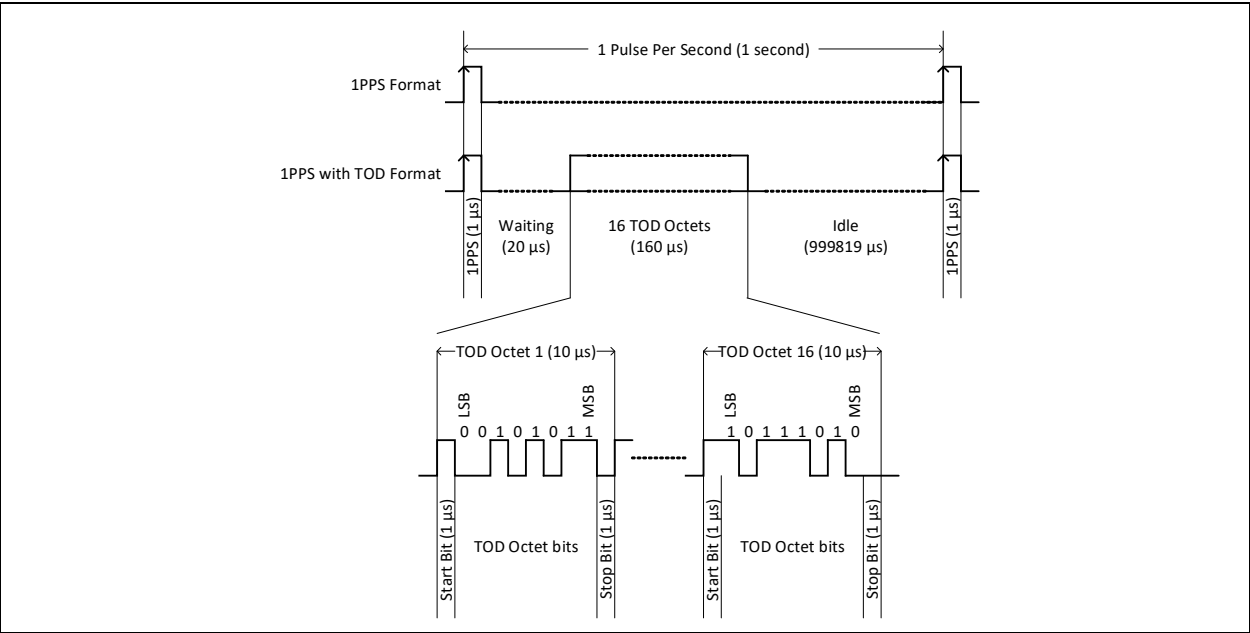
TABLE 6-18: 1588_LD_ADJ TIMING VALUES

Symbol	Description	Min	Typ	Max	Units
$t_{LD_to_LTC}$	1588_LD_ADJ assertion to LTC time	12.0		19.0	ns

6.6.12 1588 1PPS FORMAT AND TIMING

This section specifies the 1588 1PPS (with and without TOD) format and timing of the device.

FIGURE 6-11: 1588 1PPS FORMAT AND TIMING



6.6.13 1588_EVENT_A/B TIMING

This section specifies the **1588_EVENT_A/B** timing of the device.

TABLE 6-19: 1588_EVENT_A/B TIMING VALUES

Symbol	Description	Min	Typ	Max	Units
t_{clkp}	LTC Time of Day to 1588_EVENT_A/B output latency	15.0		21.0	ns

6.6.14 GPIO PTP CAPTURE TIMING

Eight GPIOs can be configured to generate PTP GPIO Capture events. This section specifies the GPIO PTP capture timing of the device.

TABLE 6-20: GPIO PTP CAPTURE TIMING VALUES

Symbol	Description	Min	Typ	Max	Units
$t_{GPIOtoLTC}$	GPIO Rising or falling edge to LTC Time of Day capture latency	12.0		19.0	ns

6.6.15 RCVRD_CLK_OUT1/2 TIMING

This section specifies the **RCVRD_CLK_OUT1/2** recovered clock timing of the device.

- When based on internal recovered clocks:
 - Duty Cycle: (40% minimum, 50% typical, 60% maximum)
 - Jitter: < 100 ps rms
- When based on external recovered clock inputs:
 - Duty Cycle: (40% minimum, 50% typical, 60% maximum)
 - Jitter: < 100 ps rms

6.6.16 CK25OUT TIMING

This section specifies the **CK25OUT** reference clock timing of the device.

- Duty Cycle: (40% minimum, 50% typical, 60% maximum)
- Jitter: < 100 ps rms

6.6.17 CK125_REF_INP/M TIMING

This section specifies the **CK125_REF_INP/M** reference clock timing of the device.

- Duty Cycle: (40% minimum, 50% typical, 60% maximum)
- Jitter: < 100 ps rms
- Frequency: 125 MHz $\pm$ 50 ppm

6.7 Clock Circuit

The device can accept either a 25 MHz crystal (preferred) or a 25 MHz single-ended clock oscillator ($\pm$ 50 ppm, max jitter 100 ps rms) input. If the single-ended clock oscillator method is implemented, **XO** must be left unconnected and **XI** must be driven with a nominal 0-3.3V clock signal. The input clock duty cycle is 40% minimum, 50% typical and 60% maximum.

It is recommended that a crystal utilizing matching parallel load capacitors be used for the crystal input/output signals (XI/XO). See [Table 6-21](#) for the recommended crystal specifications.

TABLE 6-21: CRYSTAL SPECIFICATIONS

Parameter	Symbol	Min	Nom	Max	Units	Notes
Crystal Cut	AT, typ					—
Crystal Oscillation Mode	Fundamental Mode					
Crystal Calibration Mode	Parallel Resonant Mode					
Frequency	F _{fund}	—	25.000	—	MHz	
Frequency Tolerance @ 25°C	F _{tol}	—	—	±50	ppm	Note 6-19
Frequency Stability Over Temp	F _{temp}	—	—	±50	ppm	Note 6-19
Frequency Deviation Over Time	F _{age}	—	±3 to 5	—	ppm	Note 6-20
Total Allowable PPM Budget		—	—	±50	ppm	Note 6-21
Shunt Capacitance	C _O	—	—	6	pF	—
Load Capacitance	C _L	—	—	25	pF	
Motional Inductance	LM	—	—	10	mH	
Drive Level	P _W	—	—	100	μW	
Equivalent Series Resistance	R ₁	—	—	50	Ohm	
Operating Temperature Range	—	Note 6-22	—	Note 6-23	°C	
XI Pin Capacitance	—	—	2 typ	—	pF	Note 6-24
XO Pin Capacitance	—	—	2 typ	—	pF	Note 6-24
Crystal Startup Time	t _{xso}	<2			ms	—

Note 6-19 The maximum allowable values for Frequency Tolerance and Frequency Stability are application dependent. Since any particular application must meet the IEEE ±50 ppm Total PPM Budget, the combination of these two values must be approximately ±45 ppm (allowing for aging).

Note 6-20 Frequency Deviation Over Time is also referred to as Aging.

Note 6-21 The total deviation for the Transmitter Clock Frequency is specified by IEEE 802.3u as ±50 ppm.

Note 6-22 0°C ambient for commercial version, -40°C ambient for industrial version.

Note 6-23 +85°C ambient.

Note 6-24 This number includes the pad, the bond wire and the lead frame. PCB capacitance is not included in this value. The XO/XI pin and PCB capacitance values are required to accurately calculate the value of the two external load capacitors. These two external load capacitors determine the accuracy of the 25.000 MHz frequency.

7.0 PACKAGE OUTLINE

7.1 Package Marking Information

56-VQFN (8x8 mm)

PIN 1 →


LAN8842t
Rnnn (e3)
VCOO
YYWWNNN

Legend:	t Temperature range designator (Blank = commercial, V = extended industrial) R Product revision nnn Internal code e3 Pb-free JEDEC® designator for Matte Tin (Sn) YY Year code (last two digits of calendar year) WW Week code (week of January 1 is week '01') NNN Alphanumeric traceability code V Assembler COO Country of Origin
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

* Standard device marking consists of Microchip part number, year code, week code and traceability code. For device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

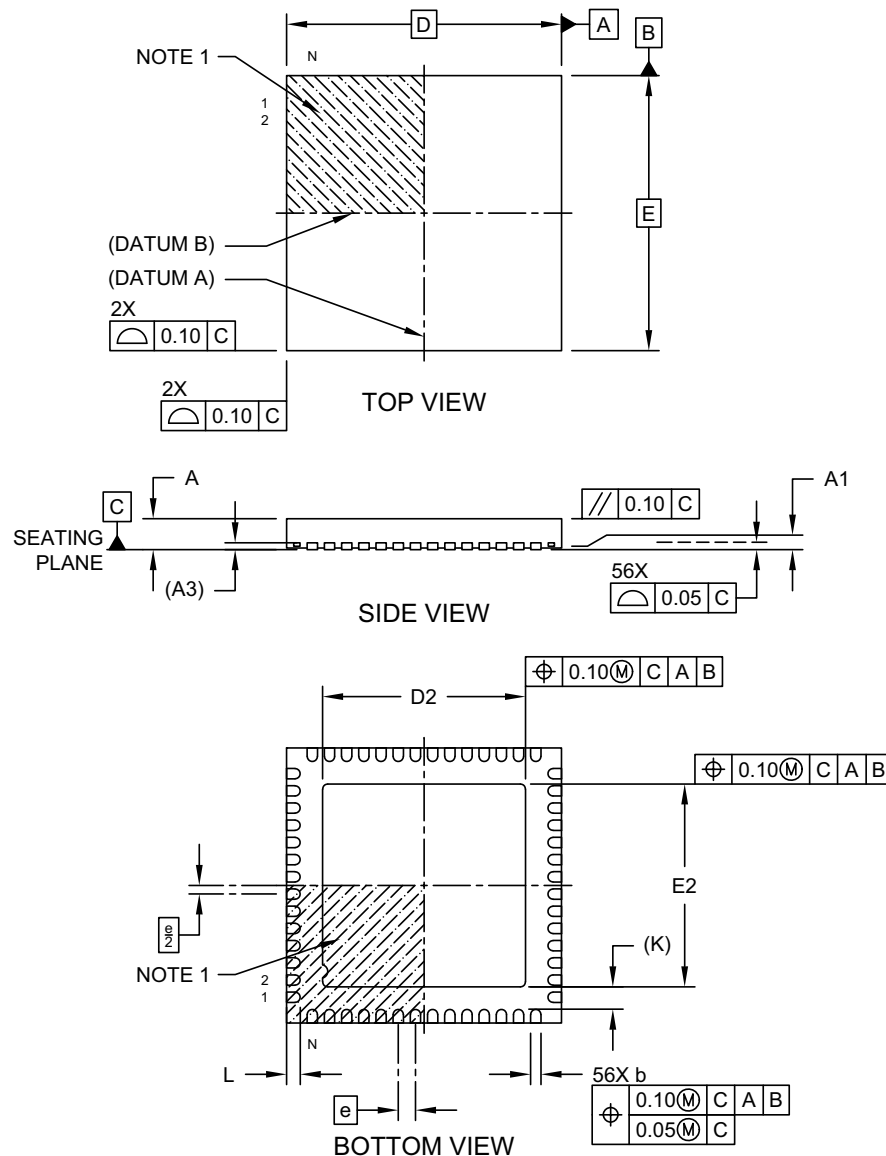
Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

7.2 Package Drawings

FIGURE 7-1: 56-VQFN PACKAGE (DRAWING)

**56-Lead Very Thin Plastic Quad Flat, No Lead Package (8JX) - 8x8 mm Body [VQFN]
With 5.9 mm Exposed Pad**

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

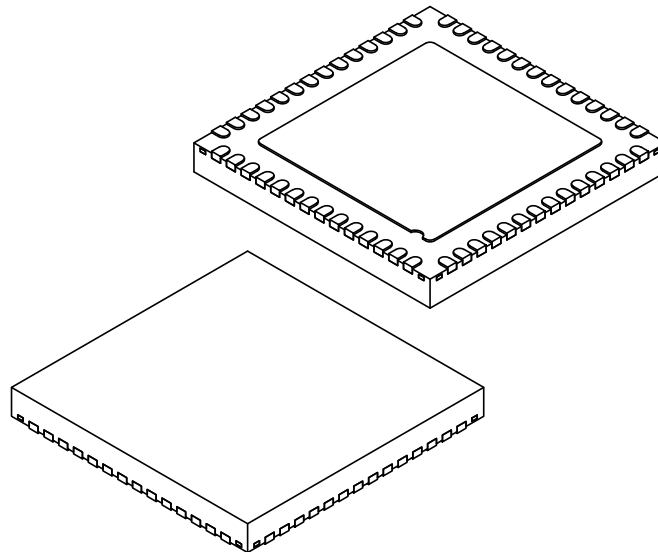


Microchip Technology Drawing C04-433 Rev A Sheet 1 of 2

FIGURE 7-2: 56-VQFN PACKAGE (DIMENSIONS)

**56-Lead Very Thin Plastic Quad Flat, No Lead Package (8JX) - 8x8 mm Body [VQFN]
With 5.9 mm Exposed Pad**

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Terminals	N	56		
Pitch	e	0.50 BSC		
Overall Height	A	—	—	0.90
Standoff	A1	—	—	0.05
Terminal Thickness	A3	0.20 REF		
Overall Length	D	8.00 BSC		
Exposed Pad Length	D2	5.80	5.90	6.00
Overall Width	E	8.00 BSC		
Exposed Pad Width	E2	5.80	5.90	6.00
Terminal Width	b	0.18	0.25	0.30
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K	0.65 REF		

Notes:

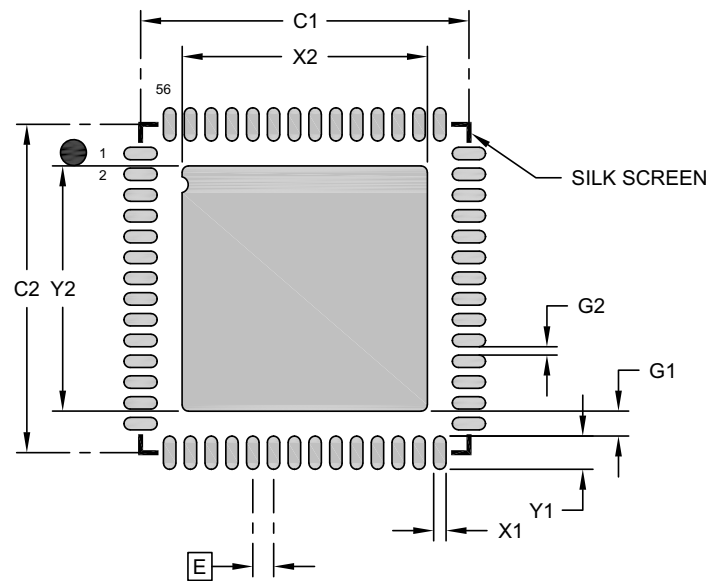
- Pin 1 visual index feature may vary but must be located within the hatched area.
- Package is saw singulated.
- Dimensioning and tolerancing per ASME Y14.5M
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 - REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-433 Rev A Sheet 2 of 2

FIGURE 7-3: 56-VQFN PACKAGE (LAND PATTERN)

**56-Lead Very Thin Plastic Quad Flat, No Lead Package (8JX) - 8x8 mm Body [VQFN]
With 5.9 mm Exposed Pad**

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Center Pad Width	X2			6.00
Center Pad Length	Y2			6.00
Contact Pad Spacing	C1		7.90	
Contact Pad Spacing	C2		7.90	
Contact Pad Width (X56)	X1			0.30
Contact Pad Length (X56)	Y1			0.85
Contact Pad to Center Pad (X56)	G1	0.60		
Contact Pad to Contact Pad (X52)	G2	0.20		

Notes:

- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
- For best soldering results, please refer to current industry standard IPC-7093.

Microchip Technology Drawing C04-2433 Rev A

APPENDIX A: DOCUMENT REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision	Section/Figure/Entry	Correction
DS00005877C (02-03-26)	Features	Cover Bullet "Power-Down and Power-Saving Modes" changed to "ActiPHY® Power Management"
	Section 5.22, ActiPHY Power Management	Functional Description chapter subsection "Power Management" changed to "ActiPHY Power Management"
DS00005877B (08-26-25)	Throughout document.	Grammatical and formatting updates.
	Section 3.3.1, "Device Mode Select (MODE_SEL[4:0])"	Removed note indicating preliminary nature of Device Mode information.
	Figure 5-14, "SGMII Loopback"	SGMII SerDes Loopback example updated.
	Section 6.1, Absolute Maximum Ratings*	HBM ESD Performance updated from "+/-4 kV" to "+/-5 kV".
	Section 6.3, Power Consumption	Power Consumption parameters and values have been updated.
	Table 6-9, "POR Thresholds"	Values updated
	Section 6.6, AC Specifications	SGMII Spec reference updated.
	Table 6-6, "100BASE-TX Transceiver Characteristics"	Typical reference voltage of ISET updated from 0.61V to 1.2V.
	Table 6-16, "GPIO SOF Timing Values"	Values updated.
DS00005877A (03-14-25)	All	Initial release

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PART NO.

Device Tape and Reel Option Temperature Range / Package

Device: LAN8842

Tape and Reel Option: Blank = Standard packaging (tray)
 T = Tape and Reel [\(Note 1\)](#)

Temperature: Blank = 0°C to +70°C (Commercial)
 V = -40°C to +105°C (Extended Industrial)

Package: 8JX = 56-pin VQFN (8 × 8 mm)

Examples:

a) LAN8842/8JX
 Tray, 0°C to +70°C, 56-pin VQFN

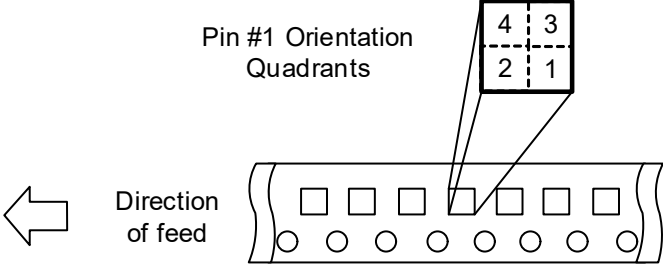
b) LAN8842-V/8JX
 Tray, -40°C to +105°C, 56-pin VQFN

c) LAN8842T/8JX
 Tape & reel, 0°C to +70°C, 56-pin VQFN

d) LAN8842T-V/8JX
 Tape & reel, -40°C to +105°C, 56-pin VQFN

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

Pin #1 Orientation Quadrants



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