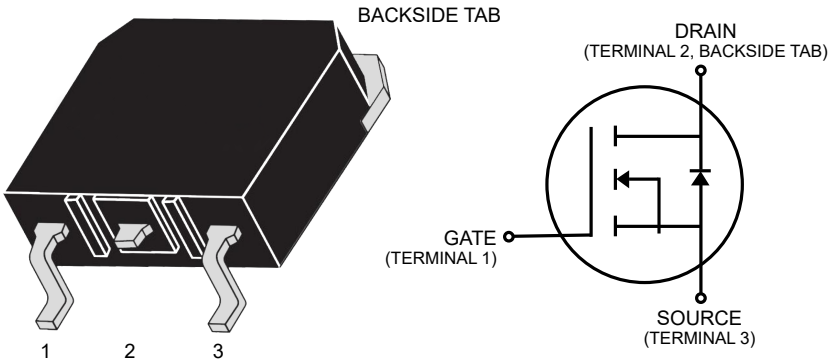
700V, 15 mΩ N-Channel mSiC™ MOSFET

MSC015SMA070S

Product Overview

700V, 15 mΩ typical at V_{GS} = 20V, 17 mΩ typical at V_{GS} = 18V, Silicon Carbide (SiC) N-Channel MOSFET, D3PAK (TO-268).



Features

- Low capacitances and low gate charge
- Fast switching speed due to low internal gate resistance (ESR)
- Stable operation at high junction temperature, $T_{J(max)}$ = 175 °C
- Fast and reliable body diode
- Superior avalanche ruggedness
- RoHS compliant

Benefits

- High efficiency to enable lighter and more compact system
- Simple to drive and easy to parallel
- Improved thermal capabilities and lower switching losses
- Eliminates the need for external freewheeling diode
- Lower system cost of ownership

Applications

- Photovoltaic (PV) inverter, converter, and industrial motor drives
- Smart grid transmission and distribution
- Induction heating and welding
- Hybrid Electric Vehicle (HEV) powertrain and Electric Vehicle (EV) charger
- Power supply and distribution

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1. Device Specifications

This section shows the specifications of this device.

1.1 Absolute Maximum Ratings

The following table shows the absolute maximum ratings of this device.

Table 1-1. Absolute Maximum Ratings

Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain source voltage	700	V
I_D	Continuous drain current at T_C = 25 °C	112	A
	Continuous drain current at T_C = 100 °C	94	
I_{DM}	Pulsed drain current[1]	450	
V_{GS}	Gate-source voltage	23 to –10	V
	Transient gate-source voltage	25 to –12	
P_D	Total power dissipation at T_C = 25 °C	477	W
	Linear derating factor	3.2	W/°C

Note:

1. Repetitive rating: pulse width and case temperature are limited by the maximum junction temperature.

The following table shows the thermal and mechanical characteristics of this device.

Table 1-2. Thermal and Mechanical Characteristics

Symbol	Characteristic/Test Conditions	Min.	Typ.	Max.	Unit
$R_{\theta JC}$	Junction-to-case thermal resistance	—	0.24	0.31	°C/W
T_J	Operating junction temperature	–55	—	175	°C
T_{STG}	Storage temperature	–55	—	150	°C
—	Reflow temperature	—	—	260	°C
Wt	Package weight	—	4.0	—	g

ESD practices should comply with JESD-625.

1.2 Electrical Performance

The following table shows the static characteristics of this device. T_J = 25 °C unless otherwise specified.

Table 1-3. Static Characteristics

Symbol	Characteristic	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0V, I_D = 100 µA	700	—	—	V
$R_{DS(on)}$	Drain-source on resistance[1]	V_{GS} = 20V, I_D = 40A	—	15	19	mΩ
		V_{GS} = 18V, I_D = 40A	—	17	—	
$V_{GS(th)}$	Gate-source threshold voltage	V_{GS} = V_{DS}, I_D = 4 mA	1.9	3.0	5.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 700V, V_{GS} = 0V	—	0.3	35	µA
		V_{DS} = 700V, V_{GS} = 0V, T_J = 175 °C	—	3.5	—	
I_{GSS}	Gate-source leakage current	V_{GS} = 20V/–10V	—	—	±100	nA

Note:

1. Pulse test: pulse width < 380 µs, duty cycle < 2%.

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The following table shows the dynamic characteristics of this device. T_J = 25 °C unless otherwise specified. The dynamic characteristics are characterized, not 100% tested, at the recommended operating V_{GS} = 20V/–5V.

Table 1-4. Dynamic Characteristics

Symbol	Characteristic	Test Conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{GS} = 0V V_{DD} = 700V V_{AC} = 25 mV ƒ = 200 kHz	—	4324	—	pF
C_{rss}	Reverse transfer capacitance		—	44	—	
C_{oss}	Output capacitance		—	506	—	
Q_G	Total gate charge	V_{GS} = –5V/20V V_{DD} = 470V I_D = 40A	—	215	—	nC
Q_{GS}	Gate-source charge		—	58	—	
Q_{GD}	Gate-drain charge		—	35	—	
$t_{d(on)}$	Turn-on delay time	V_{DD} = 470V V_{GS} = –5V/20V I_D = 50A $R_{G(ext)}$ = 4Ω	—	25	—	ns
t_r	Voltage rise time		—	34	—	
$t_{d(off)}$	Turn-off delay time		—	53	—	
t_f	Voltage fall time		—	20	—	
E_{on}	Turn-on switching energy	Freewheeling diode = MSC015SMA070S (V_{GS} = –5V); reference Figure 1-18	—	856	—	µJ
E_{off}	Turn-off switching energy		—	129	—	
ESR	Gate equivalent series resistance	f = 1 MHz, 25 mV, drain short	—	0.69	—	Ω
SCWT	Short circuit withstand time	V_{DS} = 560V, V_{GS} = 20V	—	3.0	—	µs
E_{AS}	Avalanche energy, single pulse	I_D = 40A	—	6400	—	mJ

The following table shows the body diode characteristics of this device. T_J = 25 °C unless otherwise specified. The body diode reverse recovery is characterized, not 100% tested.

Table 1-5. Body Diode Characteristics

Symbol	Characteristic	Test Conditions	Min.	Typ.	Max.	Unit
V_{SD}	Diode forward voltage	I_{SD} = 40A, V_{GS} = 0V	—	3.3	—	V
		I_{SD} = 40A, V_{GS} = –5V	—	3.6	5.0	
t_{rr}	Reverse recovery time	I_{SD} = 50A, V_{GS} = –5V, Drive R_G = 4Ω, V_{DD} = 470V, dI/dt = –6800 A/µs	—	37	—	ns
Q_{rr}	Reverse recovery charge		—	631	—	nC
I_{RRM}	Reverse recovery current		—	68	—	A

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1.3 Typical Performance Curves

Data for performance curves are characterized, not 100% tested.

Figure 1-1. Drain Current vs. V_{DS} at T_J

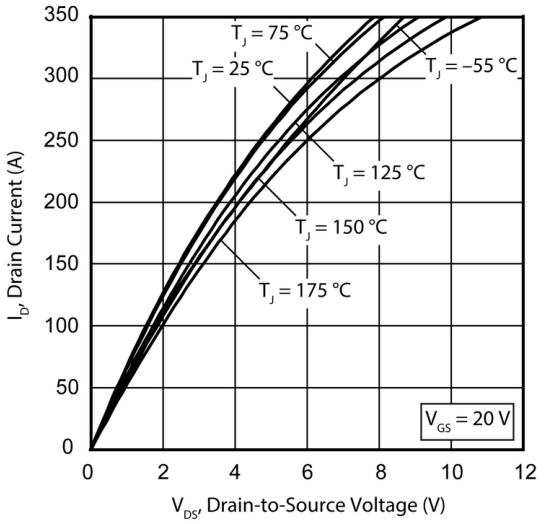

Figure 1-2. Drain Current vs. V_{DS} at V_{GS}

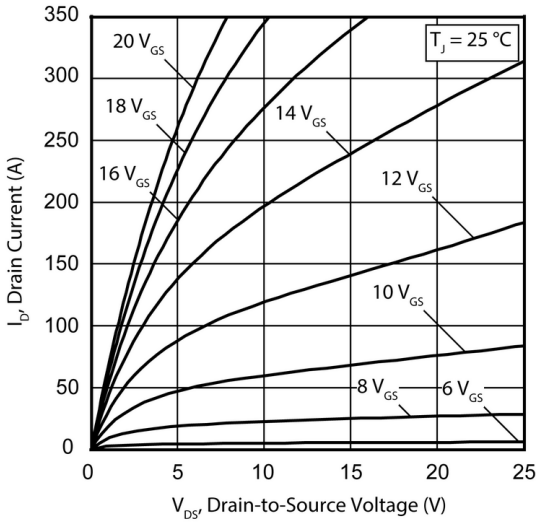

Figure 1-3. Drain Current vs. V_{DS} at V_{GS}

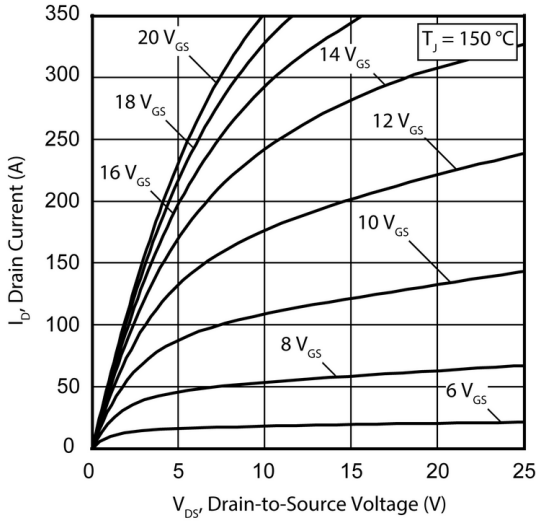

Figure 1-4. Drain Current vs. V_{DS} at V_{GS}

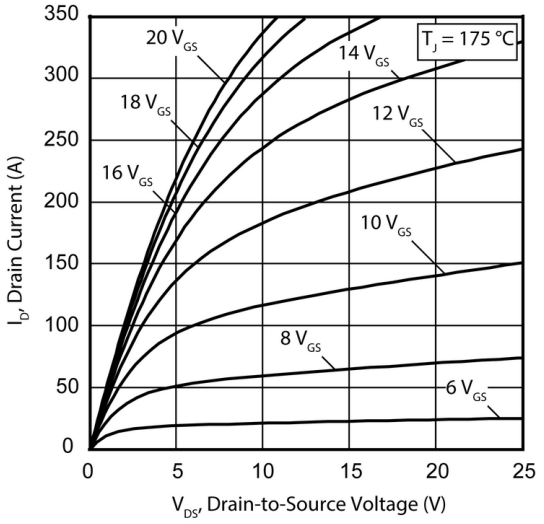

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Figure 1-5. $R_{DS(on)}$ vs. Junction Temperature

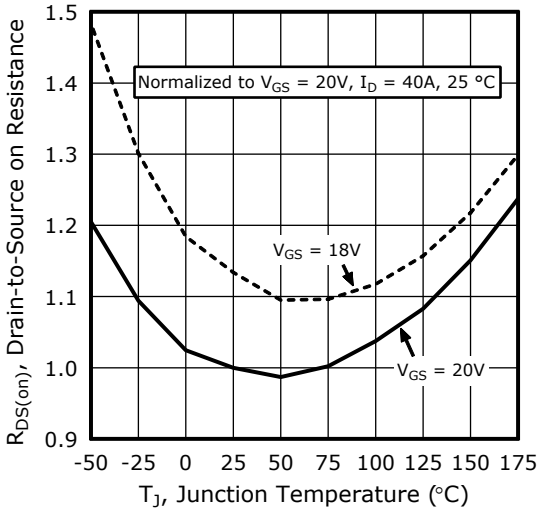

Figure 1-6. Gate Charge Characteristics

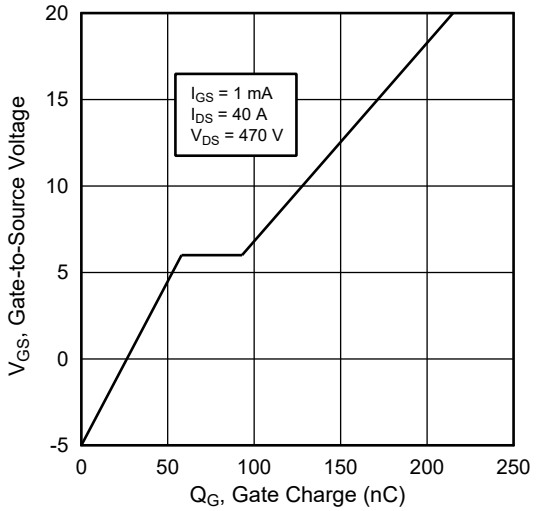

Figure 1-7. Capacitance vs. Drain-to-Source Voltage

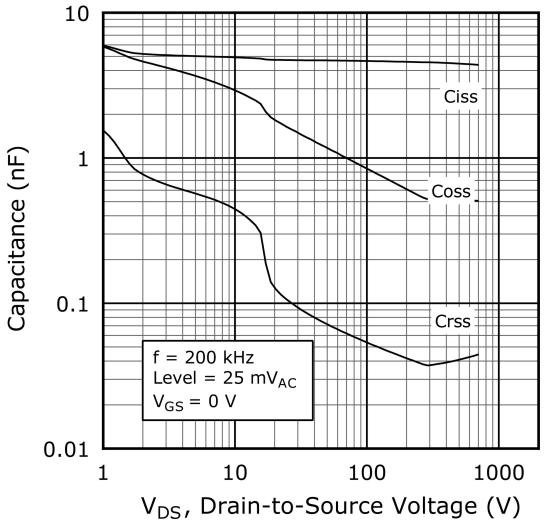

Figure 1-8. Output Charge vs. Drain-to-Source Voltage

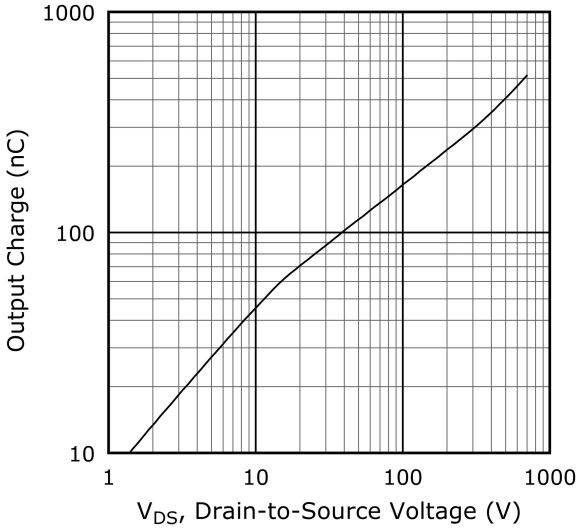

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Figure 1-9. I_D vs. V_{DS} 3rd Quadrant Conduction

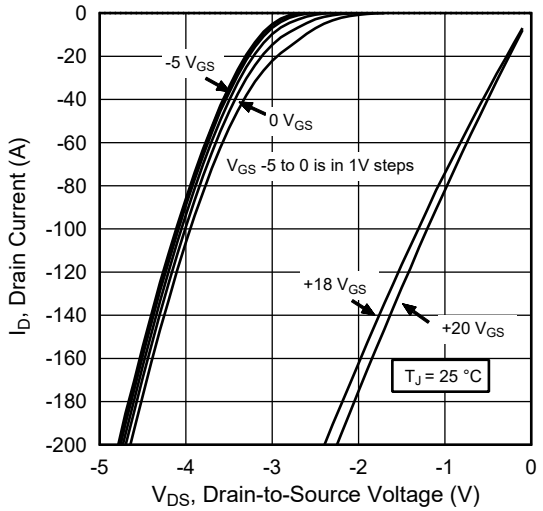

Figure 1-10. I_D vs. V_{DS} 3rd Quadrant Conduction

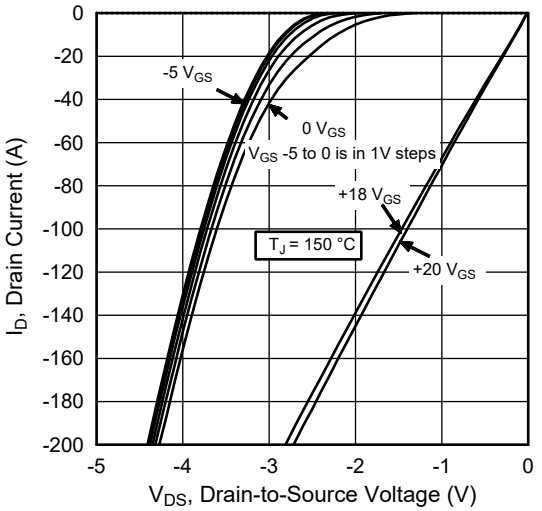

Figure 1-11. Switching Energy E_{on} vs. V_{DS} & I_D

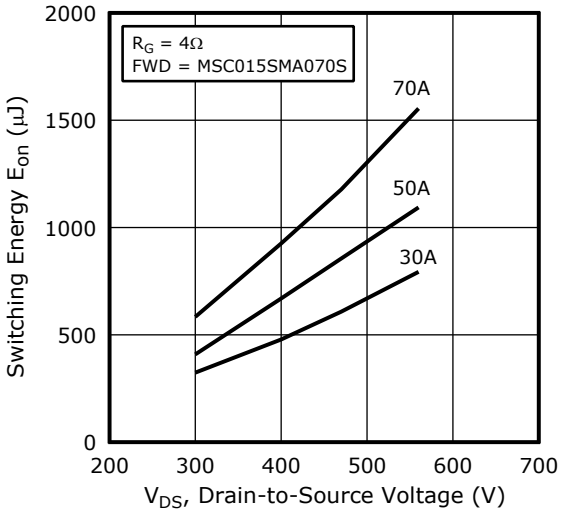

Figure 1-12. Switching Energy E_{off} vs. V_{DS} & I_D

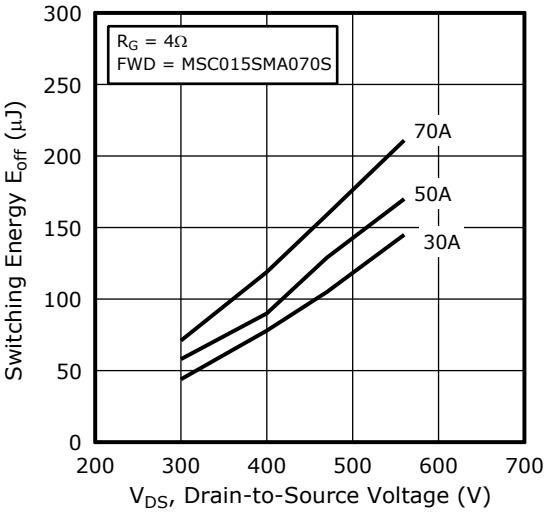

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Figure 1-13. Switching Energy vs. R_G

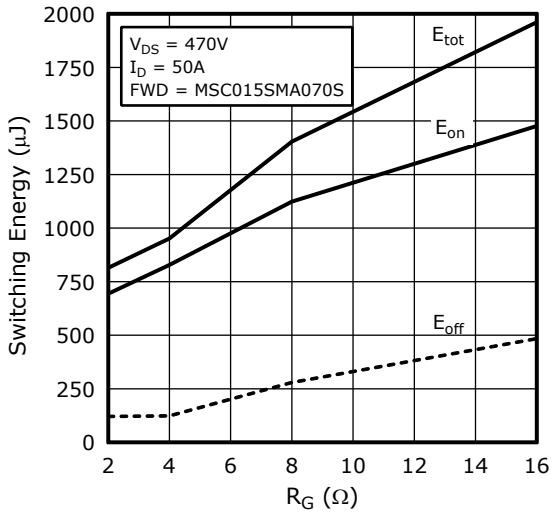

Figure 1-14. Switching Energy vs. Junction Temperature

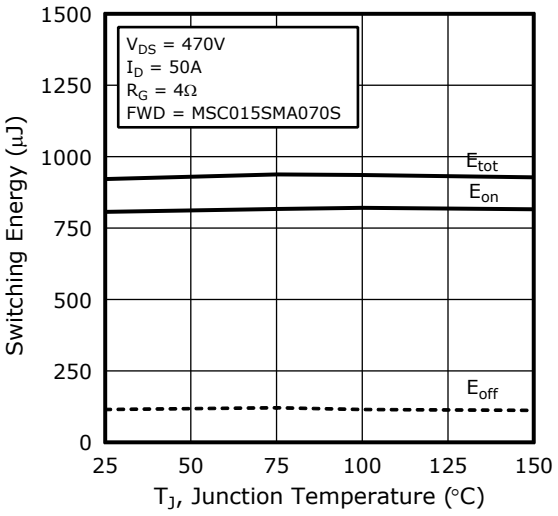

Figure 1-15. Threshold Voltage vs. Junction Temperature

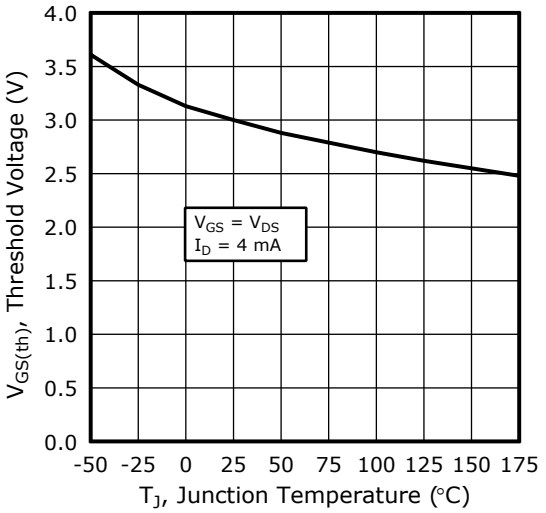

Figure 1-16. Forward Safe Operating Area

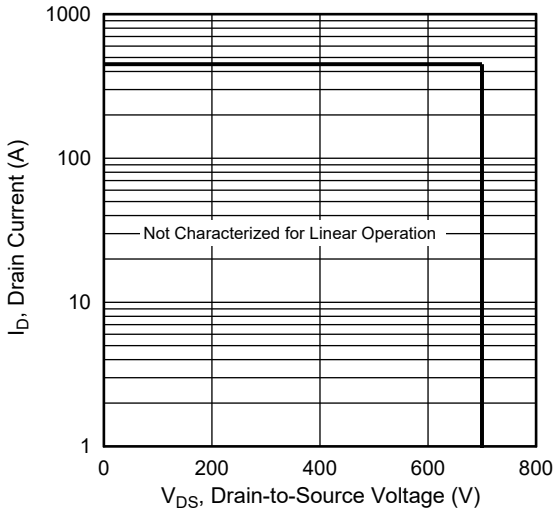

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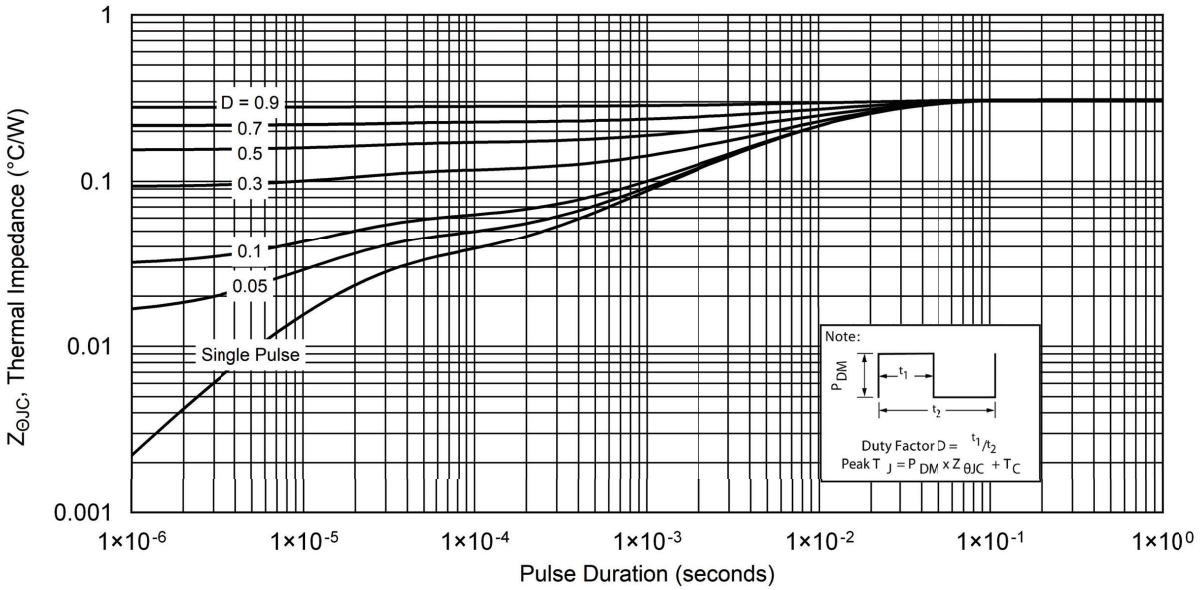
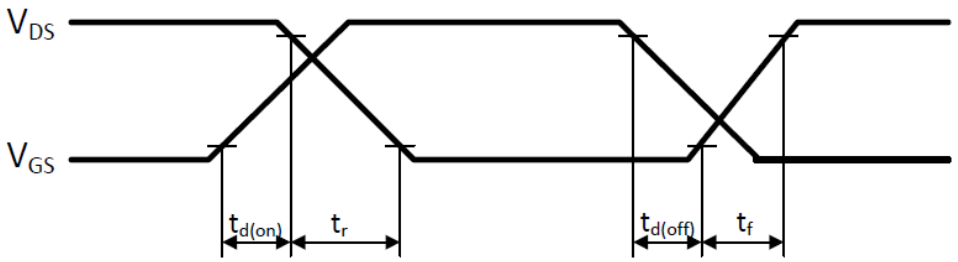
Figure 1-17. Maximum Transient Thermal Impedance



The following figure shows the switching waveform diagram of this device.

Figure 1-18. Switching Waveform



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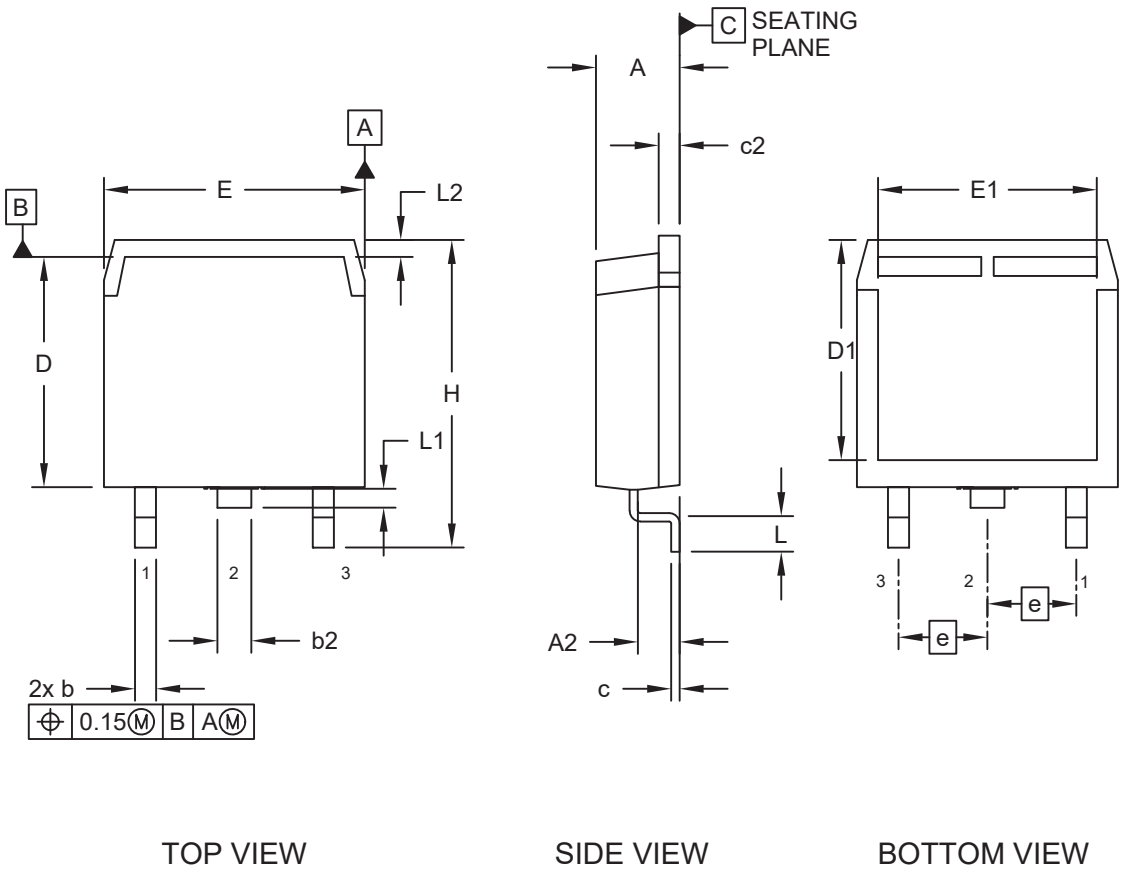
2. Package Specification

This section shows the package specification of this device.

2.1 Package Outline Drawing

The following figure illustrates the D3PAK (TO-268) package outline of this device.

Figure 2-1. Package Outline Drawing



The following table shows the D3PAK (TO-268) dimensions and should be used in conjunction with the package outline drawing.

Table 2-1. D3PAK (TO-268) Dimensions

Symbol	Description	Min. (mm)	Max. (mm)
N	Number of leads	3	
e	Pitch	5.46 BSC	
A	Overall height	4.90	5.11
A2	Seating plane to lead	2.69	2.90
b	Lead width	1.14	1.45
b2	Center lead width	1.96	2.21
H	Overall package length	18.69	19.10
c	Lead thickness	0.41	0.61
c2	Tab thickness	1.45	1.60

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Symbol	Description	Min. (mm)	Max. (mm)
L	Foot length	2.39	2.69
L1	Center lead length	0.94	1.40
L2	Tab length	0.99	1.24
D	Molded body length	13.79	14.00
D1	Thermal pad length	12.40	12.70
E	Total width	15.85	16.21
E1	Thermal pad width	13.31	13.59

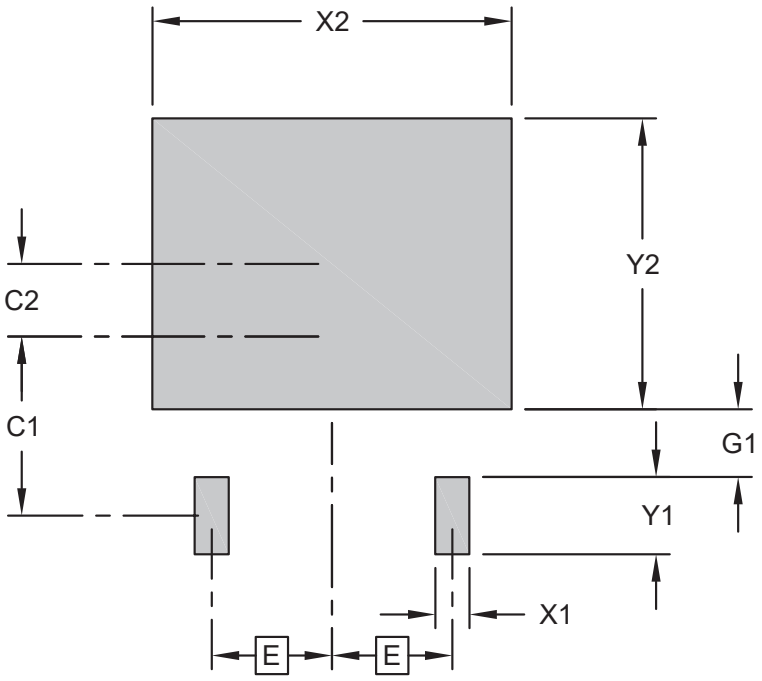
Note:
Dimensioning and tolerancing per ASME Y14.5M.

- BSC: Basic dimension. Theoretically exact value shown without tolerances.

2.2 Recommended Land Pattern

The following figure illustrates the recommended land pattern of this device.

Figure 2-2. Recommended Land Pattern



The following table shows the recommended land pattern dimensions.

Table 2-2. Recommended Land Pattern Dimensions

Symbol	Description	Min. (mm)	Nom. (mm)	Max. (mm)
E	Contact pitch	5.46 BSC		
X2	Center pad width	—	—	16.28
Y2	Center pad length	—	—	13.18
C1	Contact pad spacing	—	8.13	—
C2	Contact pad spacing	—	3.28	—
X1	Contact pad width (X2)	—	—	1.55

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Symbol	Description	Min. (mm)	Nom. (mm)	Max. (mm)
Y1	Contact pad length (X2)	—	—	3.48
G1	Contact pad to center pad (X2)	7.87	—	—

Notes:

- Dimensioning and tolerancing per ASME Y14.5M.
  - BSC: Basic dimension. Theoretically exact value shown without tolerances.
- For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process.

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3. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 3-1. Revision History

Revision	Date	Description
C	09/2024	The following changes are made in this revision of the document: • Updated value for I_{DM} in Table 1-1. • Updated Table 1-2. • Added $V_{GS(th)}$ (Max.) value in Table 1-3. • Updated I_D value (Test Conditions) in Table 1-4. • Added V_{SD} (Max.) value in Table 1-5. • Updated I_{SD} value (Test Conditions) in Table 1-5. • Updated Typical Performance Curves and Package Outline Drawing. • Added Recommended Land Pattern.
B	09/2023	The following changes are made in this revision of the document: • Replaced the lead temperature with reflow temperature in the Table 1-2. • Added Figure 1-8, Figure 1-9, Figure 1-10, and Figure 1-18. • Updated Figure 1-5 and Figure 1-16.
A	05/2023	Document migrated from Microsemi template to Microchip template; Assigned Microchip literature number DS-00004987A, which replaces the previous Microsemi literature number 050-7750.
Initial releases (Microsemi Revisions A and B)	08/2019 – 10/2019	Initial releases.

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