MD2134

High-Speed Ultrasound Beamforming Source Driver

Features

- Multiple-Level Ultrasound Pulser
- Fast-Switching Current Source for Push-Pull Topology
- 250 MHz Maximum Frequency, 4 ns Input to Output Delay
- Fifteen Independent Programmable Output Level Registers
- Pulse Amplitude Modulation (PAM) with 8-Bit Resolution
- 8-Bit Apodization DAC for Peak Output Current via SPI
- Very Low Second Order Harmonic Distortion
- Picoseconds Time-Jitter from Input to Output
- Fast SPI Write and Read-Back of Level and DAC Registers
- +5V Power Supply, 2.5V CMOS Logic Interface
- Drives DN2625 MOSFETs Output up to $230V_{P-P}$
- Programmable Aperture Windowing

Applications

- Medical Imaging Ultrasound Beamforming Transmitter
- Dynamic Focusing B-Scan CW PW Doppler and FM Chirp
- Ultrasonic Phase Array Focusing Transmitter
- Piezoelectric and Microelectromechanical Systems (MEMS) Transducer Waveform Drivers
- High-Speed Arbitrary Waveform Generator
- High-Resolution Non-Destructive Testing (NDT) Phase Array Ultrasound Pulser

General Description

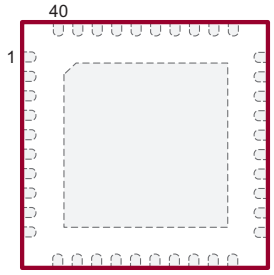
The MD2134 is a high-speed source driver for a pulsed current waveform generator. This programmable and fast arbitrary current level driver is designed for medical ultrasound imaging beamforming applications. It can also be used in High-intensity Focused Ultrasound (HIFU), NDT ultrasound, and other instrument applications.

The MD2134 consists of CMOS digital logic input circuits, an 8-bit current DAC for aperture weighting amplitude control, and a programmable 15-level PAM current-source that does not include a zero level. The fast current sources are constructed with current-switch array, controlled by the LV0–LV15 level-register as the waveform data points. Four logic inputs M[3:0] are used for transmit data level selecting and transmitting timing control pins. Each level can be programmed to a resolution of +/–127, including zero (8-bit) in addition to an 8-bit SPI apodization DAC. The outputs PA and PB are controlled by M[3:0] pins directly, as well as the polarity-flip bit S1 in the SPI register. The high-speed SPI interface will achieve per-scan-line fast data updating for dynamically changing delay time, weighting and waveforms.

The MD2134 outputs are designed to drive two very low-threshold high-voltage depletion N-MOSFETs, such as Microchip's DN2625s, as source drivers. The two DN2625 drains are connected to a center-tap RF pulse transformer. The transformer's secondary output connects to a cable and piezoelectric or capacitive transducer as a load with a good impedance match.

Package Type

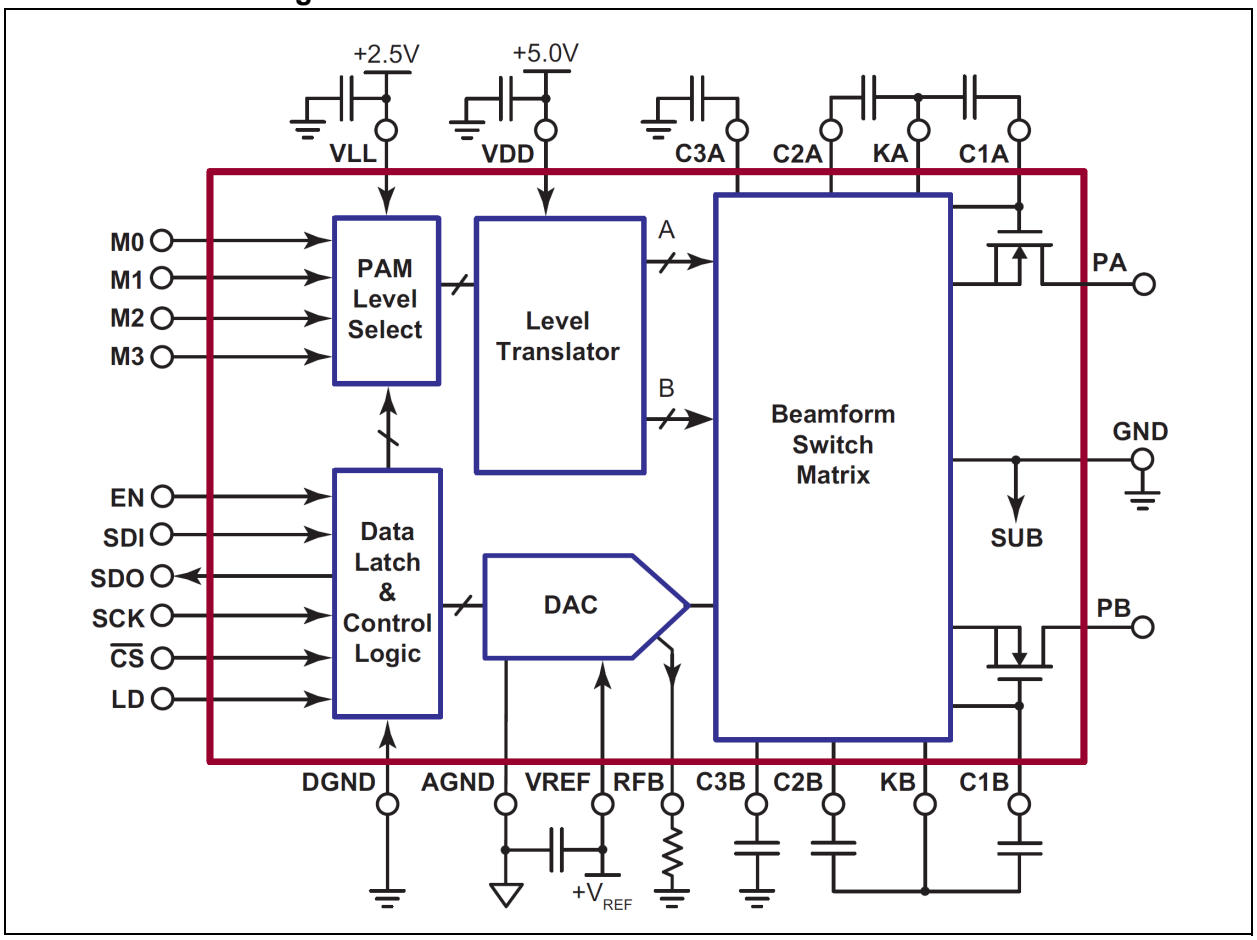
40-lead QFN
(Top view)



See Table 2-1 for pin information.

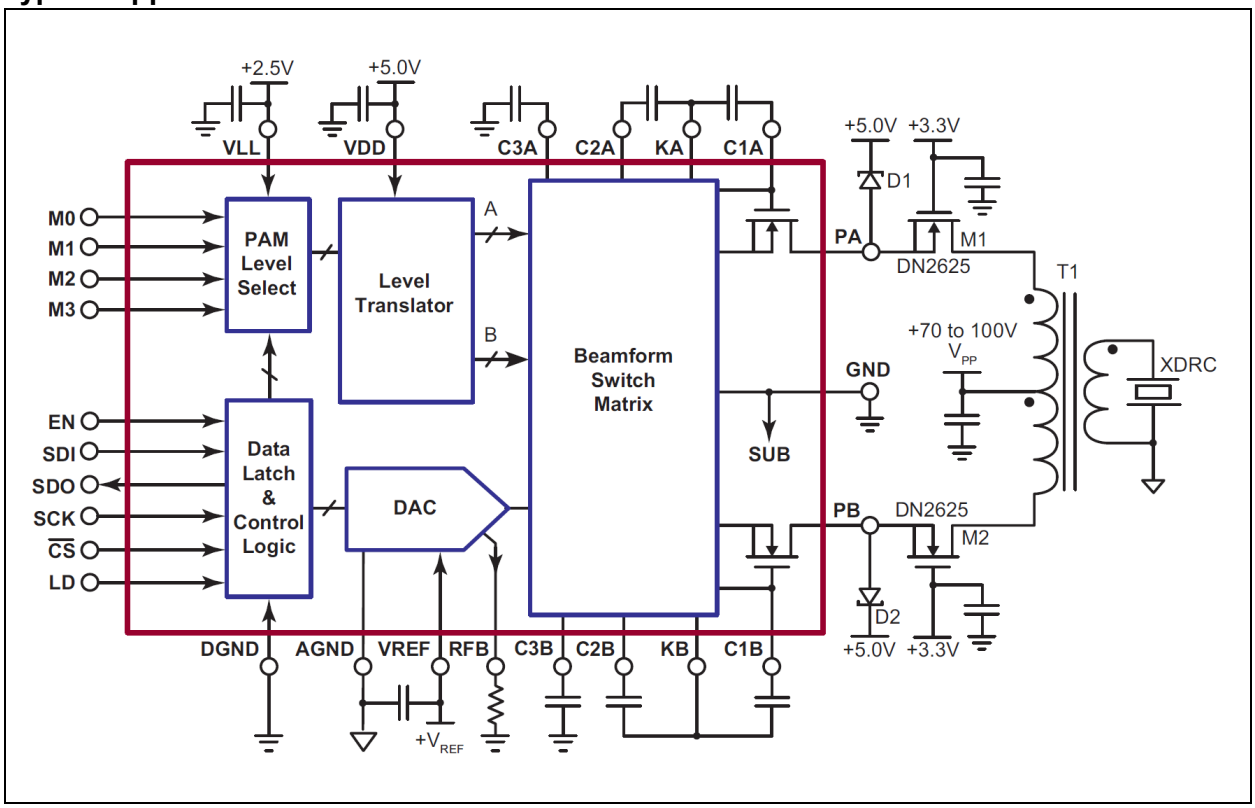
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Functional Block Diagram



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Typical Application Circuit



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Ground, V_{SUB} 0V
Logic Supply, V_{LL} ..... –0.5V to +3.5V
Positive Supply, V_{DD} ..... –0.5V to +6V
Driver Outputs, V_{PA}, V_{PB} ..... –0.5V to +6V
Operating Ambient Temperature, T_A ..... 0°C to +70°C
Storage Temperature, T_S ..... –65°C to +150°C

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: 1 oz. four-layer 3 inches x 4 inches PCB

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: Over operating conditions unless otherwise specified, V_{LL} = +2.5V, V_{DD} = +5V, V_{REF} = 2.5V, R_{FB} = 71.1 kΩ, T_A = 25°C

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
OPERATING SUPPLY VOLTAGES						
Logic Supply	V_{LL}	2.25	—	2.75	V	T_A = 0°C to 70°C, DAC = 0
Power Supply	V_{DD}	4.75	5	5.25	V	
V_{LL} Supply Current EN = 0	I_{LLQ}	—	0.1	1	µA	Standby condition, DAC = 0
V_{DD} Supply Current EN = 0	I_{DDQ}	—	0.2	1	µA	
V_{LL} Supply Current EN = 1	I_{LLEN}	—	5	20	µA	f_{SCK} = 0, all logic input, no transit, DAC = 0
V_{DD} Supply Current EN = 1	I_{DDEN}	—	5	12	mA	
V_{LL} Supply Current EN = 1	I_{LL50}	—	1	3	mA	f_{SCK} = 50 MHz, CW, M[0:3] = 0, DAC = 0
V_{DD} Supply Current EN = 1	I_{DD50}	—	40	85	mA	f_{SCK} = 0, Input = 50 MHz, CW, DAC = 0
OUTPUT CHARACTERISTICS						
Full-Scale Output Peak Current	$I_{MAX-A/B}$	2.88	—	3.52	A	DAC = 255, Level = 127
Output Current Offset	$I_{OO-A/B}$	—	0.5	2	mA	DAC = 0
Output Voltage Range, +10% of $I_{PA/B}$	V_{PA}, V_{PB}	5.3	5.8	—	V	$I_{PA/B}$ = 1A
		5	5.5	—	V	$I_{PA/B}$ = 1.5A
		4.5	5	—	V	$I_{PA/B}$ = 3A
Output Voltage Range, –10% of $I_{PA/B}$		—	1	1.5	V	$I_{PA/B}$ = 1A
		—	1.2	1.7	V	$I_{PA/B}$ = 1.5A
		—	1.8	2.3	V	$I_{PA/B}$ = 3A
APERTURE DAC CHARACTERISTIC						
Resolution	Reso	—	8	—	Bits	
Linearity Error	E_{LINEAR}	—	1	3	%	±% of FSR
Differential Non-Linearity Error	E_{DNL}	—	0.6	1	%	±% of FSR
Monotonicity	MON	—	8	—	Bits	
External Reference Voltage	V_{REF}	1.25	—	2.5	V	
CLOCK AND DATA INPUT/OUTPUT CHARACTERISTICS						
Input Logic High Voltage	V_{IH}	0.8 V_{LL}	—	V_{LL}	V	

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DC ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Over operating conditions unless otherwise specified, V_{LL} = +2.5V, V_{DD} = +5V, V_{REF} = 2.5V, R_{FB} = 71.1 kΩ, T_A = 25°C

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Input Logic Low Voltage	V_{IL}	0	—	0.2 V_{LL}	V	
Input Logic High Current	I_{IH}	—	—	1	µA	
Input Logic Low Current	I_{IL}	–1	—	—	µA	
Input Capacitance	C_{IN}	—	2	—	pF	
Output Logic High Current	I_{OH}	—	—	–5	mA	
Output Logic Low Current	I_{OL}	—	—	5	mA	
Output Logic High Voltage	V_{OH}	1.95	—	—	V	I_{OH} = –5mA
Output Logic Low Voltage	V_{OL}	—	—	0.35	V	I_{OL} = 5 mA

AC ELECTRICAL CHARACTERISTICS

Electrical Specifications: Over operating conditions unless otherwise specified, V_{LL} = +2.5V, V_{DD} = +5V, R_{FB} = 71.1 kΩ, T_A = 25°C

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
DAC to Output Setup Time	t_{ST}	—	—	10	µs	All caps 10 nF, DAC = 0 to 255, settle to 1 LSB
Output Current Rise Time	t_r	—	2	3	ns	1Ω resistor load to V_{DD}, DAC = 85, V_{REF} = 2.5V LV = 127
Output Current Fall Time	t_f	—	2	3	ns	
Input to Output Delay on Rise	t_{dr}	—	4	5	ns	
Input to Output Delay on Fall	t_{df}	—	4	5	ns	
Delay Time Matching	t_M	—	±2	±3	ns	From PA to PB and device to device
Output Jitter	t_J	—	50	—	ps	
SDI Valid to SCK Setup Time	t_1	0	2	—	ns	See **Serial Interface Timing Waveforms**.
SDI Valid to SCK Hold Time	t_2	4	—	—	ns	
SCK High Time (% of 1/f_{SCK})	t_3	45	—	55	%	See **Serial Interface Timing Waveforms**.
SCK Low Time (% of 1/f_{SCK})	t_4	45	—	55	%	
CS Pulse Width	t_5	4	—	—	ns	See **Serial Interface Timing Waveforms**.
LSB SCK High to CS High	t_6	7	—	—	ns	
CS Low to SCK High	t_7	7	—	—	ns	
SDO Propagation Delay from SCK Falling Edge	t_8	—	—	10	ns	
CS High to SCK Raising Edge	t_9	7	—	—	ns	
CS High to LD Raising Edge	t_{10}	10	—	—	ns	
Serial Clock Maximum Frequency	f_{SCK}	40	50	—	MHz	
Clock Input Slew Rate	t_{CSR}	1	—	—	V/ns	
Control/Data Input Slew Rate	t_{DSR}	1	—	—	V/ns	
Total Harmonic Distortion	THD	—	–45	–40	dB	
EN Fall to PA/PB Turn-Off Time	t_{EN-OFF}	—	5	8	ns	50% to 90%
EN Rise to PA/PB Turn-On Time	t_{EN-ON}	—	13.5	20	µs	50% to 10%

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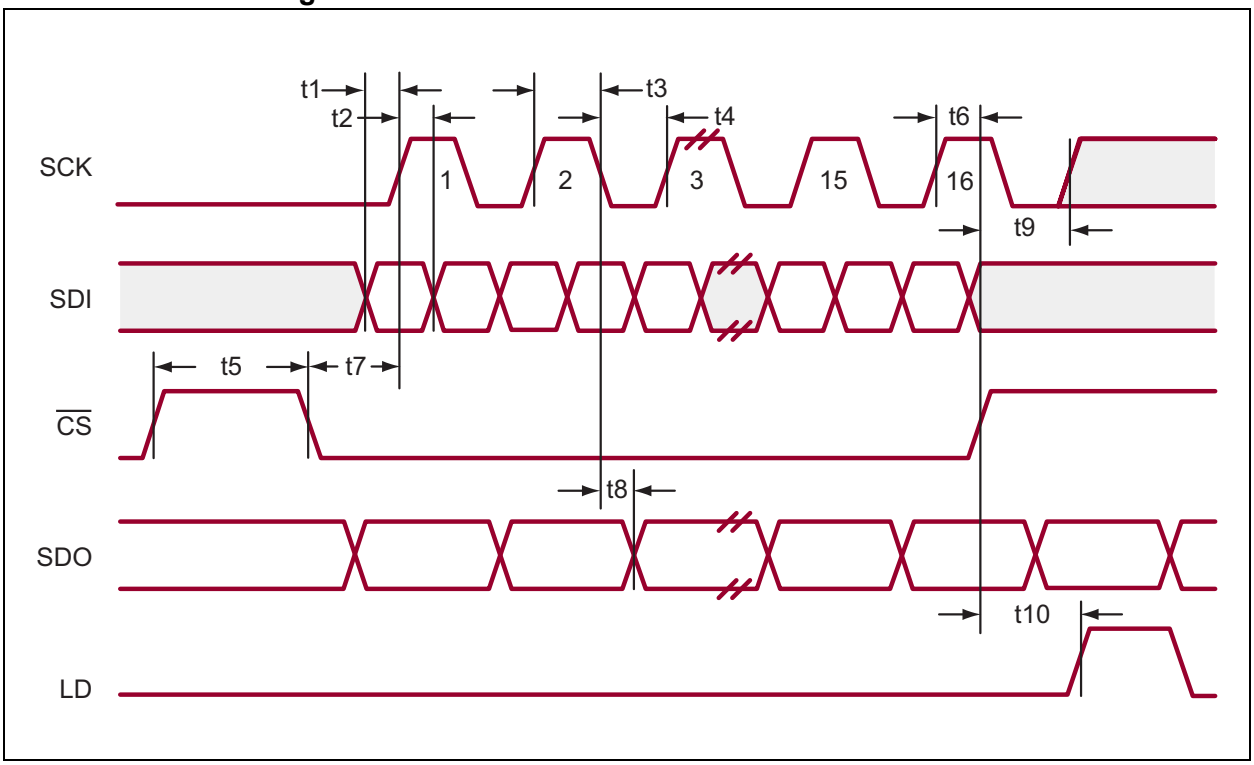
TEMPERATURE SPECIFICATIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
TEMPERATURE RANGE						
Operating Ambient Temperature	T_A	0	—	+70	°C	
Storage Temperature	T_S	–65	—	+150	°C	
PACKAGE THERMAL RESISTANCE						
40-lead QFN	θ_{JA}	—	26	—	°C/W	

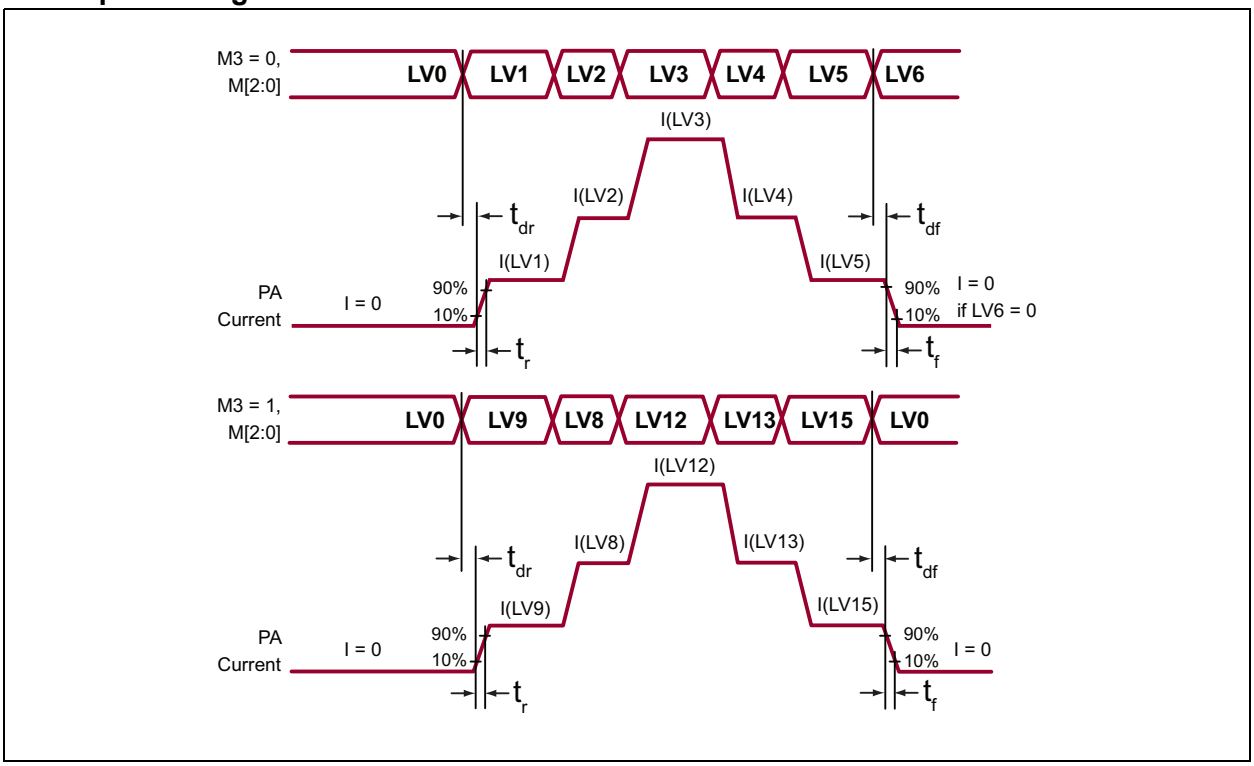
Note 1: 3 inches x 4 inches, 1 oz. four-layer 16-via PCB

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Serial Interface Timing Waveforms



TX Output Timing



2.0 PIN DESCRIPTION

Table 2-1 shows details on the pins of MD2134. See **Package Type** for the location of pins.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	KA	Kelvin connection A
2	GND	High-current output ground
3	C1A	Bypass cap to KA, 10 nF low ESR X7R ceramic cap
4	GND	High-current output ground
5	VDD	Supplies voltage of the gate driver and internal analog circuit
6	C3A	Bypass cap to GND of Pin #7, 10 nF low ESR X7R ceramic cap
7	GND	High-current output ground
8	VLL	Supply voltage of logic circuit
9	DGND	Digital logic ground
10	SCK	Serial clock input
11	SDI	Serial data input
12	M3	Control logic for selecting output current level. See Table 3-3.
13	M2	Control logic for selecting output current level. See Table 3-3.
14	M1	Control logic for selecting output current level. See Table 3-3.
15	M0	Control logic for selecting output current level. See Table 3-3.
16	VDD	Supply voltage of the gate driver and internal analog circuit
17	AGND	Analog reference ground
18	SDO	Serial data output
19	CS	Serial chip select, active low and buffer register loading clock on rising edge
20	LD	DAC data register loading clock on rising edge
21	EN	Enable, EN = Low, PA = PB = High-Z, and all internal registers freeze until next clock rising edge
22	VREF	External reference voltage input
23	RFB	Resistor to GND, 71.1 kΩ 0.1% for the best accuracy
24	GND	High-current output ground
25	C3B	Bypass cap to GND of Pin #24, 10 nF low ESR X7R ceramic cap
26	VDD	Supply voltage of the gate driver and internal analog circuit
27	GND	High-current output ground
28	C1B	Bypass cap to KB, 10 nF low ESR X7R ceramic cap
29	GND	High-current output ground
30	KB	Kelvin connection B
31	C2B	Bypass cap to KB, 10 nF low ESR X7R ceramic cap
32	PB	Current sinking source driver output B, external Schottky diode to VDD
33	PB	Current sinking source driver output B, external Schottky diode to VDD
34	PB	Current sinking source driver output B, external Schottky diode to VDD

Note 1: Pins 35 and 36 are V_{SUB} connected to the center thermal pad internally in the package.

2: All bypass capacitors need to be very close to the pins.

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TABLE 2-1: PIN FUNCTION TABLE (CONTINUED)

Pin Number	Pin Name	Description
35	VSUB	Substrate voltage must connect to the lowest potential of the IC, the ground. (See **Note 1**.)
36	VSUB	Substrate voltage must connect to the lowest potential of the IC, the ground. (See **Note 1**.)
37	PA	Current sinking source driver output A, external Schottky diode to VDD
38	PA	Current sinking source driver output A, external Schottky diode to VDD
39	PA	Current sinking source driver output A, external Schottky diode to VDD
40	C2A	Bypass cap to KA, 10 nF low ESR X7R ceramic cap

Note 1: Pins 35 and 36 are V_{SUB} connected to the center thermal pad internally in the package.

2: All bypass capacitors need to be very close to the pins.

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3.0 FUNCTIONAL DESCRIPTION

TABLE 3-1: DAC INPUT AND OUTPUT DESCRIPTION

MSB			DAC Value Register				LSB	PA/PB Output Current
D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	0	0	(0/255) $I_{MAX–A/B} + I_{OO–A/B}$
0	0	0	0	0	0	0	1	(1/255) $I_{MAX–A/B} + I_{OO–A/B}$
0	1	1	1	1	1	1	1	(127/255) $I_{MAX–A/B} + I_{OO–A/B}$
1	0	0	0	0	0	0	0	(128/255) $I_{MAX–A/B} + I_{OO–A/B}$
1	1	1	1	1	1	1	0	(254/255) $I_{MAX–A/B} + I_{OO–A/B}$
1	1	1	1	1	1	1	1	(255/255) $I_{MAX–A/B} + I_{OO–A/B}$

TABLE 3-2: OUTPUT CURRENT LEVEL CONTROL DATA REGISTER LA_X OR LB_X

MSB			Current Level Data Register LAx or LBx			LSB	Ratio of Full Scale	Output Polarity Control
D6	D5	D4	D3	D2	D1	D0		
1	1	1	1	1	1	1	127/127	M3 = 0 output to PA M3 = 1 output to PB
1	1	1	1	1	1	0	126/127	
—							—	
0	0	0	0	0	0	1	1/127	
0	0	0	0	0	0	0	0	

TABLE 3-3: FAST OUTPUT CURRENT LEVEL CONTROL PIN DESCRIPTION

Input Control Pin Name				PAM Current Level	Description
M3	M2	M1	M0		
0	0	0	0	LV0	PA & PB Both Off, Zero Current
0	0	0	1	LV1	Select LV1 current magnitude to PA
0	0	1	0	LV2	Select LV2 current magnitude to PA
0	0	1	1	LV3	Select LV3 current magnitude to PA
0	1	0	0	LV4	Select LV4 current magnitude to PA
0	1	0	1	LV5	Select LV5 current magnitude to PA
0	1	1	0	LV6	Select LV6 current magnitude to PA
0	1	1	1	LV7	Select LV7 current magnitude to PA
1	0	0	0	LV8	Select LV8 current magnitude to PB
1	0	0	1	LV9	Select LV9 current magnitude to PB
1	0	1	0	LV10	Select LV10 current magnitude to PB
1	0	1	1	LV11	Select LV11 current magnitude to PB
1	1	0	0	LV12	Select LV12 current magnitude to PB
1	1	0	1	LV13	Select LV13 current magnitude to PB
1	1	1	0	LV14	Select LV14 current magnitude to PB
1	1	1	1	LV15	Select LV15 current magnitude to PB

Note: Turning on PA and PB simultaneously can cause overcurrent and permanent damage to the IC, high-voltage MOSFETs or to the transformer.

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TABLE 3-4: SPI CONTROL REGISTERS DESCRIPTION

Data	C1	C0	RA3	RA2	RA1	RA0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Write Data	0	0	0	0	0	0	x	S1	DAC[7:0] Data Write							
	0	0	0	0	0	1	x	x	x	LV1[6:0] PAM current Level Data Write						
	0	0	0	0	1	0	x	x	x	LV2[6:0] PAM current Level Data Write						
	0	0	0	0	1	1	x	x	x	LV3[6:0] PAM current Level Data Write						
	0	0	0	1	0	0	x	x	x	LV4[6:0] PAM current Level Data Write						
	0	0	0	1	0	1	x	x	x	LV5[6:0] PAM current Level Data Write						
	0	0	0	1	1	0	x	x	x	LV6[6:0] PAM current Level Data Write						
	0	0	0	1	1	1	x	x	x	LV7[6:0] PAM current Level Data Write						
	0	0	1	0	0	0	x	x	x	LV8[6:0] PAM current Level Data Write						
	0	0	1	0	0	1	x	x	x	LV9[6:0] PAM current Level Data Write						
	0	0	1	0	1	0	x	x	x	LV10[6:0] PAM current Level Data Write						
	0	0	1	0	1	1	x	x	x	LV11[6:0] PAM current Level Data Write						
	0	0	1	1	0	0	x	x	x	LV12[6:0] PAM current Level Data Write						
	0	0	1	1	0	1	x	x	x	LV13[6:0] PAM current Level Data Write						
	0	0	1	1	1	0	x	x	x	LV14[6:0] PAM current Level Data Write						
	0	0	1	1	1	1	x	x	x	LV15[6:0] PAM current Level Data Write						
Read Back Data	0	1	0	0	0	0	x	S1	DAC[7:0] Data Read							
	0	1	0	0	0	1	x	x	x	LV1[6:0] PAM current Level Data Read						
	0	1	0	0	1	0	x	x	x	LV2[6:0] PAM current Level Data Read						
	0	1	0	0	1	1	x	x	x	LV3[6:0] PAM current Level Data Read						
	0	1	0	1	0	0	x	x	x	LV4[6:0] PAM current Level Data Read						
	0	1	0	1	0	1	x	x	x	LV5[6:0] PAM current Level Data Read						
	0	1	0	1	1	0	x	x	x	LV6[6:0] PAM current Level Data Read						
	0	1	0	1	1	1	x	x	x	LV7[6:0] PAM current Level Data Read						
	0	1	1	0	0	0	x	x	x	LV8[6:0] PAM current Level Data Read						
	0	1	1	0	0	1	x	x	x	LV9[6:0] PAM current Level Data Read						
	0	1	1	0	1	0	x	x	x	LV10[6:0] PAM current Level Data Read						
	0	1	1	0	1	1	x	x	x	LV11[6:0] PAM current Level Data Read						
	0	1	1	1	0	0	x	x	x	LV12[6:0] PAM current Level Data Read						
	0	1	1	1	0	1	x	x	x	LV13[6:0] PAM current Level Data Read						
	0	1	1	1	1	0	x	x	x	LV14[6:0] PAM current Level Data Read						
	0	1	1	1	1	1	x	x	x	LV15[6:0] PAM current Level Data Read						
PWDN	1	0	X	X	X	X	D[9:0] = X Power Down State									
N.A.	1	1	X	X	X	X	(Reserved, Do Not Use)									

Note: S1 is Tx polarity swapping control bit. When S1 = 0 LV1–7 output to PA and LV8–15 output to PB, when S1 = 1 LV1–7 output to PB and LV8–15 output to PA.

3.1 PA and PB Output Current Equations

The in-phase PA and 180° PB output sinking current magnitudes IA and IB can be calculated with Formula A and Formula B in Equation 3-1.

EQUATION 3-1:

$$I_A = \frac{48 \times V_{REF} \times DAC \times (2^6 - 1) \times \frac{LAx}{127}}{9 \times R_{FB}} \quad \text{(A)}$$

$$I_B = \frac{48 \times V_{REF} \times DAC \times (2^6 - 1) \times \frac{LBx}{127}}{9 \times R_{FB}} \quad \text{(B)}$$

In both equations, the V_{REF} is the voltage reference, DAC is the decimal value of the data in the DAC register, R_{FB}, is the setting resistor value in ohms and LAx or LBx is the decimal value of the data in the level register.

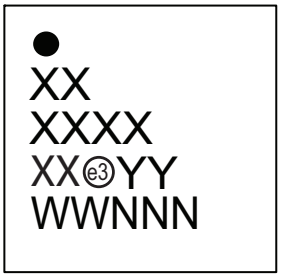
The values of the results from the equations represent the magnitude of the output current. The current flow into the port PA and PB is controlled by M0, M1, M2, and M3. Note that the maximum full scale peak current at PA or PB port only can be obtained at DAC = 255, V_{REF} = 2.5V, R_{FB} = 71.1 kΩ, LAx[6:0] = 127 for PA or LBx[6:0] = 127 for PB.

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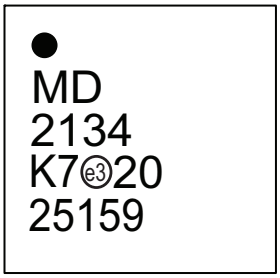
4.0 PACKAGING INFORMATION

4.1 Package Marking Information

40-lead QFN



Example

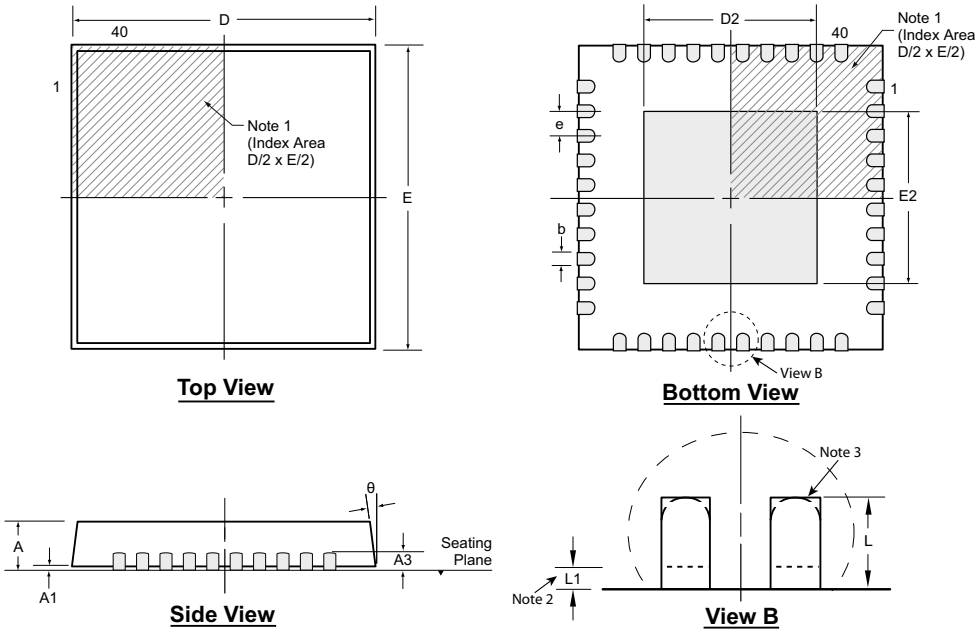


Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

40-Lead QFN Package Outline (K7)

5.00x5.00mm body, 0.80mm height (max), 0.40mm pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Notes:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.*
3. *The inner tip of the lead may be either rounded or square.*

Symbol		A	A1	A3	b	D	D2	E	E2	e	L	L1	θ
Dimension (mm)	MIN	0.70	0.00	0.20 REF	0.15	4.85*	3.45	4.85*	3.45	0.40 BSC	0.25†	0.00	0°
	NOM	0.75	0.02		0.20	5.00	3.60	5.00	3.60		0.35†	-	-
	MAX	0.80	0.05		0.25	5.15*	3.70†	5.15*	3.70†		0.45†	0.15	14°

JEDEC Registration MO-220, Variation WHHE-1, Issue K, June 2006
** This dimension is not specified in the JEDEC drawing.*
† This dimension differs from the JEDEC drawing.
Drawings not to scale.

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APPENDIX A: REVISION HISTORY

Revision A (February 2020)

- Converted Supertex Doc# DSFP-MD2134 to Microchip DS20005926A
- Changed the package marking format
- Removed the 40-lead WQFN K7 M932 media type
- Made minor text changes throughout the document

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	XX	-	X	-	X
Device	Package Options		Environmental		Media Type

Device:	MD2134	=	High-Speed Ultrasound Beamforming Source Driver
Package:	K7	=	40-lead WQFN
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package
Media Type:	(blank)	=	490/Tray for a K7 Package

Example:

a) MD2134K7-G: High-Speed Ultrasound Beamforming Source Driver, 40-lead WQFN, 490/Tray

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ISBN:978-1-5224-5607-0

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