
USB 2.0 Hi-Speed 4-Port Hub Controller with Battery Charging

General Description

The Microchip USX2064 hub is a low-power, configurable, MTT (multi transaction translator) hub controller IC with 4 downstream ports for embedded USB solutions. The 4-port hub supports low-speed, full-speed, and hi-speed (if operating as a hi-speed hub) downstream devices on all of the enabled downstream ports.

Highlights

- High performance, low-power, small footprint hub controller IC with 4 downstream ports
- Fully compliant with the *USB 2.0 Specification* [1]
- Enhanced OEM configuration options available through either a single serial I²C EEPROM, or SMBus slave port
- Available in the following packages:
 - 36-pin SQFN (6x6 mm) (Preferred)
 - 36-pin QFN (6x6 mm) (Legacy)
- **MultiTRAK™**
 - High-performance multiple transaction translator which provides one transaction translator per port
- **PortMap**
 - Flexible port mapping and disable sequencing
- **PortSwap**
 - Programmable USB differential-pair pin locations ease PCB design by aligning USB signal lines directly to connectors
- **PHYBoost**
 - Programmable USB signal drive strength for recovering signal integrity using 4-level driving strength resolution

Hardware Features

- Full power management with individual or ganged power control of each downstream port
- Integrated 1.2 V core regulator
- Fully integrated USB termination and pull-up and pull-down resistors
- Onboard 24 MHz crystal driver, ceramic resonator, or external 24 MHz clock input

Configuration Features

- Customize the vendor ID, product ID, and device ID
- Select whether or not the hub is part of a compound device
- Configure the delay time for filtering the over-current sense inputs
- Select the presence of a permanently hardwired USB peripheral device on a port-by-port basis
- Indicate the maximum current that the 4-port hub consumes from the USB upstream port
- Indicate the maximum current required for the hub controller
- Supports self- and bus-powered operation
- Supports the USB Battery Charging specification Rev. 1.1 for Charging Downstream Ports (CDP)
- Customizable string descriptors up to 31 characters in length for:
 - Product String
 - Manufacturer String
 - Serial Number String
- Pin selectable options for default configuration
 - Downstream Ports as Disabled Ports
 - USB Differential Pair Pin location

Applications

- LCD monitors and TVs
- Multi-function USB peripherals
- PC motherboards
- Set-top boxes, DVD players, DVR/PVR
- Printers and scanners
- PC media drive bay
- Portable hub boxes
- Mobile PC docking
- Embedded systems

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1.0 INTRODUCTION

The Microchip USX2064 is a low-power, configurable, MTT (multi transaction translator) hub controller IC. The hub provides 4 downstream ports for embedded USB solutions and is fully compliant with the *USB 2.0 Specification* [1]. The Microchip hub controller can attach to an upstream port as a full-speed or full-/hi-speed hub. The hub can support low-speed, full-speed, and hi-speed downstream devices when operating as a hi-speed hub.

All required resistors on the USB ports are integrated into the hub. This includes all series termination resistors and all required pull-down and pull-up resistors on D+ and D- pins. The over-current sense inputs for the downstream facing ports have internal pull-up resistors.

The USX2064 hub includes programmable features, such as:

- **MultiTRAK™ Technology:** implements a dedicated Transaction Translator (TT) for each port. Dedicated TTs help maintain consistent full-speed data throughput regardless of the number of active downstream connections.
- **PortMap:** provides flexible port mapping and disable sequences. The downstream ports of a USX2064 hub can be reordered or disabled in any sequence to support multiple platform designs with minimum effort. For any port that is disabled, the USX2064 hub controller automatically reorders the remaining ports to match the USB host controller's port numbering scheme.
- **PortSwap:** allows direct alignment of USB signals (D+/D-) to connectors to avoid uneven trace length or crossing of the USB differential signals on the PCB.
- **PHYBoost:** enables 4 programmable levels of USB signal drive strength in downstream port transceivers. PHY-Boost will also attempt to restore USB signal integrity.

1.1 Configurable Features

The Microchip USX2064 hub controller provides a default configuration that may be sufficient for most applications. Strapping option pins (see [Section 3.3.1 on page 11](#)) provide additional features to enhance the default configuration. When the hub is initialized in the default configuration, the following features may be configured using the strapping options:

- Downstream non-removable ports, where the hub will automatically report as a compound device
- Downstream disabled ports
- Downstream port power control and over-current detection on a ganged or individual basis
- USB signal drive strength
- USB differential pair pin location

The USX2064 hub controller can alternatively be configured by an external I²C EEPROM or a microcontroller as an SMBus slave device, providing the following configurable features:

- Support for compound devices on a port-by-port basis
- Selectable over-current sensing and port power control on an individual or ganged basis to match the circuit board component selection
- Customizable vendor ID, product ID, and device ID
- Configurable delay time for filtering the over-current sense inputs
- Configurable downstream port power-on time reported to the host
- Indication of the maximum current that the hub consumes from the USB upstream port
- Indication of the maximum current required for the hub controller
- Custom string descriptors (up to 31 characters):
 - Product, Manufacturer, and Serial number
- Battery charging

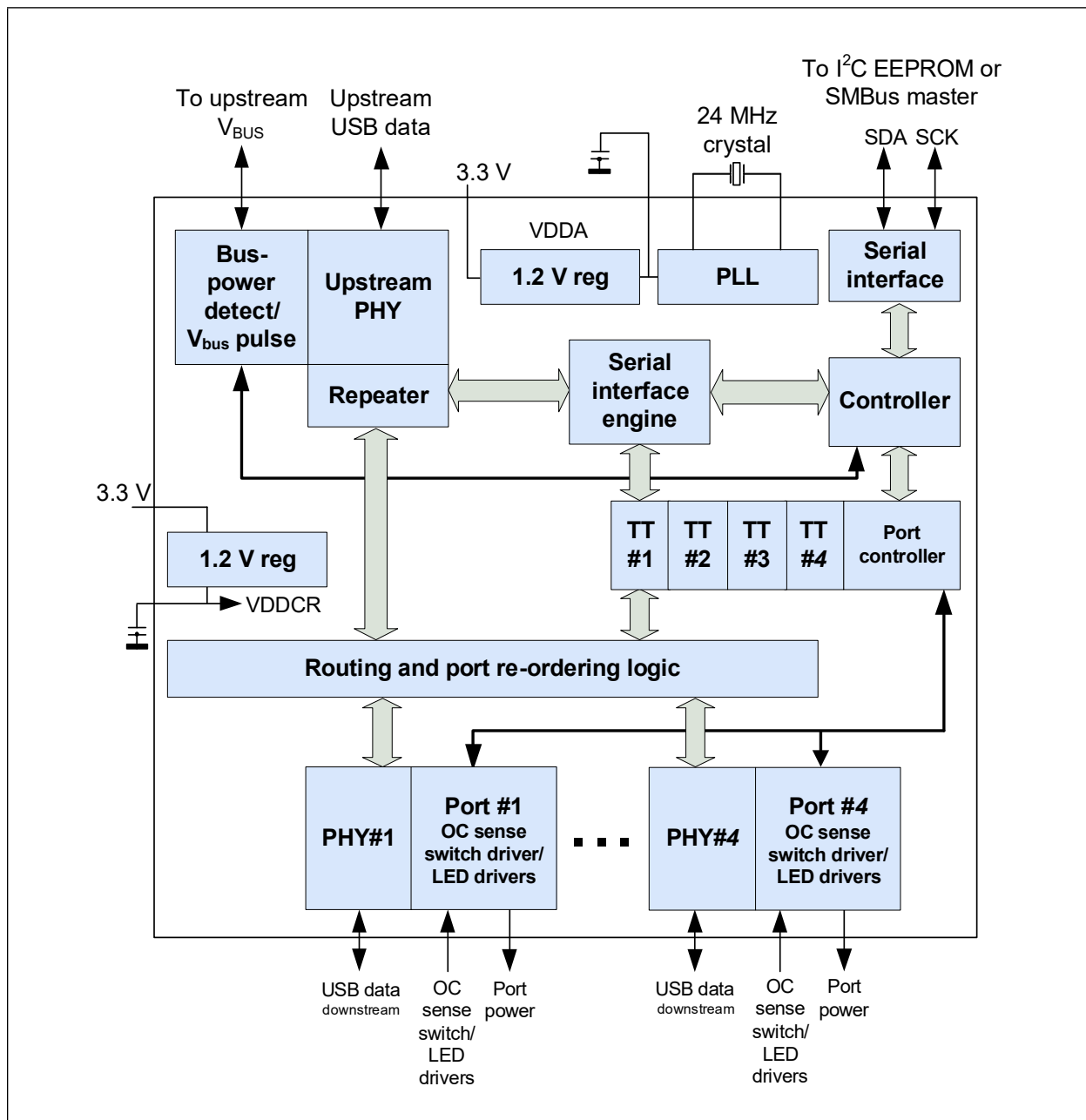
Conventions

Within this manual, the following abbreviations and symbols are used to improve readability.

Example	Description
BIT	Name of a single bit within a field
FIELD.BIT	Name of a single bit (BIT) in FIELD
x...y	Range from x to y, inclusive
BITS[m:n]	Groups of bits from m to n, inclusive
PIN	Pin Name
zzzzb	Binary number (value zzzz)
0xzzz	Hexadecimal number (value zzz)
zzh	Hexadecimal number (value zz)
rsvd	Reserved memory location. Must write 0, read value indeterminate
code	Instruction code, or API function or parameter
Section Name	Section or Document name
VAL	Over-bar indicates active low pin or register bit
x	Don't care
<Parameter>	<> indicate a Parameter is optional or is only used under some conditions
{,Parameter}	Braces indicate Parameter(s) that repeat one or more times
[Parameter]	Brackets indicate a nested Parameter. This Parameter is not real and actually decodes into one or more real parameters.

2.0 BLOCK DIAGRAM

FIGURE 2-1: USX2064 HUB BLOCK DIAGRAM



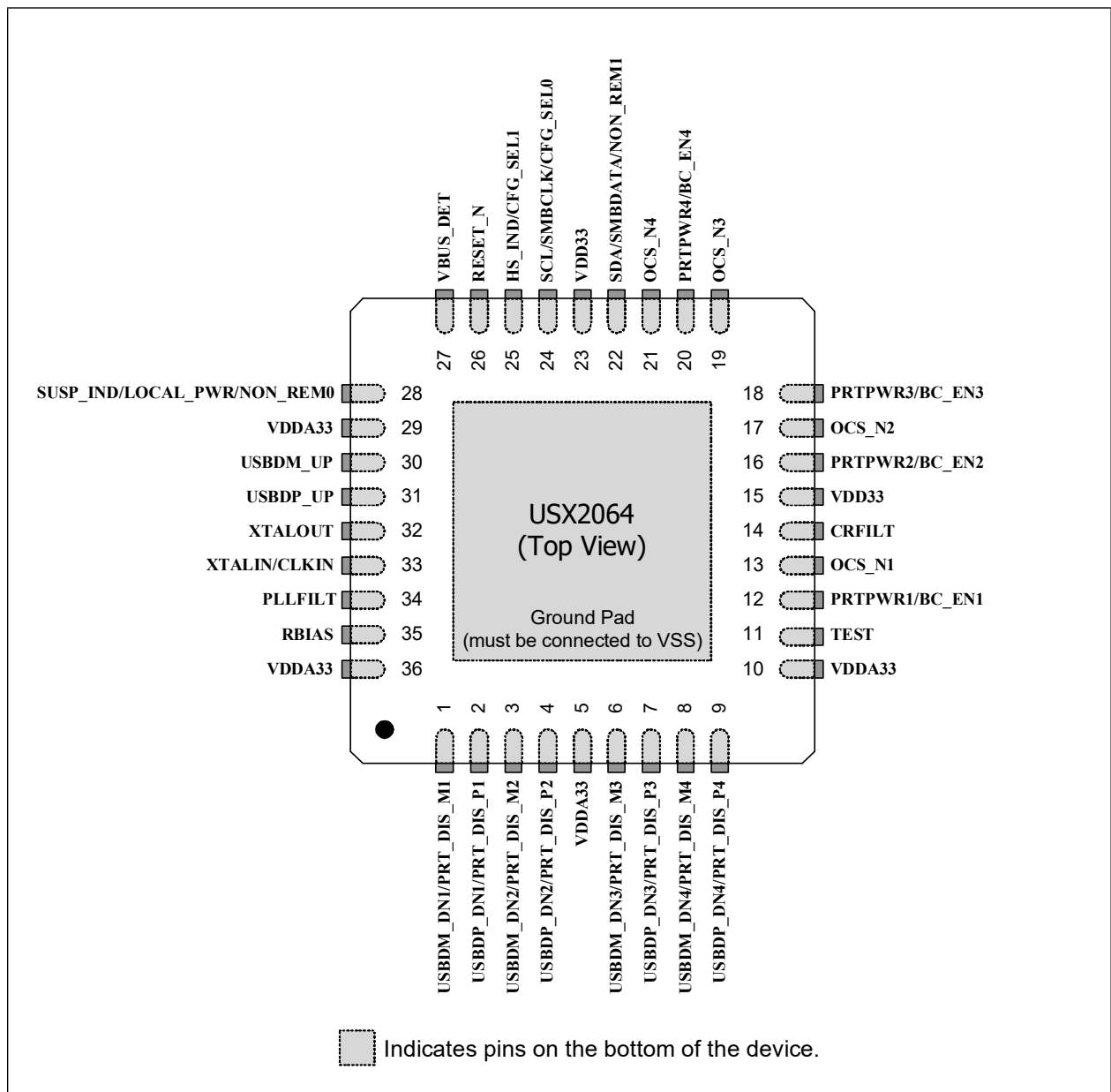
3.0 PINNING INFORMATION

This chapter outlines the device pin configuration. Detailed pin descriptions are listed and outlined by function in [Section 3.3, "Pin Descriptions \(Grouped by Function\)," on page 9](#).

3.1 Pin Configurations

The following figure details the device pinout.

FIGURE 3-1: USX2064 PIN DIAGRAM



USX2064

3.2 Pin List (Alphabetical)

TABLE 3-1: USX2064 PIN LIST

Symbol	Name	Pin Numbers
BC_EN1	Battery Charging Strap Option	12
BC_EN2		16
BC_EN3		18
BC_EN4		20
CFG_SEL0	Configuration Programming Selection	24
CFG_SEL1		25
CLKIN	External Clock Input	33
CRFILT	Core Regulator Filter Capacitor	14
Ground Pad	Exposed Pad Tied to Ground (VSS)	ePad
HS_IND	Hi-Speed Upstream Port Indicator	25
LOCAL_PWR	Local Power Detection	28
NC	No Connect	6
NC		7
NC		18
NC		19
NC		8
NC		9
NC		20
NC		21
NON_REM0	Non-Removable Port Strap Option	28
NON_REM1		22
OCS_N1	Over-Current Sense	13
OCS_N2		17
OCS_N3		19
OCS_N4		21
PLLFLT	PLL Regulator Filter Capacitor	34
PRT_DIS_M1	Downstream Port Disable Strap Option	1
PRT_DIS_M2		3
PRT_DIS_M3		6
PRT_DIS_M4		8
PRT_DIS_P1	Port Disable	2
PRT_DIS_P2		4
PRT_DIS_P3		7
PRT_DIS_P4		9
PRT_PWR1	USB Port Power Enable	12
PRT_PWR2		16
PRT_PWR3		18
PRT_PWR4		20
RBIAS	USB Transceiver Bias	35
RESET_N	Reset Input	26
SCL	Serial Clock	24
SDA	Serial Data Signal	22
SMBCLK	System Management Bus Clock	24

TABLE 3-1: USX2064 PIN LIST (CONTINUED)

Symbol	Name	Pin Numbers
SMBDATA	Server Message Block Data Signal	22
SUSP_IND	Active/Suspend Status Indicator	28
TEST	Test Pin	11
USBDM_UP	USB Bus Data	30
USBDP_UP		31
USBDM_DN1	Hi-Speed USB Data	1
USBDM_DN2		3
USBDM_DN3		6
USBDM_DN4		8
USBDP_DN1		2
USBDP_DN2		4
USBDP_DN3		7
USBDP_DN4		9
VBUS_DET	Upstream VBUS Power Detection	27
VDD33	3.3 V Power	15
VDD33		23
VDDA33	3.3 V Analog Power	5
VDDA33		10
VDDA33		29
VDDA33		36
XTALIN	Crystal Input	33
XTALOUT	Crystal Output	32

3.3 Pin Descriptions (Grouped by Function)

An *N* at the end of a signal name indicates that the active (asserted) state occurs when the signal is at a low voltage level. When the *N* is not present, the signal is asserted when it is at a high voltage level. The terms assertion and negation are used exclusively in order to avoid confusion when working with a mixture of active low and active high signals. The term assert, or assertion, indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term negate, or negation, indicates that a signal is inactive.

TABLE 3-2: USX2064 PIN DESCRIPTIONS

Symbol	Buffer Type	Description
UPSTREAM USB 2.0 INTERFACES		
USBDM_UP USBDP_UP	IO-U	USB Data: connect to the upstream USB bus data signals (host, port, or upstream hub).
VBUS_DET	I/O12	Detect Upstream VBUS Power: detects the state of the upstream VBUS power. The Microchip hub monitors VBUS_DET to determine when to assert the internal D+ pull-up resistor: (signaling a connect event). When designing a detachable hub, this pin should be connected to VBUS on the upstream port via a 2:1 voltage divider. Two 100 kΩ resistors are suggested. For self-powered applications with a permanently attached host, this pin must be connected to 3.3 V (typically VDD33).

TABLE 3-2: USX2064 PIN DESCRIPTIONS (CONTINUED)

Symbol	Buffer Type	Description
DOWNSTREAM USB 2.0 INTERFACES		
USBDP_DN[x:1]/ PRT_DIS_P[x:1]	IO-U	Hi-Speed USB Data: connect to the downstream USB peripheral devices attached to the hub's port. To disable, use a 10 k Ω pull-up resistor to 3.3 V.
USBDM_DN[x:1]/ PRT_DIS_M[x:1]		Downstream Port Disable Strap Option: when enabled by package and configuration settings (see Table 5-1 on page 16), this pin is sampled at RESET_N negation to determine if the port is disabled. To disable a port, pull up both PRT_DIS_M[x:1] and PRT_DIS_P[x:1] pins for the corresponding port number(s). See Section 3.3.1, on page 11 for pull up details.
PRTPWR[x:1]/ BC_EN[x:1]	O12	USB Power Enable: enables power to USB peripheral devices downstream.
	IPD	Battery Charging Strap Option: when enabled by package and configuration settings (see Table 5-1), the pin will be sampled at RESET_N negation to determine if ports [x:1] support the battery charging protocol. When supporting the battery charging protocol, the hub also supports external port power controllers. The battery charging protocol enables a device to draw the currents per the USB battery charging specification. See Section 3.3.1, on page 11 for strap pin details. 1 : Battery charging feature is supported for port x 0 : Battery charging feature is not supported for port x
OCS_N[x:1]	IPU	Over-Current Sense: input from external current monitor indicating an over-current condition.
RBIAS	I-R	USB Transceiver Bias: a 12.0 k Ω (+/- 1%) resistor is attached from ground to this pin to set the transceiver's internal bias settings.
SERIAL PORT INTERFACES		
SDA/ SMBDATA/ NON_REM1	I/OSD12	Serial Data Signal
		System Management Bus Signal
		Non-Removable Port 1 Strap Option: when enabled by package and configuration options (see Table 5-1 on page 16), this pin will be sampled (in conjunction with LOCAL_PWR/SUSP_IND/NON_REM0) at RESET_N negation to determine if ports [x:1] contain permanently attached (non-removable) devices: NON_REM[1:0] = 00 : all ports are removable NON_REM[1:0] = 01 : port 1 is non-removable NON_REM[1:0] = 10 : ports 1 and 2 are non-removable NON_REM[1:0] = 11 : when available, ports 1, 2, and 3 are non-removable When NON_REM[1:0] is chosen such that there is a non-removable device, the hub will automatically report itself as a compound device (using the proper descriptors).
RESET_N	IS	RESET Input: the system can reset the chip by driving this input low. The minimum active low pulse is 1 μ s.
SCL/ SMBCLK/ CFG_SEL0	I/OSD12	Serial Clock (SCL)
		System Management Bus Clock
		Configuration Select: the logic state of this multifunction pin is internally latched on the rising edge of RESET_N (RESET_N negation), and will determine the hub configuration method as described in Table 5-1 .
HS_IND/	I/O12	Hi-Speed Upstream Port Indicator: upstream port connection speed. Asserted = the hub is connected at HS Negated = the hub is connected at FS Note: When implementing an external LED on this pin, the active state is indicated above and outlined in Section 3.3.1.3, on page 12 .
CFG_SEL1		Configuration Programming Select 1: the logic state of this pin is internally latched on the rising edge of RESET_N (RESET_N negation), and will determine the hub configuration method as described in Table 5-1 .

TABLE 3-2: USX2064 PIN DESCRIPTIONS (CONTINUED)

Symbol	Buffer Type	Description
MISC		
XTALIN	ICLKx	Crystal Input: 24 MHz crystal. This pin connects to either one terminal of the crystal or to an external 24 MHz clock when a crystal is not used.
CLKIN		External Clock Input: this pin connects to either one terminal of the crystal or to an external 24 MHz clock when a crystal is not used.
XTALOUT	OCLKx	Crystal Output: the clock output, providing a crystal 24 MHz. When an external clock source is used to drive XTALIN/CLKIN, this pin becomes a no connect.
SUSP_IND/ LOCAL_PWR/ NON_REM0	I/O	Active/Suspend Status LED: indicates USB state of the hub. Negated = unconfigured; or configured and in USB suspend Asserted = hub is configured and is active (i.e., not in suspend)
		Local Power: detects availability of local self-power source. Low = self/local power source is NOT available (i.e., the hub gets all power from the upstream USB VBus) High = self/local power source is available
		Non-Removable 0 Strap Option: when enabled by package and configuration settings (see Table 5-1 on page 16), this pin will be sampled (in conjunction with NON_REM[1]) at RESET_N negation to determine if ports [x:1] contain permanently attached (non-removable) devices: Note: When implementing an external LED on this pin, the active state is outlined below and detailed in Section 3.3.1.3, on page 12.
		NON_REM[1:0] = 00 : all ports are removable; LED is active high NON_REM[1:0] = 01 : port 1 is non-removable; LED is active low NON_REM[1:0] = 10 : ports 1 and 2 are non-removable; LED is active high NON_REM[1:0] = 11 : (when available) ports 1, 2, and 3 are non-removable; LED is active low
TEST	IPD	Test Pin: treat as a no connect pin or connect to ground. No trace or signal should be routed or attached to this pin.
POWER, GROUND, and NO CONNECTS		
CRFILT		VDD Core Regulator Filter Capacitor: this pin must have a 0.1 μF low-ESR capacitor to VSS.
VDD33		3.3 V Power
VDDA33		3.3 V Analog Power
PLLFILT		PLL Regulator Filter Capacitor: this pin must have a 0.1 μF low-ESR capacitor to VSS.
VSS		Ground Pad/ePad: the package slug is the only VSS for the device and must be tied to ground with multiple vias.
NC		No Connect: no signal or trace should be routed or attached to all NC pins.

3.3.1 CONFIGURING THE STRAP PINS

If a pin's strap function is enabled through the hub configuration selection, ([Table 5-1, "Initial Interface/Configuration Options," on page 16](#)) the strap pins must be pulled either high or low using the values provided in [Table 3-3](#). Each strap option is dependent on the pin's buffer type, as outlined in the sections that follow.

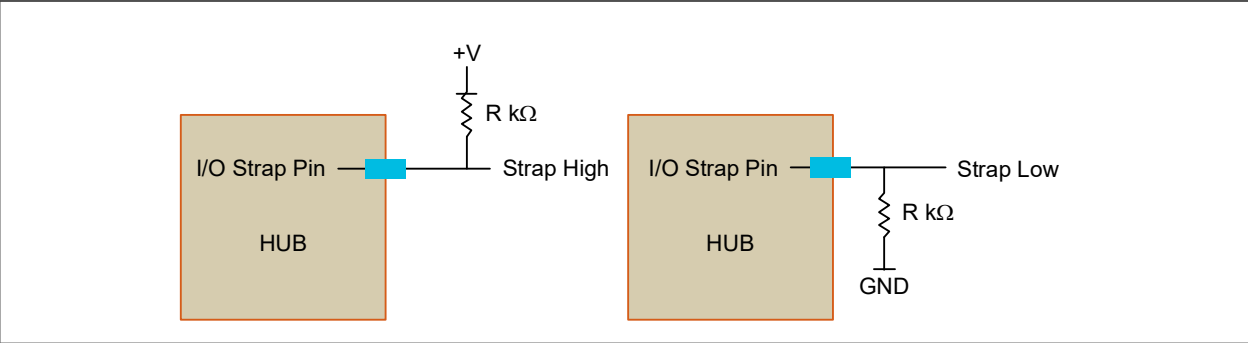
TABLE 3-3: STRAP OPTION SUMMARY

Strap Option	Resistor Value	Buffer Type	Notes
Non-Removable	47 - 100 k Ω	I/O	
Internal Pull-Down	10 k Ω	IPD	- Only applicable to port power pins - Contains a built-in resistor
LED	47 - 100 k Ω	I/O	

3.3.1.1 Non-Removable

If a strap pin's buffer type is I/O, an external pull-up or pull-down must be implemented as shown in [Figure 3-2](#). Use Strap High to set the strap option to 1 and Strap Low to set the strap option to 0. When implementing the Strap Low option, no additional components are needed (i.e., the internal pull-down provides the resistor).

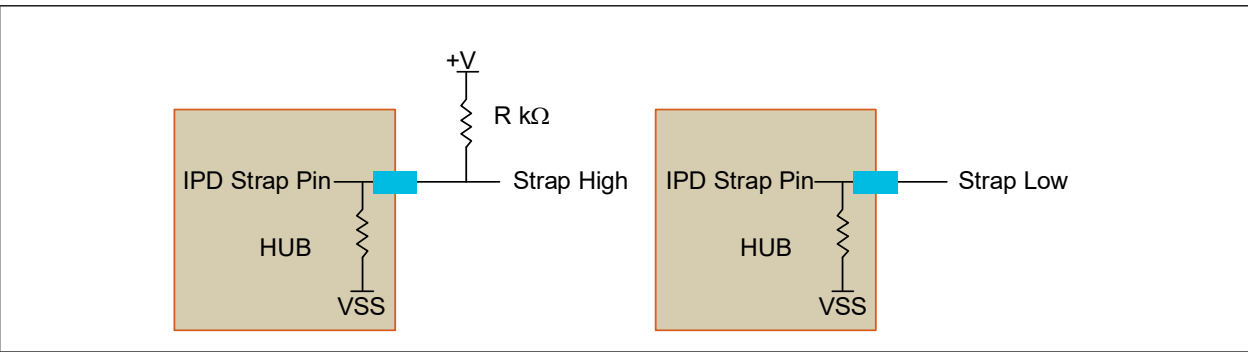
FIGURE 3-2: Non-Removable Pin Strap Example



3.3.1.2 Internal Pull-Down (IPD)

If a strap pin's buffer type is IPD (pins `BC_EN[x:1]`), one of the two hardware configurations outlined below must be implemented. Use the Strap High configuration to set the strap option value to 1 and Strap Low to set the strap option value to 0.

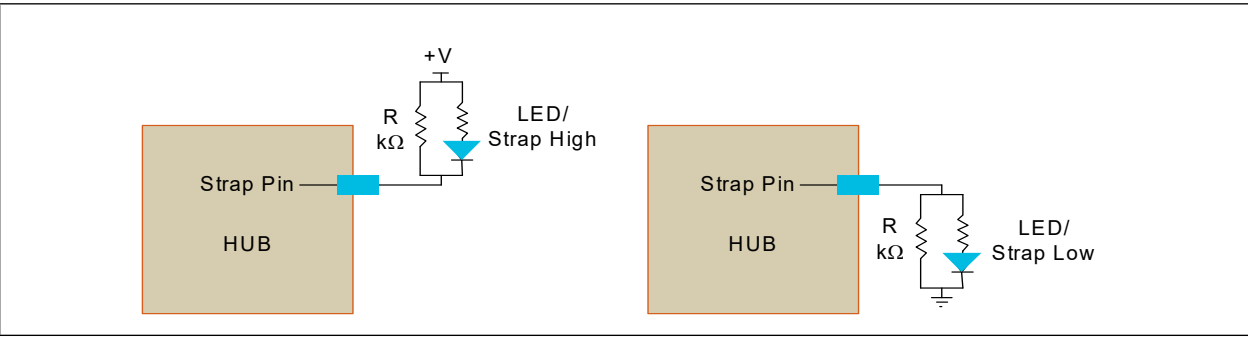
FIGURE 3-3: PIN STRAP OPTION WITH IPD PIN EXAMPLE



3.3.1.3 LED

If a strap pin's buffer type is I/O and shares functionality with an LED, the hardware configuration outlined below must be implemented. The internal logic will drive the LED appropriately (active high or low) depending on the sampled strap option. Use the Strap High configuration to set the strap option value to 1 and Strap Low to set the strap option to 0.

FIGURE 3-4: LED PIN STRAP EXAMPLE



3.4 Buffer Type Descriptions

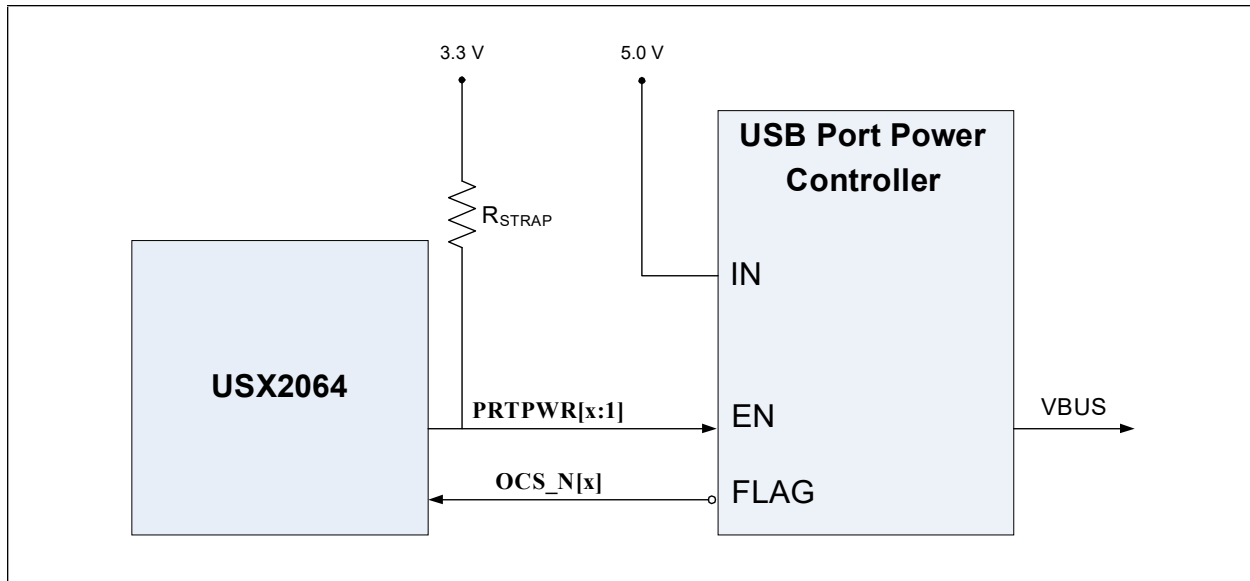
TABLE 3-4: BUFFER TYPE DESCRIPTIONS

Buffer Type	Description
I	Input
I/O	Input/output
IPD	Input with internal weak pull-down resistor
IPU	Input with internal weak pull-up resistor
IS	Input with Schmitt trigger
O12	Output 12 mA
I/O12	Input/output buffer with 12 mA sink and 12 mA source
I/OSD12	Open drain with Schmitt trigger and 12 mA sink. Meets the I ² C-Bus Specification [2] requirements.
ICLKx	XTAL clock input
OCLKx	XTAL clock output
I-R	RBIAS
I/O-U	Analog input/output defined in USB specification

4.0 BATTERY CHARGING SUPPORT

The USX2064 Microchip hub provides support for battery charging devices on a per port basis in compliance with the *USB Battery Charging Specification, Revision 1.1*. The hub can be configured to individually enable each downstream port for battery charging support either via pin strapping as illustrated in Figure 4-1 or by setting the corresponding configuration bits via I²C EEPROM or SMBus (Section 5.1 on page 16).

FIGURE 4-1: BATTERY CHARGING VIA EXTERNAL POWER SUPPLY



Note: R_{STRAP} enables battery charging.

4.1 USB Battery Charging

A downstream port enabled for battery charging turns on port power as soon as the power on reset and hardware configuration process has completed. The hub does not need to be enumerated nor does **VBUS_DET** need to be asserted for the port power to be enabled. These conditions allow battery charging in S3, S4, and S5 system power states as well as in the fully operational state. The *USB Battery Charging Specification* does not interfere with standard USB operation, which allows a device to perform battery charging at any time.

A port that supports battery charging must be able to support 1.5 amps of current on VBUS. Standard USB port power controllers typically only allow for 0.8 amps of current before detecting an over-current condition. Therefore, the 5 volt power supply, port power controller, or over-current protection devices must be chosen to handle the larger current demand compared to standard USB hub designs.

4.1.1 SPECIAL BEHAVIOR OF PRTPWR PINS

The USX2064 enables VBUS by asserting the port power (**PRTPWR**) as soon as the hardware configuration process has completed. If the port detects an over-current condition, **PRTPWR** will be turned off to protect the circuitry from over-loading. If an over-current condition is detected when the hub is not enumerated, **PRTPWR** can only be turned on from the host or if **RESET_N** is toggled. These behaviors provide battery charging even when the hub is not enumerated and protect the hub from sustained short circuit conditions. If the short circuit condition persists when the hub is plugged into a host system the user is notified that a port has an over-current condition. Otherwise **PRTPWR** turned on by the host system and the ports operate normally.

4.2 Battery Charging Configuration

The battery charging option can be configured in one of two ways:

- When the hub is brought up in the default configuration with strapping options enabled, with the **PRT-PWR[x:1]/BC_EN[x:1]** pins configured. See the following sections for details:
 - [Section 3.3, "Pin Descriptions \(Grouped by Function\)," on page 9](#)
 - [Section 3.3.1.2, "Internal Pull-Down \(IPD\)," on page 12](#)

When the hub is initialized for configuration over I²C EEPROM or SMBus. Either of these interfaces can be used to configure the battery charging option.

4.2.1 BATTERY CHARGING ENABLED VIA I²C EEPROM OR SMBUS

Register memory map location 0xD0 is allocated for battery charging support. The Battery Charging register at location 0xD0 starting from bit 1 enables battery charging for each downstream port when asserted. Bit 1 represents port 1, bit 2 represents port 2, etc. Each port with battery charging enabled asserts the corresponding **PRT-PWR[x:1]** pin.

5.0 INITIAL INTERFACE/CONFIGURATION OPTIONS

The hub must be configured in order to correctly function when attached to a USB host controller. The hub can be configured either internally or externally by setting the `CFG_SEL[1:0]` pins (immediately after `RESET_N` negation) as outlined in the table below.

Note: See Chapter 11 (Hub Specification) of the USB specification for general details regarding hub operation and functionality.

To configure the hub externally, there are two principal ways to interface to the hub: over SMBus or I²C EEPROM. The hub can be configured internally, where several default configurations are available as described in the table below. When configured internally, additional configuration is available using the strap options (listed in [Section 3.3.1 on page 11](#)).

Note: Strap options are not available when configuring the hub over I²C or SMBus.

TABLE 5-1: INITIAL INTERFACE/CONFIGURATION OPTIONS

CFG_SEL[1]	CFG_SEL[0]	Description
0	0	Default configuration: • Strap options enabled • Self-powered operation enabled • Individual power switching • Individual over-current sensing
0	1	The hub is configured externally over SMBus (as an SMBus slave device): • Strap options disabled • All registers configured over SMBus
1	0	Default configuration with the following overrides: • Bus-powered operation
1	1	The hub is configured over 2-wire I ² C EEPROM: • Strap options disabled • All registers configured by I²C EEPROM

5.1 Internal Register Set (Common to I²C EEPROM and SMBus)

The register set available when configuring the hub to interface over I²C or SMBus is outlined in the table below. Each register has R/W capability, where EEPROM reset values are 0x00. Reserved registers should be written to 0 unless otherwise specified. Contents read from unavailable registers should be ignored.

Address	Register Name	Default ROM Values (Hexidecimal)
00h	Vendor ID LSB	24
01h	Vendor ID MSB	04
02h	Product ID LSB	14
03h	Product ID MSB	25
04h	Device ID LSB	B3
05h	Device ID MSB	0B
06h	Configuration Data Byte 1	9B
07h	Configuration Data Byte 2	20
08h	Configuration Data Byte 3	02
09h	Non-Removable Devices	00
0Ah	Port Disable (Self)	00

Address	Register Name	Default ROM Values (Hexidecimal)
0Bh	Port Disable (Bus)	00
0Ch	Max Power (Self)	01
0Dh	Max Power (Bus)	32
0Eh	Hub Controller Max Current (Self)	01
0Fh	Hub Controller Max Current (Bus)	32
10h	Power-on Time	32
11h	Language ID High	00
12h	Language ID Low	00
13h	Manufacturer String Length	00
14h	Product String Length	00
15h	Serial String Length	00
16h-53h	Manufacturer String	00
54h-91h	Product String	00
92h-CFh	Serial String	00
D0h	Battery Charging Enable	00
E0h	rsvd	00
F5h	rsvd	00
F6h	Boost_Up	00
F7h	rsvd	00
F8h	Boost_x:0	00
F9h	rsvd	00
FAh	Port Swap	00
FBh	Port Map 12	00
FCh	Port Map 34	00
FD-FEh	rsvd	00
FFh	Status/Command Note: SMBus register only	00

5.1.1 REGISTER 00H: VENDOR ID (LSB)

Bit Number	Bit Name	Description
7:0	VID_LSB	Least Significant Byte of the Vendor ID: a 16-bit value that uniquely identifies the Vendor of the user device (assigned by USB-Interface Forum). Set this field using either the SMBus or I ² C EEPROM interface options.

5.1.2 REGISTER 01H: VENDOR ID (MSB)

Bit Number	Bit Name	Description
7:0	VID_MSB	Most Significant Byte of the Vendor ID: a 16-bit value that uniquely identifies the Vendor of the user device (assigned by USB-Interface Forum). Set this field using either the SMBus or I ² C EEPROM interface options.

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5.1.3 REGISTER 02H: PRODUCT ID (LSB)

Bit Number	Bit Name	Description
7:0	PID_LSB	Least Significant Byte of the Product ID: a 16-bit value that uniquely identifies the Product ID of the user device. Set this field using either the SMBus or I ² C EEPROM interface options.

5.1.4 REGISTER 03H: PRODUCT ID (MSB)

Bit Number	Bit Name	Description
7:0	PID_MSB	Most Significant Byte of the Product ID: a 16-bit value that uniquely identifies the Product ID of the user device. Set this field using either the SMBus or I ² C EEPROM interface options.

5.1.5 REGISTER 04H: DEVICE ID (LSB)

Bit Number	Bit Name	Description
7:0	DID_LSB	Least Significant Byte of the Device ID: a 16-bit device release number in BCD format (assigned by OEM). Set this field using either the SMBus or I ² C EEPROM interface options.

5.1.6 REGISTER 05H: DEVICE ID (MSB)

Bit Number	Bit Name	Description
7:0	DID_MSB	Most Significant Byte of the Device ID: a 16-bit device release number in BCD format (assigned by OEM). Set this field using either the SMBus or I ² C EEPROM interface options.

5.1.7 REGISTER 06H: CONFIG_BYTE_1

Bit Number	Bit Name	Description
7	SELF_BUS_PWR	Self or Bus Power: selects between self- and bus-powered operation. The hub is either self-powered (draws less than 2 mA of upstream bus power) or bus-powered (limited to a 100 mA maximum of upstream power prior to being configured by the host controller). When configured as a bus-powered device, the Microchip hub consumes less than 100 mA of current prior to being configured. After configuration, the bus-powered Microchip hub, along with all associated hub circuitry, any embedded devices (if part of a compound device), and all externally available downstream ports (max 100 mA) must consume no more than 500 mA of upstream VBUS current. The current consumption is system dependent and must not violate the <i>USB 2.0 Specification</i> [1]. When configured as a self-powered device, < 1 mA of upstream VBUS current is consumed and all ports are available. Each port is capable of sourcing 500 mA of current. This field is set over either the SMBus or I²C EEPROM interface options. 0 : bus-powered operation 1 : self-powered operation If dynamic power switching is enabled (Section 5.1.8), this bit is ignored and LOCAL_PWR is used to determine if the hub is operating from self or bus power.
6	rsvd	
5	HS_DISABLE	Hi-Speed Disable: disables the capability to attach as either a hi- or full-speed device, forcing full-speed attachment only (i.e., no hi-speed support). 0 : hi-/full-speed 1 : full-speed only (hi-speed disabled)
4	MTT_ENABLE	Multi-TT Enable: enables one transaction translator per port operation. Selects between a mode where only one transaction translator is available for all ports (single-TT), or each port gets a dedicated transaction translator (multi-TT). 0 : single TT for all ports 1 : multi-TT (one TT per port)
3	EOP_DISABLE	EOP Disable: disables End Of Packet (EOP) generation at End Of Frame Time #1 (EOF1) when in full-speed mode. During full-speed operation only, the hub can send EOP when no downstream traffic is detected at EOF1. See the <i>USB 2.0 Specification, Section 11.3.1</i> for details. 0 : EOP generation is normal 1 : EOP generation is disabled
2:1	CURRENT_SNS	Over-Current Sense: selects current sensing on all ports (ganged); a port-by-port basis (individual); or none (for bus-powered hubs only). The ability to support current sensing on a ganged or port-by-port basis is hardware implementation dependent. 00 : ganged sensing 01 : individual sensing 1x : over-current sensing not supported (use with bus-powered configurations)
0	PORT_PWR	Port Power Switching: enables power switching on all ports (ganged) or a port-by-port basis (individual). The ability to support power enabling on a ganged or port-by-port basis is hardware implementation dependent. 0 : ganged switching 1 : individual switching

5.1.8 REGISTER 07H: CONFIGURATION DATA BYTE 2

Bit Number	Bit Name	Description
7	DYNAMIC	Dynamic Power Enable: controls the ability of the hub to automatically change from self-powered to bus-powered operation if the local power source is removed or unavailable. It can also go from bus-powered to self-powered operation if the local power source is restored. When dynamic power switching is enabled, the hub detects the availability of a local power source by monitoring LOCAL_PWR. If the hub detects a change in power source availability, the hub immediately disconnects and removes power from all downstream devices. It also disconnects the upstream port. The hub will then re-attach to the upstream port as either a bus-powered hub (if local power is unavailable) or a self-powered hub (if local power is available). 0 : no dynamic auto-switching 1 : dynamic auto-switching capable
6	rsvd	
5:4	OC_TIMER	Over Current Timer Delay: 00 : 0.1 ms 01 : 4.0 ms 10 : 8.0 ms 11 : 16.0 ms
3	COMPOUND	Compound Device: indicates the hub is part of a compound device (see the <i>USB Specification</i> for definition). The applicable port(s) must also be defined as having a non-removable device. Note: When configured via strapping options, declaring a port as non-removable automatically causes the hub controller to report that it is part of a compound device. 0 : no 1 : yes, the hub is part of a compound device
2:0	rsvd	

5.1.9 REGISTER 08H: CONFIGURATION DATA BYTE 3

Bit Number	Bit Name	Description
7:4	rsvd	
3	PRTMAP_EN	Port Mapping Enable: selects the method used by the hub to assign port numbers and disable ports. 0 : standard mode 1 : port mapping mode
2:1	rsvd	
0	STRING_EN	Enables String Descriptor Support 0 : string support disabled 1 : string support enabled

5.1.10 REGISTER 09H: NON-REMOVABLE DEVICE

Bit Number	Bit Name	Description
7:0	NR_DEVICE	Non-Removable Device: indicates which port has a non-removable device. 0 : port is removable 1 : port is non-removable Bit 7 : rsvd Bit 6 : rsvd Bit 5 : rsvd Bit 4 : controls port 4 Bit 3 : controls port 3 Bit 2 : controls port 2 Bit 1 : controls port 1 Bit 0 : rsvd Note: The device must provide its own descriptor data. When using the default configuration, the NON_REM[1:0] pins will designate the appropriate ports as being non-removable.

5.1.11 REGISTER 0AH: PORT DISABLE FOR SELF-POWERED OPERATION

Bit Number	Bit Name	Description
7:0	PORT_DIS_SP	Port Disable Self-Powered: disables one or more ports. 0 = port is available 1 = port is disabled Bit 7 : rsvd Bit 6 : rsvd Bit 5 : rsvd Bit 4 : controls port 4 Bit 3 : controls port 3 Bit 2 : controls port 2 Bit 1 : controls port 1 Bit 0 : rsvd During self-powered operation when mapping mode is disabled (PRTMAP_EN = 0), this register selects the ports that will be permanently disabled. These ports are then unavailable and cannot be enabled or enumerated by a host controller. The ports can be disabled in any order, where the internal logic will automatically report the correct number of enabled ports to the USB host. The active ports will be reordered in order to ensure proper function. When using the default configuration, PRT_DIS_P[x:1] and PRT_DIS_M[x:1] pins disable the appropriate ports.

5.1.12 REGISTER 0BH: PORT DISABLE FOR BUS-POWERED OPERATION

Bit Number	Bit Name	Description
7:0	PORT_DIS_BP	Port Disable Bus-Powered: disables one or more ports. 0 = port is available 1 = port is disabled Bit 7 : rsvd Bit 6 : rsvd Bit 5 : rsvd Bit 4 : controls port 4 Bit 3 : controls port 3 Bit 2 : controls port 2 Bit 1 : controls port 1 Bit 0 : rsvd During self-powered operation when mapping mode is disabled (PRTMAP_EN = 0), this selects the ports which will be permanently disabled. These ports are then unavailable and cannot be enabled or enumerated by a host controller. The ports can be disabled in any order, where the internal logic will automatically report the correct number of enabled ports to the USB host. The active ports will be reordered in order to ensure proper function. When using the internal default option, the PRT_DIS_P[x:1] and PRT_DIS_M[x:1] pins disable the appropriate ports.

5.1.13 REGISTER 0CH: MAX POWER FOR SELF-POWERED OPERATION

Bit Number	Bit Name	Description
7:0	MAX_PWR_SP	Max Power Self-Powered: the value in 2 mA increments that the hub consumes from an upstream port (VBUS) when operating as a self-powered hub. This value includes the hub silicon along with the combined power consumption (from VBUS) of all associated circuitry on the board. This value also includes the power consumption of a permanently attached peripheral if the hub is configured as a compound device. The embedded peripheral reports 0 mA in its descriptors. Note: The <i>USB 2.0 Specification</i> does not permit this value to exceed 100 mA

5.1.14 REGISTER 0DH: MAX POWER FOR BUS-POWERED OPERATION

Bit Number	Bit Name	Description
7:0	MAX_PWR_BP	Max Power Bus-Powered: the value in 2 mA increments that the hub consumes from an upstream port (VBUS) when operating as a bus-powered hub. This value includes the hub silicon along with the combined power consumption (from VBUS) of all associated circuitry on the board. This value also includes the power consumption of a permanently attached peripheral if the hub is configured as a compound device. The embedded peripheral reports 0 mA in its descriptors.

5.1.15 REGISTER 0EH: HUB CONTROLLER MAX CURRENT FOR SELF-POWERED OPERATION

Bit Number	Bit Name	Description
7:0	HC_MAX_C_SP	Hub Controller Max Current Self-Powered: the value in 2 mA increments that the hub consumes from an upstream port (VBUS) when operating as a self-powered hub. This value includes the hub silicon along with the combined power consumption (from VBUS) of all associated circuitry on the board. This value does NOT include the power consumption of a permanently attached peripheral if the hub is configured as a compound device. Note: The <i>USB 2.0 Specification</i> does not permit this value to exceed 100 mA. A value of 50 (decimal) indicates 100 mA, which is the default value.

5.1.16 REGISTER 0FH: HUB CONTROLLER MAX CURRENT FOR BUS-POWERED OPERATION

Bit Number	Bit Name	Description
7:0	HC_MAX_C_BP	Hub Controller Max Current Bus-Powered: the value in 2 mA increments that the hub consumes from an upstream port (VBUS) when operating as a bus-powered hub. This value will include the hub silicon along with the combined power consumption (from VBUS) of all associated circuitry on the board. Note: This value will not include the power consumption of a permanently attached peripheral if the hub is configured as a compound device. A value of 50 (decimal) would indicate 100 mA, which is the default value.

5.1.17 REGISTER 10H: POWER-ON TIME

Bit Number	Bit Name	Description
7:0	POWER_ON_TIME	Power-On Time: the length of time that it takes (in 2 ms intervals) from the time the host initiated the power-on sequence on a port until the port has adequate power.

5.1.18 REGISTER 11H: LANGUAGE ID HIGH

Bit Number	Bit Name	Description
7:0	LANG_ID_H	USB Language ID: upper 8 bits of a 16-bit ID field

5.1.19 REGISTER 12H: LANGUAGE ID LOW

Bit Number	Bit Name	Description
7:0	LANG_ID_L	USB Language ID: lower 8 bits of a 16-bit ID field

5.1.20 REGISTER 13H: MANUFACTURER STRING LENGTH

Bit Number	Bit Name	Description
7:0	MFR_STR_LEN	Manufacturer String Length: with a maximum string length of 31 characters (when supported).

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5.1.21 REGISTER 14H: PRODUCT STRING LENGTH

Bit Number	Bit Name	Description
7:0	PRD_STR_LEN	Product String Length: with a maximum string length of 31 characters (when supported).

5.1.22 REGISTER 15H: SERIAL STRING LENGTH

Bit Number	Bit Name	Description
7:0	SER_STR_LEN	Serial String Length: with a maximum string length of 31 characters (when supported).

5.1.23 REGISTER 16H-53H: MANUFACTURER STRING

Bit Number	Bit Name	Description
7:0	MFR_STR	Manufacturer String: UNICODE UTF-16LE per <i>USB 2.0 Specification</i>: with a maximum string length of 31 characters (when supported). Note: The string consists of individual 16-bit UNICODE UTF-16LE characters. The characters will be stored starting with the LSB at the least significant address and the MSB at the next 8-bit location. (Subsequent characters must be stored in sequential contiguous addresses in the same LSB, MSB manner.) Warning: Close attention to the byte order of the selected programming tool should be monitored.

5.1.24 REGISTER 54H-91H: PRODUCT STRING

Bit Number	Bit Name	Description
7:0	PRD_STR	Product String: UNICODE UTF-16LE per <i>USB 2.0 Specification</i> When supported, the maximum string length is 31 characters (62 bytes). Note: The string consists of individual 16-bit UNICODE UTF-16LE characters. The characters will be stored starting with the LSB at the least significant address and the MSB at the next 8-bit location. (Subsequent characters must be stored in sequential contiguous address in the same LSB, MSB manner.) Warning: Close attention to the byte order of the selected programming tool should be monitored.

5.1.25 REGISTER 92H-CFH: SERIAL STRING

Bit Number	Bit Name	Description
7:0	SER_STR	Serial String: UNICODE UTF-16LE per USB 2.0 specification When supported, the maximum string length is 31 characters (62 bytes). Note: The string consists of individual 16-bit UNICODE UTF-16LE characters. The characters will be stored starting with the LSB at the least significant address and the MSB at the next 8-bit location. (Subsequent characters must be stored in sequential contiguous address in the same LSB, MSB manner.) Warning: Close attention to the byte order of the selected programming tool should be monitored.

5.1.26 REGISTER D0H: BATTERY CHARGING ENABLE

Bit Number	Bit Name	Description
7:0	BC_EN	Battery Charging Enable: enables the battery charging feature for the corresponding port. 0 : battery charging support is not enabled 1 : battery charging support is enabled Bit 7 : rsvd Bit 6 : rsvd Bit 5 : rsvd Bit 4 : controls port 4 Bit 3 : controls port 3 Bit 2 : controls port 2 Bit 1 : controls port 1 Bit 0 : rsvd

5.1.27 REGISTER F6H: BOOST_UP

Bit Number	Bit Name	Description
7:2	rsvd	
1:0	BOOST_IOUT	USB electrical signaling drive strength boost bit for the upstream port. 00 : normal electrical drive strength - no boost 01 : elevated electrical drive strength - low (~ 4% boost) 10 : elevated electrical drive strength - medium (~ 8% boost) 11 : elevated electrical drive strength - high (~12% boost) Note: Boost could result in non-USB compliant parameters. Therefore, a value of 00 should be implemented unless specific implementation issues require additional signal boosting to correct for degraded USB signalling levels.

5.1.28 REGISTER F8H: BOOST_4:0

Bit Number	Bit Name	Description
7:6	BOOST_IOUT_4	USB electrical signaling drive strength boost bit for downstream port 4. 00 : normal electrical drive strength - no boost 01 : elevated electrical drive strength - low (~4% boost) 10 : elevated electrical drive strength - medium (~ 8% boost) 11 : elevated electrical drive strength - high (~12% boost)
5:4	BOOST_IOUT_3	USB electrical signaling drive strength boost bit for downstream port 3. 00 : normal electrical drive strength - no boost 01 : elevated electrical drive strength - low (~4% boost) 10 : elevated electrical drive strength - medium (~ 8% boost) 11 : elevated electrical drive strength - high (~12% boost)
3:2	BOOST_IOUT_2	USB electrical signaling drive strength boost bit for downstream port 2. 00 : normal electrical drive strength - no boost 01 : elevated electrical drive strength - low (~4% boost) 10 : elevated electrical drive strength - medium (~ 8% boost) 11 : elevated electrical drive strength - high (~12% boost)
1:0	BOOST_IOUT_1	USB electrical signaling drive strength boost bit for downstream port 1. 00 : normal electrical drive strength - no boost 01 : elevated electrical drive strength - low (~4% boost) 10 : elevated electrical drive strength - medium (~ 8% boost) 11 : elevated electrical drive strength - high (~12% boost)

Note: Boost could result in non-USB compliant parameters. Therefore, a value of 00 should be implemented unless specific implementation issues require additional signal boosting to correct for degraded USB signaling levels.

5.1.29 REGISTER FAH: PORT SWAP

Bit Number	Bit Name	Description
7:0	PRTSP	Port Swap: swaps the upstream USBDP/USBDM pins (USBDP_UP and USBDM_UP) and the downstream USBDP/USBDM pins (USBDP_DN[x:1] and USBDM_DN[x:1]) for ease of board routing to devices and connectors. 0 : USB D+ functionality is associated with the DP pin and D- functionality is associated with the DM pin. 1 : USB D+ functionality is associated with the DM pin and D- functionality is associated with the DP pin. Bit 7 : rsvd Bit 6 : rsvd Bit 5 : rsvd Bit 4 : controls port 4 Bit 3 : controls port 3 Bit 2 : controls port 2 Bit 1 : controls port 1 Bit 0 : when set to 1, the upstream port DP/DM is swapped.

5.1.30 REGISTER FBH: PORTMAP 12

Bit Number	Bit Name	Description																										
7:0	PRTR12	PortMap Register for Ports 1 and 2: When a hub is enumerated by a USB host controller, the hub is only permitted to report how many ports it has; the hub is not permitted to select a numerical range or assignment. The host controller will number the downstream ports of the hub starting with the number 1, up to the number of ports that the hub reports having. The host's port number is called the Logical Port Number and the physical port on the hub is the Physical Port Number. When mapping mode is enabled (see PRTMAP_EN, Section 5.1.9 on page 20) the hub's downstream port numbers can be mapped to different logical port numbers (assigned by the host). Note: Contiguous logical port numbers must be implemented, starting from number 1 up to the maximum number of enabled ports. This ensures that the hub's ports are numbered in accordance with the way a host will communicate with the ports. <table border="1"> <tr> <td rowspan="6">Bit [7:4]</td><td>0000</td><td>Physical port 2 is disabled</td></tr> <tr> <td>0001</td><td>Physical port 2 is mapped to logical port 1</td></tr> <tr> <td>0010</td><td>Physical port 2 is mapped to logical port 2</td></tr> <tr> <td>0011</td><td>Physical port 2 is mapped to logical port 3</td></tr> <tr> <td>0100</td><td>Physical port 2 is mapped to logical port 4</td></tr> <tr> <td>1000 to 1111</td><td>rsvd, will default to 0000 value</td></tr> <tr> <td rowspan="6">Bit [3:0]</td><td>0000</td><td>Physical port 1 is disabled</td></tr> <tr> <td>0001</td><td>Physical port 1 is mapped to logical port 1</td></tr> <tr> <td>0010</td><td>Physical port 1 is mapped to logical port 2</td></tr> <tr> <td>0011</td><td>Physical port 1 is mapped to logical port 3</td></tr> <tr> <td>0100</td><td>Physical port 1 is mapped to logical port 4</td></tr> <tr> <td>1000 to 1111</td><td>rsvd, will default to 0000 value</td></tr> </table>	Bit [7:4]	0000	Physical port 2 is disabled	0001	Physical port 2 is mapped to logical port 1	0010	Physical port 2 is mapped to logical port 2	0011	Physical port 2 is mapped to logical port 3	0100	Physical port 2 is mapped to logical port 4	1000 to 1111	rsvd, will default to 0000 value	Bit [3:0]	0000	Physical port 1 is disabled	0001	Physical port 1 is mapped to logical port 1	0010	Physical port 1 is mapped to logical port 2	0011	Physical port 1 is mapped to logical port 3	0100	Physical port 1 is mapped to logical port 4	1000 to 1111	rsvd, will default to 0000 value
Bit [7:4]	0000	Physical port 2 is disabled																										
	0001	Physical port 2 is mapped to logical port 1																										
	0010	Physical port 2 is mapped to logical port 2																										
	0011	Physical port 2 is mapped to logical port 3																										
	0100	Physical port 2 is mapped to logical port 4																										
	1000 to 1111	rsvd, will default to 0000 value																										
Bit [3:0]	0000	Physical port 1 is disabled																										
	0001	Physical port 1 is mapped to logical port 1																										
	0010	Physical port 1 is mapped to logical port 2																										
	0011	Physical port 1 is mapped to logical port 3																										
	0100	Physical port 1 is mapped to logical port 4																										
	1000 to 1111	rsvd, will default to 0000 value																										

5.1.31 REGISTER FCH: PORTMAP 34

Bit Number	Bit Name	Description																																				
7:0	PRTR34	PortMap Register for Ports 3 and 4: When a hub is enumerated by a USB host controller, the hub is only permitted to report how many ports it has; the hub is not permitted to select a numerical range or assignment. The host controller will number the downstream ports of the hub starting with the number 1, up to the number of ports that the hub reports having. The host's port number is called the Logical Port Number and the physical port on the hub is the Physical Port Number. When mapping mode is enabled (see PRTMAP_EN, Section 5.1.9 on page 20) the hub's downstream port numbers can be mapped to different logical port numbers (assigned by the host). Note: Contiguous logical port numbers must be implemented, starting from number 1 up to the maximum number of enabled ports. This ensures that the hub's ports are numbered in accordance with the way a host will communicate with the ports. <table> <tr> <td>Bit [7:4]</td><td>0000</td><td>Physical port 4 is disabled</td></tr> <tr> <td></td><td>0001</td><td>Physical port 4 is mapped to logical port 1</td></tr> <tr> <td></td><td>0010</td><td>Physical port 4 is mapped to logical port 2</td></tr> <tr> <td></td><td>0011</td><td>Physical port 4 is mapped to logical port 3</td></tr> <tr> <td></td><td>0100</td><td>Physical port 4 is mapped to logical port 4</td></tr> <tr> <td></td><td>1000 to 1111</td><td>rsvd, will default to 0000 value</td></tr> <tr> <td>Bit [3:0]</td><td>0000</td><td>Physical port 3 is disabled</td></tr> <tr> <td></td><td>0001</td><td>Physical port 3 is mapped to logical port 1</td></tr> <tr> <td></td><td>0010</td><td>Physical port 3 is mapped to logical port 2</td></tr> <tr> <td></td><td>0011</td><td>Physical port 3 is mapped to logical port 3</td></tr> <tr> <td></td><td>0100</td><td>Physical port 3 is mapped to logical port 4</td></tr> <tr> <td></td><td>1000 to 1111</td><td>rsvd, will default to 0000 value</td></tr> </table>	Bit [7:4]	0000	Physical port 4 is disabled		0001	Physical port 4 is mapped to logical port 1		0010	Physical port 4 is mapped to logical port 2		0011	Physical port 4 is mapped to logical port 3		0100	Physical port 4 is mapped to logical port 4		1000 to 1111	rsvd, will default to 0000 value	Bit [3:0]	0000	Physical port 3 is disabled		0001	Physical port 3 is mapped to logical port 1		0010	Physical port 3 is mapped to logical port 2		0011	Physical port 3 is mapped to logical port 3		0100	Physical port 3 is mapped to logical port 4		1000 to 1111	rsvd, will default to 0000 value
Bit [7:4]	0000	Physical port 4 is disabled																																				
	0001	Physical port 4 is mapped to logical port 1																																				
	0010	Physical port 4 is mapped to logical port 2																																				
	0011	Physical port 4 is mapped to logical port 3																																				
	0100	Physical port 4 is mapped to logical port 4																																				
	1000 to 1111	rsvd, will default to 0000 value																																				
Bit [3:0]	0000	Physical port 3 is disabled																																				
	0001	Physical port 3 is mapped to logical port 1																																				
	0010	Physical port 3 is mapped to logical port 2																																				
	0011	Physical port 3 is mapped to logical port 3																																				
	0100	Physical port 3 is mapped to logical port 4																																				
	1000 to 1111	rsvd, will default to 0000 value																																				

5.1.32 REGISTER FFH: STATUS/COMMAND

Bit Number	Bit Name	Description
7:3	rsvd	
2	INTF_PW_DN	SMBus Interface Power Down: 0 : interface is active 1 : interface power down after ACK has completed
1	RESET	Reset the SMBus interface and internal memory back to RESET_N assertion default settings. 0 : normal run/idle state 1 : force a reset of registers to their default state
0	USB_ATTACH	USB Attach (and write protect) 0 : SMBus slave interface is active 1 : the hub will signal a USB attach event to an upstream device, and the internal memory (address range 0x00-0xFE) is write-protected to prevent unintentional data corruption.

5.2 I²C EEPROM

The Microchip hub can be configured via a 2-wire (I²C) EEPROM (256x8). See [Table 5-1](#) for details on enabling the I²C EEPROM interface. The I²C EEPROM interface implements a subset of the *I²C Master Specification* (refer to the Philips Semiconductor Standard I²C-Bus Specification I²C protocol for details). The hub's interface is designed to attach to a single dedicated I²C EEPROM which conforms to the Standard-mode I²C specification (100 kbit/s transfer rate and 7-bit addressing) for protocol and electrical compatibility. The I²C EEPROM shares the same pins as the SMBus interface, therefore the SMBus interface is not available when the I²C EEPROM interface has been enabled (and vice versa).

The hub acts as the master and generates the serial clock SCL, controls the bus access (determines which device acts as the transmitter and which device acts as the receiver), and generates the START and STOP conditions. The hub will read the external EEPROM for configuration data and then attach to the upstream USB host.

Note: If no external EEPROM is present, the hub will write 0 to all configuration registers.

The hub does not have the capacity to write to the external EEPROM. The hub only has the capability to read from an external EEPROM. The external EEPROM will be read (even if it is blank), and the hub will be configured with the values that are read. Any values read for unsupported registers will not be retained (i.e., they will remain as the default values). Reserved registers should be set to 0 unless otherwise specified. EEPROM reset values are 0x00. Contents read from unavailable registers should be ignored.

5.2.1 I²C SLAVE ADDRESS

The 7-bit slave address is 1010000b.

Note: 10-bit addressing is not supported.

5.2.2 PROTOCOL IMPLEMENTATION

The hub will only access an EEPROM using the sequential read protocol as outlined in Chapter 8 of *MicroChip 24AA02/24LC02B* [4].

5.2.3 PULL-UP RESISTOR

The circuit board designer is required to place external pull-up resistors (10 kΩ recommended) on the **SDA/SMBDATA** and **SCL/SMBCLK/CFG_SEL[0]** lines (per *SMBus 1.0 Specification* [3], and EEPROM manufacturer guidelines) to **VDD33** in order to assure proper operation.

5.2.4 IN-CIRCUIT EEPROM PROGRAMMING

The EEPROM can be programmed via automatic test equipment (ATE) by pulling **RESET_N** low (which tri-states the hub's EEPROM interface and allows an external source to program the EEPROM).

Note: The Hub does not have the capacity to write, or “Program,” an external EEPROM. The Hub only has the capability to read external EEPROMs. The external EEPROM will be read (even if it is blank or non-populated), and the Hub will be “configured” with the values that are read.

5.3 SMBus

The Microchip hub can be configured by an external processor via an SMBus interface (see [Table 5-1](#) for details on enabling the SMBus interface). The SMBus interface shares the same pins as the EEPROM interface, and therefore the hub no longer supports the I²C EEPROM interface when the SMBus interface has been enabled. The Microchip hub waits indefinitely for the SMBus code load to complete and only appears as a newly connected device on USB after the code load is complete.

The hub's SMBus acts as a slave-only SMBus device. The implementation only supports block write ([Section 5.3.2.1](#)) and block read ([Section 5.3.2.2](#)) protocols, where the available registers are outlined in [Section 5.1 on page 16](#). Reference the *System Management Bus Specification* [3] for additional information.

5.3.1 SMBUS SLAVE ADDRESS

The 7-bit slave address is 0101100b. The hub will not respond to the general call address of 0000000b.

5.3.2 PROTOCOL IMPLEMENTATION

Typical block write and block read protocols are shown in figures [5-1](#) and [5-2](#). Register accesses are performed using 7-bit slave addressing, an 8-bit register address field, and an 8-bit data field. The shading shown in the figures during a read or write indicates the hub is driving data on the **SMBDATA** line; otherwise, host data is on the **SDA/SMBDATA** line.

The SMBus slave address assigned to the hub (0101100b) allows it to be identified on the SMBus. The register address field is the internal address of the register to be accessed. The register data field is the data that the host is attempting to write to the register or the contents of the register that the host is attempting to read.

Note: Data bytes are transferred MSB first.

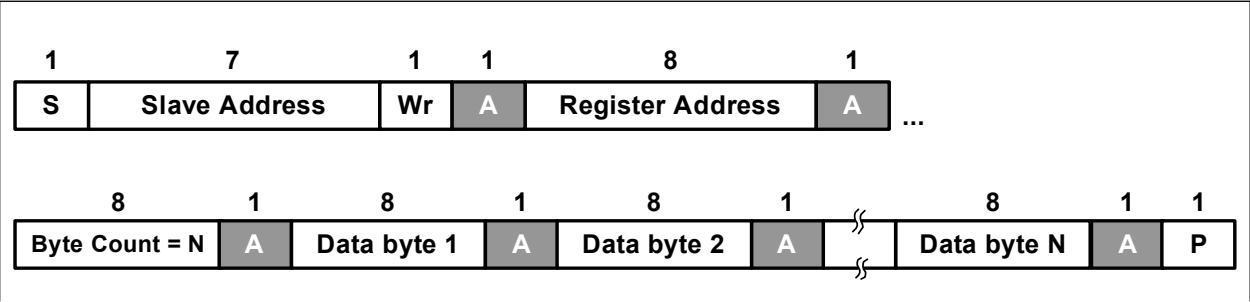
5.3.2.1 Block Write/Read

The block write begins with a slave address and a write condition. After the command code, the host issues a byte count which describes how many more bytes will follow in the message. If a slave had 20 bytes to send, the first byte would be the number 20 (14h), followed by the 20 bytes of data. The byte count may not be zero. A block write or read allows a transfer maximum of 32 data bytes.

Note: For the following SMBus tables:

Denotes Master-to-Slave Denotes Slave-to-Master

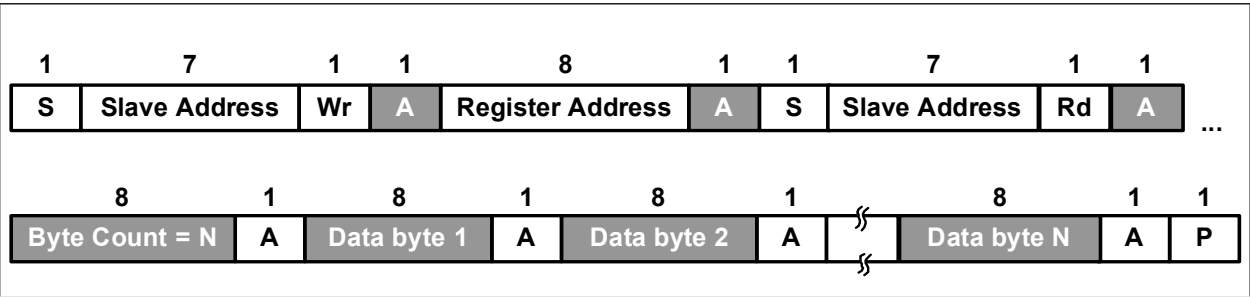
FIGURE 5-1: BLOCK WRITE



5.3.2.2 Block Read

A block read differs from a block write in that the repeated start condition exists to satisfy the I²C specification's requirement for a change in the transfer direction.

FIGURE 5-2: BLOCK READ



5.3.2.3 Invalid Protocol Response Behavior

Note that any attempt to update registers with an invalid protocol will not be updated. The only valid protocols are write block and read block (described above), where the hub only responds to the 7-bit hardware selected slave address (0101100b). Also, the only valid registers for the hub are outlined in [Section 5.1 on page 16](#). Attempts to access any other registers will return no response.

5.3.3 SLAVE DEVICE TIMEOUT

Devices in a transfer can abort the transfer in progress and release the bus when any single clock low interval exceeds 25 ms ($T_{\text{TIMEOUT, MIN}}$). The master must detect this condition and generate a stop condition within or after the transfer of the interrupted data byte. Slave devices must reset their communication and be able to receive a new START condition no later than 35 ms ($T_{\text{TIMEOUT, MAX}}$).

Note: Some simple devices do not contain a clock low drive circuit; this simple kind of device typically resets its communications port after a start or stop condition. The slave device timeout must be implemented.

5.3.4 STRETCHING THE SCLK SIGNAL

The hub supports stretching of the **SCLK** by other devices on the SMBus. However, the hub does not stretch the **SCLK**.

5.3.5 SMBUS TIMING

The SMBus slave interface complies with the *SMBus Specification Revision 1.0* [3]. See Section 2.1, *AC Specifications* on page 3 for more information.

5.3.6 BUS RESET SEQUENCE

The SMBus slave interface resets and returns to the idle state upon a **START** condition followed immediately by a **STOP** condition.

5.3.7 SMBUS ALERT RESPONSE ADDRESS

The **SMBALERT#** signal is not supported by the hub.

5.4 Default Configuration

To put the Microchip hub in the default configuration, strap **CFG_SEL[1:0]** to 00b. This procedure configures the hub to the internal defaults and enables the strapping options. To place the hub in default configuration with overrides, see [Table 5-1 on page 16](#) for the list of the options.

The internal default values are used for the registers that are not controlled by strapping option pins. Refer to [Section 5.1 on page 16](#) for the internal default values that are loaded when this option is selected. For a list of strapping option pins, see [Section 5.0 on page 16](#), and to configure the strapping pins, see [Section 3.3.1 on page 11](#).

5.5 Reset

The hub experiences the following two resets:

- Hardware reset via the **RESET_N** pin
- USB bus reset

5.5.1 EXTERNAL HARDWARE RESET_N

A valid hardware reset is defined as assertion of **RESET_N** for a minimum of 1 μ s after all power supplies are within operating range. While reset is asserted, the hub (and its associated external circuitry) consumes less than 500 μ A of current from the upstream USB power source.

Assertion of **RESET_N** causes the following:

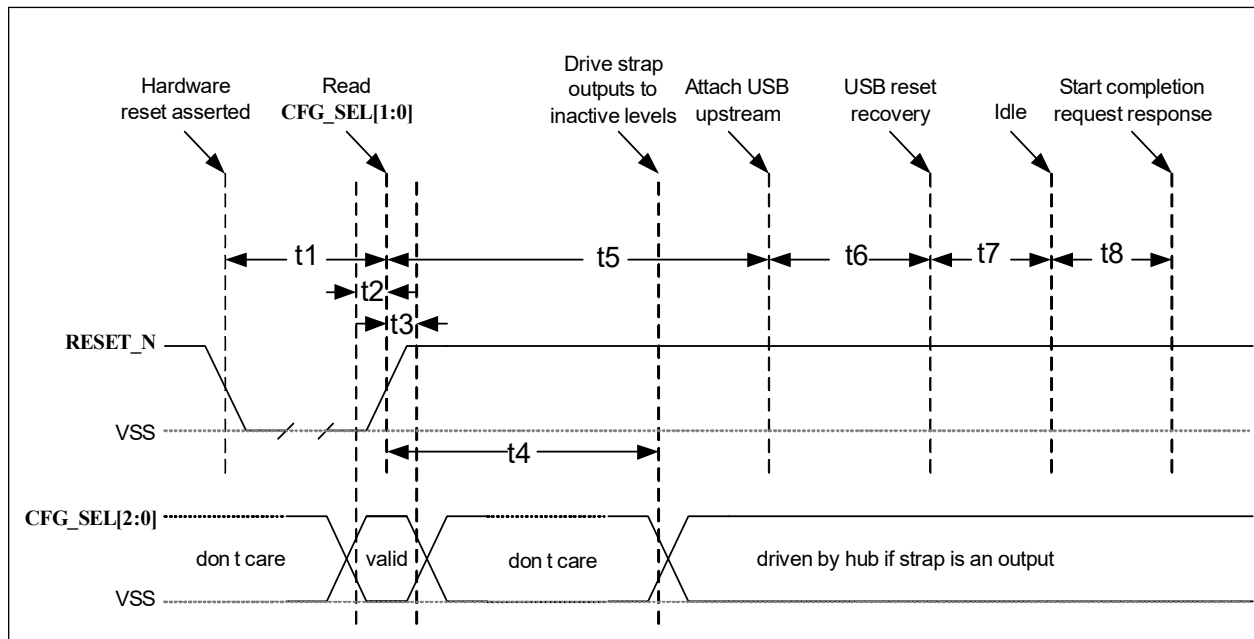
1. All downstream ports are disabled, and **PRTPWR[x:1]** to downstream devices is removed (unless **BC_EN[x:1]** is enabled).
2. The PHYs are disabled, and the differential pairs will be in a high-impedance state.
3. All transactions immediately terminate; no states are saved.
4. All internal registers return to the default state (in most cases, 00h).
5. The external crystal oscillator is halted.
6. The PLL is halted.

The hub is operational 500 μ s after **RESET_N** is negated. Once operational, the hub will do one of the following, depending on configuration:

- Read the strapping pins (default configuration with strapping options enabled)
- Read configuration information from the external I²C EEPROM
- Wait for configuration over SMBus.

5.5.1.1 RESET_N for Strapping Option Configuration

FIGURE 5-3: RESET_N TIMING FOR DEFAULT CONFIGURATION



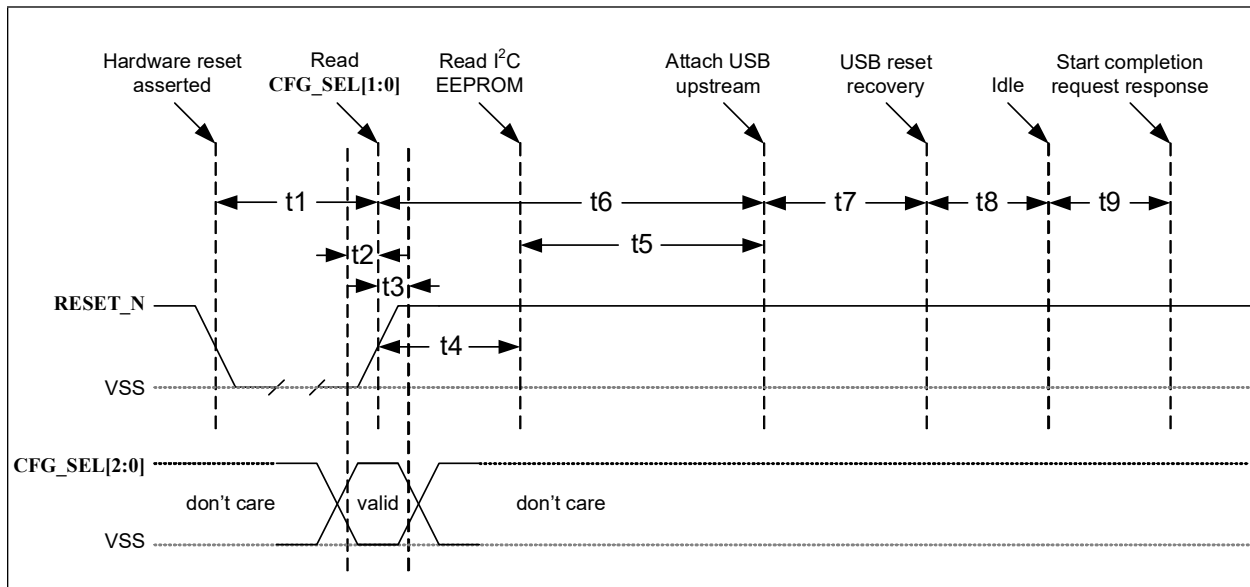
Name	Description	MIN	TYP	MAX	Units
t1	RESET_N asserted	1			μ s
t2	CFG_SEL[1:0] setup time	16.7			ns
t3	CFG_SEL[1:0] hold time	16.7		1400	ns
t4	Hub outputs driven to inactive logic states		1.5	2	μ s
t5	USB attach (see notes)			100	ms
t6	Host acknowledges attach and signals USB reset	100			ms
t7	USB idle		undefined		ms
t8	Completion time for requests (with or without data stage)			5	msec

Note:

- When in bus-powered mode, the hub and its associated circuitry must not consume more than 100 mA from the upstream USB power source during t1+t5.
- All power supplies must have reached the operating levels mandated in [Section 6.0, "DC Parameters"](#), prior to (or coincident with) the assertion of RESET_N.

5.5.1.2 RESET_N for EEPROM Configuration

FIGURE 5-4: RESET_N TIMING FOR EEPROM MODE



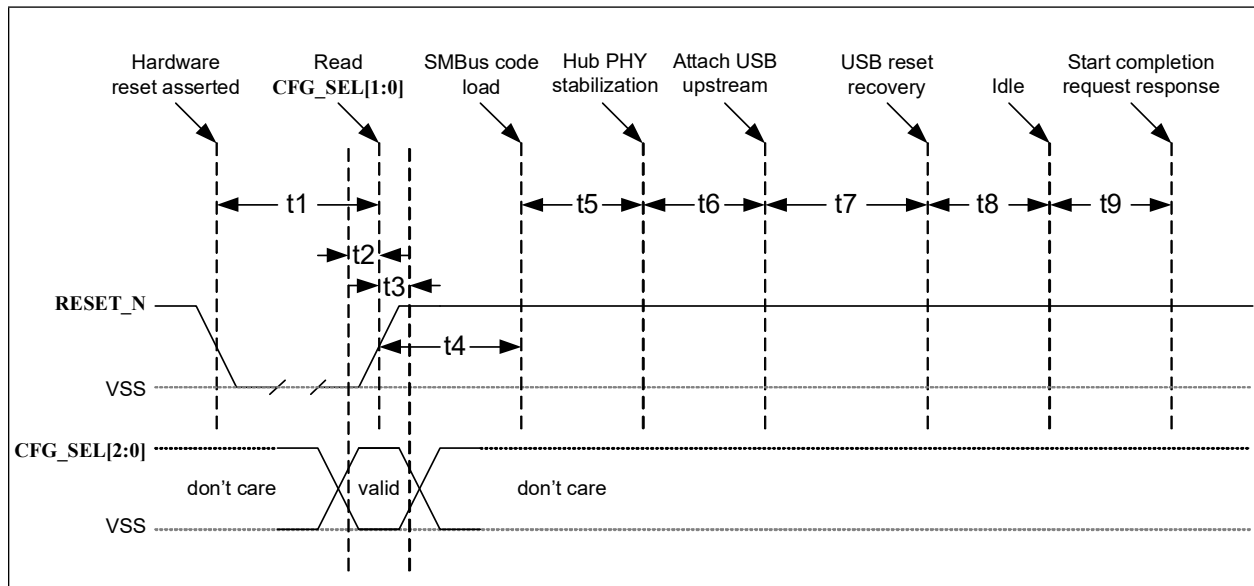
Name	Description	MIN	TYP	MAX	Units
t1	RESET_N asserted	1			μs
t2	CFG_SEL[1:0] setup time	16.7			ns
t3	CFG_SEL[1:0] hold time	16.7		1400	ns
t4	Hub recovery/stabilization			500	μs
t5	EEPROM read (hub configuration)		2.0	99.5	ms
t6	USB attach (see notes)			100	ms
t7	Host acknowledges attach and signals USB reset	100			ms
t8	USB idle		undefined		ms
t9	Completion time for requests (with or without data stage)			5	ms

Note:

- When in bus-powered mode, the hub and its associated circuitry must not consume more than 100 mA from the upstream USB power source during t6+t7+t8+t9.
- All power supplies must have reached the operating levels mandated in [Section 6.0, "DC Parameters"](#), prior to (or coincident with) the assertion of RESET_N.

5.5.1.3 RESET_N for SMBus Slave Configuration

FIGURE 5-5: RESET_N TIMING FOR SMBUS MODE



Name	Description	MIN	TYP	MAX	Units
t1	RESET_N Asserted	1			μs
t2	CFG_SEL[1:0] setup time	16.7			ns
t3	CFG_SEL[1:0] hold time	16.7		1400	ns
t4	Hub recovery/stabilization			500	μs
t5 _{BUS}	SMBus code load (Note 5-1)			99.5	ms
t5 _{SELF}	SMBus Code Load (Note 5-1)			undefined	ms
t6	Hub configuration and USB attach			100	ms
t7	Host acknowledges attach and signals USB reset	100			ms
t8	USB idle		undefined		ms
t9	Completion time for requests (with or without data stage)			5	ms

Note 5-1 For bus-powered configurations, there is a 99.5 ms MAX, and the hub and its associated circuitry must not consume more than 100 mA from the upstream USB power source during t4+t5+t6+t7+t8+t9. For self-powered configurations, t5 MAX is not applicable and the time to load the configuration is determined by the external SMBus host.

Note 5-2 All power supplies must have reached the operating levels mandated in [Section 6.0, "DC Parameters"](#), prior to (or coincident with) the assertion of RESET_N.

5.5.2 USB BUS RESET

In response to the upstream port signaling a reset to the hub, the hub does the following:

1. Sets default internal USB address to 0
2. Sets configuration to: unconfigured
3. Negates **PRTPWR[x:1]** to all downstream ports unless battery charging (**BC_EN[x:1]**) is enabled
4. Clears all TT buffers
5. Moves device from suspended to active (if suspended)
6. Complies with Section 11.10 of the *USB 2.0 Specification* [1] for behavior after completion of the reset sequence. The host then configures the hub and the hub's downstream port devices in accordance with the *USB Specification*.

Note: The hub does not propagate the upstream USB reset to downstream devices.

6.0 DC PARAMETERS

6.1 Maximum Ratings

Parameter	Symbol	MIN	MAX	Units	Comments
Storage Temperature	T _{STOR}	-55	150	°C	
Lead Temperature					Refer to JEDEC Specification J-STD-020D [5]
3.3 V supply voltage	VDD33 PLLFLT CRFLT		4.6	V	Applies to all parts
Voltage on any I/O pin		-0.5	5.5	V	
Voltage on XTALIN		-0.5	4.0	V	
Voltage on XTALOUT		-0.5	2.5	V	

Note:

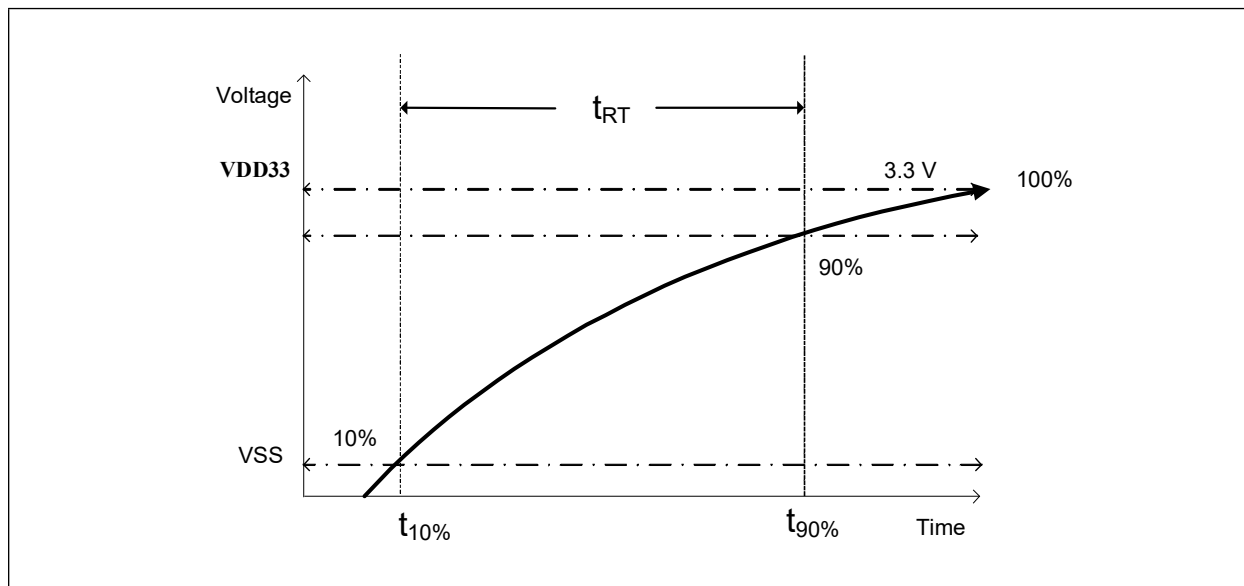
- Stresses above the specified parameters could cause permanent damage to the device. This is a stress rating only. Therefore, functional operation of the device at any condition above those indicated in the operation sections of this specification are not implied.
- When powering this device from laboratory or system power supplies, it is important that the absolute maximum ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. When this possibility exists, it is suggested that a clamp circuit be used.

6.2 Operating Conditions

Parameter	Symbol	MIN	MAX	Units	Comments
Operating Temperature	T _{AE}	Note 6-1	85	°C	Ambient temperature in still air
3.3 V supply voltage	VDD33	3.0	3.6	V	Applies to all parts
3.3 V supply rise time	t _{RT}	0	400	μs	See Figure 6-1 , Note 6-2
Voltage on any I/O pin		-0.3	5.5	V	If any 3.3 V supply voltage drops below 3.0 V, then the MAX becomes: (3.3 V supply voltage) + 0.5
Voltage on XTALIN		-0.3	VDD33	V	

Note 6-1 0°C minimum for extended commercial version, -40°C minimum for industrial version.

FIGURE 6-1: SUPPLY RISE TIME MODEL



Note 6-2 The rise time for the 3.3 V supply can be extended to 100 ms max if RESET_N is actively driven low, typically by another IC, until 1 μ s after all supplies are within operating range.

TABLE 6-1: DC ELECTRICAL CHARACTERISTICS

Parameter	Symbol	MIN	TYP	MAX	Units	Comments
I, IS Type Input Buffer						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0			V	
Input Leakage	I_{IL}	-10		+10	μ A	$V_{IN} = 0$ to VDD33
Hysteresis (IS only)	V_{HYSI}	250		350	mV	
Input Buffer with Pull-Up (IPU)						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0			V	
Low Input Leakage	I_{ILL}	+35		+90	μ A	$V_{IN} = 0$
High Input Leakage	I_{IHL}	-10		+10	μ A	$V_{IN} = \mathbf{VDD33}$
Input Buffer with Pull-Down (IPD)						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0			V	
Low Input Leakage	I_{ILL}	+10		-10	μ A	$V_{IN} = 0$
High Input Leakage	I_{IHL}	-35		-90	μ A	$V_{IN} = \mathbf{VDD33}$
ICLK Input Buffer						
Low Input Level	V_{ILCK}			0.3	V	
High Input Level	V_{IHCK}	0.9			V	
Input Leakage	I_{IL}	-10		+10	μ A	$V_{IN} = 0$ to VDD33

TABLE 6-1: DC ELECTRICAL CHARACTERISTICS (CONTINUED)

Parameter	Symbol	MIN	TYP	MAX	Units	Comments
O12, I/O12 & I/OSD12 Type Buffer						
Low Output Level	V_{OL}			0.4	V	$I_{OL} = 12 \text{ mA @ } V_{DD33} = 3.3 \text{ V}$
High Output Level	V_{OH}	2.4			V	$I_{OH} = -12 \text{ mA @ } V_{DD33} = 3.3 \text{ V}$
Output Leakage	I_{OL}	-10		+10	μA	
Hysteresis (SD pad only)	I_{HYSC}	250		350	mV	$V_{IN} = V_{DD33}$ (See Note:)
IO-U						
SUPPLY CURRENT UNCONFIGURED						
Hi-Speed Host	$I_{CCINTHS}$		45	50	mA	
Full-Speed Host	$I_{CCINITFS}$		35	40	mA	
SUPPLY CURRENT CONFIGURED						
1 Port HS	I_{HCH1}		70	80	mA	Base current of 1 downstream port
Each additional port in HS			base +25 mA	base +25 mA		
1 Port FS	I_{FCC1}		50	60	mA	Base current of 1 downstream port
Each additional port in FS			base +8 mA	base +8 mA		
Supply current suspend	I_{CSBY}		550	1200	μA	All supplies combined
Supply current reset	I_{CRST}		750	1400	μA	All supplies combined

Note 6-3 Output leakage is measured with the current pins in high impedance.

Note 6-4 See *USB 2.0 Specification* [1] for USB DC electrical characteristics.

TABLE 6-2: PIN CAPACITANCE

Parameter	Symbol	Limits			Unit	Test Condition
		MIN	TYP	MAX		
Clock Input Capacitance	C_{XTAL}			6	pF	All pins except USB pins and the pins under the test tied to AC ground (Note 6-5)
Input Capacitance	C_{IN}			6	pF	
Output Capacitance	C_{OUT}			6	pF	

Note 6-5 Capacitance $T_A = 25^\circ\text{C}$; $f_c = 1 \text{ MHz}$; $V_{DD33} = 3.3 \text{ V}$

6.2.1 PACKAGE THERMAL SPECIFICATIONS

Thermal parameters are measured or estimated for devices with the exposed pad soldered to thermal vias in a multi-layer 2S2P PCB per JESD51. Thermal resistance is measured from the die to the ambient air. The values provided are based on the package body, die size, maximum power consumption, 85°C ambient temperature, and 125°C junction temperature of the die.

TABLE 6-3: PACKAGE THERMAL RESISTANCE PARAMETERS

Symbol	USX2064 (°C/W)	Velocity (Meters/s)
Θ_{JA}	40.1	0
	35.0	1
Ψ_{JT}	0.5	0
	0.7	1
Θ_{JC}	6.3	0
	6.3	1

Use the following formulas to calculate the junction temperature:

$$T_J = P \times \Theta_{JA} + T_A$$

$$T_J = P \times \Psi_{JT} + T_T$$

$$T_J = P \times \Theta_{JC} + T_C$$

TABLE 6-4: LEGEND

Symbol	Description
T_J	Junction temperature
P	Power dissipated
Θ_{JA}	Junction-to-ambient-temperature
Θ_{JC}	Junction-to-top-of-package
Ψ_{JT}	Junction-to-bottom-of-case
T_A	Ambient temperature
T_C	Temperature of the bottom of the case
T_T	Temperature of the top of the case

7.0 AC SPECIFICATIONS

7.1 Oscillator/Crystal

Crystal: Parallel resonant, fundamental mode, 24 MHz ± 350 ppm

External Clock: 50% duty cycle $\pm 10\%$, 24/48 MHz ± 350 ppm, jitter < 100 ps rms

FIGURE 7-1: TYPICAL CRYSTAL CIRCUIT

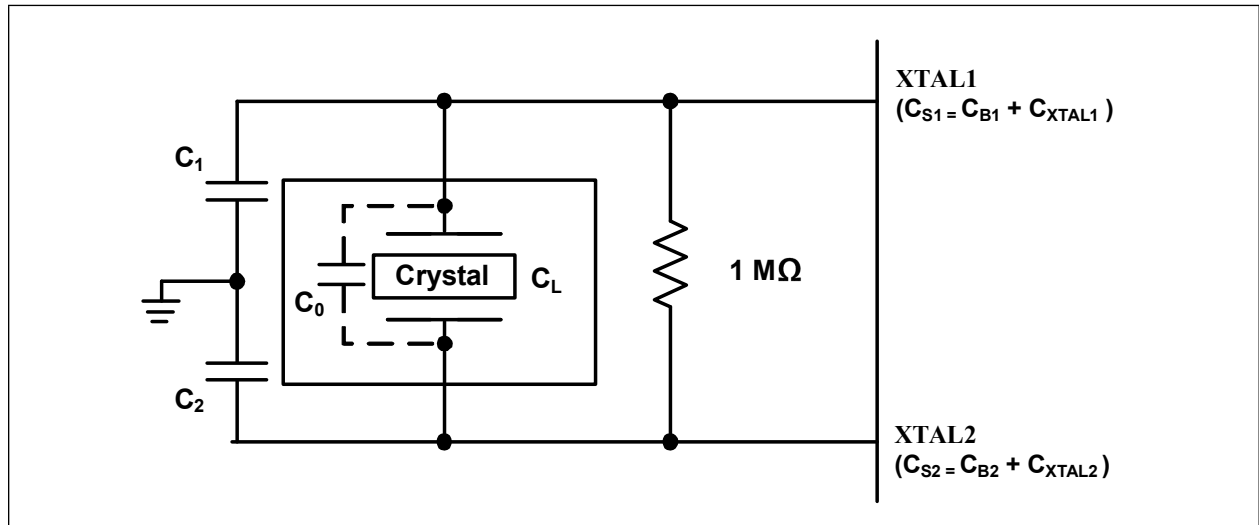


TABLE 7-1: CRYSTAL CIRCUIT LEGEND

Symbol	Description	In Accordance With
C_0	Crystal shunt capacitance	Crystal manufacturer's specification (Note 7-1)
C_L	Crystal load capacitance	
C_B	Total board or trace capacitance	OEM board design
C_S	Stray capacitance	MCHP IC and OEM board design
C_{XTAL}	XTAL pin input capacitance	MCHP IC
C_1 C_2	Load capacitors installed on OEM board	Calculated values based on Figure 7-2 (Note 7-2)

FIGURE 7-2: FORMULA TO FIND THE VALUE OF C_1 AND C_2

$$C_1 = 2 \times (C_L - C_0) - C_{S1}$$

$$C_2 = 2 \times (C_L - C_0) - C_{S2}$$

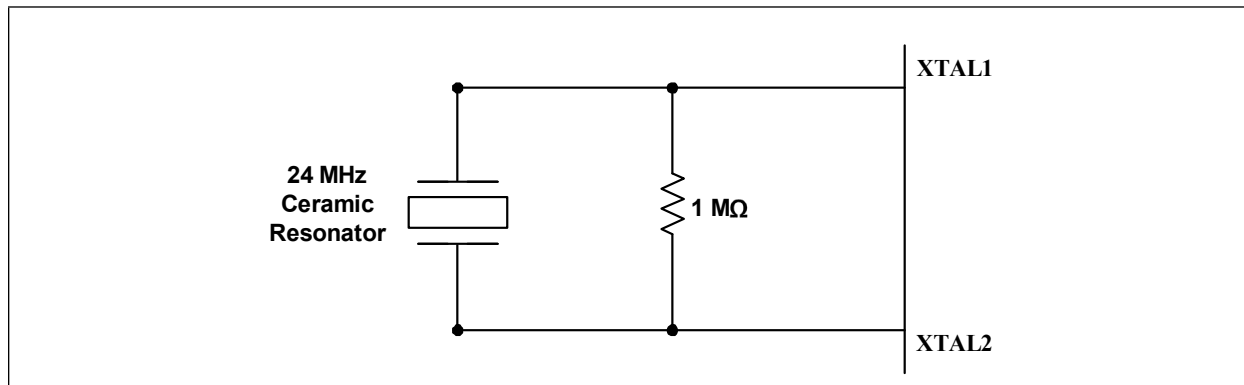
Note 7-1 C_0 is usually included (subtracted by the crystal manufacturer) in the specification for C_L and should be set to 0 for use in the calculation of the capacitance formulas in [Figure 7-2](#). However, the PCB itself may present a parasitic capacitance between XTALIN and XTALOUT. For an accurate calculation of C_1 and C_2 , take the parasitic capacitance between traces XTALIN and XTALOUT into account.

Note 7-2 Each of these capacitance values is typically around 18 pF.

7.2 Ceramic Resonator

24 MHz $\pm$ 350 ppm

FIGURE 7-3: CERAMIC RESONATOR USAGE WITH MCHP IC



7.3 External Clock

50% duty cycle $\pm$ 10%, 24 MHz $\pm$ 350 ppm, jitter < 100 ps rms.

The external clock is recommended to conform to the signaling level designated in the *JESD76-2 Specification* [5] on 1.8 V CMOS Logic. XTALOUT should be treated as a no connect.

7.3.1 SMBUS INTERFACE

The Microchip hub conforms to all voltage, power, and timing characteristics and specifications as set forth in the *SMBus 1.0 Specification* [3] for slave-only devices (except as noted in [Section 5.3, "SMBus," on page 30](#)).

7.3.2 I²C EEPROM

Clock frequency is fixed at 60 kHz $\pm$ 20%.

7.3.3 USB 2.0

The Microchip hub conforms to all voltage, power, and timing characteristics and specifications as set forth in the *USB 2.0 Specification* [1].

8.0 PACKAGE MARKING INFORMATION

The following sub-sections detail the package marking information for the 36-pin SQFN and 36-pin QFN packages. To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

Note: The diagrams shown in this section are examples only. Actual markings may be justified center or left.

8.1 36-Pin SQFN (Preferred)

36-Lead SQFN (6x6x0.9 mm)

Example

Legend:

R	Product revision
nnn	Internal code
e3	Pb-free JEDEC® designator for Matte Tin (Sn)
V	Plant of assembly
COO	Country of origin
YY	Year code (last two digits of calendar year)
WW	Week code (week of January 1 is week '01')
NNN	Alphanumeric traceability code

Note:

In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

* Standard device marking consists of Microchip part number, year code, week code and traceability code. For device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

USX2064

8.2 36-Pin QFN (Legacy) (Extended Commercial Temp.)

36-Lead QFN (6x6x0.9 mm)



Example



Legend:

R	Product revision
YY	Year code (last two digits of calendar year)
WW	Week code (week of January 1 is week '01')
A2P10	Internal code
NNN	Alphanumeric traceability code
A	Fixed character
V	Plant of assembly
COO	Country of origin
e3	Pb-free JEDEC [®] designator for Matte Tin (Sn)

Note:

In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

* Standard device marking consists of Microchip part number, year code, week code and traceability code. For device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

8.3 36-Pin QFN (Legacy) (Industrial Temp.)

36-Lead QFN (6x6x0.9 mm)



PIN 1

Example



PIN 1

Legend:

R	Product revision
YY	Year code (last two digits of calendar year)
WW	Week code (week of January 1 is week '01')
A2P10	Internal code
NNN	Alphanumeric traceability code
A	Fixed character
V	Plant of assembly
COO	Country of origin
e3	Pb-free JEDEC® designator for Matte Tin (Sn)

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

* Standard device marking consists of Microchip part number, year code, week code and traceability code. For device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

DSCORP-060001

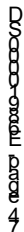
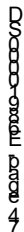
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APPENDIX A: ACRONYMS

I²C:	Inter-Integrated Circuit
OCS:	Over-Current Sense
PCB:	Printed Circuit Board
PHY:	Physical Layer
PLL:	Phase-Locked Loop
QFN:	Quad Flat No Leads
RoHS:	Restriction of Hazardous Substances Directive
SCL:	Serial Clock
SIE:	Serial Interface Engine
SMBus:	System Management Bus
TT:	Transaction Translator

APPENDIX B: REFERENCES

1. Universal Serial Bus Specification, Version 2.0, April 27, 2000 (12/7/2000 and 5/28/2002 Errata)
USB Implementers Forum, Inc. <http://www.usb.org>
2. I²C-Bus Specification Version 1.1
NXP (formerly a division of Philips). <http://www.nxp.com>
3. System Management Bus Specification, version 1.0
SMBus. <http://smbus.org/specs/>
4. Microchip 24AA02/24LC02B (Revision C)
Microchip Technology Inc. <http://www.microchip.com/>
5. JEDEC Specifications: JESD76-2 (June 2001) and J-STD-020D.1 (March 2008)
JEDEC Global Standards for the Microelectronics Industry. <http://www.jedec.org/standards-documents>

APPENDIX C: DATA SHEET REVISION HISTORY

TABLE C-1: REVISION HISTORY

Revision	Section/Figure/Entry	Correction
DS00001986E (07-05-23)	Section 5.2, I2C EEPROM	Updated the URL in the second note from “www.smsc.com” to “www.microchip.com”.
	Section 8.0, Package Marking Information	The following note has been added: “The diagrams shown in this section are examples only. Actual markings may be justified center or left.”
DS00001986D (12-10-20)	Section 6.2, Operating Conditions	Updated table and added note to include both extended commercial and industrial temperature range information.
	Section 8.3, 36-Pin QFN (Legacy) (Industrial Temp.)	Added new sub-section to detail package top marking info for the industrial temperature version.
	Product Identification System	Updated ordering code information to add industrial option.
DS00001986C (06-24-19)	Figure 3-1	Updated pin 6.
DS00001986B (08-17-18)	Figure 3-1	Corrected pin 36 name to VDDA33.
	Table 3-1	Corrected pin 5, 10, 29, and 36 name to VDDA33.
	Table 3-2	Updated capacitor value information in CRTFILT and PLLFILT pin descriptions. Added VDDA33 pin description to table.
	Section 5.2.1, I2C Slave Address	Corrected I ² C slave address to 1010000b.
	Section 6.2, Operating Conditions	Added Note 6-2 under Figure 6-1: “The rise time for the 3.3 V supply can be extended to 100 ms max if RESET_N is actively driven low, typically by another IC, until 1 μs after all supplies are within operating range.”
	Product Identification System	Clarified preferred and legacy ordering codes.
DS00001986A (08-18-15)	Document Release	

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- Technical Support

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Technical support is available through the web site at: <http://www.microchip.com/support>

USX2064

PRODUCT IDENTIFICATION SYSTEM

The USX2064 is available in a 36-pin SQFN (preferred) and 36-pin QFN (legacy) package. For new designs, the 36-pin SQFN is recommended. To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

36-pin SQFN (Preferred)

PART NO. Device [X]⁽¹⁾ Tape and Reel Option - [X] Temperature Range / XX Package	Example: a) USX2064T/M2 (Preferred) 4-Port USB hub, Tape & reel, Commercial temperature, 36-pin SQFN 6 x 6mm package size Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option. Reel size is 3,000.
Device: USX2064 = 4-Port USB 2.0 Hub Tape and Reel Option: Blank = Standard packaging (tray) T = Tape and Reel ⁽¹⁾ Temperature Range: Blank = 0°C to +85°C Commercial Package: M2 = 36-pin SQFN (Preferred)	

36-pin QFN (Legacy)

PART NO. Device [X] Temperature Range - XXXX Package - [X]⁽¹⁾ Tape and Reel Option	Example: a) USX2064-AEZG-TR (Legacy) 4-Port USB hub, Tape & reel, Commercial temperature, 36-pin QFN 6 x 6mm package size b) USX2064I-AEZG-TR (Legacy) 4-Port USB hub, Tape & reel, Industrial temperature, 36-pin QFN 6 x 6mm package size Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option. Reel size is 3,000.
Device: USX2064 = 4-Port USB 2.0 Hub Temperature Range: Blank = 0°C to +85°C Commercial I = -40°C to +85°C Industrial Package: AEZG = 36-pin QFN (Legacy) Tape and Reel Option: Blank = Standard packaging (tray) TR = Tape and Reel ⁽¹⁾	

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