

Introduction

This document provides a hardware design checklist for the Microchip PSE systems based on Microchip's PD77010 PSE Controller and PD7771xTx-family PoE Managers. Follow this checklist when utilizing the devices in a new design. The [Hardware Checklist Summary](#) section provides a summary of these items.

For simplicity, the term PD7771xTx is used throughout this document to refer collectively to the PD77718T4 , PD77718T3, and PD77714T4 devices, except where a specific feature or requirement applies to only one of these variants.

For more information, refer to the following sections:

- [General Considerations](#)
- [Grounding](#)
- [Power Supply](#)
- [Isolation](#)
- [Communication and Control Interface](#)
- [Port Configurations](#)
- [Surge Protection](#)

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1. General Considerations

The following sections describe the general check list.

1.1. Required References

The PD7771xTx implementor should have the following documents on hand:

- [8-Port and 4-Port PoE PSE Manager PD77718T4, PD77718T3 and PD77714T4 PoE PSE Manager Data Sheet](#)
- [PD77010 PoE PSE Controller Data Sheet](#)
- [AN5347-Designing an IEEE 802.3bt PoE System with PD77718T4, PD77718T3 and PD77714T4 Application Note](#)
- *AN4813- Surge Protection for Systems Based on PD777xx PSE PoE Manager Application Note (contact Microchip Representative)*

1.2. Pin Check

- Check the pinout of the part against the data sheet.
- Ensure that all pins match the data sheet and are configured as inputs, outputs, or bidirectional for error checking.
- Customer may use one of the Microchip Evaluation board reference design files.

Figure 1-1. Pin Diagram-PD7771xTx

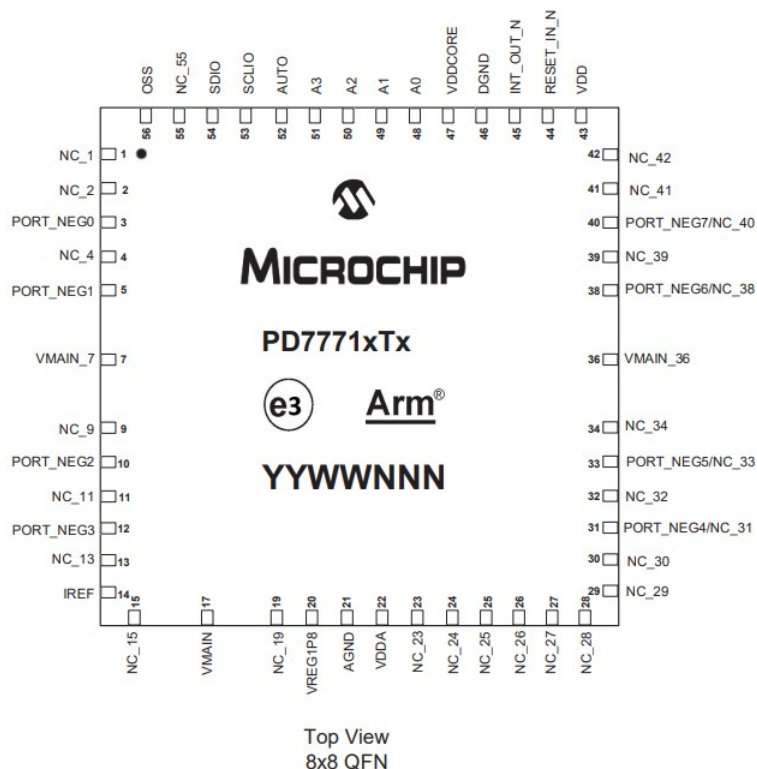
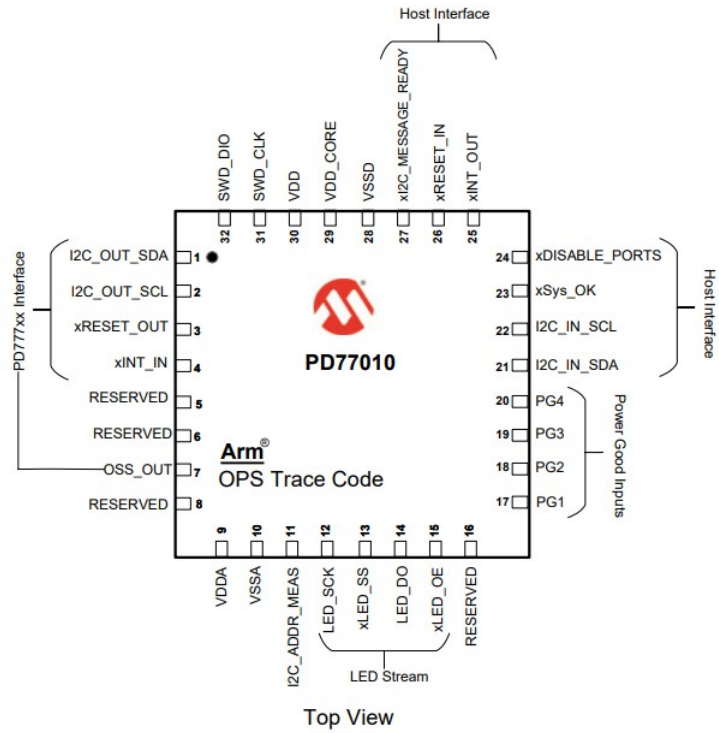


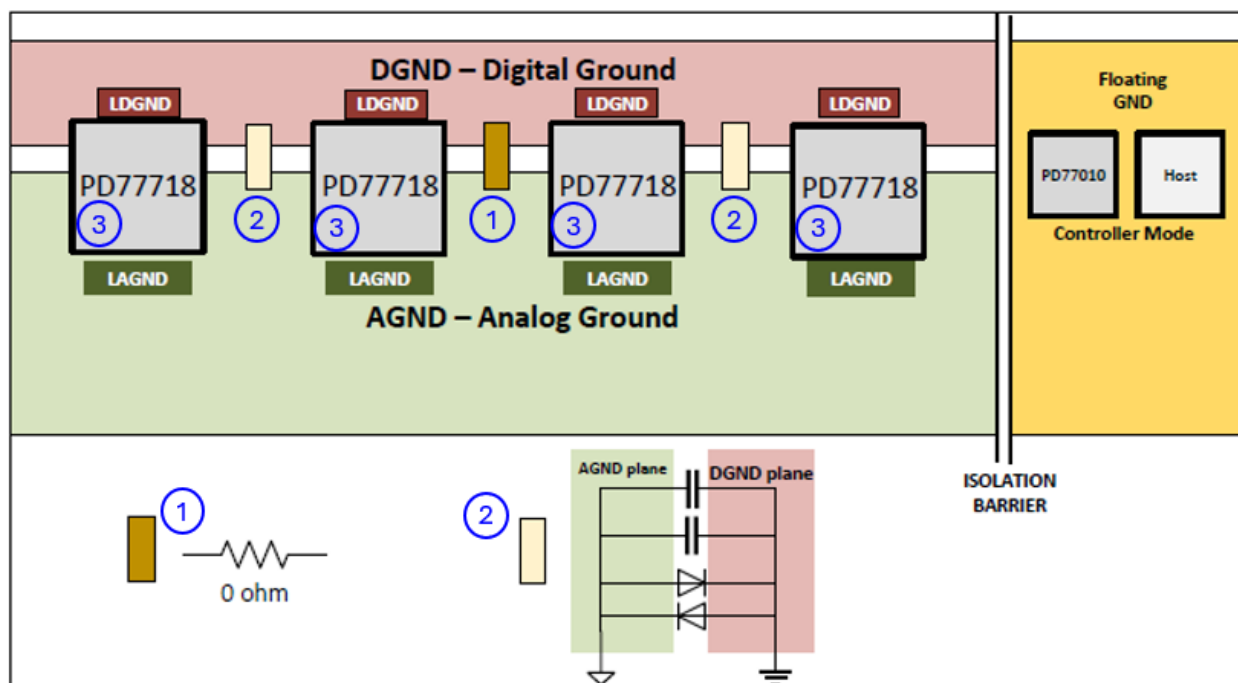
Figure 1-2. Pin Diagram-PD77010



2. Grounding

Multiple ground domains are implemented within the system to support high-current PoE operation while minimizing noise coupling and ensuring isolation compliance. These include PoE domain analog ground (AGND), local analog ground (LAGND), PoE domain digital ground (DGND), local digital ground (LDGND), chassis ground, and a host-domain floating ground.

Figure 2-1. Ground Connections



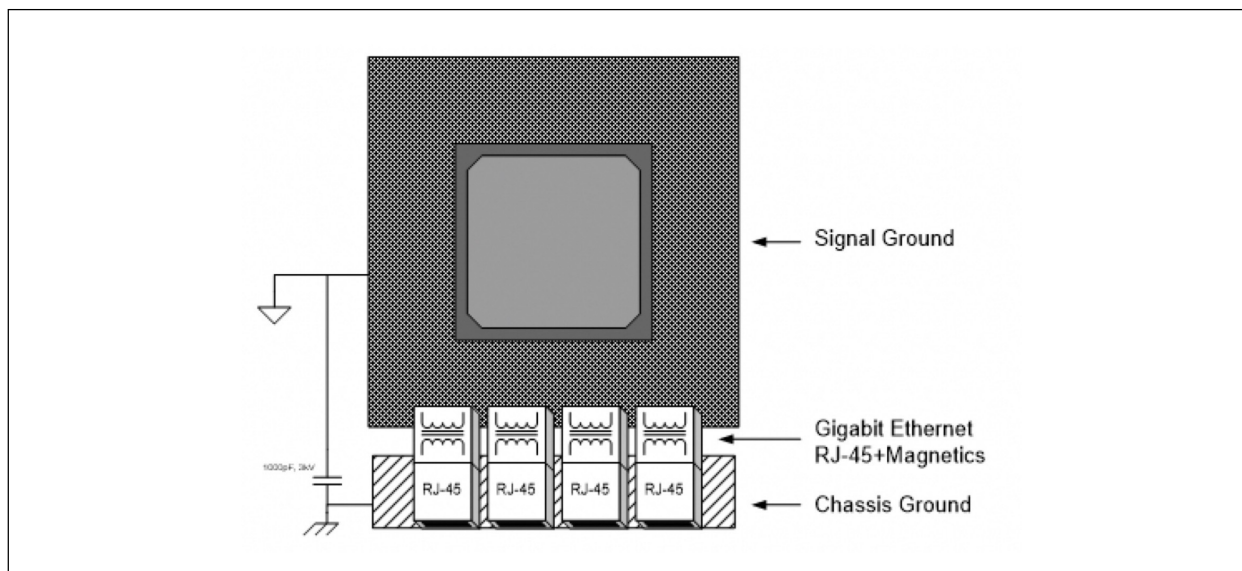
1. There is a short by a 0-ohm resistor/ Trace in a single point in the middle of the board (Marked as 1 in the pic), which connects AGND to DGND planes
 2. In a board with above 4-5 ICs, assemble two capacitors + two protection diodes in both edges of the board (Marked as 2 in the pic), For high-speed transients, between AGND to DGND planes.
 3. Near each IC, close to Iref pin, assemble two capacitors only (Marked as 3 in the pic), which connects LAGND to DGND. D1 & D2 are not required.
- AGND (PoE Analog Ground): AGND represents the negative rail of the PoE input supply and serves as the primary high-current return path for the PoE power stage. The exposed thermal pad (EPAD) of each PD7771xTx device must be directly connected to AGND to ensure proper electrical reference and thermal dissipation. Ensure AGND has sufficient thermal mass for adequate thermal response. Connect the PD7771xTx EPAD to AGND through thermal vias. Use the footprint recommended in the PD7771xTx and PD77010 data sheet.
 - LAGND (Local Analog Ground): LAGND is a quiet, local analog ground intended to provide a low-noise return for sensitive analog circuits within each PD7771xTx device. Decoupling capacitors associated with IREF, VMAIN, and VDDA must reference LAGND. To prevent ground loops, LAGND must connect to AGND at a single point located near the device EPAD. In addition, LAGND must be coupled to DGND through a capacitive network (470 nF in parallel with 1 nF), with optional back-to-back diodes where additional transient control is required.

- **DGND (PoE Digital Ground):** DGND is used as the reference for all PD7771xTx digital signals. All decoupling capacitors connected to the VDD and VDDCORE pins must return to DGND. Care must be taken to prevent high-current PoE return paths from flowing through DGND regions.
- **LDGND (Local Digital Ground):** LDGND provides a local return for VREG1P8 decoupling capacitors. LDGND must be connected to DGND at a single, controlled point to maintain a stable digital reference while limiting noise injection. Although AGND, LAGND, DGND, and LDGND are electrically common, they must remain physically partitioned on the PCB and tied together only at defined single-point connections. This approach reduces noise coupling between high-current PoE paths and sensitive analog or digital circuitry.
The AGND connection to the power supply must be capable of carrying the full PoE return current without excessive voltage drop or thermal stress.
- **Host Domain Floating Ground:** The PD77010 controller operates relative to the host-domain ground, which must remain electrically isolated from all PoE ground domains through the isolation barrier.
- **Chassis Ground:** Chassis ground is tied to the mechanical chassis of the switch and must remain isolated from PoE circuitry by at least 1500 VRMS. Surge and ESD currents must be directed to chassis ground without coupling into PoE or logic ground domains.

Grounding Checklist

- Ground Domain Definition
 - ☐ Separate ground domains implemented: AGND, LAGND, DGND, LDGND, chassis ground, and host-domain floating ground
 - ☐ AGND and DGND ground domains physically partitioned on PCB with controlled single-point connections
- AGND (PoE Analog Ground)
 - ☐ AGND used as the negative PoE input return
 - ☐ AGND return path sized to carry full PoE load current without excessive voltage drop
 - ☐ PD7771xTx device EPAD connected directly to AGND
- LAGND (Local Analog Ground)
 - ☐ IREF, VMAIN, and VDDA decoupling capacitors referenced to LAGND
 - ☐ LAGND connected to AGND at a single point near the PD7771xTx EPAD
 - ☐ LAGND coupled to DGND using 470 nF + 1 nF capacitors
 - ☐ Optional back-to-back diodes evaluated for transient control away from the AGND-DGND single point connection
- DGND (PoE Digital Ground)
 - ☐ PD7771xTx digital pins referenced to DGND
 - ☐ VDD and VDDCORE decoupling capacitors returned to DGND
 - High-current PoE return paths prevented from flowing through DGND regions
- LDGND (Local Digital Ground)
 - ☐ VREG1P8 decoupling capacitors referenced to LDGND
 - ☐ LDGND connected to DGND at a single controlled point
- Host Domain Floating Ground
 - ☐ PD77010 host-domain ground isolated from PoE ground domains
 - ☐ Digital isolation implemented across host-PoE boundary
- Chassis Ground
 - ☐ Chassis ground isolated from PoE circuitry by ≥ 1500 VRMS
 - ☐ Surge and ESD currents routed directly to chassis ground
 - ☐ No direct DC connection between chassis ground and PoE ground domains

To isolate the board from ESD events and to prevent a common-mode noise ground path, a separate chassis ground region should be allocated. This separate chassis ground, as shown in the following figure should be electrically connected to the external chassis and to the shield ground of the RJ-45 connectors.

Figure 2-2. Recommended Separate Chassis Ground

3. Power Supply

The following section outlines the power supply requirements for the PD7771xTx and PD77010 devices.

3.1. PD7771xTx Power Requirements

- 3.3 V PoE-Domain Supply (VDD / VDDA)
 - ☐ Regulated 3.3 V PoE-domain supply connected to VDD pin
 - ☐ VDDA connected to VDD at a single point near the device (not tied to a general 3.3 V plane)
 - ☐ Local decoupling placed close to VDD pin (minimum: 0.1 μ F ceramic)
 - ☐ Additional bulk decoupling on VDD (typ. 1 μ F–4.7 μ F ceramic)
 - ☐ Local decoupling placed close to VDDA pin (minimum: 0.1 μ F ceramic)
 - ☐ VDDA routing isolated from noisy digital or high-current paths
 - ☐ Regulated 3.3 V PoE-domain supply connected to VDD (pin 43)
 - ☐ VDDA (pin 22) connected to VDD at a single point near the device (not tied to the general PCB 3.3 V plane)
 - ☐ High-frequency decoupling capacitor placed close to VDD (pin 43) Recommended: 0.1 μ F ceramic
 - ☐ Bulk decoupling capacitor provided on VDD (pin 43) Recommended: 1 μ F–4.7 μ F ceramic
 - ☐ High-frequency decoupling capacitor placed close to VDDA (pin 22) Recommended: 0.1 μ F ceramic
 - ☐ VDDA (pin 22) routing isolated from noisy digital and high-current PoE paths
- Internal Regulator Decoupling
 - ☐ VREG1P8 pin decoupled locally
Pin 20: VREG1P8
Recommended: 1 μ F ceramic, placed close to the pin
Ground reference: LDGND
 - ☐ VDDCORE pin decoupled locally
Pin: VDDCORE
Recommended: 1 μ F ceramic, placed close to the pin
Ground reference: DGND
- Main PoE Input Supply (VMAIN, pin 17)
 - ☐ VMAIN connected to the main PoE power source within IEEE 802.3bt operating range
 - ☐ Bulk capacitance placed on VMAIN to support inrush current, load steps, and emergency power events
 - ☐ VMAIN bulk capacitance sized to maintain voltage during transient events and OSS response timing
 - ☐ VMAIN routing designed for high current with low impedance return paths
- Power-Up and Sequencing
 - ☐ No specific power-up sequencing required between VMAIN and 3.3 V supply

- ☐ All supply rails remain within recommended operating limits during startup and steady state
- Layout and Stability
 - ☐ All decoupling capacitors placed as close as possible to their respective pins
 - ☐ High-frequency decoupling (0.1 μ F) placed first in the return path
 - ☐ Bulk capacitors placed to minimize loop area and supply impedance

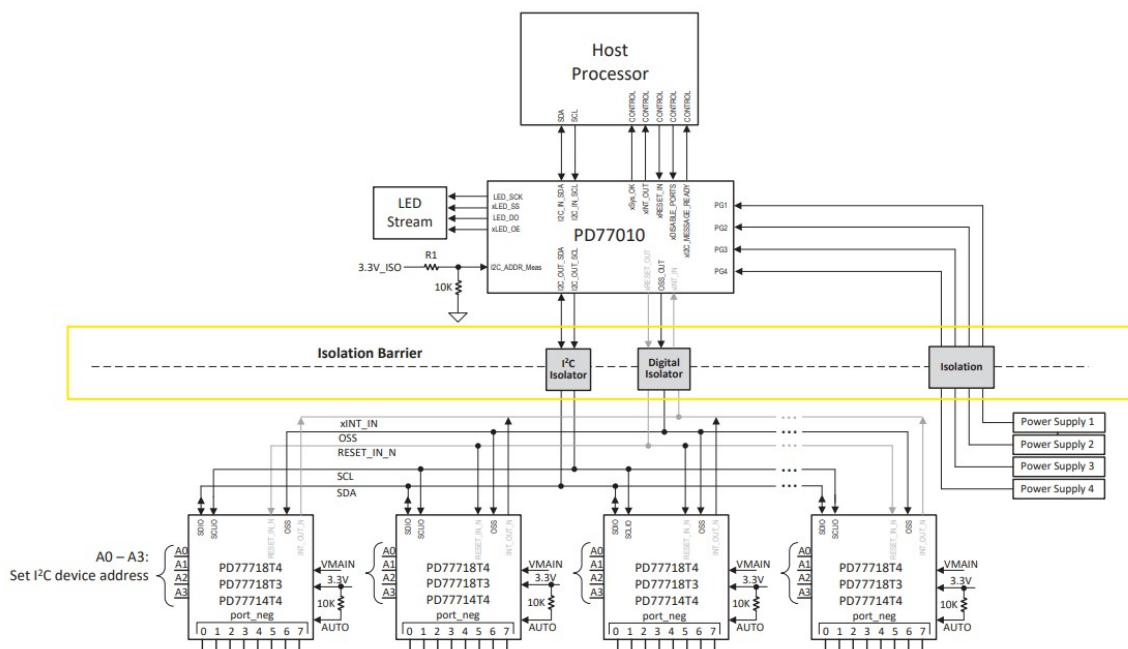
3.2. PD77010 Power Requirements

- Main 3.3 V Supply (Host Domain / 3_3V_iso)
 - ☐ Regulated, filtered 3.3 V host-domain supply provided for PD77010 operation (typical current <20 mA).
 - ☐ VDD (pin 30) connected to the 3.3 V host supply.
 - ☐ VDDA (pin 9) connected to the 3.3 V host supply (same 3.3 V domain as VDD).
 - ☐ VSSA (pin 10) connected to host ground reference for the PD77010 supply domain.
 - ☐ VSSD (pin 28) connected to host ground reference.
- 3.3 V Decoupling (VDD / VDDA)
 - ☐ 0.1 μ F ceramic decoupling capacitor placed as close as possible to VDD (pin 30) return to ground.
 - ☐ 1.0 μ F ceramic (X7R) bulk/decoupling capacitor placed close to VDD (pin 30)
 - ☐ 0.1 μ F ceramic decoupling capacitor placed close to VDDA (pin 9) return to VSSA (pin 10).
 - ☐ Keep VDD/VDDA decoupling loops small (capacitor-to-pin-to-ground loop area minimized).
- Internal Core Regulator Decoupling (Mandatory)
 - ☐ VDD_CORE (pin 29) decoupled with 1.0 μ F capacitor to VSSD (pin 28).
 - ☐ VDD_CORE decoupling capacitor placed immediately adjacent to pin 29 .
- Thermal / Ground Pad Requirements
 - ☐ EPAD connected to VSSA with sufficient copper area for thermal performance.
- Power-Bank / Power-Good Pins (Related Supply Robustness)
 - ☐ PG1–PG4 (pins 17–20) connected to valid power-good logic from up to four supplies (power banks).
 - ☐ If PG is not used, tie PG pins to GND.

4. Isolation

The PSE design must maintain an isolation barrier between the Host (Switch) domain and the PoE domain, consistent with IEEE® PoE requirements and the system topology.

Figure 4-1. Isolation Barrier



The communication path between PD77010 and the PD7771xTx managers must cross the isolation barrier using an I²C isolator rated for the required isolation level.

In addition to I²C, the PD77010 ↔ PD7771xTx design includes additional control lines:

OSS is used for fast disconnect and emergency power management actions; Use high-frequency digital isolation if used.

Placement Options for the Isolation Barrier Between the PD7771xTx and PD77010

Microchip's topology allows an architectural option where isolation may alternatively be placed between the PD77010 and the host processor (instead of between PD77010 and PD7771xTx), but this should be treated as a deliberate system-level decision because it changes which interfaces are isolated.

Powering across the barrier: Each side of the isolator must be powered from its own domain supply (host side versus PoE side). This is explicitly stated for the PD77010 ↔ PD7771xTx I²C interface (isolated I²C with separate supplies).

Practical implication: Ensure the PoE-domain 3.3V rail powering PD7771xTx-side logic and the host-domain 3.3V rail powering PD77010/host-side logic are not inadvertently shorted by pull-ups, test headers, LED circuits, or ESD structures.

I²C Timing and Clock Stretch Compatibility

The PD77010 ↔ PD7771xTx I²C interface require clock stretching. Isolator selection and pull-up sizing must not break clock-stretch behavior at the target clock rate.

Design implication: Choose an isolator that supports bidirectional SCL behavior and does not interfere with clock stretching, or add excessive delay.

Emergency power management uses the PD77010 PG1–PG4 inputs to detect supply changes and then sends a code to the PD7771xTx devices using OSS to shut down relevant ports. Isolation must not degrade this fast-response path.

Chassis Isolation

Chassis ground must remain isolated from PoE circuitry by 1500 VRMS. Verify no unintended connections through shields/mounting/ESD parts.

5. Communication and Control Interface

Communication Interfaces Overview

The controller-mode system uses two I²C interfaces plus several discrete control/status lines:

- Host CPU ↔ PD77010 through non-isolated I²C (up to 400 kHz)
- PD77010 ↔ PD7771xTx managers through isolated I²C (typ. 600 kHz; up to 1 MHz) and clock stretching required
- Discrete signals used for system control (disable/reset), status, and fast power actions (OSS)

5.1. Host CPU ↔ PD77010 (Non-Isolated I²C + Handshake)

Bus Characteristics

- Keep the Host I²C clock ≤ 400 kHz.
- Use the PD77010 host protocol (15-byte protocol) as the software layer for configuration and monitoring.
- The PD77010 provides a message-ready line (xI2C_MESSAGE_READY) so the host can avoid reading when no message is available. The controller asserts the line low when data is ready, and returns it high after the host reads the message.

5.2. PD77010 ↔ PD7771xTx (Isolated I²C)

Isolation and Powering

- The PD77010 ↔ PD7771xTx I²C link must be 1500 VRMS isolated, and each side of the isolator must be powered from its own domain supply.

Clock Stretching + Speed

- This bus requires clock stretching and operating typically around 600 kHz, with up to 1 MHz supported.
- Select an I²C isolator that supports bidirectional SCL behavior and does not break clock stretching.

PD7771xTx I²C Addressing

- PD7771xTx manager address is set by A0–A3 pins, strapped to VDD or DGND per the address table.

Table 5-1. PD7771xTx Addressing

A3	A2	A1	A0	I ² C Address
0	0	0	0	0x20
0	0	0	1	0x21
0	0	1	0	0x22
0	0	1	1	0x23
0	1	0	0	0x24
0	1	0	1	0x25
0	1	1	0	0x26
0	1	1	1	0x27
1	0	0	0	0x28
1	0	0	1	0x29
1	0	1	0	0x2A
1	0	1	1	0x2B
1	1	0	0	0x2C

Table 5-1. PD7771xTx Addressing (continued)

A3	A2	A1	A0	I ² C Address
1	1	0	1	0x2D
1	1	1	0	0x2E
1	1	1	1	0x2F

5.3. Discrete Control/Status Lines (Host ↔ PD77010)

These signals provide immediate hardware control independent of I²C:

- **xDISABLE_PORTS (active-low):** Host-driven; disables all PoE ports. PD77010 detects low and sends disable commands to PD7771xTx over I²C.
- **xRESET_IN (active-low):** Host-driven; resets PD77010 and all PD7771xTx managers. During reset, PD77010 outputs tri-state; on release it initializes and sends reset command over I²C.
- **xDISABLE_PORTS (active-low):** PD77010-generated status indicating main input voltage is within range (function depends on the serial protocol configuration).
- **xINT_OUT (active-low):** PD77010 interrupt output; asserted when host-configured events occur.
- **xI2C_MESSAGE_READY (active-low):** message-ready handshake.

Reset Line Conditioning

Use a 10 kΩ pull-up on the reset chain (xRESET_OUT on PD77010 and RESET_IN_N on PD7771xTx) and place a 47 nF filter capacitor close to the device pin .

5.4. Discrete Control/Status Lines (PD77010 ↔ PD7771xTx)

- **OSS:** Must be connected through high-frequency digital isolation. It implements fast over-budget disconnect and power-supply change disconnect behavior.

Table 5-2. PD7771xTx Interface Checklist

Interface	Signal (PD77010 pin #)	Connected To	Dir.	Domain Crossing	Isolation Required	Key Design Notes
Host ↔ PD77010	I2C_IN_SDA (21)	Host I ² C SDA	Bi-dir	Host domain only	No	2 kΩ pull-up required; host uses 15-byte protocol messages on this line.
Host ↔ PD77010	I2C_IN_SCL (22)	Host I ² C SCL	In	Host domain only	No	Speed limited to 400 kHz; 2 kΩ pull-up required.
Host ↔ PD77010	xI2C_MESSAGE_READY (27)	Host GPIO	Out	Host domain only	No	Active-low “message ready” handshake: host should only initiate I ² C read when this is low; returns high after read.
Host ↔ PD77010	xDISABLE_PORTS (24)	Host GPIO	In	Host domain only	No	Active-low; when asserted, PD77010 sends disable command over I ² C to all managers/ ports.

Table 5-2. PD7771xTx Interface Checklist (continued)

Interface	Signal (PD77010 pin #)	Connected To	Dir.	Domain Crossing	Isolation Required	Key Design Notes
Host ↔ PD77010	xRESET_IN (26)	Host reset source	In	Host domain only	No	Active-low; PD77010 enters reset and outputs tri-state; on release it initializes, and issues RESET over I ² C. Also requires 10 kΩ pull-up and 47 nF filter cap close to device
Host ↔ PD77010	xDATA_OK (23)	Host GPIO	Out	Host domain only	No	Active-low status output indicating main input voltage within range
Host ↔ PD77010	xINT_OUT (25)	Host interrupt input	Out	Host domain only	No	Active-low interrupt for host-configured events; may require pull-up per host requirements.
PD77010 ↔ PD7771xTx	I2C_OUT_SDA (1)	PD77718 SDIO (SDA) bus	Bi-dir	Host ↔ PoE boundary	Yes (I ² C isolation)	Requires 2 kΩ pull-up; PD77010 controls/ manages PD77718 devices through an isolated I ² C bus.
PD77010 ↔ PD7771xTx	I2C_OUT_SCL (2)	PD77718 SCLIO (SCL) bus	Out (but bus is bi-dir for stretch)	Host ↔ PoE boundary	Yes (I ² C isolation)	2 kΩ pull-up; 600 kHz typical. I ² C SCL is bidirectional and clock stretching is required; PD77718 supports up to 1 MHz
PD77010 ↔ PD7771xTx	OSS_OUT (7)	PD7771xTx OSS bus	Out	Host ↔ PoE boundary	Yes (digital isolation)	Must connect through digital isolation; used for fast communication to implement power-good actions and dynamic over-budget shutdown based on priority/power budget.

Table 5-2. PD7771xTx Interface Checklist (continued)

Interface	Signal (PD77010 pin #)	Connected To	Dir.	Domain Crossing	Isolation Required	Key Design Notes
PD77010 ↔ PD7771xTx	xRESET_OUT (3)	PD7771xTx RESET_IN_N bus	Out	Host ↔ PoE boundary	yes	Reset output (active-low) to managers; (10 kΩ pull-up and 47 nF filter cap close to device on the reset chain.)
PD77010 ↔ PD7771xTx	xINT_IN (4)	PD7771xTx INT_OUT_N (common)	In	Host ↔ PoE boundary	yes	Active-low open-drain interrupt input from common INT_OUT_N of all PD7771xTx devices; 10 kΩ pull-up to VDD on PD77010 side.
PD7771xTx config	(PD7771xTx A0–A3)	Strap pins A0–A3 (pins 48–51)	—	PoE domain only	No	PD7771xTx I ² C address is programmed via A0–A3; tie to VDD or DGND per address table.
Reserved / future	(Reset/Interrupt isolators)	—	—	Host ↔ PoE boundary	Footprint recommended	Reset/Interrupt functions reserved; recommended to route.

6. Port Configurations

Power Interface (PI) Overview

The PI is the physical point where the cabling connects to the PSE. In essence, it is where the two modular connectors touch.

The PI consists of eight individual contacts, that correspond to the eight conductors in a communication cable. Two conductors form a pair (a twisted pair in the cable), both always at the same nominal voltage. There are four pairs. A pairset consists of a positive and a negative pair. There are two pairsets, which are called Alternative A and Alternative B for the PSE. When a power interface consist of 4-pair, all 8 conductors are utilized.

6.1. PD7771xTx Port Configuration

- In a PD7771xTx-family based PSE, each Ethernet RJ-45 port is implemented as a power path + measurement path + protection path tied to the PoE magnetics and the PD7771xTx manager. The PD7771xTx devices are fully integrated PoE managers with integrated MOSFET switches and current-sense resistors, and are designed to be cascaded for high port-count systems.
- For port-level thermal and power-loss calculations, AN5347 defines the total channel resistance per port as 160 m Ω (typical). This value already includes the sense resistor and MOSFET R_{ds(on)}, so you should treat it as the baseline series resistance on the PSE side when estimating:
 - Per-port dissipation at high load
 - Worst-case temperature rise
 - Copper weight / plane sizing in the port-current path
- A front-end, per-line capacitor is required, rated 100 V, with a value between 47 nF and 220 nF. Place the capacitor close to the PD7771xTx port interface nodes (to keep the loop area small and reduce ringing/noise).
- Verify port front-end design is appropriate for the system surge requirements as described on AN4813.

6.2. RJ45 and Magnetics Port Configuration

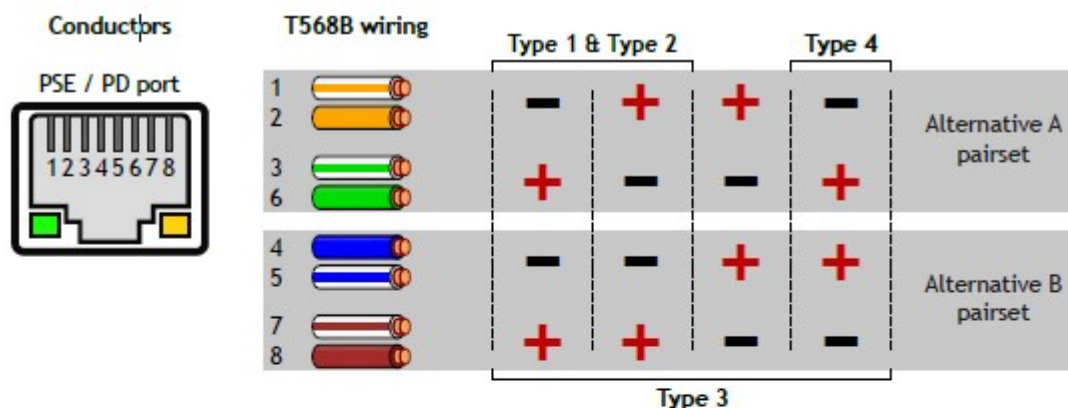
Ethernet magnetics provide the mandatory galvanic isolation between the PSE electronics and the Ethernet cable, while simultaneously enabling differential data transmission and PoE power injection. In a PoE-capable system, the magnetics must be selected and connected to support both Ethernet signal integrity and the maximum PoE power level required by the PSE type (Type 1–4).

The magnetics define the primary isolation barrier between the PSE circuitry and the external network and must meet IEEE isolation and safety requirements independent of the rest of the system design.

- Magnetics selected as PoE-capable and sized for desired PoE current
- Isolation rating and creepage/clearance verified at the port boundary.
- Each Ethernet port transformer must provide a minimum of 1500 VRMS isolation between the cable side and the PSE circuitry. This isolation applies to:
 - Differential signal windings
 - Center taps used for PoE power injection
 - Any shield or common-mode structures associated with the magnetics
- Creepage and clearance around the transformer pins, PCB traces, and termination components must be maintained according to the isolation rating of the selected magnetics. No DC connection is permitted across this isolation barrier.

- The Bob Smith termination must not connect directly to PoE ground or digital ground. Its sole reference should be chassis ground to provide a controlled RF return path for common-mode energy.
- Verify port pairs polarity follow the IEEE requirements
- Depending on the PSE type, different mappings of the PoE supply rails to the connector pins are permitted, resulting in different output polarities at the PSE power interface. In all cases, both conductors of a pair remain at the same polarity. Type 1 and Type 2 PSEs operate exclusively in 2-pair mode and may use either Alternative A or Alternative B. Type 3 PSEs may use any of the allowed polarity configurations, while Type 4 PSEs are restricted to a single polarity configuration. The selected polarity remains constant during detection, classification, and power delivery.
- Powered Devices (PDs) must accept any valid polarity configuration, requiring internal rectification. Type 3 and Type 4 PDs must also support both 2-pair and 4-pair input power. While Type 3 and Type 4 PSEs may operate in either 2-pair or 4-pair mode for Class 1 through Class 4 PDs, assignment of Class 5 or higher requires exclusive 4-pair power delivery. When operating in 2-pair mode, the selected alternative remains fixed until the port is power-cycled.

Figure 6-1. RJ45 polarity



	Assigned Class							
	1	2	3	4	5	6	7	8
Type 1 PSE	2P	2P	2P					
Type 2 PSE	2P	2P	2P	2P				
Type 3 PSE	2P 4P	2P 4P	2P 4P	2P 4P	4P	4P		
Type 4 PSE	2P 4P	2P 4P	2P 4P	2P 4P	4P	4P	4P	4P

If shielded RJ-45 connectors or magnetics with integrated shields are used:

- The shield must be connected to chassis ground, not PoE or logic ground.
- A direct, low-impedance path to chassis ground is preferred for ESD and surge current handling.
- Optional RC or ferrite coupling to chassis ground may be used if required by EMC testing, but must not violate isolation requirements

7. Surge Protection

The application note, AN4813 provides detailed explanation of the suggested surge protection circuit and components according to the system surge protection level requirements.

7.1. Surge Protection Guidelines

- Define the surge requirement and validation plan
- Confirm whether the cable installation is indoor versus outdoor, and whether you need primary protection (outdoor / high-energy at the front end) versus secondary protection (indoor / residual energy).
- Choose the target standard(s) and test sets (examples called out: ITU-T K.21, IEC61000-4-5, EN55024, GR-1089, UL/EN/IEC 62368-1)

7.2. Chassis Ground

Chassis ground provides the primary return path for ESD, surge, and common-mode noise originating from the Ethernet cable and must be treated as a separate, safety-related ground domain. The chassis ground plane must remain electrically isolated from all PoE and logic ground domains and must meet the required 1500 VRMS isolation. No DC connection between chassis ground and PoE ground is permitted.

All cable-side noise-control elements—including RJ-45 shield connections and the Bob Smith termination network—must reference chassis ground. The chassis ground connection should present a low-impedance path to the chassis to safely divert high-energy transient currents away from sensitive circuitry. If capacitive or resistive coupling to chassis ground is used, the components must be rated for the expected voltage stress and positioned to preserve isolation spacing.

Care must be taken to avoid unintended connections to chassis ground through mounting hardware, EMI or ESD components. Any optional coupling between chassis ground and PoE ground (such as RC networks or ferrites) must be evaluated at the system level and validated through EMC and surge testing.

8. Hardware Checklist Summary

Table 8-1. Hardware Design Checklist

Section	Check	Explanation	✓	Notes
General Considerations	Required References	All necessary documents are on hand.	☐	
	Pin Check	The pins match the data sheet and retain the reference design's use. See the pinout table.	☐	
Grounding	Grounding	Ground domains partitioned: AGND, LAGND, DGND, and LDGND are physically separated and tied at defined single points	☐	
		PD7771xTx EPAD connection: EPAD connected directly to AGND with sufficient copper for return current and thermal dissipation	☐	
		Analog ground tie: LAGND tied to AGND at a single point near the device EPAD.	☐	
		Ground coupling: LAGND coupled to DGND using capacitive network to control noise	☐	
		Host ground isolation: Host-domain ground isolated from PoE domain ground	☐	
		Chassis ground isolation: Chassis ground isolated ≥ 1500 VRMS and used for shields and Bob Smith termination	☐	
Power Supply	Power Supply	PD7771xTx supply-VDD and VDDA supplied from PoE-domain 3.3 V rail and properly decoupled	☐	
		PD7771xTx internal rails-VREG1P8 and VDDCORE locally decoupled for regulator stability	☐	
		VMAIN bulk capacitance-Bulk capacitance sized to support inrush and load transients	☐	
		PD77010 supply-VDD and VDDA supplied from host-domain 3.3 V rail	☐	
		PD77010 core decoupling-Mandatory VDD_CORE decoupling capacitor placed close to pin	☐	
Isolation	Isolation	Isolation boundary: Isolation boundary clearly defined between Host and PoE domains	☐	
		I ² C isolation: PD77010 to PD7771xTx I ² C link isolated and powered from separate domains	☐	
		Clock stretching: I ² C isolator supports bidirectional SCL and clock stretching	☐	
		OSS isolation: OSS routed through high-speed digital isolation	☐	
		Chassis isolation: No unintended chassis or ground shorts across isolation barrier	☐	

Table 8-1. Hardware Design Checklist (continued)

Section	Check	Explanation	✓	Notes
Communication and Control Interface	Host CPU ↔ PD77010 (Non-Isolated I ² C + Handshake)	Host I ² C speed: Host to PD77010 I ² C limited to 400 kHz and addressing matches circuit addressing with other I ² C devices	☐	
	Host CPU ↔ PD77010 (Non-Isolated I ² C + Handshake)	Reset chain: Reset pull-up and RC filtering implemented per guidance	☐	
	Discrete Control/Status Lines (Host ↔ PD77010)	PD7771xTx addressing: A0–A3 strapping documented and matches circuit addressing with other I ² C devices	☐	
	Discrete Control/Status Lines (Host ↔ PD77010)	Interrupt routing: Interrupt and control lines routed and isolated as required	☐	
Port Configurations	PD7771xTx Port Configuration	47–220 nF per-line front-end capacitors installed	☐	
	RJ45 and Magnetics Port Configuration	2-pair or 4-pair operation matches PSE type and assigned class	☐	
	RJ45 and Magnetics Port Configuration	Port polarity matches IEEE requirements	☐	
	RJ45 and Magnetics Port Configuration	Magnetics rated for Ethernet speed and PoE power level	☐	
	RJ45 and Magnetics Port Configuration	Transformer provides ≥1500 VRMS isolation	☐	
	RJ45 and Magnetics Port Configuration	PoE power injected symmetrically through transformer center taps	☐	
		Bob Smith implemented on cable side and referenced to chassis ground	☐	
		RJ-45 shield connected to chassis ground only	☐	
Surge Protection	Surge Protection Guidelines	Target surge level defined	☐	
	Surge Protection Guidelines	Surge components selected according to AN4813 guidance	☐	
	Chassis Ground	Surge and ESD currents routed to chassis ground	☐	
	Chassis Ground	Clamp components protect VMAIN rail	☐	

Table 8-2. PD7771xTx Pin Description

Pin	Designator	Description	Notes
1, 2, 4, 9, 11, 13, 15, 19, 23, 24, 25, 26, 27, 28, 29, 30, 32, 34, 39, 41, 42, 55	Not Connected (NC)	NC. Leave floating.	
3	VPORT_NEG0	Negative port 0 output	
5	VPORT_NEG1	Negative port 1 output	
6, 8, 16, 18, 35, 37	N/A	Pin removed	
7	VMAIN_7	Connect to VMAIN through PCB trace or 0Ω resistor for basic level protection. Leave unconnected for enhanced surge protection.	
10	VPORT_NEG2	Negative port 2 output	
12	VPORT_NEG3	Negative port 3 output	
14	IREF	Current reference resistor. Connect through 10K 0.1% to AGND.	
17	VMAIN	Connect to VMAIN. Connect a 1 μF, 100V, X7R capacitor near the VMAIN pin of each device.	
20	VREG1P8	Internal 1.8V regulator output capacitor connection. Connect a low-ESR, 1 μF capacitor to DGND.	
21	AGND	Analog Ground. Connect to DGND through a single point connection.	
22	VDDA	Analog 3.3V supply. Connect a capacitor to AGND. Connected to main 3.3V supply on the board.	
31	VPORT_NEG4	PD77718T4/PD77718T3: Negative port 4 output. PD77714T4: No connect, leave floating.	
33	VPORT_NEG5	PD77718T4/PD77718T3: Negative port 5 output. PD77714T4: No connect, leave floating.	
36	VMAIN_36	Connect to VMAIN through PCB trace or 0Ω resistor for basic level protection. Leave unconnected for enhanced surge protection.	
38	VPORT_NEG6	PD77718T4/PD77718T3: Negative port 6 output. PD77714T4: No connect, leave floating.	
40	VPORT_NEG7	PD77718T4/PD77718T3: Negative port 7 output. PD77714T4: No connect, leave floating.	
43	VDD	3.3V supply. Connect a low-ESR, 1 μF capacitor to DGND.	
44	RESET_IN_N	Reset Input. Active Low. Must be low for more than 50 μs for the reset to be considered valid. Connect pull-up resistor to 3.3V.	

Table 8-2. PD7771xTx Pin Description (continued)

Pin	Designator	Description	Notes
45	INT_OUT_N	Interrupt Output: The interrupt pin is asserted whenever an interrupt is required for the host to take an action. This pin is an open drain. A pull-up resistor to VDD is required when used. Interrupt output pin (open drain). Leave open if not used.	
46	DGND	Digital Ground. Connect to AGND through a single point connection.	
47	VDDCORE	Internal 1.2V regulator output capacitor connection. Connect a low-ESR, 1 μ F capacitor to DGND.	
48	A0	Address bit 0	
49	A1	Address bit 1	
50	A2	Address bit 2	
51	A3	Address bit 3	
52	AUTO	Pull this pin to VDDA with 10Kohm resistor	
53	SCLIO	I ² C clock	
54	SDIO	I ² C data	
56	OSS	Over Supply Shutdown signal. The OSS is a control pin required to turn off ports of a certain priority due to live removal or failure in one of the power supplies. Connect to Pin 7, OSS_OUT, of the PD77010 through isolation.	
Thermal Pad	EPAD	Exposed Pad. Connect to AGND. AGND must have enough copper masks to ensure adequate thermal performance.	

Table 8-3. PD77010 Pin Description

Pin	Designation	Description	Notes
1	I2C_OUT_SDA	I ² C bidirectional data to PD7771xTx devices. A 2 k Ω pull-up resistor is required.	
2	I2C_OUT_SCL	I ² C SCL signal to PD7771xTx devices. A 2 k Ω pull-up resistor (600 KHz Typical) is required.	
3	XRESET_OUT	Reset output (active low) to PD7771xTx devices.	
4	XINT_IN	An open-drain interrupt input from the common INT_OUT_N output from all the PD7771xTx devices. This pin is active low. Connect a 10K pull-up resistor to VDD.	
5	RESERVED	Unused, leave floating.	
6	RESERVED	Unused, leave floating.	
7	OSS_OUT	DATA output for OSS signaling to the PD7771xTx devices. Connect to the PD7771xTx8 OSS bus using isolation.	
8	RESERVED	Unused, leave floating.	
9	VDDA	Main supply 3.3V.	
10	VSSA	Ground.	
11	I2C_ADDR_MEAS	Analog input to determine the I ² C address.	

Table 8-3. PD77010 Pin Description (continued)

Pin	Designation	Description	Notes
12	LED_SCK	LED stream Clock out.	
13	XLED_SS	LED stream Client-Select (active low).	
14	LED_DO	LED stream Data out.	
15	XLED_OE	LED stream Output Enable (active low).	
16	RESERVED	Unused, leave floating.	
17	PG1	Power Good input 1.	
18	PG2	Power Good input 2.	
19	PG3	Power Good input 3.	
20	PG4	Power Good input 4.	
21	I2C_IN_SDA	I ² C bidirectional data to Host. 15-byte protocol messages are transmitted on this line. 2K pull-up required.	
22	I2C_IN_SCL	I ² C clock from the host processor. Speed is limited to 400 KHz. 2K pull-up required.	
23	xSys_OK	System validity indication. The behavior of this output is controlled by individual software mask (active low). This pin is a push-pull output.	
24	XDISABLE_PORTS	Disable all PoE ports. When this input is asserted low, the controller shuts down all PoE ports in the system.	
25	XINT_OUT	Interrupt output indication. This line is asserted low when a pre-configured event is in progress (active low). May require a pull-up resistor depending on Host requirements.	
26	XRESET_IN	Host Reset input (active low).	
27	XI2C_MESSAGE_READY	I ² C message ready indication to the host. This signal is LOW when a message is ready to be read.	
28	VSSD	Ground.	
29	VDD_CORE	1.2V core voltage. Connect 1 μ F capacitor to VSSD.	
30	VDD	Main 3.3V supply.	
31	SWD_CLK	Connect 1 k Ω pull-up to 3.3V.	
32	SWD_DIO	Leave open.	
ePAD	ePAD	Connect to VSSA. It must have sufficient copper mass to ensure adequate thermal performance.	

9. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 9-1. Revision History

Revision	Date	Description
A	May 2026	Initial Revision

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