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## 8-Channel 7-Level $\pm 80\text{V}$ High-Voltage Pulser with T/R Switches

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### Features

- High-Voltage CMOS Technology for High Performance
- 8-Channel, True 5-Level or Pseudo 7-Level,  $\pm 80\text{V}$ , 2A, with Return-to-Zero (RTZ) to True Zero Voltage
- Programmable  $\pm 0.5\text{A}$ ,  $1.0\text{A}$ ,  $1.5\text{A}$  and  $2\text{A}$  Output Current from  $V_{PP1}/V_{NN1}$
- Integrated Radio Frequency (RF) Blocking, Clamp Diode and RX Damp
- $13\Omega$  Transmit/Receive (T/R) and Low Voltage (LV) Switches Allow Receiver Multiplexing
- $160\Omega$  Auto-Bleeding Switches for RTZ True Zero
- 220 MHz Clock Retiming Synchronization Capability
- 2.5V, 3.3V Logic Control Voltage, designed to work with FPGA Inputs and Outputs (I/O) directly.
- Adjusting T/R Switch Delay, Avoid Echo Saturating
- TX Output Frequency up to 20 MHz
- -40 dB HD2 Second Harmonic Distortion at 5 MHz
- 12 mm x 12 mm x 1.20 mm 206-Lead TFBGA Package

### Applications

- Medical ultrasound imaging system
- NDT (nondestructive testing) ultrasound transmission pulsers
- Piezoelectric or capacitive transducer drivers

### Description

The HV7322 device is an 8-channel, true 5-level or pseudo 7-level, high-voltage pulser, with integrated T/R switches. HV7322 is designed for medical ultrasound applications. It is also fitted for NDT and other transducer drive applications.

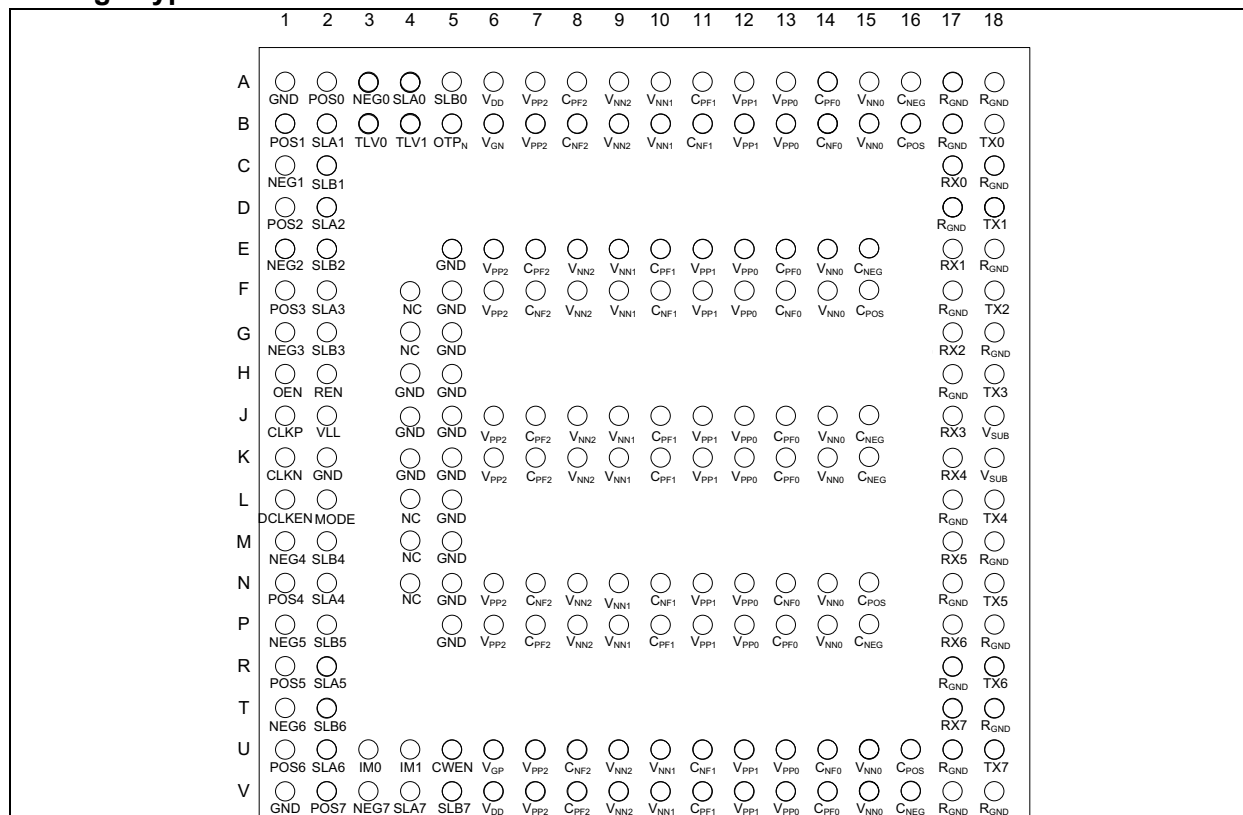
The HV7322 device's output has seven different voltage levels:  $V_{PP0,1,2}$ ,  $V_{NN0,1,2}$  and GND. The output MOSFET transistors can provide up to  $\pm 2\text{A}$  of current at the maximum voltage of  $\pm 80\text{V}$ . HV7322 has channel RTZ for the return-to-zero feature. The three sets of high-voltage outputs, with  $\pm 2\text{A}$  of peak output current in B-Mode and programmable 2-bit, use the  $V_{PP1}/V_{NN1}$  voltage rails for the CW-Mode ( $IM<1:0> = 0$ ), in order to reduce the CW-Mode power dissipations on chip.

The high-voltage T/R and LV analog switches (total  $13\Omega$ ) and RX damp switch are integrated in each channel, while the  $160\Omega$  RTZ switches dedicated for true zero voltage minimize the received noise.

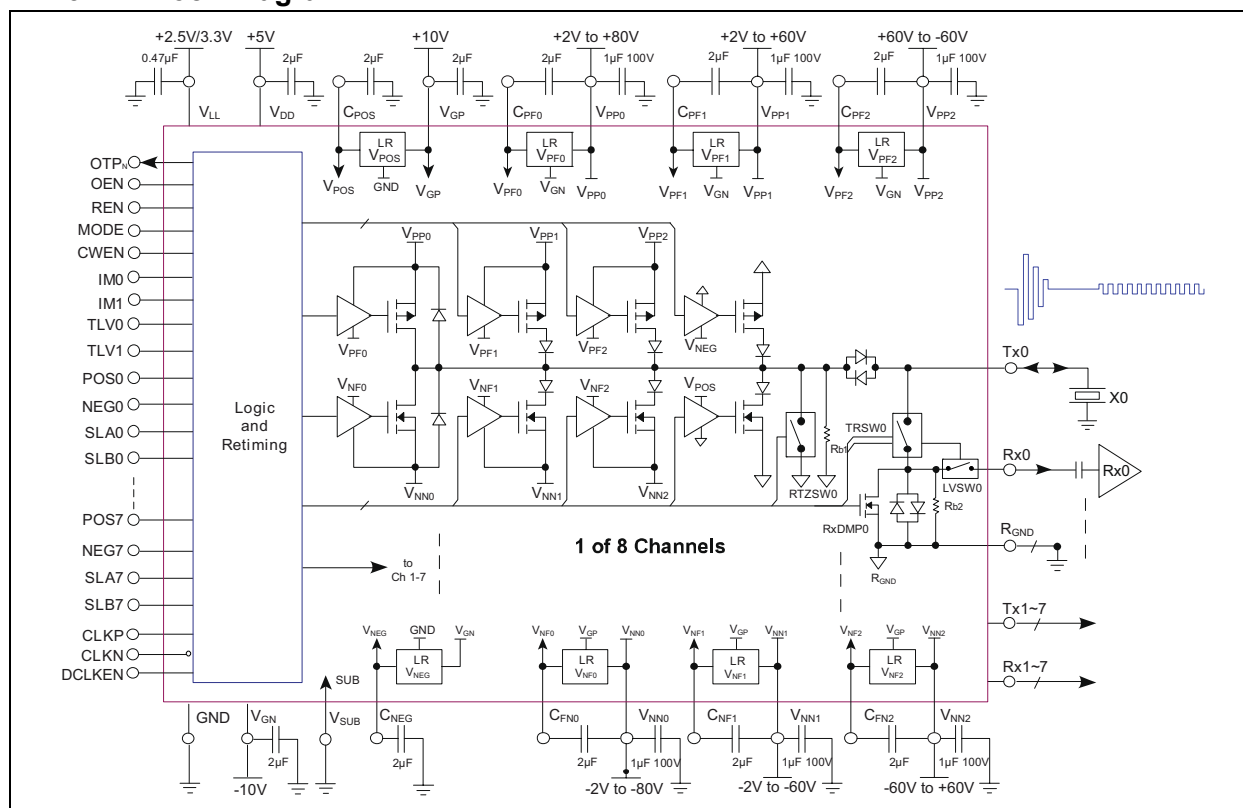
The 220 MHz differential retiming clock inputs and built-in registers are capable of providing low jitter in Continuous Wave Doppler (CWD) mode, in Pulse Wave (PW) mode or in B-mode. The clock synchronization realigns the logic input signals to a master clock, which reduces various propagation delays caused by FPGA inaccuracies and/or long PCB traces.

The integrated circuit (IC) has built-in gate-driver floating voltage regulators, allowing  $V_{PP0,1,2}$  and  $V_{NN0,1,2}$  high-voltage rails to move the voltage interdependently from 0 to  $\pm 80\text{V}$  or to 60V. Each of the pulsers has output voltage overshoot clamping diodes to the highest level of the supply pin of  $V_{PP0}$  or  $V_{NN0}$  rails respectively. The differential clock inputs take Differential Clock or LVCMOS output signals. The logic control voltages are designed to work with the Differential Clock or the LVCMOS logic families directly.

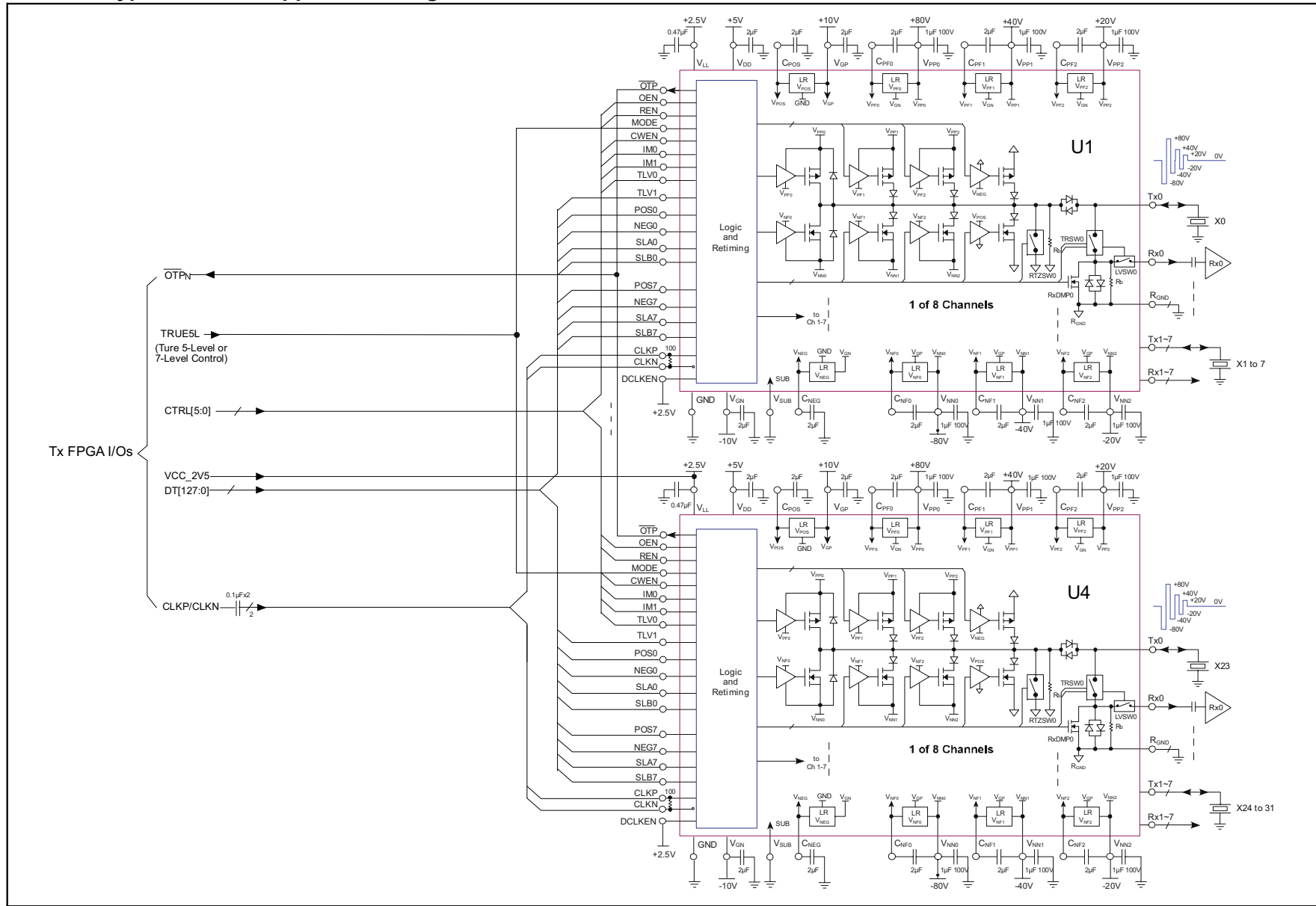
## Package Types



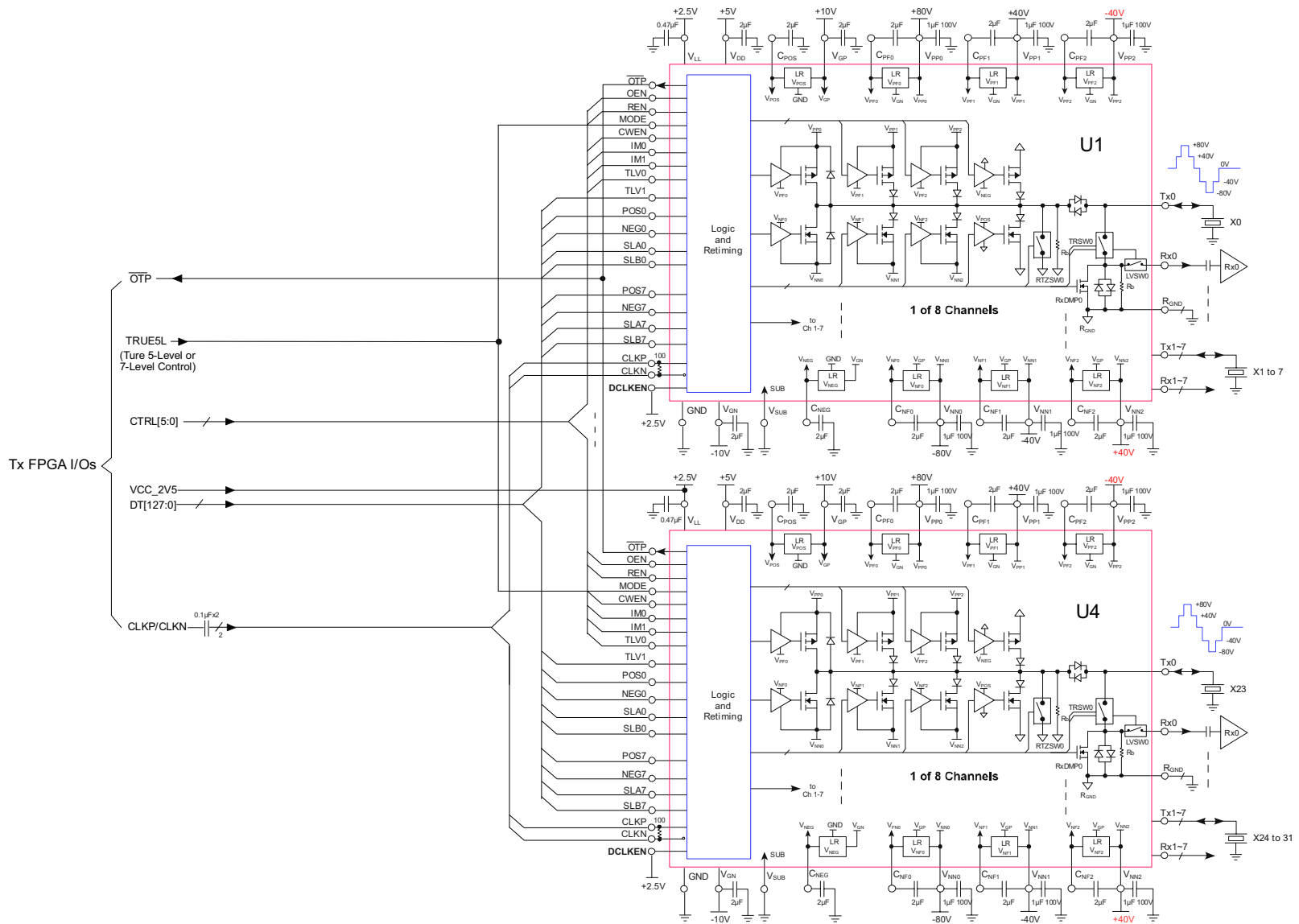
## HV7322 - Block Diagram



## HV7322 - Typical 7-Level Application Diagram



# HV7322 - Typical True 5-Level Application Diagram



# HV7322

## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings†

|                                                                                                                 |                   |
|-----------------------------------------------------------------------------------------------------------------|-------------------|
| Logic Voltage ( $V_{LL}$ )                                                                                      | –0.5V to +5.5V    |
| All I/O and CLK pin voltage ( $V_{IO}$ )                                                                        | –0.5V to +5.5V    |
| Positive voltage supply ( $V_{DD}$ )                                                                            | –0.5V to +5.5V    |
| Positive gate driver supply ( $V_{GP}$ )                                                                        | –0.5V to +13.5V   |
| Negative gate driver supply ( $V_{GN}$ )                                                                        | –13.5V to +0.5V   |
| High-voltage positive supply ( $V_{PP0}$ )                                                                      | –1.0V to +85V     |
| High-voltage positive supply ( $V_{PP1}$ )                                                                      | –1.0V to +65V     |
| High-voltage positive supply ( $V_{PP2}$ )                                                                      | –65V to +65V      |
| High-voltage negative supply ( $V_{NN0}$ )                                                                      | –85V to +1.0V     |
| High-voltage negative supply ( $V_{NN1}$ )                                                                      | –65V to +1.0V     |
| High-voltage negative supply ( $V_{NN2}$ )                                                                      | –65V to +65V      |
| TX pin voltage ( $V_{TX}$ )                                                                                     | –85V to +85V      |
| RX pin to GND voltage ( $V_{RX}$ )                                                                              | ±0.7 to ±1.4V     |
| Maximum not-latch-up current ( $I_{LU}$ )                                                                       | +100 mA           |
| ESD HBM Rating $T_X$ , $V_{PP}$ , $V_{NN}$ , CPF, CNF, CNEG, CPOS, $V_{GP}$ , $V_{GN}$ , $R_X$ , $R_{GND}$ pins | –0.50 to +0.50 kV |
| ESD HBM Rating – all other LV pins                                                                              | –2.0 to +2.0 kV   |

† **Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

### ELECTRICAL CHARACTERISTICS

**Electrical specifications:**  $V_{LL} = +2.5V$ ,  $V_{DD} = +5.0V$ ,  $V_{PP0} = +80V$ ,  $V_{NN0} = -80V$ ,  $V_{PP1,2} = +60V$ ,  $V_{NN1,2} = -60V$ ,  $V_{GP} = +10V$ ,  $V_{GN} = -10V$ ,  $V_{SUB} = 0V$ ,  $MODE = 0$ ,  $OEN = REN = 1$ ,  $T_A = 25^\circ C$ .

| Parameter                        | Sym.      | Min.            | Typ.      | Max.            | Unit | Conditions                                                         |
|----------------------------------|-----------|-----------------|-----------|-----------------|------|--------------------------------------------------------------------|
| <b>Operating Supply Voltages</b> |           |                 |           |                 |      |                                                                    |
| Positive Logic Supply            | $V_{LL}$  | 2.25            | 2.50      | 3.60            | V    | —                                                                  |
| Internal Voltage Supply          | $V_{DD}$  | 4.75            | 5.0       | 5.25            | V    | —                                                                  |
| Positive Gate Driver Supply      | $V_{GP}$  | 8.0             | 10        | 12              | V    | —                                                                  |
| Negative Gate Driver Supply      | $V_{GN}$  | –12             | –10       | –8.0            |      |                                                                    |
| High Voltage Positive Supply     | $V_{PP0}$ | 0               | —         | 80              | V    | Must be $V_{PP0} \geq V_{PP1}$ and $V_{PP2}$                       |
|                                  | $V_{PP1}$ | 0               | —         | 60              |      | Must be $V_{PP1} \leq V_{PP0}$                                     |
|                                  | $V_{PP2}$ | 0               | —         | 60              | V    | MODE = 0<br>In the 7-Level Mode.<br>Must be $V_{PP2} \leq V_{PP0}$ |
|                                  | $V_{PP2}$ | $V_{NN1} - 0.7$ | $V_{NN1}$ | $V_{NN1} + 0.7$ | V    | MODE = 1<br>$ V_{PP2} - V_{NN1}  \leq 0.7$                         |

**Note 1:** Characterized only; not 100% tested in production.

**2:** Design guidance only.

## ELECTRICAL CHARACTERISTICS (CONTINUED)

| <b>Electrical specifications:</b> $V_{LL} = +2.5V$ , $V_{DD} = +5.0V$ , $V_{PP0} = +80V$ , $V_{NN0} = -80V$ , $V_{PP1,2} = +60V$ , $V_{NN1,2} = -60V$ , $V_{GP} = +10V$ , $V_{GN} = -10V$ , $V_{SUB} = 0V$ , $MODE = 0$ , $OEN = REN = 1$ , $T_A = 25^\circ C$ . |                |                 |           |                 |         |                                                                                                                                                         |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|-----------------|-----------|-----------------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------|
| Parameter                                                                                                                                                                                                                                                        | Sym.           | Min.            | Typ.      | Max.            | Unit    | Conditions                                                                                                                                              |
| High Voltage Negative Supply                                                                                                                                                                                                                                     | $V_{NN0}$      | -80             | —         | 0               | V       | Must be $V_{NN0} \leq V_{NN1}$ and $V_{NN2}$                                                                                                            |
|                                                                                                                                                                                                                                                                  | $V_{NN1}$      | -60             | —         | 0               |         | Must be $V_{NN1} \geq V_{NN0}$                                                                                                                          |
|                                                                                                                                                                                                                                                                  | $V_{NN2}$      | -60             | —         | 0               | V       | MODE = 0<br>In the 7-Level Mode.<br>Must $V_{NN2} \geq V_{NN0}$                                                                                         |
|                                                                                                                                                                                                                                                                  | $V_{NN2}$      | $V_{PP1} - 0.7$ | $V_{PP1}$ | $V_{PP1} + 0.7$ | V       | MODE = 1<br>$ V_{NN2} - V_{PP1}  \leq 0.7$                                                                                                              |
| <b>Operating Supply Current</b>                                                                                                                                                                                                                                  |                |                 |           |                 |         |                                                                                                                                                         |
| $V_{LL}$ Quiescent Current                                                                                                                                                                                                                                       | $I_{LLQ}$      | —               | 2         | 5               | $\mu A$ | OEN = REN = 0                                                                                                                                           |
| $V_{DD}$ Quiescent Current                                                                                                                                                                                                                                       | $I_{DDQ}$      | —               | 54        | 65              | $\mu A$ |                                                                                                                                                         |
| $V_{PP0}$ Quiescent Current                                                                                                                                                                                                                                      | $I_{PP0Q}$     | —               | —         | 15              | $\mu A$ |                                                                                                                                                         |
| $V_{NN0}$ Quiescent Current                                                                                                                                                                                                                                      | $I_{NN0Q}$     | -15             | —         | —               | $\mu A$ |                                                                                                                                                         |
| $V_{PP1}$ Quiescent Current                                                                                                                                                                                                                                      | $I_{PP1Q}$     | —               | —         | 20              | $\mu A$ |                                                                                                                                                         |
| $V_{NN1}$ Quiescent Current                                                                                                                                                                                                                                      | $I_{NN1Q}$     | -20             | —         | —               | $\mu A$ |                                                                                                                                                         |
| $V_{PP2}$ Quiescent Current                                                                                                                                                                                                                                      | $I_{PP2Q}$     | —               | —         | 40              | $\mu A$ |                                                                                                                                                         |
| $V_{NN2}$ Quiescent Current                                                                                                                                                                                                                                      | $I_{NN2Q}$     | -40             | —         | —               | $\mu A$ |                                                                                                                                                         |
| $V_{DD}$ Current                                                                                                                                                                                                                                                 | $I_{DDEN}$     | —               | 1         | 2               | mA      | DCLKEN = 0<br>$f_{TX} = 0$ MHz<br>$f_{CLK} = 0$                                                                                                         |
| $V_{PP0}$ Current                                                                                                                                                                                                                                                | $I_{PP0EN}$    | —               | 0.26      | 0.4             | mA      |                                                                                                                                                         |
| $V_{NN0}$ Current                                                                                                                                                                                                                                                | $I_{NN0EN}$    | -0.4            | -0.34     | —               | mA      |                                                                                                                                                         |
| $V_{PP1}$ Current                                                                                                                                                                                                                                                | $I_{PP1EN}$    | —               | 0.12      | 0.3             | mA      |                                                                                                                                                         |
| $V_{NN1}$ Current                                                                                                                                                                                                                                                | $I_{NN1EN}$    | -0.3            | -0.13     | —               | mA      |                                                                                                                                                         |
| $V_{PP2}$ Current                                                                                                                                                                                                                                                | $I_{PP2EN}$    | —               | 0.12      | 0.3             | mA      |                                                                                                                                                         |
| $V_{NN2}$ Current                                                                                                                                                                                                                                                | $I_{NN2EN}$    | -0.3            | -0.12     | —               | mA      |                                                                                                                                                         |
| $V_{LL}$ Current with Re-Timing                                                                                                                                                                                                                                  | $I_{LL\_DCLK}$ | —               | 0.41      | 0.45            | mA      | DCLKEN = 1, $f_{CLK} = 160$ MHz<br>TX one-channel output active, no load.<br>The continuous values are calculated from measured burst-mode 5 MHz cases. |
| $V_{DD}$ Current with Re-Timing                                                                                                                                                                                                                                  | $I_{DD\_DCLK}$ | —               | 25        | 30              | mA      |                                                                                                                                                         |

**Note 1:** Characterized only; not 100% tested in production.

**2:** Design guidance only.

## ELECTRICAL CHARACTERISTICS (CONTINUED)

| Electrical specifications: $V_{LL} = +2.5V$ , $V_{DD} = +5.0V$ , $V_{PP0} = +80V$ , $V_{NN0} = -80V$ , $V_{PP1,2} = +60V$ , $V_{NN1,2} = -60V$ , $V_{GP} = +10V$ , $V_{GN} = -10V$ , $V_{SUB} = 0V$ , $MODE = 0$ , $OEN = REN = 1$ , $T_A = 25^{\circ}C$ . |               |      |       |      |          |                                                                                                                                                                                                                      |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|------|-------|------|----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Parameter                                                                                                                                                                                                                                                  | Sym.          | Min. | Typ.  | Max. | Unit     | Conditions                                                                                                                                                                                                           |
| $V_{LL}$ Maximum Current in B-Mode                                                                                                                                                                                                                         | $I_{LL5}$     | —    | 26    | 60   | $\mu A$  | DCLKEN = 0 $f_{CLK} = 0$ MHz, in B-Mode<br>TX one-channel output, no loads.<br>The continuous values are calculated from the measured burst-mode 5 MHz cases.<br>$I_{NN25}$ and $I_{PP25}$ are only in 7-Level Mode. |
| $V_{DD}$ Maximum Current in B-Mode                                                                                                                                                                                                                         | $I_{DD5}$     | —    | 1.4   | 1.6  | mA       |                                                                                                                                                                                                                      |
| $V_{GP}$ Maximum Current in B-Mode                                                                                                                                                                                                                         | $I_{GP5}$     | —    | 3.4   | 6    | mA       |                                                                                                                                                                                                                      |
| $V_{GN}$ Maximum Current in B-Mode                                                                                                                                                                                                                         | $I_{GN5}$     | -16  | -12.9 | —    | mA       |                                                                                                                                                                                                                      |
| $V_{PP0}$ Current in B-Mode                                                                                                                                                                                                                                | $I_{PP05}$    | —    | 102   | 115  | mA       |                                                                                                                                                                                                                      |
| $V_{NN0}$ Current in B-Mode                                                                                                                                                                                                                                | $I_{NN05}$    | -105 | -96   | —    | mA       |                                                                                                                                                                                                                      |
| $V_{PP1}$ Current in B-Mode                                                                                                                                                                                                                                | $I_{PP15}$    | —    | 85    | 95   | mA       |                                                                                                                                                                                                                      |
| $V_{NN1}$ Current in B-Mode                                                                                                                                                                                                                                | $I_{NN15}$    | -95  | -84   | —    | mA       |                                                                                                                                                                                                                      |
| $V_{PP2}$ Current in B-Mode                                                                                                                                                                                                                                | $I_{PP25}$    | —    | 94    | 105  | mA       |                                                                                                                                                                                                                      |
| $V_{NN}$ Current in B-Mode                                                                                                                                                                                                                                 | $I_{NN25}$    | -100 | -91   | —    | mA       |                                                                                                                                                                                                                      |
| $V_{GP}$ Current in CW-Mode                                                                                                                                                                                                                                | $I_{GPCW}$    | —    | 1.5   | 2    | mA       | TX one-channel output 5 MHz, continuous, no loads.<br>$V_{PP1}/V_{NN1} = \pm 5V$ in CW-Mode.<br>SLB = 0, SLA = 1, <a href="#">Note 1</a>                                                                             |
| $V_{GN}$ Current in CW-Mode                                                                                                                                                                                                                                | $I_{GNCW}$    | -4.4 | -4    | —    | mA       |                                                                                                                                                                                                                      |
| $V_{PP1}$ Current in CW-Mode                                                                                                                                                                                                                               | $I_{PP1CW}$   | —    | 24.4  | 26   | mA       |                                                                                                                                                                                                                      |
| $V_{NN1}$ Current in CW-Mode                                                                                                                                                                                                                               | $I_{NN1CW}$   | -26  | -23.5 | —    | mA       |                                                                                                                                                                                                                      |
| TX Output P-Channel MOSFET on $V_{PP0}$ , $V_{PP2}$                                                                                                                                                                                                        |               |      |       |      |          |                                                                                                                                                                                                                      |
| On-Resistance                                                                                                                                                                                                                                              | $R_{ON\_P0}$  | —    | 13    | 16   | $\Omega$ | $I_{SD} = 100$ mA                                                                                                                                                                                                    |
| Peak Output Current                                                                                                                                                                                                                                        | $I_{OUT\_P0}$ | 0.9  | 1.1   | —    | A        | $V_{PP0} = 25V$ , $R_L = 1.0\Omega$ to GND, <a href="#">Note 1</a>                                                                                                                                                   |
|                                                                                                                                                                                                                                                            |               | 1.7  | 2.02  | —    | A        | $V_{PP0} = 80V$ , $R_L = 1.0\Omega$ to GND, <a href="#">Note 1</a>                                                                                                                                                   |
| On-Resistance                                                                                                                                                                                                                                              | $R_{ON\_P2}$  | —    | 12.1  | 14   | $\Omega$ | $I_{SD} = 100$ mA                                                                                                                                                                                                    |
| Peak Output Current                                                                                                                                                                                                                                        | $I_{OUT\_P2}$ | 1.2  | 1.4   | —    | A        | $V_{PP2} = 25V$ , $R_L = 1.0\Omega$ to GND, <a href="#">Note 1</a>                                                                                                                                                   |
|                                                                                                                                                                                                                                                            |               | 1.6  | 2.0   | —    | A        | $V_{PP2} = 60V$ , $R_L = 1.0\Omega$ to GND, <a href="#">Note 1</a>                                                                                                                                                   |

**Note 1:** Characterized only; not 100% tested in production.

**2:** Design guidance only.

## ELECTRICAL CHARACTERISTICS (CONTINUED)

| Electrical specifications: $V_{LL} = +2.5V$ , $V_{DD} = +5.0V$ , $V_{PP0} = +80V$ , $V_{NN0} = -80V$ , $V_{PP1,2} = +60V$ , $V_{NN1,2} = -60V$ , $V_{GP} = +10V$ , $V_{GN} = -10V$ , $V_{SUB} = 0V$ , $MODE = 0$ , $OEN = REN = 1$ , $T_A = 25^{\circ}C$ . |                             |      |       |      |          |                                                                                                                         |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------|------|-------|------|----------|-------------------------------------------------------------------------------------------------------------------------|
| Parameter                                                                                                                                                                                                                                                  | Sym.                        | Min. | Typ.  | Max. | Unit     | Conditions                                                                                                              |
| TX Output P-Channel MOSFET on $V_{PP1}$                                                                                                                                                                                                                    |                             |      |       |      |          |                                                                                                                         |
| Peak Output Current<br>$IM<1:0> = 00$                                                                                                                                                                                                                      | $I_{OUT\_P1}$<br>$CWEN = 0$ | 0.3  | 0.39  | —    | A        | $V_{PP1} = 25V$ , $R_L = 1.0\Omega$ to GND<br>20 ns pulse width at the duty cycle.<br>D% = 0.1%, <a href="#">Note 1</a> |
| Peak Output Current<br>$IM<1:0> = 01$                                                                                                                                                                                                                      |                             | 0.6  | 0.76  | —    |          |                                                                                                                         |
| Peak Output Current<br>$IM<1:0> = 10$                                                                                                                                                                                                                      |                             | 0.9  | 0.11  | —    |          |                                                                                                                         |
| Peak Output Current<br>$IM<1:0> = 11$                                                                                                                                                                                                                      |                             | 1.2  | 1.44  | —    |          |                                                                                                                         |
| Peak Output Current<br>$IM<1:0> = 00$                                                                                                                                                                                                                      |                             | 0.35 | 0.5   | —    |          | $V_{PP1} = 60V$ , $R_L = 1.0\Omega$ to GND<br>20 ns pulse width at the duty cycle.<br>D% = 0.1%, <a href="#">Note 1</a> |
| Peak Output Current<br>$IM<1:0> = 01$                                                                                                                                                                                                                      |                             | 0.8  | 1.0   | —    |          |                                                                                                                         |
| Peak Output Current<br>$IM<1:0> = 10$                                                                                                                                                                                                                      |                             | 1.15 | 1.5   | —    |          |                                                                                                                         |
| Peak Output Current<br>$IM<1:0> = 11$                                                                                                                                                                                                                      |                             | 1.6  | 1.9   | —    |          |                                                                                                                         |
| On-resistance<br>$IM<1:0> = 11$                                                                                                                                                                                                                            | $R_{ON\_P1}$<br>$CWEN = 0$  | —    | 11.2  | 13   | —        | $I_{SD} = 100\text{ mA}$ , <a href="#">Note 1</a>                                                                       |
| Peak Output Current<br>$IM<1:0> = 00$                                                                                                                                                                                                                      | $I_{OUT\_P1}$<br>$CWEN = 1$ | 160  | 192   | —    | mA       | $V_{PP1} = 10V$ , $R_L = 1.0\Omega$ to GND<br>20 ns pulse width at the duty cycle.<br>D% = 0.1%, <a href="#">Note 1</a> |
| Peak Output Current<br>$IM<1:0> = 01$                                                                                                                                                                                                                      |                             | 320  | 362   | —    |          |                                                                                                                         |
| CW On-Resistance<br>$IM<1:0> = X0$                                                                                                                                                                                                                         | $R_{ON\_P1}$<br>$CWEN = 1$  | —    | 41.6  | 47   | $\Omega$ | $I_{SD} = 100\text{ mA}$ , <a href="#">Note 1</a>                                                                       |
| CW On-Resistance<br>$IM<1:0> = X1$                                                                                                                                                                                                                         |                             | —    | 20    | 22   |          |                                                                                                                         |
| TX Output N-Channel MOSFET on $V_{NN0}$ , $V_{NN2}$                                                                                                                                                                                                        |                             |      |       |      |          |                                                                                                                         |
| On-Resistance                                                                                                                                                                                                                                              | $R_{ON\_N0}$                | —    | 10    | 12   | $\Omega$ | $I_{DS} = 100\text{ mA}$                                                                                                |
| Peak Output Current                                                                                                                                                                                                                                        | $I_{OUT\_N0}$               | —    | -1.3  | -1.1 | A        | $V_{NN0} = -25V$ , $R_L = 1.0\Omega$ to GND, <a href="#">Note 1</a>                                                     |
|                                                                                                                                                                                                                                                            |                             | —    | -1.8  | -1.5 | A        | $V_{NN0} = -80V$ , $R_L = 1.0\Omega$ to GND, <a href="#">Note 1</a>                                                     |
| On-Resistance                                                                                                                                                                                                                                              | $R_{ON\_N2}$                | —    | 8.6   | 10   | $\Omega$ | $I_{DS} = 100\text{ mA}$                                                                                                |
| Peak Output Current                                                                                                                                                                                                                                        | $I_{OUT\_N2}$               | —    | -1.5  | -1.3 | A        | $V_{NN2} = -25V$ , $R_L = 1.0\Omega$ to GND, <a href="#">Note 1</a>                                                     |
|                                                                                                                                                                                                                                                            |                             | —    | -1.92 | -1.5 | A        | $V_{NN2} = -60V$ , $R_L = 1.0\Omega$ to GND, <a href="#">Note 1</a>                                                     |

**Note 1:** Characterized only; not 100% tested in production.

**2:** Design guidance only.

## ELECTRICAL CHARACTERISTICS (CONTINUED)

**Electrical specifications:**  $V_{LL} = +2.5V$ ,  $V_{DD} = +5.0V$ ,  $V_{PP0} = +80V$ ,  $V_{NN0} = -80V$ ,  $V_{PP1,2} = +60V$ ,  $V_{NN1,2} = -60V$ ,  $V_{GP} = +10V$ ,  $V_{GN} = -10V$ ,  $V_{SUB} = 0V$ ,  $MODE = 0$ ,  $OEN = REN = 1$ ,  $T_A = 25^\circ C$ .

| Parameter                                      | Sym.                            | Min. | Typ.  | Max.  | Unit | Conditions                                                                                                                        |
|------------------------------------------------|---------------------------------|------|-------|-------|------|-----------------------------------------------------------------------------------------------------------------------------------|
| TX Output N-Channel MOSFET on V <sub>NN1</sub> |                                 |      |       |       |      |                                                                                                                                   |
| Peak Output Current<br>IM<1:0> = 00            | I <sub>OUT_N1</sub><br>CWEN = 0 | —    | -0.42 | -0.3  | A    | V <sub>NN1</sub> = -25V, R <sub>L</sub> = 1.0Ω to GND<br>20 ns pulse width at the duty cycle<br>D% = 0.1%, <a href="#">Note 1</a> |
| Peak Output Current<br>IM<1:0> = 01            |                                 | —    | -0.8  | -0.6  |      |                                                                                                                                   |
| Peak Output Current<br>IM<1:0> = 10            |                                 | —    | -1.16 | -0.9  |      |                                                                                                                                   |
| Peak Output Current<br>IM<1:0> = 11            |                                 | —    | -1.51 | -1.3  |      |                                                                                                                                   |
| Peak Output Current<br>IM<1:0> = 00            |                                 | —    | -0.5  | -0.35 |      | V <sub>NN1</sub> = -60V, R <sub>L</sub> = 1.0Ω to GND<br>20 ns pulse width at the duty cycle<br>D% = 0.1%, <a href="#">Note 1</a> |
| Peak Output Current<br>IM<1:0> = 01            |                                 | —    | -1.0  | -0.7  |      |                                                                                                                                   |
| Peak Output Current<br>IM<1:0> = 10            |                                 | —    | -1.5  | -1.25 |      |                                                                                                                                   |
| Peak Output Current<br>IM<1:0> = 11            |                                 | —    | -1.9  | -1.6  |      |                                                                                                                                   |
| On-Resistance<br>IM<1:0> = 11                  | R <sub>ON_N1</sub><br>CWEN = 0  | —    | 8.3   | 10    | Ω    | I <sub>DS</sub> = 100 mA, <a href="#">Note 1</a>                                                                                  |
| Peak Output Current<br>IM<1:0> = X0            | I <sub>OUT_N1</sub><br>CWEN = 1 | —    | -212  | -180  | mA   | V <sub>NN1</sub> = -10V, R <sub>L</sub> = 1.0Ω to GND<br>20 ns pulse width at the duty cycle<br>D% = 0.1%, <a href="#">Note 1</a> |
| Peak Output Current<br>IM<1:0> = X1            |                                 | —    | -386  | -340  |      |                                                                                                                                   |
| CW On-Resistance<br>IM<1:0> = X0               | R <sub>ON_N1</sub><br>CWEN = 1  | —    | 42    | 48    | Ω    | I <sub>DS</sub> = 100 mA, <a href="#">Note 1</a>                                                                                  |
| CW On-Resistance<br>IM<1:0> = X1               |                                 | —    | 17    | 19    |      |                                                                                                                                   |
| TX Damping MOSFET on GND                       |                                 |      |       |       |      |                                                                                                                                   |
| On-Resistance                                  | R <sub>ON_PDMP</sub>            | —    | 9     | 14    | Ω    | I <sub>SD</sub> = 100 mA, <a href="#">Note 1</a>                                                                                  |
| B-Mode Peak Output Current <sup>(1)</sup>      | I <sub>OUT_PDMP</sub>           | 1.15 | 1.57  | —     | A    | R <sub>L</sub> = 1.0Ω at TX to V <sub>NN0</sub> = - 25V<br>20 ns pulse width at<br>D% = 0.1%, <a href="#">Note 1</a>              |
|                                                |                                 | 1.35 | 1.9   | —     | A    | R <sub>L</sub> = 1.0Ω at TX to V <sub>NN0</sub> = - 80V<br>20 ns pulse width at<br>D% = 0.1%, <a href="#">Note 1</a>              |
| On-Resistance                                  | R <sub>ON_NDMP</sub>            | —    | 7     | 13    | Ω    | I <sub>DS</sub> = 100 mA, <a href="#">Note 1</a>                                                                                  |
| B-Mode Peak Output Current <sup>(1)</sup>      | I <sub>OUT_NDMP</sub>           | —    | -1.56 | -1.15 | A    | R <sub>L</sub> = 1.0Ω at TX to V <sub>PP0</sub> = +25V<br>20 ns pulse width at<br>D% = 0.1%, <a href="#">Note 1</a>               |
|                                                |                                 | —    | -2.02 | -1.6  | A    | R <sub>L</sub> = 1.0Ω at TX to V <sub>PP0</sub> = +80V<br>20 ns pulse width at<br>D% = 0.1%, <a href="#">Note 1</a>               |

**Note 1:** Characterized only; not 100% tested in production.

**2:** Design guidance only.

## ELECTRICAL CHARACTERISTICS (CONTINUED)

| <b>Electrical specifications:</b> $V_{LL} = +2.5V$ , $V_{DD} = +5.0V$ , $V_{PP0} = +80V$ , $V_{NN0} = -80V$ , $V_{PP1,2} = +60V$ , $V_{NN1,2} = -60V$ , $V_{GP} = +10V$ , $V_{GN} = -10V$ , $V_{SUB} = 0V$ , $MODE = 0$ , $OEN = REN = 1$ , $T_A = 25^{\circ}C$ . |             |      |      |      |           |                                                           |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|------|------|------|-----------|-----------------------------------------------------------|
| Parameter                                                                                                                                                                                                                                                         | Sym.        | Min. | Typ. | Max. | Unit      | Conditions                                                |
| <b>RTZSW Auto Bleed High-Voltage Analog Switch</b>                                                                                                                                                                                                                |             |      |      |      |           |                                                           |
| RTZSW On-Resistance                                                                                                                                                                                                                                               | $R_{RTZSW}$ | —    | 152  | 164  | $\Omega$  | $I_{RTZSW} = \pm 1.0 \text{ mA}$ , <a href="#">Note 1</a> |
| RTZSW to GND Bleed Resistors                                                                                                                                                                                                                                      | $R_{b1}$    | 18   | 20   | 22   | $k\Omega$ | <a href="#">Note 1</a>                                    |
| RTZSW Off Withstand Voltage                                                                                                                                                                                                                                       | $V_{RTZSW}$ | -80  | —    | +80  | V         | $I_{RTZSW} = \pm 100 \mu A$ , <a href="#">Note 1</a>      |
| <b>TX OUTPUT Isolation Diodes and Bleed Resistor</b>                                                                                                                                                                                                              |             |      |      |      |           |                                                           |
| Diode Forward Voltage                                                                                                                                                                                                                                             | $V_F$       | —    | 1.2  | 1.9  | V         | $I_{FM} = 300 \text{ mA}$ , <a href="#">Note 2</a>        |
| Forward Continuous Current                                                                                                                                                                                                                                        | $I_{FM}$    | —    | 250  | —    | mA        | <a href="#">Note 2</a>                                    |
| Peak Forward Pulse Current                                                                                                                                                                                                                                        | $I_{FSM}$   | —    | 3.0  | —    | A         | $PW = 50 \text{ ns}$ , <a href="#">Note 2</a>             |
| Total Capacitance of 2-Diode                                                                                                                                                                                                                                      | $C_T$       | —    | 3.2  | 4    | pF        | At 1 MHz, 1 dBm, 0V DC, <a href="#">Note 2</a>            |
| <b>TRSW, LVSW and RXDMP Switches</b>                                                                                                                                                                                                                              |             |      |      |      |           |                                                           |
| TRSW and LVSW Switch-On Resistor                                                                                                                                                                                                                                  | $R_{TRSW}$  | —    | 13   | 18   | $\Omega$  | $I_{TRSW} = \pm 1.0 \text{ mA}$ , <a href="#">Note 1</a>  |
| TRSW Off Withstand Voltage                                                                                                                                                                                                                                        | $V_{TRSW}$  | -80  | —    | +80  | V         | $I_{SW} = \pm 100 \mu A$ , <a href="#">Note 1</a>         |
| LVSW Off Withstand Voltage                                                                                                                                                                                                                                        | $V_{LVSW}$  | -5.0 | —    | +5.0 | V         | $I_{SW} = \pm 10 \mu A$ , <a href="#">Note 1</a>          |
| RX to GND Protection Diode                                                                                                                                                                                                                                        | $V_F$       | —    | 1    | 1.2  | V         | $I_F = \pm 20 \text{ mA}$ , <a href="#">Note 1</a>        |
| RXDMP Switch On-Resistance                                                                                                                                                                                                                                        | $R_{RXDMP}$ | —    | 14   | 19   | $\Omega$  | $I_{SD} = \pm 1.0 \text{ mA}$ , <a href="#">Note 1</a>    |
| RX0~7 Pin to GND Bleed Resistor                                                                                                                                                                                                                                   | $R_{b2}$    | 13   | 20   | 27   | $k\Omega$ | <a href="#">Note 2</a>                                    |
| RX Pin to GND Capacitance                                                                                                                                                                                                                                         | $C_{RXG}$   | —    | 20   | 22   | pF        | 1 MHz, 1 dBm, 0V DC, <a href="#">Note 2</a>               |
| <b>Built-In Gate Drive Voltage Linear Regulators</b>                                                                                                                                                                                                              |             |      |      |      |           |                                                           |
| Output P-Channel Gate Drive Voltage Referenced to $V_{PP0}$                                                                                                                                                                                                       | $V_{PF0}$   | -5.2 | -4.5 | -4.1 | V         | $V_{GN} - V_{PP0} < -10V$                                 |
| Output P-Channel Gate Drive Voltage Referenced to $V_{PP1}$                                                                                                                                                                                                       | $V_{PF1}$   | -5.2 | -4.5 | -4.1 | V         | $V_{GN} - V_{PP1} < -10V$                                 |
| Output P-Channel Gate Drive Voltage Referenced to $V_{PP2}$                                                                                                                                                                                                       | $V_{PF2}$   | -5.2 | -4.5 | -4.1 | V         | $V_{NN0} - V_{PP2} < -10V$                                |
| Output N-Channel Gate Drive Voltage Referenced to $V_{NN0}$                                                                                                                                                                                                       | $V_{NF0}$   | 3.6  | 4.4  | 5.2  | V         | $V_{GP} - V_{NN0} > 10V$                                  |

**Note 1:** Characterized only; not 100% tested in production.

**2:** Design guidance only.

## ELECTRICAL CHARACTERISTICS (CONTINUED)

**Electrical specifications:**  $V_{LL} = +2.5V$ ,  $V_{DD} = +5.0V$ ,  $V_{PP0} = +80V$ ,  $V_{NN0} = -80V$ ,  $V_{PP1,2} = +60V$ ,  $V_{NN1,2} = -60V$ ,  $V_{GP} = +10V$ ,  $V_{GN} = -10V$ ,  $V_{SUB} = 0V$ ,  $MODE = 0$ ,  $OEN = REN = 1$ ,  $T_A = 25^\circ C$ .

| Parameter                                                   | Sym.       | Min.         | Typ. | Max.         | Unit | Conditions                                                                                                         |
|-------------------------------------------------------------|------------|--------------|------|--------------|------|--------------------------------------------------------------------------------------------------------------------|
| Output N-Channel Gate Drive Voltage Referenced to $V_{NN1}$ | $V_{NF1}$  | 3.6          | 4.4  | 5.2          | V    | $V_{GP} - V_{NN1} > 10V$                                                                                           |
| Output N-Channel Gate Drive Voltage Referenced to $V_{NN2}$ | $V_{NF2}$  | 3.6          | 4.3  | 5.2          | V    | $V_{PP0} - V_{NN2} > 10V$                                                                                          |
| Output N-Channel Gate Drive Voltage Referenced to GND       | $V_{POS}$  | 3.1          | 3.6  | 5.2          | V    | —                                                                                                                  |
| Output P-Channel Gate Drive Voltage Referenced to GND       | $V_{NEG}$  | −5.2         | −4.3 | −3.6         | V    | —                                                                                                                  |
| Logic & Clock Input Characteristics                         |            |              |      |              |      |                                                                                                                    |
| Input Logic Low Voltage                                     | $V_{IL}$   | 0            | —    | $0.2 V_{LL}$ | V    | —                                                                                                                  |
| Input Logic High Voltage                                    | $V_{IH}$   | $0.8 V_{LL}$ | —    | $V_{LL}$     | V    | —                                                                                                                  |
| Input Logic Low Current                                     | $I_{IL}$   | −1.0         | —    | —            | μA   | Note 1                                                                                                             |
| Input Logic High Current                                    | $I_{IH}$   | —            | —    | 1.0          | μA   | Note 1                                                                                                             |
| Input Capacitance                                           | $C_{IN}$   | —            | 3.0  | 4.0          | pF   | Note 2                                                                                                             |
| OEN Switching On Time                                       | $t_{OEN}$  | —            | 240  | 300          | μs   | 50% OEN rise to TX ready, Note 2                                                                                   |
| OEN Switching Off Time                                      |            | —            | 0.4  | —            | μs   | 50% OEN fall to TX all output FETs on HV rails are off, Note 1                                                     |
| MODE Switching On Time                                      | $t_{MODE}$ | —            | 2    | 2.4          | μs   | 50% Mode edge to the TX logic ready. Not including $V_{PP2}/V_{NN2}$ decoupling capacitors recharging time, Note 2 |
| MODE Switching Off Time                                     |            | —            | 2    | 2.4          | μs   |                                                                                                                    |
| Thermal protection $OTP_N$ & 5UVLO                          |            |              |      |              |      |                                                                                                                    |
| $OTP_N$ Output Maximum Pull-Up                              | $V_{OH}$   | —            | —    | 5.25         | V    | —                                                                                                                  |
| $OTP_N$ Output Low Maximum Voltage                          | $V_{OL}$   | —            | 0    | 0.1          | V    | at 100 μA                                                                                                          |
|                                                             |            | —            | 0.1  | 0.4          | V    | at 4.0 mA                                                                                                          |
| $OTP_N$ Output High Current                                 | $I_{OFF}$  | —            | 0.3  | 10           | μA   | 0 to 125°C, at 5.25V pull-up, Note 1                                                                               |
| Thermal Shutdown Trip Point                                 | $T_{TRIP}$ | 126          | 142  | 158          | °C   | $OTP_N = 0$ when thermal shutdown occurs, Note 1                                                                   |
| Thermal Shutdown Hysteresis                                 | $T_{HYS}$  | —            | 48   | —            | °C   |                                                                                                                    |

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**2:** Design guidance only.

## ELECTRICAL CHARACTERISTICS (CONTINUED)

| Electrical specifications: $V_{LL} = +2.5V$ , $V_{DD} = +5.0V$ , $V_{PP0} = +80V$ , $V_{NN0} = -80V$ , $V_{PP1,2} = +60V$ , $V_{NN1,2} = -60V$ , $V_{GP} = +10V$ , $V_{GN} = -10V$ , $V_{SUB} = 0V$ , $MODE = 0$ , $OEN = REN = 1$ , $T_A = 25^{\circ}C$ . |                |                       |                       |                       |      |            |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|-----------------------|-----------------------|-----------------------|------|------------|
| Parameter                                                                                                                                                                                                                                                  | Sym.           | Min.                  | Typ.                  | Max.                  | Unit | Conditions |
| $V_{DD}$ UVLO OK Voltage                                                                                                                                                                                                                                   | $V_{DDUVON}$   | 4.0                   | 4.2                   | 4.3                   | V    | —          |
| $V_{DD}$ UVLO Trip Voltage                                                                                                                                                                                                                                 | $V_{DDUVOFF}$  | 3.7                   | 3.78                  | 3.9                   |      |            |
| $V_{LL}$ UVLO OK Voltage                                                                                                                                                                                                                                   | $V_{LLUVON}$   | 1.7                   | 1.76                  | 1.9                   |      |            |
| $V_{LL}$ UVLO Trip Voltage                                                                                                                                                                                                                                 | $V_{LLUVOFF}$  | 1.5                   | 1.62                  | 1.7                   |      |            |
| $V_{POS}$ UVLO OK Voltage                                                                                                                                                                                                                                  | $V_{POSUVON}$  | $0.7 \times V_{POS}$  | $0.8 \times V_{POS}$  | $0.9 \times V_{POS}$  | V    | Note 1     |
| $V_{POS}$ UVLO Trip Voltage                                                                                                                                                                                                                                | $V_{POSUVOFF}$ | $0.63 \times V_{POS}$ | $0.73 \times V_{POS}$ | $0.83 \times V_{POS}$ |      |            |
| $V_{NEG}$ UVLO OK Voltage                                                                                                                                                                                                                                  | $V_{NEGUON}$   | $0.7 \times V_{NEG}$  | $0.8 \times V_{NEG}$  | $0.9 \times V_{NEG}$  |      |            |
| $V_{NEG}$ UVLO Trip Voltage                                                                                                                                                                                                                                | $V_{NEGUVOFF}$ | $0.63 \times V_{NEG}$ | $0.73 \times V_{NEG}$ | $0.83 \times V_{NEG}$ |      |            |
| $V_{PF0}$ UVLO OK Voltage                                                                                                                                                                                                                                  | $V_{PF0UVON}$  | $0.7 \times V_{PF0}$  | $0.8 \times V_{PF0}$  | $0.9 \times V_{PF0}$  | V    | Note 1     |
| $V_{PF0}$ UVLO Trip Voltage                                                                                                                                                                                                                                | $V_{PF0UVOFF}$ | $0.63 \times V_{PF0}$ | $0.73 \times V_{PF0}$ | $0.83 \times V_{PF0}$ |      |            |
| $V_{NF0}$ UVLO OK Voltage                                                                                                                                                                                                                                  | $V_{NF0UVON}$  | $0.7 \times V_{NF0}$  | $0.8 \times V_{NF0}$  | $0.9 \times V_{NF0}$  |      |            |
| $V_{NF0}$ UVLO Trip Voltage                                                                                                                                                                                                                                | $V_{NF0UVOFF}$ | $0.63 \times V_{NF0}$ | $0.73 \times V_{NF0}$ | $0.83 \times V_{NF0}$ |      |            |
| $V_{PF1}$ UVLO OK Voltage                                                                                                                                                                                                                                  | $V_{PF1UVON}$  | $0.7 \times V_{PF1}$  | $0.8 \times V_{PF1}$  | $0.9 \times V_{PF1}$  | V    | Note 1     |
| $V_{PF1}$ UVLO Trip Voltage                                                                                                                                                                                                                                | $V_{PF1UVOFF}$ | $0.63 \times V_{PF1}$ | $0.73 \times V_{PF1}$ | $0.83 \times V_{PF1}$ |      |            |
| $V_{NF1}$ UVLO OK Voltage                                                                                                                                                                                                                                  | $V_{NF1UVON}$  | $0.7 \times V_{NF1}$  | $0.8 \times V_{NF1}$  | $0.9 \times V_{NF1}$  |      |            |
| $V_{NF1}$ UVLO Trip Voltage                                                                                                                                                                                                                                | $V_{NF1UVOFF}$ | $0.63 \times V_{NF1}$ | $0.73 \times V_{NF1}$ | $0.83 \times V_{NF1}$ |      |            |
| $V_{PF2}$ UVLO OK Voltage                                                                                                                                                                                                                                  | $V_{PF2UVON}$  | $0.7 \times V_{PF2}$  | $0.8 \times V_{PF2}$  | $0.9 \times V_{PF2}$  | V    | Note 1     |
| $V_{PF2}$ UVLO Trip Voltage                                                                                                                                                                                                                                | $V_{PF2UVOFF}$ | $0.63 \times V_{PF2}$ | $0.73 \times V_{PF2}$ | $0.83 \times V_{PF2}$ |      |            |
| $V_{NF2}$ UVLO OK Voltage                                                                                                                                                                                                                                  | $V_{NF2UVON}$  | $0.7 \times V_{NF2}$  | $0.8 \times V_{NF2}$  | $0.9 \times V_{NF2}$  |      |            |
| $V_{NF2}$ UVLO Trip Voltage                                                                                                                                                                                                                                | $V_{NF2UVOFF}$ | $0.63 \times V_{NF2}$ | $0.73 \times V_{NF2}$ | $0.83 \times V_{NF2}$ |      |            |

**Note 1:** Characterized only; not 100% tested in production.

**2:** Design guidance only.

## ELECTRICAL CHARACTERISTICS (CONTINUED)

**Electrical specifications:**  $V_{LL} = +2.5V$ ,  $V_{DD} = +5.0V$ ,  $V_{PP0} = +80V$ ,  $V_{NN0} = -80V$ ,  $V_{PP1,2} = +60V$ ,  $V_{NN1,2} = -60V$ ,  $V_{GP} = +10V$ ,  $V_{GN} = -10V$ ,  $V_{SUB} = 0V$ ,  $MODE = 0$ ,  $OEN = REN = 1$ ,  $T_A = 25^{\circ}C$ .

| Parameter                                                     | Sym.             | Min. | Typ. | Max. | Unit | Conditions                                                                                                                                                                                                                                                                                                                |
|---------------------------------------------------------------|------------------|------|------|------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| TX Output & Switch Timing Characteristics                     |                  |      |      |      |      |                                                                                                                                                                                                                                                                                                                           |
| Second Harmonic Distortion                                    | HD2              | —    | -40  | —    | dB   | HD2, test conditions:<br>2-waveform of 0° and 180° sin-<br>gle-cycle 5.0 MHz,<br>V <sub>PP0</sub> /V <sub>NN0</sub> = ±60V launched in<br>100 μs apart, with load of<br>220 pF//1 kΩ.<br>All these tr, tf and td values are<br>also at V <sub>PP0</sub> /V <sub>NN0</sub> = ±60V,<br>220 pF//1 kΩ, <a href="#">Note 1</a> |
| Output Rise Time<br>from 0V to V <sub>PP0</sub>               | t <sub>r1</sub>  | —    | 14   | 16.5 | ns   |                                                                                                                                                                                                                                                                                                                           |
| Output Fall Time<br>from 0V to V <sub>NN0</sub>               | t <sub>f1</sub>  | —    | 13   | 16.5 |      |                                                                                                                                                                                                                                                                                                                           |
| Output Rise Time<br>from V <sub>NN0</sub> to V <sub>PP0</sub> | t <sub>r2</sub>  | —    | 18   | 21   |      |                                                                                                                                                                                                                                                                                                                           |
| Output Fall Time from<br>V <sub>PP0</sub> to V <sub>NN0</sub> | t <sub>f2</sub>  | —    | 18   | 21   |      |                                                                                                                                                                                                                                                                                                                           |
| Output Rise Time<br>from V <sub>NN0</sub> to 0V               | t <sub>r3</sub>  | —    | 13.5 | 17   |      |                                                                                                                                                                                                                                                                                                                           |
| Output Fall Time<br>from V <sub>PP0</sub> to 0V               | t <sub>f3</sub>  | —    | 13.5 | 17   |      |                                                                                                                                                                                                                                                                                                                           |
| Propagation Delay<br>Rise Time 1                              | t <sub>dr1</sub> | —    | 18   | 21   | ns   |                                                                                                                                                                                                                                                                                                                           |
| Propagation Delay<br>Fall Time 1                              | t <sub>df1</sub> | —    | 18   | 21   |      |                                                                                                                                                                                                                                                                                                                           |
| Propagation Delay<br>Rise Time 2                              | t <sub>dr2</sub> | —    | 19   | 21.5 |      |                                                                                                                                                                                                                                                                                                                           |
| Propagation Delay<br>Fall Time 2                              | t <sub>df2</sub> | —    | 19   | 21.5 |      |                                                                                                                                                                                                                                                                                                                           |
| Propagation Delay<br>Rise Time 3                              | t <sub>dr3</sub> | —    | 18   | 21   |      |                                                                                                                                                                                                                                                                                                                           |
| Propagation Delay<br>Fall Time 3                              | t <sub>df3</sub> | —    | 18   | 21   |      |                                                                                                                                                                                                                                                                                                                           |

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**2:** Design guidance only.

## ELECTRICAL CHARACTERISTICS (CONTINUED)

| Electrical specifications: $V_{LL} = +2.5V$ , $V_{DD} = +5.0V$ , $V_{PP0} = +80V$ , $V_{NN0} = -80V$ , $V_{PP1,2} = +60V$ , $V_{NN1,2} = -60V$ , $V_{GP} = +10V$ , $V_{GN} = -10V$ , $V_{SUB} = 0V$ , $MODE = 0$ , $OEN = REN = 1$ , $T_A = 25^{\circ}C$ . |           |      |      |      |      |                                                                                                        |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|------|------|------|------|--------------------------------------------------------------------------------------------------------|
| Parameter                                                                                                                                                                                                                                                  | Sym.      | Min. | Typ. | Max. | Unit | Conditions                                                                                             |
| Output Rise Time from 0V to $V_{PP1}$                                                                                                                                                                                                                      | $t_{r4}$  | —    | 10.5 | 13   | ns   | All the tr, tf, td values, at $V_{PP1}/V_{NN1} = \pm 60V$ , 220 pF//1k $\Omega$ <a href="#">Note 1</a> |
| Output Fall Time from 0V to $V_{NN1}$                                                                                                                                                                                                                      | $t_{f4}$  | —    | 9.5  | 13   |      |                                                                                                        |
| Output Rise Time from $V_{NN1}$ to $V_{PP1}$                                                                                                                                                                                                               | $t_{r5}$  | —    | 16   | 20   |      |                                                                                                        |
| Output Fall Time from $V_{PP1}$ to $V_{NN1}$                                                                                                                                                                                                               | $t_{f5}$  | —    | 15.5 | 20   |      |                                                                                                        |
| Output Rise Time from $V_{NN1}$ to 0V                                                                                                                                                                                                                      | $t_{r6}$  | —    | 10.5 | 15   |      |                                                                                                        |
| Output Fall Time from $V_{PP1}$ to 0V                                                                                                                                                                                                                      | $t_{f6}$  | —    | 11   | 15   |      |                                                                                                        |
| Propagation Delay Rise Time 4                                                                                                                                                                                                                              | $t_{dr4}$ | —    | 19   | 21   | ns   |                                                                                                        |
| Propagation Delay Fall Time 4                                                                                                                                                                                                                              | $t_{df4}$ | —    | 18.5 | 21   |      |                                                                                                        |
| Propagation Delay Rise Time 5                                                                                                                                                                                                                              | $t_{dr5}$ | —    | 19.5 | 21.5 |      |                                                                                                        |
| Propagation Delay Fall Time 5                                                                                                                                                                                                                              | $t_{df5}$ | —    | 19.5 | 21.5 |      |                                                                                                        |
| Propagation Delay Rise Time 6                                                                                                                                                                                                                              | $t_{dr6}$ | —    | 18.5 | 21   |      |                                                                                                        |
| Propagation Delay Fall Time 6                                                                                                                                                                                                                              | $t_{df6}$ | —    | 18.5 | 21   |      |                                                                                                        |

**Note 1:** Characterized only; not 100% tested in production.

**2:** Design guidance only.

## ELECTRICAL CHARACTERISTICS (CONTINUED)

| Electrical specifications: $V_{LL} = +2.5V$ , $V_{DD} = +5.0V$ , $V_{PP0} = +80V$ , $V_{NN0} = -80V$ , $V_{PP1,2} = +60V$ , $V_{NN1,2} = -60V$ , $V_{GP} = +10V$ , $V_{GN} = -10V$ , $V_{SUB} = 0V$ , $MODE = 0$ , $OEN = REN = 1$ , $T_A = 25^\circ C$ . |                 |      |      |      |      |                                                                                                        |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|------|------|------|------|--------------------------------------------------------------------------------------------------------|
| Parameter                                                                                                                                                                                                                                                 | Sym.            | Min. | Typ. | Max. | Unit | Conditions                                                                                             |
| Output Rise Time from 0V to $V_{PP2}$                                                                                                                                                                                                                     | $t_{r7}$        | —    | 11   | 13.5 | ns   | All the tr, tf, td values, at $V_{PP2}/V_{NN2} = \pm 60V$ , 220 pF//1k $\Omega$ <a href="#">Note 1</a> |
| Output Fall Time from 0V to $V_{NN2}$                                                                                                                                                                                                                     | $t_{f7}$        | —    | 10   | 13.5 |      |                                                                                                        |
| Output Rise Time from $V_{NN2}$ to $V_{PP2}$                                                                                                                                                                                                              | $t_{r8}$        | —    | 16   | 21   |      |                                                                                                        |
| Output Fall Time from $V_{PP2}$ to $V_{NN2}$                                                                                                                                                                                                              | $t_{f8}$        | —    | 16   | 21   |      |                                                                                                        |
| Output Rise Time from $V_{NN2}$ to 0V                                                                                                                                                                                                                     | $t_{r9}$        | —    | 10.5 | 15   |      |                                                                                                        |
| Output Fall Time from $V_{PP2}$ to 0V                                                                                                                                                                                                                     | $t_{f9}$        | —    | 11   | 15   |      |                                                                                                        |
| Propagation Delay Rise Time 7                                                                                                                                                                                                                             | $t_{dr7}$       | —    | 19   | 21.5 | ns   |                                                                                                        |
| Propagation Delay Fall Time 7                                                                                                                                                                                                                             | $t_{df7}$       | —    | 18.5 | 21.5 |      |                                                                                                        |
| Propagation Delay Rise Time 8                                                                                                                                                                                                                             | $t_{dr8}$       | —    | 19.5 | 22   |      |                                                                                                        |
| Propagation Delay Fall Time 8                                                                                                                                                                                                                             | $t_{df8}$       | —    | 19.5 | 22   |      |                                                                                                        |
| Propagation Delay Rise Time 9                                                                                                                                                                                                                             | $t_{dr9}$       | —    | 18.5 | 20.5 |      |                                                                                                        |
| Propagation Delay Fall Time 9                                                                                                                                                                                                                             | $t_{df9}$       | —    | 18.5 | 20.5 |      |                                                                                                        |
| Delay Time Matching with SLB = 0, SLA = 0                                                                                                                                                                                                                 | $\Delta t_{d1}$ | —    | 0.5  | 2.5  | ns   | P to N, channel-to-channel matching in IC, <a href="#">Note 1</a>                                      |
| Delay Time Matching with SLB = 0, SLA = 1                                                                                                                                                                                                                 | $\Delta t_{d2}$ | —    | 0.5  | 2.5  | ns   |                                                                                                        |
| Delay Time Matching with SLB = 1, SLA = 0                                                                                                                                                                                                                 | $\Delta t_{d3}$ | —    | 0.5  | 2.5  | ns   |                                                                                                        |

**Note 1:** Characterized only; not 100% tested in production.

**2:** Design guidance only.

## ELECTRICAL CHARACTERISTICS (CONTINUED)

| Electrical specifications: $V_{LL} = +2.5V$ , $V_{DD} = +5.0V$ , $V_{PP0} = +80V$ , $V_{NN0} = -80V$ , $V_{PP1,2} = +60V$ , $V_{NN1,2} = -60V$ , $V_{GP} = +10V$ , $V_{GN} = -10V$ , $V_{SUB} = 0V$ , $MODE = 0$ , $OEN = REN = 1$ , $T_A = 25^{\circ}C$ . |                |              |      |              |      |                                                                                                                                           |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|--------------|------|--------------|------|-------------------------------------------------------------------------------------------------------------------------------------------|
| Parameter                                                                                                                                                                                                                                                  | Sym.           | Min.         | Typ. | Max.         | Unit | Conditions                                                                                                                                |
| RTZSW Switch On Delay Time                                                                                                                                                                                                                                 | $t_{RTZSW}$    | 95           | 106  | 120          | ns   | Note 1                                                                                                                                    |
| RTZSW Switch Off Delay Time                                                                                                                                                                                                                                |                | 95           | 108  | 120          | ns   |                                                                                                                                           |
| RX Damp Switch On Delay Time                                                                                                                                                                                                                               | $t_{RXDMP}$    | 6            | 17   | 28           | ns   |                                                                                                                                           |
| RX Damp Switch Off Delay Time                                                                                                                                                                                                                              |                | 80           | 91   | 100          | ns   |                                                                                                                                           |
| TRSW and LVSW Switch Off Delay Time                                                                                                                                                                                                                        | $t_{LVSW}$     | 135          | 160  | 185          | ns   |                                                                                                                                           |
| TRSW and LVSW Switch On Delay Time TLV<1:0> = 00                                                                                                                                                                                                           |                | 485          | 515  | 545          | ns   |                                                                                                                                           |
| TRSW and LVSW Switch On Delay Time TLV<1:0> = 01                                                                                                                                                                                                           |                | 560          | 597  | 635          | ns   |                                                                                                                                           |
| TRSW and LVSW Switch On Delay Time TLV<1:0> = 10                                                                                                                                                                                                           |                | 635          | 680  | 735          | ns   |                                                                                                                                           |
| TRSW and LVSW Switch On Delay Time TLV<1:0> = 11                                                                                                                                                                                                           |                | 715          | 763  | 815          | ns   |                                                                                                                                           |
| Output Maximum Frequency Range                                                                                                                                                                                                                             | $f_{OUT}$      | —            | 20   | 28           | MHz  | 100 $\Omega$ resistor load, Note 1                                                                                                        |
| Clock Time Low                                                                                                                                                                                                                                             | $t_{CLK\_LO}$  | 2.0          | —    | 100          | ns   | CLK input must have at least one pulse POS and NEG inputs are not zero. Inputs must be returned to zero before stopping the clock, Note 2 |
| Clock Time High                                                                                                                                                                                                                                            | $t_{CLK\_HI}$  | 2.0          | —    | 100          |      |                                                                                                                                           |
| Clock Recognition Time                                                                                                                                                                                                                                     | $t_{CLK\_REC}$ | 2.0          | —    | —            |      |                                                                                                                                           |
| Clock Release Time                                                                                                                                                                                                                                         | $t_{CLK\_RLS}$ | 200          | 430  | 600          |      |                                                                                                                                           |
| LVCMOS25 Single-Ended Clock Input, DCLKEN = 0                                                                                                                                                                                                              |                |              |      |              |      |                                                                                                                                           |
| Clock Input Frequency Range                                                                                                                                                                                                                                | $F_{CLK}$      | 10           | 160  | 180          | MHz  | Note 1                                                                                                                                    |
| Logic Input High Voltage                                                                                                                                                                                                                                   | $V_{IH}$       | 0.8 $V_{LL}$ | —    | $V_{LL}$     | V    | —                                                                                                                                         |
| Logic Input Low Voltage                                                                                                                                                                                                                                    | $V_{IL}$       | 0            | —    | 0.2 $V_{LL}$ | V    | —                                                                                                                                         |
| Clock Input Rise/fall Time                                                                                                                                                                                                                                 | $t_{rf}$       | —            | 0.5  | 5.0          | ns   | Note 2                                                                                                                                    |
| Set-up Time POS/NEG to CLK                                                                                                                                                                                                                                 | $t_{su}$       | 2.0          | —    | —            | ns   | Note 2                                                                                                                                    |
| Hold Time CLK to POS/NEG                                                                                                                                                                                                                                   | $t_H$          | 1.0          | —    | —            | ns   | Note 2                                                                                                                                    |
| Differential Clock Input, DCLKEN = 1, with Differential Clock driver's $V_{CC} = 1.8V$                                                                                                                                                                     |                |              |      |              |      |                                                                                                                                           |

**Note 1:** Characterized only; not 100% tested in production.

**2:** Design guidance only.

## ELECTRICAL CHARACTERISTICS (CONTINUED)

| <b>Electrical specifications:</b> $V_{LL} = +2.5V$ , $V_{DD} = +5.0V$ , $V_{PP0} = +80V$ , $V_{NN0} = -80V$ , $V_{PP1,2} = +60V$ , $V_{NN1,2} = -60V$ , $V_{GP} = +10V$ , $V_{GN} = -10V$ , $V_{SUB} = 0V$ , $MODE = 0$ , $OEN = REN = 1$ , $T_A = 25^{\circ}C$ . |                  |      |      |      |            |                                              |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------|------|------|------|------------|----------------------------------------------|
| Parameter                                                                                                                                                                                                                                                         | Sym.             | Min. | Typ. | Max. | Unit       | Conditions                                   |
| Clock Input Frequency Range                                                                                                                                                                                                                                       | $F_{CLK}$        | 10   | 200  | 220  | MHz        | Note 1                                       |
| Differential Sensitivity                                                                                                                                                                                                                                          | $V_{SNS}$        | 300  | 400  | —    | mVp-p      | at 160 MHz, Note 2                           |
| AC Common-Mode Voltage                                                                                                                                                                                                                                            | $V_{CMAC}$       | —    | 1.25 | —    | V          | AC coupled, Note 2                           |
| DC Common-Mode Voltage                                                                                                                                                                                                                                            | $V_{CMDC}$       | 1.0  | —    | 1.4  | V          | DC coupled, Note 2                           |
| CLK Input Offset Voltage                                                                                                                                                                                                                                          | $V_{OFFSET}$     | —    | 37   | —    | mV         | Note 2                                       |
| CLK Input Differential Resistance                                                                                                                                                                                                                                 | $R_{IN\_CLK}$    | —    | 21   | —    | k $\Omega$ | Note 2                                       |
| CLK Input Common Resistance                                                                                                                                                                                                                                       |                  | —    | 4.8  | —    | k $\Omega$ | Note 2                                       |
| CLK Input Capacitance                                                                                                                                                                                                                                             | $C_{IN\_CLK}$    | —    | 4.0  | —    | pF         | Note 2                                       |
| <b>TRSW &amp; RXDMP Switching Spike Voltages</b>                                                                                                                                                                                                                  |                  |      |      |      |            |                                              |
| TRSW Turn On Spike Voltage at TX Pins                                                                                                                                                                                                                             | $V_{TRSW\_ON}$   | —    | 130  | 150  | mVp-p      | $TX_{(ch)}$ 50 $\Omega$ load to GND, Note 2  |
| TRSW Turn Off Spike Voltage at TX Pins                                                                                                                                                                                                                            | $V_{TRSW\_OFF}$  | —    | 130  | 150  |            |                                              |
| RXDMP Turn On Spike Voltage at RX Pins                                                                                                                                                                                                                            | $V_{RXDMP\_ON}$  | —    | 130  | 150  |            | $RX_{(ch)}$ 300 $\Omega$ load to GND, Note 2 |
| RXDMP Turn Off Spike Voltage at RX Pins                                                                                                                                                                                                                           | $V_{RXDMP\_OFF}$ | —    | 130  | 150  |            |                                              |

**Note 1:** Characterized only; not 100% tested in production.

**2:** Design guidance only.

## TEMPERATURE CHARACTERISTICS

| Unless otherwise indicated, all parameters apply with $V_{LL} = +2.5V$ , $V_{DD} = +5.0V$ , $V_{PP0} = +80V$ , $V_{NN0} = -80V$ , $V_{PP1,2} = +60V$ , $V_{NN1,2} = -60V$ , $V_{GP} = +10V$ , $V_{GN} = -10V$ , $V_{SUB} = 0V$ , $OEN = REN = 1$ |               |      |      |      |               |            |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|------|------|------|---------------|------------|
| Parameters                                                                                                                                                                                                                                       | Sym.          | Min. | Typ. | Max. | Units         | Conditions |
| <b>Temperature Ranges</b>                                                                                                                                                                                                                        |               |      |      |      |               |            |
| Operating Ambient Temperature Range                                                                                                                                                                                                              | $T_A$         | 0    | —    | 85   | $^{\circ}C$   | —          |
| Storage Temperature Range                                                                                                                                                                                                                        | $T_S$         | -55  | —    | 150  | $^{\circ}C$   | —          |
| Maximum Junction Temperature                                                                                                                                                                                                                     | $T_J$         | —    | —    | 130  | $^{\circ}C$   | —          |
| <b>Thermal Package Resistances (206L 12 mm x 12 mm TFBGA)</b>                                                                                                                                                                                    |               |      |      |      |               |            |
| Junction-to-Ambient Thermal Resistance                                                                                                                                                                                                           | $\theta_{JA}$ | —    | 16   | —    | $^{\circ}C/W$ | —          |
| Junction-to-Board Thermal Resistance                                                                                                                                                                                                             | $\theta_{JB}$ | —    | 3.5  | —    | $^{\circ}C/W$ | —          |
| Junction-to-Case Top Thermal Resistance                                                                                                                                                                                                          | $\theta_{JC}$ | —    | 2.0  | —    | $^{\circ}C/W$ | —          |

**TABLE 1-1: INPUT OUTPUT LOGIC TRUTH TABLE**

| Function                         | OTP <sub>N</sub> | Logic Inputs (No-Re-timing) |      |      |     |     |     |     | Tx Output        | RTZSW & TRSW | LVSW | RXDMP |
|----------------------------------|------------------|-----------------------------|------|------|-----|-----|-----|-----|------------------|--------------|------|-------|
|                                  |                  | OEN                         | MODE | CWEN | SLB | SLA | NEG | POS |                  |              |      |       |
| 7-Level Mode <sup>(1)</sup>      | 1                | 1                           | 0    | 0    | 0   | 0   | 0   | 0   | RTZ              | OFF          | OFF  | ON    |
|                                  | 1                | 1                           | 0    | 0    | 0   | 0   | 0   | 1   | V <sub>PP0</sub> | OFF          | OFF  | ON    |
|                                  | 1                | 1                           | 0    | 0    | 0   | 0   | 1   | 0   | V <sub>NN0</sub> | OFF          | OFF  | ON    |
|                                  | 1                | 1                           | 0    | 0    | 0   | 0   | 1   | 1   | RTZ+             | ON           | ON   | OFF   |
|                                  | 1                | 1                           | 0    | 0    | 0   | 1   | 0   | 0   | RTZ              | OFF          | OFF  | ON    |
|                                  | 1                | 1                           | 0    | 0    | 0   | 1   | 0   | 1   | V <sub>PP1</sub> | OFF          | OFF  | ON    |
|                                  | 1                | 1                           | 0    | 0    | 0   | 1   | 1   | 0   | V <sub>NN1</sub> | OFF          | OFF  | ON    |
|                                  | 1                | 1                           | 0    | 0    | 0   | 1   | 1   | 1   | Hi-Z             | OFF          | OFF  | ON    |
|                                  | 1                | 1                           | 0    | 0    | 1   | 0   | 0   | 0   | RTZ              | OFF          | OFF  | ON    |
|                                  | 1                | 1                           | 0    | 0    | 1   | 0   | 0   | 1   | V <sub>PP2</sub> | OFF          | OFF  | ON    |
|                                  | 1                | 1                           | 0    | 0    | 1   | 0   | 1   | 0   | V <sub>NN2</sub> | OFF          | OFF  | ON    |
|                                  | 1                | 1                           | 0    | 0    | 1   | 0   | 1   | 1   | RTZ+             | ON           | ON   | OFF   |
|                                  | 1                | 1                           | 0    | 0    | 1   | 1   | 0   | 0   | RTZ              | OFF          | OFF  | ON    |
|                                  | 1                | 1                           | 0    | 0    | 1   | 1   | 0   | 1   | V <sub>PP2</sub> | OFF          | OFF  | ON    |
|                                  | 1                | 1                           | 0    | 0    | 1   | 1   | 1   | 0   | V <sub>NN2</sub> | OFF          | OFF  | ON    |
|                                  | 1                | 1                           | 0    | 0    | 1   | 1   | 1   | 1   | RTZ+             | ON           | ON   | OFF   |
| True 5-Level Mode <sup>(1)</sup> | 1                | 1                           | 1    | 0    | 0   | 0   | 0   | 0   | RTZ              | OFF          | OFF  | ON    |
|                                  | 1                | 1                           | 1    | 0    | 0   | 0   | 0   | 1   | V <sub>PP0</sub> | OFF          | OFF  | ON    |
|                                  | 1                | 1                           | 1    | 0    | 0   | 0   | 1   | 0   | V <sub>NN0</sub> | OFF          | OFF  | ON    |
|                                  | 1                | 1                           | 1    | 0    | 0   | 0   | 1   | 1   | RTZ+             | ON           | ON   | OFF   |
|                                  | 1                | 1                           | 1    | 0    | 0   | 1   | 0   | 0   | RTZ              | OFF          | OFF  | ON    |
|                                  | 1                | 1                           | 1    | 0    | 0   | 1   | 0   | 1   | V <sub>PP1</sub> | OFF          | OFF  | ON    |
|                                  | 1                | 1                           | 1    | 0    | 0   | 1   | 1   | 0   | V <sub>NN1</sub> | OFF          | OFF  | ON    |
|                                  | 1                | 1                           | 1    | 0    | 0   | 1   | 1   | 1   | Hi-Z             | OFF          | OFF  | ON    |
|                                  | 1                | 1                           | 1    | 0    | 1   | 0   | 0   | 0   | Hi-Z             | OFF          | OFF  | ON    |
|                                  | 1                | 1                           | 1    | 0    | 1   | 0   | 1   | 0   |                  |              |      |       |
|                                  | 1                | 1                           | 1    | 0    | 1   | 0   | 1   | 1   |                  |              |      |       |
|                                  | 1                | 1                           | 1    | 0    | 1   | 1   | 0   | 0   |                  |              |      |       |
|                                  | 1                | 1                           | 1    | 0    | 1   | 1   | 1   | 0   |                  |              |      |       |
|                                  | 1                | 1                           | 1    | 0    | 1   | 1   | 1   | 1   |                  |              |      |       |
| Not Recommended                  | 1                | 1                           | x    | 1    | 0   | 0   | 0   | 0   | RTZ              | OFF          | OFF  | ON    |
|                                  | 1                | 1                           | x    | 1    | 0   | 0   | 0   | 1   | V <sub>PP0</sub> | OFF          | OFF  | ON    |
|                                  | 1                | 1                           | x    | 1    | 0   | 0   | 1   | 0   | V <sub>NN0</sub> | OFF          | OFF  | ON    |
|                                  | 1                | 1                           | x    | 1    | 0   | 0   | 1   | 1   | RTZ+             | ON           | ON   | OFF   |

- Note 1:** In B-Mode, the low-duty cycle must be used, due to the IC power dissipation limit.
- Note 2:** In CW-Mode, the MOSFET transistors of V<sub>PP1</sub>/V<sub>NN1</sub> voltage must be ≤±8V. Nothing other than SLB = 0 and SLA = 1 logic input status listed in above table should be used, due to the power dissipation limit.
- Note 3:** When the TX output is in RTZ+ state, the channel is in receiving mode (RTZ+).
- Note 4:** When the TX output is in Hi-Z state, all output MOSFET transistors are OFF.
- Note 5:** In the Re-Timing mode, SLA, SLB, NEG and POS inputs are latched-in at CLKP rising edge. The single-ended clock or the CLKP and CLKN are crossing points if the re-timing clock inputs are in differential configuration.

**TABLE 1-1: INPUT OUTPUT LOGIC TRUTH TABLE (CONTINUED)**

| Function                     | OTP <sub>N</sub> | Logic Inputs (No-Re-timing) |      |      |     |     |     |     | Tx Output        | RTZSW & TRSW | LVSW | RXDMP |
|------------------------------|------------------|-----------------------------|------|------|-----|-----|-----|-----|------------------|--------------|------|-------|
|                              |                  | OEN                         | MODE | CWEN | SLB | SLA | NEG | POS |                  |              |      |       |
| CW-Mode <sup>(2)</sup>       | 1                | 1                           | x    | 1    | 0   | 1   | 0   | 0   | RTZ              | OFF          | OFF  | ON    |
|                              | 1                | 1                           | x    | 1    | 0   | 1   | 0   | 1   | V <sub>PP1</sub> | OFF          | OFF  | ON    |
|                              | 1                | 1                           | x    | 1    | 0   | 1   | 1   | 0   | V <sub>NN1</sub> | OFF          | OFF  | ON    |
|                              | 1                | 1                           | x    | 1    | 0   | 1   | 1   | 1   | Hi-Z             | OFF          | OFF  | ON    |
| Not Recommended              | 1                | 1                           | x    | 1    | 1   | 0   | 0   | 0   | RTZ              | OFF          | OFF  | ON    |
|                              | 1                | 1                           | x    | 1    | 1   | 0   | 0   | 1   | V <sub>PP2</sub> | OFF          | OFF  | ON    |
|                              | 1                | 1                           | x    | 1    | 1   | 0   | 1   | 0   | V <sub>NN2</sub> | OFF          | OFF  | ON    |
|                              | 1                | 1                           | x    | 1    | 1   | 0   | 1   | 1   | RTZ+             | ON           | ON   | OFF   |
|                              | 1                | 1                           | x    | 1    | 1   | 1   | 0   | 0   | RTZ              | OFF          | OFF  | ON    |
|                              | 1                | 1                           | x    | 1    | 1   | 1   | 0   | 1   | V <sub>PP2</sub> | OFF          | OFF  | ON    |
|                              | 1                | 1                           | x    | 1    | 1   | 1   | 1   | 0   | V <sub>NN2</sub> | OFF          | OFF  | ON    |
|                              | 1                | 1                           | x    | 1    | 1   | 1   | 1   | 1   | RTZ+             | ON           | ON   | OFF   |
| Device Disabled              | x                | 0                           | x    | x    | x   | x   | x   | x   | Hi-Z             | OFF          | OFF  | ON    |
| Thermal Protection Activated | 0                | x                           | x    | x    | x   | x   | x   | x   | Hi-Z             | OFF          | OFF  | ON    |

- Note 1:** In B-Mode, the low-duty cycle must be used, due to the IC power dissipation limit.
- 2:** In CW-Mode, the MOSFET transistors of V<sub>PP1</sub>/V<sub>NN1</sub> voltage must be  $\leq \pm 8V$ . Nothing other than SLB = 0 and SLA = 1 logic input status listed in above table should be used, due to the power dissipation limit.
- 3:** When the TX output is in RTZ+ state, the channel is in receiving mode (RTZ+).
- 4:** When the TX output is in Hi-Z state, all output MOSFET transistors are OFF.
- 5:** In the Re-Timing mode, SLA, SLB, NEG and POS inputs are latched-in at CLKP rising edge. The single-ended clock or the CLKP and CLKN are crossing points if the re-timing clock inputs are in differential configuration.

## 1.1 Typical Timing Diagrams

Figure 1-1 displays the logic inputs of the TX output timing-delay and the TX high-voltage pulses output slew-rates timing parameters of the HV7322 device.

Figure 1-2 displays the logic inputs of the RTZSW, TRSW and RXDMP switches timing-delay parameters of the HV7322 device.

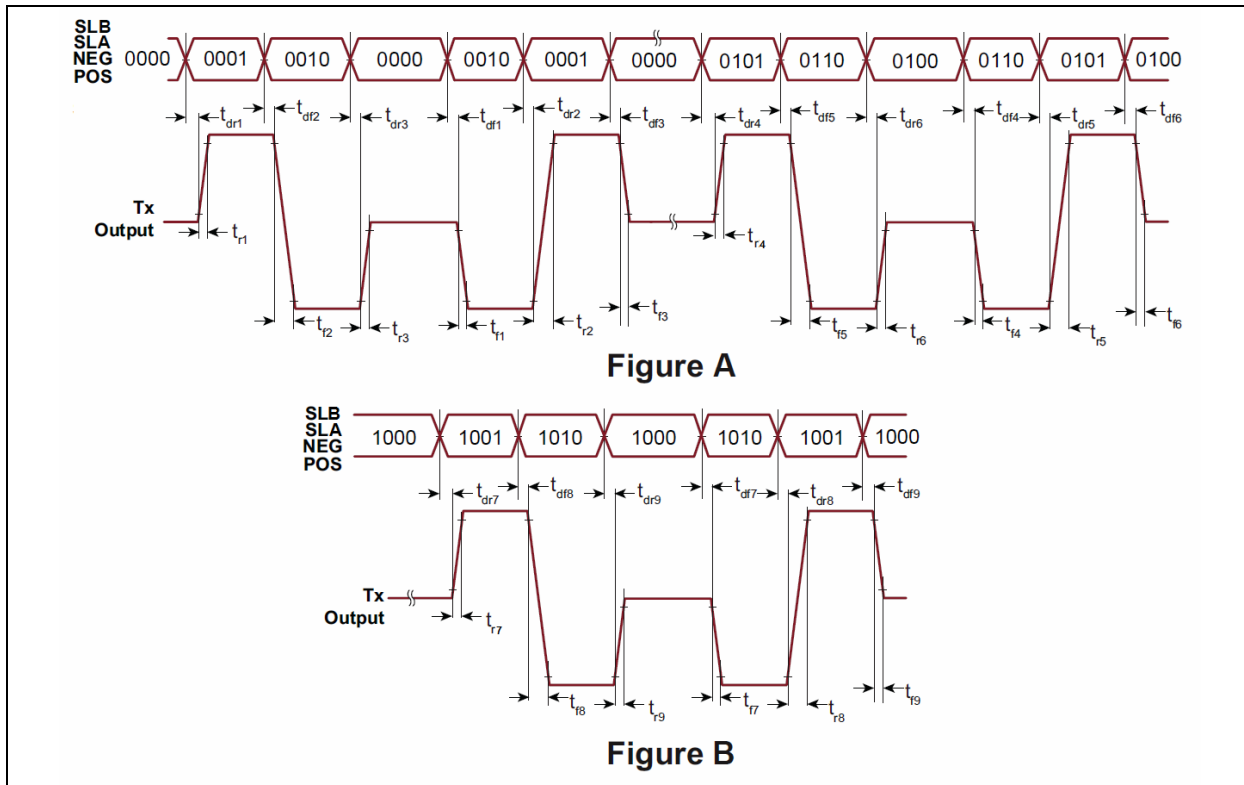


**FIGURE 1-1:** Logic Input and TX Output Timing Diagram.

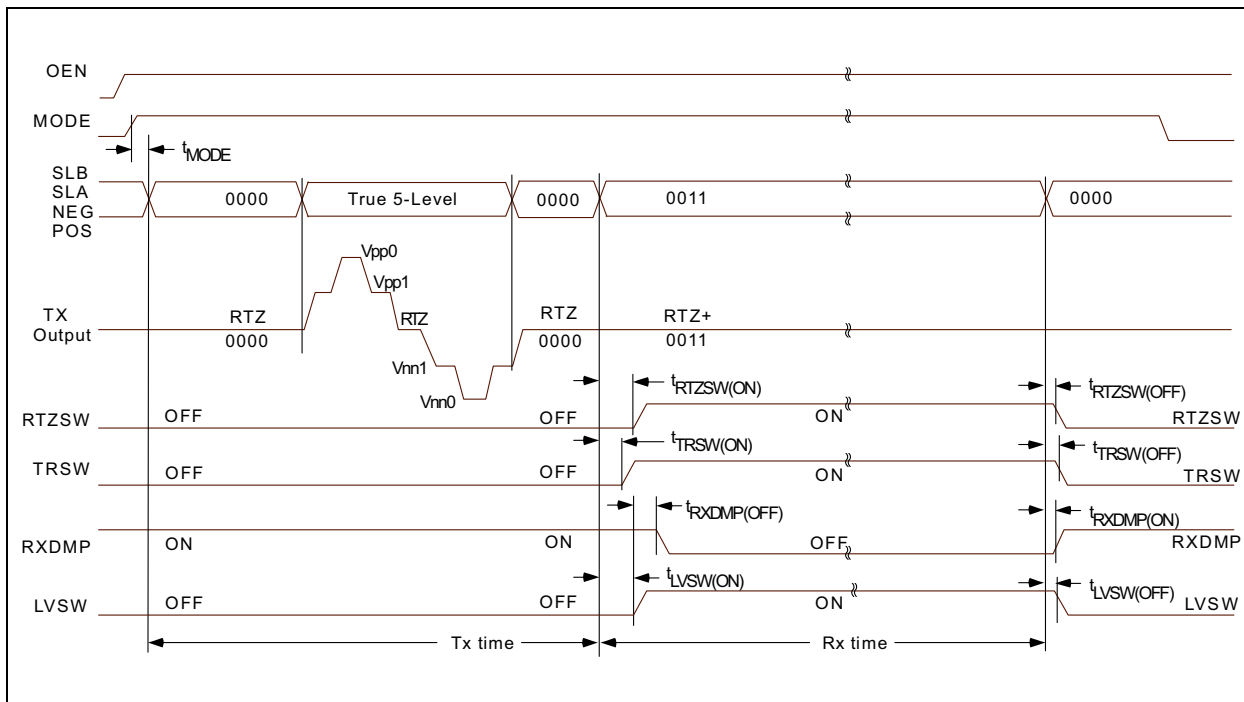


**FIGURE 1-2:** True 5-Level TX and Switches Timing Diagram (CWEN = 0).

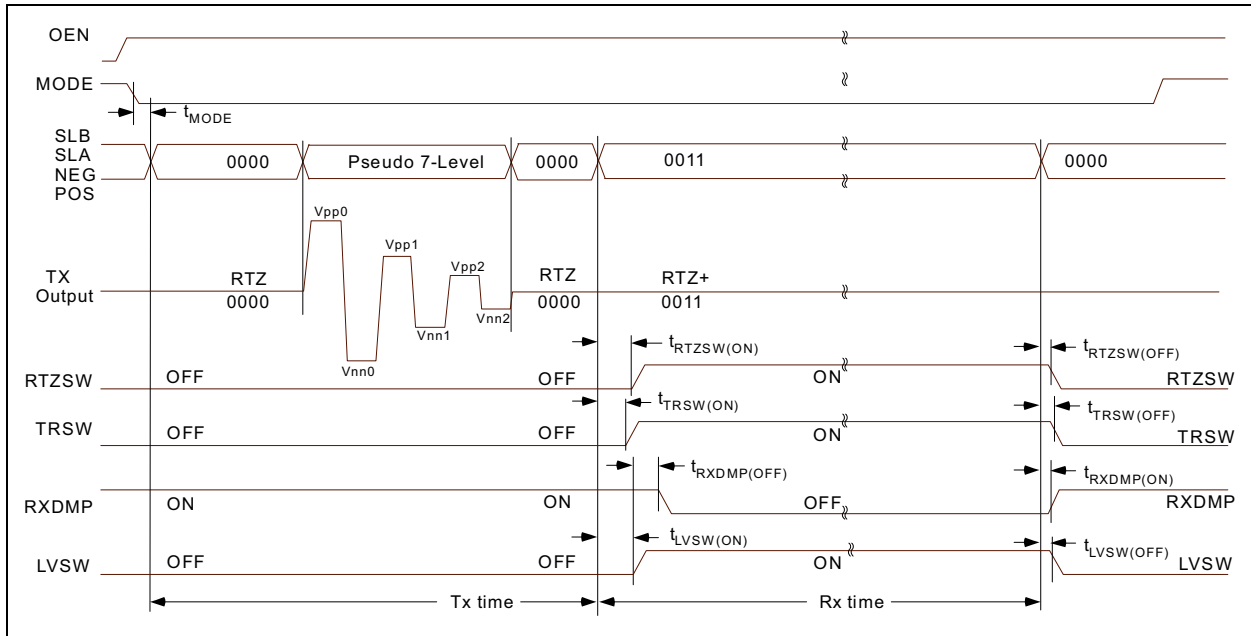


**FIGURE 1-3:** 7-Level TX and Switches Timing Diagram ( $CWEN = 0$ ).

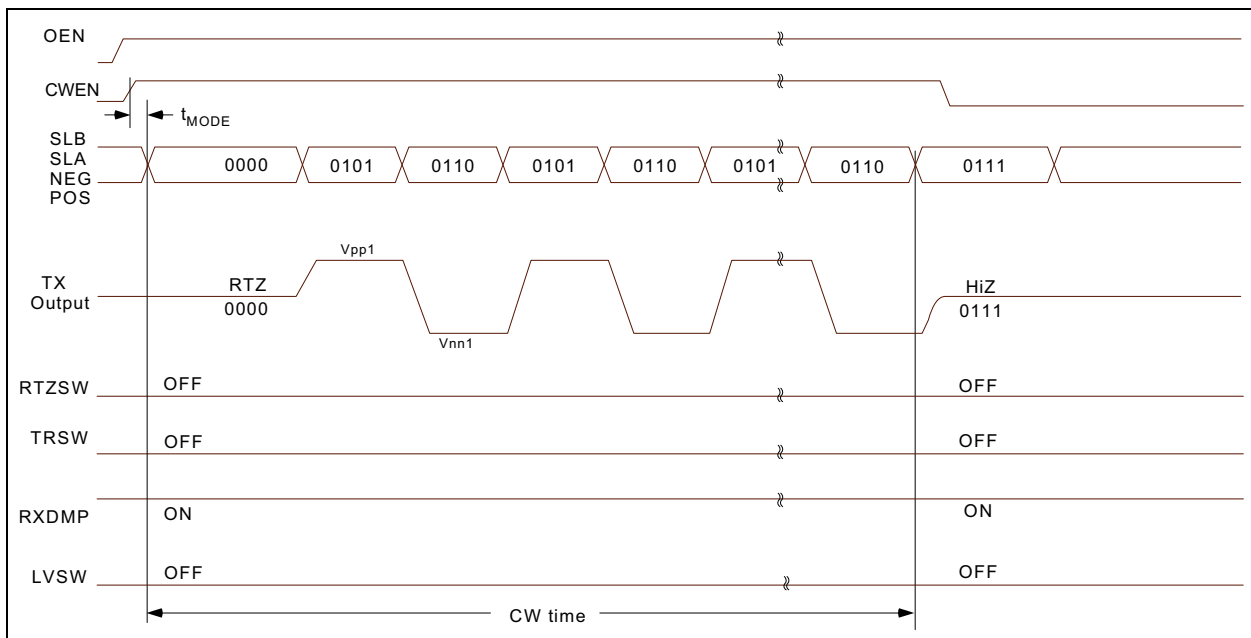


**FIGURE 1-4:** CW TX Waveform Timing Diagram ( $CWEN = 1$ ).

## 2.0 TYPICAL PERFORMANCE CURVES

**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

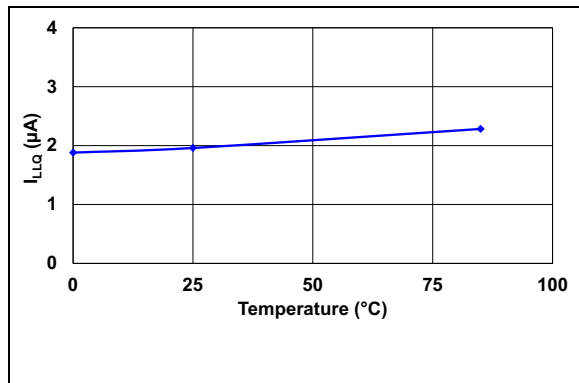


**FIGURE 2-1:**  $I_{LLQ}$  vs. Temperature.

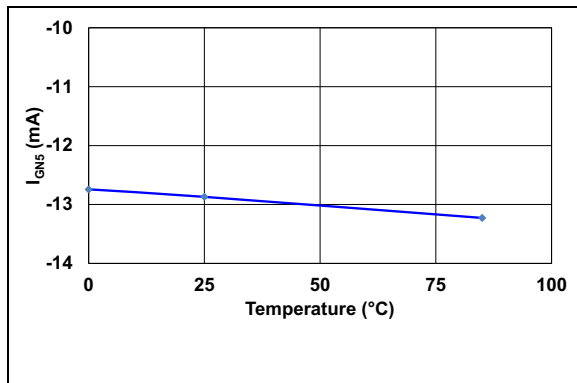


**FIGURE 2-4:**  $I_{GN5}$  vs. Temperature.

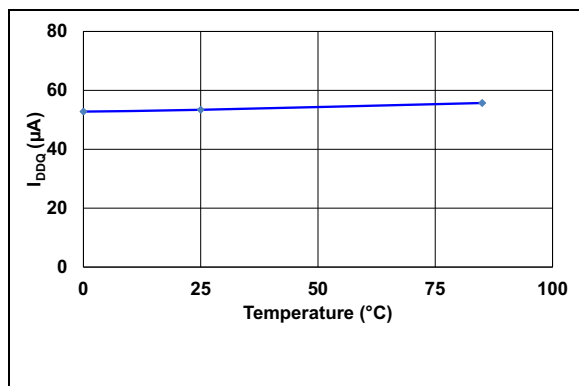


**FIGURE 2-2:**  $I_{DDQ}$  vs. Temperature.

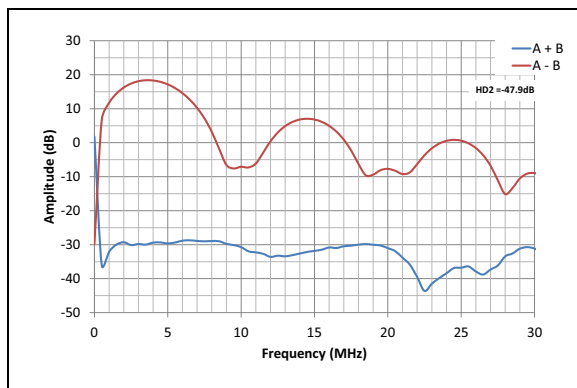


**FIGURE 2-5:** TX Output Pulse Cancellation FFT, using  $V_{NN0}$  and  $V_{PP0}$ , 1-Cycle 5 MHz with 220 pF//1 kΩ Load.

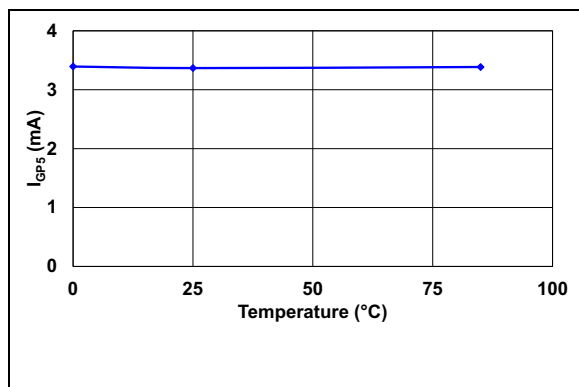


**FIGURE 2-3:**  $I_{GP5}$  vs. Temperature.

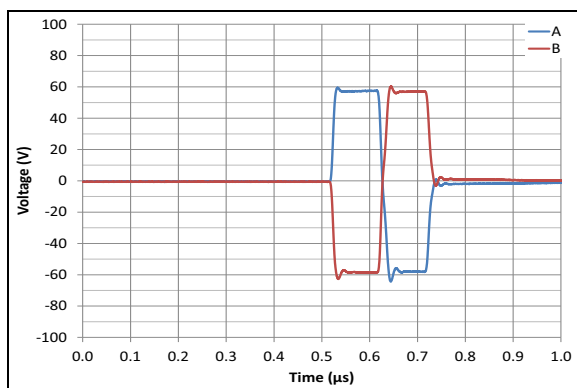


**FIGURE 2-6:** TX Output Pulse Cancellation, using  $V_{NN0}$  and  $V_{PP0}$ , 1-Cycle 5 MHz with 220 pF//1 kΩ Load.

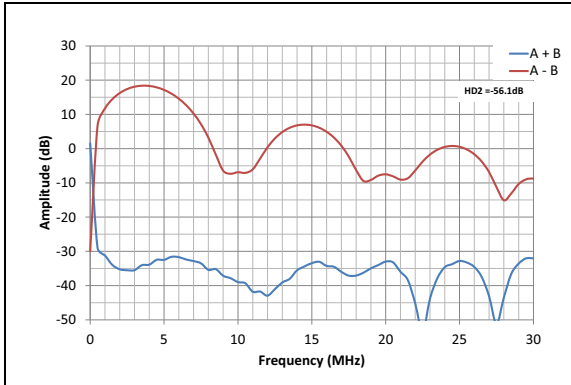


**FIGURE 2-7:** TX Output Pulse Cancellation FFT, using  $V_{NN1}$  and  $V_{PP1}$ , 1-Cycle 5 MHz with 220 pF/1 k $\Omega$  Load.

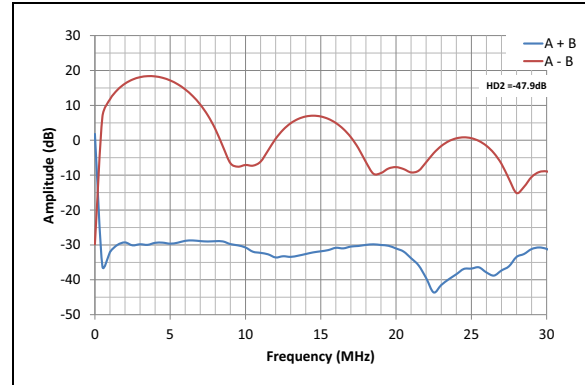


**FIGURE 2-9:** TX Output Pulse Cancellation FFT, using  $V_{NN2}$  and  $V_{PP2}$ , 1-Cycle 5 MHz with 220 pF/1 k $\Omega$  Load.

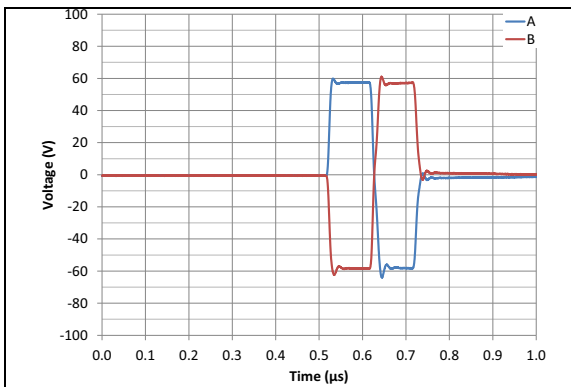


**FIGURE 2-8:** TX Output Pulse Cancellation, using  $V_{NN1}$  and  $V_{PP1}$ , 1-Cycle 5 MHz with 220 pF/1 k $\Omega$  Load.

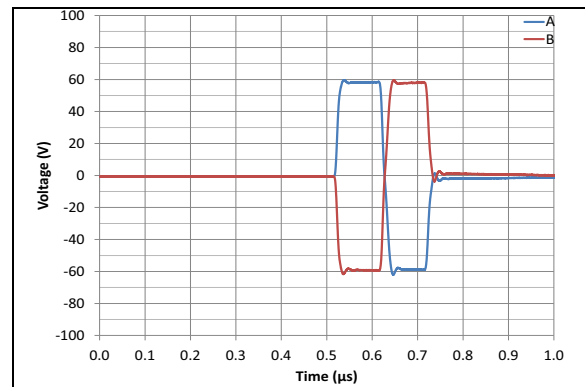


**FIGURE 2-10:** TX Output Pulse Cancellation, using  $V_{NN2}$  and  $V_{PP2}$ , 1-Cycle 5 MHz with 220 pF/1 k $\Omega$  Load.

NOTES:

## 3.0 PIN DESCRIPTIONS

Table 3-1 lists the descriptions of the pins.

**TABLE 3-1: PIN FUNCTION TABLE**

| Pin                                                        | Symbol           | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|------------------------------------------------------------|------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| A4, B2, D2, F2, N2, R2, U2, V4                             | SLA<0:7>         | Selects $V_{PP0}/V_{NN0}$ or $V_{PP1}/V_{NN1}$ high-voltage rails. See Table 1-1.                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| A5, C2, E2, G2, M2, P2, T2, V5                             | SLB<0:7>         | Selects $V_{PP2}/V_{NN2}$ high-voltage rails. See Table 1-1.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| A3, C1, E1, G1, M1, P1, T1, V3                             | NEG<0:7>         | Turns ON and OFF the corresponding output N-channel MOSFET. See Table 1-1.                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| A2, B1, D1, F1, N1, R1, U1, V2                             | POS<0:7>         | Turns ON and OFF the corresponding output P-channel MOSFET. See Table 1-1.                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| L1                                                         | DCLKEN           | Logic input pin. When DCLKEN = 1, the CLKP/CLKN is set as Differential Clock type of inputs. When DCLKEN = 0, the CLKP/CLKN is set as LVCMOS single-ended clock input. Turning ON the Differential Clock function will result in the device consuming more power on $V_{LL}$ .                                                                                                                                                                                                                                                                  |
| H1                                                         | OEN              | Output enable logic input pin. When OEN = $V_{LL}$ , the transmitter outputs are enabled. When OEN = 0, the transmitter outputs are disabled.                                                                                                                                                                                                                                                                                                                                                                                                   |
| U3, U4                                                     | IM<1:0>          | Logic input pins for $V_{PP1}/V_{NN1}$ output current, for all channels.                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| U5                                                         | CWEN             | Logic input pins for TX mode control. CWEN = 0 B-Mode, CWEN = 1 CWD Mode.                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| B3, B4                                                     | TLV<1:0>         | Logic input pins for $t_{LVS\overline{W}(ON)}$ delay time selecting, for all channels.                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| J1, K1                                                     | CLKP<br>CLKN     | Differential/LVCMOS input clock. The inputs POS, NEG, SLA and SLB are aligned to the rising edge of the CLKP input clock signal.<br>When the CLKP input is driven by LVCMOS, CLKN = DCLKEN = 0 permanently.<br>When CLKP = CLKN = 0, the synchronization function is set to OFF and the internal retiming registers is bypassed.<br>When DCLKEN = 1, CLKP/CLKN is internally self-biased and is be driven differentially through AC couples. An 100 $\Omega$ Differential line termination resistor needs to be connected between the two pins. |
| A1, E5, F5, G5, H4, H5, J4, J5, K4, K5, L5, M5, N5, P5, V1 | GND              | Ground, 0V, input logic reference is low and the return ground of $V_{LL}$ and $V_{DD}$ .                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| J2                                                         | $V_{LL}$         | Input logic power supply pin.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| H2                                                         | REN              | Enable pin for the built-in voltage regulators. When REN = $V_{LL}$ , all the regulators are ON. When REN = 0, all the regulator are OFF.                                                                                                                                                                                                                                                                                                                                                                                                       |
| B5                                                         | OTP <sub>N</sub> | Temperature sensor open drain output.<br>When OTP <sub>N</sub> = 0, the over temperature is detected. When the over temperature is detected, all outputs are in Hi-Z state, regardless of the input logic control.                                                                                                                                                                                                                                                                                                                              |
| A6, V6                                                     | $V_{DD}$         | Level translator supply voltage, +5V, bypass capacitor, 2 $\mu$ F, 10V to GND per pin.                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| B6                                                         | $V_{GN}$         | –10V supply pin for the linear regulator.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| U6                                                         | $V_{GP}$         | +10V supply pin for the linear regulator.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| A13, B13, E12, F12, J12, K12, N12, P12, U13, V13           | $V_{PP0}$        | Positive high-voltage supply pin. $V_{PP0}$ must be equal to or more positive than $V_{PP1}$ or $V_{PP2}$ .                                                                                                                                                                                                                                                                                                                                                                                                                                     |

**TABLE 3-1: PIN FUNCTION TABLE (CONTINUED)**

| Pin                                                          | Symbol    | Description                                                                                                                                                                                                                                                                                                     |
|--------------------------------------------------------------|-----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| A14, E13,<br>P13, K13,<br>J13, V14                           | $C_{PF0}$ | Internal linear regulator output pin. Connects the 2 $\mu$ F, 10V capacitor to $V_{PP0}$ .                                                                                                                                                                                                                      |
| A15, B15,<br>E14, F14,<br>J14, K14,<br>N14, P14,<br>U15, V15 | $V_{NN0}$ | Negative high-voltage supply pin. $V_{NN0}$ must be equal to or more negative than $V_{NN1}$ or $V_{NN2}$ .                                                                                                                                                                                                     |
| B14, F13,<br>N13, U14                                        | $C_{NF0}$ | Internal linear regulator output pin. Connects the 2 $\mu$ F, 10V capacitor to $V_{NN0}$ .                                                                                                                                                                                                                      |
| A12, B12,<br>E11, F11,<br>J11, K11,<br>N11, P11,<br>U12, V12 | $V_{PP1}$ | Positive high-voltage supply. $V_{PP1}$ must be equal to or lower than $V_{PP0}$ and +60V.                                                                                                                                                                                                                      |
| A11, E10,<br>J10, K10,<br>P10, V11                           | $C_{PF1}$ | Internal $V_{PF1}$ gate drive voltage linear regulator output bypass capacitor. Connects 2 $\mu$ F, 10V capacitor to $V_{PP1}$ .                                                                                                                                                                                |
| A10, B10,<br>E9, F9, J9,<br>K9, N9, P9,<br>U10, V10          | $V_{NN1}$ | Negative high-voltage supply pin. $V_{NN1}$ must be equal to or less negative than $V_{NN0}$ and -60V.                                                                                                                                                                                                          |
| B11, F10,<br>N10, U11                                        | $C_{NF1}$ | Internal $V_{NF1}$ gate drive voltage linear regulator output bypass capacitor. Connects 2 $\mu$ F, 10V capacitor to $V_{NN1}$ .                                                                                                                                                                                |
| A7, B7, E6,<br>F6, J6, K6,<br>N6, P6, U7,<br>V7              | $V_{PP2}$ | Positive or negative high-voltage supply. When the device is configured as pseudo 7-level pulsers, $V_{PP2}$ voltage should be equal to or less positive than $V_{PP0}$ and +60V. When the device is configured as true 5-level pulsers, the $V_{PP2}$ voltage should always be the same voltage as $V_{NN1}$ . |
| A9, B9, E8,<br>F8, J8, K8,<br>N8, P8, U9,<br>V9              | $V_{NN2}$ | Negative or positive high-voltage supply. When the device is configured as pseudo 7-level pulser, $V_{NN2}$ voltage should be equal to or less negative than $V_{NN0}$ and -60V. When the device is configured as true 5-level pulser, $V_{NN2}$ voltage should always be the same voltage as $V_{PP1}$ .       |
| A8, E7, J7,<br>P7, V8, K7                                    | $C_{PF2}$ | Internal $V_{PF2}$ gate drive voltage linear regulator output bypass capacitor. Connects the 2 $\mu$ F, 10V capacitor to $V_{PP2}$ .                                                                                                                                                                            |
| B8, F7, N7,<br>U8                                            | $C_{NF2}$ | Internal $V_{NF2}$ gate drive voltage linear regulator output bypass capacitor. Connects the 2 $\mu$ F, 10V capacitor to $V_{NN2}$ .                                                                                                                                                                            |
| A16, E15,<br>J15, K15,<br>P15, V16                           | $C_{NEG}$ | Internal $V_{NEG}$ gate drive voltage linear regulator output bypass capacitor. Connects the 2 $\mu$ F, 10V capacitor to GND.                                                                                                                                                                                   |
| B16, F15,<br>N15, U16                                        | $C_{POS}$ | Internal $V_{POS}$ gate drive voltage linear regulator output bypass capacitor. Connects the 2 $\mu$ F, 10V capacitor to GND.                                                                                                                                                                                   |
| U18, R18,<br>N18, L18,<br>H18, F18,<br>D18, B18              | TX<7:0>   | High-voltage pulser B-Mode and CW output of the Ch<7:0>.                                                                                                                                                                                                                                                        |
| T17, P17,<br>M17, K17,<br>J17, G17,<br>E17, C17              | RX<7:0>   | T/R switch output of the Ch<7:0>.                                                                                                                                                                                                                                                                               |

**TABLE 3-1: PIN FUNCTION TABLE (CONTINUED)**

| Pin                                                                                                              | Symbol            | Description                                                                                                             |
|------------------------------------------------------------------------------------------------------------------|-------------------|-------------------------------------------------------------------------------------------------------------------------|
| A17, A18,<br>B17, C18,<br>D17, E18,<br>F17, G18,<br>H17, L17,<br>M18, N17,<br>P18, R17,<br>T18, U17,<br>V17, V18 | $R_{GND}$         | Output power grounds.                                                                                                   |
| F4, G4, L4,<br>M4, N4                                                                                            | NC                | Do-Not-Connect for user application.                                                                                    |
| L2                                                                                                               | MODE              | Logic input pin for mode selection. If MODE = 0, IC is in Pseudo 7-Level Mode. If MODE = 1, IC is in True 5-Level Mode. |
| J18, K18                                                                                                         | GND ( $V_{SUB}$ ) | $V_{SUB}$ pins must be connected to GND (0V).                                                                           |

NOTES:

## 4.0 DEVICE DESCRIPTION

### 4.1 Overview

The HV7322 device is a 8-channel, true 5-level, pseudo 7-level ultrasound transmitter with built-in T/R switches, output protection diodes and clamp diodes.

HV7322 can provide up to  $\pm 2.0A$  and the output voltage swing can be up to  $\pm 80V$ .

HV7322 supports both Transparent and Re-Timing mode. The retiming clock frequency can support up to 220 MHz. The retiming feature helps reduce the output jitter introduced by the driving FPGA.g

### 4.2 Recommended Power-Up Sequence

Powering up and down in any arbitrary sequence will not cause any damage to the device. The powering up sequences in Table 4-1 are only recommended in order to minimize possible in-rush current. Figure 4-1 shows the timing diagram of related signals.

**TABLE 4-1: POWER-UP SEQUENCE**

| Step | Power-Up Description                            |
|------|-------------------------------------------------|
| 1    | $V_{LL}$ ON with logic signal low               |
| 2    | $V_{DD}$ , $V_{GP}$ and $V_{GN}$ ON             |
| 3    | REN = Logic - 1                                 |
| 4    | $V_{PP0,1,2}$ and $V_{NN0,1,2}$ ON              |
| 5    | OEN = Logic - 1 and Logic control signal active |

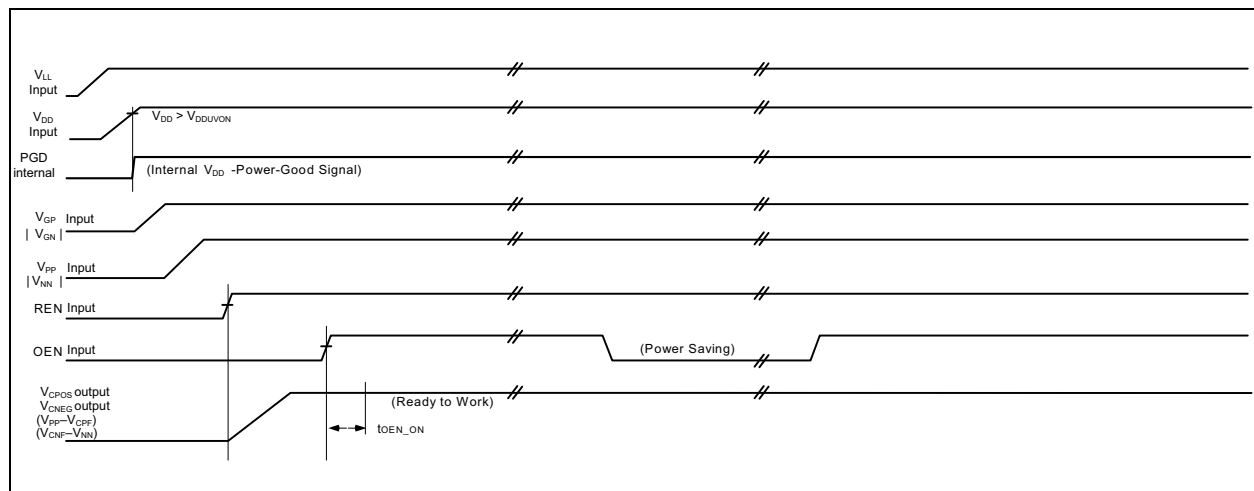


**FIGURE 4-1:** Power-On Events and Power-Saving Time Diagram.

### 4.3 Operation Modes

There are four modes of operation: Device Disabled, Output Disabled, Pulsed-Echo Mode and CW-Mode.

#### 4.3.1 DEVICE DISABLED MODE

In the Device Disabled mode, the regulators are turned off when REN is low. The regulators are ON when REN = Logic - 1. When REN is low, OEN = X (OEN = Logic - 1 or Logic - 0), since the device is disabled. Table 4-2 shows the REN and the OEN logic inputs.

#### 4.3.2 OUTPUT DISABLED MODE

In the Output Disabled mode, regulators are enabled. REN = Logic - 1 and OEN = Logic - 0 (Output Enable logic input) and output pins(TX0-7) are in Hi-Z state. OEN = Logic - 1 enables the outputs.

**TABLE 4-2: REN & OEN LOGIC INPUTS**

| REN | OEN | Device   | TX Outputs |
|-----|-----|----------|------------|
| 0   | X   | Disabled | Hi-Z       |
| 1   | 0   | Enabled  | Hi-Z       |
| 1   | 1   | Enabled  | ON         |

#### 4.3.3 PULSE-ECHO (B) MODE

Pulse-Echo mode (B-Mode) enables the true 5-level or pseudo 7-level waveform generation. MODE = Logic - 1 enables the true 5-level outputs. When OEN = Logic - 1, REN = Logic - 1, and CWEN = Logic - 0, the Pulse-Echo mode is enabled after the HV7322 device is powered on. The SLB/SLA/NEG/POS inputs of the desired channel determine the corresponding TX Output pulse.

## 4.3.4 CW-MODE

When  $OEN = \text{Logic} - 1$  and  $CWEN = \text{Logic} - 1$ , the CW-Mode is activated. FPGA selects  $V_{PP1}$  and  $V_{NN1}$  amplitudes through SLB/SLA/NEG/POS inputs. In theory,  $V_{PP0}$  and  $V_{NN0}$  can be selected, but this is strongly discouraged, since  $V_{PP0}$  and  $V_{NN0}$  usage increases power consumption and cause excessive heating in CW-Mode.

## 4.4 High Temperature Protection

When over temperature is detected,  $OTP_N = \text{Logic} - 0$  and all the outputs are set in Hi-Z state, regardless of  $OEN$  and the other logic control inputs. [Table 4-3](#) shows the relationship between  $REN$ ,  $OEN$  inputs,  $OTP_N$  output and corresponding device status.

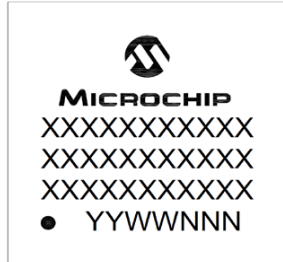
**TABLE 4-3:  $REN$ ,  $OEN$ ,  $OTP_N$  AND DEVICE STATUS**

| $OTP_N$ | EN | OEN | Device   | TX Output |
|---------|----|-----|----------|-----------|
| 0       | 0  | X   | disabled | Hi-Z      |
| 0       | 1  | X   | disabled | Hi-Z      |
| 1       | 0  | X   | disabled | Hi-Z      |
| 1       | 1  | 0   | enabled  | Hi-Z      |
| 1       | 1  | 1   | enabled  | ON        |

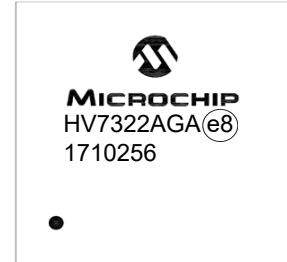
## 5.0 PACKAGING INFORMATION

### 5.1 Package Marking Information

206-Lead TFBGA (12 x 12 x 1.20 mm)



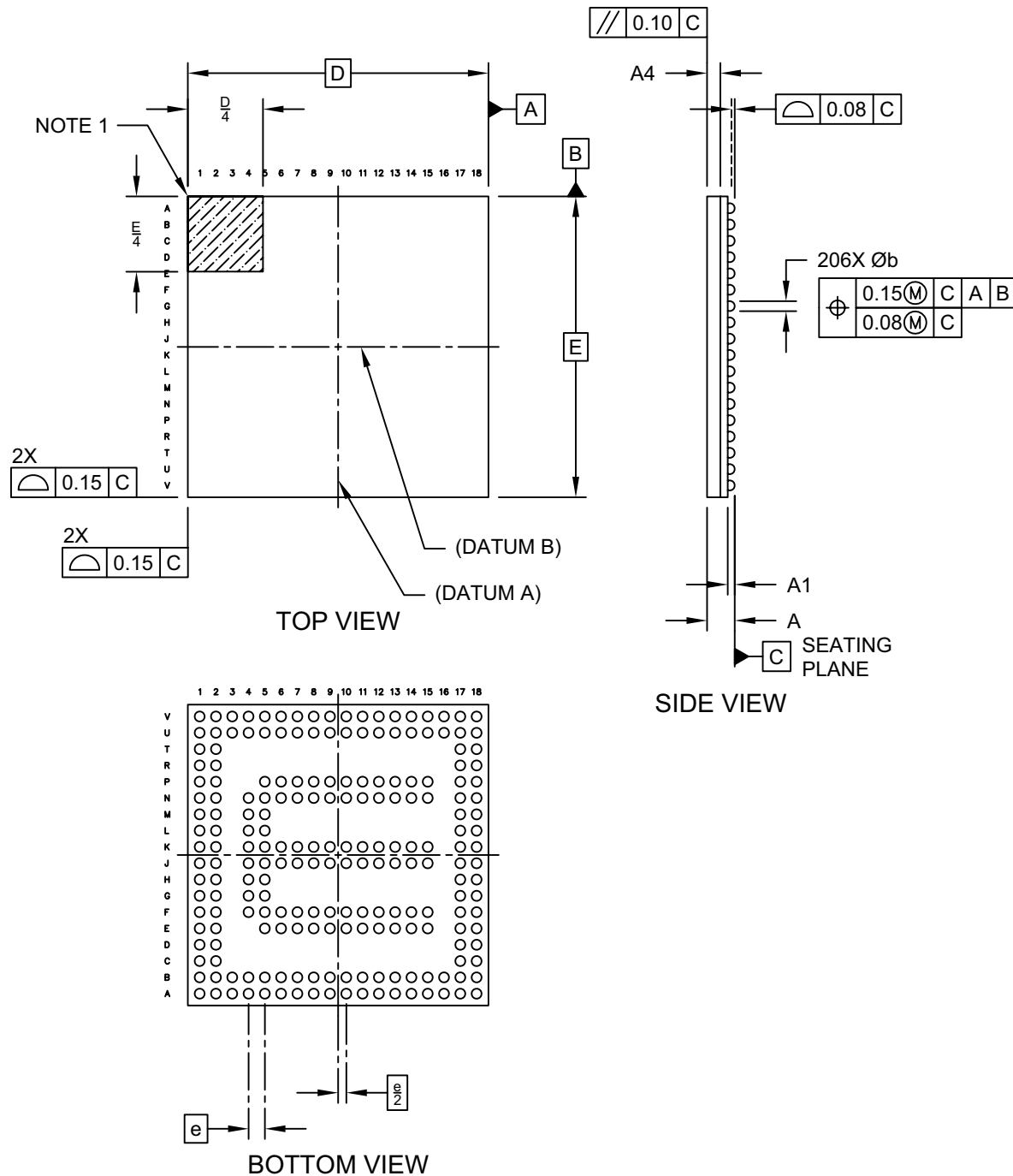
Example



|                |                                                                                                                                                                                                                                                            |                                                                                                                  |
|----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------|
| <b>Legend:</b> | XX...X                                                                                                                                                                                                                                                     | Product Code or Customer-specific information                                                                    |
|                | Y                                                                                                                                                                                                                                                          | Year code (last digit of calendar year)                                                                          |
|                | YY                                                                                                                                                                                                                                                         | Year code (last 2 digits of calendar year)                                                                       |
|                | WW                                                                                                                                                                                                                                                         | Week code (week of January 1 is week '01')                                                                       |
|                | NNN                                                                                                                                                                                                                                                        | Alphanumeric traceability code                                                                                   |
|                | (e8)                                                                                                                                                                                                                                                       | Pb-free JEDEC designator for Matte Tin (Sn)                                                                      |
|                | *                                                                                                                                                                                                                                                          | This package is Pb-free. The Pb-free JEDEC designator (e8) can be found on the outer packaging for this package. |
| <b>Note:</b>   | In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo. |                                                                                                                  |

## 206-Ball Thin Fine Pitch Ball Grid Array (AGA) - 12x12x1.2 mm Body [TFBGA] Internal Flip chip

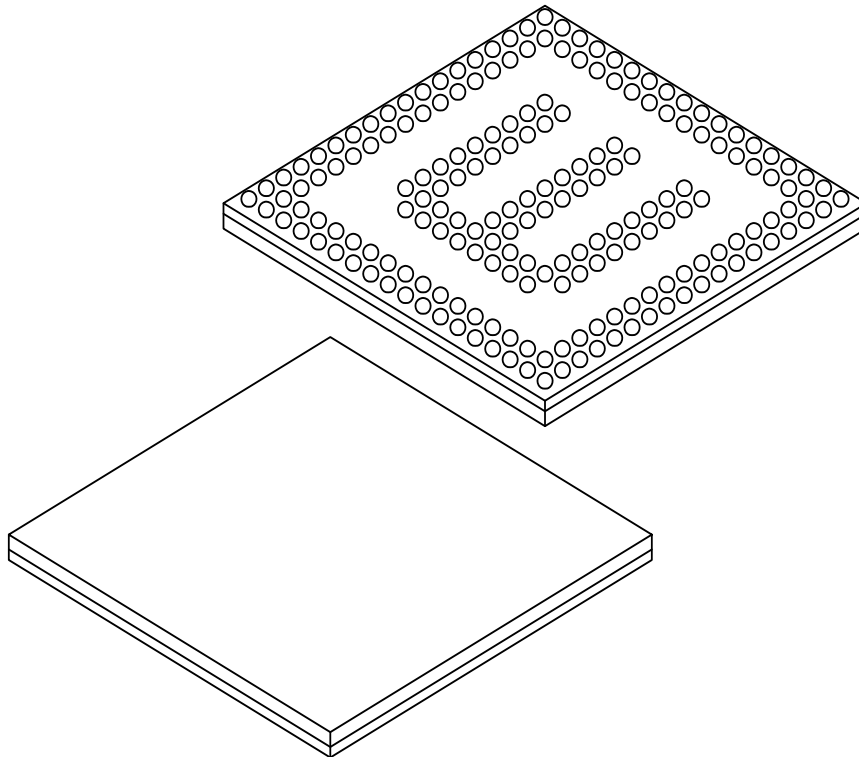
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-C04-1192 Rev. A Sheet 1 of 2

## 206-Ball Thin Fine Pitch Ball Grid Array (AGA) - 12x12x1.2 mm Body [TFBGA] Internal Flip chip

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Units               |    | MILLIMETERS |      |      |
|---------------------|----|-------------|------|------|
| Dimension Limits    |    | MIN         | NOM  | MAX  |
| Number of Terminals | N  | 206         |      |      |
| Pitch               | e  | 0.65 BSC    |      |      |
| Overall Height      | A  | -           | -    | 1.20 |
| Ball Height         | A1 | 0.27        | -    | 0.37 |
| Mold Cap Thickness  | A4 | 0.53 REF    |      |      |
| Overall Length      | D  | 12.00 BSC   |      |      |
| Overall Width       | E  | 12.00 BSC   |      |      |
| Terminal Width      | b  | 0.35        | 0.40 | 0.45 |

**Notes:**

1. Terminal A1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M

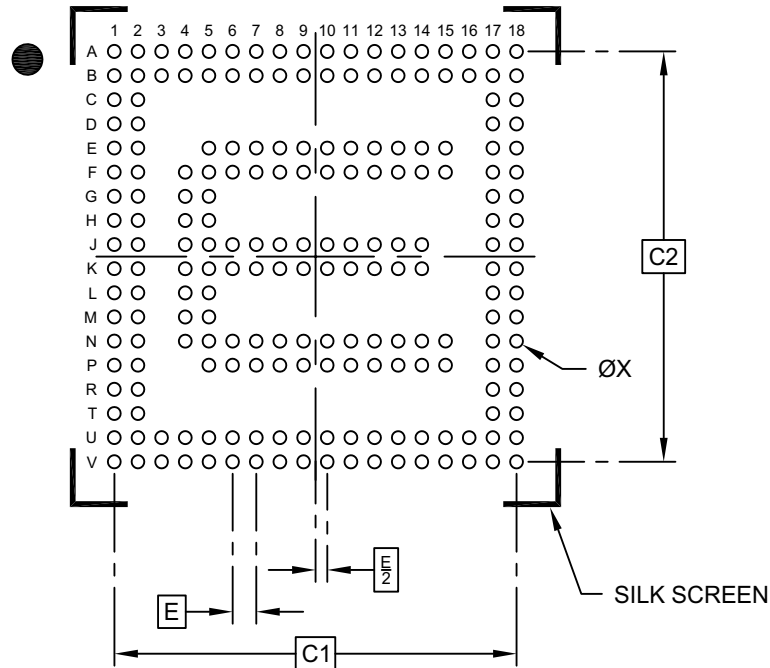
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-C04-1192 Rev. A Sheet 2 of 2

## 206-Ball Thin Fine Pitch Ball Grid Array (AGA) - 12x12x1.2 mm Body [TFBGA] Internal Flip chip

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



### RECOMMENDED LAND PATTERN

| Dimension Limits            | Units | MILLIMETERS |      |     |
|-----------------------------|-------|-------------|------|-----|
|                             |       | MIN         | NOM  | MAX |
| Contact Pitch               | E     | 0.65 BSC    |      |     |
| Contact Pad Spacing         | C1    | 11.05 BSC   |      |     |
| Contact Pad Spacing         | C2    | 11.05 BSC   |      |     |
| Contact Pad Diameter (X206) | ØX    |             | 0.35 |     |

#### Notes:

1. Dimensioning and tolerancing per ASME Y14.5M  
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-3192 Rev. A

## **APPENDIX A: REVISION HISTORY**

### **Revision B (August 2026)**

- Added “Obsolete Device” label to the first page.

### **Revision A (December 2017)**

- Original Release of this Document.

NOTES:

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| <u>PART NO.</u>       | <u>[X]<sup>(1)</sup></u>                      | — | <u>X</u>          | <u>XX</u> |
|-----------------------|-----------------------------------------------|---|-------------------|-----------|
| Device                | Tape and Reel Option                          |   | Temperature Range | Package   |
| Device:               | HV7322                                        |   |                   |           |
| Tape and Reel Option: | Blank = Standard packaging (tube or tray)     |   |                   |           |
| Temperature Range:    | V = 0°C to +85°C (Industrial)                 |   |                   |           |
| Package:              | AGA = TFBGA (Thin Fine Pitch Ball Grid Array) |   |                   |           |

**Examples:**

a) HV7322 -V/AGA= Standard packaging (tube or tray), Industrial Temperature, 206LD TFBGA 12x12x1.20mm Package

**Note 1:** Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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