

Single 5V Bias, Low Harmonic Distortion, 32-Channel, High-Voltage Analog Switch

Features

- 32-Channel, High-Voltage Analog Switch
- Only +5V Bias Supply Required
- 3.3V and 5V CMOS Input Logic Level
- 10 mm x 10 mm Package Size
- 66 MHz Data Shift Clock Frequency
- Low Parasitic Capacitance
- Low Harmonic Distortion
- DC to 50 MHz Analog Small-Signal Frequency
- 200 kHz to 50 MHz Large-Signal Frequency
- -70 dB Typical Off Isolation at 5.0 MHz
- Excellent Noise Immunity
- Cascadable Serial Data Register with Latches
- Integrated Bleed Resistors on the Outputs (Both Sides for HV2915, SWT Side for HV2916)

Application

- Medical Ultrasound Imaging
- Non-Destructive Testing (NDT) Metal Flaw Detection
- Piezoelectric Transducer Drivers
- Inkjet Printer Head
- Optical MEMS Module

General Description

HV2815/HV2915/HV2916 are low harmonic distortion, low charge injection, 32-channel, high-voltage analog switches without high-voltage bias supplies. They are intended for use in applications requiring high-voltage switching controlled by low-voltage control signals, such as medical ultrasound imaging, driving piezoelectric transducers and printers.

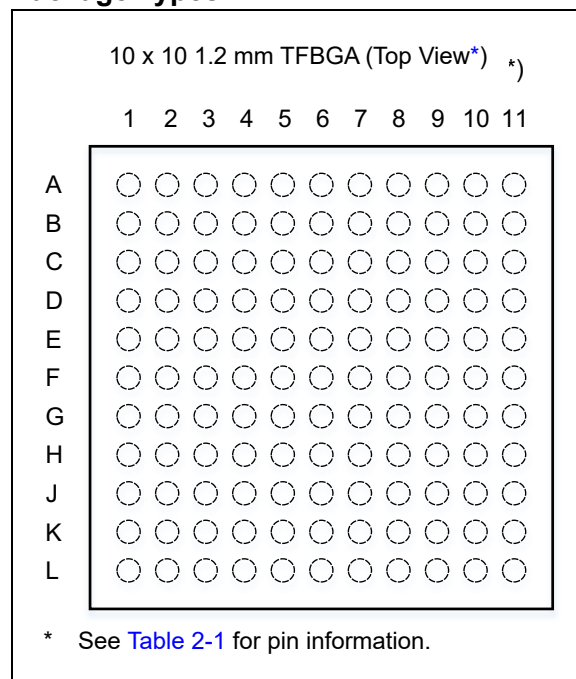
The HV2815/HV2915/HV2916 are pin-to-pin compatible with the low-voltage bias HV2070, except for the V_{SS} voltage pin. The package of HV2815/HV2915/HV2916 is the same 10 mm x 10 mm TFBGA package as HV2070. The HV2815/HV2915/HV2916 have a smaller size compared to the HV2803/HV2903/HV2904 and better off-isolation than the HV2070. When using the devices, the high voltage applied at the SWS pin is transmitted to the SWT pin when the switch is in the ON state.

When the switch is in the OFF state, high voltage should not be applied to the SWT pin. In a medical ultrasound system, the SWS pin should be connected to the AFE (Analog Front End), and the SWT pin should be connected to only one piezoelectric transducer element to avoid high voltage at the SWT pin during the switch OFF state.

The HV2915 has bleed resistors at the SWS pins and SWT pins. The HV2815 does not have bleed resistors. The HV2916 has bleed resistors at the SWT pins only. The bleed resistors eliminate possible voltage build-up on capacitive load, such as a piezoelectric transducer. The ON/OFF state of 32 switches is programmed individually through a digital serial interface.

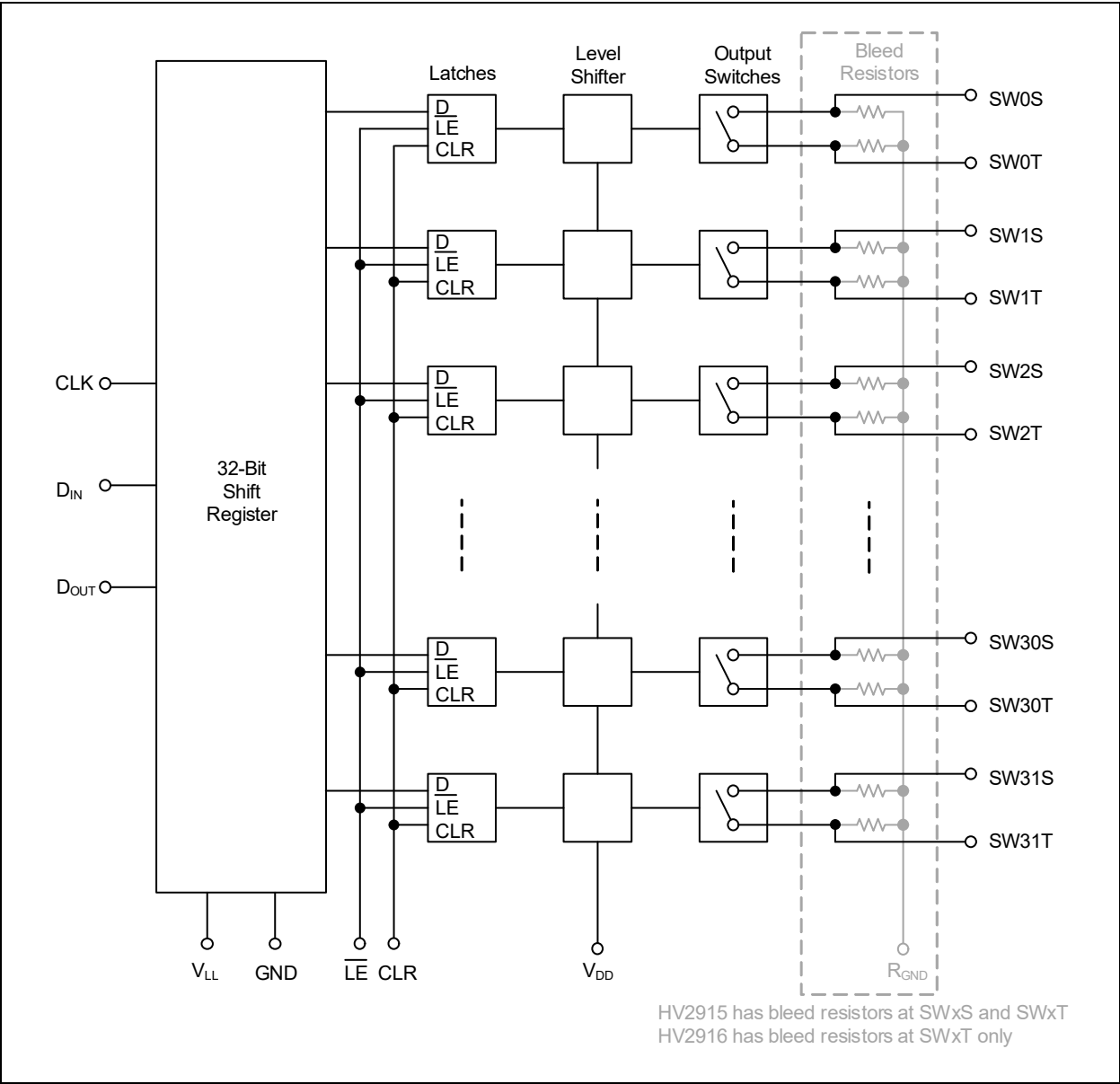
The devices require only a +5V low-voltage bias supply. However, all of the analog switches can pass up to $\pm 100V$ high-voltage pulsed signal from the SWS pin to the SWT pin. Like other low-voltage bias switches, HV2815/HV2915/HV2916 cannot pass high-voltage DC signals. They can only pass a high-voltage pulsed signal up to a 2.5 μsec pulse width. These devices have 6 Ω on-resistance and 50 MHz bandwidth for small-signals.

Package Types



HV2815/HV2915/HV2916

Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS†

Logic Supply Voltage (V_{LL})	-0.5V to 6.6V
Positive Supply Voltage (V_{DD})	-0.5V to 6.6V
Logic Input Voltage (V_{IN})	-0.5V to V_{LL} +0.3V
Analog Signal Voltage SWS pin (V_{SWS})	-110V to +110V
Analog Signal Voltage SWT pin (V_{SWT}) when switch is on	-110V to +110V
Analog signal voltage SWT pin (V_{SWT}) when switch is off	-2V to +2V
Peak Analog Signal Current/Channel (I_{PK})	3.8A

† **Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS^(1,2,3)

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Logic Supply Voltage	V_{LL}	3	—	5.5	V	
Positive Supply Voltage	V_{DD}	4.5	—	6.3	V	
High-Level Input Voltage	V_{IH}	0.9 V_{LL}	—	V_{LL}	V	
Low-Level Input Voltage	V_{IL}	0	—	0.1 V_{LL}	V	
Analog Signal Voltage SWS Pin Peak-to-Peak	V_{SWS}	-100	—	100	V	

- Note 1:** Power-up sequence is V_{LL} first and then V_{DD} . Powered-down sequence is reverse of power-up.
Note 2: V_{SWS} and V_{SWT} must be within V_{DD} and GND or floating during power-up/down transition.
Note 3: Rise and fall times of power supplies, V_{LL} and V_{DD} , should be greater than 1.0 ms.

DC ELECTRICAL CHARACTERISTICS

Unless otherwise specified, $V_{DD} = +5V$, $V_{LL} = +5V$, $T_{AMB} = +25^{\circ}C$; **Boldface** specifications apply over the full operating temperature range.

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Small-Signal Switch On-Resistance	R_{ONS}	—	6	9	Ω	$I_{SIG} = 5 \text{ mA}$
		—	6	9	Ω	$I_{SIG} = 200 \text{ mA}$
Small-Signal Switch On-Resistance Matching	ΔR_{ONS}	—	—	20	%	$I_{SIG} = 5 \text{ mA}$
Large-Signal Switch On-Resistance	R_{ONL}	—	7	—	Ω	$V_{SIG} = 90V$, $R_{LOAD} = 80\Omega$ (Note 1)
Value of Output Bleed Resistor (HV2915/HV2916)	R_{INT}	20	35	50	k Ω	Output switch to RGND, $I_{RINT} = 20 \mu A$
Switch-Off Leakage per SWT Pin	I_{SOL}	—	—	3	μA	$V_{SIG} = +100V$, 500 μs pulse, see Figure 3-1
		—	—	3	μA	$V_{SIG} = -100V$, 100 μs pulse, see Figure 3-1 (Note 1)

- Note 1:** Specification is obtained by characterization and is not 100% tested.
Note 2: Design guidance only.

HV2815/HV2915/HV2916

DC ELECTRICAL CHARACTERISTICS (CONTINUED)

Unless otherwise specified, $V_{DD} = +5V$, $V_{LL} = +5V$, $T_{AMB} = +25^{\circ}C$; **Boldface** specifications apply over the full operating temperature range.

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
HV2815						
Switch-Off Bias per SWS Pin	I _{SOB}	—	—	5	μA	V _{SIG} = +100V, 500 μs pulse, see Figure 3-2
		—	—	3	mA	V _{SIG} = -100V, 100 μs pulse, see Figure 3-2 (Note 1)
Switch-Off Bias per SWT Pin		—	—	3	μA	V _{SIG} = +300 mV, -300 mV, see Figure 3-3
HV2915						
Switch-Off Bias of all SWT Pin	I _{SOB}	—	—	10	μA	V _{SIG} = +300 mV, -300 mV, see Figure 3-3
HV2916						
Switch-Off Bias per SWS Pin	I _{SOB}	—	—	5	μA	V _{SIG} = +100V, 500 μs pulse, see Figure 3-2
		—	—	3	mA	V _{SIG} = -100V, 100 μs pulse, see Figure 3-2 (Note 1)
Switch-Off Bias of all SWT Pins		—	—	10	μA	V _{SIG} = +300 mV, -300 mV, see Figure 3-3
DC Offset Switch Off	V _{OS}	—	1	10	mV	R _{LOAD} = 25 kΩ (HV2815), 50 kΩ (HV2916), no load (HV2915), see Figure 3-4
DC Offset Switch On		—	1	10		
Quiescent V _{DD} Supply Current	I _{DDQ}	—	—	10	μA	All switches off
		—	—	10	μA	All switches on, V _{SW} = 1V
Quiescent V _{LL} Supply Current	I _{LLQ}	—	—	10	μA	All logic inputs are static
Switch Output Peak Current	I _{SW}	2	2.9	—	A	V _{SIG} duty cycle < 0.1% (Note 1)
Output Switching Frequency	f _{SW}	—	—	50	kHz	Duty cycle = 50% (Note 1)
Average V _{DD} Supply Current	I _{DD}	—	7	10	mA	All output switches are turning on and off at 50 kHz with no load
Average V _{LL} Supply Current	I _{LL}	—	1	2.5	mA	f _{CLK} = 5.0 MHz
Data Out Source Current	I _{SOR}	10	—	—	mA	V _{OUT} = V _{LL} – 0.7V
Data Out Sink Current	I _{SINK}	10	—	—	mA	V _{OUT} = 0.7V
Logic Input Capacitance	C _{IN}	—	8	—	pF	Note 2

Note 1: Specification is obtained by characterization and is not 100% tested.

2: Design guidance only.

AC ELECTRICAL CHARACTERISTICS

Unless otherwise specified, $V_{DD} = +5V$, $V_{LL} = +5V$, $T_{AMB} = +25^{\circ}C$; **Boldface** specifications apply over the full operating temperature range.

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Setup Time Before $\overline{LE}$ rises	t_{SD}	25	—	—	ns	Note 1
Time Width of $\overline{LE}$	t_{WLE}	12	—	—	ns	Note 1
Clock Delay Time to Data Out	t_{DO}	—	—	13.5	ns	
Time Width of CLR	t_{WCLR}	55	—	—	ns	Note 1
Setup Time Data to Clock	t_{SU}	1.5	—	—	ns	Note 1
Hold Time Data from clock	t_H	1.5	—	—	ns	Note 1
Clock Frequency	f_{CLK}	—	—	66	MHz	50% duty cycle, $f_{DIN} = (1/2)f_{CLK}$, $C_{DOUT} = 20$ pF (Note 1)
Clock Rise and Fall Times	t_R, t_F	—	—	50	ns	Note 2
Turn-on Time	t_{ON}	—	1.6	5	μs	$V_{SIG} = 5V$, $R_{LOAD} = 550\Omega$, see Figure 3-5
Turn-off Time	t_{OFF}	—	2.8	5	μs	
Input Large-Signal Pulse Width	t_{PW}	—	—	2.5	μs	$V_{PULSE} = 0V$ to $\pm 100V$, measured at 90% amplitude, see Figure 3-6 (Note 1)
Maximum V_{SIG} Slew Rate	dv/dt	—	—	20	V/ns	Note 1
Analog Small-Signal Frequency	f_{BWS}	—	50	—	MHz	Note 1
Off Isolation SWS to SWT	K_O	—	-65	-55	dB	$f = 5.0$ MHz, 1.0 k Ω // 15 pF load, see Figure 3-7 (Note 1)
		—	-70	-65		$f = 5.0$ MHz, 50Ω load, see Figure 3-7 (Note 1)
Off Isolation SWT to SWS		—	-65	-60	dB	$f = 5.0$ MHz, 1.0 k Ω // 15 pF load, see Figure 3-8 (Note 1)
		—	-70	-65		$f = 5.0$ MHz, 50Ω load, see Figure 3-8 (Note 1)
Switch Crosstalk	K_{CR}	—	-70	-60	dB	$f = 5.0$ MHz, 50Ω load, see Figure 3-9 (Note 1)
Off Capacitance SWT to GND	$C_{SG(OFF)}$	—	5	—	pF	$V_{SIG} = 50$ mV @ 1 MHz, no load (Note 1)
Off Capacitance SWS to GND		—	13	—		
On Capacitance SWT to GND	$C_{SG(ON)}$	—	14	—	pF	$V_{SIG} = 50$ mV @ 1 MHz, no load (Note 1)
On Capacitance SWS to GND		—	14	—		
Output Voltage Spike at SWT, SWS	$+V_{SPK}$	—	—	40	mV	$R_{LOAD} = 50\Omega$, see Figure 3-10 (Note 1)
	$-V_{SPK}$	-10	—	—		
Charge Injection at SWT	QC	—	50	—	pC	See Figure 3-11 (Note 1)
Charge Injection at SWS		—	100	—	pC	See Figure 3-11 (Note 1)
Second Harmonic Distortion	HD2	—	-65	—	dBc	$V_{SIG} = 1.5$ V _{PP} @ 5 MHz, 50Ω load (Note 1)
		—	-65	—	dBc	$V_{SIG} = 1.5$ V _{PP} @ 5 MHz, 1 k Ω // 15 pF load (Note 1)

Note 1: Specification is obtained by characterization and is not 100% tested.

2: Design guidance only.

HV2815/HV2915/HV2916

TEMPERATURE SPECIFICATION

Parameters	Sym	Min	Typ	Max	Units	Conditions
Temperature Range						
Operating Temperature Range	T_A	0	—	+70	°C	
Storage Temperature Range	T_S	-65	—	+150	°C	
Maximum Junction Temperature	T_J	—	—	+125	°C	
Package Thermal Resistance						
Thermal Resistance, TFBGA	θ_{JA}	—	+20	—	°C/W	

TABLE 1-1: TRUTH TABLE^(1,2,4)

D0	D1	...	D15	D16	...	D31	D _{IN}	$\overline{LE}^{(3,5)}$	CLR ⁽⁶⁾	SW0	SW1	...	SW15	SW16	...	SW31		
L	—	...	—	—	...	—	X	L	L	OFF	—	...	—	—	...	—		
H	—		—	—		—	X	L	L	ON	—		—	—				
—	L		—	—		—	X	L	L	—	OFF		—	—				
—	H		—	—		—	X	L	L	—	ON		—	—				
—	—		—	—		—	X	L	L	—	—		—	—				
—	—		—	—		—	X	L	L	—	—		—	—				
—	—		L	—		—	X	L	L	—	—		OFF	—		—		
—	—		H	—		—	X	L	L	—	—		ON	—		—		
—	—		—	L		—	X	L	L	—	—		—	OFF		—	—	
—	—		—	H		—	X	L	L	—	—		—	ON		—	—	
—	—		—	—		—	X	L	L	—	—		—	—		—	—	
—	—		—	—		—	X	L	L	—	—		—	—		—	—	
—	—		—	—		—	X	L	L	—	—		—	—		—	—	
—	—		—	—		—	L	X	L	L	—		—	—		—	—	OFF
—	—		—	—		—	H	X	L	L	—		—	—		—	—	ON
X	X		X	X		X	X	X	X	H	L		HOLD PREVIOUS STATE					
X	X	X	X	X	X	X	X	X	H	ALL SWITCHES OFF								

- Note 1:** The 32 switches operate independently.
2: Serial data are clocked in on the L to H transition of the CLK.
3: All 32 switches go to a state retaining their latched condition at the rising edge of $\overline{LE}$. When $\overline{LE}$ is low the shift registers' data flow through the latch.
4: D_{OUT} is high when data in Register 31 are high.
5: Shift register clocking has no effect on the switch states if $\overline{LE}$ is high.
6: The CLR input overrides all the inputs.

1.1 Typical Timing Diagram

Figure 1-1 shows timing of the AC characteristic parameters graphically.

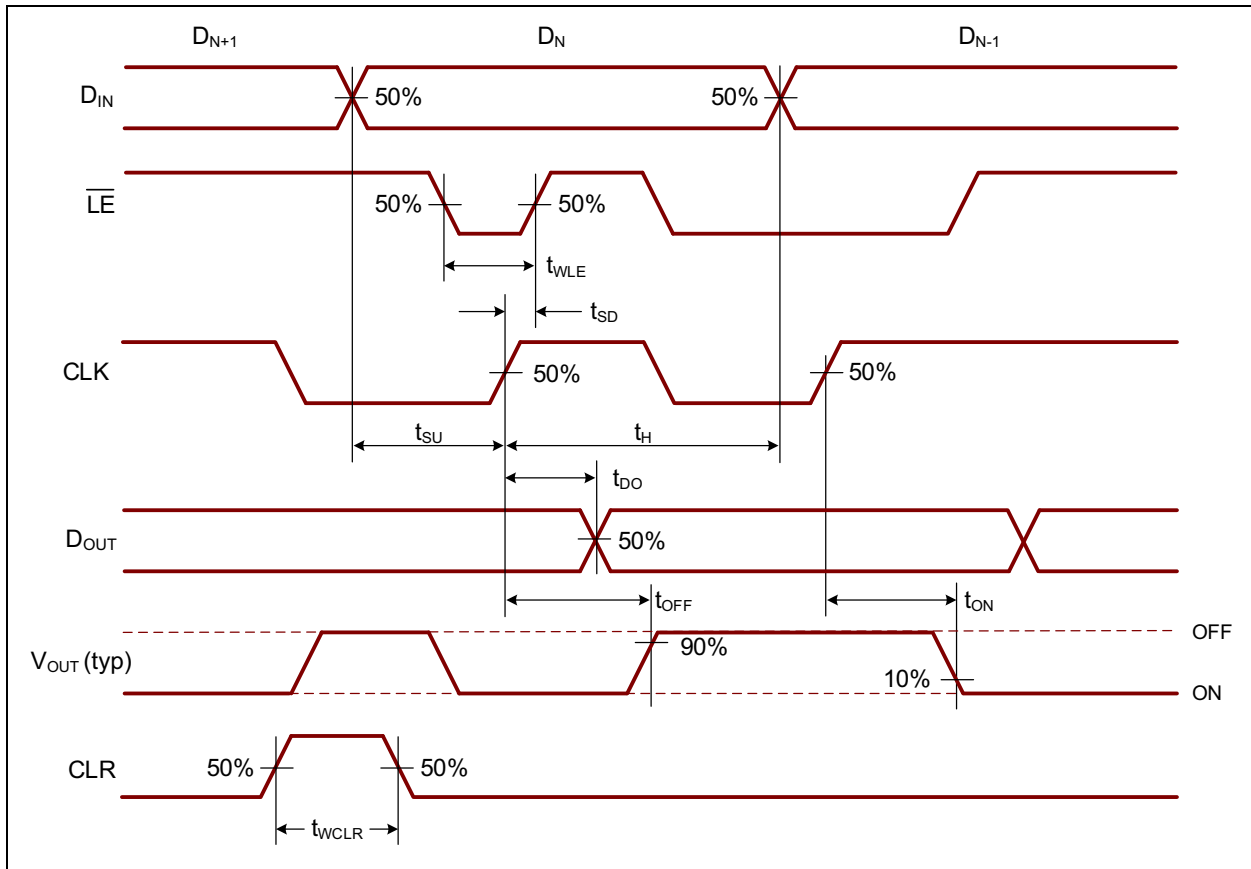


FIGURE 1-1: Logic Input Timing Diagram.

HV2815/HV2915/HV2916

2.0 PIN DESCRIPTION

This section details the pin description for the 121-Ball TFBGA package (Figure 2-1). The descriptions of the pins are listed in Table 2-1.

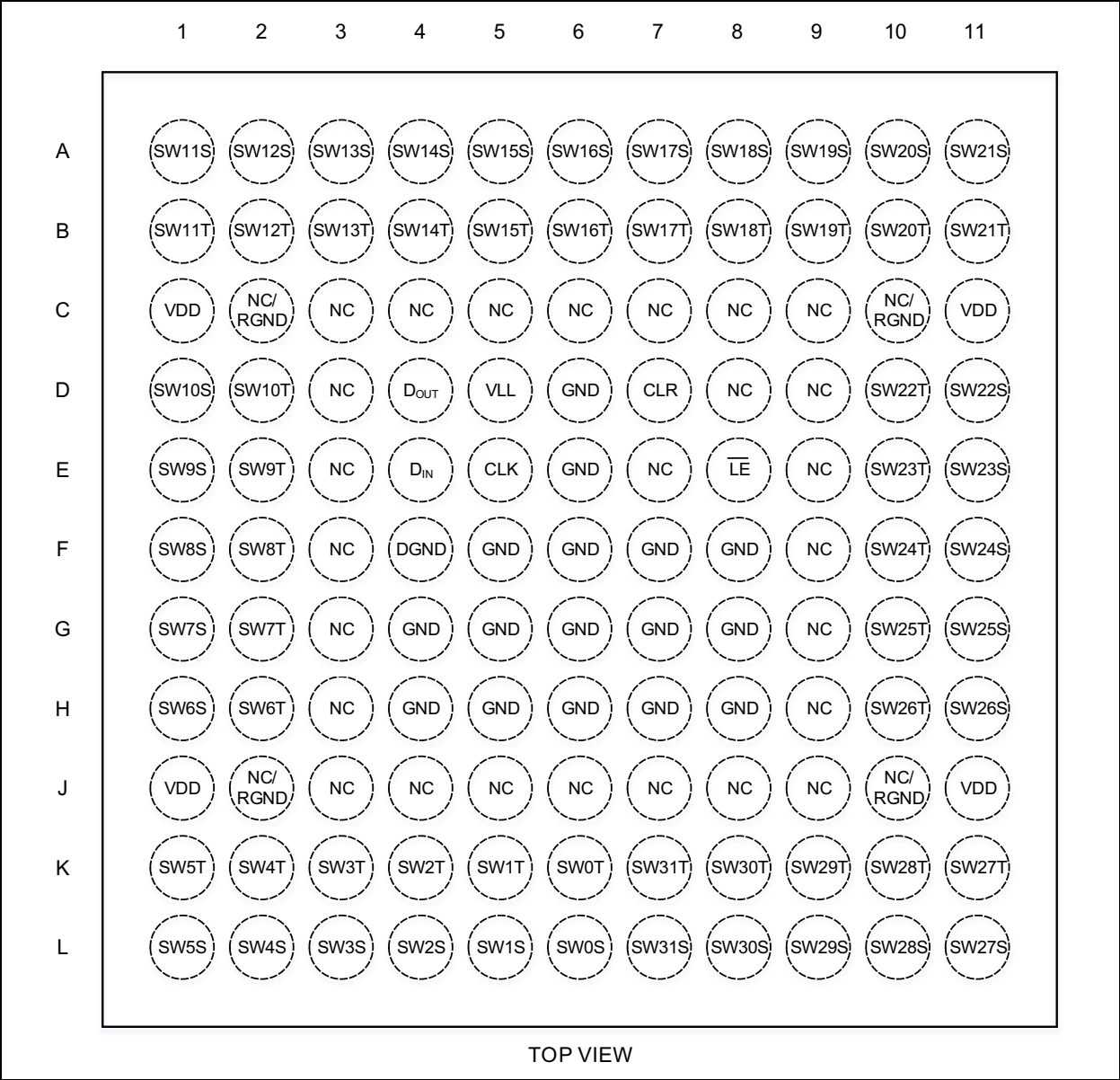


FIGURE 2-1: 121-Ball TFBGA Package – Top View.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Symbol		Description
	HV2815	HV2915/ HV2916	
A1	SW11S	SW11S	Analog Switch 11 Terminal S
A2	SW12S	SW12S	Analog Switch 12 Terminal S
A3	SW13S	SW13S	Analog Switch 13 Terminal S
A4	SW14S	SW14S	Analog Switch 14 Terminal S
A5	SW15S	SW15S	Analog Switch 15 Terminal S
A6	SW16S	SW16S	Analog Switch 16 Terminal S
A7	SW17S	SW17S	Analog Switch 17 Terminal S
A8	SW18S	SW18S	Analog Switch 18 Terminal S
A9	SW19S	SW19S	Analog Switch 19 Terminal S
A10	SW20S	SW20S	Analog Switch 20 Terminal S
A11	SW21S	SW21S	Analog Switch 21 Terminal S
B1	SW11T	SW11T	Analog Switch 11 Terminal T; Connect to a Piezoelectric Element
B2	SW12T	SW12T	Analog Switch 12 Terminal T; Connect to a Piezoelectric Element
B3	SW13T	SW13T	Analog Switch 13 Terminal T; Connect to a Piezoelectric Element
B4	SW14T	SW14T	Analog Switch 14 Terminal T; Connect to a Piezoelectric Element
B5	SW15T	SW15T	Analog Switch 15 Terminal T; Connect to a Piezoelectric Element
B6	SW16T	SW16T	Analog Switch 16 Terminal T; Connect to a Piezoelectric Element
B7	SW17T	SW17T	Analog Switch 17 Terminal T; Connect to a Piezoelectric Element
B8	SW18T	SW18T	Analog Switch 18 Terminal T; Connect to a Piezoelectric Element
B9	SW19T	SW19T	Analog Switch 19 Terminal T; Connect to a Piezoelectric Element
B10	SW20T	SW20T	Analog Switch 20 Terminal T; Connect to a Piezoelectric Element
B11	SW21T	SW21T	Analog Switch 21 Terminal T; Connect to a Piezoelectric Element
C1	V _{DD}	V _{DD}	Positive Supply Voltage
C2	NC	R _{GND}	No Connect/Ground for Bleed Resistor
C3~C9	NC	NC	No Connect
C10	NC	R _{GND}	No Connect/Ground for Bleed Resistor
C11	V _{DD}	V _{DD}	Positive Supply Voltage
D1	SW10S	SW10S	Analog Switch 10 Terminal S
D2	SW10T	SW10T	Analog Switch 10 Terminal T; Connect to a Piezoelectric Element
D3	NC	NC	No Connect
D4	D _{OUT}	D _{OUT}	Data Out Logic Output
D5	V _{LL}	V _{LL}	Logic Supply Voltage
D6	GND	GND	Ground
D7	CLR	CLR	Latch Clear Logic Input
D8~D9	NC	NC	No Connect
D10	SW22T	SW22T	Analog Switch 22 Terminal T; Connect to a Piezoelectric Element
D11	SW22S	SW22S	Analog Switch 22 Terminal S
E1	SW9S	SW9S	Analog Switch 9 Terminal S
E2	SW9T	SW9T	Analog Switch 9 Terminal T; Connect to a Piezoelectric Element
E3	NC	NC	No Connect
E4	D _{IN}	D _{IN}	Data In Logic Input

HV2815/HV2915/HV2916

TABLE 2-1: PIN FUNCTION TABLE (CONTINUED)

Pin Number	Symbol		Description
	HV2815	HV2915/ HV2916	
E5	CLK	CLK	Clock Logic Input for Shift Register
E6	GND	GND	Ground
E7	NC	NC	No Connect
E8	$\overline{\text{LE}}$	$\overline{\text{LE}}$	Latch Enable Logic Input, Low Active
E9	NC	NC	No Connect
E10	SW23T	SW23T	Analog Switch 23 Terminal T; Connect to a Piezoelectric Element
E11	SW23S	SW23S	Analog Switch 23 Terminal S
F1	SW8S	SW8S	Analog Switch 8 Terminal S
F2	SW8T	SW8T	Analog Switch 8 Terminal T; Connect to a Piezoelectric Element
F3	NC	NC	No Connect
F4	DGND	DGND	Ground for Logic Circuitry
F5~F8	GND	GND	Ground
F9	NC	NC	No Connect
F10	SW24T	SW24T	Analog Switch 24 Terminal T; Connect to a Piezoelectric Element
F11	SW24S	SW24S	Analog Switch 24 Terminal S
G1	SW7S	SW7S	Analog Switch 7 Terminal S
G2	SW7T	SW7T	Analog Switch 7 Terminal T; Connect to a Piezoelectric Element
G3	NC	NC	No Connect
G4~G8	GND	GND	Ground
G9	NC	NC	No Connect
G10	SW25T	SW25T	Analog Switch 25 Terminal T; Connect to a Piezoelectric Element
G11	SW25S	SW25S	Analog Switch 25 Terminal S
H1	SW6S	SW6S	Analog Switch 6 Terminal S
H2	SW6T	SW6T	Analog Switch 6 Terminal T; Connect to a Piezoelectric Element
H3	NC	NC	No Connect
H4~H8	GND	GND	Ground
H9	NC	NC	No Connect
H10	SW26T	SW26T	Analog Switch 26 Terminal T; Connect to a Piezoelectric Element
H11	SW26S	SW26S	Analog Switch 26 Terminal S
J1	V _{DD}	V _{DD}	Positive Supply Voltage
J2	NC	R _{GND}	No Connect/Ground for Bleed Resistor
J3~9	NC	NC	No Connect
J10	NC	R _{GND}	No Connect / Ground for Bleed Resistor
J11	V _{DD}	V _{DD}	Positive Supply Voltage
K1	SW5T	SW5T	Analog Switch 5 Terminal T; Connect to a Piezoelectric Element
K2	SW4T	SW4T	Analog Switch 4 Terminal T; Connect to a Piezoelectric Element
K3	SW3T	SW3T	Analog Switch 3 Terminal T; Connect to a Piezoelectric Element
K4	SW2T	SW2T	Analog Switch 2 Terminal T; Connect to a Piezoelectric Element
K5	SW1T	SW1T	Analog Switch 1 Terminal T; Connect to a Piezoelectric Element
K6	SW0T	SW0T	Analog Switch 0 Terminal T; Connect to a Piezoelectric Element
K7	SW31T	SW31T	Analog Switch 31 Terminal T; Connect to a Piezoelectric Element
K8	SW30T	SW30T	Analog Switch 30 Terminal T; Connect to a Piezoelectric Element

TABLE 2-1: PIN FUNCTION TABLE (CONTINUED)

Pin Number	Symbol		Description
	HV2815	HV2915/ HV2916	
K9	SW29T	SW29T	Analog Switch 29 Terminal T; Connect to a Piezoelectric Element
K10	SW28T	SW28T	Analog Switch 28 Terminal T; Connect to a Piezoelectric Element
K11	SW27T	SW27T	Analog Switch 27 Terminal T; Connect to a Piezoelectric Element
L1	SW5S	SW5S	Analog Switch 5 Terminal S
L2	SW4S	SW4S	Analog Switch 4 Terminal S
L3	SW3S	SW3S	Analog Switch 3 Terminal S
L4	SW2S	SW2S	Analog Switch 2 Terminal S
L5	SW1S	SW1S	Analog Switch 1 Terminal S
L6	SW0S	SW0S	Analog Switch 0 Terminal S
L7	SW31S	SW31S	Analog Switch 31 Terminal S
L8	SW30S	SW30S	Analog Switch 30 Terminal S
L9	SW29S	SW29S	Analog Switch 29 Terminal S
L10	SW28S	SW28S	Analog Switch 28 Terminal S
L11	SW27S	SW27S	Analog Switch 27 Terminal S

3.0 TEST CIRCUIT EXAMPLES

This section details a few example of test circuits.

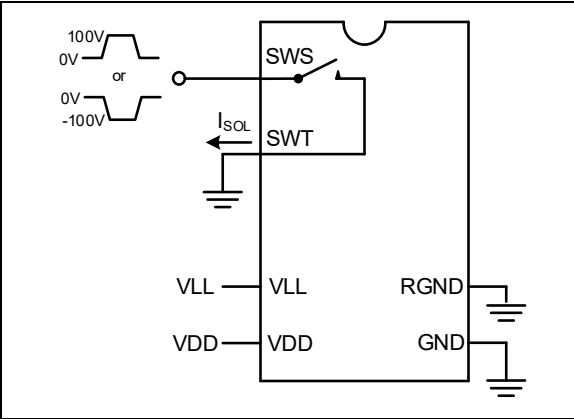


FIGURE 3-1: Switch-Off Leakage SWT.

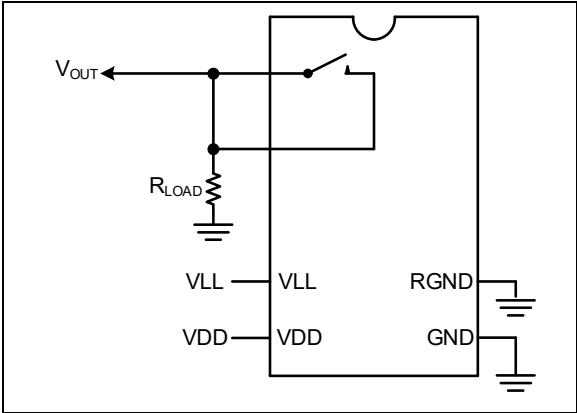


FIGURE 3-4: Switch DC Offset.

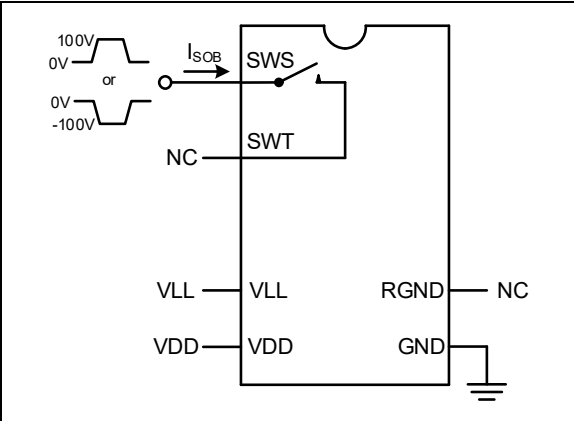


FIGURE 3-2: Switch-Off Bias SWS.

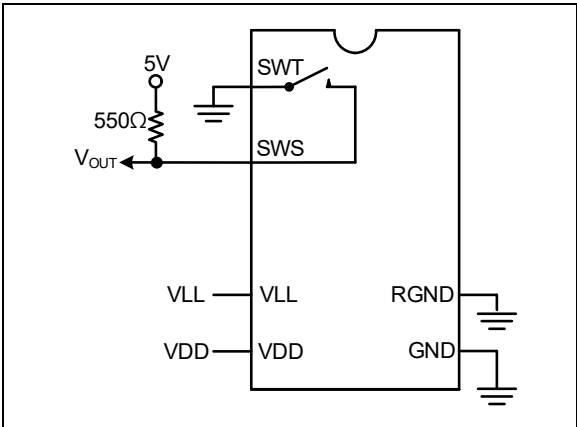


FIGURE 3-5: T_{ON}/T_{OFF} Test Circuit.

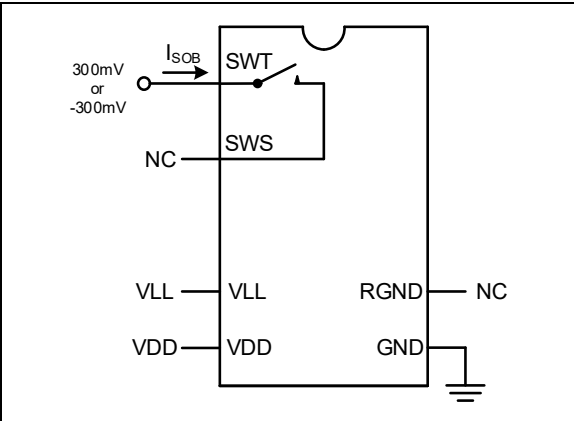


FIGURE 3-3: Switch-Off Bias SWT.

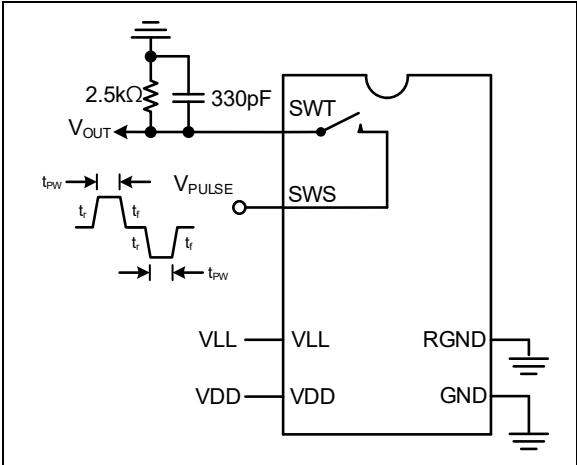


FIGURE 3-6: Tx Pulse Width.

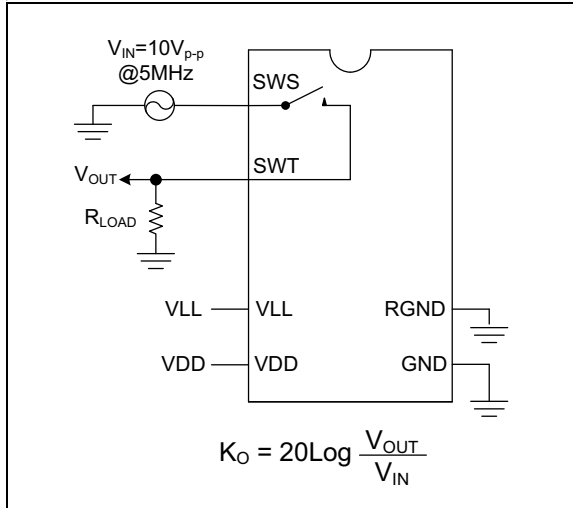


FIGURE 3-7: Off Isolation SWS to SWT.

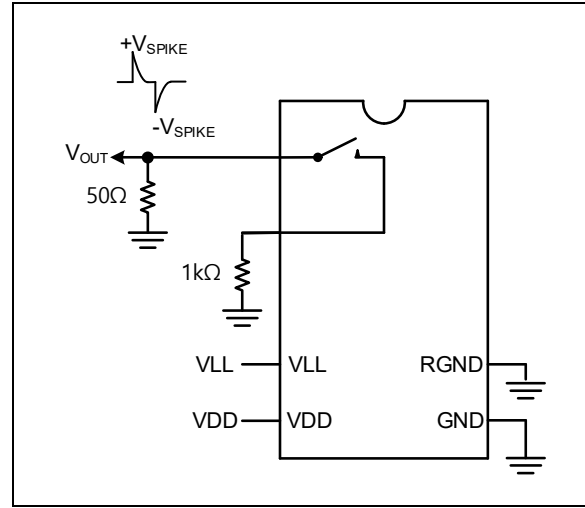


FIGURE 3-10: Output Voltage Spike.

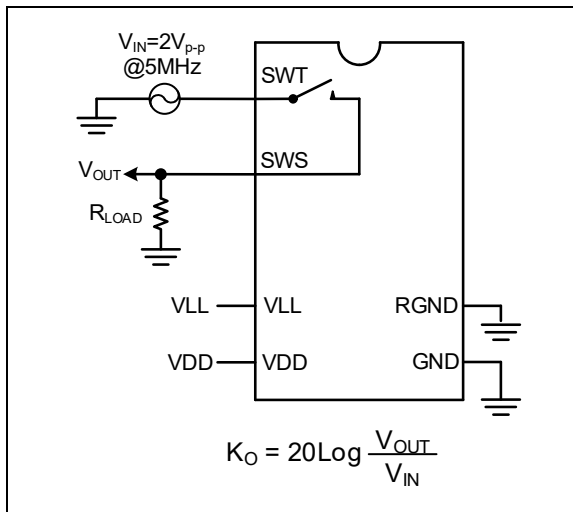


FIGURE 3-8: Off Isolation SWT to SWS.

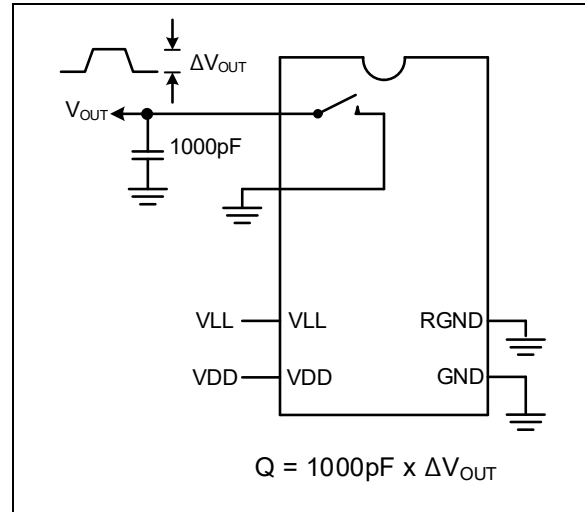


FIGURE 3-11: Charge Injection.

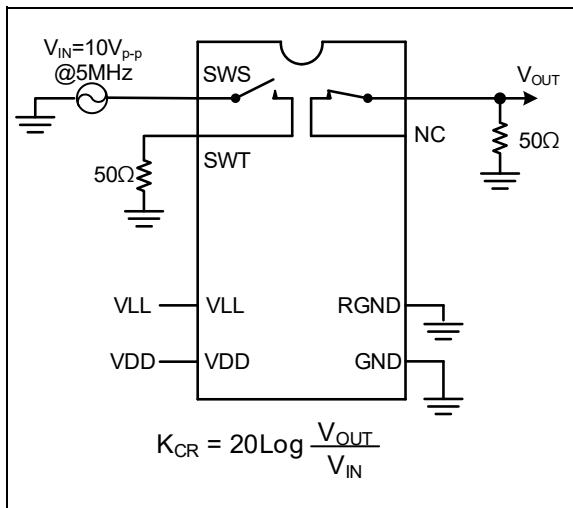


FIGURE 3-9: Switch Crosstalk.

HV2815/HV2915/HV2916

4.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated: $V_{DD} = +5V$, $V_{LL} = +5V$, $T_A = +25^\circ C$.

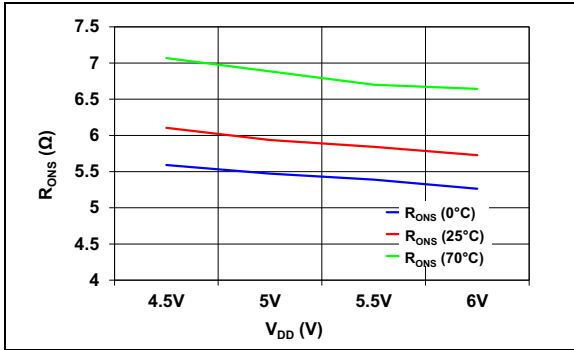


FIGURE 4-1: R_{ONS} at 5 mA vs. V_{DD} .

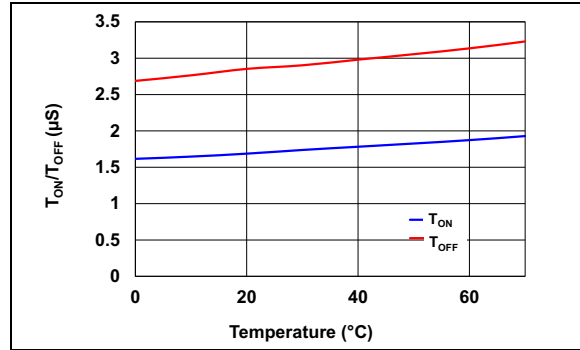


FIGURE 4-4: T_{ON}/T_{OFF} vs. Temperature.

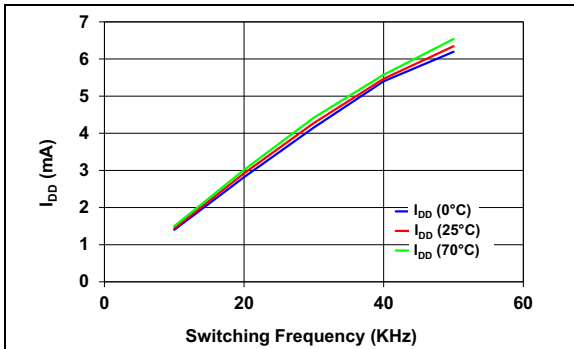


FIGURE 4-2: I_{DD} vs. Switching Frequency.

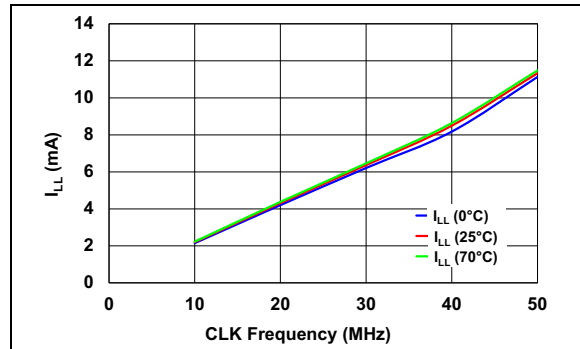


FIGURE 4-5: I_{LL} vs. CLK Frequency.

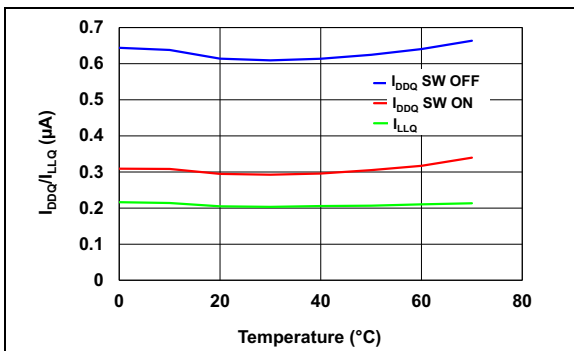


FIGURE 4-3: I_{DDQ}/I_{LLQ} vs. Temperature.

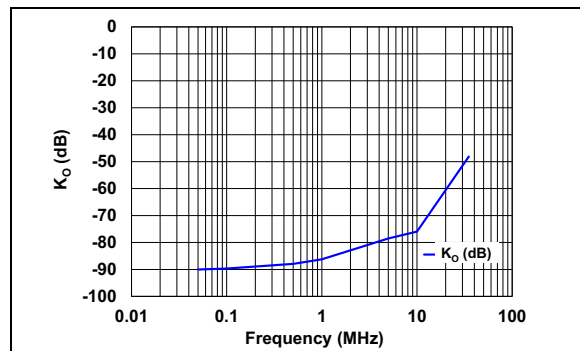


FIGURE 4-6: K_O , SWS to SWT vs. Frequency with 50Ω Load.

5.0 DETAILED DESCRIPTION AND APPLICATION INFORMATION

5.1 Device Overview

The HV2815/HV2915/HV2916 are low harmonic distortion, low charge injection, 32-channel, high-voltage analog switches without high-voltage supplies. The devices require only A +5V bias voltage for operation. The high-voltage analog switches are used for multiplexing a piezoelectric transducer array in a probe to multiple channel transmitter (Tx) arrays in a medical ultrasound system.

The HV2815/HV2915/HV2916 have asymmetric topology to achieve a smaller size as compared to previous low-voltage bias, high-voltage switches. Each switch has an SWS terminal and an SWT terminal. The SWS and SWT pins are not interchangeable. The high-voltage pulsed signal applied at the SWS pin is transmitted to the SWT pin when the switch is in the ON state. When the switch is in the OFF state, a high-voltage signal should not be applied to the SWT pin due to the asymmetric topology. In a medical ultrasound system, the SWS pin should be connected to

the AFE (Analog Front End) and the SWT pin should be connected to only one piezoelectric transducer element to avoid high voltage at the SWT pin during a switch OFF state.

The HV2815/HV2915/HV2916 are distinguished by bleed resistors that eliminate voltage build-up in capacitance load, such as piezoelectric transducers. HV2815 has no bleed resistors. HV2915 has bleed resistors in both sides of the switch. HV2916 has bleed resistors only in the SWT pin of the switch. These devices can pass a $\pm 100\text{V}$ high-voltage pulsed signal without high-voltage bias supplies, such as $\pm 100\text{V}$. The HV2815/HV2915/HV2916 have typical 6Ω on-resistance and 50 MHz bandwidth for small signals. Like other low-voltage bias switches, HV2815/HV2915/HV2916 cannot pass a high-voltage DC signal and can pass a high-voltage pulsed signal up to a 2.5 μsec pulse width.

Figure 5-1 shows a typical medical ultrasound imaging system, consisting of 64 channels of transmit pulsers (Tx), 64 channels of receivers (Rx and ADC) and 64 channels of T/R switches connecting to 256 elements of an ultrasound probe via a HV2XXX high-voltage analog switch array.

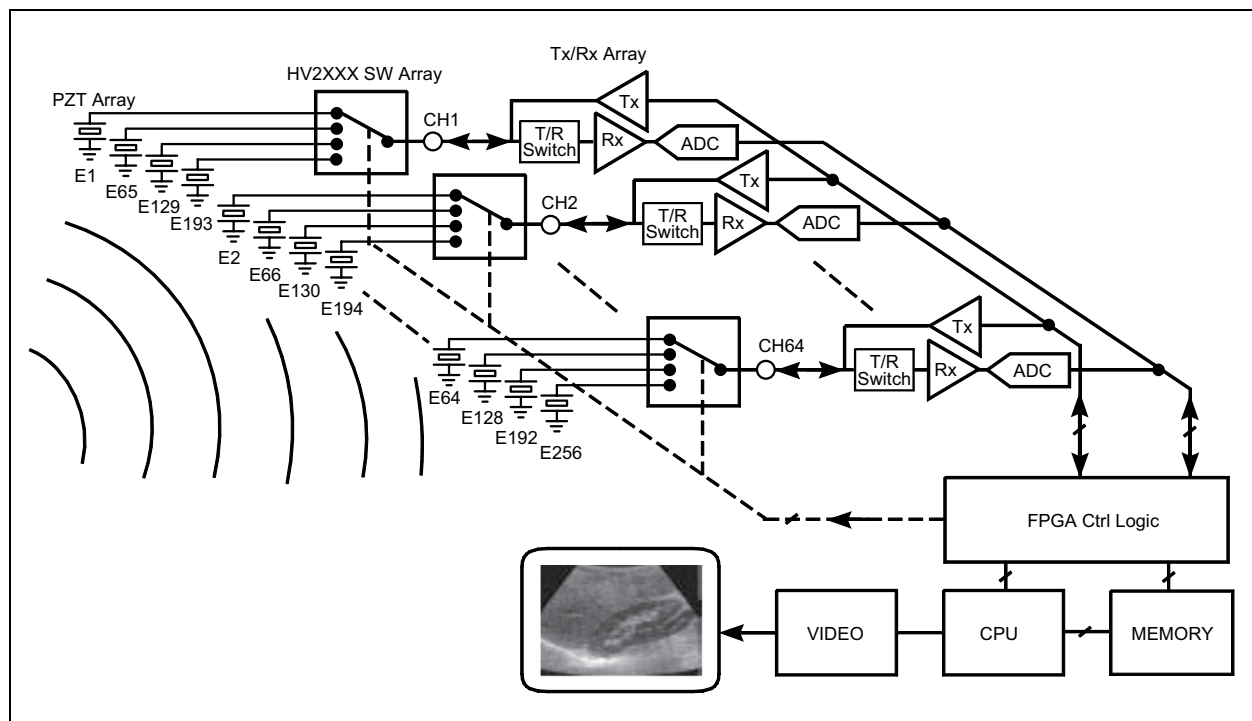


FIGURE 5-1: Typical Medical Ultrasound Imaging System.

HV2815/HV2915/HV2916

5.2 Logic Input Timing

HV2815/HV2915/HV2916 have a digital serial interface consisting of Data In (D_{IN}), Clock (CLK), Data Out (D_{OUT}), Latch Enable ($\overline{LE}$), and Clear (CLR) to control 32 switches independently.

The digital circuits are supplied by V_{LL} that are +3.3V or +5V. The serial clock frequency is up to 66 MHz.

The switch state configuration data, 32-bit D_{IN} , are shifted into the 32 shift registers on the rising edge of the clock (low-to-high transition) of the clock. The D_{OUT} has the same logic state of the 31st shift register data.

The switch configuration bit of SW31 is shifted in first and the Configuration bit of SW0 is shifted in last. To change all the switch ON/OFF states at the same time, the $\overline{LE}$ should remain high while the 32-bit Data In signal is shifted into the 32-bit register. After the valid

32-bit data complete shifting into the shift registers, the high-to-low transition of the $\overline{LE}$ signal transfers the contents of the shift registers into the latches. Finally, setting the $\overline{LE}$ back to high allows all the latches to keep the current state, while new data can be shifted into the shift registers without disturbing the latches.

It is recommended to change all the latch states at the same time through this method to avoid possible clock feed through noise (see Figure 5-2 for details).

When the CLR input is set high, it resets the data of all 32 latches to low. Consequently, all the high-voltage switches are set to the OFF state. However, the CLR signal does not affect the contents of the shift register, so the shift register can operate independently of the CLR signal. Therefore, the shift register still retains the previous data when the CLR input is low (see Table 1-1 for details).

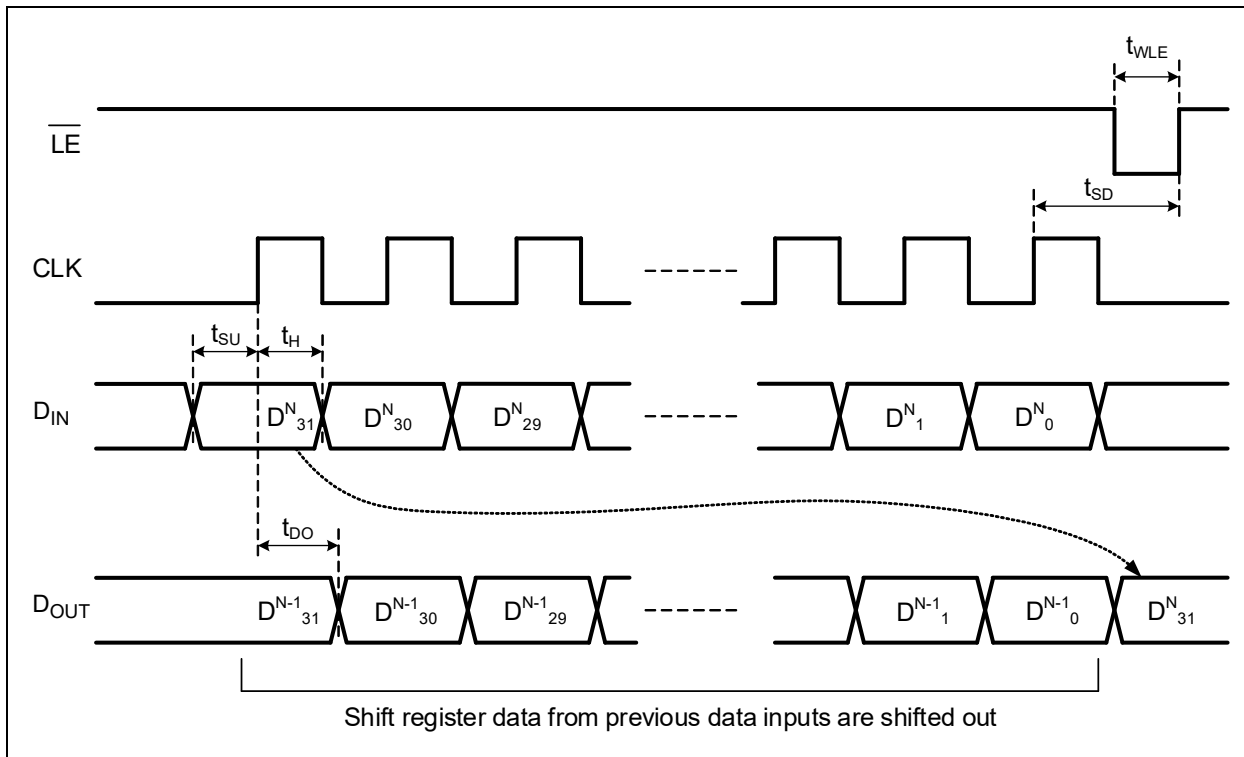


FIGURE 5-2: Latch Enable Timing Diagram.

5.3 Multiple Devices Connection

Multiple HV2815/HV2915/HV2916 devices can be connected in a daisy-chain through a digital serial interface. In a daisy-chain connection, D_{OUT} of the first device is connected to the D_{IN} of the second device, and so forth. The last D_{OUT} of the daisy-chained HV2815/HV2915/HV2916 can either be floating or fed back to an FPGA to check the previously stored shift register data. CLK, CLR and $\overline{LE}$ of daisy-chained devices can be connected to each other to save the number of control signals from FPGA.

To control all the high-voltage analog switch states of daisy-chained N devices, Nx32 clocks and Nx32 bits of data are shifted into shift registers, while $\overline{LE}$ remains high and CLR remains low. After all the data finish shifting in, one single negative pulse of $\overline{LE}$ transfers the data from shift registers to latches simultaneously. Consequently, all Nx32 high-voltage analog switches change states simultaneously.

5.4 Power-up/Down Sequence

The recommended power-up sequence of HV2815/HV2915/HV2916 is V_{LL} first, then V_{DD} . The power-down sequence is in reverse order of power-up. During the power-up/down period, all the analog switch inputs should be within V_{DD} and GND or floating.

5.5 Layout Considerations

The HV2815/HV2915/HV2916 devices have two separate ground connections. DGND is the ground connection for digital circuitry, and GND is the ground connection for substrate and analog switches. High

transient current passes through the switches and returns through GND in the ultrasound system. The high current path needs to be designed as short as possible to avoid ground bouncing.

It is recommended to use two separate ground planes in the PCB, connected together at the return terminal of the input power line, as shown in Figure 5-3. It is recommended that 0.1 μF , or larger, ceramic decoupling capacitors with low-Equivalent Series Resistance (low-ESR), and appropriate voltage rating be connected between DGND and power supplies, V_{LL} and V_{DD} . These decoupling capacitors should be placed as close as possible to the device in the PCB layout.

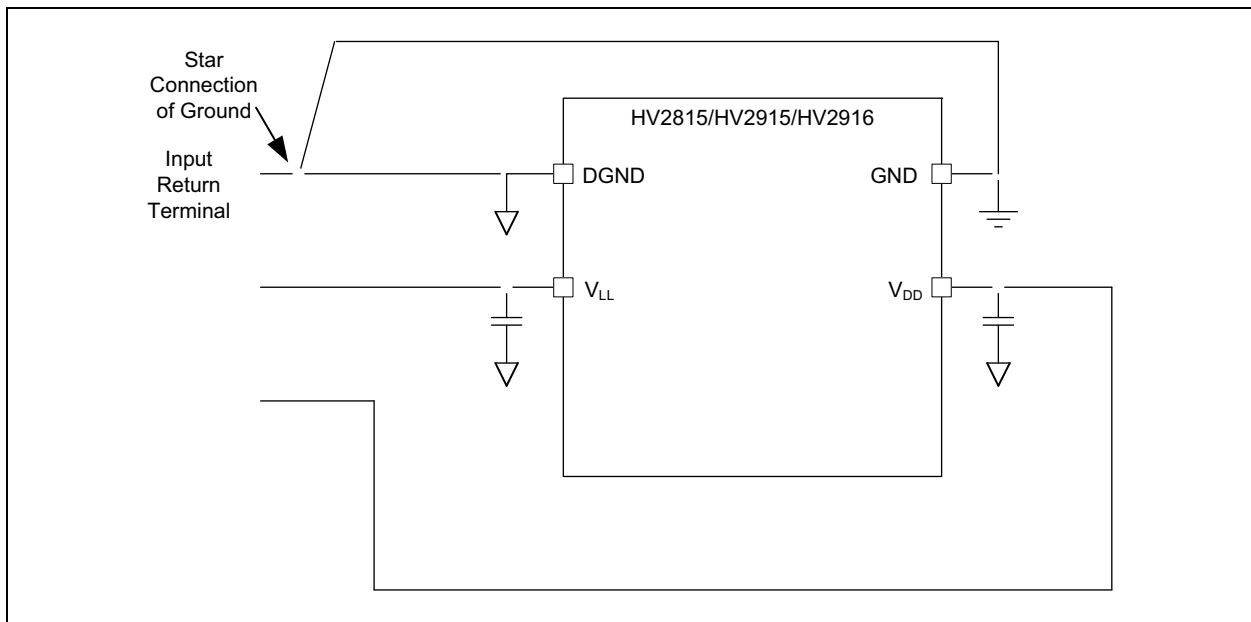


FIGURE 5-3: Layout Guidelines.

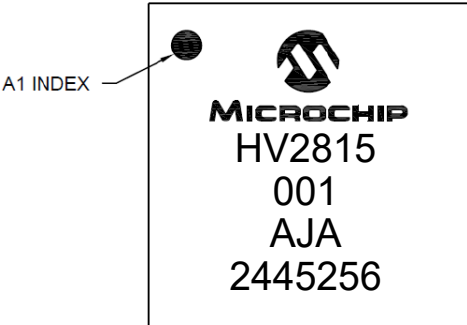
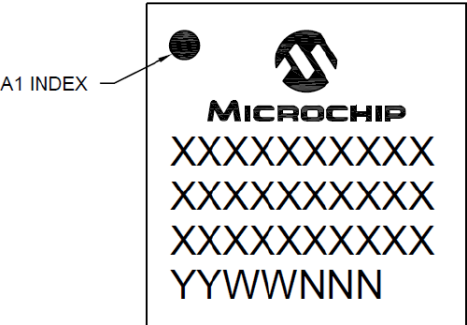
HV2815/HV2915/HV2916

6.0 PACKAGING INFORMATION

6.1 Package Marking Information

121-Lead TFBGA (10x10x1.2 mm)

Example

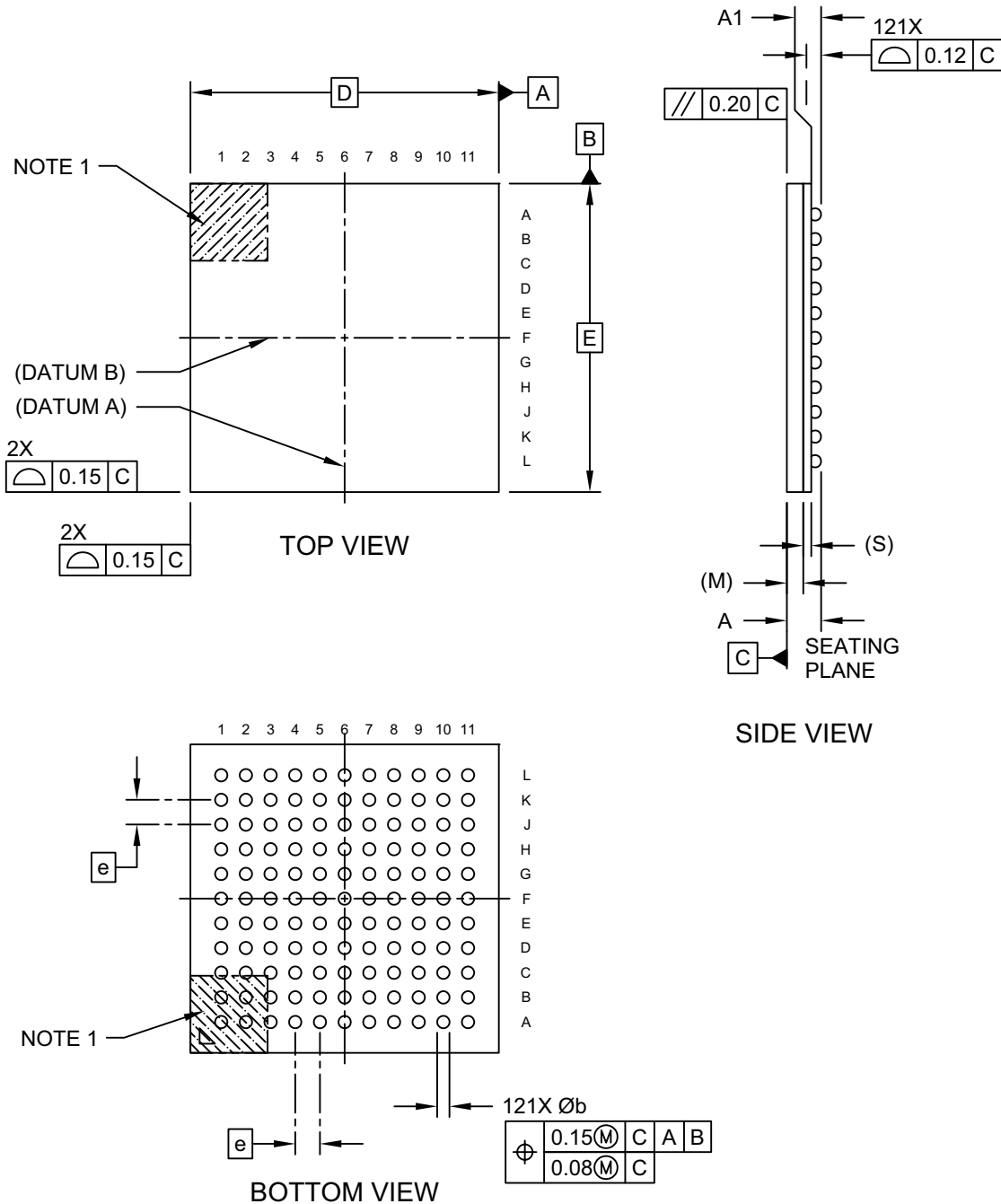


Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.		

HV2815/HV2915/HV2916

121-Ball Thin, Fine Pitch Ball Grid Array (AJA) - 10x10 mm Body [TFBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

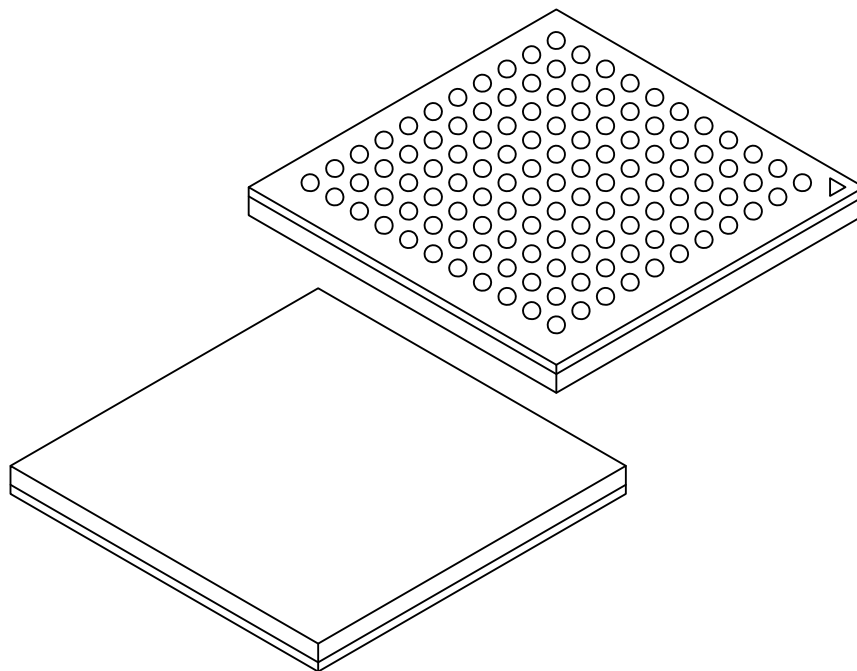


Microchip Technology Drawing C04-1216A Sheet 1 of 2

HV2815/HV2915/HV2916

121-Ball Thin, Fine Pitch Ball Grid Array (AJA) - 10x10 mm Body [TFBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N	121		
Pitch	e	0.80 BSC		
Overall Height	A	-	-	1.20
Terminal (ball) height	A1	0.270	-	0.37
Substrate Thickness	S	0.26 REF		
Mold Cap Thickness	M	0.53 REF		
Overall Length	D	10.00 BSC		
Overall Width	E	10.00 BSC		
Terminal Width	b	0.38	0.40	0.48

Notes:

1. Terminal A1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

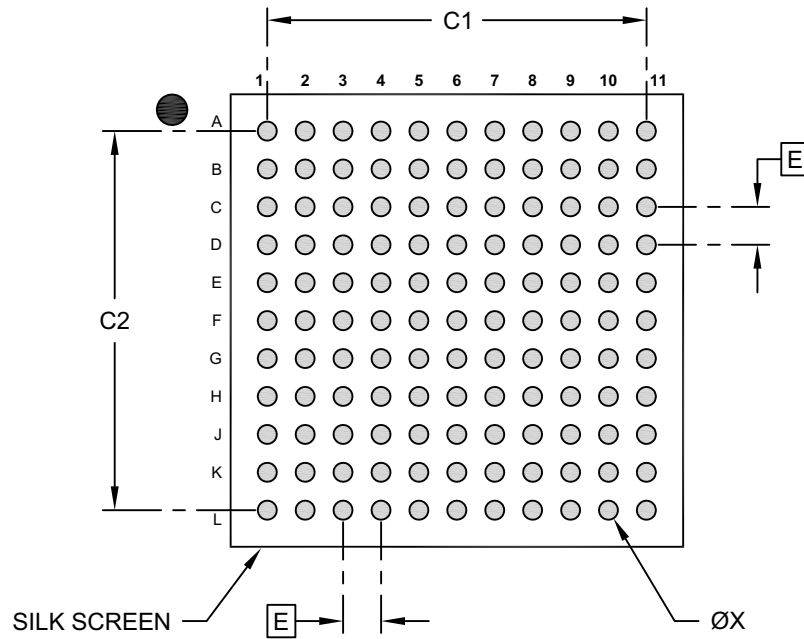
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1216A Sheet 2 of 2

HV2815/HV2915/HV2916

121-Ball Thin, Fine Pitch Ball Grid Array (AJA) - 10x10 mm Body [TFBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.80 BSC		
Contact Pad Spacing	C1		8.00	
Contact Pad Spacing	C2		8.00	
Contact Pad Diameter (X121)	X			0.40

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-3216A

HV2815/HV2915/HV2916

NOTES:

APPENDIX A: REVISION HISTORY

Revision C (November 2024)

The following is the list of modifications:

1. Updated the [DC Electrical Characteristics](#) table.
2. Updated the [AC Electrical Characteristics](#) table.

Revision B (September 2021)

The following is the list of modifications:

1. Updated the [Package Types](#) height information.
2. Updated the [DC Electrical Characteristics](#) table.
3. Updated the [AC Electrical Characteristics](#) table.
4. Updated [Figure 3-7](#).
5. Updated the [Typical Performance Curves](#).
6. Updated [Section 6.1 “Package Marking Information”](#).

Revision A (June 2021)

- Original release of this document.

HV2815/HV2915/HV2916

NOTES:

HV2815/HV2915/HV2916

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	<u>/XXX</u>
Device	Package
Device:	Examples:
HV2815: Single 5V Bias, Low Harmonic Distortion, 32-Channel High-Voltage Analog Switch	a) HV2815/AJA: Single 5V Bias, Low Harmonic Distortion, 32-Channel High-Voltage Analog Switch, Thin Fine Pitch Ball Grid Array (TFBGA), 121-Ball Package
HV2915: Single 5V Bias, Low Harmonic Distortion, 32-Channel High-Voltage Analog Switch with Bleed Resistor	b) HV2915/AJA: Single 5V Bias, Low Harmonic Distortion, 32-Channel High-Voltage Analog Switch with Bleed Resistor, Thin Fine Pitch Ball Grid Array (TFBGA), 121-Ball Package
HV2916: Single 5V Bias, Low Harmonic Distortion, 32-Channel High-Voltage Analog Switch with Bleed Resistor at One Side of Switch	c) HV2916/AJA: Single 5V Bias, Low Harmonic Distortion, 32-Channel High-Voltage Analog Switch with Bleed Resistor at One Side of Switch, Thin Fine Pitch Ball Grid Array (TFBGA), 121-Ball Package
Package:	
AJA = Thin Fine Pitch Ball Grid Array – 10x10x1.2mm (TFBGA), 121-Ball	

HV2815/HV2915/HV2916

NOTES:

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ISBN: 979-8-3371-0117-0

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