MCP6446/7/9

500 nA, 11 kHz Op Amp with ±2.2 mV Max. Offset

Features

- Low Quiescent Current: 500 nA (typical)
- Input Offset Voltage: ±2.2 mV Max
- Gain Bandwidth Product: 11 kHz (typical)
- Supply Voltage Range: 1.4V to 5.5V
- Rail-to-Rail Input and Output
- Unity Gain Stable
- Slew Rate: 3V/ms (typical)
- Extended Temperature Range: -40°C to +125°C
- No Phase Reversal
- Small Packages
- AEC-Q100 qualified, Grade 1

Applications

- Portable Equipment
- Battery Powered System
- Data Acquisition Equipment
- Sensor Conditioning
- Battery Current Sensing
- Analog Active Filters

Design Aids

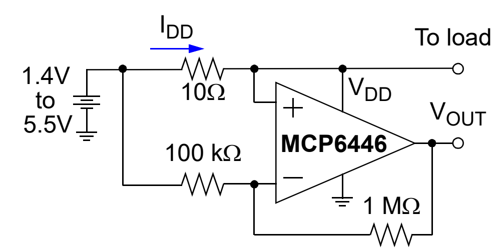
- SPICE Macro Models
- FilterLab® Software
- Microchip Advanced Part Selector (MAPS)
- Analog Demonstration and Evaluation Boards
- Application Notes

Description

The MCP6446/7/9 device is a single nanopower operational amplifier (op amp), which has low quiescent current (500 nA, typical) and rail-to-rail input and output operation. This op amp is unity gain stable and has a gain bandwidth product of 11 kHz (typical). These devices operate with a single supply voltage as low as 1.4V. These features make the family of op amps well suited for single-supply, battery-powered applications.

The MCP6446/7/9 op amp is designed with Microchip's advanced CMOS process and offered in single (MCP6446), dual (MCP6447), and quad (MCP6449) configurations. All devices are available in the extended temperature range, with a power supply range of 1.4V to 5.5V.

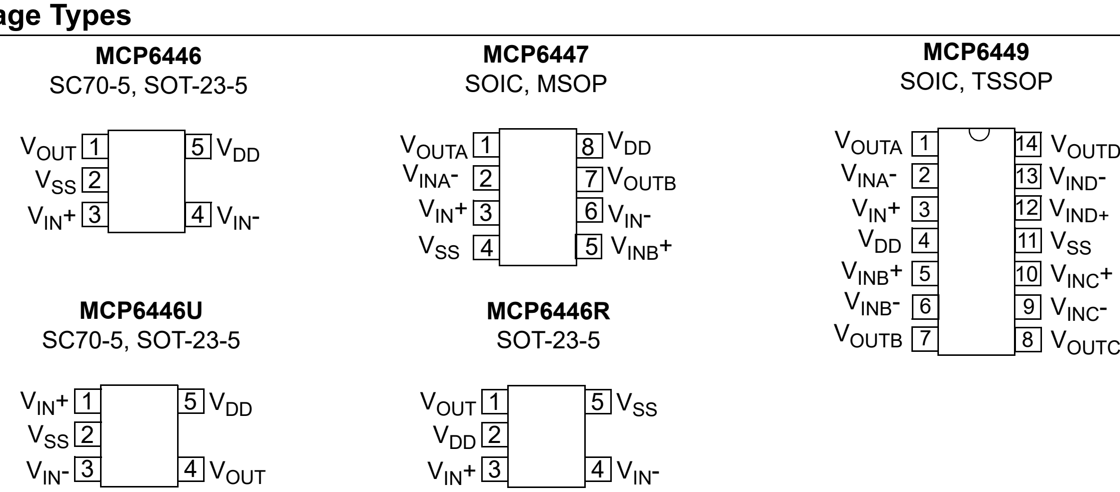
Typical Application



$$I_{DD} = \frac{V_{DD} - V_{OUT}}{(10\ V/V) \cdot (10\Omega)}$$

Battery Current Sensing

Package Types



1.0 ELECTRICAL CHARACTERISTICS

1.1 Absolute Maximum Ratings †

$V_{DD} – V_{SS}$ 6V
Current at Input Pins ....±5 mA
Analog Inputs (V_{IN}+, V_{IN}-)†† .... V_{SS} – 0.5V to V_{DD} + 0.5V
All Other Inputs and Outputs .... V_{SS} – 0.3V to V_{DD} + 0.3V
Difference Input Voltage .... $|V_{DD} – V_{SS}|$
Output Short-Circuit Current ....Continuous
Current at Output and Supply Pins ....±30 mA
Storage Temperature ....-65°C to +150°C
Maximum Junction Temperature (T_J) ....+150°C
ESD Protection on All Pins (HBM) ....≥ 2 kV

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

†† See **Section 4.1.2 “Input Voltage Limits”**.

DC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, V_{DD} = +1.4V to +5.5V, V_{SS}= GND, T_A= +25°C, V_{CM} = V_{DD}/4, $V_{OUT} \approx V_{DD}/2$, V_L = V_{DD}/2 and R_L = 1 MΩ to V_L. (Refer to Figure 1-1).

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Input Offset						
Input Offset Voltage	V_{OS}	-2.2	—	+2.2	mV	
Input Offset Drift with Temperature	$\Delta V_{OS}/\Delta T_A$	—	±2	—	µV/°C	T_A= -40°C to +125°C, V_{CM} = V_{DD}/4
Power Supply Rejection Ratio	PSRR	66	90	—	dB	V_{CM} = V_{DD}/4
Input Bias Current and Impedance						
Input Bias Current	I_B	—	±1	—	pA	
		—	20	—	pA	T_A = +85°C, V_{DD} = 3.3V
		—	80	—	pA	T_A = +125°C, V_{DD} = 3.3V
Input Offset Current	I_{OS}	—	±1	—	pA	
Common Mode Input Impedance	Z_{CM}	—	10^{13}‖6	—	Ω‖pF	
Differential Input Impedance	Z_{DIFF}	—	10^{13}‖6	—	Ω‖pF	
Common Mode						
Common Mode Input Voltage Range	V_{CMR}	V_{SS}-0.1V	—	V_{DD}+0.1V	V	T_A= -40°C to +125°C
Common Mode Rejection Ratio	CMRR	60	76	—	dB	V_{CM} = V_{CMR}, V_{DD} = 5.5V
Open-Loop Gain						
DC Open-Loop Gain (Large Signal)	A_{OL}	85	110	—	dB	V_{OUT} = 0.2V to V_{DD}-0.2V R_L = 10 kΩ to V_L
Output						
Maximum Output Voltage Swing	V_{OL}, V_{OH}	V_{SS}+50	—	V_{DD}–50	mV	V_{DD} = 5.5V, R_L = 50 kΩ 0.5V input overdrive
Output Short-Circuit Current	I_{SC}	—	±0.5	—	mA	V_{DD} = 1.4V
		—	±7	—	mA	V_{DD} = 5.5V
Power Supply						
Supply Voltage	V_{DD}	1.4	—	5.5	V	
Quiescent Current per Amplifier	I_Q	300	500	760	nA	I_O = 0, V_{DD} = 5.5V

AC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.4V to +5.5V, V_{SS} = GND, $V_{CM} = V_{DD}/4$, $V_{OUT} \approx V_{DD}/2$, $V_L = V_{DD}/2$, R_L = 1 MΩ to V_L and C_L = 30 pF. (Refer to Figure 1-1).

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
AC Response						
Gain Bandwidth Product	GBWP	—	11	—	kHz	
Phase Margin	PM	—	65	—	°	G = +1 V/V
Slew Rate	SR	—	3	—	V/ms	
Noise						
Input Noise Voltage	E_{ni}	—	16	—	µVp-p	f = 0.1 Hz to 10 Hz
Input Noise Voltage Density	e_{ni}	—	244	—	nV/√Hz	f = 1 kHz
Input Noise Current Density	i_{ni}	—	0.6	—	fA/√Hz	f = 1 kHz
Electromagnetic Interference Rejection Ratio	EMIRR	—	80	—	dB	V_{IN} = 0.1 V_{PK}, f = 400 MHz
		—	85	—	dB	V_{IN} = 0.1 V_{PK}, f = 900 MHz
		—	90	—	dB	V_{IN} = 0.1 V_{PK}, f = 1.8 GHz
		—	95	—	dB	V_{IN} = 0.1 V_{PK}, f = 24 GHz
		—	100	—	dB	V_{IN} = 0.1 V_{PK}, f = 5.8 GHz

TEMPERATURE SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, V_{DD} = +1.4V to +5.5V and V_{SS} = GND.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Temperature Ranges						
Operating Temperature Range	T_A	-40	—	+125	°C	Note 1
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 5L-SOT-23	θ_{JA}	—	220.7	—	°C/W	
Thermal Resistance, 8L-MSOP	θ_{JA}	—	211	—	°C/W	
Thermal Resistance, 8L-SOIC	θ_{JA}	—	149.5	—	°C/W	
Thermal Resistance, 14L-SOIC	θ_{JA}	—	95.3	—	°C/W	
Thermal Resistance, 14L-TSSOP	θ_{JA}	—	100	—	°C/W	

Note 1: The internal junction temperature (T_J) must not exceed the absolute maximum specification of +150°C.

1.2 Test Circuits

The circuit used for most DC and AC tests is shown in Figure 1-1. This circuit can independently set V_{CM} and V_{OUT} (see Equation 1-1). Note that V_{CM} is not the circuit's Common Mode voltage ($(V_P + V_M)/2$), and that V_{OST} includes V_{OS} plus the effects (on the input offset error, V_{OST}) of the temperature, CMRR, PSRR and A_{OL}.

EQUATION 1-1:

$$G_{DM} = R_F / R_G$$
$$V_{CM} = (V_P + V_{DD}/2)/2$$
$$V_{OST} = V_{IN-} - V_{IN+}$$
$$V_{OUT} = (V_{DD}/2) + (V_P - V_M) + V_{OST}(1 + G_{DM})$$

Where:

G_{DM}	=	Differential Mode Gain	(V/V)
V_{CM}	=	Op Amp's Common Mode Input Voltage	(V)
V_{OST}	=	Op Amp's Total Input Offset Voltage	(mV)

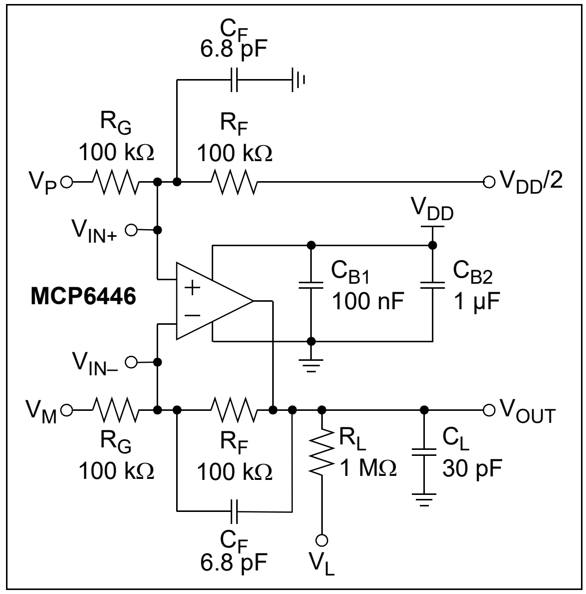


FIGURE 1-1: *AC and DC Test Circuit for Most Specifications.*

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.4V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/4, $V_{OUT} \approx V_{DD}$/2, V_L = V_{DD}/2, R_L = 1 MΩ to V_L and C_L = 30 pF.

2.1 DC Inputs

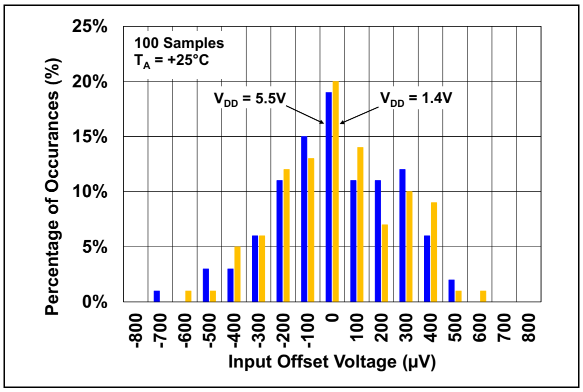


FIGURE 2-1: Input Offset Voltage Histogram.

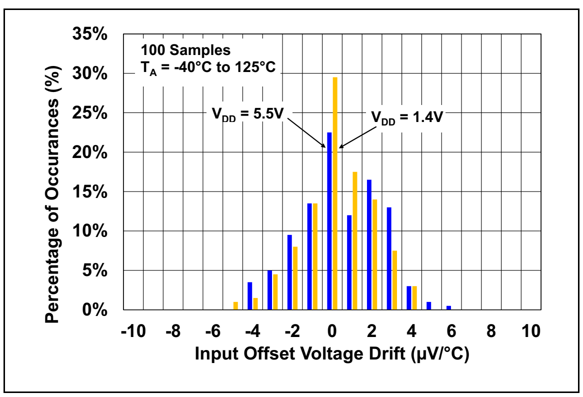


FIGURE 2-2: Input Offset Voltage Drift Histogram.

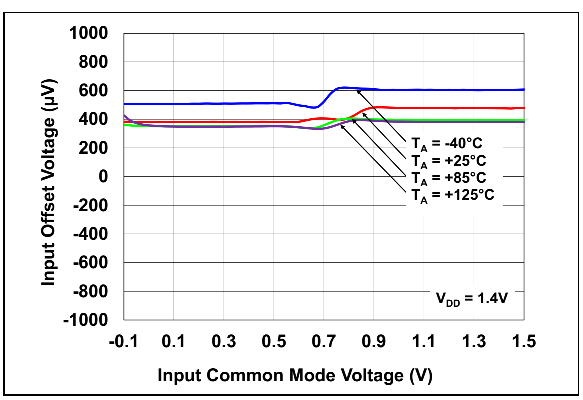


FIGURE 2-3: Input Offset Voltage vs. Common Mode Input Voltage.

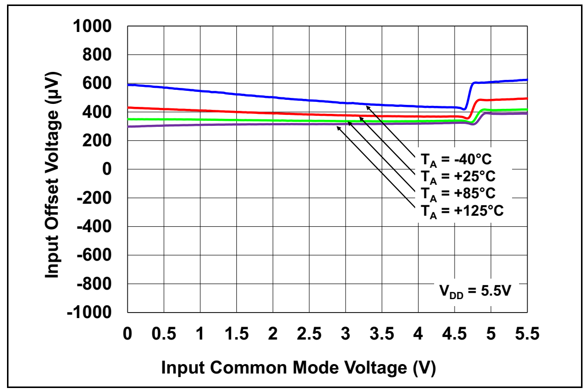


FIGURE 2-4: Input Offset Voltage vs. Common Mode Input Voltage.

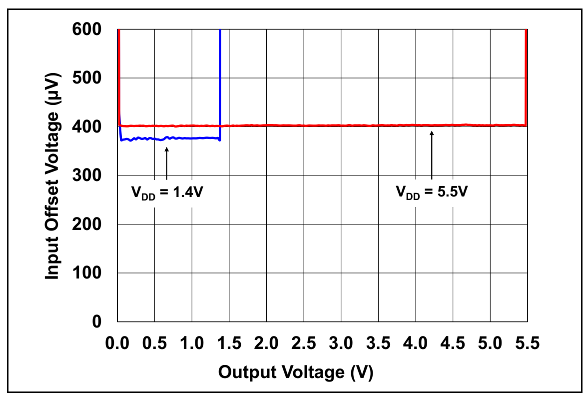


FIGURE 2-5: Input Offset Voltage vs. Output Voltage.

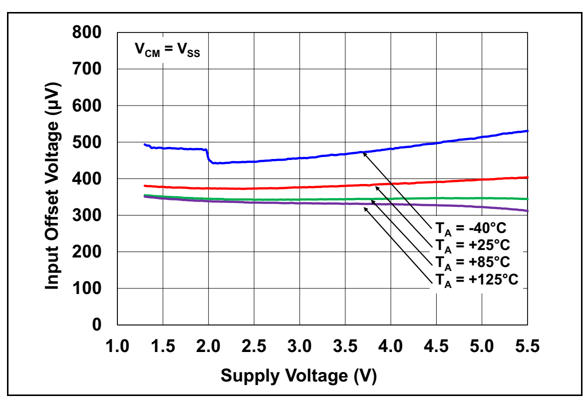


FIGURE 2-6: Input Offset Voltage vs. Power Supply Voltage.

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.4V to +5.5V, V_{SS} = GND, V_{CM} = $V_{DD}/4$, $V_{OUT} \approx V_{DD}/2$, $V_L = V_{DD}/2$, R_L = 1 MΩ to V_L and C_L = 30 pF.

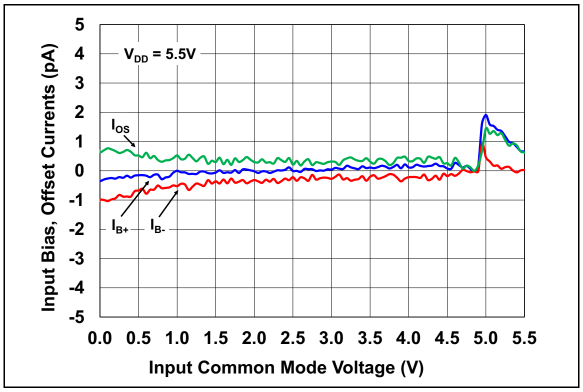


FIGURE 2-7: *Input Bias, Offset Currents vs. Common Mode Input Voltage.*

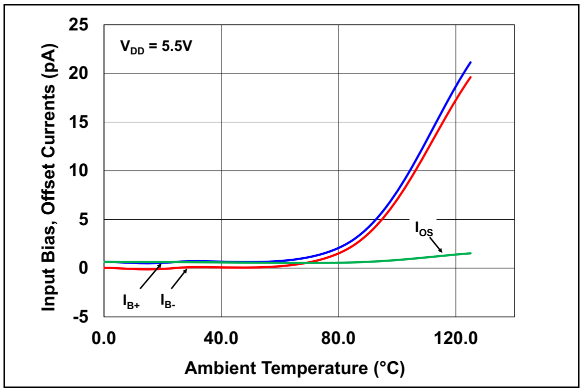


FIGURE 2-8: *Input Bias, Offset Currents vs. Common Mode Input Voltage.*

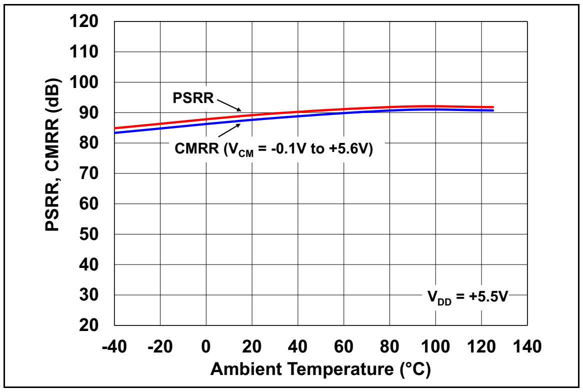


FIGURE 2-9: *CMRR, PSRR vs. Ambient Temperature.*

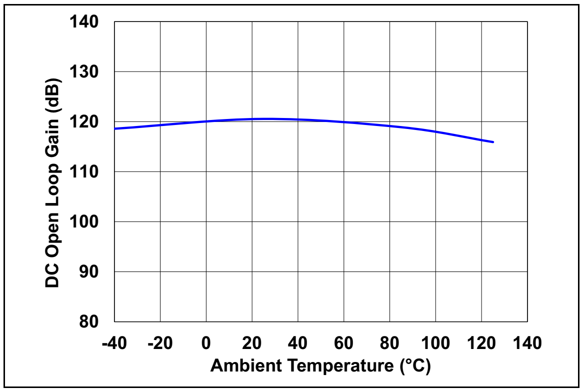


FIGURE 2-10: *DC Open-Loop Gain vs. Ambient Temperature.*

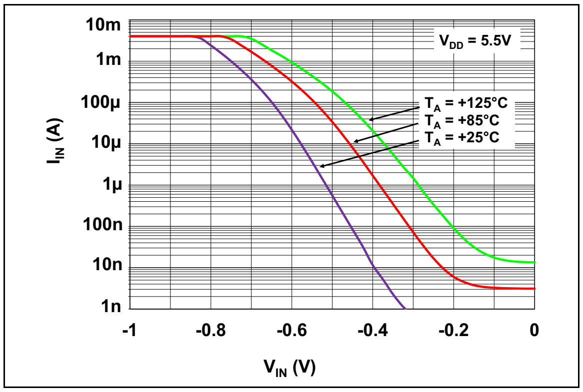


FIGURE 2-11: *Measured Input Current vs. Input Voltage (below V_{SS}).*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.4V to +5.5V, V_{SS} = GND, V_{CM} = $V_{DD}/4$, $V_{OUT} \approx V_{DD}/2$, V_L = $V_{DD}/2$, R_L = 1 MΩ to V_L and C_L = 30 pF.

2.2 Other DC Voltages and Currents

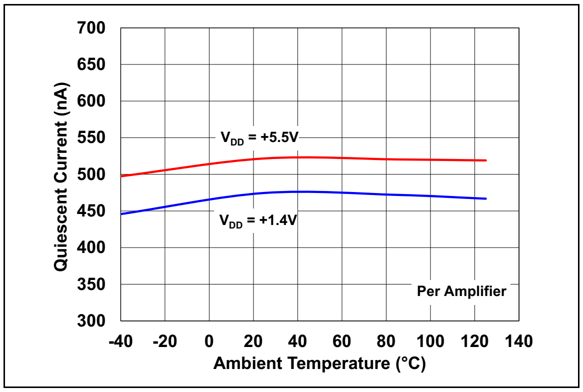


FIGURE 2-12: *Quiescent Current vs. Ambient Temperature.*

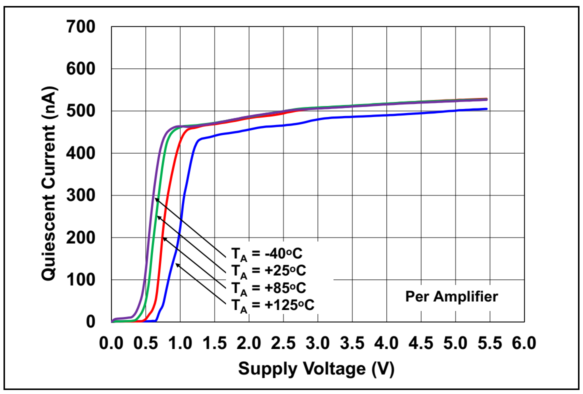


FIGURE 2-13: *Quiescent Current vs. Power Supply Voltage.*

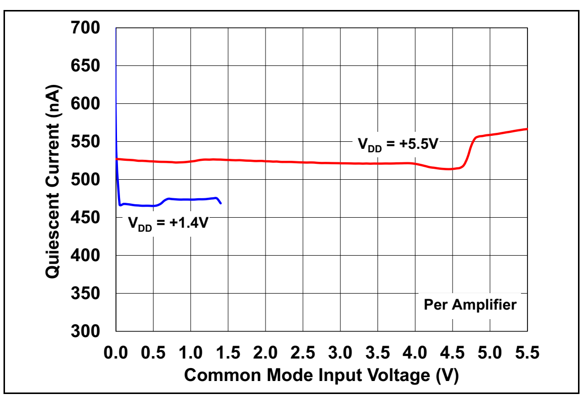


FIGURE 2-14: *Quiescent Current vs. Common-Mode Input Voltage.*

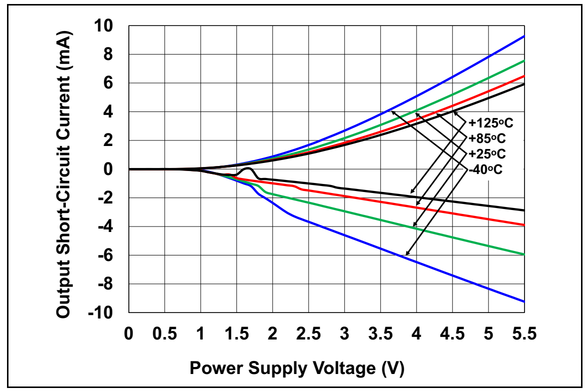


FIGURE 2-15: *Output Short-Circuit Current vs. Power Supply Voltage.*

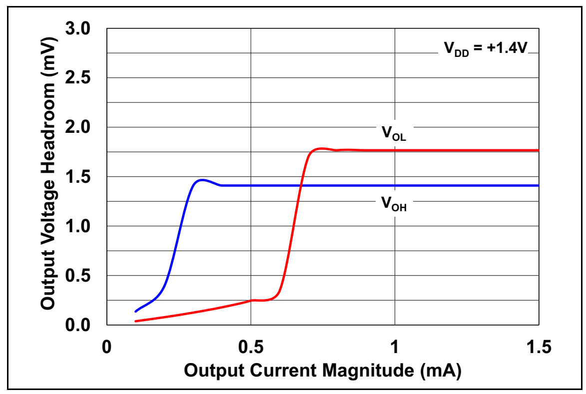


FIGURE 2-16: *Output Voltage Headroom vs. Output Current.*

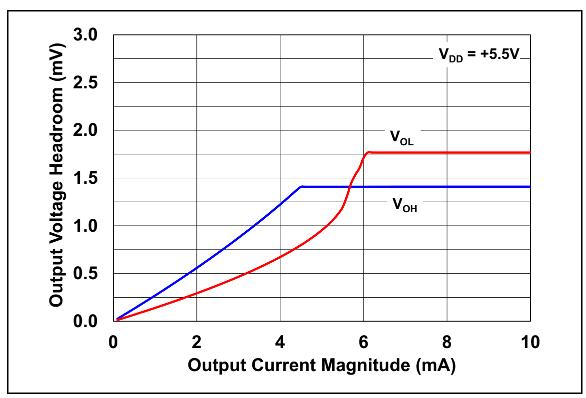


FIGURE 2-17: *Output Voltage Headroom vs. Output Current.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.4V to +5.5V, V_{SS} = GND, V_{CM} = $V_{DD}/4$, $V_{OUT} \approx V_{DD}/2$, $V_L = V_{DD}/2$, R_L = 1 MΩ to V_L and C_L = 30 pF.

2.3 Frequency Response

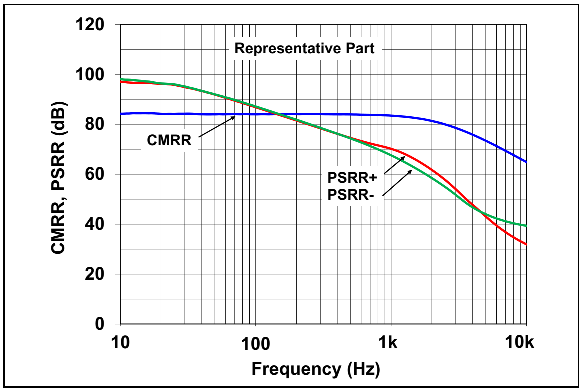


FIGURE 2-18: *CMRR, PSRR vs. Frequency.*

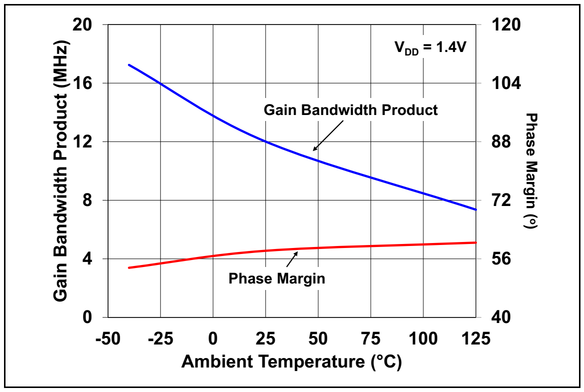


FIGURE 2-21: *Gain Bandwidth Product, Phase Margin vs. Ambient Temperature.*

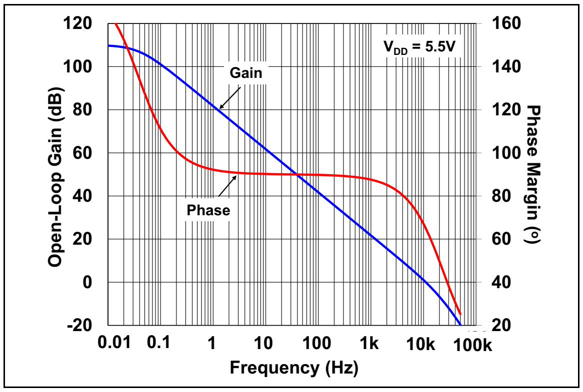


FIGURE 2-19: *Open-Loop Gain, Phase vs. Frequency.*

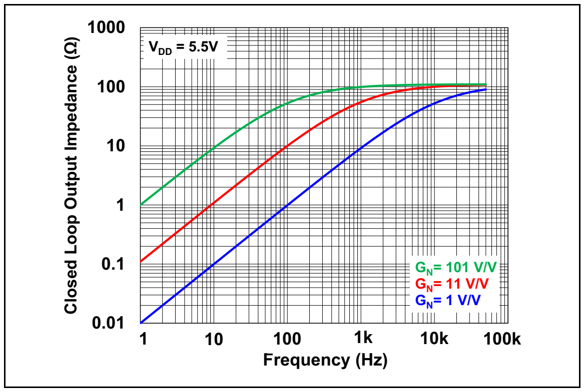


FIGURE 2-22: *Closed-Loop Output Impedance vs. Frequency.*

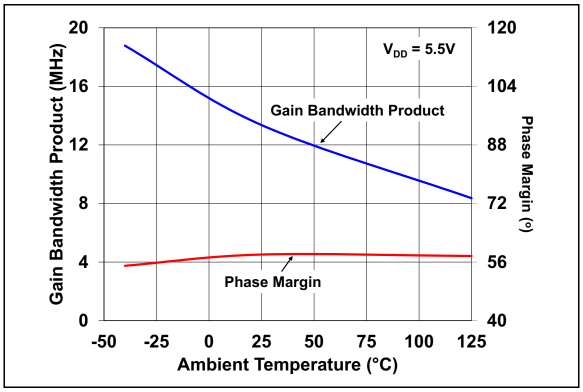


FIGURE 2-20: *Gain Bandwidth Product, Phase Margin vs. Ambient Temperature.*

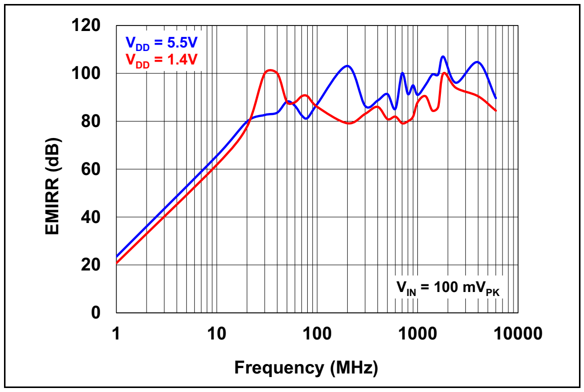


FIGURE 2-23: *EMIRR vs. Frequency.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.4V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/4, $V_{OUT} \approx V_{DD}$/2, V_L = V_{DD}/2, R_L = 1 MΩ to V_L and C_L = 30 pF.

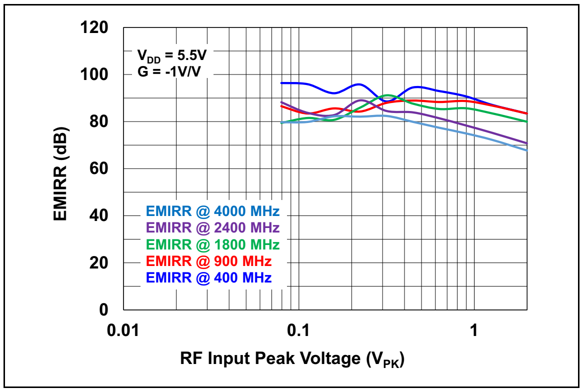


FIGURE 2-24: *EMIRR vs. RF Input Peak-to-Peak Voltage.*

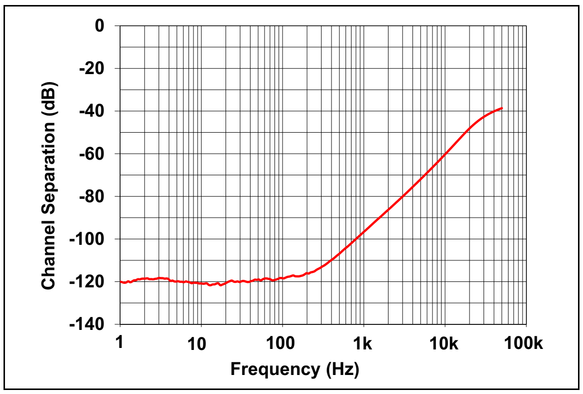


FIGURE 2-25: *Channel Separation vs. Frequency.*

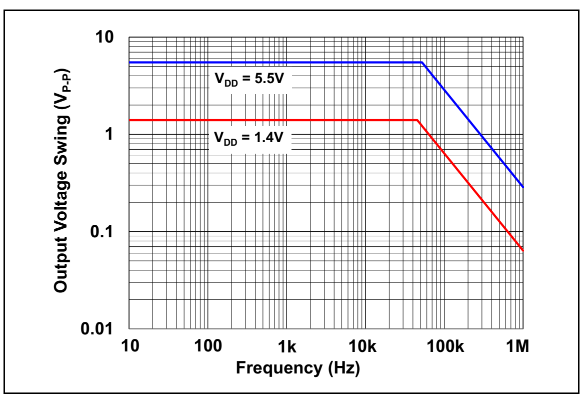


FIGURE 2-26: *Maximum Output Voltage Swing vs. Frequency.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.4V to +5.5V, V_{SS} = GND, V_{CM} = $V_{DD}/4$, $V_{OUT} \approx V_{DD}/2$, V_L = $V_{DD}/2$, R_L = 1 MΩ to V_L and C_L = 30 pF.

2.4 Input Noise

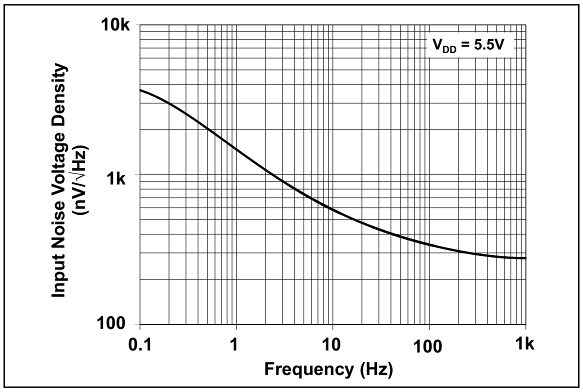


FIGURE 2-27: *Input Noise Voltage Density vs. Frequency.*

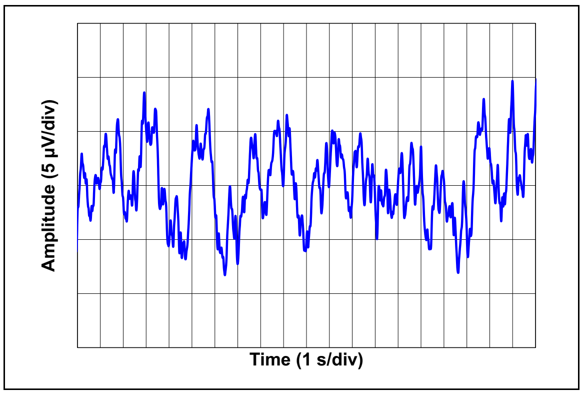


FIGURE 2-28: *0.1 Hz to 10 Hz Voltage Noise.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.4V to +5.5V, V_{SS} = GND, V_{CM} = $V_{DD}/4$, $V_{OUT} \approx V_{DD}/2$, $V_L = V_{DD}/2$, R_L = 1 MΩ to V_L and C_L = 30 pF.

2.5 Time Response

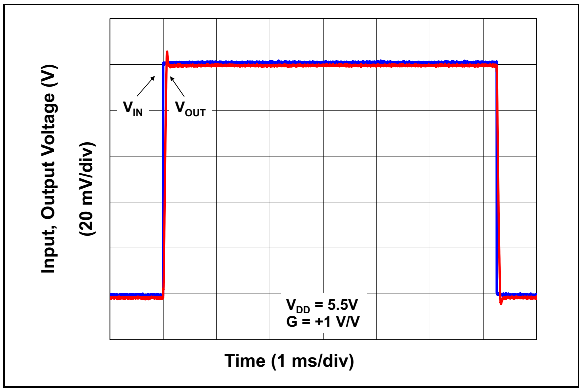


FIGURE 2-29: *Small Signal Noninverting Pulse Response.*

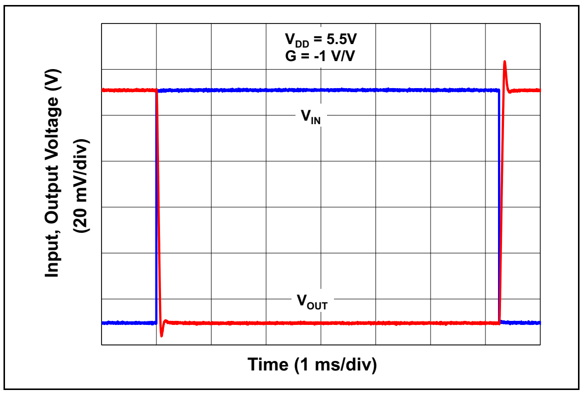


FIGURE 2-30: *Small Signal Inverting Pulse Response.*

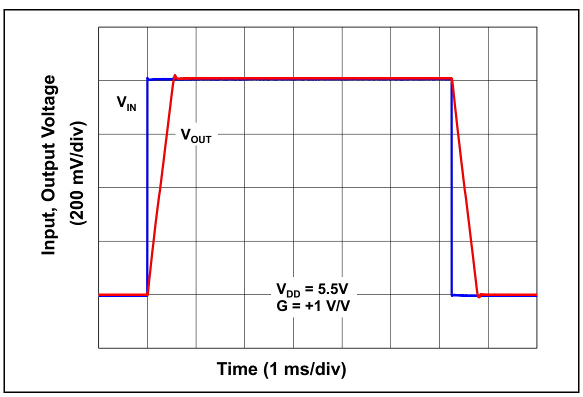


FIGURE 2-31: *Large Signal Noninverting Pulse Response.*

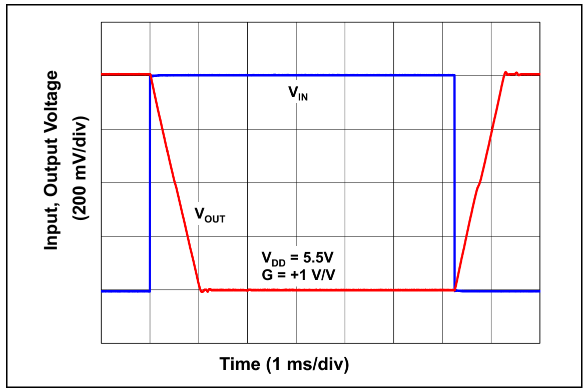


FIGURE 2-32: *Large Signal Inverting Pulse Response.*

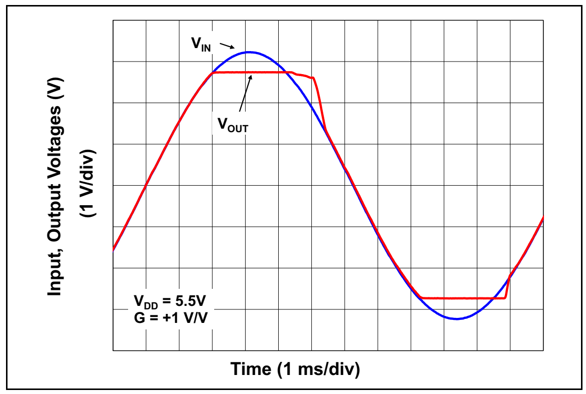


FIGURE 2-33: *The MCP6446/7/9 Device Shows No Phase Reversal.*

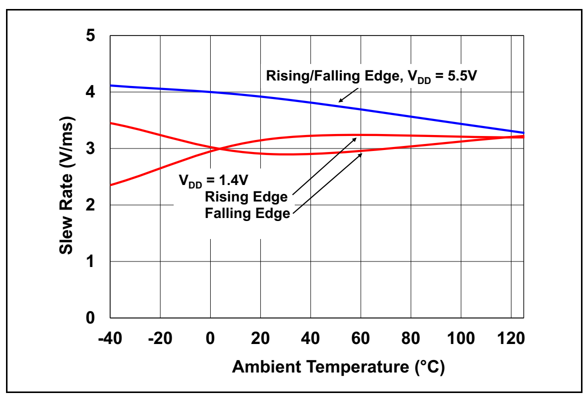


FIGURE 2-34: *Slew Rate vs. Ambient Temperature.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.4V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/4, $V_{OUT} \approx V_{DD}$/2, V_L = V_{DD}/2, R_L = 1 MΩ to V_L and C_L = 30 pF.

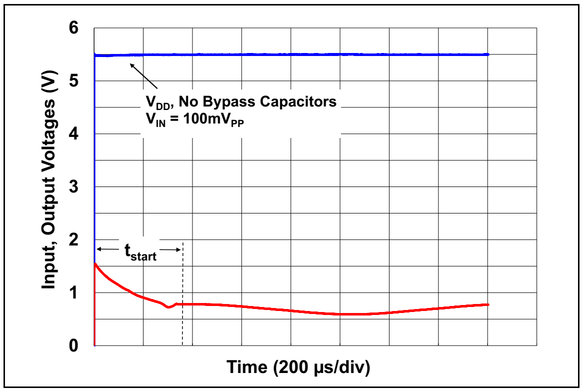


FIGURE 2-35: *Start-up Time.*

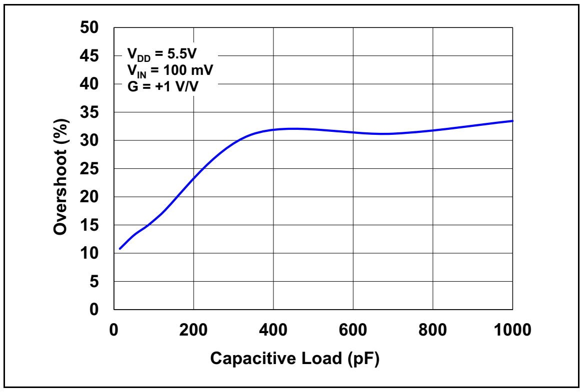


FIGURE 2-36: *Overshoot vs. Capacitive Load.*

3.0 PIN DESCRIPTIONS

Descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

MCP6446	MCP6446R	MCP6446U	MCP6447	MCP6449	Symbol	Description
SOT-23-5	SOT-23-5	SOT-23-5	SOIC, MSOP	SOIC, TSSOP		
1	1	4	1	1	V_{OUT}, V_{OUTA}	Analog Output (op amp A)
4	4	3	2	2	$V_{IN}–$, $V_{INA}–$	Inverting Input (op amp A)
3	3	1	3	3	$V_{IN}+$, $V_{INA}+$	Noninverting Input (op amp A)
5	2	5	8	4	V_{DD}	Positive Power Supply
—	—	—	5	5	$V_{INB}+$	Noninverting Input (op amp B)
—	—	—	6	6	$V_{INB}-$	Inverting Input (op amp B)
—	—	—	7	7	V_{OUTB}	Analog Output (op amp B)
—	—	—	—	8	V_{OUTC}	Analog Output (op amp C)
—	—	—	—	9	$V_{INC}-$	Inverting Input (op amp C)
—	—	—	—	10	$V_{INC}+$	Noninverting Input (op amp C)
2	5	2	4	11	V_{SS}	Negative Power Supply
—	—	—	—	12	$V_{IND}+$	Noninverting Input (op amp D)
—	—	—	—	13	$V_{IND}-$	Inverting Input (op amp D)
—	—	—	—	14	V_{OUTD}	Analog Output (op amp D)
—	—	—	—	—	EP	Exposed Thermal Pad (EP); must be connected to V_{SS}

3.1 Analog Output (V_{OUT})

The output pin is a low-impedance voltage source.

3.2 Power Supply Pins (V_{DD}, V_{SS})

The positive power supply (V_{DD}) is 1.4V to 5.5V higher than the negative power supply (V_{SS}). For normal operation, the other pins are at voltages between V_{SS} and V_{DD}.

Typically, these parts are used in a single (positive) supply configuration. In this case, V_{SS} is connected to ground and V_{DD} is connected to the supply. V_{DD} will need bypass capacitors.

3.3 Analog Inputs ($V_{IN}+$, $V_{IN}-$)

The noninverting and inverting inputs are high-impedance CMOS inputs with low bias currents.

4.0 APPLICATION INFORMATION

The MCP6446/7/9 op amp is manufactured using Microchip's state-of-the-art CMOS process, specifically designed for low power applications.

4.1 Rail-to-Rail Input

4.1.1 PHASE REVERSAL

The MCP6446/7/9 op amp is designed to prevent phase reversal, when the input pins exceed the supply voltages. Figure 2-33 shows the input voltage exceeding the supply voltage with no phase reversal.

4.1.2 INPUT VOLTAGE LIMITS

In order to prevent damage and/or improper operation of the amplifier, the circuit must limit the voltages at the input pins (see **Section 1.1, Absolute Maximum Ratings †**).

The Electrostatic Discharge (ESD) protection on the inputs can be depicted as shown in Figure 4-1. This structure was chosen to protect the input transistors against many, but not all, over-voltage conditions, and to minimize the input bias current (I_B).

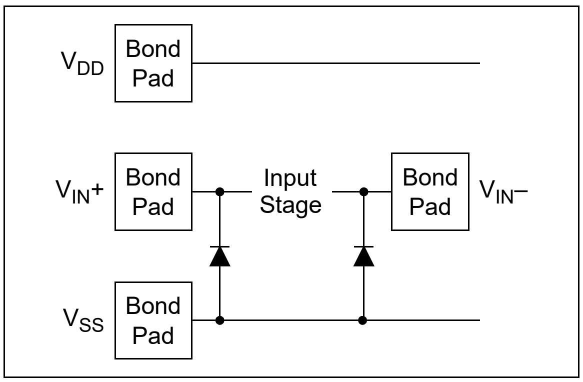


FIGURE 4-1: *Simplified Analog Input ESD Structures.*

The input ESD diodes clamp the inputs when they try to go more than one diode drop below V_{SS}. They also clamp any voltages that go well above V_{DD}; their breakdown voltage is high enough to allow normal operation, but not low enough to protect against slow over-voltage (beyond V_{DD}) events. Very fast ESD events that meet the spec are limited so that damage does not occur.

In some applications, it may be necessary to prevent excessive voltages from reaching the op amp inputs; Figure 4-2 shows one approach to protecting these inputs.

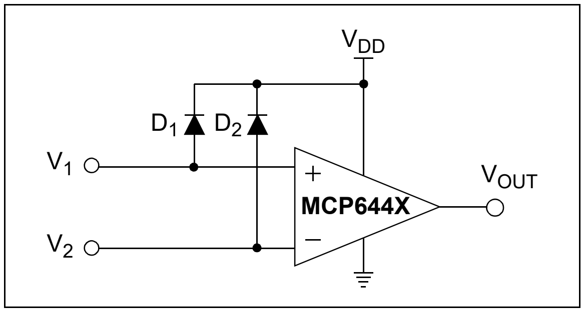


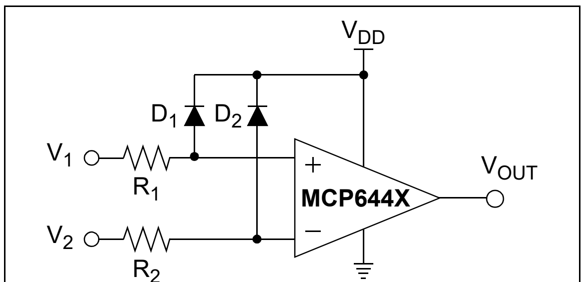
FIGURE 4-2: *Protecting the Analog Inputs.*

A significant amount of current can flow out of the inputs when the Common Mode voltage (V_{CM}) is below V_{CMR}, see Figure 2-11.

4.1.3 INPUT CURRENT LIMITS

In order to prevent damage and/or improper operation of the amplifier, the circuit must limit the currents into the input pins (see **Section 1.1 "Absolute Maximum Ratings †"**).

Figure 4-3 shows one approach to protecting these inputs. The resistors R_1 and R_2 limit the possible currents in or out of the input pins (and the ESD diodes, D_1 and D_2). The diode currents will go through either V_{DD} or V_{SS}.



$$min(R_1,R_2) > \frac{V_{SS} - min(V_1, V_2)}{2\ mA}$$

$$min(R_1,R_2) > \frac{max(V_1,V_2) - V_{DD}}{2\ mA}$$

FIGURE 4-3: *Protecting the Analog Inputs.*

4.1.4 NORMAL OPERATION

The input stage of the MCP6446/7/9 op amp uses two differential input stages in parallel. One operates at a low Common Mode input voltage (V_{CM}), while the other operates at a high V_{CM}. With this topology, the device operates with a V_{CM} up to 100 mV above V_{DD} and 100 mV below V_{SS}. The input offset voltage is measured at $V_{CM} = V_{SS} - 0.1V$ and $V_{DD} + 0.1V$, to ensure proper operation.

The transition between the input stages occurs when V_{CM} is near V_{DD} – 0.6V (see Figure 2-3 and Figure 2-4). For the best distortion performance and gain linearity, with noninverting gains, avoid this region of operation.

4.2 Rail-to-Rail Output

The output voltage range of the MCP6446/7/9 op amp is V_{SS} + 50 mV (minimum) and V_{DD} – 50 mV (maximum) when R_L = 50 kΩ is connected to $V_{DD}/2$ and V_{DD} = 5.5V. Refer to Figure 2-16 and Figure 2-17 for more information.

4.3 Capacitive Loads

Driving large capacitive loads can cause stability problems for voltage feedback op amps. As the load capacitance increases, the feedback loop's phase margin decreases, and the closed-loop bandwidth is reduced. This produces gain peaking in the frequency response, with overshoot and ringing in the step response. While a unity-gain buffer (G = +1 V/V) is the most sensitive to the capacitive loads, all gains show the same general behavior.

When driving large capacitive loads with the MCP6446/7/9 op amp (e.g., > 100 pF when G = +1 V/V), a small series resistor at the output (R_{ISO} in Figure 4-4) improves the feedback loop's phase margin (stability) by making the output load resistive at higher frequencies. The bandwidth will be generally lower than the bandwidth with no capacitance load.

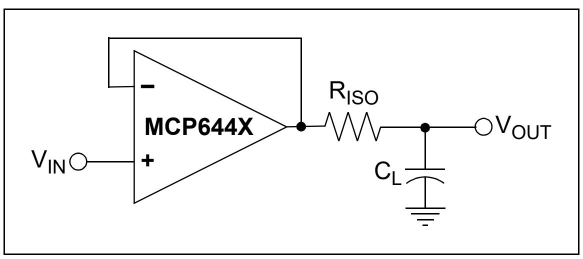


FIGURE 4-4: *Output Resistor, R_{ISO} Stabilizes Large Capacitive Loads.*

Figure 4-5 gives the recommended R_{ISO} values for the different capacitive loads and gains. The x-axis is the normalized load capacitance (C_L/G_N), where G_N is the circuit's noise gain. For noninverting gains, G_N and the Signal Gain are equal. For inverting gains, G_N is 1+|Signal Gain| (e.g., -1 V/V gives G_N = +2 V/V).

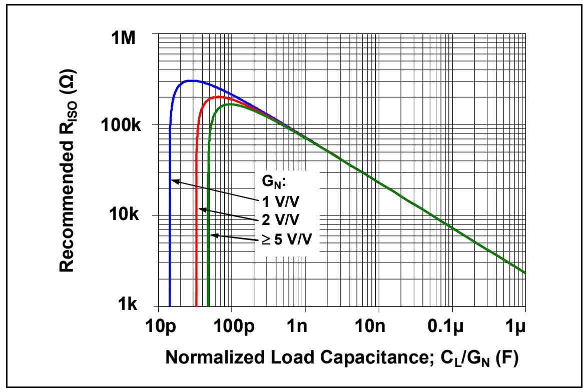


FIGURE 4-5: *Recommended R_{ISO} Values for Capacitive Loads.*

After selecting R_{ISO} for your circuit, double-check the resulting frequency response peaking and step response overshoot. Modify R_{ISO}'s value until the response is reasonable. Bench evaluation and simulations with the MCP6446/7/9 SPICE macro model are very helpful.

4.4 Supply Bypass

The MCP6446/7/9 op amp's power supply pin (V_{DD} for single-supply) should have a local bypass capacitor (i.e., 0.01 µF to 0.1 µF) within 2 mm for good high frequency performance. It can use a bulk capacitor (i.e., 1 µF or larger) within 100 mm to provide large, slow currents. This bulk capacitor can be shared with other analog parts.

4.5 PCB Surface Leakage

In applications where low input bias current is critical, Printed Circuit Board (PCB) surface leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is 10^{12}Ω. A 5V difference would cause 5 pA of current to flow, which is greater than the MCP6446/7/9 op amp's bias current at +25°C (±1 pA, typical).

The easiest way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in Figure 4-6.

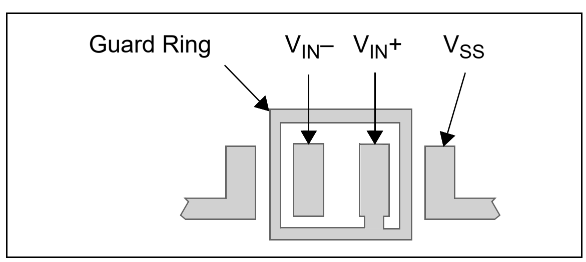


FIGURE 4-6: *Example Guard Ring Layout for Inverting Gain.*

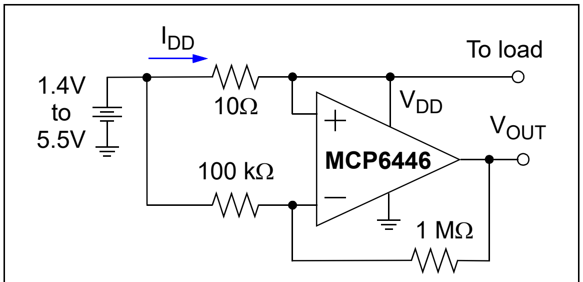
1. Noninverting Gain and Unity-Gain Buffer:
   a) Connect the noninverting pin ($V_{IN}+$) to the input with a wire that does not touch the PCB surface.
   b) Connect the guard ring to the inverting input pin ($V_{IN}–$). This biases the guard ring to the Common Mode input voltage.
2. Inverting Gain and Transimpedance Gain Amplifiers (convert current to voltage, such as photo detectors):
   a) Connect the guard ring to the noninverting input pin ($V_{IN}+$). This biases the guard ring to the same reference voltage as the op amp (e.g., $V_{DD}/2$ or ground).
   b) Connect the inverting pin ($V_{IN}–$) to the input with a wire that does not touch the PCB surface.

4.6 Application Circuits

4.6.1 BATTERY CURRENT SENSING

The MCP6446/7/9 op amp's Common Mode Input Range, which goes 0.1V beyond both supply rails, supports their use in high-side and low-side battery current sensing applications. The low quiescent current (500 nA, typical) helps prolong battery life, and the rail-to-rail output supports detection of low currents.

Figure 4-7 shows a high side battery current sensor circuit. The 10Ω resistor is sized to minimize power losses. The battery current (I_{DD}) through the 10Ω resistor causes its top terminal to be more negative than the bottom terminal. This keeps the Common Mode input voltage of the op amp below V_{DD}, which is within its allowed range. The output of the op amp will also be below V_{DD}, within its Maximum Output Voltage Swing specification.



$$I_{DD} = \frac{V_{DD} - V_{OUT}}{(10\ V/V) \cdot (10\Omega)}$$

FIGURE 4-7: *Battery Current Sensing.*

4.6.2 PRECISION HALF-WAVE RECTIFIER

The precision half-wave rectifier, which is also known as a super diode, is a configuration obtained with an operational amplifier in order to have a circuit behaving like an ideal diode and rectifier. It effectively cancels the forward voltage drop of the diode in such a way that very low level signals can still be rectified, with minimal error. This can be useful for high-precision signal processing. The MCP6446/7/9 op amp has high input impedance, low input bias current and rail-to-rail input/output, which makes this device suitable for precision rectifier applications.

Figure 4-8 shows a precision half-wave rectifier and its transfer characteristic. The rectifier's input impedance is determined by the input resistor R_1. To avoid the loading effect, it must be driven from a low-impedance source.

When V_{IN} is greater than zero, D_1 is OFF, D_2 is ON, and V_{OUT} is zero. When V_{IN} is less than zero, D_1 is ON, D_2 is OFF, and V_{OUT} is the V_{IN} with an amplification of $-R_2/R_1$.

The rectifier circuit shown in Figure 4-8 has the benefit that the op amp never goes in saturation, so the only thing affecting its frequency response is the amplification and the gain bandwidth product.

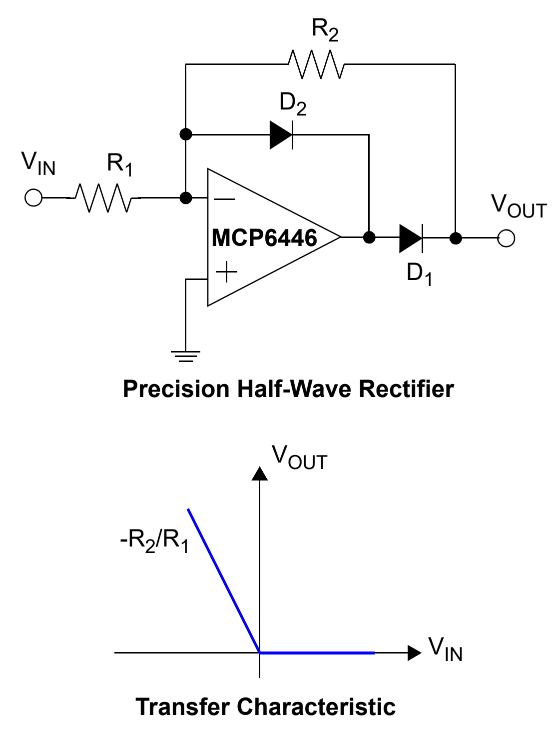
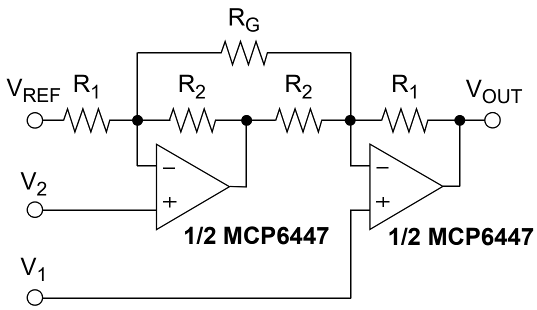


FIGURE 4-8: *Precision Half-Wave Rectifier.*

4.6.3 INSTRUMENTATION AMPLIFIER

The MCP6446/7/9 op amp is well suited for conditioning sensor signals in battery-powered applications. Figure 4-9 shows a two op amp instrumentation amplifier, using the MCP6446/7/9 device, that works well for applications requiring rejection of Common

Mode noise at higher gains. The reference voltage (V_{REF}) is supplied by a low-impedance source. In single supply applications, V_{REF} is typically $V_{DD}/2$.



$$V_{OUT} = (V_1 - V_2)\left(1 + \frac{R_1}{R_2} + \frac{2R_1}{R_G}\right) + V_{REF}$$

FIGURE 4-9: *Two Op Amp Instrumentation Amplifier.*

5.0 DESIGN AIDS

Microchip provides the basic design tools needed for the MCP6446/7/9 op amp.

5.1 SPICE Macro Model

The latest SPICE macro model for the MCP6446/7/9 op amp is available on the Microchip web site at www.microchip.com. The model was written and tested in the official OrCAD- (Cadence®) owned PSpice®. For the other simulators, translation may be required.

The model covers a wide aspect of the op amp's electrical specifications. Not only does the model cover voltage, current and resistance of the op amp, but it also covers the temperature and the noise effects on the behavior of the op amp. The model has not been verified outside of the specification range listed in the op amp data sheet. The model behaviors under these conditions cannot ensure it will match the actual op amp performance.

Moreover, the model is intended to be an initial design tool. Bench testing is a very important part of any design and cannot be replaced with simulations. Also, simulation results using this macro model need to be validated by comparing them to the data sheet specifications and characteristic curves.

5.2 FilterLab® Software

Microchip's FilterLab software is an innovative software tool that simplifies analog active filter design using op amps. Available at no cost from the Microchip web site at www.microchip.com/filterlab, the FilterLab design tool provides full schematic diagrams of the filter circuit with component values. It also outputs the filter circuit in SPICE format, which can be used with the macro model to simulate the actual filter performance.

5.3 Microchip Advanced Part Selector (MAPS)

MAPS is a software tool that helps semiconductor professionals efficiently identify the Microchip devices that fit a particular design requirement. Available at no cost from the Microchip website at www.microchip.com/ maps, the MAPS is an overall selection tool for Microchip's product portfolio that includes Analog, Memory, MCUs and DSCs. Using this tool, you can define a filter to sort features for a parametric search of devices and export side-by-side technical comparison reports. Helpful links are also provided for Data Sheets, Purchase and Sampling of Microchip parts.

5.4 Analog Demonstration and Evaluation Boards

Microchip offers a broad spectrum of Analog Demonstration and Evaluation Boards that are designed to help you achieve faster time to market. For a complete listing of these boards and their corresponding user's guides and technical information, visit the Microchip web site at www.microchip.com/analogtools.

Some boards that are especially useful are:

- MCP6XXX Amplifier Evaluation Board 1
- MCP6XXX Amplifier Evaluation Board 2
- MCP6XXX Amplifier Evaluation Board 3
- MCP6XXX Amplifier Evaluation Board 4
- Active Filter Demo Board Kit
- 5/6-Pin SOT-23 Evaluation Board, P/N VSUPEV2

5.5 Application Notes

The following Microchip Analog Design Note and Application Notes are available on the Microchip web site at www.microchip.com/appnotes, and are recommended as supplemental reference resources.

- **ADN003 –** *"Select the Right Operational Amplifier for your Filtering Circuits",* DS21821
- **AN722 –** *"Operational Amplifier Topologies and DC Specifications",* DS00722
- **AN723 –** *"Operational Amplifier AC Specifications and Applications",* DS00723
- **AN884 –** *"Driving Capacitive Loads With Op Amps",* DS00884
- **AN990 –** *"Analog Sensor Conditioning Circuits – An Overview",* DS00990
- **AN1177 –** *"Op Amp Precision Design: DC Errors",* DS01177
- **AN1228 –** *"Op Amp Precision Design: Random Noise",* DS01228
- **AN1297 –** *"Microchip's Op Amp SPICE Macro Models",* DS01297
- **AN1332:** *"Current Sensing Circuit Concepts and Fundamentals"'* DS01332

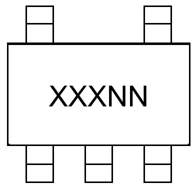
These application notes and others are listed in the design guide:

- *"Signal Chain Design Guide",* DS21825.

6.0 PACKAGING INFORMATION

6.1 Package Marking Information

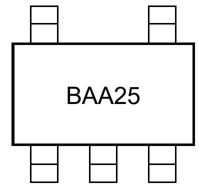
5-Lead SC-70 (**MCP6446/6R/6U**)



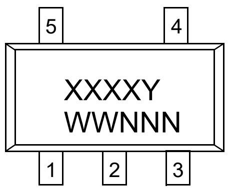
Device	Marking
MCP6446	BAANN
MCP6446U	BABNN

Note: Applies to 5-Lead SC-70.

Example:



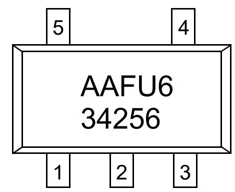
5-Lead SOT-23 (**MCP6446/6R/6U**)



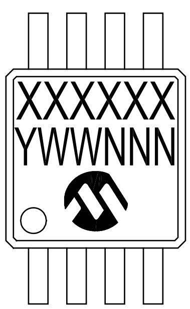
Device	Marking
MCP6446	AAFUY
MCP6446R	AAFXY
MCP6446U	AAFVY

Note: Applies to 5-Lead SOT-23.

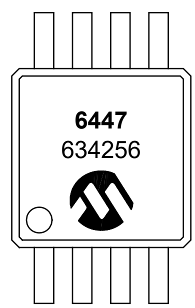
Example:



8-Lead MSOP **(MCP6447)**



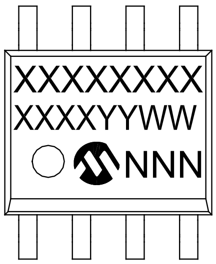
Example:



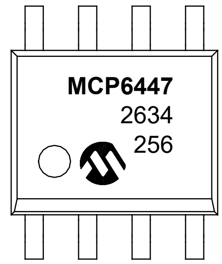
Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	e3	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

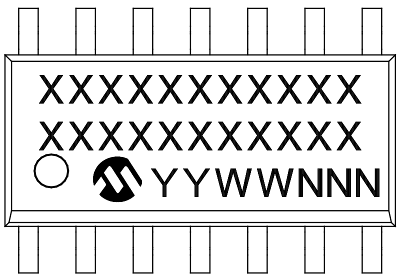
8-Lead SOIC (150 mil) **(MCP6447)**



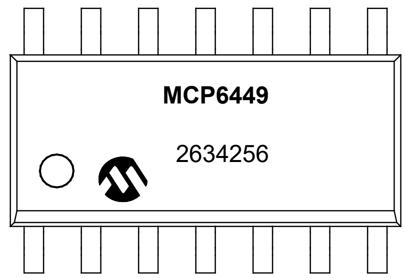
Example:



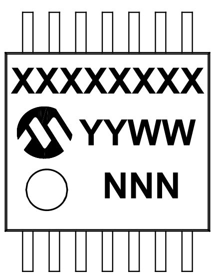
14-Lead SOIC (150 mil) (**MCP6449**)



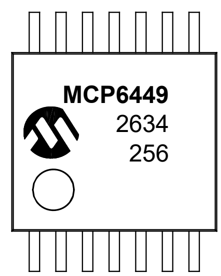
Example:



14-Lead TSSOP (**MCP6449**)



Example:



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
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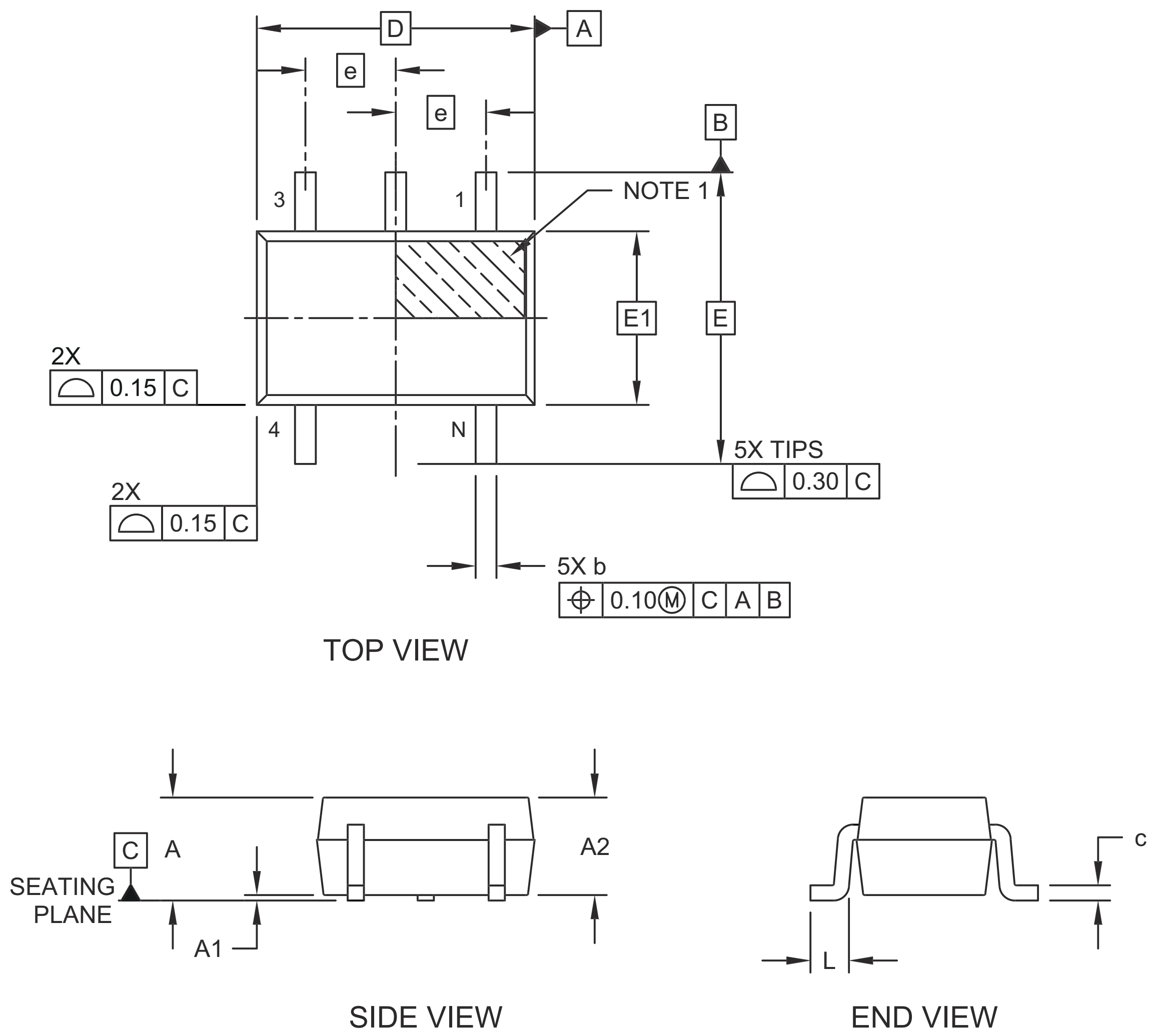
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

5-Lead Plastic Small Outline Transistor (B4X) [SC70]

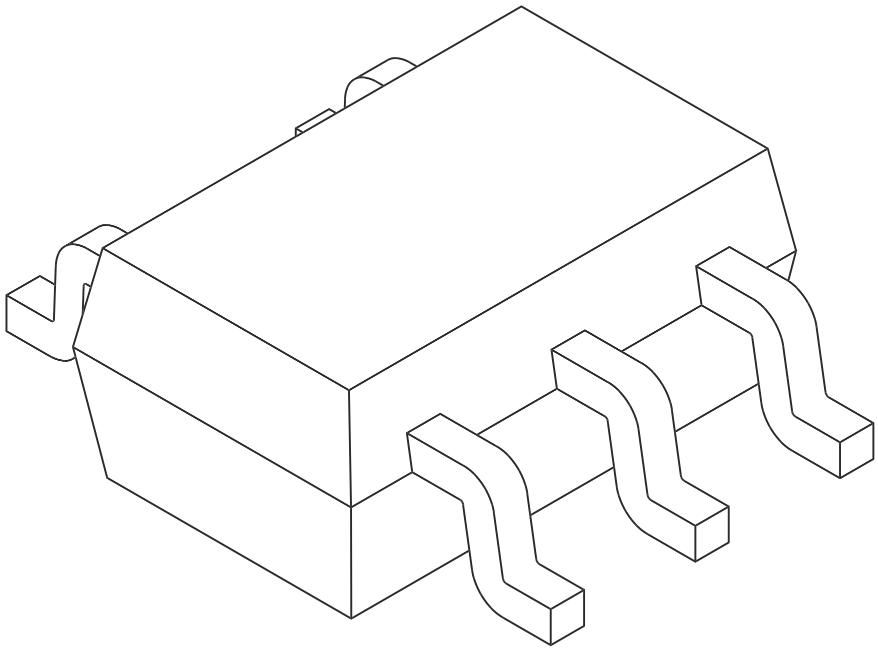
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-00061-B4X Rev F Sheet 1 of 2

5-Lead Plastic Small Outline Transistor (B4X) [SC70]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		5	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	-	1.10
Standoff	A1	0.00	-	0.10
Molded Package Thickness	A2	0.80	-	1.00
Overall Length	D		2.00 BSC	
Overall Width	E		2.10 BSC	
Molded Package Width	E1		1.25 BSC	
Terminal Width	b	0.15	-	0.40
Terminal Length	L	0.10	0.20	0.46
Lead Thickness	c	0.08	-	0.26

Notes:

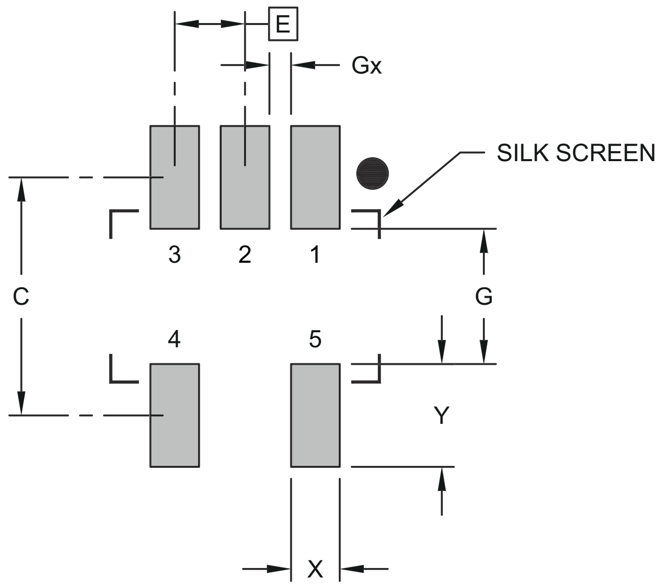
1. The Pin 1 visual index feature may vary, but it must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. The theoretically exact value is shown without tolerances.
   REF: Reference Dimension, usually without tolerance, is for information purposes only.

Microchip Technology Drawing C04-00061-B4X Rev F Sheet 2 of 2

5-Lead Plastic Small Outline Transistor (B4X) [SC70]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	C		2.20	
Contact Pad Width	X			0.45
Contact Pad Length	Y			0.95
Distance Between Pads	G	1.25		
Distance Between Pads	Gx	0.20		

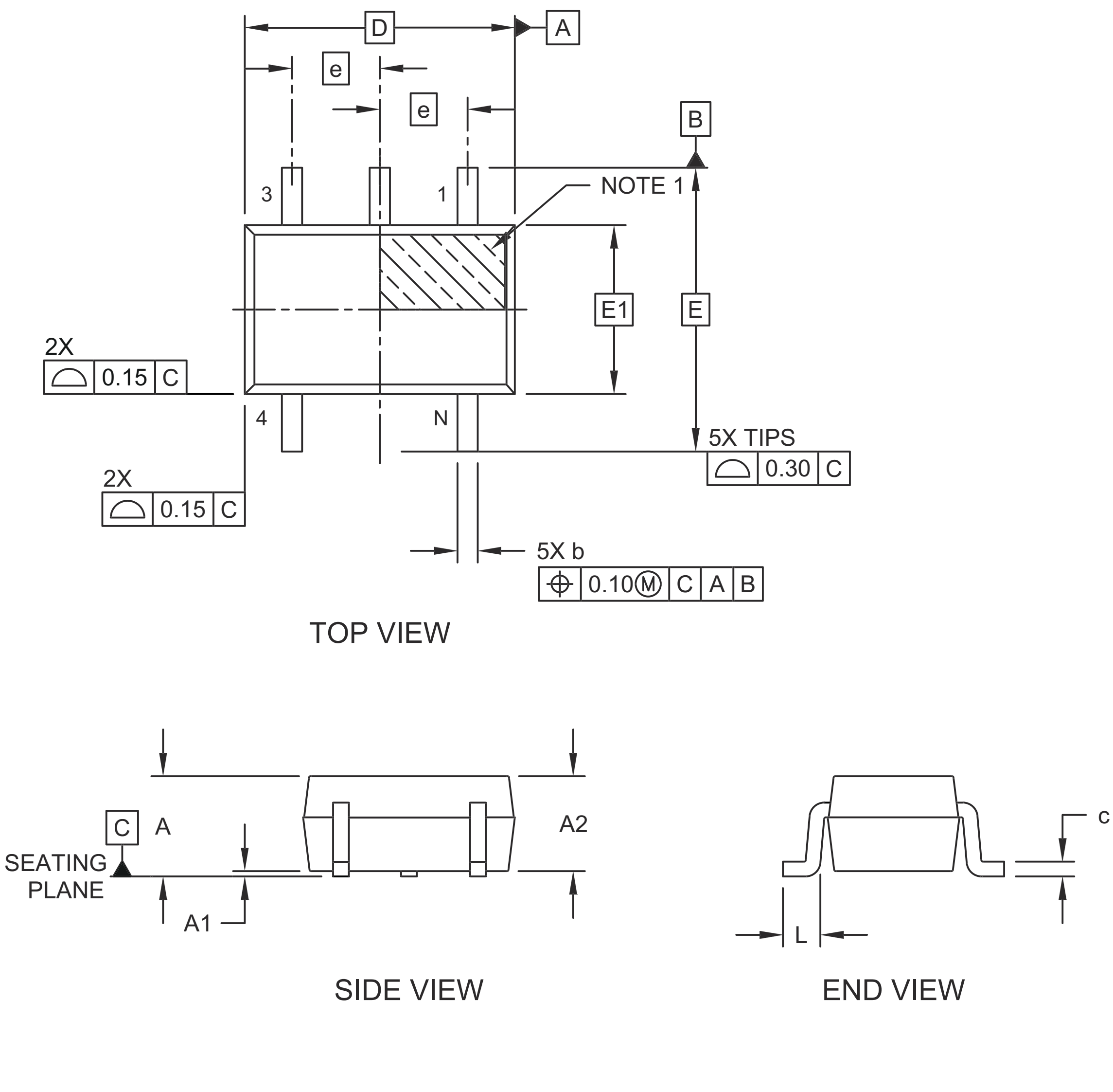
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. The theoretically exact value is shown without tolerances.

Microchip Technology Drawing No. C04-02061-B4X Rev F

5-Lead Plastic Small Outline Transistor (B4X) [SC70]

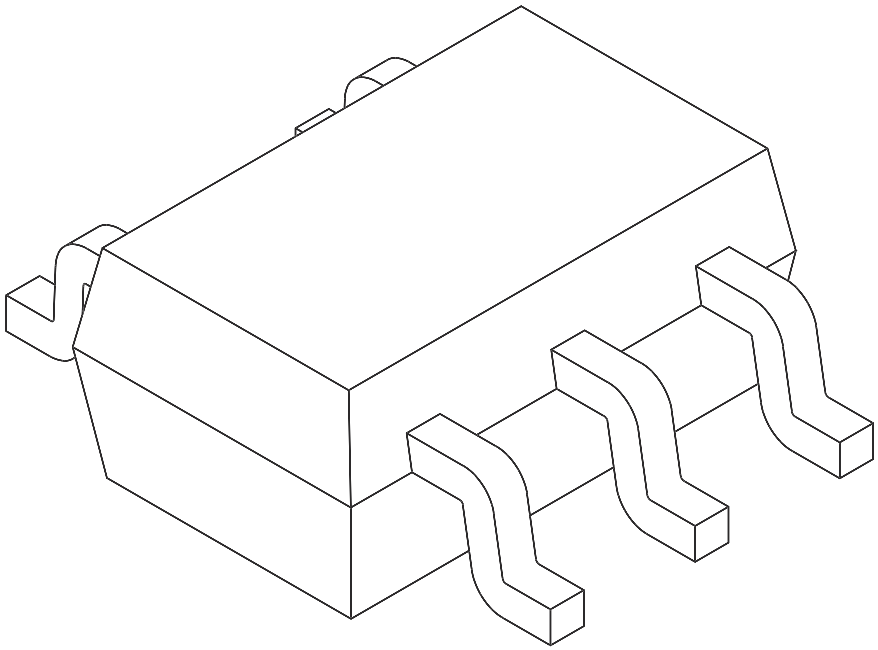
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-00061-B4X Rev F Sheet 1 of 2

5-Lead Plastic Small Outline Transistor (B4X) [SC70]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		5	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	-	1.10
Standoff	A1	0.00	-	0.10
Molded Package Thickness	A2	0.80	-	1.00
Overall Length	D		2.00 BSC	
Overall Width	E		2.10 BSC	
Molded Package Width	E1		1.25 BSC	
Terminal Width	b	0.15	-	0.40
Terminal Length	L	0.10	0.20	0.46
Lead Thickness	c	0.08	-	0.26

Notes:

1. The Pin 1 visual index feature may vary, but it must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M

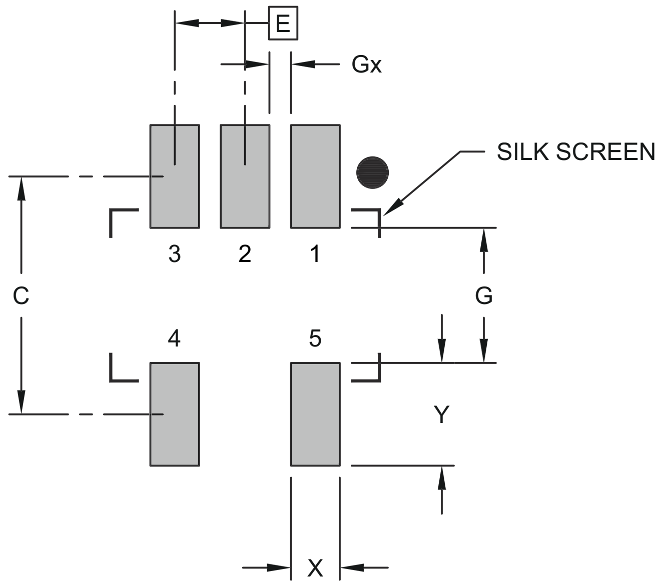
BSC: Basic Dimension. The theoretically exact value is shown without tolerances.

REF: Reference Dimension, usually without tolerance, is for information purposes only.

Microchip Technology Drawing C04-00061-B4X Rev F Sheet 2 of 2

5-Lead Plastic Small Outline Transistor (B4X) [SC70]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		2.20	
Contact Pad Width	X			0.45
Contact Pad Length	Y			0.95
Distance Between Pads	G	1.25		
Distance Between Pads	Gx	0.20		

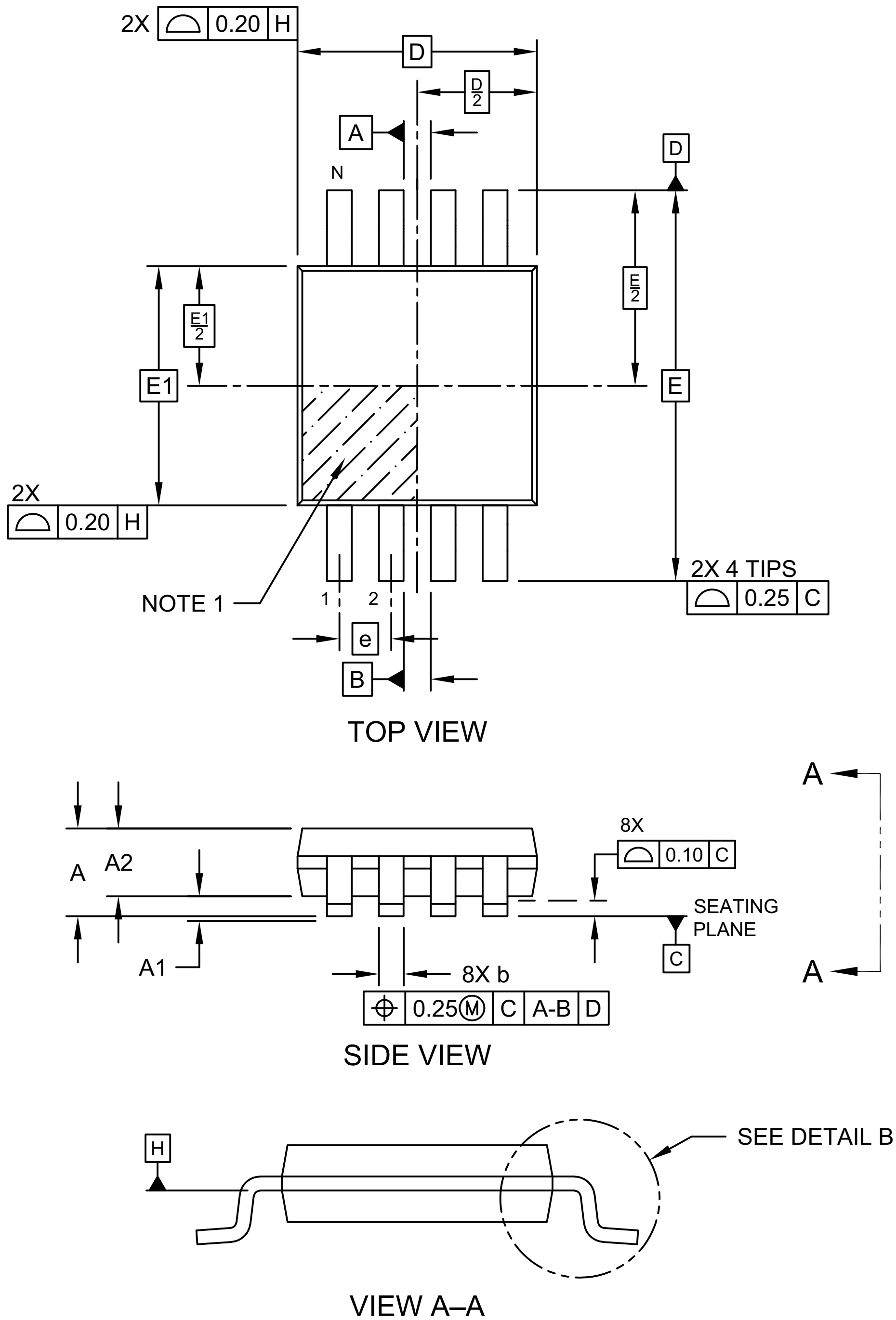
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. The theoretically exact value is shown without tolerances.

Microchip Technology Drawing No. C04-02061-B4X Rev F

8-Lead Plastic Micro Small Outline Package (A3X) - 3x3 mm Body [MSOP]

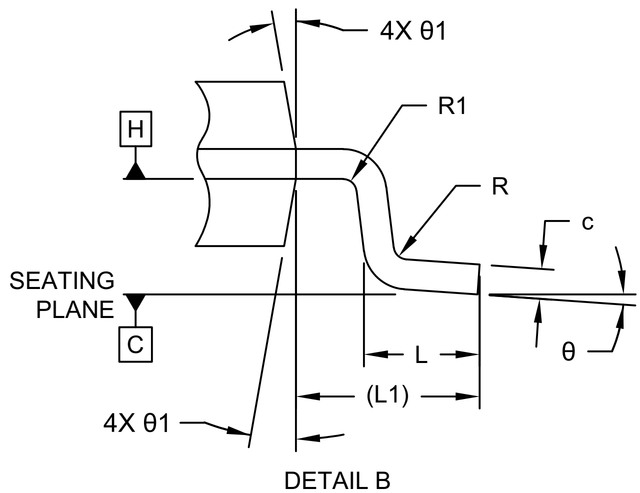
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

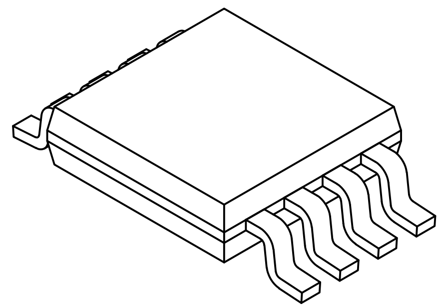


Microchip Technology Drawing C04-111-A3X Rev F Sheet 1 of 2

8-Lead Plastic Micro Small Outline Package (A3X) - 3x3 mm Body [MSOP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N	8		
Pitch	e	0.65 BSC		
Overall Height	A	–	–	1.10
Standoff	A1	0.00	–	0.15
Molded Package Thickness	A2	0.75	0.85	0.95
Overall Length	D	3.00 BSC		
Overall Width	E	4.90 BSC		
Molded Package Width	E1	3.00 BSC		
Terminal Width	b	0.22	–	0.40
Terminal Thickness	c	0.08	–	0.23
Terminal Length	L	0.40	0.60	0.80
Footprint	L1	0.95 REF		
Lead Bend Radius	R	0.07	–	–
Lead Bend Radius	R1	0.07	–	–
Foot Angle	θ	0°	–	8°
Mold Draft Angle	θ1	5°	–	15°

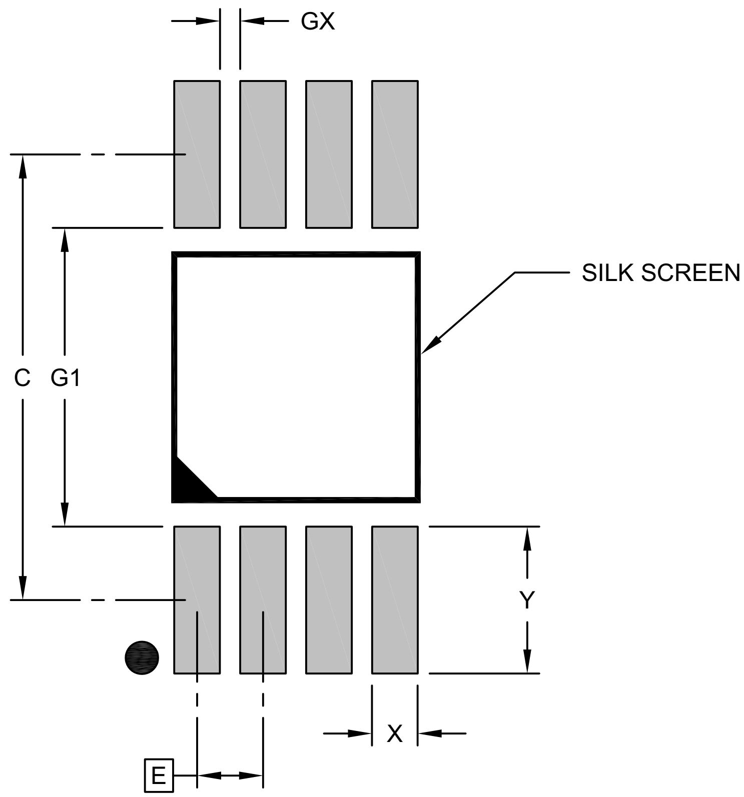
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111-A3X Rev F Sheet 2 of 2

8-Lead Plastic Micro Small Outline Package (A3X) - 3x3 mm Body [MSOP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		4.40	
Contact Pad Width (X8)	X			0.45
Contact Pad Length (X8)	Y			1.45
Contact Pad to Contact Pad (X4)	G1	2.95		
Contact Pad to Contact Pad (X6)	GX	0.20		

Notes:

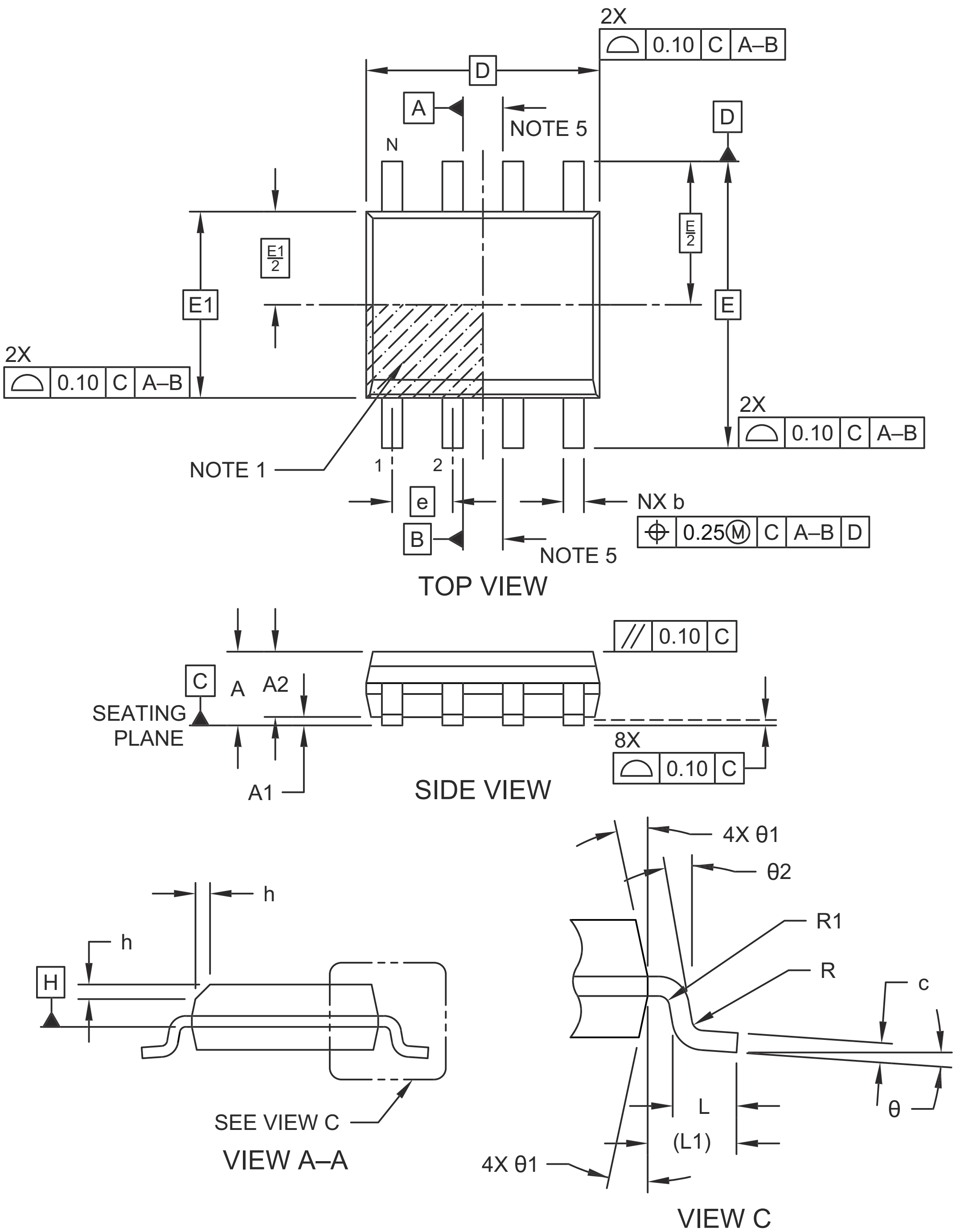
1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2111-A3X Rev F

8-Lead Plastic Small Outline (C2X) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

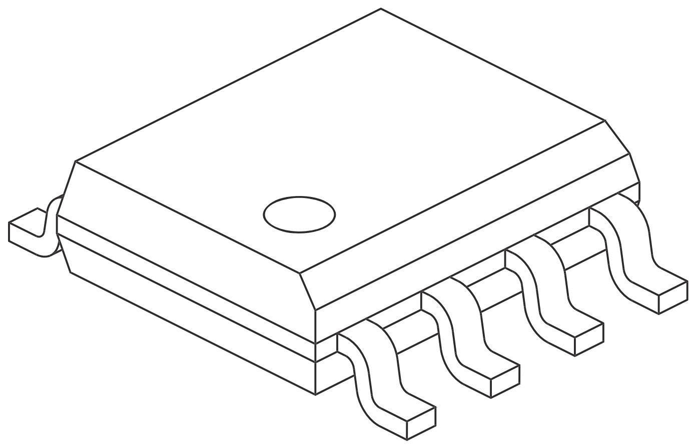
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-00057-C2X Rev L Sheet 1 of 2

8-Lead Plastic Small Outline (C2X) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	1.27 BSC		
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	-
Standoff §	A1	0.10	–	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	4.90 BSC		
Chamfer (Optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1	1.04 REF		
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Lead Bend Radius	R	0.07	–	–
Lead Bend Radius	R1	0.07	–	–
Foot Angle	θ	0°	–	8°
Mold Draft Angle	θ1	5°	–	15°
Lead Angle	θ2	0°	–	–

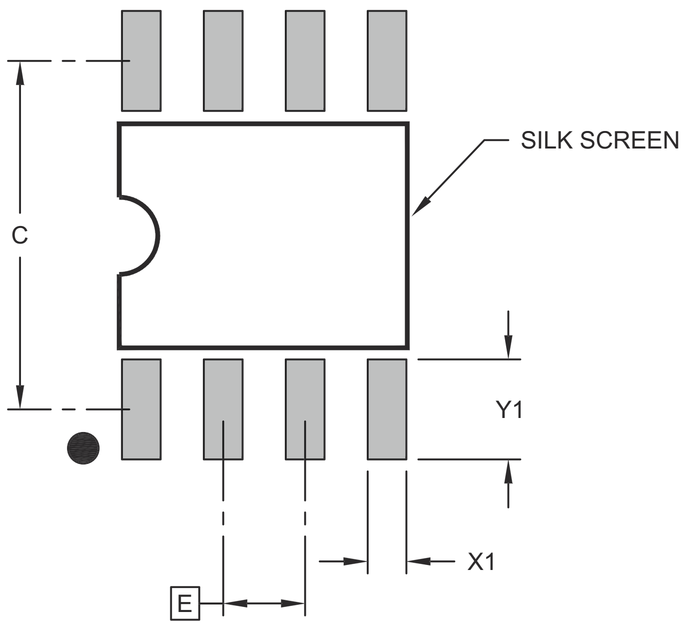
Notes:

1. The Pin 1 visual index feature may vary, but it must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-00057-C2X Rev L Sheet 2 of 2

8-Lead Plastic Small Outline (C2X) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

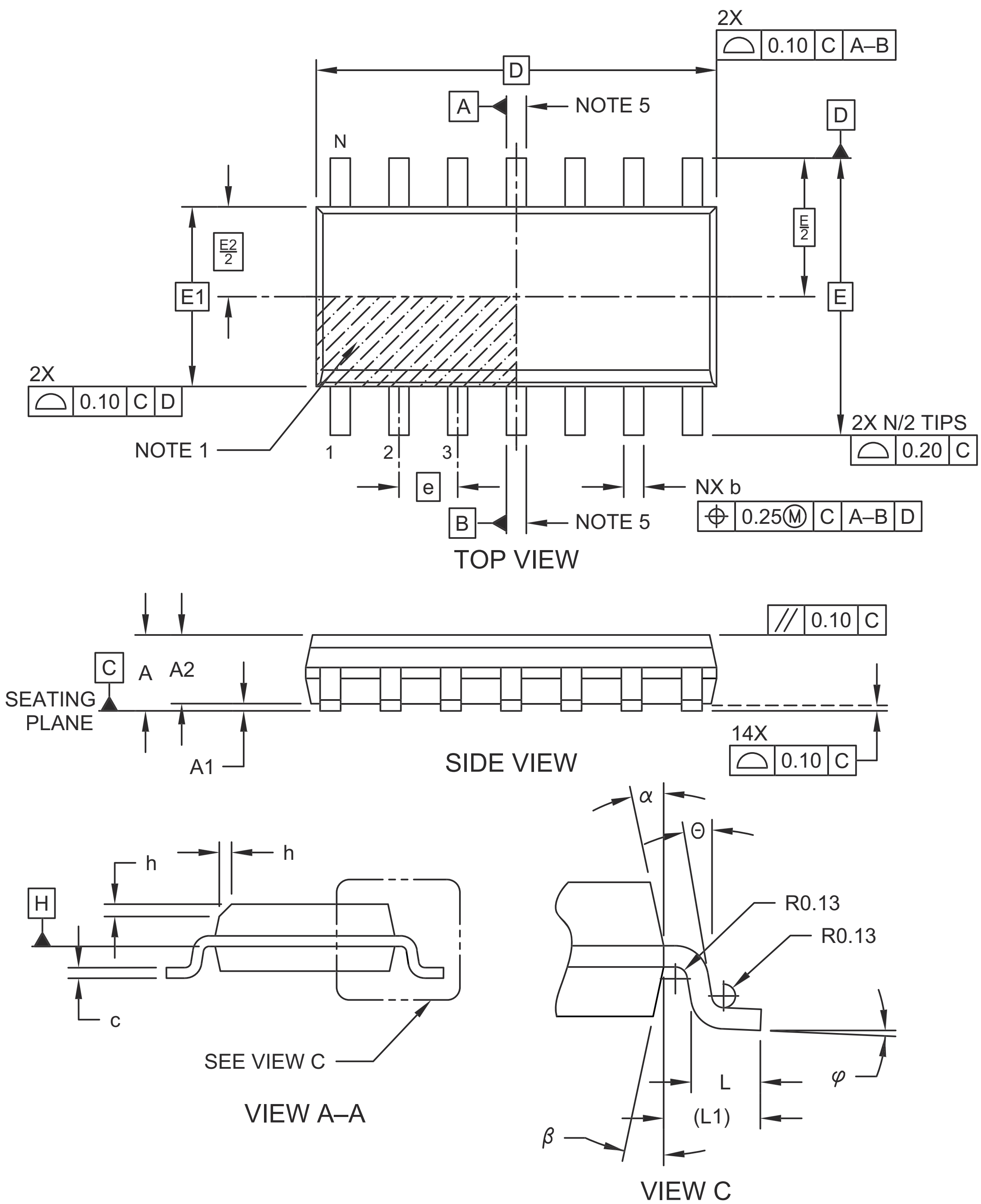
1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-02057-C2X Rev L

14-Lead Plastic Small Outline (D3X) - Narrow, 3.90 mm Body [SOIC]

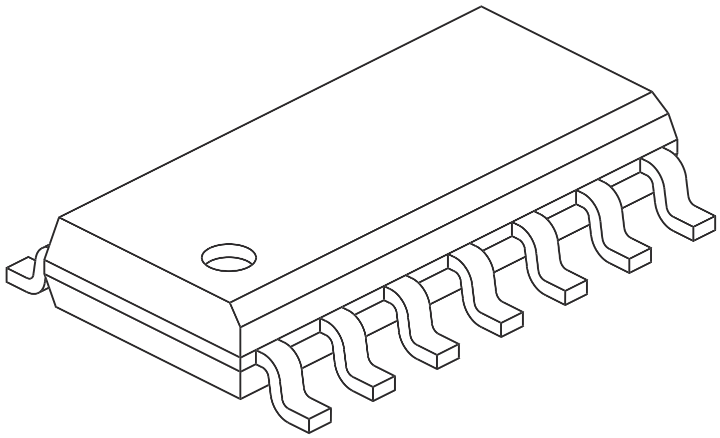
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-00065 (D3X) Rev F Sheet 1 of 2

14-Lead Plastic Small Outline (D3X) - Narrow, 3.90 mm Body [SOIC]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Number of Pins	N	14		
Pitch	e	1.27 BSC		
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	8.65 BSC		
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1	1.04 REF		
Lead Angle	Θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.10	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

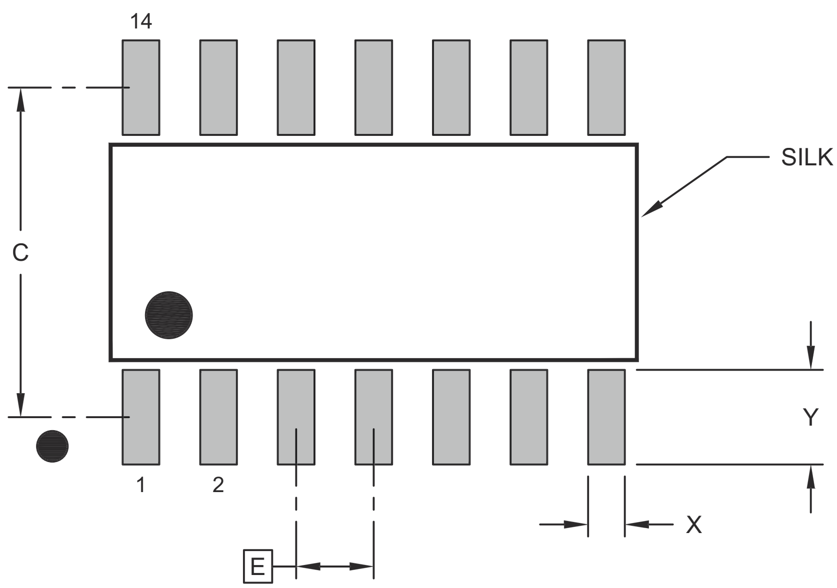
Notes:

1. The Pin 1 visual index feature may vary, but it must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold Flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead Flash or protrusions, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. The theoretically exact value is shown without tolerances.
   REF: Reference Dimension, usually without tolerance, is for information purposes only.
5. Datums A and B to be determined at Datum H.

Microchip Technology Drawing No. C04-00065 (D3X) Rev F Sheet 2 of 2

14-Lead Plastic Small Outline (D3X) - Narrow, 3.90 mm Body [SOIC]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X14)	X			0.60
Contact Pad Length (X14)	Y			1.55

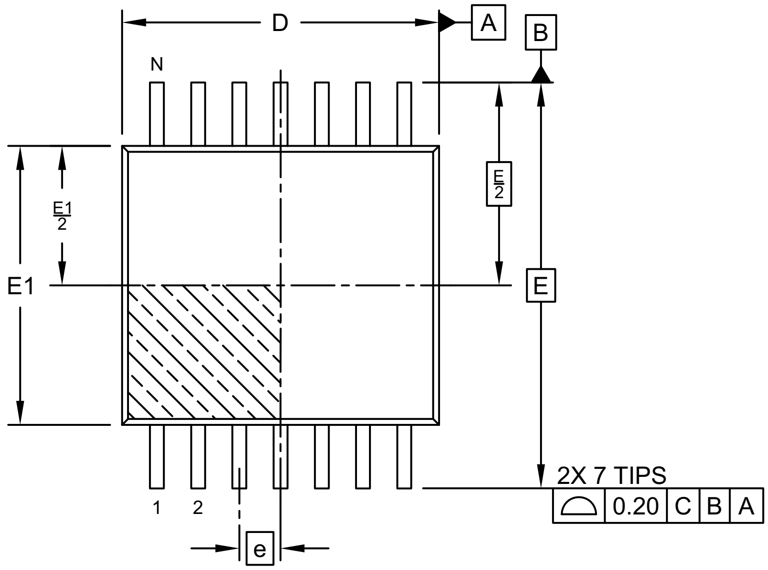
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. The theoretically exact value is shown without tolerances.

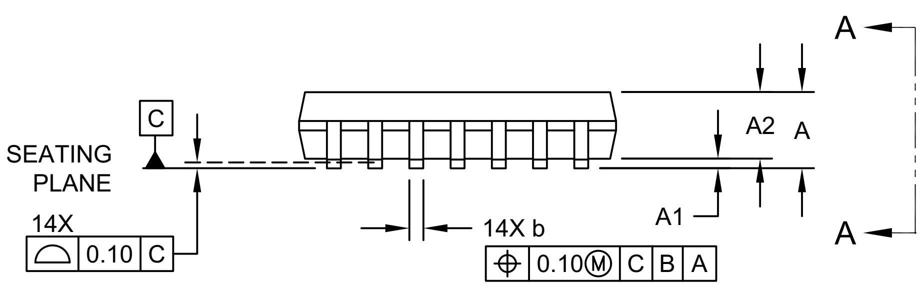
Microchip Technology Drawing No. C04-02065 (D3X) Rev F

14-Lead Plastic Thin Shrink Small Outline Package [D4X] - 4.4 mm Body [TSSOP]

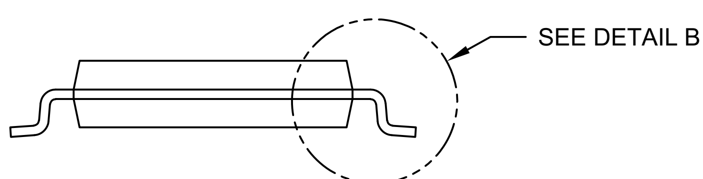
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

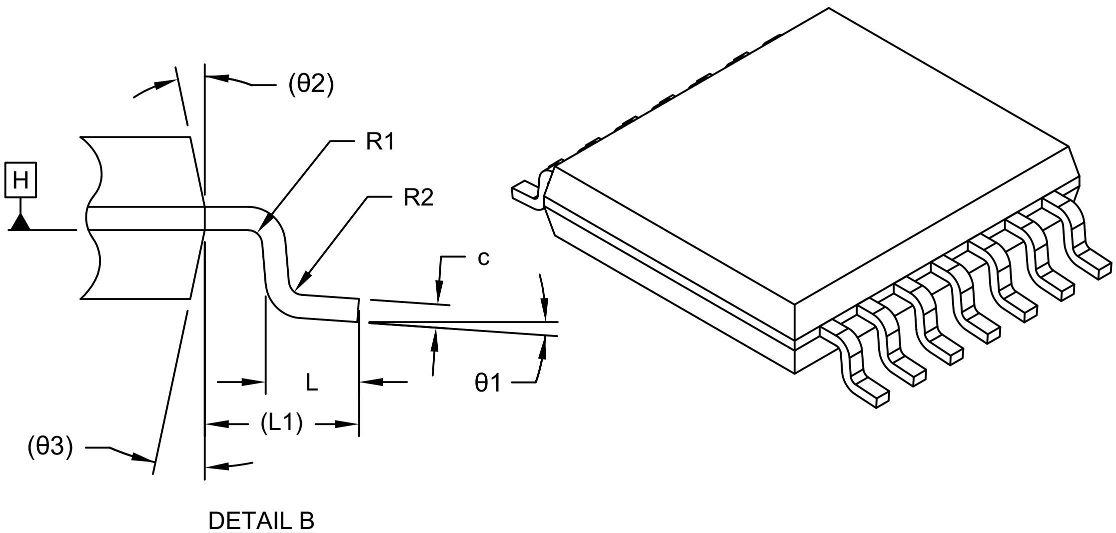


VIEW A–A

Microchip Technology Drawing C04-087-D4X Rev F Sheet 1 of 2

14-Lead Plastic Thin Shrink Small Outline Package [D4X] - 4.4 mm Body [TSSOP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Number of Terminals	N		14	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	1.20
Standoff	A1	0.05	–	0.15
Molded Package Thickness	A2	0.80	1.00	1.05
Overall Length	D	4.90	5.00	5.10
Overall Width	E		6.40 BSC	
Molded Package Width	E1	4.30	4.40	4.50
Terminal Width	b	0.19	–	0.30
Terminal Thickness	c	0.09	–	0.20
Terminal Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Lead Bend Radius	R1	0.09	–	–
Lead Bend Radius	R2	0.09	–	–
Foot Angle	θ1	0°	–	8°
Mold Draft Angle	θ2	–	12° REF	–
Mold Draft Angle	θ3	–	12° REF	–

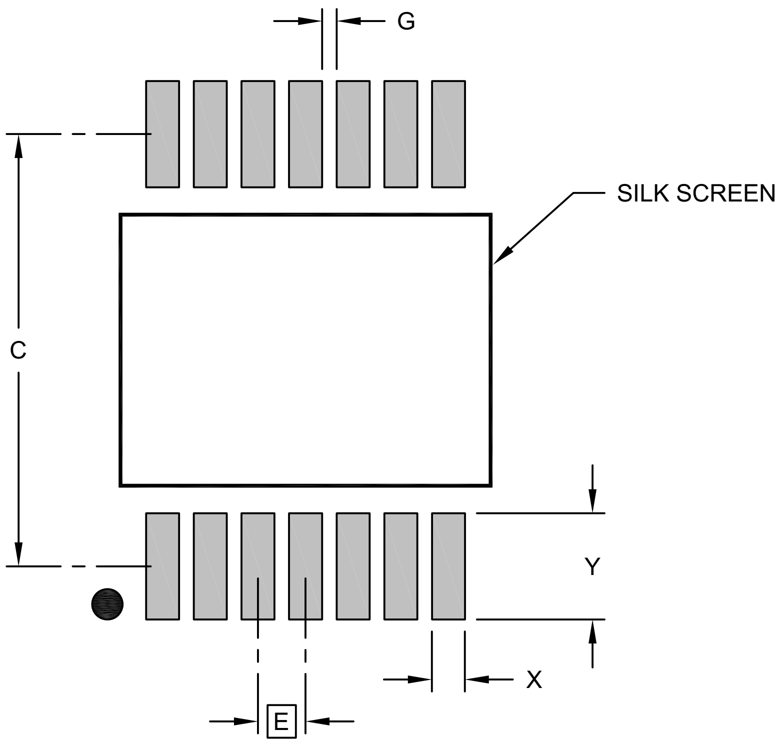
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-087-D4X Rev F Sheet 2 of 2

14-Lead Plastic Thin Shrink Small Outline Package [D4X] – 4.4 mm Body [TSSOP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	C		5.90	
Contact Pad Width (X14)	X			0.45
Contact Pad Length (X14)	Y			1.45
Contact Pad to Contact Pad (X12)	G	0.20		

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2087-D4X Rev F

APPENDIX A: REVISION HISTORY

Revision A (August 2026)

- Original release of this document.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X(1)	-X	/XX	XXX(2)
Device	Tape and Reel Option	Temperature Range	Package	CLASS

Device:	MCP6446T	Single Op Amp (Tape and Reel)
	MCP6446RT	Single Op Amp (Tape and Reel)
	MCP6446UT	Single Op Amp (Tape and Reel)
	MCP6447T	Dual Op Amp (Tape and Reel)
	MCP6449T	Quad Op Amp (Tape and Reel)
Temperature Range:	E =	-40°C to +125°C
Package:	LT =	Plastic Package (SC-70), 5-lead
	OT =	Plastic Small Outline transistor (SOT-23), 5-lead
	SN =	Plastic Small Outline, (3.90 mm), 8-lead
	MS =	Plastic MSOP, 8-lead
	ST =	Plastic Thin Shrink Small Outline (4.4 mm),
	SL =	Plastic Small Outline, (3.90 mm), 14-lead
Class:	(Blank) =	Non-Automotive

Note 1: The Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

2: Automotive parts are AEC-Q100 qualified. Grade 1.

Examples:

a) MCP6446T-E/LT: Tape and Reel, Extended temperature, 5LD SC-70 package

b) MCP6446T-E/OT: Tape and Reel, Extended temperature, 5LD SOT-23 package

c) MCP6446RT-E/OT: Tape and Reel, Extended temperature, 5LD SOT-23 package

d) MCP6446UT-E/LT: Tape and Reel, Extended temperature, 5LD SC-70 package

e) MCP6446UT-E/OT: Tape and Reel, Extended temperature, 5LD SOT-23 package

a) MCP6447-E/SN: Extended temperature, 8LD SOIC package

b) MCP6447-E/MS: Extended temperature, 8LD MSOP package

c) MCP6447T-E/SN: Tape and Reel, Extended temperature, 8LD SOIC package

d) MCP6447T-E/MS: Tape and Reel, Extended temperature, 8LD MSOP package

a) MCP6449-E/ST: Extended temperature, 14LD TSSOP package

b) MCP6449-E/SL: Extended temperature, 14LD SOIC package

c) MCP6449T-E/SL: Tape and Reel, Extended temperature, 14LD SOIC package

d) MCP6449T-E/ST: Tape and Reel, Extended temperature, 14LD TSSOP package

PRODUCT IDENTIFICATION SYSTEM (AUTOMOTIVE)

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office
.\

PART NO.	X[1]	-X	/XX	XXX[2]
Device	Tape and Reel Option	Temperature Range	Package	CLASS

Device:
- MCP6446T Single Op Amp (Tape and Reel)
- MCP6446RT Single Op Amp (Tape and Reel)
- MCP6446UT Single Op Amp (Tape and Reel)
- MCP6447T Dual Op Amp (Tape and Reel)
- MCP6449T Quad Op Amp (Tape and Reel)

Temperature Range: E = -40°C to +125°C

Package:
- LT = Plastic Package (SC-70), 5-lead
- OT = Plastic Small Outline transistor (SOT-23), 5-lead
- SN = Plastic Small Outline, (3.90 mm), 8-lead
- MS = Plastic MSOP, 8-lead
- ST = Plastic Thin Shrink Small Outline (4.4 mm),
- SL = Plastic Small Outline, (3.90 mm), 14-lead

Class:
- (Blank) = Non-Automotive
- VAO = Automotive

Note 1: The Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

2: Automotive parts are AEC-Q100 qualified. Grade 1.

Examples:

a) MCP6446T-E/LTVAO: Tape and Reel, Automotive, Extended temperature, 5LD SC-70 package

b) MCP6446T-E/OTVAO: Tape and Reel, Automotive, Extended temperature, 5LD SOT-23 package

c) MCP6446RT-E/OTVAO: Tape and Reel, Automotive, Extended temperature, 5LD SOT-23 package

d) MCP6446UT-E/LTVAO: Tape and Reel, Automotive, Extended temperature, 5LD SC-70 package

e) MCP6446UT-E/OTVAO: Tape and Reel, Automotive, Extended temperature, 5LD SOT-23 package

a) MCP6447T-E/SNVAO: Tape and Reel, Extended temperature, Automotive, 8LD SOIC package

b) MCP6447T-E/MSVAO: Tape and Reel, Extended temperature, Automotive, 8LD MSOP package

a) MCP6449T-E/STVAO: Tape and Reel, Extended temperature, Automotive, 14LD TSSOP package

b) MCP6449T-E/SLVAO: Tape and Reel, Extended temperature, Automotive, 14LD SOIC package

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