

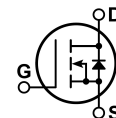
N-Channel FREDFET

Power MOS 8™ is a high speed, high voltage N-channel switch-mode power MOSFET. This 'FREDFET' version has a drain-source (body) diode that has been optimized for high reliability in ZVS phase shifted bridge and other circuits through reduced t_{rr} , soft recovery, and high recovery dv/dt capability. Low gate charge, high gain, and a greatly reduced ratio of C_{rss}/C_{iss} result in excellent noise immunity and low switching loss. The intrinsic gate resistance and capacitance of the poly-silicon gate structure help control di/dt during switching, resulting in low EMI and reliable paralleling, even when switching at very high frequency.



ISOTOP*
APT53F80J

Single die FREDFET



FEATURES

- Fast switching with low EMI
- Low t_{rr} for high reliability
- Ultra low C_{rss} for improved noise immunity
- Low gate charge
- Avalanche energy rated
- RoHS compliant 

TYPICAL APPLICATIONS

- ZVS phase shifted and other full bridge
- Half bridge
- PFC and other boost converter
- Buck converter
- Single and two switch forward
- Flyback

Absolute Maximum Ratings

Symbol	Parameter	Ratings	Unit
I_D	Continuous Drain Current @ $T_C = 25^\circ\text{C}$	57	A
	Continuous Drain Current @ $T_C = 100^\circ\text{C}$	36	
I_{DM}	Pulsed Drain Current ^①	325	
V_{GS}	Gate-Source Voltage	± 30	V
E_{AS}	Single Pulse Avalanche Energy ^②	3725	mJ
I_{AR}	Avalanche Current, Repetitive or Non-Repetitive	43	A

Thermal and Mechanical Characteristics

Symbol	Characteristic	Min	Typ	Max	Unit
P_D	Total Power Dissipation @ $T_C = 25^\circ\text{C}$			960	W
$R_{\theta JC}$	Junction to Case Thermal Resistance			0.13	$^\circ\text{C/W}$
$R_{\theta CS}$	Case to Sink Thermal Resistance, Flat, Greased Surface		0.15		
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55		150	$^\circ\text{C}$
$V_{Isolation}$	RMS Voltage (50-60Hz Sinusoidal Waveform from Terminals to Mounting Base for 1 Min.)	2500			V
W_T	Package Weight		1.03		oz
			29.2		g
Torque	Terminals and Mounting Screws.			10	in·lbf
				1.1	N·m

Static Characteristics
T_J = 25°C unless otherwise specified
APT53F80J

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{BR(DSS)}$	Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	800			V
$\Delta V_{BR(DSS)}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	Reference to 25°C, $I_D = 250\mu A$		0.87		V/°C
$R_{DS(on)}$	Drain-Source On Resistance ^③	$V_{GS} = 10V, I_D = 43A$		0.07	0.11	Ω
$V_{GS(th)}$	Gate-Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 5mA$	2.5	4	5	V
$\Delta V_{GS(th)}/\Delta T_J$	Threshold Voltage Temperature Coefficient			-10		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 800V$ $V_{GS} = 0V$			250	μA
		$T_J = 25^\circ C$ $T_J = 125^\circ C$			1000	
I_{GSS}	Gate-Source Leakage Current	$V_{GS} = \pm 30V$			±100	nA

Dynamic Characteristics
T_J = 25°C unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
g_{fs}	Forward Transconductance	$V_{DS} = 50V, I_D = 43A$		80		S
C_{iss}	Input Capacitance	$V_{GS} = 0V, V_{DS} = 25V$ $f = 1MHz$		17550		pF
C_{rss}	Reverse Transfer Capacitance			300		
C_{oss}	Output Capacitance			1745		
$C_{o(cr)}^{④}$	Effective Output Capacitance, Charge Related	$V_{GS} = 0V, V_{DS} = 0V \text{ to } 533V$		825		
$C_{o(er)}^{⑤}$	Effective Output Capacitance, Energy Related			410		
Q_g	Total Gate Charge	$V_{GS} = 0 \text{ to } 10V, I_D = 43A,$ $V_{DS} = 400V$		570		nC
Q_{gs}	Gate-Source Charge			95		
Q_{gd}	Gate-Drain Charge			290		
$t_{d(on)}$	Turn-On Delay Time	Resistive Switching $V_{DD} = 533V, I_D = 43A$ $R_G = 2.2\Omega^{⑥}, V_{GG} = 15V$		100		ns
t_r	Current Rise Time			145		
$t_{d(off)}$	Turn-Off Delay Time			435		
t_f	Current Fall Time			125		

Source-Drain Diode Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_S	Continuous Source Current (Body Diode)	MOSFET symbol showing the integral reverse p-n junction diode (body diode)			57	A
I_{SM}	Pulsed Source Current (Body Diode) ^①				325	
V_{SD}	Diode Forward Voltage	$I_{SD} = 43A, T_J = 25^\circ C, V_{GS} = 0V$			1.2	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 43A^{③}$ $di_{SD}/dt = 100A/\mu s$ $V_{DD} = 100V$	$T_J = 25^\circ C$	405	470	ns
			$T_J = 125^\circ C$	800	960	
Q_{rr}	Reverse Recovery Charge		$T_J = 25^\circ C$	2.95		μC
			$T_J = 125^\circ C$	8.86		
I_{rrm}	Reverse Recovery Current		$T_J = 25^\circ C$	14		A
			$T_J = 125^\circ C$	21		
dv/dt	Peak Recovery dv/dt	$I_{SD} \leq 43A, di/dt \leq 1000A/\mu s, V_{DD} = 400V,$ $T_J = 125^\circ C$			20	V/ns

① Repetitive Rating: Pulse width and case temperature limited by maximum junction temperature.

② Starting at $T_J = 25^\circ C, L = 4.03mH, R_G = 25\Omega, I_{AS} = 43A$.

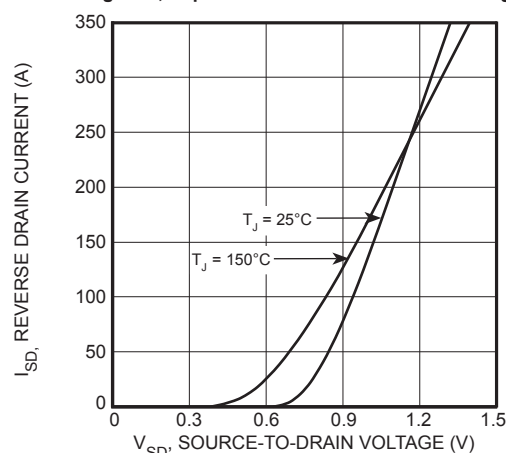
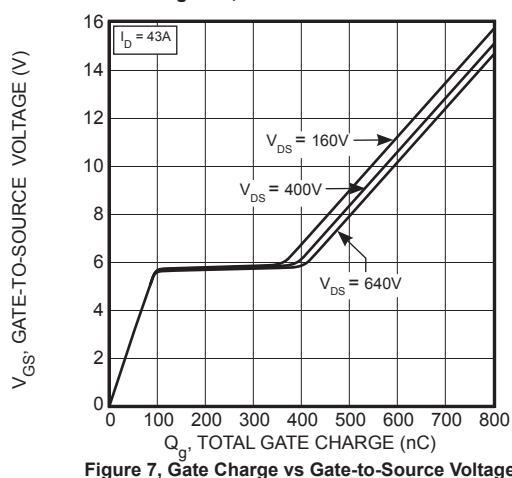
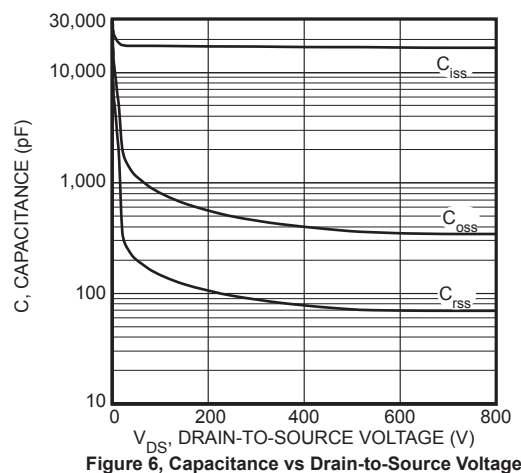
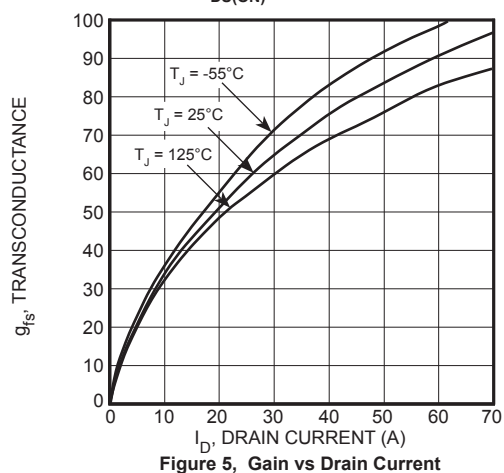
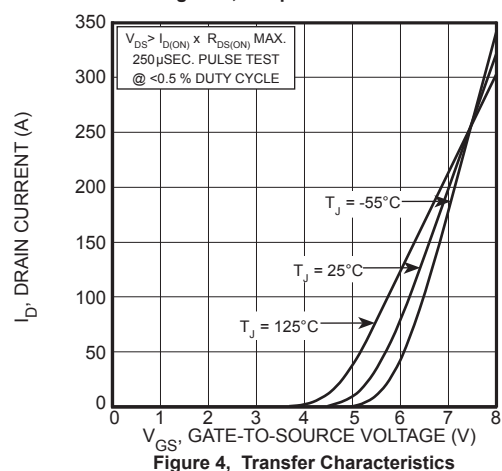
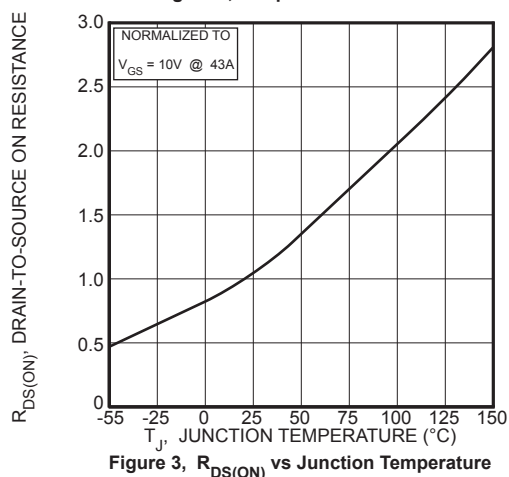
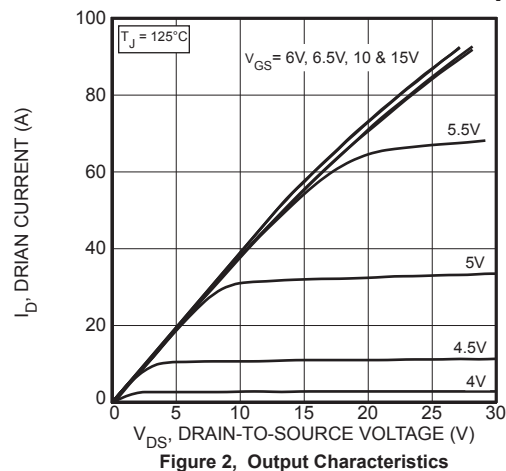
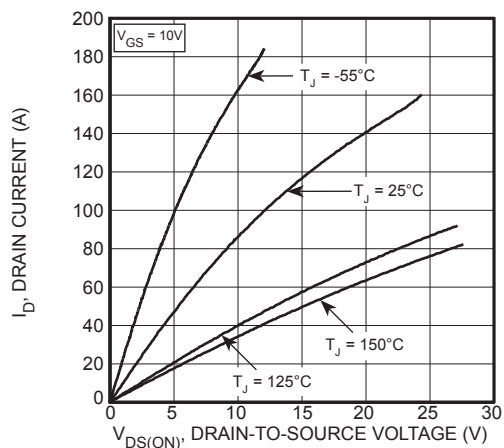
③ Pulse test: Pulse Width < 380μs, duty cycle < 2%.

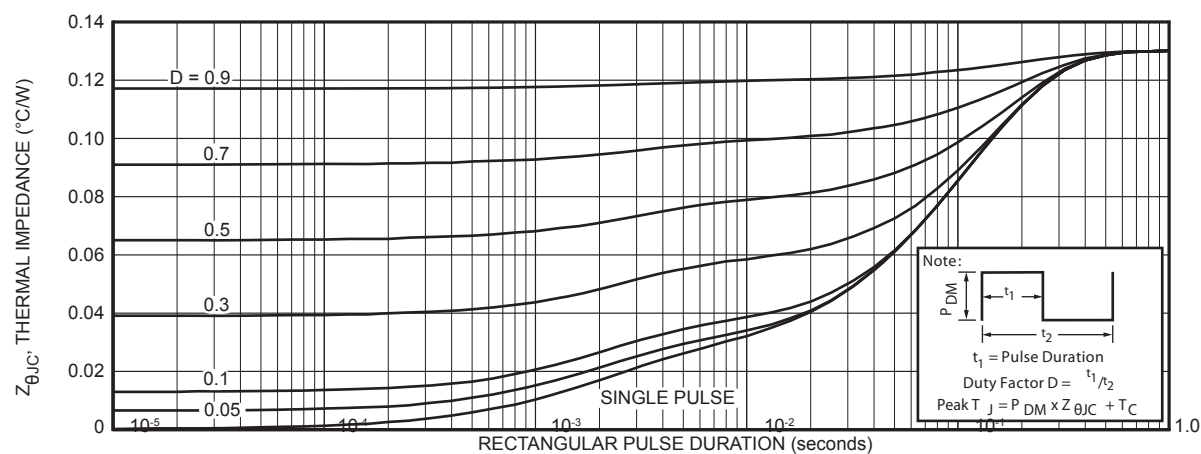
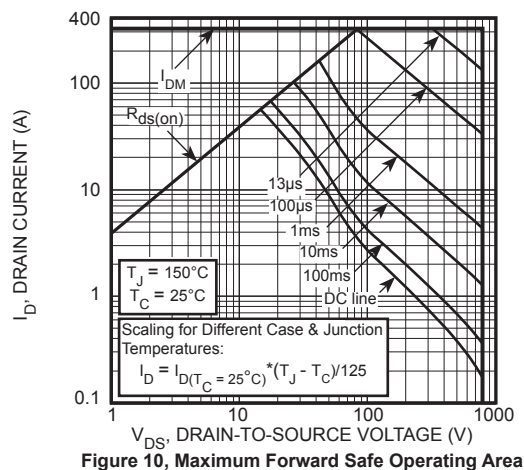
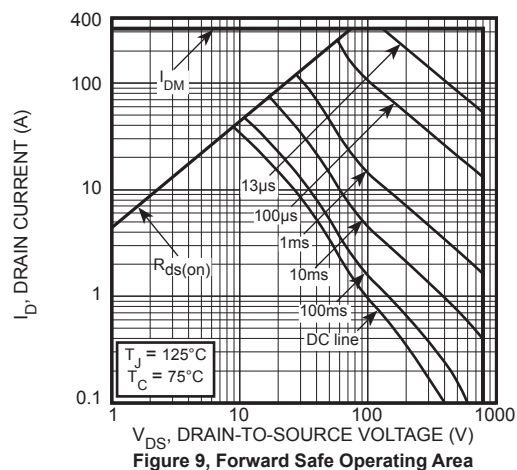
④ $C_{o(cr)}$ is defined as a fixed capacitance with the same stored charge as C_{OSS} with $V_{DS} = 67\%$ of $V_{(BR)DSS}$.

⑤ $C_{o(er)}$ is defined as a fixed capacitance with the same stored energy as C_{OSS} with $V_{DS} = 67\%$ of $V_{(BR)DSS}$. To calculate $C_{o(er)}$ for any value of V_{DS} less than $V_{(BR)DSS}$, use this equation: $C_{o(er)} = 5.57E-8/V_{DS}^2 + 7.15E-8/V_{DS} + 2.75E-10$.

⑥ R_G is external gate resistance, not including internal gate resistance or gate driver impedance. (MIC4452)

Microsemi reserves the right to change, without notice, the specifications and information contained herein.





SOT-227 (ISOTOP®) Package Outline

