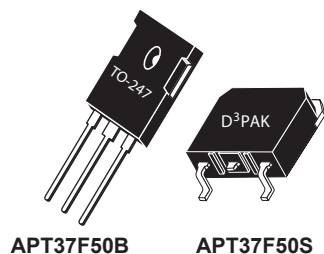
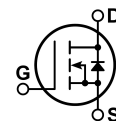


N-Channel FREDFET

Power MOS 8™ is a high speed, high voltage N-channel switch-mode power MOSFET. This 'FREDFET' version has a drain-source (body) diode that has been optimized for high reliability in ZVS phase shifted bridge and other circuits through reduced t_{rr} , soft recovery, and high recovery dv/dt capability. Low gate charge, high gain, and a greatly reduced ratio of C_{rss}/C_{iss} result in excellent noise immunity and low switching loss. The intrinsic gate resistance and capacitance of the poly-silicon gate structure help control di/dt during switching, resulting in low EMI and reliable paralleling, even when switching at very high frequency.



Single die FREDFET



FEATURES

- Fast switching with low EMI
- Low t_{rr} for high reliability
- Ultra low C_{rss} for improved noise immunity
- Low gate charge
- Avalanche energy rated
- RoHS compliant 

TYPICAL APPLICATIONS

- ZVS phase shifted and other full bridge
- Half bridge
- PFC and other boost converter
- Buck converter
- Single and two switch forward
- Flyback

Absolute Maximum Ratings

Symbol	Parameter	Ratings	Unit
I_D	Continuous Drain Current @ $T_C = 25^\circ\text{C}$	37	A
	Continuous Drain Current @ $T_C = 100^\circ\text{C}$	24	
I_{DM}	Pulsed Drain Current ^①	115	
V_{GS}	Gate-Source Voltage	±30	V
E_{AS}	Single Pulse Avalanche Energy ^②	780	mJ
I_{AR}	Avalanche Current, Repetitive or Non-Repetitive	18	A

Thermal and Mechanical Characteristics

Symbol	Characteristic	Min	Typ	Max	Unit
P_D	Total Power Dissipation @ $T_C = 25^\circ\text{C}$			520	W
$R_{\theta JC}$	Junction to Case Thermal Resistance			0.24	$^\circ\text{C/W}$
$R_{\theta CS}$	Case to Sink Thermal Resistance, Flat, Greased Surface		0.11		
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55		150	$^\circ\text{C}$
T_L	Soldering Temperature for 10 Seconds (1.6mm from case)			300	
W_T	Package Weight		0.22		oz
			6.2		g
Torque	Mounting Torque (TO-247 Package), 6-32 or M3 screw			10	in·lbf
				1.1	N·m

Static Characteristics
T_J = 25°C unless otherwise specified
APT37F50B_S

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V _{BR(DSS)}	Drain-Source Breakdown Voltage	V _{GS} = 0V, I _D = 250μA	500			V
ΔV _{BR(DSS)} /ΔT _J	Breakdown Voltage Temperature Coefficient	Reference to 25°C, I _D = 250μA		0.60		V/°C
R _{DS(on)}	Drain-Source On Resistance ^③	V _{GS} = 10V, I _D = 18A		0.13	0.15	Ω
V _{GS(th)}	Gate-Source Threshold Voltage	V _{GS} = V _{DS} , I _D = 1mA	2.5	4	5	V
ΔV _{GS(th)} /ΔT _J	Threshold Voltage Temperature Coefficient			-10		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 500V V _{GS} = 0V			250	μA
		T _J = 25°C T _J = 125°C			1000	
I _{GSS}	Gate-Source Leakage Current	V _{GS} = ±30V			±100	nA

Dynamic Characteristics
T_J = 25°C unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
g _{fs}	Forward Transconductance	V _{DS} = 50V, I _D = 18A		27		S
C _{iss}	Input Capacitance	V _{GS} = 0V, V _{DS} = 25V f = 1MHz		5710		pF
C _{rss}	Reverse Transfer Capacitance			75		
C _{oss}	Output Capacitance			615		
C _{o(cr)} ^④	Effective Output Capacitance, Charge Related	V _{GS} = 0V, V _{DS} = 0V to 333V		355		
C _{o(er)} ^⑤	Effective Output Capacitance, Energy Related			180		
Q _g	Total Gate Charge	V _{GS} = 0 to 10V, I _D = 18A, V _{DS} = 250V		145		nC
Q _{gs}	Gate-Source Charge			32		
Q _{gd}	Gate-Drain Charge			65		
t _{d(on)}	Turn-On Delay Time	Resistive Switching V _{DD} = 333V, I _D = 18A R _G = 4.7Ω ^⑥ , V _{GG} = 15V		25		ns
t _r	Current Rise Time			29		
t _{d(off)}	Turn-Off Delay Time			65		
t _f	Current Fall Time			21		

Source-Drain Diode Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I _S	Continuous Source Current (Body Diode)	MOSFET symbol showing the integral reverse p-n junction diode (body diode)			37	A
I _{SM}	Pulsed Source Current (Body Diode) ^①				115	
V _{SD}	Diode Forward Voltage	I _{SD} = 18A, T _J = 25°C, V _{GS} = 0V			1.2	V
t _{rr}	Reverse Recovery Time	I _{SD} = 18A ^③ di _{SD} /dt = 100A/μs V _{DD} = 100V	T _J = 25°C		250	ns
			T _J = 125°C		450	
Q _{rr}	Reverse Recovery Charge		T _J = 25°C	0.88		μC
			T _J = 125°C	2.18		
I _{rrm}	Reverse Recovery Current		T _J = 25°C	8.4		A
			T _J = 125°C	11.8		
dv/dt	Peak Recovery dv/dt	I _{SD} ≤ 18A, di/dt ≤ 1000A/μs, V _{DD} = 333V, T _J = 125°C			20	V/ns

① Repetitive Rating: Pulse width and case temperature limited by maximum junction temperature.

② Starting at T_J = 25°C, L = 4.81mH, R_G = 25Ω, I_{AS} = 18A.

③ Pulse test: Pulse Width < 380μs, duty cycle < 2%.

④ C_{o(cr)} is defined as a fixed capacitance with the same stored charge as C_{oss} with V_{DS} = 67% of V_{(BR)DSS}.

⑤ C_{o(er)} is defined as a fixed capacitance with the same stored energy as C_{oss} with V_{DS} = 67% of V_{(BR)DSS}. To calculate C_{o(er)} for any value of V_{DS} less than V_{(BR)DSS}, use this equation: C_{o(er)} = -1.33E-7/V_{DS}² + 3.06E-8/V_{DS} + 8.83E-11.

⑥ R_G is external gate resistance, not including internal gate resistance or gate driver impedance. (MIC4452)

Microsemi reserves the right to change, without notice, the specifications and information contained herein.

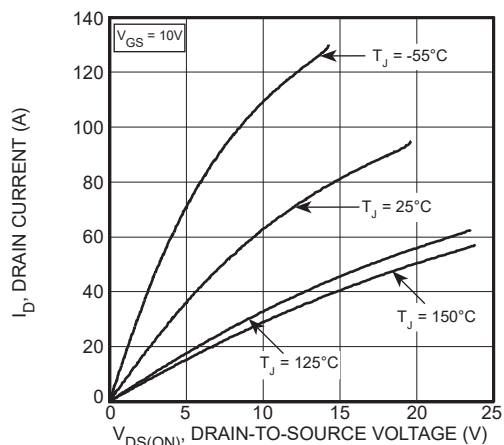


Figure 1, Output Characteristics

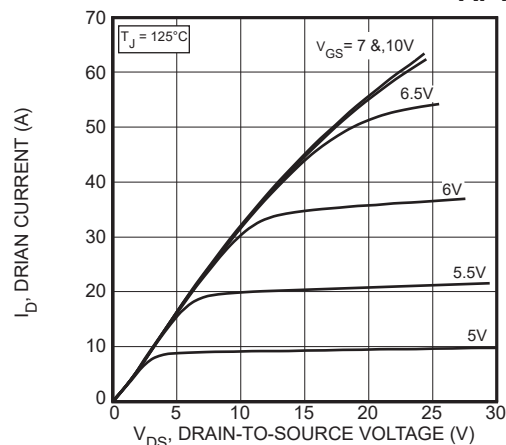


Figure 2, Output Characteristics

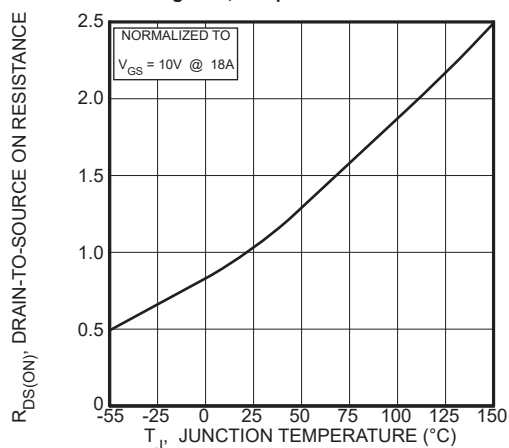
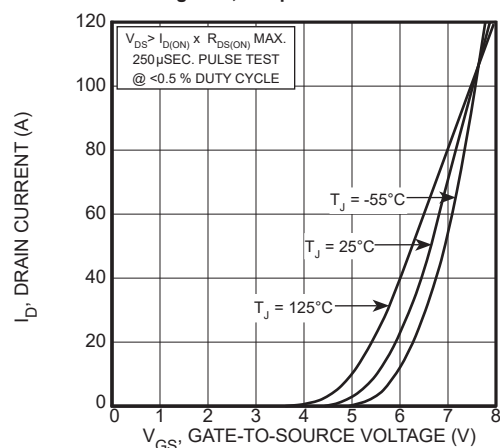
Figure 3, $R_{DS(ON)}$ vs Junction Temperature

Figure 4, Transfer Characteristics

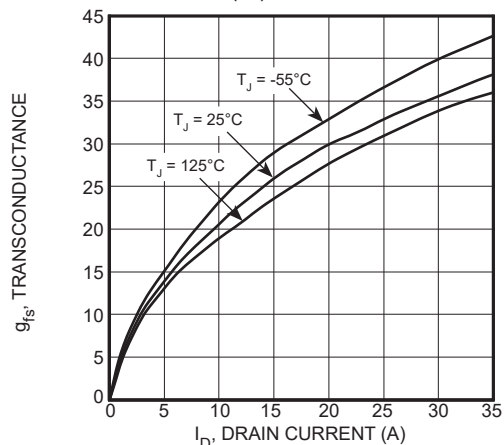


Figure 5, Gain vs Drain Current

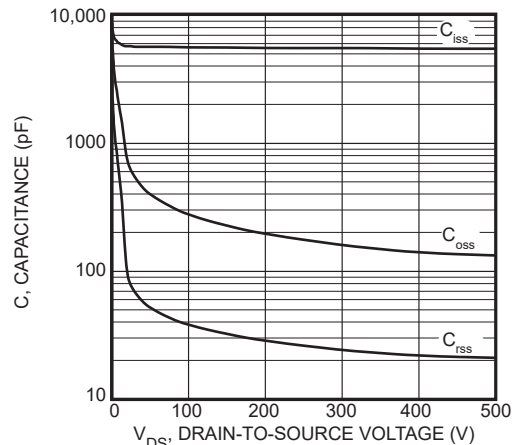


Figure 6, Capacitance vs Drain-to-Source Voltage

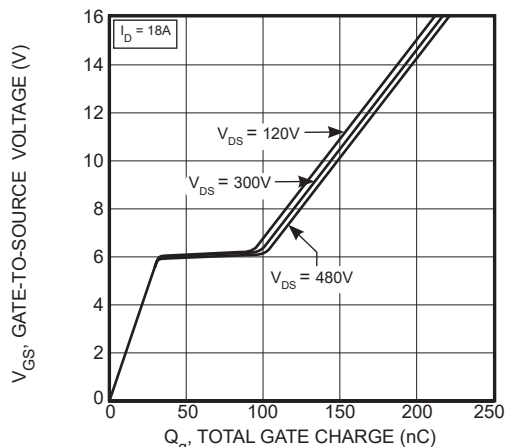


Figure 7, Gate Charge vs Gate-to-Source Voltage

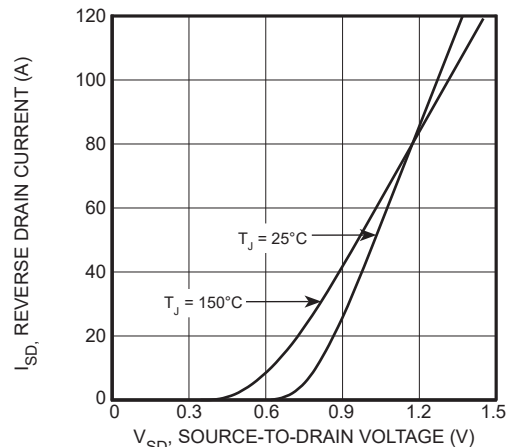
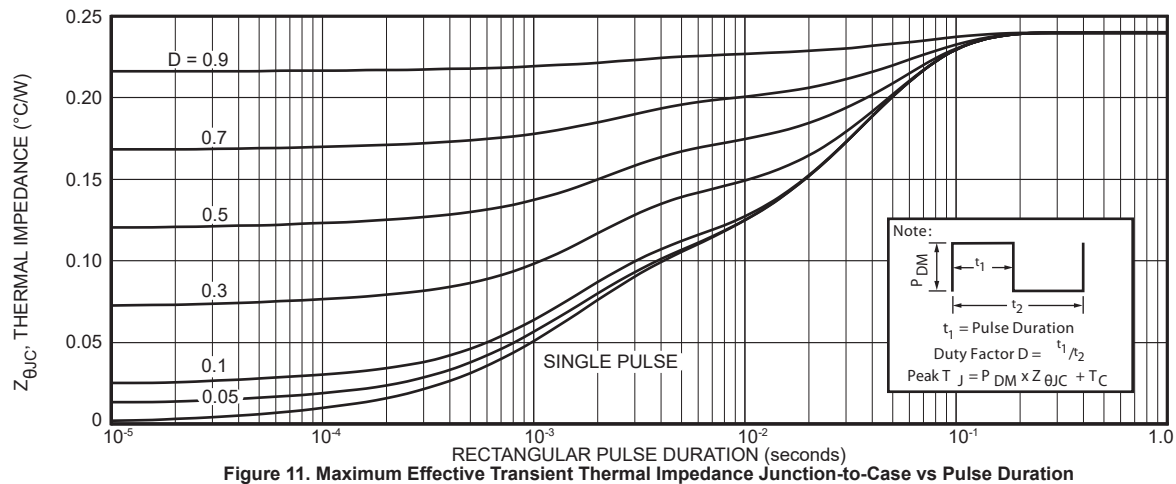
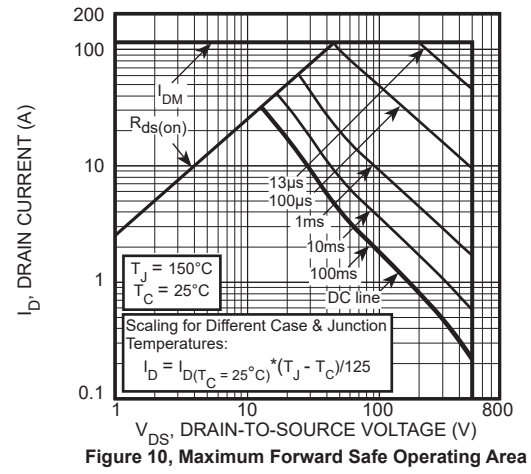
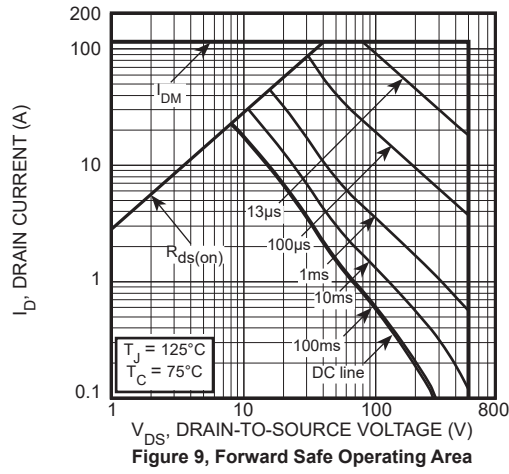
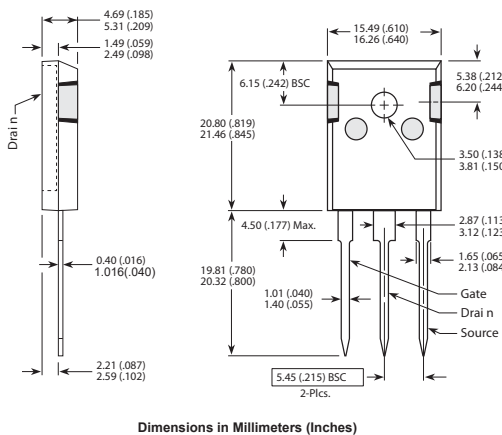


Figure 8, Reverse Drain Current vs Source-to-Drain Voltage



TO-247 (B) Package Outline

(e1) SAC: Tin, Silver, Copper



D³PAK Package Outline

(e3) 100% Sn Plated

