

Introduction

The EV17F91A evaluation board supports the MEC1653B, a highly configurable embedded keyboard controller that accommodates a broad range of peripheral functions. The device provides a wide range of security features and includes support for Post Quantum Computing (PQC). The board is primarily intended for use with the Intel Meteor Lake Reference Validation Platform (RVP). The EV17F91A board serves as a platform for the development of BIOS, drivers, firmware and related software. This evaluation board can be also used as a standalone embedded controller development board for embedded and industrial computing applications. This document outlines the features of the EV17F91A evaluation board and provides setup procedures for comprehensive system development, application validation, or standalone operation for application development. The board is equipped with an Intel-specified 240-Pin Expansion Connector and MS Windows keyboard connectors, enabling direct connection to the Intel Meteor Lake RVP via the expansion connector.

To enhance flexibility, the board includes a JTAG header for programming the MEC1653B, a QSPI Socket that allows users to select their preferred QSPI memory, and configurable resistor options to enable various MEC1653B features and interface them with the 240-Pin Expansion Connector.

Figure 1. EV17F91A Evaluation Board

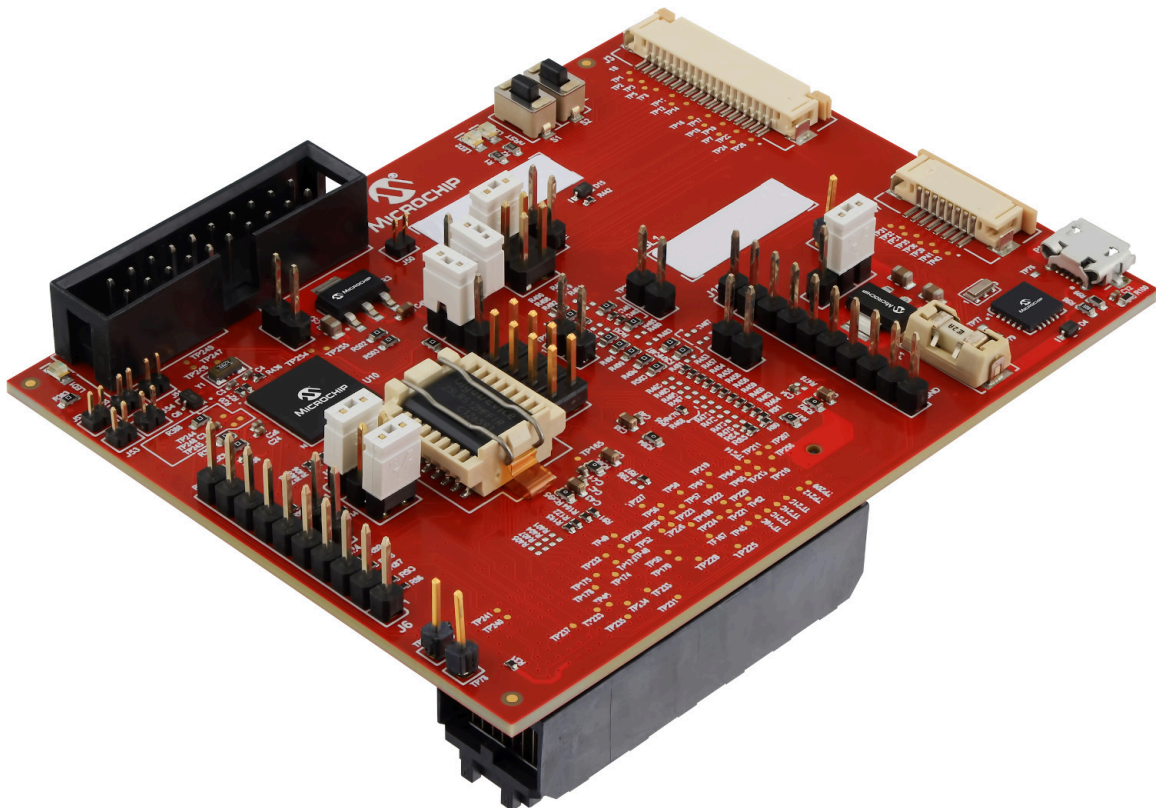


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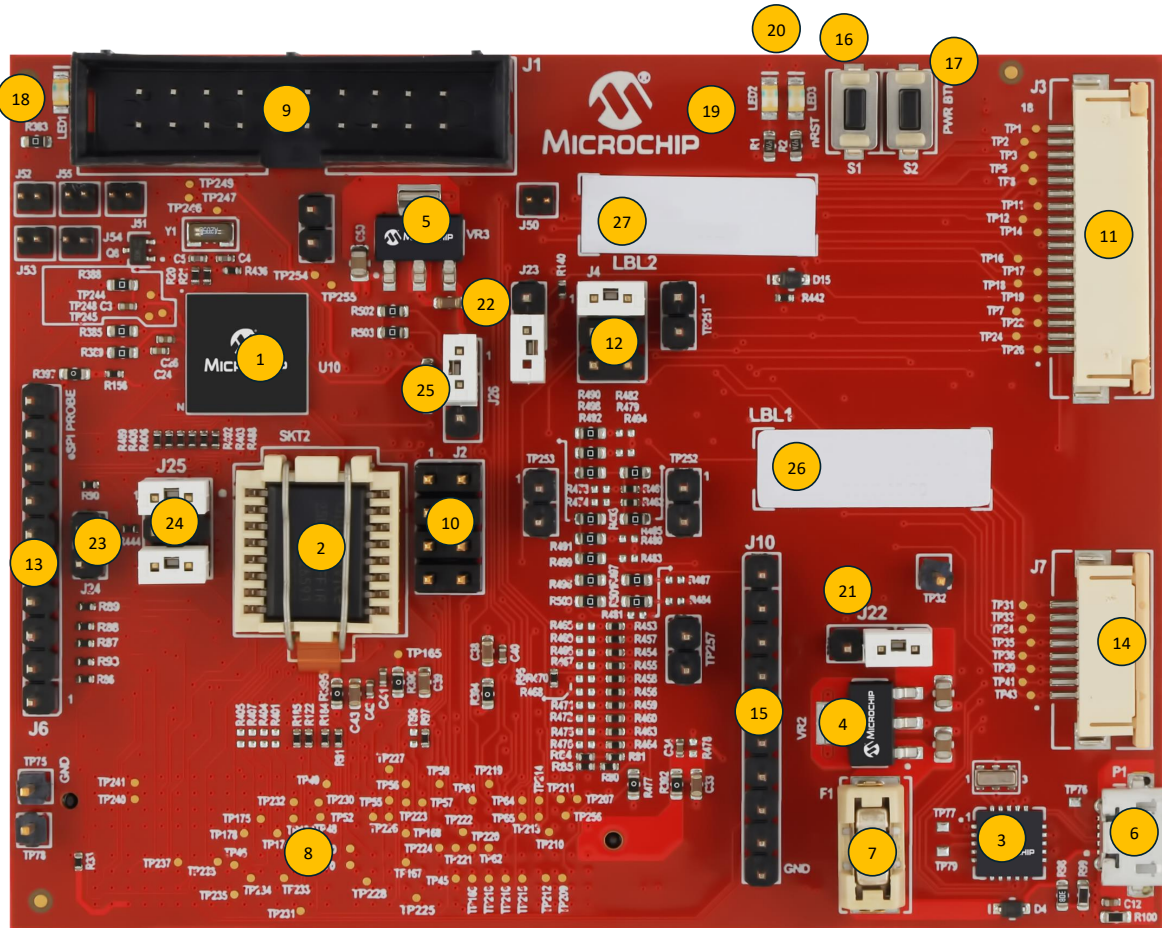
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1. Evaluation Board Hardware

1.1. Features

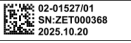
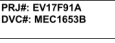
The following diagram highlights the features of the EV17F91A evaluation board.

Figure 1-1. EV17F91A Evaluation Board



- | | | |
|--|---------------------------------------|---|
| 1. MEC1653B Device | 10. J2 Dediprog SF100 Header | 19. LED2 - Connected to GPIO153 |
| 2. 512 Mb QSPI Memory Socket and Device | 11. J3 - 18-Pin KSI Keyboard Header | 20. LED3 - Connected to GPIO157 |
| 3. MCP2200 USB-to-UART Interface | 12. J4 - Software Developer Interface | 21. J22 - Power Source Selection ⁽¹⁾ |
| 4. VR2 3.3V LDO | 13. J6 - ESPI Probe Header | 22. J23 - Crisis Recovery Strap ⁽¹⁾ |
| 5. VR3 1.8V LDO | 14. J7 - 8-Pin KSO Keyboard Header | 23. J24 - BSS Strap ⁽¹⁾ |
| 6. Micro USB Connector | 15. J10 - Power Sequence Header | 24. J25 - Configuration Jumper ⁽¹⁾ |
| 7. Board Fuse | 16. S1 - Reset Switch | 25. J26 - VTR2 Power Select ⁽¹⁾ |
| 8. P2 240-Pin Connector (Backside Mounted) | 17. S2 - Power Button Switch | 26. LBL1 - Serial Number Label ⁽²⁾ |
| 9. J1 - JTAG Header | 18. LED1 - EC-CORE Power | 27. LBL2 - Identification Label ⁽³⁾ |

Notes:

1. See [Jumper Settings](#) for possible jumper settings and default values
2. Example format of LBL1 - Serial Number Label: 
3. Format of LBL2 - Identification label: 

1.2. Jumper Settings

The EV17F91A evaluation board provides several jumper settings that allow users to configure features and operational modes as needed.

Table 1-1. EV17F91A Jumper Settings

Jumper #	Description	Jumper Settings
J22	Power Source Selection	1-2 (Default): Board is powered from the USB connector 2-3: Board is powered through the 240-pin connector
J23	Crisis Recovery Strap	Open (Default): Crisis recovery is disabled Closed: Crisis recovery is enabled
J24	BSS Strap	Open (Default): Bootstrap mode is disabled Closed: Bootstrap mode is enabled
J25	6-Pin Configuration	1-2 (Closed, Default): GPIO054 connected to PM_RSMRST 3-4 (Open, Default): GPIO054 connected to EC_SPI_FLASH_CS_L 5-6 (Closed, Default): GPIO055 connected to EC_SPI_FLASH_CS_L
J26	VTR2 - Power Select	1-2 (Default): VTR2 is connected to 1.8V power 2-3: VTR2 is connected to 3.3V power

1.3. Component Description

The EV17F91A development board includes the following integrated circuits:

MEC1653B

Microchip's MEC1653B is a highly configurable, mixed-signal advanced I/O controller designed for desktop and notebook PCs, provided in a 144-pin WFBGA package. The device contains a 32-bit ARM® Cortex-M4F or M4 processor core with closely coupled memory for optimal code execution and data access. This device includes a wide range of security features for authentication, data integrity, data privacy, secure boot, root-of-trust and a NIST-certified true random number generator. It also supports Post Quantum Computing (PQC) algorithms for authentication and secure boot.

MCP2200

Microchip's MCP2200, in a 20-pin UDFN package, converts a USB signal to UART to facilitate communication with the MEC1653B embedded controller. The device communicates through a USB 2.1 interface.

MCP1826S

The development board includes two Microchip MCP1826S low drop-out (LDO) regulators. The MCP1826S/3.3V generates a 3.3V supply from the USB 5.0V input. The MCP1826S/1.8V generates a 1.8V supply from the output of the 3.3V LDO.

GD25LR512MFFIR

The development board includes a socketed Gigadevice GD25LR512MFFIR 512 Mbit QSPI memory device, capable of operating at a 1.8V supply. The socketed interface allows users to select the memory supplier of their choice. The J26 jumper controls the VTR2 power rail, enabling the memory device to operate at either 1.8V or 3.3V.



CAUTION If the memory is switched, it is the user's responsibility to validate the operating voltage of the selected device and set the J26 jumper accordingly.

1.4. Connectors

Connectors and headers on the board are divided between those needed for the Meteor Lake Reference Validation Platform (RVP) connections and those provided by Microchip to program or observe signals on the evaluation board. For a detailed understanding of the connections, please refer to the EV17F91A validation board schematics available on MyMicrochip.

Meteor Lake RVP Connectors

P2 - 240-Pin Expansion Connector: Defined by Intel, this connector serves as the primary interface between the MEC1653B embedded controller and the Intel RVP.

J3 - KSO Keyboard Connector: An 18-pin FFC/FPC connector specified by Intel, used to connect the board to the RVP platform. This interface provides a direct connection between the MEC1653B and the Windows keyboard interface.

J7 - KSI Keyboard Connector: An 8-pin FFC/FPC connector specified by Intel, used to connect the board to the RVP platform. This interface provides a direct connection between the MEC1653B and the Windows keyboard interface.

Additional Connectors

P1 - USB Connector: The micro USB connector supplies power to the board and communicates with the MCP2200 USB-to-UART converter.

J1 - JTAG Connector: The 20-pin JTAG connector provides a configuration and programming interface for the MEC1653B embedded controller. The device can be configured using Microchip's MPLAB® X IDE or IPE.

J2 - SF100 Dediprog Header: The 8-pin SF100 Dediprog header allows users to flash a firmware image into the onboard QSPI memory.

J4 - Software Developer Interface: The 6-pin header can be used to assist in setting up and validating some of the features of the evaluation board.

J6 - eSPI Probe Header: The eSPI probe header enables monitoring and communication between the eSPI interface and the MEC1653B embedded controller.

J10 - Power Sequence Header: The power sequence header allows users to observe the relative timing of signals associated with the board's power ramp-up sequence.

2. Collateral

The following references may be useful in developing applications for the EV17F91A MEC1653B evaluation board.

Kit Information:

- Ordering Code - EV17F91A
- [EV17F91A Kit](#) web page

Device Web Pages:

- [MEC1653B](#) - Embedded controller and keyboard interface for notebook and desktop computers
- [MCP2200](#) - USB to UART protocol converter
- [GD25LR512MF](#) - Gigadevice 512 Mb QSPI memory

Intel Meteor Lake RVP Documentation:

- [Intel Meteor Lake Technical Documentation](#)
- Intel Document #646710 – Meteor Lake P DDR5 SODIMM RVP Schematic Package (Contact Intel for access)

Software Support:

- [MPLAB®X](#) Version 6.20 or higher - Microchip Integrated Design Environment
- MEC165xB/MEC175xB Blinking LEDs Sample Code (available on the [MyMicrochip](#) SDE Portal)
- Intel Zephyr EC Firmware (Contact your MCHP representative for more information)

Hardware Debuggers:

- Microchip [DV164055](#) ICD5 In-Circuit Debugger
- Microchip [PG164150](#) MPLAB® PICKit™ 5 In-Circuit Debugger
- Microchip [AC102015](#) Target Adapter Board
- Keil [ULINK2](#) Debug Adapter

3. Board Programming

The following section provides an overview of programming the various features of the EV17F91A evaluation board. For comprehensive instructions, please refer to the resources available on [MyMicrochip](#) and the [Secure Document Extranet](#) (SDE) for the MEC1653B. Please note that access to these resources requires a Non-Disclosure Agreement (NDA).

MEC1653B SPI Image Generation

Before operating the board for a specific application, an image defining the device and board operation must be generated. This can be accomplished using Microchip's PC-based image generation tool, which is compatible with both Windows x64 and Linux x64 operating systems. The generated customer image can then be programmed into the onboard QSPI memory using the SF100 DediProg programmer.

Note: For initial verification, a predefined image is preloaded on the board that flashes LED2 and LED3.

Programming the On-board QSPI memory

The onboard QSPI memory can be loaded with an image via the J2 DediProg header, which is compatible with the [SF100](#) SPI Nor Flash DediProg programmer. After loading the image, it is recommended to verify that the MEC1653B boots correctly before configuring the device.

Configuring the MEC1653B

The MEC1653B includes a set of One-Time-Programmable (OTP) registers. Microchip's OTP generator tool must be used to define the configuration image. The actual image generated will be based on the customers requirements for configuring the device. Once defined, the registers can be programmed through the J1 JTAG header using Microchip's MPLAB® X Integrated Development Environment (IDE) and one of Microchip's debuggers, such as the ICD5 or the PICKIT™ 5. Alternately, the Keil ULINK2 debug adapter or other supported tools may be used.



The OTP registers cannot be programmed unless a bootable image is already installed on the device. OTP bits can only be set to a "1" value once, and once programmed, the configuration cannot be altered.

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